Critical Release Notice

Publication number: 297-5001-548
Publication release: Standard 12.02

The content of this customer NTP supports the SN06 (DMS) and ISN06 (TDM) software releases.

Bookmarks used in this NTP highlight the changes between the baseline NTP and the current release. The bookmarks provided are color-coded to identify release-specific content changes. NTP volumes that do not contain bookmarks indicate that the baseline NTP remains unchanged and is valid for the current release.

Bookmark Color Legend

Black: Applies to new or modified content for the baseline NTP that is valid through the current release.

Red: Applies to new or modified content for NA017/ISN04 (TDM) that is valid through the current release.

Blue: Applies to new or modified content for NA018 (SN05 DMS)/ISN05 (TDM) that is valid through the current release.

Green: Applies to new or modified content for SN06 (DMS)/ISN06 (TDM) that is valid through the current release.

Attention!
Adobe® Acrobat® Reader™ 5.0 is required to view bookmarks in color.

Publication History

March 2004

Standard release 12.02 for software release SN06 (DMS) and ISN06 (TDM).

Card NT9X30AB is Manufacture Discontinued and is replaced by new card NT9X30AC.

297-5001-548

DMS-100 Family

DMS SuperNode and DMS SuperNode SE Computing Module

CM Maintenance Guide

BASE14 Standard 12.01 March 3, 2000

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DMS-100 Family

DMS SuperNode and DMS SuperNode SE Computing Module

CM Maintenance Guide

Publication number: 297-5001-548
Product release: BASE14
Document release: Standard 12.01
Date: March 3, 2000

Publication history

March 2000

BASE14 Standard 12.01

- updated MMINFO in "User interface and commands" chapter

August 1999

BASE13 Standard 11.01

- add MTCTST to "Preventative maintenance strategies" chapter
- add MTCTST to "Trouble isolation tools" chapter

April 1999

BASE10 Standard 10.03

- editing changes requested by NTJI.

June 1998

BASE10 Standard 10.02

- editing changes

February 1998

BASE10 Standard 10.01

For feature SR7066, added information on the following cards:

- NT9X10DA processor card (Chapters 1, 2, and 6)
- NT9X14FA memory card (Chapters 1, 5, and 8)
- NT9X26GA RT1F card (Chapters 6)

November 1997

BASE09 Standard 09.02

- editing changes

August 1997

BASE09 Standard 09.01

- revisions to Chapters 5 and 9 for feature CM0902

May 1997

BASE08 Standard 08.02

- technical edit changes to Chapter 8

March 1997

BASE08 Standard 08.01

- revisions associated with the following features:
  - — CM0801 (Chapter 3, "Logs")
  - — SR0075 (Chapter 1, "Overview"; Chapter 2 "Preventive maintenance"; Chapter 5, "User interface"; and Chapter 6, "Cards and paddle boards")
- addition of StrAlc alarm triggers to Chapter 8 ("Troubleshooting charts")
- revision of MemLim alarm trigger points in Chapter 8
- addition of detailed descriptions of the LowMem, StrAlc, LOWSpr, LowSpr, MemLim, SLMLIM, and SLMLim alarms

November 1996

BASE07 Standard 07.03

- changes associated with PRS CM60296

September 1996

BASE07 Standard 07.02

- editing and verification changes to chapter 5
- addition of missing command parameter information to chapter 5

August 1996

BASE07 Standard 07.01

- revisions associated with the new CM RExFlt alarm

  — revisions associated with the critical REx test disable feature

November 1995

CSP05 Standard 06.01

- added new chapter "Mismatch analysis”
- added feature information to the "Overview" chapter
- added feature information to the "Preventive maintenance strategies" chapter
- added feature information to the "Logs" chapter
- added feature information to the "User interface and commands″ chapter
- added feature information to the "Cards and paddle boards″ chapter
- reference to BCSMON changed to DMSMON in the "Trouble isolation tools" chapter
- added feature information to the "Troubleshooting charts" chapter
- added "Troubleshooting an StrAlc alarm" section to the "Advanced troubleshooting procedures" chapter
- deleted "Responding to mismatch logs" section in "Advanced troubleshooting procedures" chapter

August 1995

CSP04 Standard 05.02

Added "Responding to a CMTrap alarm procedure" to "Advanced troubleshooting procedures" chapter

May 1995

CSP04 Standard 05.01

- added feature information to the "Overview″ chapter
- added feature information to the "Preventive maintenance strategies″ chapter

- added feature information to the "Logs" chapter
- added feature information to the "User interface and commands″ chapter
- added feature information to the "Cards and paddle boards" chapter
- added feature information to the "Trouble isolation tools" chapter
- added feature information to the "Troubleshooting charts" chapter
- added feature information to the "Advanced troubleshooting procedures" chapter

January 1995

CSP03 Preliminary 04.01

- added feature information to the "Preventive maintenance strategies″ chapter
- added feature information to the "Logs" chapter
- added feature information to the "Troubleshooting charts" chapter
- added feature information to the "Advanced troubleshooting procedures" chapter

April 1994

CSP02 Preliminary 03.01

CSP02 is a temporary identification that identifies a preliminary release of post-BCS36 NTPs.

- added feature information to the "Logs" chapter

December 1993

BCS36 Standard 02.02

- incorporated editor and technical review changes

September 1993

BCS36 Preliminary 02.01

Added the following chapters:

- "Trouble isolation tools”
- "Troubleshooting charts”
- "Advanced troubleshooting procedures"

Added information to the chapters that remain based on design review and feature updates.

March 1993

BCS35 Preliminary 01.01 first release of document

Contents

About this document

This document helps maintenance personnel locate and clear faults in the computing module. This document applies to the DMS SuperNode and the DMS SuperNode SE switches.

How to check the version and issue of this document

This document uses numbers (like 01.01) to indicate the version and issue of the document.

The first two digits indicate the version. The version number increases with each update that support a new software release. For example, the first release of a document is 01.01. In the *next* software release cycle, the first release of the same document is 02.01.

The second two digits indicate the issue. The issue number increases with each revision when the document is released again in the *same* software release cycle. For example, the second release of a document in the same software release cycle is 01.02.

Determine which version of this document applies to the software you have and determine the order of this document. Refer to the release information in *Product Documentation Directory*.

References in this document

This document refers to the following documents:

- *Switch Performance Monitoring System Application Guide*, 297-1001-330
- *DMS-100 Family Commands Reference Manual*, 297-1001-822
- *DMS SuperNode and SuperNode SE Message Switch Maintenance Guide*, 297-5001-549
- *Alarm and Performance Monitoring Procedures*
- *Card Replacement Procedures*
- *Log Report Reference Manual*
- *Operational Measurements Reference Manual*

- *Routine Maintenance Procedures*
- *Trouble Locating and Clearing Procedures*

1 Overview

This chapter provides an overview of the DMS SuperNode (SN) and DMS SuperNode SE (SNSE) switches and the architecture of the computing module (CM).

This chapter consists of the following sections:

Section , "DMS SuperNode and SuperNode SE system architecture" on page 1-1 describes SuperNode and SuperNode SE system architecture.

Section , "DMS SuperNode and SuperNode SE cabinet layouts" on page 1-3 illustrates the SuperNode and SuperNode SE cabinet layouts.

Section , "DMS SuperNode and SuperNode SE computing module architecture" on page 1-5 describes SuperNode and SuperNode SE CM architecture.

Section , "DMS SuperNode and SuperNode SE computing module configuration" on page 1-11 describes SuperNode and SuperNode SE CM configurations.

DMS SuperNode and SuperNode SE system architecture

The SN and SNSE systems, in Figure 1-1, "SuperNode system architecture" on page 1-2 and Figure 1-2, "SuperNode SE system architecture" on page 1-3, share the following components:

- DMS-core
- DMS-bus
- DMS-link

The DMS-core provides data storage and computing resources. The DMS-core contains a duplexed CM and two system load modules (SLM).

The DMS-bus processes and distributes messages to nodes in the SuperNode and SNSE switches. The DMS-bus contains two message switches (MS) that share loads.

The DMS-link allows the DMS-core and DMS-bus to communicate with each other. The DMS also allows the DMS-core and the DMS-bus to communicate with other nodes in the SN and SNSE switches.

The user can configure the SNSE with a 16K enhanced network (ENET) and CCS7 link interface units (LIU7). The 16K ENET provides voice and data signal switching for nodes in the SNSE switch. The 16K ENET also provides message routes to the MS. The LIU7 provides CCS7 message processing.

Figure 1-1 SuperNode system architecture

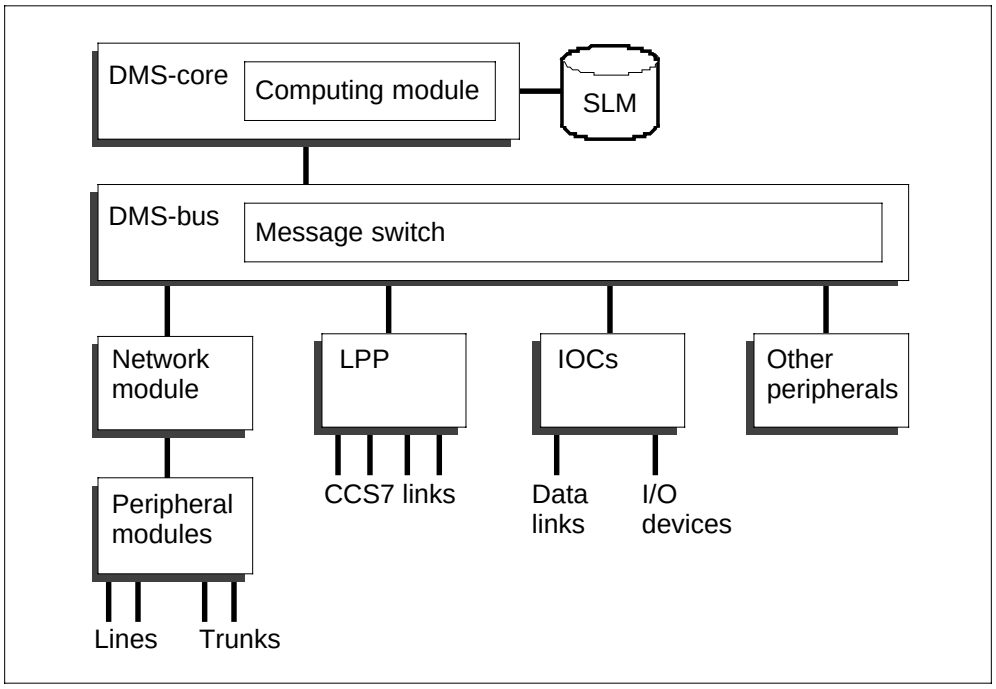
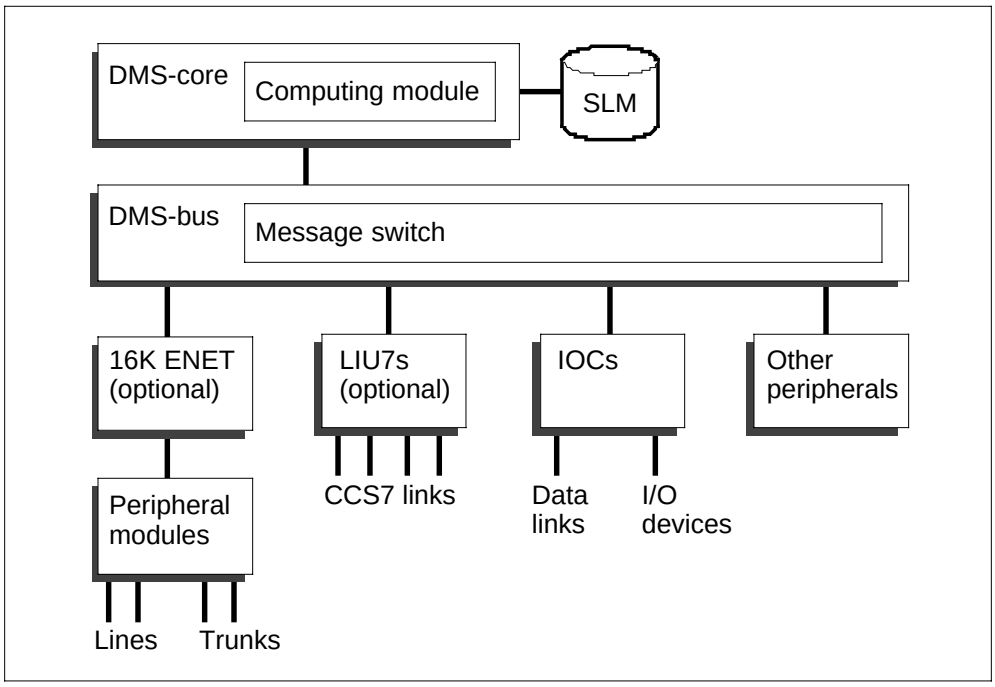


Figure 1-2 SuperNode SE system architecture



DMS SuperNode and SuperNode SE cabinet layouts

In a SN cabinet, the CM does not share a shelf. In a SNSE cabinet, the CM shares a shelf with the SLMs. The SN cabinet is called the dual plane combined core (DPCC) cabinet. The SNSE cabinet is called the SN combined core (SCC) cabinet. Figure 1-3, "SuperNode DPCC cabinet layout" on page 1-4 and Figure 1-4, "SuperNode SE SCC cabinet layout" on page 1-5 show SN and SNSE cabinet layouts.

Figure 1-3 SuperNode DPCC cabinet layout

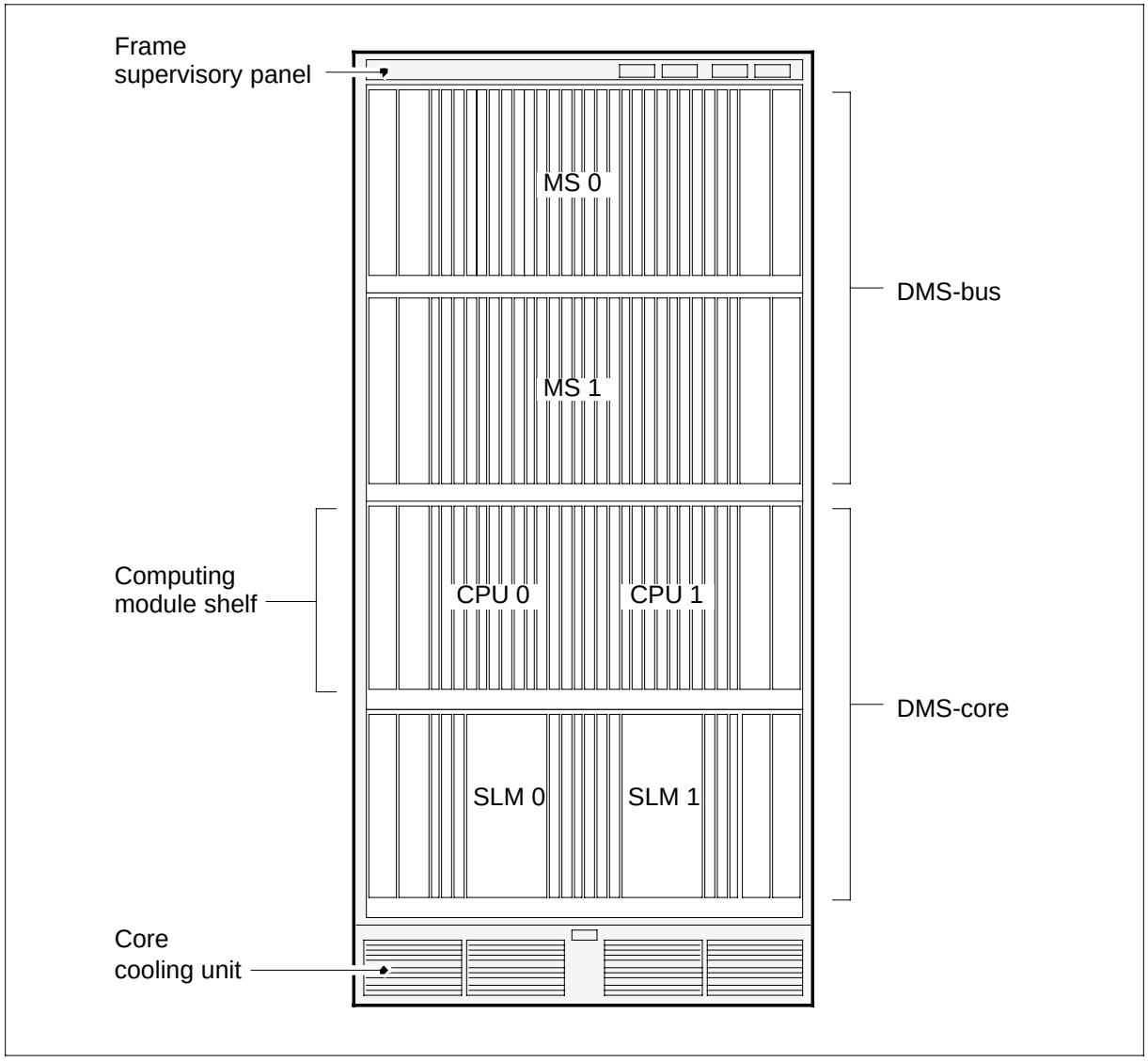
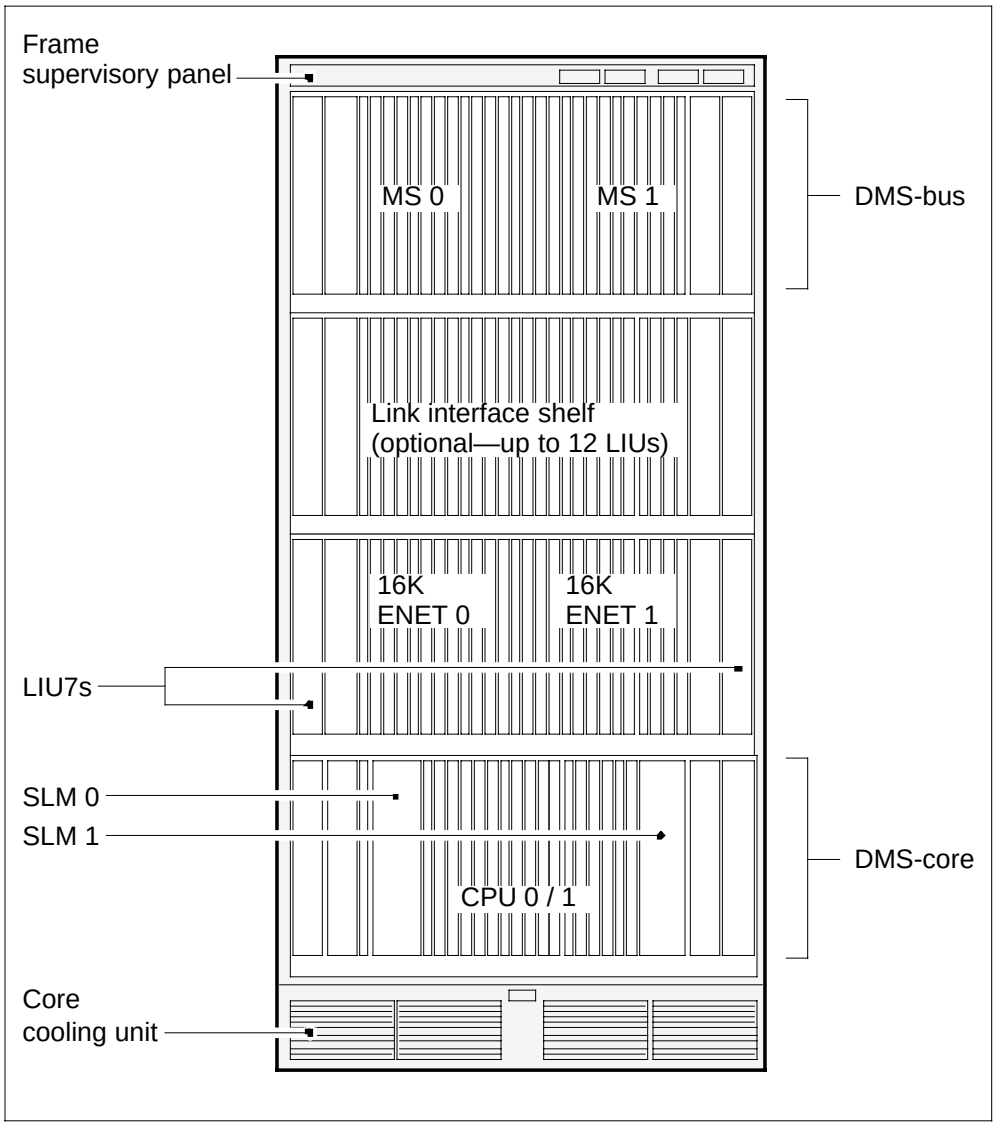


Figure 1-4 SuperNode SE SCC cabinet layout



DMS SuperNode and SuperNode SE computing module architecture

The CM architecture is the same in the SN and SNSE switches. The CM contains the following subsystems:

- processor and memory
- interfaces
- reset control
- bus termination
- bus extension

- subsystem clock
- power supply

For redundancy, the CM contains two identical planes. Each plane can carry the full processing load. During normal synchronized operation, one plane is active and controls call processing activity. The system updates the inactive plane with the active plane. The inactive plane can control call processing activity if a problem occurs on the active plane.

Processor and memory

The processor and memory system consists of CPU cards (NT9X10 or NT9X13) and memory cards (NT9X14). The processor and memory system controls call processing and configuration and maintenance of the other systems.

The NT9X10 and NT9X13 CPU cards house microprocessor circuits and a limited amount of memory for program store. The NT9X14 memory cards provide additional memory for data store.

Burst mode provides fast memory access. When burst mode is active, each fetch operation reads four words of data. Fetch operations normally read one word.

The SN switch uses the following CPU card and memory card groups:

- NT9X13BB and NT9X14DB
- NT9X13BC and NT9X14BB
- NT9X13BC and NT9X14DB
- NT9X13GA and NT9X14BB
- NT9X13GA and NT9X14DB
- NT9X13HB and NT9X14BB
- NT9X13HB and NT9X14DB
- NT9X10AA and NT9X14DB
- NT9X10AA and NT9X14EA
- NT9X10BA and NT9X14EA
- NT9X10CA and NT9X14EA
- NT9X10DA and NT9X14FA

The SNSE switch uses the following CPU card and memory card groups:

- NT9X13MA and NT9X14DB
- NT9X13MB and NT9X14EA

- NT9X13MB and NT9X14DB
- NT9X10AA and NT9X14EA
- NT9X10BA and NT9X14EA
- NT9X10BA and NT9X14EA
- NT9X10CA and NT9X14EA
- NT9X10DA and NT9X14FA

Modes of operation

The SN and SNSE switches use two processors with matched synchronization. These processors are designed for duplex operation. When the switch operates normally, the processors are synchronized. The synchronization provides protection from faults.

The processors can run out of synchronization or in split mode (split) for different maintenance operations. A description of these three modes of operation follows.

In sync

Both CPUs perform call processing when the CM runs in synchronisation. The memory contents of the two planes are the same. The active CPU has write control over all message controller (MC) ports. The inactive CPU can read from all MC ports, but does not have write access.

If a hardware fault causes the two CPUs to be out of synchronization, matcher circuitry on the processor cards flag a mismatch. The mismatch handler must determine which side is sane (fault free). The mismatch handler makes sure the CPU that does not have faults is active. The mismatch handler also makes sure that synchronization drops.

Out of sync

When the CM runs while out of synchronization, the system isolates the inactive CPU from call processing activity. The active CPU initiates firmware processes on the CPU that is not active. The active CPU performs this action to test the hardware on the plane that is not active.

The system uses out of synchronization mode to perform maintenance on the inactive plane. The maintenance system can initiate this mode when the system detects a fault. Maintenance personnel can also begin the mode manually.

Split

When the CM runs in split mode, both CPUs run on their own. The CPUs use one or two the links to communicate to each other. For call processing, one CPU operates as active and does all call processing.

The system uses split mode while software is upgraded. When a switch is split, the operating company personnel can load software to the inactive plane. The data tables on the active plane can copy on to the inactive plane over the split links. When the process is complete, personnel can perform a controlled switch of activity to activate the CPU that is not active.

Interfaces

In-band communication between the CM and the MSs occurs through port cards, interface paddle boards and DS512 fiber optic cables. The SN uses two NT9X12 single-port cards and two NT9X20 DS 512 paddle boards on each CM plane. One card and paddle board pair connects to each MS. The SNSE uses one NT9X86 dual-port card and one NT9X62 interface paddle board on each CM plane.

Communication between each CM plane and the corresponding SLM occurs with one NT9X12 single-port card and one NT9X46 interface paddle board. For SN, the card and paddle board are in the SLM shelf. The bus extension connects the card and paddle to the CM plane. For SNSE, the card and paddle board reside within the CM part of the CM/SLM shelf.

Port cards and paddle boards group into functional blocks. The peripheral module controller (PMC) is the name for the logical grouping of ports that communicate with the SLMs and the bus extenders.

The message controller is the name for the logical grouping of ports on each CM plane that communicates with both MSs. The complete messaging path between the CM and MSs consists of the following components:

- MCs (one on each CM plane)
- computing module interface cards (CMIC) (two on each MS)
- DS512 cables (CMIC links)

Figure 1-5, "SuperNode CM-to-MS port connection diagram" on page 1-9 and Figure 1-6, "SuperNode SE CM-to-MS port connection diagram" on page 1-10 show the port connections for SuperNode and SuperNode SE CM-to-MS communication.

Figure 1-5 SuperNode CM-to-MS port connection diagram

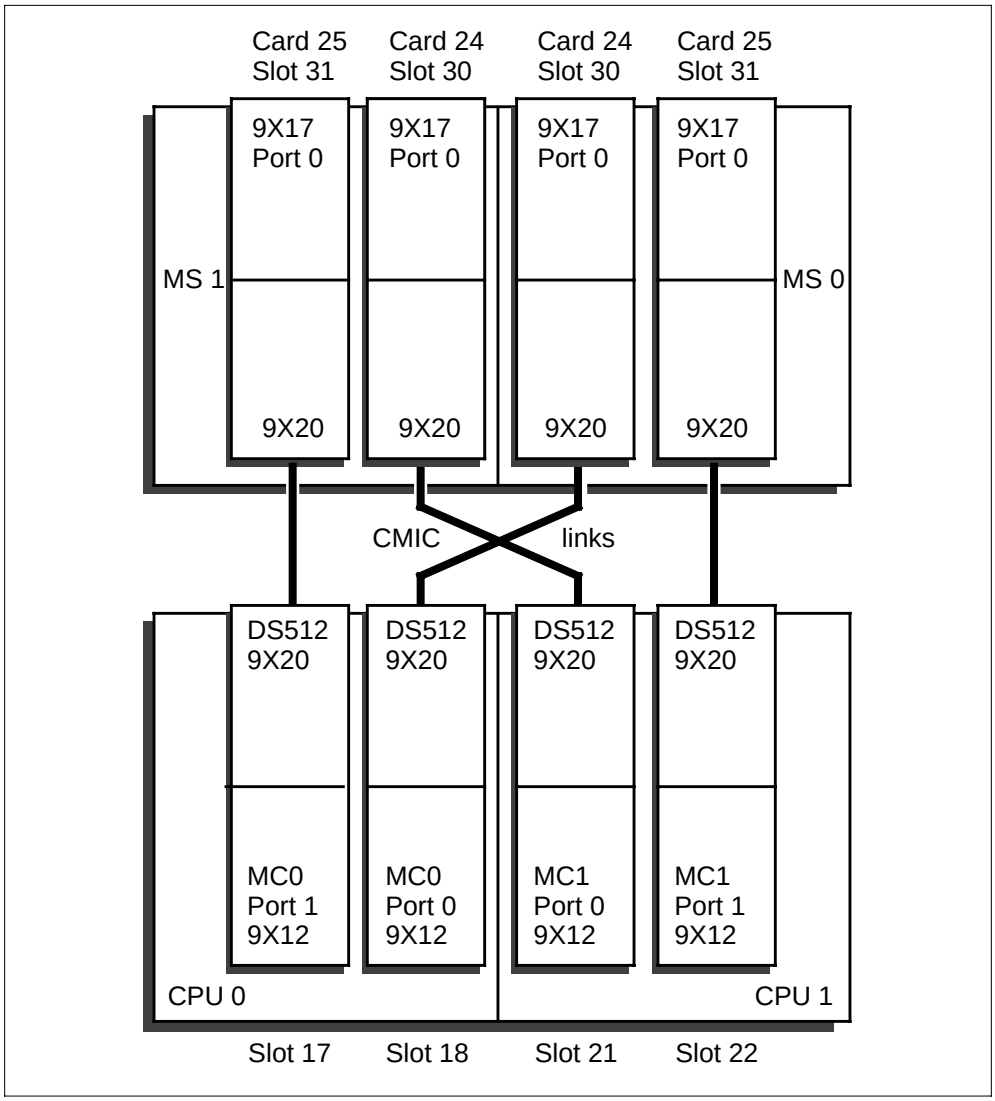
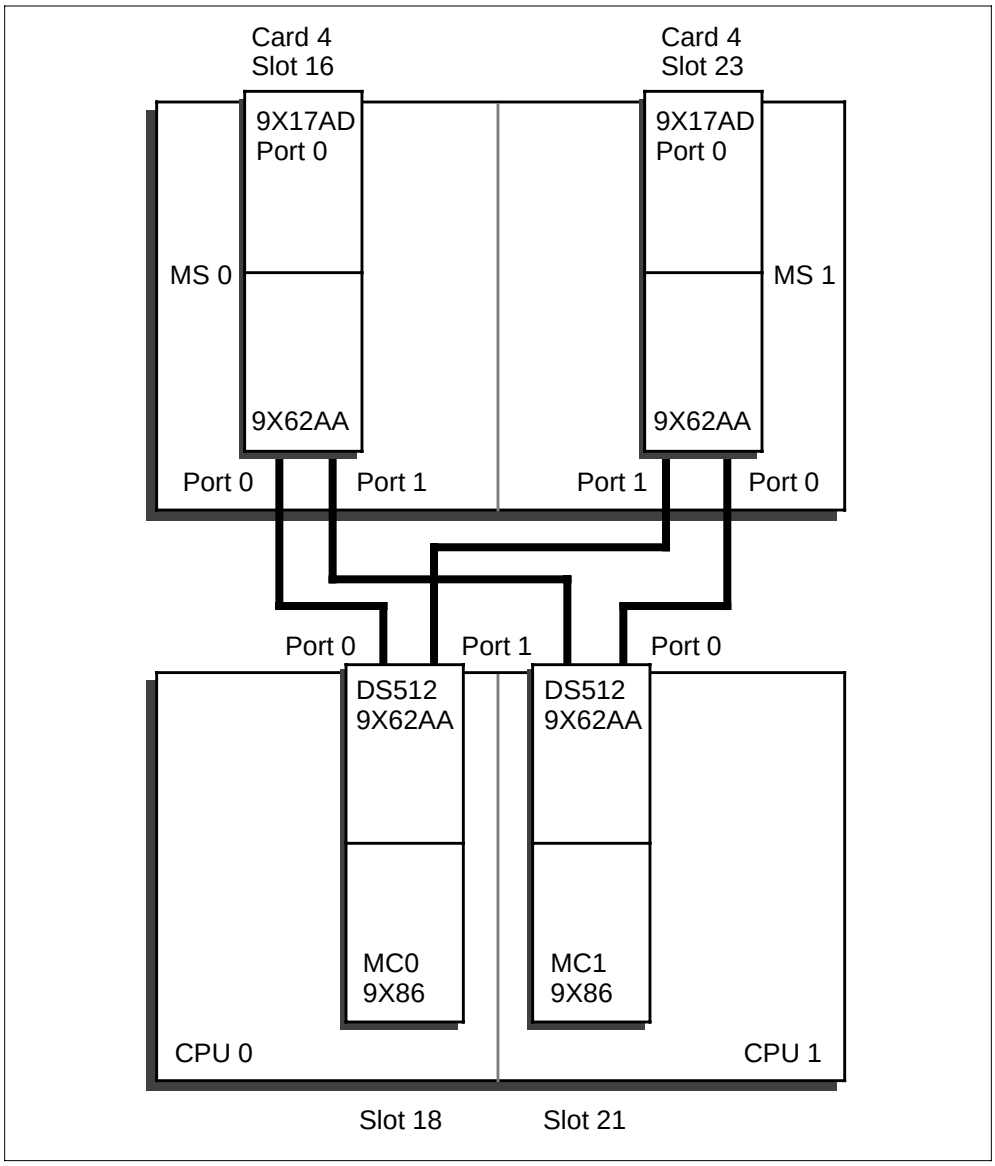


Figure 1-6 SuperNode SE CM-to-MS port connection diagram



Reset control

Processor state information appears on the reset terminal. The reset terminal provides a utility for local and remote resetting of the CM. The NT9X26 RTIF paddle board has two interface ports. One port connects to the local reset terminal and the other port connects to an optional remote reset terminal.

When the subsystem functions normally, the reset system is in a monitoring mode. A CPU can require initialization to a known state for maintenance, bootloading or error recovery. If this event occurs the reset system initiates the reset sequence to initialize the processor.

Bus termination

The NT9X21 paddle board provides resistive termination for the A32 system bus in the CM.

Bus extension

The NT9X27 CM bus extension paddle board links the CM and the SLM shelf.

Subsystem clock

Each SN CM plane contains a subsystem clock (SSC) paddle board (NT9X22) that provides link synchronization with the MS. The SNSE subsystem clock circuits are integrated on the NT9X62 interface paddle board. The office clock in the MS determines SSC accuracy for the SN and SNSE subsystem clock circuits.

Time-of-day (TOD) clocking circuits are on the SuperNode NT9X12 port cards and on the SuperNode SE NT9X86 dual port cards. The office clock in the MS determines TOD accuracy.

Power supply

The power supply provides power for the CM processor shelf. The SN power supply has two +5V dc power converters (NT9X30) and two -5V dc power converters (NT9X31). On SNSE, two 5V dc power converters (NTDX15) power the CM part of the shelf.

DMS SuperNode and SuperNode SE computing module configuration

Figure 1-7, "Example of a Series 20 to 40 SuperNode computing module shelf layout" on page 1-12 and Figure 1-8, "Example of a Series 20 to 40 SuperNode SE CM/SLM shelf layout" on page 1-13 show example Series 20 to 60 SN and SNSE CM shelf layouts.

Figure 1-9, "Example of a Series 50 to 70 SuperNode CM/SLM shelf layout" on page 1-14 and Figure 1-10, "Example of a Series 50 to 70 SuperNode SE CM/SLM shelf layout" on page 1-15 show example Series 70 SN and SNSE CM shelf layouts.

Figure 1-7 Example of a Series 20 to 40 SuperNode computing module shelf layout

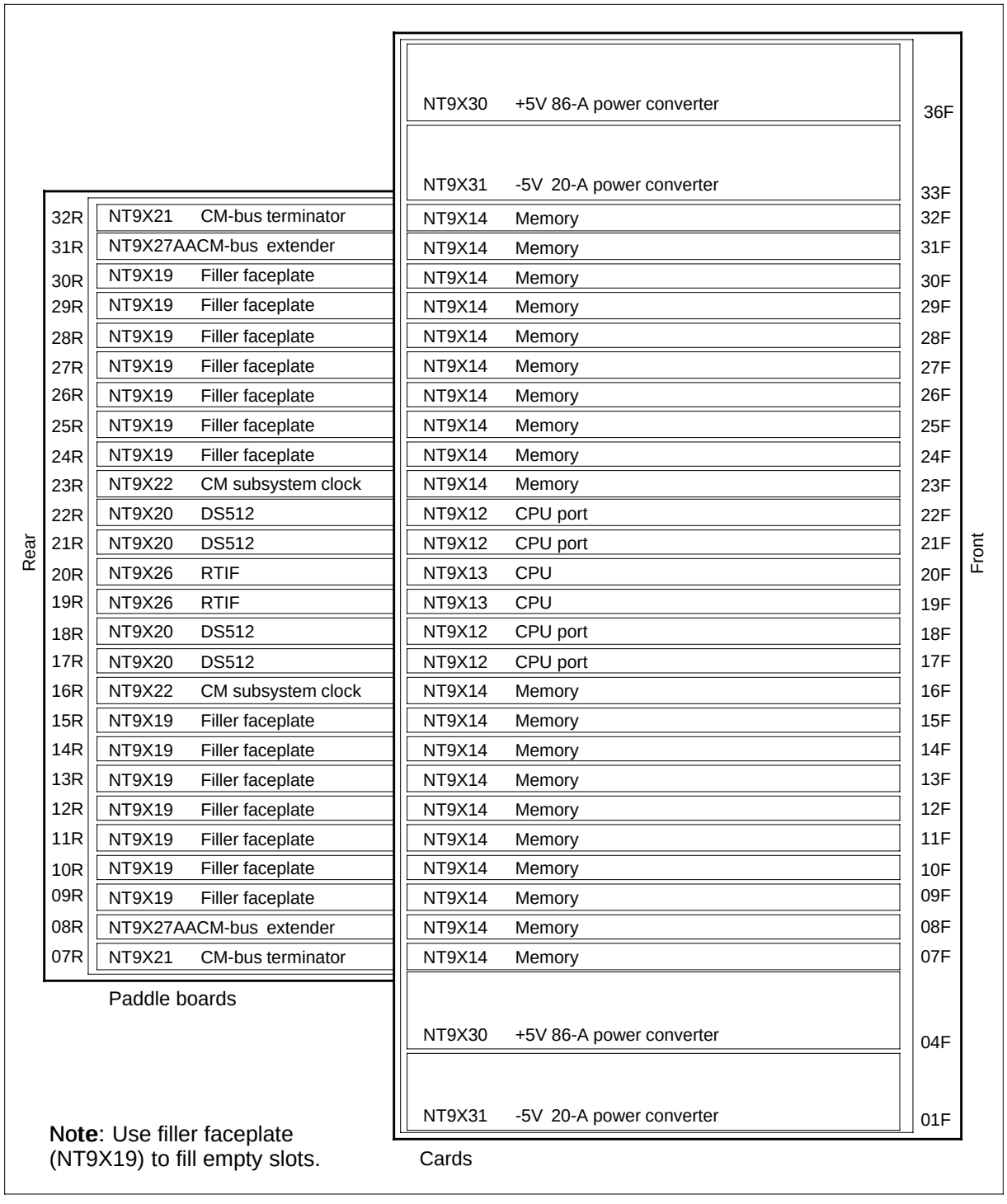


Figure 1-8 Example of a Series 20 to 40 SuperNode SE CM/SLM shelf layout

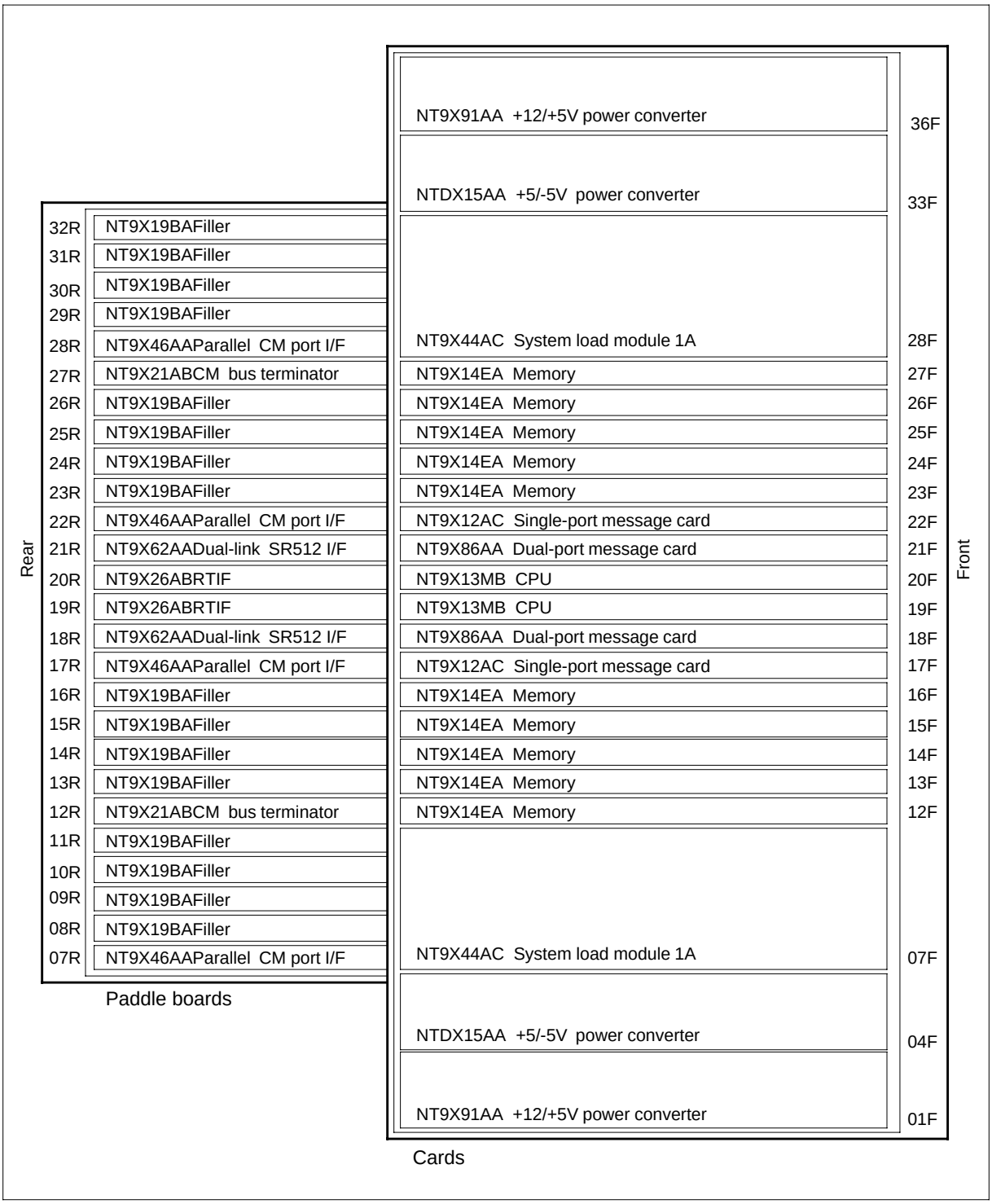
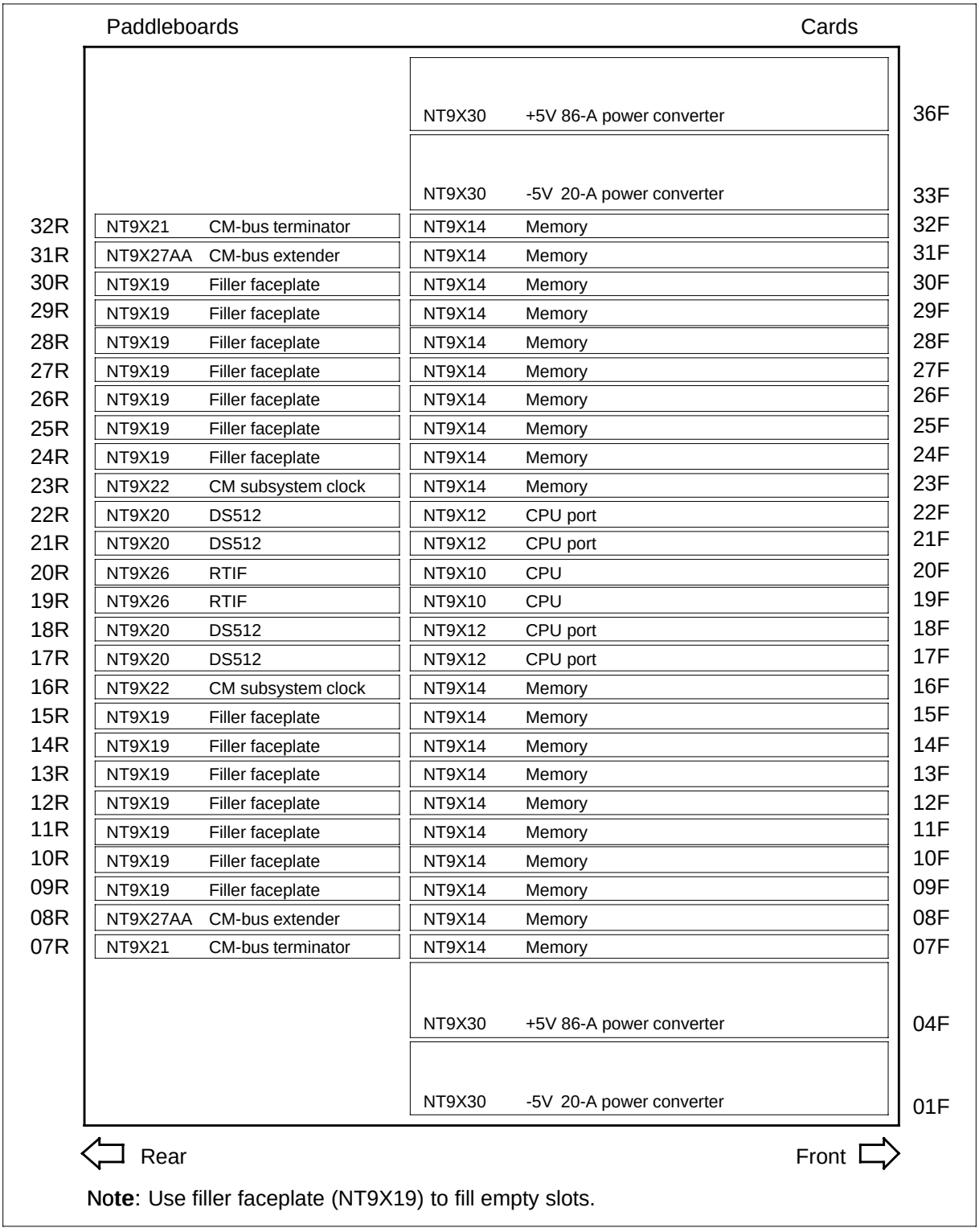
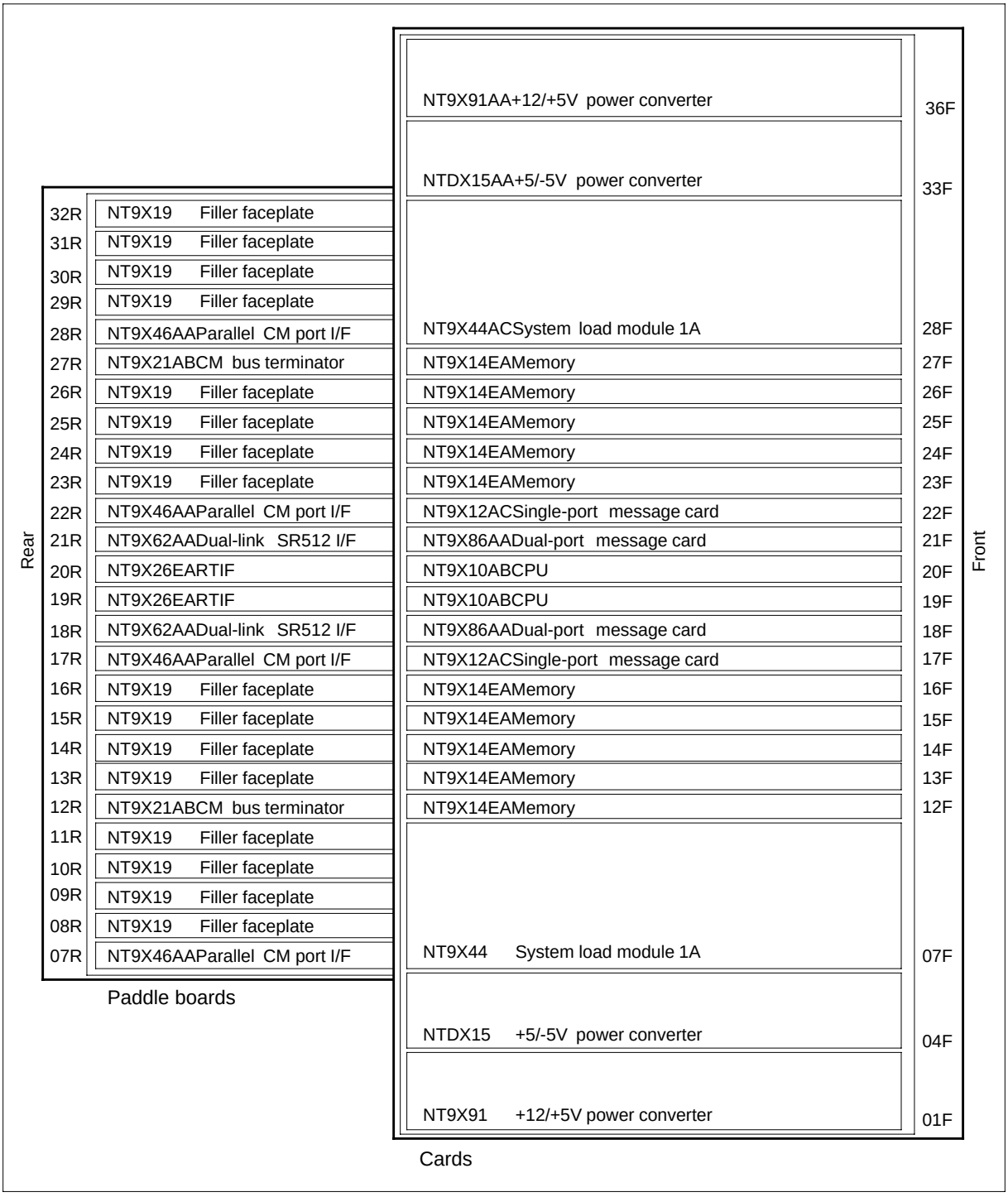


Figure 1-9 Example of a Series 50 to 70 SuperNode CM/SLM shelf layout



Note: Use filler faceplate (NT9X19) to fill empty slots.

Figure 1-10 Example of a Series 50 to 70 SuperNode SE CM/SLM shelf layout



2 Preventive maintenance strategies

This chapter lists the preventive routine maintenance procedures that operating company personnel must perform. This chapter describes the automatic maintenance activities that the DMS SuperNode (SN) and the DMS SuperNode SE (SNSE) computing module (CM) perform.

This chapter consists of the sections that follow:

Routine maintenance procedures

Operating company personnel perform routine procedures according to a schedule. Routine procedures keep the hardware and software of the switch fault-free. Some of the following procedures do not directly relate to the CM. These procedures do affect switch operations.

The CM preventive procedures contain the following:

- cleaning system load module (SLM) tape drive heads
- verifying and adjust the time-of-day (TOD) clock
- testing wrist-strap grounding cords
- replacing cooling unit filters
- testing power converter voltages.

  For instructions on how to perform these procedures, see *Routine Maintenance Procedures*.

Automatic maintenance

The primary source for error detection in the CM is the mismatch handler. The CM also runs software audits and routine exercise (REx) tests to detect faults.

Mismatch handler

The mismatch handler for Series 20 to 60 SN is a software program that can determine which call pickup (CPU) is at fault. Differences in operation can occur between the two planes of the CM.

The mate exchange bus (MEB) monitors data that the CPUs send and receive. When the data that the CPUs send and receive does not match, both CPUs raise a mismatch interrupt. When a mismatch occurs, the mismatch handler tests each CPU and determines the correct CPU.

The following events occur during a mismatch:

- system drops synchronization
- system queries the hardware for faults
- system synchronizes CPUs again
- system copies data for in-synchronization analysis
- system runs matcher test to make sure that the CM remains synchronized
- system analyzes hardware fault indication register (FIR)
- system analyzes memory
- system analyzes address hold register (AHR)
- system compares microprocessor status registers
- system compares microprocessor address and data registers

The process terminates when the system finds a fault. The mismatch logs contain the information from the queries and analysis. Progress markers and error messages in the log reports indicate where the fault is in the sequence. The mismatch handler can end the analysis cycle before the handler isolates a fault. When the mismatch handler cannot isolate the fault, the analysis result indicates that a transient fault caused the mismatch.

For Series 70 SuperNode, the mismatch handler performs the mismatch analysis and diagnostics in duplex is not in synchronization mode. In this mode, both CPUs perform mismatch handling when coupled to the mate CPU. This coupling involves handling and data exchange between the CPUs and controlled activity switching, to allow diagnostics to proceed safely. With this out-of-synchronization approach, both CPUs are ready to take activity. Both CPUs can proceed with the normal operation if the other side fails to meet.

The SR70 mismatch handler handles faults by priority. The handler does not handle faults in the order they are found.

Software audits

Software audits are the scheduled programs that the CPU runs to monitor the state of CM.

Computing module duplex audit

The CM duplex audit runs every 5 s to determine the status of the CM. The audit updates the user interface when the status changes. The audit resets the mismatch thresholds each hour.

The audit determines the state of the CPU and the E2A links, and the jam status. To determine these states, the audit queries the processor card or reads the correct reset terminal interface (RTIF) register. The audit compares the current status with the status determined the last time the audit ran. When necessary, the audit updates the user interface information.

When a Switch of Activity (SWACT) occurs, the system records a footprint entry. The system transfers system logs and footprint buffers, if the system failed to complete the transfer after the last restart or no-restart SWACT.

Subsystem clock/time-of-day clock audit

The subsystem audits the subsystem clocks (SSC) once each minute. The subsystem audits the TOD clocks in 2 min intervals to make sure the clocks function normally.

Computing module link audit

A link audit tests the computing module interface card (CMIC) links each minute to make sure the CMIC links function normally.

Message switch link audit

The message switch (MS) requests that the CM test the CMIC links in 5 min intervals to make sure CMIC links function normally.

Routine exercise tests

The CM routine exercise (REX) tests are preventive maintenance procedures that identify latent hardware failures. REX tests allow the correction of the faults before an outage or performance degradation occurs. The system schedules CM REX tests for automatic execution. Operating company personnel can request manual CM REX tests at the CM level of the MAP. When the system performs a REX test, a REX test indication appears under the CM header of the MTC level MAP display.

Note: Perform a manual maintenance test (MTCTST) to detect faults on new hardware installations or hardware that may have faults. For more

information about MTCTST, refer to Chapter 7, "Trouble isolation tools" on page -1 in this document.

Base CM REX test

The base CM REX test includes the following test activities:

1. pre-REX stability check
2. pre-REX inventory check
3. CM image test
4. Switch of activity (SWACT)

Full CM REX test

The full CM REX test includes the following test activities:

1. pre-REX stability check
2. pre-REX inventory check
3. CM image test
4. out-of-synchronization tests that are not destructive
5. out-of-synchronization destructive tests
6. in-synchronization tests that are not destructive
7. SWACT
8. in-synchronization tests that are not destructive
9. out-of-synchronization destructive tests
10. 0out-of-synchronization tests that are not destructive.

The scheduled REX tests generated by the system run each night at the default time of 1:30 a.m. On Wednesdays, the system runs the full REX test. On all other days of the week, the system runs the base REX test. The user can modify this schedule through datafill. Refer to procedure "Changing CM REX intensity" in *Routine Maintenance Procedures*.

Before the system begins an REX test, the system checks the dedicated stability threshold counters. These counters monitor static random access memory (SRAM) parity fault counts. If these counters record a large number of SRAM parity faults in a period before the test request, the system responds as follows:

- If operating company personnel generate the REX test request manually, a warning and confirmation prompt appear on the MAP. These prompts

indicate that the REX test is not advised. Personnel can choose to abort or execute the test.

- When the REX test is scheduled for automatic execution, the system aborts the test and generates an alarm and a log. The alarm and log indicate the reason that the test did not proceed.

The stability of the system is monitored during execution of REX tests. If a mismatch, trap, link closure, or restart occur during a REX test, the system aborts the remainder of the test. The system resets the CM to a known state.

REX test results reporting

When the system performs a CM REX test, the system produces a CM179 log that indicates if the test passes or fails. If the test fails, the system raises a CM Flt major alarm. The CM179 log indicates the reason for the test failure, the class of the failed test and a list of suspect hardware.

If REX test generated by the system cannot complete because of switch conditions, the system produces a failure reason message. The following conditions prevent the completion of the system REX test:

- The mate is jammed inactive. A complete REX test includes a switch of activity between the active processors and the processors that are not active. A jam condition prevents a SWACT.
- The mate CPU is under test. Another maintenance activity is in process, and the REX test cannot interfere.
- The CPUs are not synchronized. A complete REX test includes dropping of synchronization and synchronizing again. To perform this action, the CPUs must synchronize at the beginning.
- System resources are not available. The system cannot allocate enough resources to run the REX test. The REX tests must run at low traffic periods.

To clear the alarm when a CM REX test fails, run the test again on the failed CPU.

If the REX test cannot start because of error conditions that exceed preset thresholds, a REXSch alarm appears. The alarm appears under the CM header of the MTC level MAP display. The alarm clears when the syestem completes a manual REX. For the instructions to clear this alarm, refer to Chapter 10, "Advanced troubleshooting procedures" on page -1. Refer also to *Alarm and Performance Monitoring Procedures*.

CPU class REX tests

The following table lists the tests in the CPU class REX test for the MC68000 NT9X13 family of processors.

Table 2-1 CPU class REX tests (NT9X13 processors)

Test name	Description
inact_mau_rex	Executes firmware self-test on the inactive CPU for the memory access unit (MAU). This test checks MAU address decodes, parity detection, access protection mask bits, range error detection, latching of all error status bits, and latching of appropriate FIR bits on an error.
inact_clock_rex	Makes sure the circuit of the inactive CPU can detect clock failures.
inact_rtif_rex	Exercises the remote terminal interface (RTIF) diagnostics of the inactive CPU.
inact_reset_rex	Checks the ability of the inactive CPU to handle manual and mate resets.
inact_interrupt_rex	Checks the ability of the inactive CPU to handle different types of interrupts. This test does not check level 1 interrupts. The link class of REX tests checks level 1 interrupts.
inact_access_prot_rex	Makes sure the access protection RAM of the inactive CPU can contain access protection mapping.
inact_os_timer_rex	Tests the operating system timer circuit on the inactive CPU.
inact_address_hold_rex	Makes sure the address hold register can latch an address. The test runs in firmware.
inact_interrupt_mask_rex	Makes sure all bits of the interrupt mask register can be set.
inact_data_cache_rex	Tests the data cache memory and control of the inactive CPU. This test includes a: • march over cache RAM • a check of cache parity and parity RAM • a check for proper cache hit and miss.
inact_mate_fir_rex	Makes sure that all bits on the FIR of the inactive CPU that can be set. Bits remain on the FIR so that the active CPU can determine if its mate FIR can read the latched status.
inact_rom_checksum_rex	Makes sure that the ROM is not corrupt on the inactive CPU.

Table 2-1 CPU class REX tests (NT9X13 processors)

Test name	Description
inact_sanity_rex	Forces the inactive CPU through a complete sanity breakdown. This test does not write to the primary or the super-sanity timer. When the first timer expires, the system generates an interrupt. When the second timer expires, a reset occurs. This test checks these events and the time between these events.
matcher_rex	Makes sure mismatch detection circuits work. The system runs this test under firmware control and when the CPUs are in synchronization.

The following table lists the tests in the CPU class REX test for the MC88100 BRISC NT9X10AA family of processors.

Table 2-2 CPU class REX tests (NT9X10AA BRISC processors)

Test name	Description
inact_clock_rex	Makes sure that the inactive CPU clock circuit can detect clock failures.
inact_rtif_rex	Exercises the RTIF diagnostics of the inactive CPU.
inact_reset_rex	Checks the ability of the inactive CPU to handle manual and mate resets.
mate_fir_rex	Tests that the FIR latches and that the active CPU can read the FIR through the mate FIR.
inact_rom_checksum_rex	Makes sure that the ROM is not corrupt on the inactive CPU.
inact_tic_rex_timer	Tests tracer/interrupt controller (TIC) timing functions.
inact_tic_rex_config	Tests TIC basic functions.
inact_tic_rex_interrupt	Tests the ability of the TIC to generate and mask interrupts.
inact_tic_rex_trace	Tests the tracing functions of the TIC.
inact_mei_parity_rex	Tests the ability of the memory bus (M-bus) Ecore interface (MEI) to detect and latch parity errors.
inact_mei_mem_access_rex	Tests the ability of MEI to detect and latch invalid memory accesses.
inact_mei_rto_rex	Tests the ability of MEI to detect and latch response time-out errors.
inact_pccab_rex	Tests the prefetcher with circular content addressable buffer (PCCAB) functions.

Table 2-2 CPU class REX tests (NT9X10AA BRISC processors)

Test name	Description
inact_sanity_rex	Forces the inactive CPU through a sanity breakdown. This test does not write to the primary or the super-sanity timer. When the first timer expires, the system generates an interrupt. When the second timer expires, a reset occurs. This test checks these events and the time between these events.
matcher_rex	Tests matching on the processor bus (P-Bus) and ECore backplane.

The following table lists the tests in the CPU class REX test for the MC88110 BRISC NT9X10BA, NT9X10CA and NT9X10DA group of processors:

Table 2-3 CPU class REX tests (NT9X10BA/NT9X10CA BRISC processors)

Test name	Description
inact_reset_rex	Checks the ability of the inactive CPU to handle manual and mate resets.
inact_sanity_rex	Forces the inactive CPU through a sanity breakdown. This test does not write to the primary or the super-sanity timer. When the first timer expires, the system generates an interrupt. When the second timer expires, a reset occurs. This test checks these events and the time between these events.
mate_fir_rex	Tests that the FIR latches and that the active CPU can read the FIR through the mate FIR.
matcher_rex	Tests the BRISC Bus matching.
inact_rom_checksum_rex	Makes sure the ROM is not corrupt on the inactive CPU.
inact_rtif_rex	Exercises the RTIF diagnostics of the inactive CPU.
inact_mei_mem_access_rex	Tests the ability of SCIE to detect and latch invalid memory accesses.
inact_mei_rto_rex	Tests the ability of SCIE to detect and latch response time-out errors.
inact_tic_rex_interrupt	Tests the ability of the TMISC to generate and mask interrupts.
inact_pc2_ecc_enabled_rex	Invokes F/W test pccab2_ecc_enabled_RAM test.
inact_pc2_march_dlw_rex	Invokes F/W test pccab2_march_dlw_test.
inact_pll_rex	Invokes F/W out of frequency PLL test.

Table 2-3 CPU class REX tests (NT9X10BA/NT9X10CA BRISC processors)

Test name	Description
inact_lms_march_ecc_enabled_rex	Invokes F/W test lms_march_test_ecc_enabled
inact_tmisc_tracer_rex	Invokes F/W TMISC tracer test.

Memory routine exercise tests

The following table lists the memory class tests:

Table 2-4 Memory class REX tests (all CM processors)

Test name	Description
inact_mem_control_rex	Performs a firmware memory module controller test for each memory module on the inactive CPU.
inact_mem_decode_rex	Programs the mate addressing configuration and checks for double decodes between memory modules.
inact_mem_march_rex	Performs a destructive march test for the memory cards at the rate of one card for each CPU each night.

Link routine exercise tests

The link class REX test checks the operation of the message controller (MC). The MC consists of ports, SSCs and TOD clocks. The MC runs if all links are in-service. The link class tests appear in the following table.

Table 2-5 Link class REX tests (all CPU processors)

Test name	Description
mc_split_mode_rex	Places the CM in split mode. Batch change supplement (BCS) applications require split mode. If the system cannot place the CM in split mode, the test fails.
mc_inservice_test_rex	Performs an in-service test on the MC.
mc_port_test_rex	Takes the MC links that do not have faults out of service one at a time, and performs destructive tests on the MC links. The tests include all hardware and error modes provided.
mc_test_rex	Takes a complete MC out of service and performs a destructive MC test on the MC.
ssc0_rex_general_test	Performs a REX test on the SSC.

Table 2-5 Link class REX tests (all CPU processors)

Test name	Description
ssc1_rex_general_test	Performs a REX test on the SSC.
ssc_id_prom_test_rex	Reads the IDProms of the SSC cards.

Peripheral module controller routine exercise tests

The peripheral module controller (PMC) class REX tests are like the link class tests. The system performs these tests when all links are in service. The PMC class tests appear in the following table.

Table 2-6 PMC class REX tests (all CM processors)

Test name	Description
pmc_port_test_rex	Tests the PMC port and link handler hardware.
pmc_node_test_rex	Tests the PMC with the crossover bus of the PMC.

Base class routine exercise tests

The base class tests appear in the following table.

Table 2-7 Base class REX tests (all CM processors)

Test name	Description
inact_rex_image_test	Tests inactive image to make sure the image can start again. Tests restart capabilities on a rotational basis in a three night cycle: • tests warm restart capabilities on the first night • tests cold restart capability the second nightt • tests reload restart capabilities the third night. The rotation repeats.
cm_rex_check_inventory	Makes sure all product equipment codes (PECs) meet baseline requirements.

Indications of automatic test results

The following indicators inform operating company personnel of the results of automatic maintenance tests:

- alarms
- logs
- operational measurements (OMs).

To detect and resolve minor problems, operating company personnel must monitor these indicators for trends and patterns.

For information on how to clear alarms, refer to Chapter 8, "Troubleshooting charts" on page -1 , and *Alarm and Performance Monitoring Procedures*. For more information about logs, refer to Chapter 3, "Logs" on page -1 , and the *Log Report Reference Manual*. For more information about the OMs, refer to Chapter 4, "Operational measurements" on page -1, and the *Operational Measurements Reference Manual*.

3 Logs

This chapter describes logs that relate to the DMS SuperNode and DMS SuperNode SE computing module (CM).

Logs provide information to monitor the components of the CM. Some logs can isolate a problem to one component. Other logs can indicate problems that cannot be attributed to one component.

DMS SuperNode and SuperNode SE CM-related logs

The following types of logs relate to CMs:

- computing module (CM)
- footprint (FP)
- input/output audit (IOAU)
- mismatch (MM)

Chapter 10, "Advanced troubleshooting procedures" on page -1 provides information used to analyze the root cause of the most difficult logs. For more detailed information on logs, refer to the Log Report Reference Manual.

Computing module logs

The logs report information from the following:

- CPU
- CM cards
- subsystem clocks (SSC)
- imaging
- traps
- routine exercise (REX) tests
- link tests

Table 3-1 lists the SN and SNSE CM logs and triggers.

Table 3-1 SuperNode and SuperNode SE CM logs

Log	Title	Trigger
CM100	SUMM CM REPORT	The system generates this summary report each day at 9:00 a.m. This log provides the status of the CM.
CM101	INFO CM STATUS	A change in the CM synchronized, activity, jam status, or CPU clock source.
CM102	INFO CM STATUS	The system generates this log one time each hour when the CM is out of synchronization.
CM103	TBL HIGH TRAP RATE	The occurrence of many traps. The log specifies the number of traps that occur each minute.
CM104	SYSB MC STATUS CHANGE	A change in state of the message controller indicates system busy (SysB). The log report indicates the reason for the state change.
CM105	CBSY MC STATUS CHANGE	A change in state of the indicated message controller to C-side busy. The log report indicates the reason for the state change.
CM106	MANB MC STATUS CHANGE	A change in state of the indicated message controller to manual busy.
CM107	TBL MC STATUS CHANGE	A change in state of the indicated message controller to in-service trouble. The log report indicates the reason for the state change.
CM108	RTS MC STATUS CHANGE	The return to services (RTS) of the indicated message controller. The log report indicates the reason for the state change.
CM109	TBL MC STATUS CHANGE	The indicated message controller has a time-of-day (TOD) register with a fault, or does not have a TOD set.
CM110	TBL MC STATUS CHANGE	The indicated message controller has an interface to the SSC card that has faults.
CM111	TBL RUNNING OUT OF MEMORY	The amount of memory for the indicated CM is below a set threshold. The log specifies the amount of memory that remains. The system generates this log one time each hour.
CM112	FLT MEM CARD FAULT	A memory test has failed on the indicated memory card and the indicated memory card has a memory location that has faults. The log can also indicate that the number of transient errors on the card exceeds the transient error threshold.

Table 3-1 SuperNode and SuperNode SE CM logs

Log	Title	Trigger
CM113	TBL MEM CARD IN SERVICE	The indicated memory card is in-service trouble because of memory faults. The memory faults can be corrected.
CM114	INFO MEM CARD OK	This log indicates a memory card that passed a memory test after being in the problem or defective state. A CM112 or a CM113 log generates before this log.
CM115	FLT LOSS OF TOD TIME	The TOD clocks do not have a reliable time reference.
CM116	FLT IMAGE TEST FAILED	Image test failure indicates that the load on the inactive CPU is not sane.
CM117	INFO IMAGE TEST PASSED	All image tests pass.
CM118	INFO RMS REQUEST OVERFLOW	A delay in at least one resource management scheme (RMS) request. The system generates this log one time each hour.
CM119	TRAP	Occurrence of trap on the active CPU when the switch is not synchronized, or on the active or inactive CPU when the switch is synchronized. The report includes the following information: • a summary of the trap reason and an indication of which part of the program was operational when the trap occurred • a traceback of the procedures completed before the trap occurred • additional information about the trap reason
CM120	INIT	A system restart occurred. Includes additional information about the type of restart.
CM121	INFO REX PASSED	A REX test passes (application processors only)
CM122	FAIL REX TEST	A REX test fails. The log contains information about the type of test and the possible failure reason (application processors only).
CM123	INFO LOW SPARE MINOR CONDITION	The CM amount of spare memory on one CPU while in synchronization is low.
CM124	INFO CPU PASS	A CPU test passes.
CM125	FAIL CPU TEST	A CPU test fails. The log contains information about the type of test.

Table 3-1 SuperNode and SuperNode SE CM logs

Log	Title	Trigger
CM126	INFO PRIMARY AUTOLOAD	A change in the contents of the autoload register (the primary autoload device changes)
CM127	CM SYNC FAILURE	The attempt to synchronize the CPUs fails.
CM128	INFO MC LINKHIT DATA	The CM port card hardware detects a bus access controller (BAC) or link handler (LH) fault. The log contains information about the type of fault detected by the CM port card.
CM129	INFO TIME-OF-DAY CLOCK	The indicated message controller loses access to the TOD clock register. The log contains the possible cause of the lost access.
CM130	INFO SSC STATUS CHANGE	A change in the state of the SSC. The log contains information about the initial state, the present state, and the reason for the change.
CM131	INVALID AUTOLOAD DEVICE	The system attempts to enter an autoload route and specifies an invalid autoload route.
CM132	MANB PMC-NODE STATUS CHANGE	The indicated P-side message controller changes to manual busy.
CM133	SYSB PMC-NODE STATUS CHANGE	The indicated P-side message controller changes to system busy. The log report indicates the reason for the state change.
CM134	TBL PMC-NODE STATUS CHANGE	The indicated P-side message controller changes to in-service trouble.
CM135	RTS PMC-NODE STATUS CHANGE	The indicated P-side message controller changes to in service.
CM136	MANB PMC-PORT STATUS CHANGE	The indicated P-side message controller port changes to manual busy.
CM137	SYSB PMC-PORT STATUS CHANGE	The indicated P-side message controller port changes to system busy. The log report indicates the reason for the state change.
CM138	RTS PMC-PORT STATUS CHANGE	The indicated P-side message controller port changes to in service.
CM139	INFO PMC HITS SUMMARY	This log indicates the number of hits recorded on the peripheral module controller (PMC) links during the last audit cycle.

Table 3-1 SuperNode and SuperNode SE CM logs

Log	Title	Trigger
CM140	INFO PMC LINK HIT DATA	The PMC hardware detects a BAC or LH fault. The log contains information about the type of fault the PMC detects.
CM141	INFO SPLIT CM MODE FAULT	The system detected a fault when the CM attempted to enter split mode.
CM142	PMC-NODE TEST RESULT	This information log reports the result of a PMC-node test. The log contains information about the result of the test on each port.
CM143	PMC-PORT TEST RESULT	This information log reports the result of a PMC-port test. If test failure occurred, the log provides information about the type of test.
CM144	INFO SSC REFERENCE CHANGE	The status of the frame pulse reference links of an in-service or in-service trouble SSC changes. The log contains information about the previous and current status of the links.
CM145	FAIL SSC TEST FAILURE	The system detects a one or more faults on the indicated SSC. The types of faults that the log specifies include the following: • SSC test failure • SSC paddle board does not respond • interface between message controller and SSC has faults • reference frame pulse lock is not available • SSC paddle board failure • second reference frame pulse failure • reference frame is not available
CM146	RESOURCES FOR THIS CLASS ARE IN USE	A CM REX test cannot run because resources were not available. The log contains information about the class of the REX test.
CM147	XBUS TEST RESULT	Failure of the PMC extension bus test. The log indicates possible failure reason.
CM148	PMC PORT FAULTY	Test failure of the PMC port that the log indicates. The log indicates the type of test.
CM149	PMC SPLIT STATUS	The status of the PMC that the log indicates changes when a loadmate operation occurs. The log contains information about the result of the loadmate.

Table 3-1 SuperNode and SuperNode SE CM logs

Log	Title	Trigger
CM150	INFO CM SYNC COMPLETE	A synchronization attempt is complete. The log contains information about the type of synchrnonization.
CM151	INFO DIRECT LOADMATE RESULT	This information log reports the result of a direct loadmate operation, if the NOWAIT option was specified.
CM152	INFO PERIPHERAL INTERRUPT RECEIVED	The processors received a peripheral interrupt mismatch. Diagnostics were run on the port cards. The log contains information about the results of the tests.
CM153	FAIL TOD TOLERANCE AUDIT	Failure of a TOD tolerance audit.
CM154	REX FAILED SETUP	Conditions in the CM prevented a REX test. The log contains information about the class of tests that cannot run and the reason that the tests cannot run.
CM155	INFO IMAGE TEST INFO	An image test cannot determine the state of the image.
CM156	INFO INVENTORY UPDATE	An update of the card inventory tables.
CM157	INFO INVENTORY ERROR	Detection of a difference between the inventory tables and the cards on the CM or CM/SLM shelf.
CM158	INFO LOW SPARE MAJOR CONDITION	The CM has a low amount of spare memory on both CPU planes when the switch is in synchronization, or on the active plane when the switch is out of synchronization. The log indicates the number of spare memory modules that remain.
CM159	INFO CM STATUS CHANGE	The CM changed from in synchronization to out of synchronization.
CM160	INFO	The CM REX test detected a difference between the card inventory tables and the cards on the CM or CM/SLM shelf.
CM162	FLT PROCESSOR CLOCK FAULT	The system detected a processor clock fault on one of the CPUs. The log contains information about the type of fault.
CM163	FLT E2A LINK FAULT	An E2A link on the specified CPU is not active or is disabled.
CM164	FLT PROCESSOR MEMORY FAULT	The PCCAB memory ECC audit on the inactive CPU (BRISC processor only) detected a processor memory fault or high number of transient errors.

Table 3-1 SuperNode and SuperNode SE CM logs

Log	Title	Trigger
CM165	FLT PROCESSOR OPTION ERROR	The processor and memory card PECs mismatch with the processor optionality information entered.
CM166	SRAM CORRECTION	The system detects a program store parity error during an out-of-sync SRAM snapshot. The system automatically corrected the error.
CM167	SRAM AUDIT STATE CHANGE	The system changed the SRAM audit frequency. The normal interval between audits is 30 s. If a trap threshold is reached, the interval automatically changes to 5 min. If an SRAM snapshot cannot initialize after a restart, the interval changes to 30 min.
CM168	SRAM MINOR ALARM	The system raises a minor alarm because the number of SRAM faults detected in the last 48 h exceeded the threshold.
CM169	SRAM SYNC PREVENTION	The system prevented a synchronization operation because the number of SRAM faults detected in the last 48 h exceeded the threshold.
CM170	SRAM COUNTER CLEARED	Manual action cleared a counter for SRAM or CM REx faults.
CM171	SRAM SYNC OVERRIDE	Operating company personnel selected the SRAM synchronization override option. The system determined that a manual attempt to synchronize the CM is not recommended because one or more SRAM fault counters reached a threshold. The system will display a warning and a yes/no confirmation prompt. If personnel enter the word yes to override the warning, the system attempts the synchronizaton operation without regard for the possible results. The system records the id of the personnel.
CM172	SRAM SWACT OVERRIDE	The SRAM SWAct override option was selected. The system determines that a manual attempt to switch CM activity is not recommended because a threshold is reached in one or more SRAM fault counters. The system displays a warning and a yes/no confirmation prompt. Enter the word yes to override the warning. The system attempts the SWAct operation without any regard for the possible results. The system records the id of the user.

Table 3-1 SuperNode and SuperNode SE CM logs

Log	Title	Trigger
CM173	SRAM REX OVERRIDE	Operating company personnel selected the SRAM REX test override option. The system determined that a manual attempt to perform a REX test is not recommended because one or more SRAM fault counters reached a threshold. The system will display a warning and a yes/no confirmation prompt. If personnel enter the word yes to override the warning, the system attempts to perform the REX test without regard for the possible results. The system records the id of the personnel.
CM174	TBL INVALID MEMORY CONFIGURATION	The CM has an invalid memory configuration on one of the planes.
CM175	TBL APPROACHING/EXCEEDING MEMORY LIMIT CM	Operating system memory approaches or reaches the platform exact memory limit.
CM176	INFO CMMNT ALARM CLEARED	The system generates this information log when a CMMnt level alarm clears
CM177	INFO CMMNT ALARM ENABLED/DISABLED CM	The system generates this information log when a user enables or disables a CMMnt level alarm with the ALARM command.
CM178	TBL APPROACHING SLM LIMIT CM	The dumpable image size approaches a size too large to be dumped to SLM tape or to store in two loads to SLM disk.
CM179	CM REX GENERIC INFO	Provides different details on REX test passes and failures. Provides notification of the disabling of CM REX testing. This log can help personnel debug REX test failures.
CM180	TBL EXCEEDED SLM LIMIT CM	The dumpable image size is greater than the capacity of the SLM tape or the capacity of one half the SLM disk.
CM181	TBL STORE ALLOCATOR LIMIT	The memory allocation reaches or is higher than a defined threshold for a given CPU/SLM combination.
CMSM101	INFO MC LINKHIT SUMMARY	The system generates this information log at 9:05 a.m. each day, after the system generates the CM100 log. Log CMSM101 adds the counts for each link error type according to the link number on which the hit occurred. Counts are set to zero every day after the system generates the log.

Table 3-1 SuperNode and SuperNode SE CM logs

Log	Title	Trigger
CMSM102	INFO PMC LINKHIT DAILY SUMMARY	The system generates this information log at 9:05 a.m. each day The log contains counts of all the link hits that occurred on the PMC links after the system generated the last report.
CMSM103	INFO MC BUFF PARITY DAILY SUMMARY	The system generates this information log at 9:05 a.m. each day. The log contains a summary of the contents of the message controller parity buffer.
CMSM104	INFO PMC BUFF PARITY DAILY SUMMARY	The system generates this information log at 9:05 a.m. each day. The log contains a summary of the contents of the peripheral module controller parity buffer.

Footprint logs

After restarts, the DMS-core generates FP logs for given conditions. The FP logs include the following information:

- a message indicating corruption of FP data
- snapshot data obtained from the active CPU during a restart
- snapshot data obtained from the inactive CPU during a restart
- a message that indicates failure of the initial transfer attempt of the inactive CPU FP data
- a message that indicates failure of the second and last transfer of the inactive CPU FP data

After a restart, the DMS-core generates a log that contains the active CPU snapshot data. If a restart occurs while the CM is out of synchronization, the DMS-core generates an additional log. This additional log indicates if the transfer of the data between the inactive CPU and the active CPU is complete. If the transfer is successful, the log contains snapshot data from the inactive CPU. If the transfer is not successful, the log contains a message. The message indicates the active CPU failed to obtain the inactive CPU data.

If the initial data transfer from the inactive CPU failed, the next manual synchronization attempts a transfer. If this second data transfer is successful, the log contains the inactive CPU snapshot data. If the second data transfer of data is not successful, the log contains a message. The message indicates the active CPU failed a second and last attempt to obtain the inactive CPU data.

If an image test fails during a CM REX test, the system attempts to transfer the footprint buffers of the inactive CPU. The system attempts to transfer the buffers to the active side for debugging purposes.

Table 3-2 lists the SN and SNSE FP logs and triggers.

Table 3-2 SuperNode and SuperNode SE FPlogs

Log	Title	Trigger
FP100	ACTIVE CPU FOOTPRINT SNAPSHOT	The DMS-core collected footprint snapshot data from the active CPU. The system generates the report after each restart completes. The system does not generate the report after restarts caused by power loss.
FP101	INACTIVE CPU FOOTPRINT SNAPSHOT	An out-of-sync restart occured. The active CPU obtained the FP data from the inactive CPU.
FP102	RESTART OUT OF SYNC	An out-of-sync restart occured. The transfer of the inactive CPU FP data to the active CPU did not complete.
FP103	RESTART OUT OF SYNC	The transfer of the inactive CPU FP failed after the completion of a manual transfer.
FP104	RESTART SYNCTXT	An out-of-sync restart occured. The transfer of the inactive CPU footprint data to the active CPU was not successful.

Input/output audit logs

Input/output audit logs provide information related to I/O subsystem audits.

Table 3-3 lists the I/O audit logs and triggers related to the CM.

Table 3-3 SuperNode and SuperNode SE I/O audit logs

Name	Title	Trigger
IOAU112	INFO REX SCHEDULER NOTICE	A change to the system REX (SREX) controller schedule occured. This log reports changes to the CM REX test schedule.

Mismatch logs

A mismatch is an error condition. This error occurs when the two CPUs that operate in synchronization perform different instructions or operate with different data. A hardware fault (duplicated or not duplicated faults) or a software fault can cause a mismatch.

Table 3-4 lists the SN and SNSE MM logs and the events that trigger the logs.

Table 3-4 SuperNode and SuperNode SE MM logs

Name	Title	Trigger
MM100	FLT MISMATCH	A mismatch occured. The software mismatch handler isolated the mismatch fault. The system indicated the mismatch recovery process with the correct recovery action.
MM110	INFO MM RECOVERY	The system completed a successful mismatch recovery. The CM is in synchronization. The system generates MM110 log after the system generates an MM100 log.
MM111	INFO MM RECOVERY	The system completed a successful mismatch recovery The CM remains out of synchronization. The system requires manual tests or replacement of the suspect hardware before the hardware can return to synchronization. The system generates log MM111 after the system generates an MM100 log.
MM112	INFO MM RECOVERY	A mismatch recovery is canceled because of the high rate of mismatch faults. You require manual action to synchronization the CM again. The system generates log MM112 after the system generates an MM100 log.
MM113	INFO MM RECOVERY	Mismatch recovery failure. After this event, the CM remains out of synchronization. The mismatch recovery process cannot perform the recommended recovery action correctly. You require manual action to synchronize the CM again after the replacement of defective hardware components. The system generates log MM113 after the system generates an MM100 log.

Table 3-5 lists the SN and SNSE MFC logs and the events that trigger the logs.

Table 3-5 SuperNode and SuperNode SE MFC logs

Log	Title	Trigger
MFC100	INFO MFC MISMATCH	A memory fault correctable (MFC) mismatch occured. The software mismatch handler isolated the mismatch fault. The system indicated the correct recovery action with the mismatch recovery process.

Table 3-5 SuperNode and SuperNode SE MFC logs

Log	Title	Trigger
MFC110	INFO MFC RECOVERY	The system detected a memory fault correctable (MFC). The system recovered successfully. The CM in synchronization. The system generates log MFC110 after the system generates a MFC100 log.
MFC111	MFC THRESHOLD	This log indicates a high number of MFCs occuring for this card. The card is marked FLT (faulty). Personnel can change the card during the next maintenance shift. The system generates log MFC111 after the system generates an MFC100 log.

4 Operational measurements

This chapter describes operation measurements (OM) that relate to DMS SuperNode (SN) and DMS SuperNode SE (SNSE) computing module (CM).

DMS SuperNode and SuperNode SE CM-related OMs

The OMs provide load and performance information. The OM system controls the collection, display, and generation of OM data for the operating company.

Computing module group

The CM group OM registers provide performance information about the CM. Refer to the *Operational Measurements Reference Manual* for additional information about OMS.

Table 4-1 lists the registers in the CM group and the register peg reason or use description.

Table 4-1 CM group registers

Register name	Peg reason or use description
CMCPUFLT	CPU fault
CMDPSYNC	CM loss of synchronization because of a mismatch interrupt
CMMCINIT	Manual initiation of cold restarts
CMMCSBSY	MC changed to system busy
CMMEMFLT	Memory fault
CMMSMPXU	Amount of time the CM is out of synchronization because of manual action
CMMSWACT	Manual initiation of activity switches
CMMWINIT	Manual initiation of warm restarts
CMRCPUFL	CPU class routine exercise (REX) test failure

Table 4-1 CM group registers

Register name	Peg reason or use description
CMREXFLT	System REX test cancellation
CMRLNKFL	Link class REX test failure
CMRMCFL	MC part of link class REX test failure
CMRMEMFL	MEM class REX test failure
CMRPMCFL	PMC class REX test failure
CMRSMPXU	Amount of time the CM is out of synchronization because of fault detected during REX test
CMRSSCFL	SSC part of link class REX
CMRSWACT	REX test caused activity switch
CMSCINIT	System action caused cold restart
CMSSCFLT	SSC fault
CMSSMPXU	Amount of time the CM is out of synchronization because of system action
CMSSWACT	System action caused activity switches
CMSWINIT	System action caused warm restart
CMTRAP	Hardware-detected fault
CMTRMISM	Transient mismatches
PMCLKBSY	Peripheral module controller port changed to system busy
PMCNDBSY	Peripheral module controller changed to system busy

5 User interface and commands

This chapter provides the following:

- DMS SuperNode (SN) and DMS SuperNode SE (SNSE) computing module (CM) subsystem commands
- examples of maintenance and administration position (MAP) displays
- status field indicators that appear in the MAP displays
- commands used at the reset terminal

This chapter consists of the following sections:

Section , "DMS SuperNode and SuperNode SE CM subsystem commands" on page 5-1 describes nonmenu commands available at the each MAP level of the CM subsystem. Each section includes an example of a MAP terminal display for the associated level. The section includes a table that describes all possible values that can appear in the different fields of the display.

Section , "Reset terminal commands" on page 5-14 describes the commands available at the CM reset terminal.

Section , "Series 50Mx SuperNode and Series 70 SuperNode and SuperNode SE commands" on page 5-20 describes the use of some Series 50Mx and Series 70 SuperNode CM commands for BASE05 and up. The section describes the changes and additions to these commands.

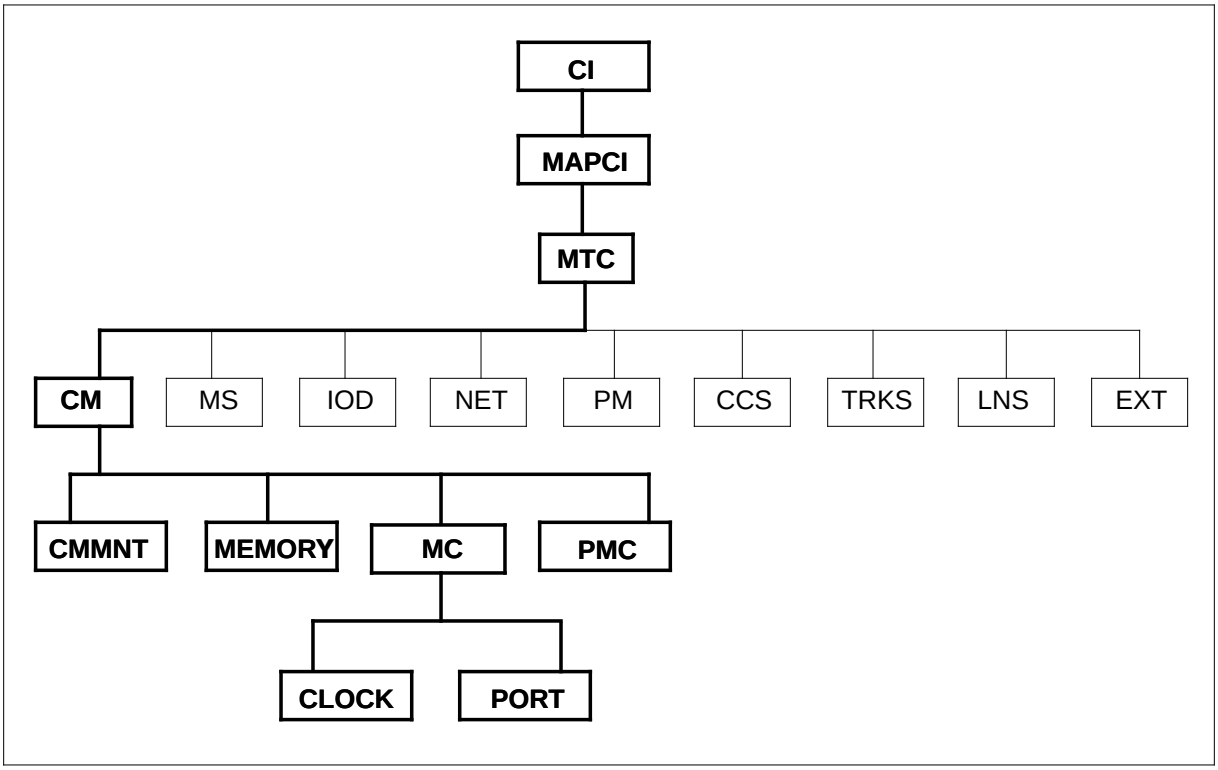
Section , "CM mismatch commands" on page 5-41 describes the Series 20 through 60 commands associated with CM mismatches. The section includes the changes and additions to these commands for BASE06 and up.

DMS SuperNode and SuperNode SE CM subsystem commands

For additional information on CM menu and nonmenu commands, refer to the *DMS Family Commands Reference Manual*.

Figure 5-1, "SuperNode and SuperNode SE CM MAP level hierarchy" on page 5-2 on illustrates the MAP levels of the CM subsystem.

Figure 5-1 SuperNode and SuperNode SE CM MAP level hierarchy



CM level unlisted menu commands

You can perform the following commands from the CM level of the MAP display.

ABTK

This command cancels a process in progress on the inactive CPU of a CPU pair. This command releases the MCR flag and resources so that a new task can be performed on the inactive CPU.

CHECKINV

This command verifies and updates internal inventory tables.

CHECKREL

This command determines if a replacement card is compatible with the switch.

CONFIG

This command performs memory extension upgrades. Memory extension requires inserting additional memory cards on the mate CPU. Memory upgrade requires replacing one or more memory cards with memory cards that have a different product engineering code (PEC).

E2ALINK
This command enables, disables, or checks E2A link status on both CPU planes.

INSYNC
This command verifies CPU synchronization, activity, jam and memory error, and correction status.

QUERYCLK
This command displays the clock source for each CPU in a CPU pair.

QUERYCM
This command displays current hardware configurations for CM and SLM shelves.

QUERYFLG
This command displays the holder of the MCR flag. This command also displays the estimated time before the holder releases the MCR flag.

REXCMINT
This command controls the automatic routine exercise (REX) test schedule.

SRAMCNT
This command accesses the command directory for the static random access memory (SRAM) fault counters. You can access this command from the CM level or directly from the CI level. The following section describes SRAMCNT directory commands.

SRAMCNT commands
Use the SRAMCNT directory to access the following non-menu commands

CLEARCNT
This command clears the specified SRAM fault counter and sets the value to zero.

QUERYCNT
This command queries the value of the specified SRAM fault counter.

QUERYSNP
This command provides detailed SRAM snapshot data. Nortel (Northern Telecom) support personnel use this command for fault analysis.

Figure 5-2 Example of a CM level MAP display

```
CM      MS     IOD     Net      PM     CCS     Lns     Trks    Ext     APPL
 .        .      .       .        .      .       .       .       .       .
CM            CM   Sync  Act  CPU0  CPU1  Jam  Memory  CMMnt  MC  PMC
  0 Quit       0     .   cpu 1   .     .           .       .    .    .
  2 CMMnt

  3 Memory    CM:
  4 MC
  5 PMC
  6 Tst
  7
  8
  9
 10  11
 12 RExTst
 13 SwAct
 14 Sync
 15 DpSync
 16
 17
 18 Locate_
   TEAM26
 Time  10:18  >
```

CM level status field indicators

The following table describes CM level status field indicators.

Table 5-1 CM level status field indicators

Field	Indicator	Description
Sync	.	CM is synchronized.
	No	CM is not synchronized.
	NoOvr	CM is synchronized. No handshake override.
	InStp	CM is synchronizing.
Act	cpu 0	CPU 0 is active.
	cpu 1	CPU 1 is active.
CPU0 **or** CPU1	.	CPU is in service.
	flt	CPU has faults.
	ut	CPU is under test

Table 5-1 CM level status field indicators

Field	Indicator	Description
Jam	(blank)	Inactive CPU is not jammed.
	yes	Inactive CPU is jammed.
Memory	.	Memory is in service.
	ut	Memory is under test.
	flt	Fault detected on at least one memory card.
CMMnt	.	CM maintenance did not detect faults.
	IMAGE	CM maintenance detected a critical image fault.
	cmtrap	CM maintenance detected a cmtrap fault.
	autold	CM maintenance detected an autold fault.
	lowmem	CM maintenance detected a lowmem fault.
	lowspr	CM maintenance detected a minor lowspr fault.
	LOWSpr	CM maintenance detected a major lowspr fault.
	RExSch	CM maintenance detected a rexsch fault.
MC	tbl	Message controller (MC) is in-service trouble.
	.	MC is in service.
	mbsy	MC is manually busy.
PMC	.	Peripheral message controller (PMC) is in service.
	tbl	PMC is in-service trouble.

CMMNT level unlisted menu commands

There are no CMMNT level nonmenu commands.

Figure 5-3 Example of a CMMNT level MAP display

```
CM      MS     IOD     Net      PM     CCS     Lns     Trks    Ext     APPL
.        .      .       .        .      .       .        .      .       .
CMMNT          CM   Sync  Act  CPU0  CPU1  Jam  Memory  CMMnt  MC  PMC
 0 Quit        0     .   cpu 1   .    .           .       .    .    .
 2
 3 AutoLd_     Traps:          Per minute =     0      Total =     0
 4 Image
 5 Alarm_      AutoLdev:       Primary = SLM 0 DISK  Secondary =  SLM 0 DISK
 6
 7             Image Restartable = No image test since last restart
 8
 9             Next image test restart type = WARM
10
11             Last CMREXTST executed
12 RExTst
13 SwAct       System memory in kbytes as of  12:23:39
14 Sync        Memory (kbytes): Used = 122272 Avail =  45664 Total = 167936
15 DpSync      CM:
16             CMMNT:
17
18
  TEAM40
Time  12:53  >
```

CMMNT level status filed indicators

The following table describes CMMNT level status field indicators.

Table 5-2 CMMNT level status field indicators

Field	Indicator	Description
AutoLdev	SLM n DISK	The autoload route is to the SLM disk.
	SLM n TAPE	The autoload route is to the SLM tape.
	DEV a, b, c, (or) d	The autoload route is to the specified device.
	MS n	The associated MS number for the specified autoload route.
Image Restartable	No image test since last restart	The system did not run an image test since the last restart.
	Yes	The image survived the last inactive and out-of-sync restart.

Table 5-2 CMMNT level status field indicators

Field	Indicator	Description
	Maybe	The last image test could not determine the sanity of the image.
	No	The image did not survive the last inactive and out-of-sync restart.
Next CM REXTST restart type	warm	The next CM REXTST will perform a warm restart on the inactive CPU.
	cold	The next CM REXTST will perform a cold restart on the inactive CPU.
	reload	The next CM REXTST will perform a reload restart on the inactive CPU.

Memory level unlisted menu commands

You can enter the following commands from the Memory level of the MAP display.

ALIGN

This command aligns memory, data store and program store along 8 Mbyte limits.

Note: Synchronize the CM before performing this command.

CLAIM

This command returns all memory that the system did not use to the spare memory pools. Reclaim spare memory during periods of low traffic because the reclaiming process takes a long time.

CONFIG

This command configures the memory of the inactive CPU of a CPU pair to a set of adjoining addresses. The command queries a new card and sends the new information to the CM memory maintenance software. The new information allows the system to identify and correctly diagnose the card.

ROTATE

This command activates or deactivates the memory rotation algorithm. This algorithm operates at intervals of two days after a daily system CM REx test.

QUERYMEMLIMS

This command provides the following information to personnel:

- the platform the system uses
- the amount of memory the used
- available memory in the data store
- available memory in the program store
- available memory on the SLM
- the allocation thresholds reached, if the system reaches any thresholds

Figure 5-4 Example of a Memory level MAP display

```
CM      MS     IOD     Net      PM     CCS     Lns     Trks    Ext     APPL
.        .      .       .        .      .       .       .      .       .
Memory       CM   Sync  Act  CPU0  CPU1  Jam  Memory  CMMnt  MC  PMC
 0 Quit       0     .   cpu 1   .     .           .       .    .    .
 2
 3           CM 0   Plane 0  Plane 1
 4             1                1
 5             0987654321  P P  1234567890
 6 Tst_        ----......  - -  ......----
 7 Spare
 8 Cntrs_    MEMORY:
 9 Qrymem
10 Match_
11
12 RExTst
13 SwAct
14 Sync
15 DpSync
16
17 Trnsl_
18 Locate_
  TEAM26
Time  10:26  >
```

Memory level status field indicators

Table 5-3 lists the Memory level status field indicators.

Table 5-3 Memory level status field indicators

Field	Indicator	Description
Plane 0 or Plane 1	.	Card is in service.
	f	Card is has faults.

Table 5-3 Memory level status field indicators

Field	Indicator	Description
	x	Card is under test.
	-	Not equipped

MC level unlisted menu commands

You can perform the following command from the MC level of the MAP display.

LOGMASK

This command queries or alters the mask that determines which link hit errors generate a CM link hit log (CM128).

Figure 5-5 Example of an MC level MAP display

```
CM      MS     IOD     Net      PM     CCS     Lns     Trks    Ext     APPL
.        .      .       .        .      .       .        .      .       .
MC            CM   Sync  Act  CPU0  CPU1  Jam  Memory  CMMnt  MC  PMC
 0 Quit       0     .   cpu 1   .    .           .       .    .    .
 2
 3 Clock      CM 0
 4 Port        MC 0    MC 1
 5               .       .
 6 Tst_
 7 Bsy_      MC:
 8 RTS_
 9 DispCnts
10 Route
11 ClrCnts
12 RExTst
13 SwAct
14 Sync
15 DpSync
16
17 Trnsl_
18 Locate_
  TEAM26
Time  10:29  >
```

MC level status field indicators

Table 5-4 lists the MC level status field indicators.

Table 5-4 MC level status field indicators

Field	Indicator	Description
MC 0 and MC 1	mbsy	Personnel manually busied the message controller (MC) from the MAP terminal.
	sbsy	Both links on the MC are system busy.
	cbsy	The MS busied both links on the MC.
	istb	One link on the MC is out of service.
	sscf	Subsystem clock (SSC) on the MC has faults.
	todf	One or more time-of-day clocks (TOD) on this MC has faults.
	.	MC is in service.

Port level unlisted menu commands

You can perform the following command from the Port level of the MAP display.

ROUTE

This command displays primary and secondary MC routes for the MS.

Figure 5-6 Example of a Port level MAP display

```
CM      MS     IOD     Net      PM     CCS     Lns     Trks    Ext     APPL
.        .      .       .        .      .       .       .      .       .
Port          CM   Sync  Act  CPU0  CPU1  Jam  Memory  CMMnt  MC  PMC
 0 Quit        0    .   cpu 1  .     .           .       .    .    .
 2
 3            CM 0
 4             MC 0    MC 1
 5               .       .
 6 Tst_
 7                       P O R T
 8                      MC 0  MC 1
 9            Link  0   .     .
10            Link  1  oos    .
11           PORT:
12 RExTst
13 SwAct
14 Sync
15 DpSync
16
17 Trnsl_
18 Locate_
  TEAM6
Time  10:33  >
```

Port level status field indicators

Table 5-5 lists the Port level status field indicators.

Table 5-5 Port level status field indicators

Field	Indicator	Description
P O R T	oos	Port is out of service.
	sp	Port is split. The inactive plane uses the port.
	.	Port is in service.

Clock level unlisted menu commands

There are no CM clock level nonmenu commands.

Figure 5-7 Example of a Clock level MAP display

```
CM      MS     IOD     Net      PM     CCS     Lns     Trks    Ext     APPL
.        .      .       .        .      .       .       .      .       .
CLOCK         CM   Sync  Act  CPU0  CPU1  Jam  Memory  CMMnt  MC  PMC
 0 Quit        0    .   cpu 1  .     .           .       .    .    .
 2
 3            CM 0
 4             MC 0    MC 1
 5               .       .
 6 Tst_
 7                      T O D
 8 RTS_                 MC0   MC1
 9            Link  0   .     .
10 Route      Link  1   .     .
11
12 RExTst         SSC   .     .
13 SwAct
14 Sync      CLOCK:
15 DpSync
16
17
18 Locate_
  TEAM6
Time  10:34  >
```

Clock level status field indicators

Table 5-6 lists the Clock level status field indicators.

Table 5-6 Clock level status field indicators

Field	Indicator	Description
T O D	flt	TOD clock is on a busied MC or has faults.
	sp	TOD is on a split port card.
	.	TOD is in service.
	-	TOD is not equipped.
SSC	flt	Subsystem clock (SSC) has a system-detected fault.
	src	Both links that this SSC uses as frame pulse sources are out of service.
	ut	SSC is being tested.
	sp	SSC is split.

Table 5-6 Clock level status field indicators

Field	Indicator	Description
	istb	One of the links that this SSC uses as a frame pulse source is out of service.
	.	SSC is in service.

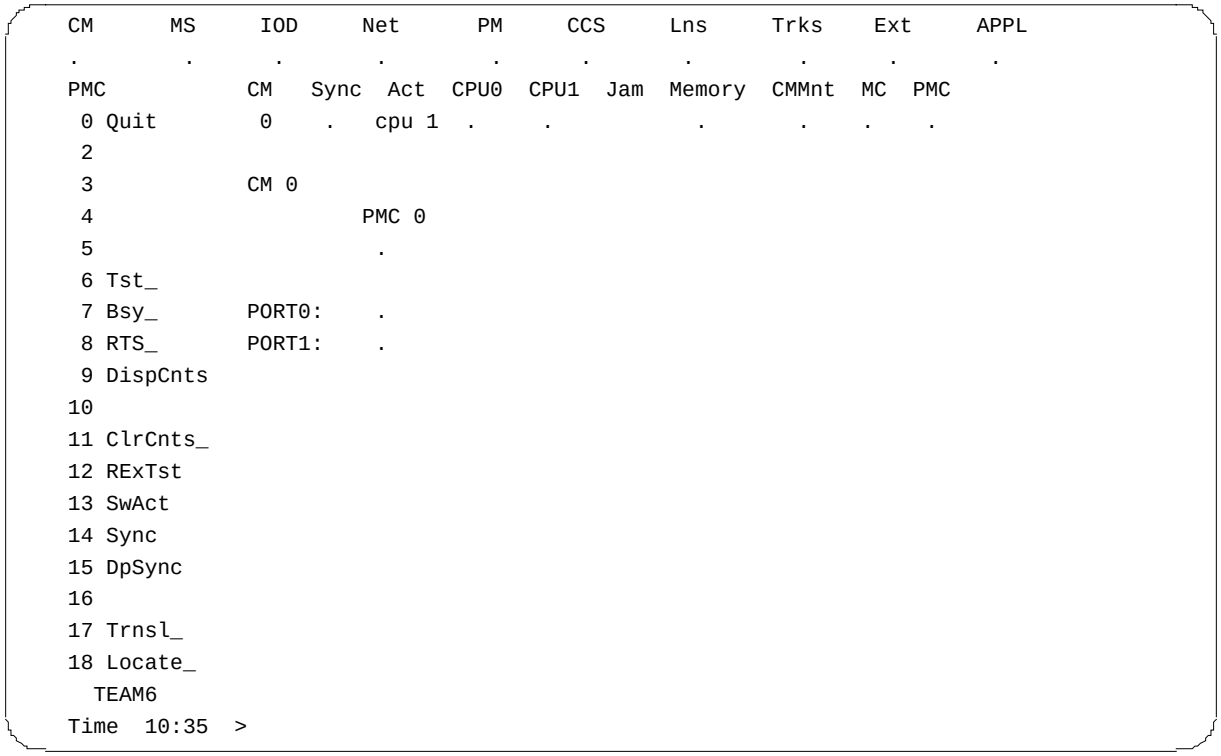
PMC level unlisted menu commands

You can perform the following command from the PMC level of the MAP display.

LOGMASK

This command queries or alters the mask that determines which link hit errors generate a CM link hit log.

Figure 5-8 Example of a PMC level MAP display



PMC level status field indications

Table 5-7 lists the PMC level status field indicators.

Table 5-7 PMC level status field indicators

Field	Indicator	Description
PMC	sbsy	Both PMC ports are system busy.
	mbsy	The user manually busied the PMC from the MAP terminal.
	istb	One of the PMC ports is busy.
	.	PMC is in service.
	-	PMC is not equipped.
Port0 **or** Port1	offl	Port is offline.
	mbsy	The user manually busied the port from the MAP terminal.
Port0 **or** Port1	sp	Port is split. The inactive plane uses the port.
	sbsy	Port is system busy.
	pbsy	SLM at the other end of the port is busy.
	istb	Port is in service, but had problems.
	.	Port is in service.
	-	Port is not equipped.

Reset terminal commands

Reset terminals allow operating company personnel to perform resets, boots, cold restarts, reload restarts, and warm restarts on the switch. The associated commands and maintenance activities for the reset terminal are advanced activities because these commands can interrupt subscriber service.

This section describes the CM reset terminal commands. This section also gives information about available parameters and options for each command.

\BOOT

This command bootloads the system. To bootload the system, this command reloads software (image files) from a specified storage device. If no parameters

are entered, this command reloads software from the primary autoload device. The system cannot process calls during a reboot. A reboot restarts all memory.

The \BOOT parameters appear in the following table.

Table 5-8 /BOOT parameters

Parameter	Description
SLM slm_no	Boots from the specified SLM disk.
SLM slm_noT	Boots from the specified SLM tape.
help	Displays syntax and usage notes for the command.

\JAM

Use this command only on the reset terminal for the inactive CPU. A jam forces the inactive CPU to remain inactive. The system cannot switch activity between CM planes. The system contains a procedure to make sure both CPUs do not jam at the same time. The command requires a yes or no confirmation before the command runs.

\RESTART

This command restarts the switch. The command also restores the software and hardware to known states. Fault severity determines the type of restart that the system performs. The system system diagnoses and determines fault severity.

The \RESTART parameters appear in the following table.

Table 5-9 \RESTART parameters

Parameter	Description
base	The system stops all call processing and clears temporary data store (DS).
warm	Calls in process remain up and the system clears temporary DS.
cold	Calls in process remain up until the peripherals start to come up. The peripherals take all calls down. The system clears temporary DS.
reload	Calls in process remain up until the peripherals start to come up. The peripherals take all calls down. The system clears temporary and permanent DS, and clears and deallocates DS RAM.

Table 5-9 \RESTART parameters

Parameter	Description
rtif	Reinitializes reset terminal firmware. This does not affect CM.
help	Displays syntax and usage notes for the command.

\BAUD

This command displays possible parameter values for baud rate settings.

\REMBAUD

This command sets the remote baud rate to the specified value.

The \REMBAUD parameters appear in the following table.

Table 5-10 \REMBAUD parameters

Parameter	Description
96	Sets baud rate to 9600 bit/s.
48	Sets baud rate to 4800 bit/s.
24	Sets baud rate to 2400 bit/s.
12	Sets baud rate to 1200 bit/s.
3	Sets baud rate to 300 bit/s.
help	Displays syntax and usage notes for the command.

\ENABLE

This command enables the specified function. The ENABLE and FREEZE commands work together. The ENABLE command activates specified functions. The FREEZE command turns off or disables specified functions.

The \ENABLE parameters appear in the following table.

Table 5-11 \ENABLE parameters

Parameter	Description
autoclr	Automatically clears the reset terminal display area 12 s after the user enters a command.
buffer	Controls the reception of CPU restart indexes.
e2a	Determines E2A control of CPU.

Table 5-11 \ENABLE parameters

Parameter	Description
remecho	Controls CPU and local video display unit (VDU) characters to the remote VDU.
waitrem	Determines display rate according to the slower of the local or remote baud rate.
help	Displays syntax and usage notes for the command.

\FREEZE

This command stops the specified function.

The \FREEZE parameters appear in the following table.

Table 5-12 \FREEZE parameters

Parameter	Description
autoclr	Stops automatic clearing of the reset terminal display area 12 s after the user enters a command.
buffer	Stops control of the reception of CPU restart indexes.
e2a	Stops determination of E2A control of CPU.
remecho	Stops control of CPU and local VDU characters to the remote VDU.
waitrem	Stops determination of display rate according to the slower of the local or remote baud rate.
help	Displays syntax and usage notes for the command.

\RELEASE JAM

This command releases the jam on the inactive CPU.

\REMIF

This command displays remote interface settings.

\RESET

This command forces a reset on the inactive CPU. Personnel can use this command when the CPU is in an unknown state. Personnel can use this command when other measures cannot restore the CPU.

The \RESET parameters appear in the following table.

Table 5-13 \RESET parameters

Parameter	Description
restart	Performs a cold restart on the inactive CPU.
FWCI	Enters the firmware command interpreter. Use this parameter only on the inactive side.
help	Displays syntax and usage notes for the command.

\OVERRIDE

This command allows a command that follows to perform resets and jams on the active CPU.

\QUERY

This command displays information for the parameters described in the following table.

Table 5-14 \QUERY parameters

Parameter	Description
hexcode	Displays the hexadecimal address for which data memory contents are to be displayed.
astatus	Displays a list of status bits. A 0 indicates the state exists. A 1 indicates the state does not exist or a failure occurred.
bstatus	Displays a list of status bits. A 0 indicates the state exists. A 1 indicates the state does not exist or a failure occurred.
cardin	Determines if the NT9X26 card had a power-up reset. A 1 indicates the card had a power-up reset.
cstatus	Displays a list of status bits. A 0 indicates the state exists. A 1 indicates the state does not exist or a failure occurred.
dstatus	Displays a list of status bits. A 0 indicates the state exists. A 1 indicates the state does not exist or a failure occurred.
linkflt	Displays the E2A serial link reception errors.
OOB band_no	Displays out-of-band (OOB) data for either band (0 or 1).

Table 5-14 \QUERY parameters

Parameter	Description
reset	Displays the most recent reset code in hexadecimal.
restart	Displays the most recent restart code in hexadecimal.
status	Displays the following information: • CM and CPU numbers • most recent restart index • activity, synchronization, and CPU clock states • NT9X26 RTIF paddle board state • jammed status
version	Displays the release version of the firmware in the NT9X26.
help	Displays syntax and usage notes for the command.

\SELF TEST

This command queries and displays the results of the most recent test performed on the NT9X26 paddle board.

\SET

This command sets specified parameters to a specified value.

The \SET parameters appear in the following table.

Table 5-15 \SET parameters

Parameter	Description
linkflt	Sets the link error count to zero.
remif1	Sets the NT9X26 interface protocol to RS-232C and the CPU interface protocol to RS-422.
remif2	Sets the NT9X26 interface protocol to RS-422 and the CPU interface protocol to RS-232C.
remif3	Sets the NT9X26 and CPU interface protocols to RS-422.
reset	Sets the reset code to FF.
help	Displays syntax and usage notes for the command.

Series 50Mx SuperNode and Series 70 SuperNode and SuperNode SE commands

This section describes some of the MAP terminal CM commands for the following switches:

- Series 50Mx SN
- Series 70 SN
- Series 70 SNSE

This section describes additions or changes to these commands. This section describes MAP responses for BASE05 and up.

QRYMEM

Use the Qrymem command to check both CM planes to make sure that the current memory configurations are supported. The system checks to determine if the CM is out of sync. The system determines if processor optionality problems are present. The Qrymem command is a menu command.

Table 5-16 QRYMEM command parameters and variables

Command	Parameters and variables
QRYMEM	There are no parameters or variables.

Usage examples

An example MAP response for the QRYMEM command appears in the following table.

Table 5-17 Usage examples of the Qrymem command

Task	Command and output example

Determine if both CM planes have valid memory configurations.	**>MAPCI;MTC;CM;MEMORY;QRYMEM**
	MAP response example:
	`CM 0`
	`  Plane 1`
	` 1 Plane 0 C  | C Plane 1  1`
	` 0987654321 P | P 1234567890`
	`---- ..... U | U .....----`
	` Memory: CPU 0 has a valid memory configuration CPU 1 has a valid memory configuration`

Error messages

The following table describes error messages for the QRYMEM command.

Table 5-18 Error messages for the QRYMEM command

MAP output	Meaning and action
`WARNING: The CM is out of sync with the CPU <act_num> active. The data for CPU <act_num> may be out of date.`	
	Meaning: The CM is out of sync. It is possible that internal inventory tables are not up to date for the inactive plane. This condition occurs if operating company personnel performed CPU/memory maintenance, like card replacement since the node was last in sync. The system always displays this warning for the inactive plane if the CM is out of sync.
	Action: Configure the memory of the inactive plane or resync the CM to make sure that the QRYMEM command accesses the latest data.
`WARNING: CPU <n> has a processor optionality error.`	
	Meaning: The QRYMEM command determined that the processor option entered in table OFCOPT is not valid in the context of the current CPU/memory configuration.
	Action: Contact next level of support.
`WARNING: CPU <n> has a processor optionality inconsistency. Datafill indicates <df_option> but CPU <n> is configured as <actual_option>.`	
	Meaning: The QRYMEM command determined that the processor option entered in table OFCOPT does not match the installed CPU/memory configuration.
	Action: Contact next level of support to correct datafill.
`CPU <n> has an invalid memory configuration.There are empty slots between memory cards. Fill the empty slots so that memory is contiguous.`	
	Meaning: The indicated CM plane has an invalid memory configuration. The QRYMEM command detected empty slots between memory cards.

Table 5-18 Error messages for the QRYMEM command

MAP output	Meaning and action
	Action: Move memory cards on the indicated plane to fill the empty slots. Move the minimum number of memory cards to fill the empty slots.
`CPU <n> has an invalid memory configuration.Empty slots found between the outer port card (<port>) and the first memory card. Shift memory cards so that memory grows away from the processor.`	**Meaning:** The indicated CM plane has an invalid memory configuration. The QRYMEM command found empty slots between the outer port card and the first memory card. Mixed memory on the CM must expand out from the processor, with all empty slots on the ends of each plane. **Action:** Move memory cards on the indicated plane to fill the empty slots. Move the minimum number of memory cards to fill the empty slots.
`CPU <n> has an invalid memory configuration. The NT91X14DB and NT9X14EA cards are intermixed. The NT9X14EA cards should be kept together and placed closest to the processor followed by the block of NT91X14DB cards.`	**Meaning:** The indicated CM plane has an invalid memory configuration. Memory cards are intermixed. You should keep the NT91X14DB and NT9X14EA cards together as contiguous sets. The NT9X14EA set must be the nearest set to the processor. The NT91X14DB set must follow this set. **Action:** Move memory cards on the indicated plane. This action makes sure memory cards do not intermix and that NT9X14EA cards are the nearest cards to the processor. Empty slots between memory cards cannot occur.
`CPU <n> has an invalid memory configuration. The block of NT9X14DB cards are closest to the processor. The NT9X14EA block of memory cards should be placed between the outer port card and the block of NT9X14DB cards.`	

Table 5-18 Error messages for the QRYMEM command

MAP output	Meaning and action
	Meaning: The NT9X14DB cards are the nearest cards to the processor. You must keep the NT9X14EA and NT9X14DB cards together as continuous sets. The NT9X14EA set should be nearest the processor and followed by the NT9X14DB set. **Action:** Move the NT9X14EA memory cards. These cards must be the nearest cards to the processor. The NT9X14DB set must follow these cards. Empty slots cannot occur between memory cards.
`CPU <n> has an invalid memory configuration. There are too many <memory_type> cards present on CPU . There should be a maximum of <limit> <memory_type> cards on CPU <n>.`	**Meaning:** Too many memory cards of a specified memory type are present on the plane. The system supports a maximum number of both NT9X14DB and NT9X14EA in mixed memory configurations. **Action:** Reduce the number of memory cards to a number that is equal to or less than the indicated limit.
`CPU <n> has an invalid memory configuration. There are too few <memory_type> cards present on CPU <n>. There should be a minimum of <limit> <memory_type> cards on CPU <n>.`	**Meaning:** Too few memory cards of a specified memory type are present on the plane. The system supports a minimum number of both NT9X14DB and NT9X14EA in mixed memory configurations. **Action:** Increase the number of memory cards to a number that is equal to or less than the indicated limit.
`CPU <n> has an invalid memory configuration. There are too few <memory_type> cards present on CPU <n>. On the SN50MX platform, a minimum memory configuration consists of two NT9X14EA's and four NT9X14DB's or three NT9X14EA's and two NT9X14DB's.`	**Meaning:** Too few memory cards of a specified memory type are present on the plane. Mixed memory configurations require a minimum number of NT9X14DB and NT9X14EA memory cards.

Table 5-18 Error messages for the QRYMEM command

MAP output	Meaning and action	
	Action:	Increase the number of memory cards of the indicated type to conform to a supported configuration.
`CPU <n> has an invalid memory configuration. There are too many NT9X14DB cards present on CPU <n>. There should be a maximum of <limit> NT9X14DB cards on a CPU plane with <ea_num> NT9X14EA cards.`		
	Meaning:	Too many NT9X14DB cards are present on a plane. The system requires a maximum number of NT9X14DB cards on a plane with a specified number of NT9X14EA cards.
	Action:	Increase the number of NT9X14DB cards to be equal to or more than the indicated limit.
`No reply from request.`		
	Meaning:	The QRYMEM command timed out.
	Action:	Gather logs and contact next level of support.
`Software inconsistancy - action aborted`		
	Meaning:	An internal software error occurred while the system waited for the action to complete.
	Action:	Save logs and contact next level of support.
`CPU <n> has an invalid memory configuration. The internal inventory tables are corrupt`		
	Meaning:	The command cannot complete because of an internal software problem.
	Action:	Contact next level of support.
`CPU <n> has an invalid memory configuration. The <component> PEC <pec> is not recognized.`		
	Meaning:	The system does not recognize a PEC code in the internal software inventory tables.
	Action:	If the information is correct, and the PEC described is present on the indicated plane, remove the component from the shelf. Replace the shelf with the correct component. Under any other conditions, contact the next level of support.

Table 5-18 Error messages for the QRYMEM command

MAP output	Meaning and action
`CPU <n> has an invalid memory configuration. The memory PEC <pec> is not supported by processor option <option>`	
	Meaning: The current configuration does not support a memory card.
	Action: Remove the memory card from the shelf and replace this card with the correct memory card.
`CPU <n> has an invalid memory configuration. This platform does not support mixed memory.`	
	Meaning: There are multiple memory types on a platform that do not support mixed memory.
	Action: Reconfigure the memory configuration with a single memory type.
`No mailbox available.`	
	Meaning: The system aborted the command.
	Action: Contact the next level of support.
`Request has been aborted.`	
	Meaning: System action or use of the ABTK command aborted the command.
	Action: Attempt the command again.
`The resources required to execute this command are in use.`	
	Meaning: Another maintenance action is in progress and uses internal resources required to complete the command.
	Action: Attempt the command again.

SYNC

Use the SYNC command to synchronize the two CPUs of the CM. The SYNC command is a menu command.

The following tables apply to SuperNode Series 70 only.

Table 5-19 SYNC command parameters and variables

Command	Parameters and variables
SYNC	[<Sync type> {normal nomatch notest}] [<Options> {nowait noprompt nocheck}]
Item	**Description**
normal	With the normal option (default), synchronization includes CPU testing and memory matching.
nomatch	With the nomatch option, the system does not perform a post synchronization memory match.
notest	With the notest option, the system does not perform CPU testing or memory matching.
nowait	The nowait option spawns a CI process to execute the synchronization command. The current MAP terminal does not lock until synchronization finishes. With the nowait option, the CI command prompt returns immediately.
noprompt	With the noprompt option, the system suppresses all warning messages that require confirmation.
nocheck	With the nocheck option, the system does not check call processing (CP) occupancy before a synchronization attempt.

Usage examples

The following table provides an example of the SYNC command.

Table 5-20 Usage examples of the SYNC command

Task	Sample command and input
Synchronize the CPUs with warnings that require suppressed confirmation. Synchronize the CPUs without memory matching after synchronization.	**>MAPCI;MTC;CM;SYNC NOMATCH NOPROMPT** *MAP response example:* `SYNCHRONIZATION SUCCESSFUL.`

Error messages

The following table describes the warning messages for the SYNC command.

Table 5-21 Error messages for the SYNC command

MAP output	Meaning and action
`WARNING: The CPUs are out of sync due to a problem with mismatches. The mismatch logs and mminfo should be analyzed before a manual resyncing is performed. Do you wish to continue?` `Please confirm ("Yes", "Y", or "No", "N").`	**Meaning:** This response warns the user that the CPUs are out of synchronization because of a mismatch. This response warns the user to determine the cause of the mismatch before the user attempts to synchronize again. **Action:** Analyze the mismatch logs and mminfo to determine the type of faults in the system. Handle these problems before you attempt to synchronize again.

CONFIG

Use the CONFIG command to configure the mate memory. The CONFIG command is a menu command that is not listed.

The following tables refer to SN Series 70 only.

Table 5-22 CONFIG command parameters and variables

Command	Parameters and variables
CONFIG	[<Options> {nowait noprompt notext}]

Item	Description
nowait	The current MAP terminal must not be locked during synchronization.
noprompt	The system does not display warning about possible side effects before a synchronization attempt.
notest	The system does not test the memory of the inactive CPU.

Usage examples

The following table provides an example of the CONFIG command.

Table 5-23 Usage examples of the CONFIG command

Task	Sample command and input
Configure the memory on the mate CPU with no prompting, no testing, and no waiting.	**>MAPCI;MTC;CM;MEMORY;CONFIG NOPROMPT NOTEST NOWAIT** *MAP response example:* `Configure Successful`

TST

Use the TST command to test memory cards on the CM shelf. The TST command is a menu command.

Execution of the TST command destroys the inactive software load.

The following tables refer to SN Series 70 only.

Table 5-24 TST command parameters and variables

Command	Parameters and variables
TST	<Test what> {CARD <card number> (1 to 10), ALL PROC} [<Length> {Short Long}] [<Options> {Nowait Noprompt}]
Item	**Description**
CARD	Test the specified card only (1 to 10).
ALL	Test all the memory cards on the inactive plane.
PROC	Test the memory located on the inactive processor only.

Usage examples

The following table provides an example of the TST command.

Table 5-25 Usage examples of the TST command

Task	Sample command and input
Perform a memory test on all the memory cards located on the inactive plane.	**>MAPCI;MTC;CM;MEMORY;TST ALL** *MAP response example:* `Maintenance action submitted. Memory test ok.`
Perform a memory test on card 5 only.	**>MAPCI;MTC;CM;MEMORY;TST CARD 5** *MAP response example:* `Maintenance action submitted. Memory test ok.`

TRNSL

Use the TRNSL command to map between memory cards and memory addresses. The TRNSL command is a CM;MEMORY menu command.

Table 5-26 TRNSL command parameters and variables

Command	Parameters and variables
TRNSL	<Plane number> {0 or } <translate what> {ALL CARD <Card number> {1 to 10} ADDRESS <Page>{-32768 to 32767} <Offset> {-32768 to 32767} PROC
Item	**Description**
ALL	Performs a translation for all memory on the specified plane.
CARD	Performs a translation for the specified card (1 to 10).
ADDRESS	Performs a translation of the specified address (-32768 to 32767).
PROC	Performs a translation of processor memory on the specified plane.

Usage examples

The following table provides an example of the TRNSL command.

Table 5-27 Usage examples of the TRNS

Task	Sample command and input

Display a memory inventory for plane 0.	**MAPCI;MTC;CM;MEMORY;TRNSL 0 PROC**
	
	Note: The following example contains the portion of the response for a Series 70EM processor.
	
	MAP response example:
	
	`Processor on plane contains 512 MBytes of memory.`
	`Usable module address ranges are:`
	`Address Range: #04000000 to #05FFFFFE`
	`Address Range: #20000000 to #21FFFFFE`
	`Address Range: #06000000 to #07FFFFFE`
	`Address Range: #22000000 to #23FFFFFE`
	`Spare memory: 384 MBytes`
	`Card 1 on plane 0 contains 3 32MBYTE memory modules.`
	`Usable module address ranges are:`
	`Module 0: spare,`
	`Module 1: spare,`
	`Module 2: spare.`
	`Card 2 on plane 0 contains 3 32MBYTE memory modules.`
	`Usable module address ranges are:`
	`Module 0: spare,`
	`Module 1: spare,`
	`Module 2: spare.`
	`Card 3 on plane 0 contains 3 32MBYTE memory modules.`
	`Usable module address ranges are:`
	`Module 0: spare,`
	`Module 1: spare,`
	`Module 2: spare.`

CNTRS

Use the CNTRS command to display the ECC error counts associated with each memory card. The CNTRS command is a menu command.

Table 5-28 CNTRS command parameters and variables

Command	Parameters and variables
CNTRS	<Plane number> {0 or 1} <Display what> CARD {1 to 10} ALL PROC}

Item	Description
CARD	Displays ECC error counts for the specified card only.
ALL	Displays ECC error counts for all cards on the specified plane. This display includes the processor ECC error counts.
PROC	Displays ECC error counts for the processor memory only.

Usage examples

The following table provides an example of the CNTRS command.

Table 5-29 Usage examples of the CNTRS command

Task	Sample command and input
Display ECC error counts for all the memory cards on plane 0.	**>MAPCI;MTC;CM;MEMORY;CNTRS 0 ALL** *MAP response example:* `CM 0 CPU Plane 0 Backplane Card 12 ERR CNTS 00 PCCAB error count 0`

LOCATE

Use the LOCATE command to locate a memory card on the CM. The information provided indicates the bay, shelf, and slot for a memory card. The LOCATE command is not listed as a menu command.

Note: In SN Series 70, the LOCATE command for card 0 generates a display of valid information. For Series 20 through 60, the LOCATE command for card 0 generates an error message.

Table 5-30 LOCATE command parameters and variables

Command	Parameters and variables
LOCATE	<Plane Number> {0 or 1} <Card number> {0 to 10}

Usage examples

The following table provides an example of the LOCATE command.

Table 5-31 Usage examples of the LOCATE command

Task	Sample command and output

Generate the display of location information for card 0 on plane 1.	**>MAPCI;MTC;CM;MEMORY;LOCATE 1 0**
	MAP response example:
	`Site FLr RPos Bay_id Shf Description Slot EqPEC`
	`HOST 00 A00 DPCC:00 18 MEM :00:1:0 20 9X10BA FRNT`

Error messages

The following table provides an explanation of the error messages for the LOCATE command.

Table 5-32 Error messages for the LOCATE command

MAP output	Meaning and action
`Specified card does not exist Memory card plane number: 1 card number: 10`	**Meaning:** The card specified by the LOCATE command does not exist on the plane of the CPU shelf. **Action:** Enter the LOCATE command again and specify a valid plane and card combination.

MATCH

Use the Match command to synchronize the two CPUs of the CM. The Match command is a menu command.

Table 5-33 MATCH command parameters and variables

Command	Parameters and variables
MATCH	<Match what> {CARD card number to 10}, ALL, PROC} [<Options> {nowait noprompt}]
Item	**Description**
CARD	Specifies that the system is to perform a memory match on the specified card
ALL	Specifies that the system is to perform the memory match on all memory cards. These memory cards include the processor card
PROC	Specifies that the system is to perform memory match on the processor memory only.
nowait	With the nowait option, the CI command prompt returns immediately. This option allows the use of the MAP for other functions while the system executes the MATCH command.
noprompt	With the noprompt option, the system suppresses the warning messages that require confirmation. The system will confirm warning automatically.

Usage examples

The following table provides an example of the Match command.

Table 5-34 Usage Examples of the MATCH command

Task	Sample command and input

Perform a match on all memory cards while the CM planes are in sync.	**>MAPCI;MTC;CM;MEMORY;MATCH ALL**
	MAP response example:
	`Matching memory between CPUs in SYNC.`
	`Match OK.`

Table 5-34 Usage Examples of the MATCH command

Task	Sample command and input

Perform a match on all memory cards while the CM planes are out of sync.	**MAPCI;MTC;CM;MEMORY;MATCH ALL**
	MAP response example:
	`Matching memory between CPUs out of SYNC.`
	`Match Ok.`

Error messages

The following table provides an explanation of error messages for the Match command.

Table 5-35 Error messages for the Match command

MAP output	Meaning and action
`MATCH FAILED. PROCESS MAY HAVE TRAPPED ON MEMORY FAULT. CHECK CARD STATUS INDICATOR FOR REMAINING 'X' INDICATOR.`	**Meaning:** The memory match trapped on a memory error while the computing module (CM) was out of sync. **Action:** There is no action required.
`MATCH FAILED: SYNC DROPPED ON MATCH OF CARD <n>.`	**Meaning:** The system discovered a mismatch, where is the number of the card, as shown in the memory level status display. **Action:** There is no action required.
`MATCHING MEMORY BETWEEN CPUS IN SYNC.`	**Meaning:** The CPUs are in sync. **Action:** There is no action required.
`SPECIFIED CARD DOES NOT EXIST.`	**Meaning:** The specified card is not equipped. **Action:** There is no action required.
`THE INACTIVE CPU SHOULD NOT BE JAMMED WHILE MATCHING IN SYNC. DO YOU WISH TO CONTINUE? PLEASE CONFIRM ("YES", "Y", "NO", "N"):`	

Table 5-35 Error messages for the Match command

MAP output	Meaning and action	
	Meaning:	The system prompts for confirmation before the system prompts the match test with the inactive CPU jammed in sync.
	Action:	Enter YES or Y to continue with the match command. Enter NO or N to abort the command.
`VERIFYING OWN MEMORY WHILE CPUS OUT OF SYNC.`		
	Meaning:	The CPUs are out of sync.
	Action:	There is no action required.

MMINFO

Use the MMINFO command to display information about mismatches that occurred in the DMS Core. The MMINFO command is a nonmenu command.

Table 5-36 MMNFO command parameters and variables

Command	Parameters and variables
MMINFO	[SUMMARY CLEAR NEW LAST [<format>{decode, brief, meminfo, debug}], RESTART [<format> {decode, brief, meminfo, debug}], ALL [<format>{decode, brief, meminfo, debug}] [<mismatch no> {0 t0 32767}] {<format>{decode, brief, meminfo,}]

Item	Description
SUMMARY	A short summary for each mismatch. Default.
CLEAR	Clear all mismatch data saved in the MMINFO buffer. Optional.

Table 5-36 MMNFO command parameters and variables

Command	Parameters and variables
NEW	Display a summary of the most recent mismatches. Optional.
LAST	Display the last mismatch only. Optional.
RESTART	Display the mismatch before last restart. Optional.
ALL	Display a maximum of 10 mismatches. Optional.
<mismatch no.>	Display specific mismatch number. Numeric string.
DECODE	DECODE. Displays all relevant mismatched information. Decodes all relevant registers and faulty functional object information blocks (FOIB). Default. Nortel Networks recommends this option.
BRIEF	Displays the mismatch information in brief format. Optional.
MEMINFO	Displays memory configuration and memory inventory snapshot. Optional.
DEBUG	Displays all mismatch information only used by Nortel Networks for debugging purposes. Optional.

Usage examples

The following table provides an example of the MMINFO command.

Table 5-37 Usage examples of the MMINFO command

Task	Sample command and input
Display information about the MMINFO command.	

Table 5-37 Usage examples of the MMINFO command

Task	Sample command and input
>HELP MMINFO *MAP response example:* MMINFO - Display data about the last few mismatches. SUMMARY : Two line summary for each mismatch (default). CLEAR : Clear all saved mismatch data. NEW : Display most recent mismatch. LAST <format> : Display the last mismatch only. RESTART <format> : Display the mismatch before last restart. ALL <format> : Display all mismatches. <n> <format> : Display specific mismatch number. where <format> is DECODE - displays all relevant mismatch data. All registers and faulty FOIBs are decoded. (default) MEMINFO - displays memory configuration and memory inventory snapshot only. BRIEF - displays mismatch information in brief format. DEBUG - displays a complete mismatch dump. All registers and FOIBs are output in hex and are decoded. Parms: [<Which Option> {SUMMARY, CLEAR, NEW, LAST [<Format> {DECODE, BRIEF, MEMINFO, DEBUG}], RESTART [<Format> {DECODE, BRIEF, MEMINFO, DEBUG}], ALL [<Format> {DECODE, BRIEF, MEMINFO, DEBUG}]}] [<Mismatch no.> {0 TO 32767}] [<Format> {DECODE, BRIEF, MEMINFO, DEBUG}]	

Table 5-37 Usage examples of the MMINFO command

Task	Sample command and input

>MMINFO SUMMARY
 	
Note: The following example contains an mminfo summary of a mismatch for a SuperNode Series 70.
 	
MAP response example:
 	
`Mismatch Log number: 1 1999-NOV-24 14:23:58`
`Activity: Start: CPU0, Final: CPU0`
 	
`No more mismatches`	

Warning messages for the MMINFO command

The following table describes warning responses to the MMINFO command.

Table 5-38 Warning messages for the MMINFO command

MAP output	Meaning and action
`The following report is incomplete. Analysis and recovery are still in progress for this mismatch Please generate the report again when the recovery is complete.`	
	Meaning: The analysis for the requested mismatch is not complete.
	Action: Enter MMINFO SUMMARY to check if analysis and recovery for requested mismatch is complete.
`Analysis/Recovery for this mismatch is currently in progress.`	
	Meaning: The analysis and recovery is still in progress.
	Action: There is no action required.
`The registers dump within this group is invalid for CPU 0.`	
	Meaning: This message indicates that the snapshot for the register group did not complete for CPU 0. This message applies for one or more register groups PCCAB2, TMISC, SCIE, CACHE, SR70 registers.
	Action: There is no action required.
`The registers dump within this group is invalid for CPU 1.`	

Table 5-38 Warning messages for the MMINFO command

MAP output	Meaning and action
	Meaning: This message indicates that the snapshot for the register group did not complete for CPU 1. This message applies for one or more register groups PCCAB2, TMISC, SCIE, CACHE, SR70 registers. **Action:** There is no action required.
`The registers dump within this group is invalid for both CPUs.`	**Meaning:** This message indicates that the snapshot for the register group did not complete for both CPUs. This message applies for one or more register groups PCCAB2, TMISC, SCIE, CACHE, SR70 registers. **Action:** There is no action required.

Error messages

The following table provides an explanation of the error messages for the MMINFO command.

Table 5-39 Error messages for the MMINFO command

MAP output	Meaning and action
`MMINFO DATABASE IS CLEARED.`	**Meaning:** The system clears the MMINFO database. This message appears when you enter the MMINFO CLEAR command. **Action:** There is no action required.

`NEW MISMATCH SUMMARY`
` <list of new mismatches>`
` NO MORE MISMATCHES`
	Meaning: This list appears when you enter the MMINFO NEW command. The system lists all mismatches that occurred since the last MMINFO NEW command.
	
	Action: There is no action required.

`NO NEW MISMATCHES`	

Table 5-39 Error messages for the MMINFO command

MAP output	Meaning and action	
	Meaning:	This message appears when you enter the MMINFO NEW command and no new mismatches occured since the previous MMINFO NEW command.
	Action:	There is no action required.

`MISMATCH SUMMARY`
` <list of mismatches>`
` NO MORE MISMATCHES`		

	Meaning:	This list appears when you enter a MMINFO, MMINFO SUMMARY, or MMINFO ALL command. The system lists all stored mismatches.
	Action:	There is no action required.
`NO MISMATCHES`		
	Meaning:	This message appears when you enter a MMINFO, MMINFO SUMMARY, or MMINFO ALL command and the system has no stored mismatches.
	Action:	There is no action required.
`<Mismatch information regarding a particular mismatch number>`		
	Meaning:	The information that appears is associated with a specified mismatch when you enter the command MMINFO . can be BRIEF, DECODE, MEMINFO. If you do not specify a format, the system uses the default.
	Action:	There is no action required.
`NO SUCH MISMATCH`		
	Meaning:	This message appears when you enter the command MMINFO and the system has no stored mismatch in the database.
	Action:	There is no action required.
`<Last mismatch information>`		
	Meaning:	This information appears when you enter the MMINFO LAST command.

Table 5-39 Error messages for the MMINFO command

MAP output	Meaning and action
	Action: There is no action required.
`<Mismatch information before restart>`	
	Meaning: This information appears when you enter the MMINFO RESTART command. can be one of FORMAT, BRIEF, DECODE. If you do not specify a format, the system uses the default.
	Action: There is no action required.

CM mismatch commands

This section describes the commands and responses used at the MAP for computing module (CM) mismatching. This section describes additions or changes to these commands and MAP responses for BASE06 and up.

SYNC

Use the SYNC command to place the CPUs of the CM in synchronized-matched mode. The SYNC command is a menu command.

The following responses apply to SN Series 20 through 60 only.

Note: The responses described are created or changed for CM mismatching only.

Table 5-40 SYNC command parameters and variables

Command	Parameters and variables
SYNC	[<configuration> {optimum}] <sync type> {normal nomatch notest nohands}] [<options> {nowait noprompt eccon noburst nocheck force}]

Table 5-40 SYNC command parameters and variables

Command	Parameters and variables
configuration	This parameter specifies the memory configuration. With the optimum option, the system configures the memory on the inactive side. The system populates the memory cards closest to the CPU first. Without the optimum option, the system configures the memory on the inactive side as a mirror image of active side memory.
sync type	This parameter specifies the type of synchronization. With the normal option (default), synchronization includes CPU testing and memory matching. With the nomatch option, the system does not perform a post synchronization memory match. With the notest option, the system does not perform CPU testing or memory matching. With the nohands option, a handshake override does not occur. This option is available with 68k processors only.
options	This parameter specifies the synchronization option. With the nowait option, the CI command prompt returns immediately. With the noprompt option, the system suppresses the warning messages that require confirmation. With the eccon on option, the system leaves the error correction code (ECC) on. With the noburst option, the system disables the burst mode. The noburst option is available with Series 60 processors only. With the< nocheck option, the system does not check CP occupancy before a synchronization attempt. The force option overrides the CM MMNoSy alarm and the system attempts synchronization.

Error messages

The following table describes the error messages for the SYNC command.

Table 5-41 Error messages for the SYNC command

MAP output	Meaning and action
`Synchronization was dropped due to a mismatch event. Please ensure that all mismatch logs have been properly analyzed, and that all appropriate recovery actions been taken before continuing with the synchronization attempt. Regaining sync with unresolved mismatch causing conditions could compromise system integrity. The MMNoSy alarm should be cleared prior to attempting CM synchronization. Re-enter the SYNC command with the FORCE option in order to override this condition.`	**Meaning:** The system generates this response on any manual synchronization attempt when the system raises the MMNoSyc alarm. The message warns site personnel to not place the CM back in synchronization after mismatch handling software detects a fault. Site personnel must first analyze the mismatch logs and take correct recovery action. **Action:** Follow NTP procedures for mismatch log analysis. Contact the next level of support if necessary. Clear the MMNoSy alarm as part of this manual recovery from a mismatch. If you decide to override the MMNoSyc alarm and synchronize the CM, enter the SYNC command again and specify the FORCE option.
`No record has been made of any replacement of hardware by manual action. Manual card replacements must be recorded via the SWAPHW command in order to ensure proper fault isolation in future mismatch events. Proceed with CM synchronization only if no hardware has been replaced.Do you wish to continue? Please confirm ("YES", "Y", "NO", "N")`	**Meaning:** There is no meaning.

Table 5-41 Error messages for the SYNC command

MAP output	Meaning and action
	Action: If operating company personnel did not replace hardware since synchronization was dropped, enter Y or YES. This entry confirms that you will proceed with synchronization of the CPUs. If operating company personnel replaced any hardware since the system dropped synchronization, enter N or NO and the correct SWAPHW commands. This action records the hardware changes with the software maintenance systems. After you perform the correct commands, enter the SYNC command again.
`The FORCE option has been specified, and the MMNoSyc alarm is raised. System integrity could be compromised if synchronization is attempted before all appropriate analysis and recovery actions have been performed. Do you wish to continue? Please confirm ("YES", "Y", "NO", "N")` **Meaning:** The system displays this response if you specify the FORCE option and the system raised the MMNoSyc alarm. You can compromise system integrity if you do not correctly follow mismatch recovery procedures documented in the NTPs to synchronize the CM. This response indicates this risk and requests confirmation from the user before the system proceeds with the synchronization attempt. **Action:** If you enter Y or YES, the system clears the MMNOSyc alarm. The system generates a log that indicates that you entered and confirmed the FORCE option. The log indicates the terminal ID of the user that performed the action. If you enter Y or YES, the system confirms that the user violated the documented mismatch recovery procedure. You can compromise system integrity if you do not perform analysis of potentially unstable hardware to synchronize the CM . If you enter N or NO, the system aborts the synchronization attempt. This action allows the system to follow the mismatch recovery process.	

Table 5-41 Error messages for the SYNC command

MAP output	Meaning and action

`The following cards have been reported as being replaced since the last drop of synchronization. Verify that these cards truly reflect all hardware which has been replaced before continuing with the synchronization attempt.`
 	
`Site Flr RPos Bay-id Shf Description Slot EqPEC`
`Do you wish to continue?`
`Please confirm ("YES", "Y", "NO", "N")`
	Meaning: The system displays this response if any recorded manual card replacements occurred since the last drop of synchronization.
	
	Action: If you confirm the prompt with a Y or YES, the system deletes all mismatch history database information. This information applies to all events that involve any of the replaced circuit packs.
	
	If the response accurately displays all hardware replaced since the last drop sync, enter Y or YES. This response confirms that you want to proceed with synchronization of the CPUs.
	
	If the response does not accurately display all hardware replaced since synchronization was dropped, enter N or NO. Enter SWAPHW or UNSWAPHW commands in order to record the hardware changes with the software maintenance systems. After you perform the correct commands, enter the SYNC command again.
	
	Note: If you entered the commands that record a manual change of hardware since the last drop in synchronization, the system updates the mismatch history database. The system performs this update after successful synchronization. The system deletes all mismatch history data related to the replaced cards. The system clears the MMNoSyc alarm after successful synchronization.

SWAPHW

Use the SWAPHW command to notify the maintenance software system of any card replacements since the CM was last in synchronization. The SWAPHW command is not listed as a menu command.

This command does not apply to the SuperNode Series 70 platform.

The following responses appear on SuperNode Series 20 through 60.

Table 5-42 SWAPHW command parameters and variables

Command	Parameters and variables
SWAPHW	<swap what> CARD {<shelf> {0 to 1} <slot> {1 to 38} <side> {frnt, back}, PLANE, QUERY} <option> {noprompt}]
Item	**Description**
shelf	The shelf parameter identifies the circuit pack that personnel replaced.
slot	The slot parameter identifies the circuit pack that personnel replaced.
side	The side parameter identifies the circuit pack that personnel replaced.
option	The noprompt option causes the system to bypass manual confirmation steps. This option eliminates the need for manual intervention to perform the command to completion.

Usage examples

An example of the SWAPHW command appears in the following table.

Table 5-43 Usage examples of the SWAPHW command

Task	Sample command and input

Display information about the SWAPHW command.	**>MAPCI;MTC;CM;HELP SWAPHW**
	MAP response example:
	`[<Swap_What> {CARD <Shelf> {0 TO 1}`
	`<Slot> {1 TO 38}`
	`<Side> {FRNT,`
	`BACK}, PLANE,`
	`QUERY}]`
	`[<Option> {NOPROMPT}]`

Warning messages

The following table explains warning messages for the SWAPHW command.

Table 5-44 Warning messages for the SWAPHW command

MAP output	Meaning and action

`You have indicated that the following circuit pack has been replaced. Please verify that the following list accurately reflects the location of the replaced circuit pack, and that the displayed PEC code matches the pack currently equipped in that slot:`
`Site Flr RPos Bay-id Shf Description Slot EqPEC`
`<site> <flr> <rpos> <bay> <shf><desc> <slot> <pec> <side>`
`Do you wish to continue?`
`Please confirm ("YES", "Y", "NO", "N")`
	Meaning: The prompt echoes the parameter data entered by user. The user uses the CARD option of the SWAPHW command to indicate that the user replaced a single circuit pack. The system requires confirmation before the system records the circuit pack as replaced.
	
	Action: If the card list accurately represents the location of the replaced circuit pack, enter Y or YES.
	
	If the card list does not accurately represent the location of the replaced circuit pack, enter N or NO. Enter the SWAPHW command again with the correct arguments.

`All "Memory Fault, Correctable" history will be deleted during the next manual SYNC attempt. The PLANE option of this command should be used only during manual recovery from a MFC plane threshold being exceeded.`
`Do you wish to continue?`
`Please confirm ("YES", "Y", "NO", or "N")`
	Meaning: The prompt confirms that the user entered the PLANE argument. The prompt confirms that the site will perform a manual recovery from an exceeded MFC plane threshold. Manual recovery invalidates all MFC history.

Table 5-44 Warning messages for the SWAPHW command

MAP output	Meaning and action
	Action: The MFC history database enables software maintenance systems to identify suspected hardware that has faults before the hardware fails completely. An excessive number of MFC events not localized to a specified memory card can exceed the MFC plane threshold. The MFC111 log indicates this condition. Invalidate this database only as part of the manual recovery for this type of fault indication. If you perform a manual recovery from an exceeded MFC plane threshold, enter Y or YES to confirm. If you do not perform the manual recovery, enter N or NO.

`You have indicated that the following circuit pack has been replaced. Please verify that the following list accurately reflects the location of the replaced circuit pack, and that the displayed PEC code matches the pack currently equipped in that slot:`
`Site Flr RPos Bay-id Shf Description Slot EqPEC`
`<site> <flr> <rpos> <bay> <shf><desc> <slot> <pec> <side>`
`Do you wish to continue? Please confirm ("YES", "Y", "NO", "N")`
	Meaning: The prompt echoes back the parameter data that the user entered. The user uses the CARD option of the SWAPHW command to indicate that a single circuit pack is being replaced. The system requires *confirmation before the system records the circuit pack as replaced.
	
	Action: If the card list accurately represents the location of the replaced circuit pack, enter Y or YES.
	
	If the card list does not accurately represent the location of the replaced circuit pack, enter N or NO. Enter the SWAPHW command again with the correct arguments.

Error messages

The following table describes the error messages for the SWAPHW command.

Table 5-45 Error messages for the SWAPHW command

MAP output	Meaning and action
`This command is not supported on Series 70.`	**Meaning:** The system does not support the mismatch history database on Series 70. This command has no effect. **Action:** There is no action required.
`Card replacement has been recorded.`	**Meaning:** This response appears when the user enters Y or YES to the prompt. **Action:** The system adds the specified card to the list of replaced cards. The system will not actually update the mismatch history database until the next manual SYNC attempt.
`Aborted. Card replacement has NOT been recorded.`	**Meaning:** This response appears when the user enters N or NO to the prompt. **Action:** The system does not store card replacement information.
`No circuit pack replacements have been recorded.`	**Meaning:** This response appears when the user supplies the QUERY argument to the SWAPHW command. The system recorded no circuit packs replacements. **Action:** There is no action required.

`The following cards have been identified as being replaced.`
`The displayed PEC codes correspond to the cards which currently reside in the appropriate slots.`
`Site Flr RPos Bay-id Shf Description Slot EqPEC`
`<site> <flr> <rpos> <bay> <shf><desc> <slot> <pec> <side>`	

Table 5-45 Error messages for the SWAPHW command

MAP output	Meaning and action	
	Meaning:	This response appears when the user supplies the QUERY argument to the SWAPHW command. The user previously recorded circuit pack replacements with the SWAPHW command.
	Action:	There is no action required.

UNSWAPHW

Use the UNSWAPHW command to reverse any card replacement information not correctly entered with the SWAPHW command. The UNSWAPHW command is a menu command that is not listed.

This command does not apply to the SuperNode Series 70 platform.

The following responses appear on SuperNode Series 20 through 60.

Table 5-46 UNSWAPHW command parameters and variables

Command	Parameters and variables
UNSWAPHW]	<swap what> CARD {<shelf> {0 to 1} <slot> {1 to 38} <side> {frnt, back}, PLANE, QUERY} [<option> {noprompt}
Item	**Description**
shelf	The shelf parameter identifies each circuit pack that the system will indicate as NOT replaced.
slot	The slot parameter identifies each circuit pack that the system will indicate as NOT replaced.
side	The side parameter identifies each circuit pack that the system will indicate as NOT replaced.
option	The noprompt option causes the system to bypass the manual confirmation step. This option eliminates the need for manual intervention to allow the system to execute the command to completion.

Usage examples

An example of the UNSWAPHW command appears in the following table.

Table 5-47 Usage examples of the UNSWAPHW command

Task	Sample command and input

Display information about the UNSWAPHW command.	**>MAPCI;MTC;CM;HELP UNSWAPHW**
	MAP response example:
	`[<UnSwap_What> {CARD <shelf> {0 to 1}`
	`<slot> {1 to 38}`
	`<side> {FRNT,`
	`BACK}`
	`PLANE}]`
	`[<Optoin>} {NOPROMPT}`

Warning messages

The following table describes warning messages for the UNSWAPHW command.

Table 5-48 Warning messages for the UNSWAPHW command

MAP output	Meaning and action

`You have indicated that the following circuit pack has NOT been replaced. Please verify that the displayed PEC code accurately reflects the circuit pack that resides in the slot:`
 	
`Site Flr RPos Bay-id Shf Description Slot EqPEC`
`<site> <flr> <rpos> <bay> <shf><desc> <slot> <pec> <side>`
 	
`Do you wish to continue?`
`Please confirm ("YES", "Y", "NO", "N")`
	Meaning: The prompt echoes the parameter data that the user entered. The system requires the user to verify the parameter data before the system records the card as not replaced.
	
	Action: If the displayed card list correctly describes the circuit pack that was not correctly entered in a SWAPHW command, enter Y or YES.
	
	If the card description does not match the desired circuit pack, enter N or NO.

Error messages

The following table describes the responses to the UNSWAPHW command.

Table 5-49 Error messages for the UNSWAPHW command

MAP output	Meaning and action
`This command is not supported on Series 70.`	
	Meaning: The system does not support the mismatch history database on Series 70. This command has no effect.
	Action: There is no action required.
`Aborted. This card is still recorded as having been replaced.`	
	Meaning: This response appears when the user enters N or NO to the prompt. In this case, the system aborts the UNSWAPH command. This action does not affect the card replacement information.
	Action: If necessary, enter the UNSWAPHW command again with the correct arguments.
`This card has been recorded as NOT having been replaced.`	
	Meaning: This response confirms that the user entered Y or YES to the prompt, and that the system backed out card replacement.
	Action: The system removed the card from the list of replaced cards. Following a successful manual synchronization again of the CM, the system does NOT delete mismatch history information for this card.

CLRALARM

Use the CLRALARM command to clear MMNoSy, MMsync, and MemFlt alarms. The DISABLE command disabled these alarms at the CMMNT MAP level. The CLRALARM command is a menu command that is not listed. Release BASE06 introduced this command.

Note: The MMNoSy, MMsync and MemFlt are mismatch related alarms are MMNoSy, MMsync and MemFlt. These alarms do not always require

the same manual recovery steps. This command clears the alarms after the user performs all necessary analysis of the mismatch log data.

Table 5-50 CLRALARM command parameters and variables

Command	Parameters and variables
CLRALARM	<alarm> {mmnosy mmsync memflt} [<option> {noprompt}]
Item	**Description**
alarm	This parameter specifies the type of CM alarm that the command will clear. The options are mmnosy, mmsync, and memflt.
option	This parameter specifies the alarm clearing option. The only available option is noprompt. The option noprompt suppresses the warning messages that require confirmation.

Usage examples

An example of the CLRALARM command appears in the following table.

Table 5-51 Usage examples of the CLRALARM command

Task	Sample command and input

Display information about the CLRALARM command.	**>MAPCI;MTC;CM;HELP CLRALARM**
	MAP response example:
	`<Alarm> {MMNOSY,`
	`{MMSYNC,`
	`MEMFLT}`
	`[<Option> {NOPROMPT}]`

Error messages

The following table describes the error messages for the CLRALARM command.

Table 5-52 Error messages for the CLRALARM command

MAP output	Meaning and action

`The <alarm> will be cleared.`
`Do you wish to continue?`
`Please confirm ("YES", "Y", "NO", "N")`
	Meaning: This response echoes the parameters and required confirmation that the user entered before the system proceeds.
	
	Action: To continue and clear the specified alarm, enter Y or YES. If you do not want to clear the specified alarm, enter N or NO.

`The <alarm> has been cleared.`	**Meaning:** The system clears the alarm, regardless of the previous state of the alarm. The system generates a CM176 log that indicates which alarm the system cleared. **Action:** There is no action required.

MMINFO

Use the MMINFO command to display information about mismatches that occurred in the DMS-Core. The MMINFO command is a nonmenu command.

Table 5-53 MMINFO command parameters and variables

Command	Parameters and variables
MMINFO	[<which> {SUMMARY, CLEAR, NEW, LAST [<format>{decode}] RESTART [<format> {decode}] ALL [<format> {decode}]}] [<mismatch no.> {0 to 32767}] [<format> {decode}]
Item	**Description**
SUMMARY	This default variable generates a one-line summary for each mismatch.

Table 5-53 MMINFO command parameters and variables

Command	Parameters and variables
CLEAR	This variable clears all saved mismatch data.
NEW	This variable displays mismatches since the last execution of the command MMINFO-NEW
LAST	This variable displays a complete mismatch dump for the last mismatch only.
RESTART	This variable displays a complete mismatch dump for the last mismatch before restart.
ALL	This variable displays all mismatches in MMINFO.
<mismatch no.>	This variable specifies the mismatch for which the system displays information.

Usage examples

An example of the MMINFO command appears in the following table.

Table 5-54 Usage examples of the MMINFO command

Task	Sample command and input

Display information about mismatches.	**>MMINFO**
	MAP response example:
	`Mismatch Log number : 0 ???-00 00:00:00`
	`Activity: Start: CPU 242, Final: CPU 223`
	`Mismatch result: Unknown Result`
	`Mismatch condition: Unknown Condition`
	`System recovery action: aborted, too many mismatches.`
	`No mismatch recovery status.`
	`No more mismatches.`

MMSYNC

Operating company personnel can use the MMSYNc command to perform the following actions:

- clear the matcher transient mismatch (MTM) counts
- determine the synchronization and drop synchronization thresholds for MTM

- determine the current MTM count
- determine if MTM count exceeded the synchronization or drop synchronization threshold
- set the MMsync alarm threshold for MTM

The MMSYNC command is a menu command that is not listed that applies only to Series 60 processors.

Execute the MMSYNC command from the CM, MC, Memory, and PMC MAP levels.

Table 5-55 MMSYNC command parameters and variables

Command	Parameters and variables
MMSYNC	[<action> {CLEAR, QUERY, SET,<new_value> (10 to 50)}]
Item	**Description**
CLEAR	This variable clears the MTM count.
QUERY	This variable determines the following: • the synchronization and drop synchronization thresholds for MTM • the current MTM count • if the synchronization or drop synchronization threshold for MTM was exceeded
SET	This variable clears the MTM threshold for the MMsync alarm.
<new_value>	This variable specifies the new MMsync alarm threshold for MTMs.

Usage examples

Examples of the MMSYNC command appear in the following table.

Table 5-56 Usage examples of the MMSYNC command

Task	Sample command and output

Clear the MTM count.	**>MAPCI;MTC;CM;MMSYNC CLEAR**
	MAP response example:
	`This command will clear the MTM count. Do you want to continue? (Y/N)`
	>Y
	MAP response example:
	`Matcher Transient Count reset to 0.`
	>N

Query the MTM count.	**>MAPCI;MTC;CM;MMSYNC QUERY**
	MAP response example:
	`The drop sync threshold is: 10`
	`The current MMSYNC threshold is: 10`
	`The current matcher transient mismatch count is: 12`
	`Number of MTM in last 10 minutes: 10`
	`Number of MTM in last 24 hours: 11`
	`The MMSYNC threshold has ben exceeded.`

Table 5-56 Usage examples of the MMSYNC command

Task	Sample command and output
Set the MTM MMsync alarm threshold.	**>MAPCI;MTC;CM;MMSYNC SET 10** *MAP response example:* The threshold you have specified is below the current mismatch count and one more mismatch will cause the MMSYNC alarm to be raised. Do you want to continue? (Y/N) **>Y** The MMSYNC threshold for matcher transients has been set to: 40. The MMSYNC threshold has been set to: 20. This is below the current mismatch count and one more MTM will cause the MMSYNC alarm to be raised. **>N** No action taken.

6 Cards and paddle boards

This chapter describes the following in numeric order:

- DMS SuperNode (SN)
- DMS SuperNode SE computing module (SNSE CM) cards
- paddle boards

DMS SuperNode and SuperNode SE CM card and paddle board descriptions

The SN CM shelf and SNSE CM/system load module (SLM) shelf have cards on the front of the shelf. The SN CM shelf and the SLM shelf have paddle boards that correspond on the back of the shelf. The CM planes have identical circuit cards, paddle boards, and associated hardware. All cards and paddle boards in plane 0 appear in plane 1 in a mirror image. The cards share a common bus with the paddle boards.

Table 6-1 lists all SN and SNSE CM cards and paddle boards.

Table 6-1 SuperNode and SuperNode SE CM cards and paddle boards

PEC	Name	SuperNode	SuperNode SE
NT9X10AA	33-MHz 88100 BRISC CPU card	√	√
NT9X10BA	60-MHz 88110 BRISC CPU card	√	√
NT9X10CA	60-MHz 88110 BRISC CPU card	√	√
NT9X10DA	66-MHz 88110 BRISC CPU card	√	√
NT9X12AB	CPU port card	√	√
NT9X12AC	CPU port card	√	√
NT9X13BB	CPU processor card	√	
NT9X13BC	CPU processor card	√	

Table 6-1 SuperNode and SuperNode SE CM cards and paddle boards

PEC	Name	SuperNode	SuperNode SE
NT9X13GA	CPU processor card	√	
NT9X13HB	CPU processor card		
NT9X13JA	CPU processor card	√	
NT9X13MA	SuperNode SE core CM processor card		√
NT9X13MB	SuperNode SE core CM processor card		√
NT9X14BB	6-Mbyte memory card	√	
NT9X14DB	24-Mbyte memory card	√	√
NT9X14EA	96-Mbyte memory card	√	√
NT9X14FA	96-Mbyte memory card	√	√
NT9X20AA	DS512 paddle board	√	
NT9X21AA	CM-bus terminator paddle board		√
NT9X21AB	Bus terminator paddle board	√	√
NT9X22CA	CM subsystem clock paddle board	√	
NT9X26AA	Reset terminal interface paddle board	√	√
NT9X26AB	Reset terminal interface paddle board	√	
NT9X26DA	BRISC RTIF paddle board	√	
			√
NT9X26DB	BRISC RTIF paddle board	√	√
NT9X26DC	BRISC RTIF paddle board	√	√
NT9X26EA	BRISC RTIF paddle board	√	√
NT9X26FA	BRISC RTIF paddle board	√	√
NT9X26GA	BRISC RTIF paddle board	√	√
NT9X27AA	CM bus extender paddle board	√	

Table 6-1 SuperNode and SuperNode SE CM cards and paddle boards

PEC	Name	SuperNode	SuperNode SE
NT9X27BA	CM bus extender paddle board	√	
NT9X30AA	+5V 86-A power converter	√	
NT9X30AC	Global +5V 86-A power converter	√	
NT9X31AA	-5V 20-A power converter	√	
NT9X10AA	33-MHz 8810 BRISC CPU card	√	
NT9X46AA	Parallel port interface paddle board		√
NT9X62AA	Two-port subrate DS512 paddle board		√
NT9X86AA	Dual-port message controller card		√
NTDX15AA	Power converter +5V		√
NTDX15AB	Global power converter +5V		√

NT9X10 BRISC CPU card

The NT9X10AA BRISC CPU card is based on the Motorola MC88100 group of processors. The functionality of this processor resembles the NT9X13 card. The NT9X10 card has better performance than the NT9X13.

The NT9X10 card provides the following functions:

- Motorola 88100 reduced instruction set computer (RISC) processor
- Motorola 88200 cache and memory management units
- precacher application-specific integrated circuit (ASIC) with circular content addressable buffer (PCCAB)
- high bandwidth code dynamic RAM (DRAM)
- memory bus (M-bus) to external bus interface ASIC
- local M-bus static RAM (LMS)
- trace/interrupt controller (TIC) ASIC
- Bell Northern Research RISC (BRISC) interrupt controller (BIC ASIC)
- DMS-core Maintenance ASIC (DMC)

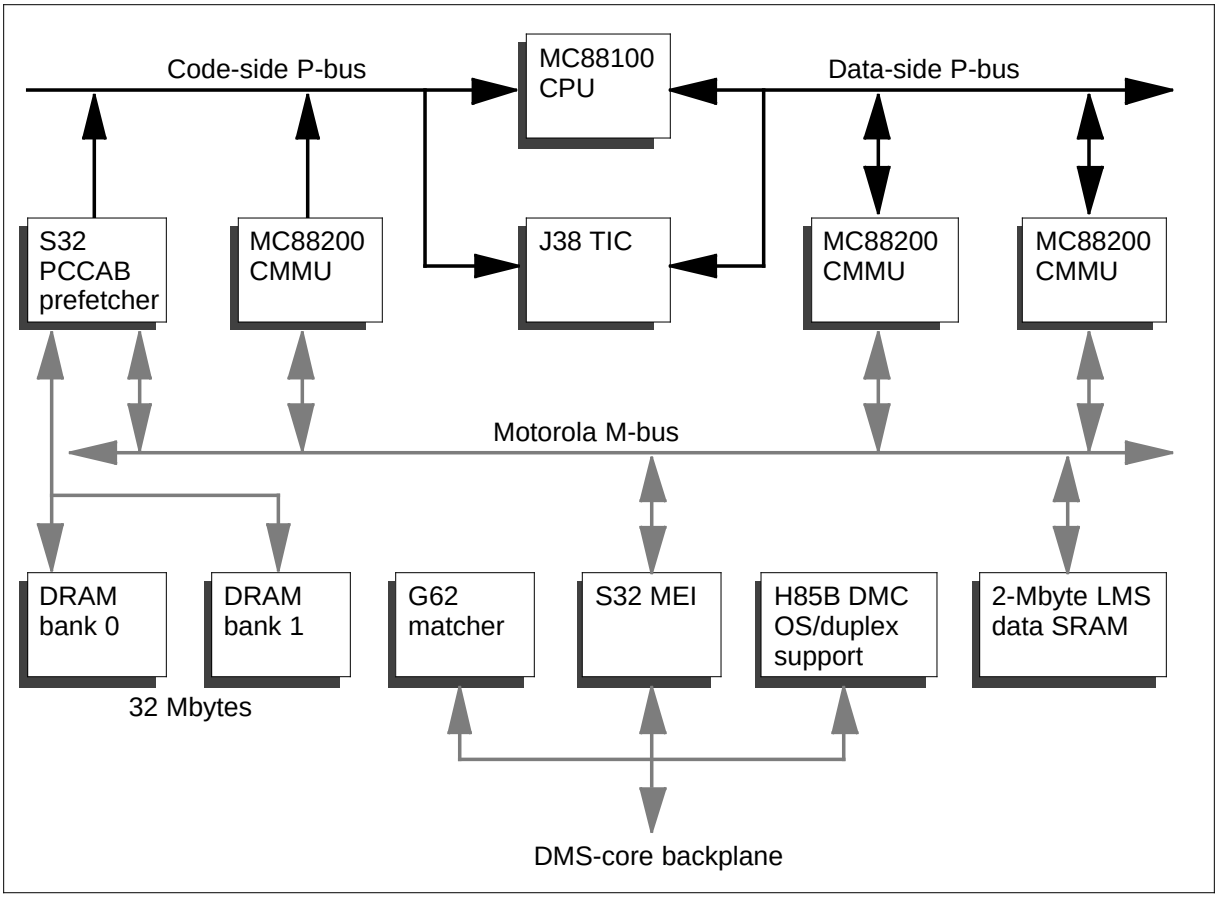
- matcher ASIC (MCH)
- EPROM
- element identification (ID) PROM
- element decode
- clock control
- M-bus arbitration and global status
- Processor bus (P-bus) decoding
- interrupt windowing

NT9X10AA

The CM uses the NT9X10AA BRISC CPU card. The NT9X10AA is based on the Motorola 88100 microprocessor. This microprocessor operated at 33 MHz. The NT9X10AA has 32-Mbyte of cache memory, 2-Mbyte of static RAM (SRAM), and 32-Mbyte of DRAM on board. The card supports SN and SNSE applications.

The following figure shows the architecture of the NT9X10AA BRISC CPU card.

Figure 6-1 NT9X10AA BRISC CPU card architecture



NT9X10BA

The Series 70 SN and SNSE CM user the NT9X10BA BRISC CPU card. The NT9X10BA BRISC SPU card is based on the Motorola 88110 microprocessor. This operates at 60 MHz. The functionality of this processor resembles that of the NT9X13 card. The NT9X10BA card has better performance than the NT9X13. The NT9X10BA acts as a CPU and a memory card. The NT9X10BA contains 256-Mbyte of general purpose (PS and DS) memory (DRAM).

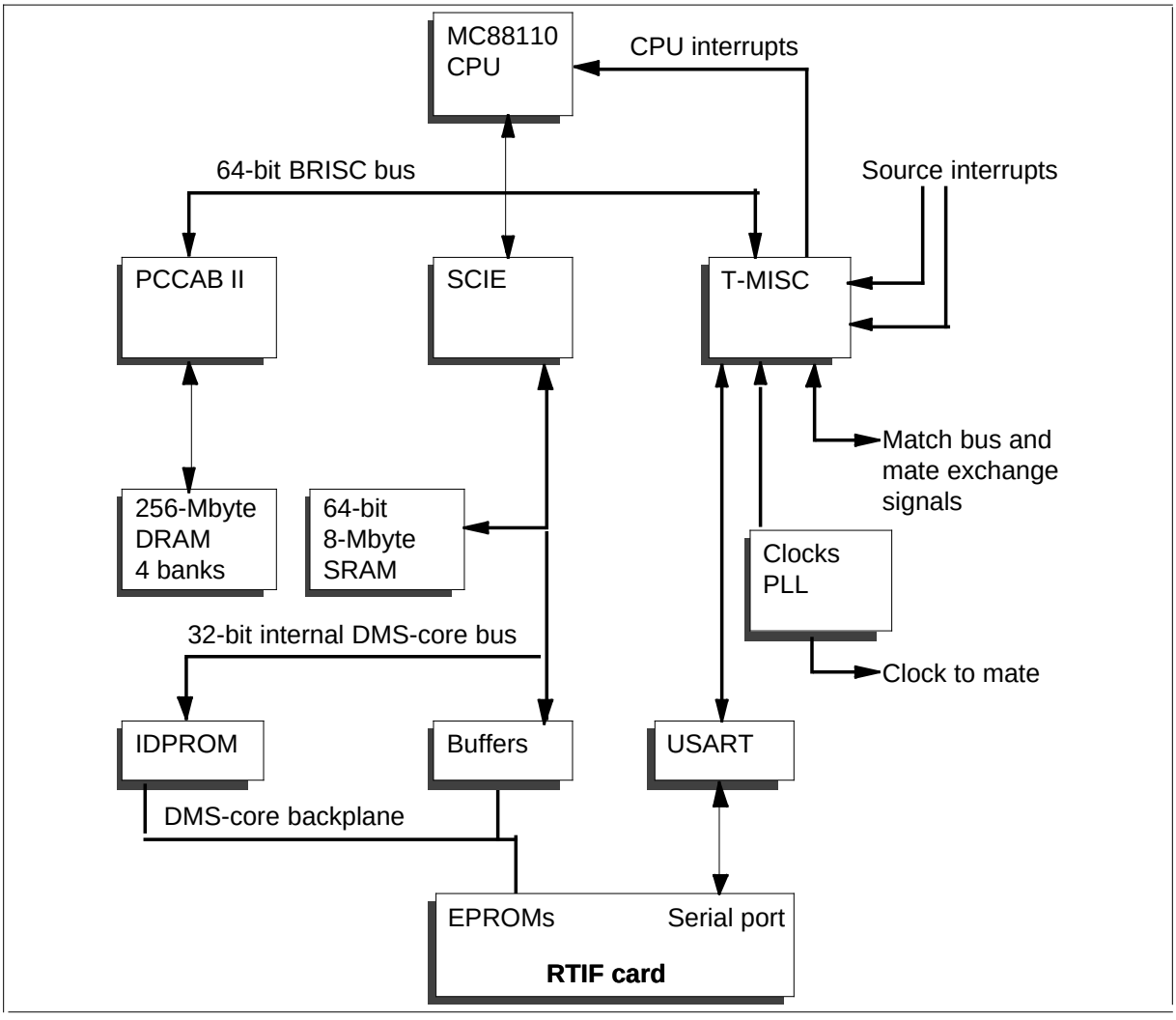
The NT9X10BA card provides the following functions:

- Motorola 88110 RISC processor
- two separate 8-Kbyte internal caches and two memory management units (MMU). One unit is for code and the other unit is for data
- precacher with circular content addressable buffer (PCCABII)
- high bandwidth code DRAM (PCCABII)
- BRISC bus
- tracer/matcher/interrupt synchronization controller (T-MSIC)

- SRAM controller and Interface to ECORE bus ASIC (SCIE)
- DMS-core Maintenance ASIC (DMC)
- EPROM
- clock control
- BRISC-bus control
- JTAG bus master
- interrupt windowing

The following figure shows the architecture of the NT9X10BA BRISC CPU card.

Figure 6-2 NT9X10BA BRISC CPU card architecture

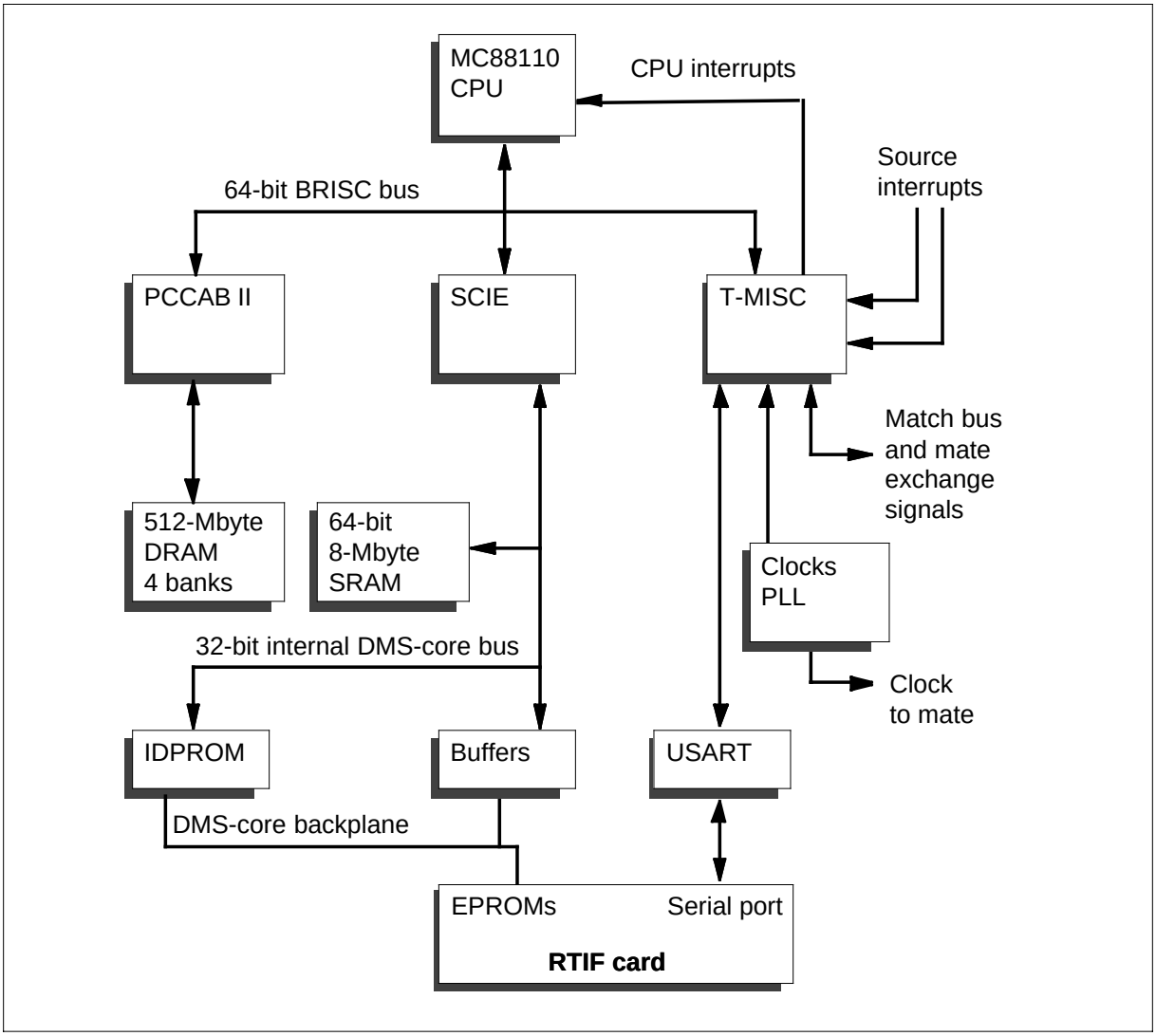


NT9X10CA

The Series 70 EM SuperNode and SuperNode SE CM use, the NT9X10CA BRISC CPU card. The NT9X10CA BRISC CPU card is based on the Motorola 88110 microprocessor. This microprocessor operates at 60 MHz. The functionality of this processor is the same as the NT10XBA. The NT10XCA card has 512-Mbyte PS and DS DRAM. The NT9X10CA card acts as a CPU and a memory card.

The following figure shows the architecture of the NT9X10CA BRISC CPU card.

Figure 6-3 NT9X10CA BRISC CPU card architecture

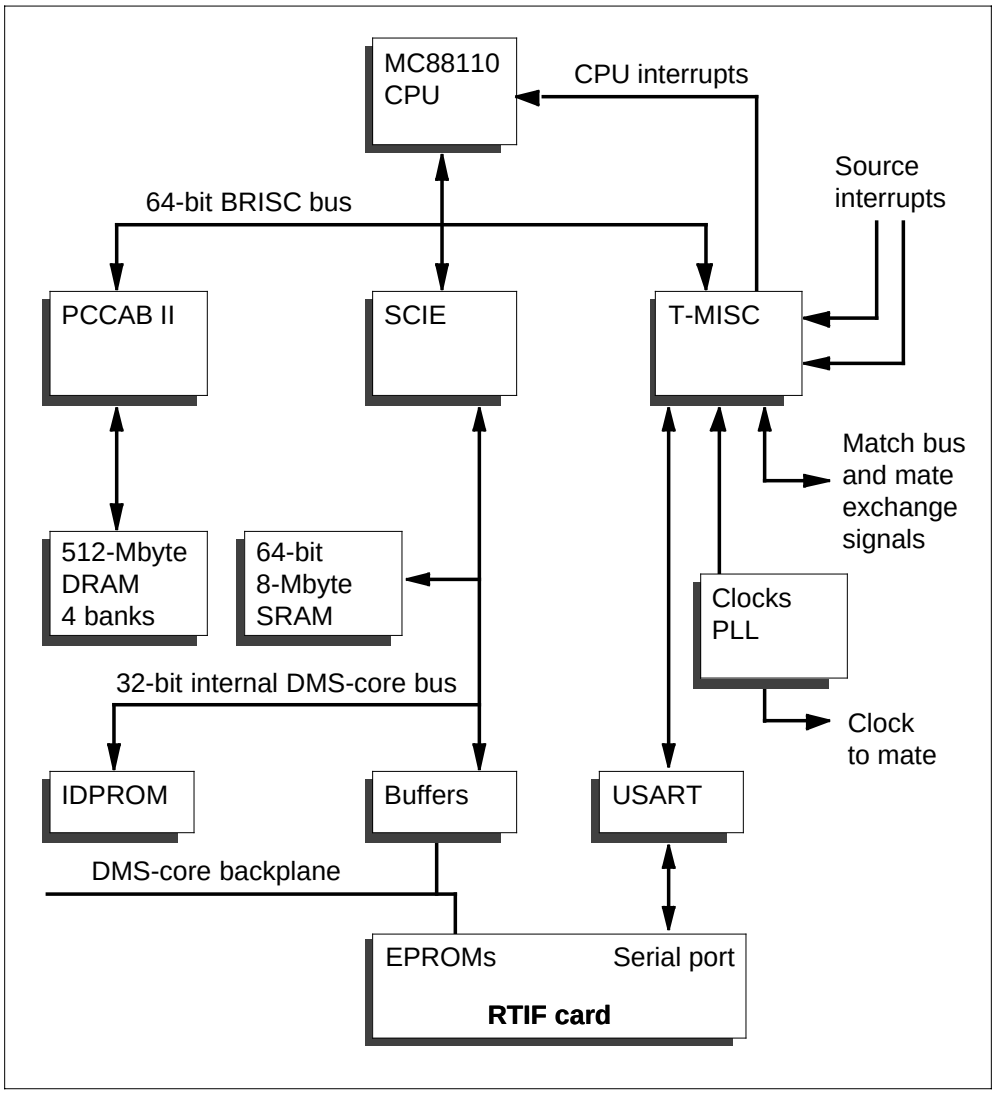


NT9X10DA

The Series 70EM SuperNode and SuperNode SE CM use the NT9X10DA BRISC CPU card. The card uses the Motorola 88110 microprocessor, operated at 66 MHz. The functionality of this processor card is the same as the NT9X10CA card. However, the NT9X10DA CPU card only functions with the NT9X26GA RTIF paddle board and the optional NT9X14FA extended memory card. The NT9X10DA card has 512-Mbyte on-board PCCAB DRAM memory used for code and data store. The NT9X10DA card acts as both a CPU and a memory card.

The following figure shows the architecture of the NT9X10DA BRISC CPU card.

Figure 6-4 NT9X10DA BRISC CPU card architecture



NT9X12 CPU port card

For SuperNode, the NT9X12 single-port message card provides high bandwidth communication between:

- the CM and the message switch (MS)
- the CM and the SLM

For SuperNode SE, the NT9X12 card provides communication between the CM and the SLM. The card supports four link protocols.

The NT9X12 card provides the following functions:

- time-of-day (TOD) clock
- interface to the port crossover bus
- interface port
- split mode destination register (SMDR)
- bus access controller (BAC)
- link handler (LH)x

Time-of-day clock

All clock signals originate in the master clock in the MS. The system sends the signals to the CM subsystem clock (SSC) cards NT9X22. The TOD clock is a 48-bit wide register. The SSC sends a frame pulse that increases the TOD clock. On SuperNode, the CPU scans the TOD clocks on the four MC port cards. The CPU determines the clocks that are within the tolerance level defined by the software. The CPU selects three of the four clocks to use as the CPU timing reference. Loss of all four TOD clocks causes a critical alarm. The alarm indicates that the system is performing procedures, like billing, without a time reference.

Interface to the port crossover bus

The NT9X12 card connects to a crossover bus that links the card to the mate card in the other plane. The card allows the active CPU to access all CPU ports. The active CPU has read/write capability over all in-service (IN SVC) ports. The inactive CPU has read-only capability.

Interface port

The NT9X12 card provides a single interface port. For SuperNode, this card facilitates communication between a CM plane and an MS. For SuperNode and SuperNode SE, the card facilitates communication between a CM plane and an SLM.

Split mode destination register

The SMDR contains a card and a port number for messaging during split mode operations. The firmware on the inactive CPU defines the card and port number when the system enters split mode.

Bus access controller

A BAC gate array controls and coordinates access to the A32-bus with on-board transmit and receive buffers. The BAC scans every address on the A32-bus.

If an address matches the address range the BAC performs the following:

- latches the information from the A32-bus
- places the information in the transmit buffer.

The BAC contains control signals to signal the following:

- to notify the link handler (LH) that the BAC has a message to send
- to notify the NT9X13 or NT9X10 of a message to process

Link handler

The LH is a gate array that supports DS30, DS512 (DMS-Y), DMS-X, and Framer system protocols. To transmit messages, the BAC notifies the LH to remove messages from the transmit buffer and formulate the messages for transmission. To receive messages, the paddle board behind the NT9X12 signals the LH. The signal indicates that a message is present. The LH places the message in a receive buffer and notifies the BAC that the message is pending.

The CM can use the following NT9X12 CPU port cards:

- the NT9X12AB card for SN applications
- the NT9X12AC card for SN and SNSE applications.

The NT9X12AC card is like the NT9X12AB card. The NT9X12AC card adds parity and fault isolation capabilities to the transmit and receive buffers on the card.

NT9X13 CPU card

The NT9X13 CPU card is a high-performance microcomputer card based on the Motorola 68000 group of 32-bit microprocessors. The CPU on the active plane of the switch directs call processing and administrative tasks. Each NT9X13 card stores its own software and a copy of the Support Operating System (SOS) software and the different software of the card in memory. Each CPU has a clock for program instruction sequencing and timing. The active clock drives both CM CPUs for synchronization.

The NT9X13 card contains the following functional blocks:

- CPU
- memory
- bus interface

CPU section

The processor on the NT9X13 card is a Motorola MC68000 series chip.

Memory section

The NT9X13 card contains a limited amount of SRAM. Access to SRAM is faster than access to other types of CM memory.

Bus interface section

The NT9X13 card interfaces with the A32-bus The interface allows communication between the CPUs and other CM components. The CPUs communicate through a dedicated 32-bit bus called the mate exchange bus. The mate communication register (MCR) on each CPU controls the mate exchange bus.

The CM can use the following NT9X13 CPU cards:

- the NT9X13BB series 20 card for SN applications. This card is based on the Motorola MC68020 32-bit microprocessor. This microprocessor operates at 20MHz. This card has 4 kbyte of cache memory and 256 kbyte of SRAM on board.
- the NT9X13BC series 20 card for SN applications. This card is based on the NT9X13BB card. This card uses the E87 version of the 68020 and the H42 version of the memory access unit.
- the NT9X13GA series 30 card for SN applications. This card is based on the Motorola 68030 microprocessor. This microprocessor operates at 33MHz. This card has 32 kbyte of cache memory and 1.5 Mbyte of SRAM on board.
- the NT9X13HB series 40 card for SN applications. This card is based on the Motorola 68030 microprocessor. This microprocessor operates at 40MHz. This card has 32 kbyte of cache memory and 1.5 Mbyte of SRAM on board.
- the NT9X13JA series 20 card for SN applications. This card is based on the NT9X13BC card. The NT9X13JA has a different ID PROM from the NT9X13BC card.
- the NT9X13MA series 20 card for SNSE applications. This card is a recycled board based on the NT9X13BC. This card replaces the H04 maintenance timing and control (MTC) maintenance gate array. The card

replaces the H04 MTC with the H85 DMC DMS maintenance controller gate array. The card does not support the NT9X14EA memory card.

- the NT9X13MB card for SNSE applications. The card has 1-Gbyte access protection. SuperNode SE applications that use NT9X14EA memory cards use the NT9X13MB.

NT9X14 memory card

The NT9X14 memory cards store integrated memory program and data store for operation and call processing. Memory is organized on the MS as it is on the CM; the MS uses an NT9X14 card. For more information on the MS maintenance, refer to the *DMS SuperNode and DMS SuperNode SE Message Switch Maintenance Guide*.

On standard SN switches, the CM shelf holds a maximum of 20 memory cards (10 memory cards for each plane). Operating company requirements determine the number of cards on a CM shelf. On SNSE switches, the CM shelf holds a maximum of 10 memory cards; 5 for each plane.

The CM uses the following NT9X14 memory cards:

- the NT9X14BB card is a 6-Mbyte memory card that supports error checking and correction (ECC) for SN applications. This card has three 2-Mbyte memory modules. Each memory module has a 2X40 array of 256X1 DRAM. Modules are subdivided into banks of 1X40 DRAMs. The 40-bit memory width consists of 32 data bits, seven check bits, and one parity bit.
- the NT9X14DB card is a 24-Mbyte memory card that supports ECC for SN and SNSE applications. The card has three separate 8-Mbyte memory modules. Each memory module consists of a 2X40 array of 256X1 DRAM. Modules are subdivided into banks of 1X40 DRAMs. The 40-bit memory width consists of 32 data bits, 7 check bits, and 1 parity bit.
- The NT9X14EA card is a 96-Mbyte memory card that supports ECC and parity for SN and SNSE applications. This card consists of three 32-Mbyte memory modules. Each module consists of two banks of 44-Mbyte by 1-bit DRAMs. Each bank contains 32 DRAMs for data and 8 DRAMS for the ECC bits. The NT9X14EA card supports the following functions:
  - — allows memory modules to be mapped on a 2-Mbyte limit in MEMBUS address space
  - — retains complete memory contents when a module is moved to a different base address
  - — supports synchronous memory bus (MEMBUS) accesses and high speed, multilongword burst accesses
  - — stores longwords that follow without interruption in alternate memory banks for interleaved burst accesses

— supports page mode for faster accesses when the row addresses of accesses that follow without interruption are the same

— provides software with refresh synchronization control. This software allows memory accesses in handshake override mode with NT9X13 and NT9X10 processors. This software allows software control over refresh staggering on the backplane.

— supports error detection and correction

— corrects all single-bit errors

— detects all single-bit and double-bit errors

— detects errors in a combination of bits in the same NIBBLE (group of 4 bits on a 4-bit limit)

- The NT9X14FA card is a 96-Mbyte memory card that supports ECC and parity. SuperNode and SuperNode SE applications use this card. The NT9X14FA extended memory card only functions with the NT9X10DA CPU card platform. The NT9X14FA card consists of three 32-Mbyte memory modules. Each module consists of two banks of forty 4-Mbyte by 1-bit DRAMs. Each bank contains 32 DRAMs for data, 7 for the ECC bits, and 1 for parity. The card also supports the following functions:

  — allows memory modules to be mapped on any 2-Mbyte boundary in MEMBUS address space

  — retains memory contents intact when a module is moved to a different base address

  — supports synchronous memory bus (MEMBUS) accesses and high speed, multilongword burst accesses

  — stores successive longwords in alternate memory banks for interleaved burst accesses

  — supports page mode for faster accesses when the row addresses of successive accesses are the same

  — provides software with refresh sync control, allowing memory accesses in handshake override mode with NT9X13 and NT9X10 processors

  — enables software control over refresh staggering on the backplane

  — supports error detection and correction

  — corrects all possible single-bit errors

  — detects all possible single-bit and double-bit errors

  — detects errors where any combination of bits in the same nibble (group of 4 bits on a 4-bit boundary) is in error

NT9X20 DS512 interface paddle board

The DS512 interface paddle board provides parallel-to-serial and serial-to-parallel message conversion for the CM subsystem on a standard SN switch. (SNSE uses the NT9X62 dual-link SR512 interface paddle board for message conversion).

Each NT9X20 connects to a CPU port card (NT9X12) and two fiber optic cables. Each fiber optic cable is a one-way transmission path. One cable transmits signals, and the other receives signals. The upper port connection always transmits signals and the lower port connection always receives signals.

The interface to the port card is a shorting bus (S-bus), that runs at an average rate of 4.088 Mword/s or less. The S-bus is divided into in-band and out-of-band (OOB) segments. The in-band segment consists of eight bits that carry the messaging information to or from the link handlers on port cards. The remaining two OOB bits carry system reset information.

The NT9X20 has a bidirectional P-bus, that provides access to read and write registers on the paddle board. The following process use these registers:

- initialization
- maintenance activities
- system reset requirements

When the CM sends a message to the MS, the NT9X20 interface paddle board performs the following functions:

- encodes the 10-bit message into 12-bit signals
- converts the message from parallel to serial
- changes the message from an electrical signal to an optical signal

When the CM receives a message from the MS, the NT9X20 interface paddle board performs the following functions:

- changes the message from an optical signal to an electrical signal
- converts the message from serial to parallel
- encodes the 12-bit signals into a 10-bit message

Out-of-band system resets

To transmit a reset, the NT9X20 receives OOB information from the A32-bus in parallel form through the NT9X12 card. The BAC or LH do not process the OOB information. The NT9X20 card separates OOB information from message data. The card sends OOB reset information along the backplane to the reset paddle board.

Messaging links between the CM and the MS for SuperNode applications use the NT9X20AA card.

NT9X21 bus terminator paddle board

The NT9X21 bus terminator provides resistance to terminate signals without an address on the 12-layer backplane. The NT9X21 keeps the A32 buses free of additional noise or interference. This paddle board extends parts of the A32 bus to power converters. These extensions provide CPU access to power converter IDPROMs.

SN and SNSE applications use the NT9X21AA and the NT9X21AB bus terminator paddle boards.

NT9X22 subsystem clock paddle board

The NT9X22 subsystem clock (SSC) paddle board produces a 16.384-MHz synchronous clock signal for each SN CM plane. This paddle board provides an 8-kHz frame pulse signal that synchronizes frames and channels to transmit and receive messages. The system sends the frame pulse signals to the NT9X12 CPU port circuit cards for message buffering.

The SSC on the SNSE is on the NT9X62 paddle board. The SSC on the SNSE provides the same functionality as the SSC on the SN.

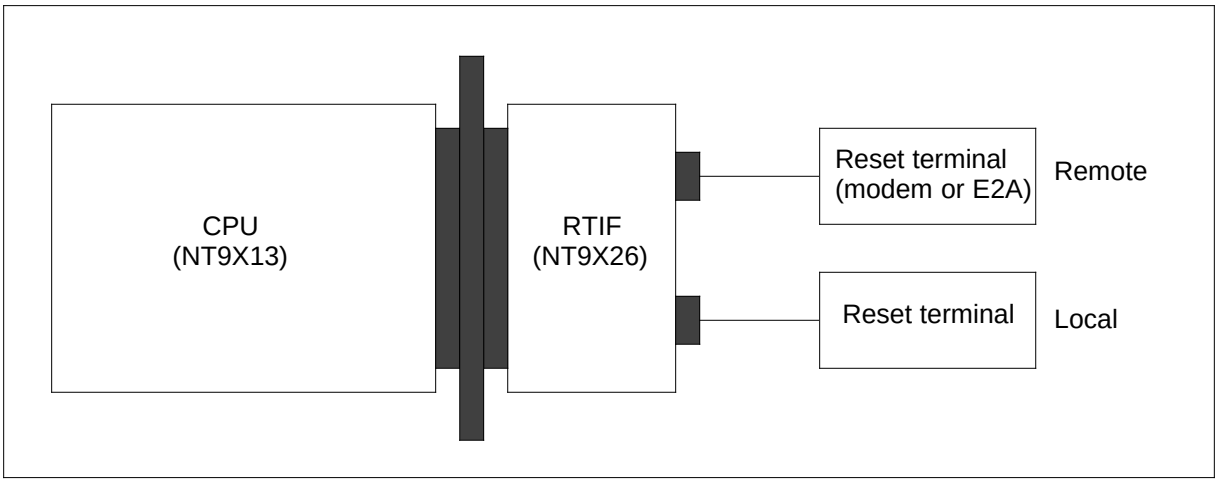
The SN applications use NT9X22CA SSC paddle board.

NT9X26 reset terminal interface paddle board

The reset terminal interface (RTIF) paddle board is a microprocessor-based controller that communicates with the associated CPU and reset terminal. The RTIF is located behind a CPU card and is part of the reset control subsystem.

The RTIF paddle boards have two RS-232 ports. The lower port connects to the local reset terminal and has a baud rate of 9600 bit/s. The upper port configures as a remote RTIF modem or E2A. The port configuration appears in the following figure.

Figure 6-5 Reset terminal interface ports



The NT9X26 card contains the OOB link interface that collects OOB reset code bits. The system assembles the bits and sends them to the CPU of the RTIF. This CPU determines the type of reset to perform. The RTIF contains a CPU, RAM, and EPROM. The OOB link between modules allows the CM to reset other nodes.

The RTIF E2A provides the following functions:

- a serial data link that connects the CPU to an E2A digital alarm scanner (DAS)
- remote monitoring of the CPU card status
- remote monitoring of the control lines on the CPU card
- remote control of the CPUs

Reset terminal operation

The reset terminal operates in normal mode or command collection mode. In normal operation, the terminal is transparent to the processor. Operating company personnel enter a backslash (\ ) character to place the terminal in command collection mode. The command collection mode allows operating company personnel to enter RTIF commands.

The CM can use the following NT9X26 reset terminal interface paddle boards:

- The NT9X26AA RTIF paddle board controls the NT9X13BC and NT9X13MA CPU cards.
- The NT9X26AB board performs the same functions as the NT9X26AA board.

- The NT9X26DA BRISC RTIF paddle board incorporates the features of all RTIF paddle boards. This board provides firmware support to the NT9X10AA CPU cards on SuperNode switches.
- The NT9X26DB BRISC RTIF paddle board contains firmware that supports the NT9X10AA BRISC CPU card on SuperNode SE switches.
- The NT9X26DC BRISC RTIF paddle board contains firmware that supports the SuperNode 50MX product.
- The NT9X26EA BRISC RTIF paddle board contains firmware that supports the NT9X10BA BRISC CPU card on Series 70 SuperNode and SuperNode SE switches.
- The NT9X26FA BRISC RTIF paddle board contains firmware that supports the NT9X10CA BRISC CPU card on Series 70EM SuperNode and SuperNode SE switches.
- The NT9X26GA BRISC RTIF paddle board contains firmware that supports the NT9X10DA BRISC CPU card on Series 70EM SuperNode and SuperNode SE switches.

NT9X27 bus extender paddle board

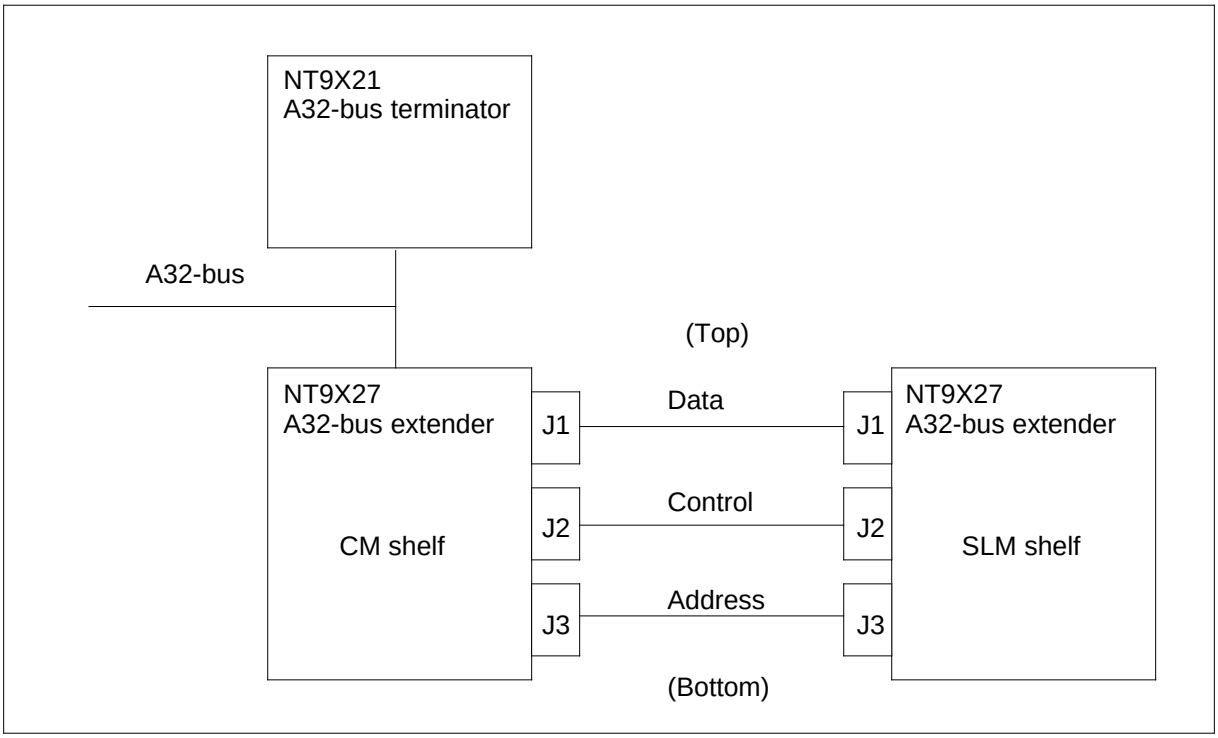
The SN switch uses NT9X27 bus extender paddle boards to extend the A32 bus between the CM and the SLM shelf. Each side of the switch contains one pair of paddle boards. One paddle board in each pair is in the CM shelf, the other paddleboard is in the SLM shelf.

The following cables connect the paddle board pairs:

- J1 (data)
- J2 (control)
- J3 (address)

The following figure shows the connections.

Figure 6-6 NT9X27 bus extender paddle board connections



The CM can use the following NT9X27 bus extender paddle boards:

- The CM shelf uses the NT9X27AA paddle board.
- The SLM shelf uses the NT9X27AB paddle board.

NT9X30 +5V power converter card

The NT9X30 power converters regulate the -48V office voltage and provide +5V dc to the CM shelf on a standard SuperNode switch.

Each power converter has a set of test points which the operating company personnel can use to check operating parameters. Operating company personnel must use a digital voltmeter, because the internal resistance of analog meters affects the readings. For more information, refer to *Routine Maintenance Procedures*

The CM uses the following NT9X30 +5V power converter cards:

- North American SuperNode applications use the NT9X30AA card.
- International SuperNode applications use the NT9X30AC card.

NT9X31 -5V power converter

The NT9X31 power converters provide -5V dc at a maximum current of 20A.

Power converters have a set of test points which the operating company personnel can use to check operating parameters. Operating company personnel must use a digital voltmeter because internal resistance of analog meters, affects the readings. For more information, refer to *Routine Maintenance Procedures*

The CM supports the following NT9X31 -5V power converter cards:

- North American SuperNode applications use the NT9X31AA card.
- International SuperNode applications use the NT9X31AB card.

NT9X46 parallel port interface paddle board

The SN and SNSE switches use NT9X46 parallel port interface paddle boards in pairs. These paddle boards provide the communication link between each CM plane and the associated SLM. An interconnect cable that functions as an S-bus links each paddle board pair.

The SLM shelf uses NT9X46 paddle board pairs for SN. The CM part of the CM/SLM shelf contains one paddle board in each pair for SuperNode SE. The SLM part of the shelf contains the other paddle board.

The SNSE applications use the NT9X46AA parallel port interface paddle board.

NT9X62 SR512 paddle board

The dual-port subrate DS512 (SR512) paddle board provides an interface between the NT9X86 and two SR512 optical links. The dual-port subrate DS512 (SR512) paddle board does this with the dual-port subrate message controller card NT9X86 on SuperNode SE. The SR512 paddle board houses the circuit for the subsystem clock. The 16.384-MHz clock and 8-kHz frame pulses lock to a reference frame pulse extracted from one of the SR512 optical links.

The SNSE applications use the NT9X62AA SR512 parallel port interface paddle board.

NT9X86 dual-port message controller card

The NT9X86 dual-port message controller card performs the following functions:

- provides high bandwidth communication between the CM and MS
- houses the circuit for the local TOD clock
- provides the interface for the port cross-over bus so that both CPUs can access all ports.

SuperNode SE applications use the NT9X86AA dual-port message controller card.

NTDX15 power converter card

The NTDX15 power converter provides +5V dc and -5V dc to the CM part of the SuperNode SE CM/SLM shelf.

Each power converter has a set of test points which the operating company personnel can use to check operating parameters. Operating company personnel must use a digital voltmeter because the internal resistance of analog meters, impacts on the readings. For more information, refer to *Routine Maintenance Procedures*.

The CM uses the following NTDX15 power converter cards:

- North American SNSE applications use the NDX15AA.
- International SNSE applications use the NDX15AB.

7 Trouble isolation tools

This chapter describes the tools that troubleshoot fault conditions on the DMS SuperNode (SN) and DMS SuperNode SE (SNSE) computing module (CM). For information on nonresident tools, refer to the Technical Assistance Manuals.

Diagnostic tools

This chapter describes the following diagnostic tools:

- alarms
- DMS monitoring (DMSMON) tool
- log reports
- manual maintenance test (MTCTST)
- morning report of the maintenance manager (AMREPORT)
- MMINFO
- OM-log-alarm cross reference charts
- operational measurements (OM)
- Sherlock
- switch performance monitoring system (SPMS)
- TRAPINFO

Alarms

Alarms indicate system problems and provide information about the following types of problems:

- equipment failure
- equipment operating at degraded level
- equipment that has reached operating company defined capacity level
- loss of synchronization
- full or partial system sanity

- software errors
- failed automatic recovery attempt
- reboot that is not authorized
- auto transfer to standby
- cannot transfer from have faults to standby
- loss of communication between entities or subsystems
- loss of ability to store operational information (data exceeds threshold)
- inter-node transmission failure
- loss of communication with operation support systems
- power distribution failure
- security violations
- fire and intrusion

The alarms have three levels of seriousness: minor, major, and critical.

A minor alarm indicates a problem that causes a small loss of service. Examples of minor alarm conditions include the following:

- conditions that can cause a major alarm if the user does not correct the conditions
- the system made one piece of a pool of equipment busy
- service degradation below an operating company defined threshold

A major alarm means one-half of a duplicated system is out of service. This condition can cause a large loss of service. Backup is not available if another fault occurs on the active system. This alarm can also occur if service degrades below an operating company defined threshold can also generate this alarm level.

A critical alarm indicates a problem that results in an important loss of service. Examples of critical alarm conditions include the following:

- loss of call processing capability (dead system)
- part or full loss of system sanity
- service degradation to below an operating company defined threshold

A log accompanies each alarm. The logs provide information about conditions in the switch.

The CM header of the MTC level MAP display shows CM system alarms. See the chapter 8, "Troubleshooting charts" on page -1 for a list of all CM alarms

and possible CM alarm causes. The chapter "Troubleshooting charts" also indicates where to find information to clear each alarm.

DMSMON

The DMS monitoring tool (DMSMON) monitors changes in operation when operating company personnel change a release load. The DMSMON formats this information in to a report that the user can generate manually or automatically. The type of information in the report includes the following:

- counts of internal events (warm and cold restarts) and downtime information
- system trap information
- counts of various log occurrences
- hardware counts (configuration information)

For more information about the DMSMON tool, refer to the *DMS Family Commands Reference Manual*.

Log reports

Log reports are a primary source of information about the components of the CM. Some logs can isolate a problem to a single component. Other logs identify problems that are the result of more than one component.

Log reports include the following information:

- severity of the log (represented by number of asterisks)
- type of log
- time and date
- suspected problem
- list of suspected cards

See Chapter 3, "Logs" on page -1 of this document for information about the CM-related logs.

MTCTST

Perform manual maintenance test (MTCTST) to detect faults on new hardware installations or hardware that may have faults. The MTCTST test executes CPU and memory tests on an inactive CPU on the CM. The MTCTST does not execute a SWACT.

Refer to *Trouble Locating and Clearing Procedures* for more information about MTCTST.

Maintenance manager's morning report

AMREPORT provides a 24-h summary of performance, administrative, and maintenance information. Corrective and preventative programs can use this information. The AMREPORT log includes the following information:

- switch performance information
  - — SPMS indicators
  - — call processing performance
  - — CPU occupancy
  - — network integrity
  - — peripheral module (PM) switch of activity (SWACT) information
  - — software performance: trap and swerr counts
  - — footprint (FP) and OM log counts
  - — XMS-based peripheral module (XPM) SWACT information
- scheduled test results
  - — automatic line test (ALT)
  - — automatic trunk test (ATT)
- switch operations
  - — image dump results
  - — patch summary
  - — outage indicators
  - — table data integrity check
  - — unscheduled XPM REx test

Refer to the *Digital Switching Systems DMS-100 Family Maintenance Managers Morning Report* for more information about AMREPORT.

MMINFO

MMINFO is a Command Interface (CI) tool that consolidates, manages, and displays mismatch information in an easy-to-read format. The MMINFO performs the following functions:

- management of the mismatch information database
- generation of MMINFO reports on request

When the user enters a MMINFO CI command, the system records a snapshot of the database. The system copies the snapshot into a local database version. The MMINFO database accommodates a maximum of 20 entries for the Series

20 to 60 SN. The database accommodates a maximum number of 10 entries for the Series 70 SN.

See the "User Interface and Commands" chapter in this document for more information about the MMINFO tool. See the "Mismatch analysis" chapter of this document for more information about CM mismatch analysis.

OM-log-alarm cross-reference charts

The "Troubleshooting charts" chapter of this document contains a set of three charts relating to OMs, logs, and alarms. Each chart uses an indicator as the key, so that operating company personnel can find all associated information.

Operational measurements

The OMs provide load and performance information. The OM system controls collection, display, and generation of OM data for the operating company.

See Chapter 4, "Operational measurements" on page -1 of this document for information about CM-related OMs.

Sherlock

Sherlock is a data collection tool designed for use after a service outage. Sherlock automatically collects the data required to analyze the cause of failure. Only one person at a time can use Sherlock.

Sherlock initiates a set of parallel processes that collect all available data for the type of service failure. The system sends the data to a series of temporary files. Operating company personnel cannot access or manipulate the files unless you stop the Sherlock process before data collection completes.

When data collection is complete, the system creates a data file and a console file on the storage device and erases the temporary files. The system calls the file that contains the data SHRKyymmddhhmmss(Z) and calls the console file SHERLOCK$OUT. The console file contains all the messages and responses sent to the terminal, and some additional messages.

Refer to the *DMS Family Commands Reference Manual* for more information about how to use Sherlock.

Switch performance monitoring system

The Switch performance monitoring system (SPMS) monitors all areas of switch operation and produces reports on performance from several points of view. The system provides a medium-term review with reports that consist of detailed and summary level data.

The SPMS bases the reports on a wide range of index values computed from OMs the switch generates. The time period covered in each report ranges from

half-an-hour to a month. You can monitor day-to-day events, and also receive a longer-term view of switch performance.

Switch performance index plans can refer to SPMS results for administrative purposes. The operating company can use the overall office performance index, any section of lower-level indexes, or both.

The SPMS consists of three sections: the service section, the maintenance performance section, and the provisionable resources section. Refer to the *Switch Performance Monitoring System Application Guide*, for more information on SPMS.

TRAPINFO

TRAPINFO is a tool that extracts information about software traps from the log utility and displays the information.

Refer to the*DMS Family Commands Reference Manual* for more information about the TRAPINFO tool. See the procedure , "Responding to a CMTrap alarm" on page -2 for more information about traps.

8 Troubleshooting charts

This chapter contains seven charts designed to help operating company personnel. The charts helps operating company personnel find information to clear alarmed and nonalarmed trouble conditions in the computing module (CM).

CM alarm and trouble condition procedures

The following table lists CM-related alarmed and nonalarmed conditions. The table also describes the causes of each alarm or condition. This table provides the location of the alarm clearing or trouble loading procedures for each alarm or condition.

Table 8-1 Computing module alarms and trouble conditions

Condition	Possible cause	Action
Critical alarms		
IMAGE	Software load on inactive central processing unit (CPU) cannot maintain a restart.	See the "Advanced troubleshooting procedures" chapter in this document.
LowMem	There is no spare memory left in the CM.	See the LowMem critical alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
NoTOD	There is no accurate time of day (TOD) source available for one of the following reasons: • MC Tbl condition • loss of reference on both TOD clocks.	See the NoTOD critical alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
StrAlc	Memory capacity reached defined limits.	See the section on Memory allocation limits in this chapter and the "Advanced troubleshooting procedures" chapter in this document.

Table 8-1 Computing module alarms and trouble conditions

Condition	Possible cause	Action
Major alarms		
CBsyMC	Both message controller (MC) links to the message system (MS) are out of service for one of the following reasons: • hardware fault in the MS affecting both links • hardware fault in the MC affecting both links • manual busy (MBsy) MS • running in split mode (SNSE)	See the CBsyMC major alarm clearing procedure in *Alarm and Performance Monitoring Procedures*. See the "Advanced troubleshooting procedures" chapter in this document.
CLKFlt	Processor clock fault (CLK Flt) is present.	See the CLK Flt major alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
CM Flt	One of the following faults is present in one of the processor card components: • CLK Flt • E2A interface • found by REx • processor fault • memory fault	See the CM Flt major alarm clearing procedure in *Alarm and Performance Monitoring Procedures* See the "Advanced troubleshooting procedures" chapter in this document.
CM Trap	Trap rate approaches threshold and can cause a warm restart.	See the "Advanced troubleshooting procedures" chapter in this document.
LOWSpr	Spare memory of both CPUs is low.	See the LOWSpr major alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
MBsyMC	MC is manual busy (MBsy).	See the MBsyMC major alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
MMnoSyc	Switch is out of synchronization when the number of mismatches exceeds a threshold.	See the MMnoSync alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.

Table 8-1 Computing module alarms and trouble conditions

Condition	Possible cause	Action
Major alarms continued		
MMSync	A fault mismatch occurred and the mismatch recovery process put the CM back in synchronization.	See the MMSync alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
NoSYNC	CPUs are out of synchronization for one of the following reasons: • CPU under test • memory fault • MC fault • manually initiated • running in split mode • processor selection mismatch	See the NoSYNC major alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
PMCFlt	Both PMC ports are out of service for one of the following reasons: • MBsy • pbsy (SLM out of service) • SBsy hard fault	See the PMCFlt major alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
PrcOpt	Processor card product engineering code (PEC) and optional datafill do not match.	See the "Advanced troubleshooting procedures" chapter in this document.
RExFlt	Scheduled REx testing failed to complete.	See the "Advanced troubleshooting procedures" chapter in this document.
SBsyMC	MC is out of service for one of the following reasons: • hard fault • SSC fault.	See the SBsyMC major alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
SLMLIM	Image is too large to dump to system load module (SLM) tape. Two CM loads this size cannot fit on a SLM disk.	The SLM can require an upgrade to a larger size to clear this alarm. See tables 8-6 and 8-7 to determine the SLM trigger points and capacities. See the SLM link interface module (LIM) major alarm clearing procedure and NT9X44 card replacement in *Card Replacement Procedures*.

Table 8-1 Computing module alarms and trouble conditions

Condition	Possible cause	Action
Major alarms continued		
SRAMFL	The 48-hour SRAM fault counter reaches the maximum threshold of two. You must replace the affected processor card.	See the SRAMFL alarm clearing procedure in the CM alarm clearing document that applies to the system you use.
Minor alarms		
Autold	Problem or error will prevent automatic reload of the switch.	See the "Advanced troubleshooting procedures" chapter in this document.
E2A	E2A links to RTIF are not in service for one of the following reasons: • link not stable or disconnected • link not enabled.	See the E2A minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
EccOn	CM is synchronized, Memory error checking and correction is on.	Refer to the EccOn minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*. Does not apply on Series 70 SuperNode.
JInact	Inactive CPU is jammed.	Refer to the JInact minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
LowSpr	Spare memory of one CPU is low.	Refer to the LowSpr minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*
MC Tbl	MC is in trouble for one of the following reasons: • MC port out-of-service • MS computing module interface card (CMIC) port out of service • link between MC port and MS port is out-of-service • SSC has faults • time of day (TOD) clock has faults • running in split mode SN.	Refer to the MC Tbl minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.

Table 8-1 Computing module alarms and trouble conditions

Condition	Possible cause	Action
Minor alarms continued		
MemCfg	Memory card configuration on one of the CM planes is not valid.	Refer to the MemCfg minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*
MemFlt	Number of memory fault correctable (MFC) events exceeds a threshold for one of the following: • memory module • memory card • plane of the CM	Refer to the MemFlt minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
MemLim	Memory allocation to the operating system reached approximately 90% of the limit for the platform.	Refer to the memory limit (MemLim) minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*
NoBrst	CM is in synchronization. The no-burst (NoBrst) option is enabled.	Refer to the NoBrst minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*
NoOvr	Synchronization entered with nohands option.	Refer to the NoOvr minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*
PMCTbl	PMC is in-service trouble, (one port out-of-service) for one of the following reasons: • pbsy port (SLM out of-service) • MBsy port • SBsy port (hard fault).	Refer to the PMCTbl minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.
RExSch	The system cancels two consecutive automatic REx tests. Datafill in table REXSCHED disables CM REx testing.	See the "Advanced troubleshooting procedures" chapter in this document.
RExTst	A REx test is in effect.	Refer to the RExTst minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*.

Table 8-1 Computing module alarms and trouble conditions

Condition	Possible cause	Action
Minor alarms continued		
SLMLim	Image approaches a size too large to dump to SLM tape. Two CM loads of this size cannot fit on the SLM disk.	The SLM can require an upgrade to a larger size to clear this alarm. See tables 8-6 and 8-7 to determine the SLM trigger points and capacities. Refer to the SLMLim minor alarm clearing procedure in *Alarm and Performance Monitoring Procedures*. and the NT9X44 card replacement in *Card Replacement Procedures*.
SRAMFl	The 48 h SRAM fault counter reaches the minor alarm threshold of one.	If no additional SRAM faults occur in 48 h, the alarm clears automatically. If additional SRAM faults occur within 48 h, the alarm escalates to a major SRAMFL alarm. The major alarm indicates that the affected processor card requires replacement. The CM alarm clearing document for the system provides detailed procedures for clearing SRAMFl minor and SRAMFL major alarms.
Nonalarmed trouble conditions		
CM160 logs	Invalid card installed.	Refer to the procedure Correcting release mismatch problems in *Trouble Locating and Clearing*.
MM logs		See the "Mismatch analysis" chapter in this document.
Cooling fan failure		See one of the following procedures in *Trouble Locating and Clearing*: • Replacing a cooling unit assembly • Replacing a cooling unit electronic module • Replacing a cooling unit fan • Replacing an NT9X95 card in a cooling unit.

OM-log-alarm cross reference charts

Table 8-2, "OM-log-alarm cross reference chart" on page 8-7, Table 8-3, "Log-OM-alarm cross reference chart" on page 8-8, and Table 8-4,

"Alarm-log-OM cross reference chart" on page 8-12 list CM-related logs, operational measurement OMs, and alarms. Each table describes one of the three indicators. Each table cross-references and maps the indicator to the two other indicators.

The following table maps CM-related OMs to the associated log reports and alarms.

Table 8-2 OM-log-alarm cross reference chart

OM group	Register	Associated logs	Associated alarms
CM	CMCPUFLT	CM125	CM FLT
	CMDPSYNC	MM100, MM101, CM101, CM102, CM159	NoSYNC
	CMMCINIT	CM120	none
	CMMCSBSY	CM104	SBsyMC
	CMMEMFLT	CM112	MemFlt
	CMMSMPXU	CM102	NoSYNC
	CMMSWACT	CM101	none
	CMMWINIT	CM120	none
	CMRCPUFL	CM122, CM179	CM Flt
	CMREXFLT	CM122, CM179	CM Flt
	CMRLNKFL	CM122, CM179	CM Flt
	CMRMCFL	CM122	CM Flt
	CMRMEMFL	CM122, CM179	CM Flt
	CMRPMCFL	CM122, CM179	CM Flt
	CMRSMPXU	CM102	none
	CMRSSCFL	CM122	CM Flt
	CMRSWACT	CM101	none
	CMSCINIT	CM120	none
	CMSSCFLT	CM145	MCTbl

Table 8-2 OM-log-alarm cross reference chart

OM group	Register	Associated logs	Associated alarms
	CMSSMPXU	CM102	NoSYNC
	CMSSWACT	CM101	none
	CMSWINIT	CM120	none
	CMTRAP	CM103, CM119	CMTrap
	CMTRMISM	MM101	none
	PMCLKBSY	CM137	PMCTbl
	PMCNDBSY	CM133	PMCFlt

The following table maps CM-related logs to the associated OMs and alarms.

Table 8-3 Log-OM-alarm cross reference chart

Log	Associated OMs	Associated alarms
CM100	none	none
CM101	CMDPSYNC, CMMSWACT, CMRSWACT, CMSSWACT	NoSYNC, JInact
CM102	CMMSXPXU, CMRSMPXU, CMSSMPXU	NoSYNC, RExTst
CM103	CMTRAP	CMTrap
CM104	CMMCSBSY	SBsyMC
CM105	none	CBsyMC
CM106	none	MBsyMC
CM107	none	MCTbl
CM108	none	none
CM109	none	MCTbl
CM110	none	MCTbl
CM111	none	LowMem

Table 8-3 Log-OM-alarm cross reference chart

Log	Associated OMs	Associated alarms
CM112	CMMEMFLT	MemFlt
CM113	none	MemFlt
CM114	none	none
CM115	none	NoTOD
CM116	none	IMAGE
CM117	none	none
CM118	none	none
CM119	CMTRAP	CMTrap
CM120	CMMCINIT, CMMWINIT, CMSCINIT, CMSWINIT	RExTst
CM121 (application processors only)	none	CMFlt
CM122 (application processors only)	CMRCPUFL, CMREXFLT, CMRLNKFL, CMRMCFL, CMRMEMFL, CMRPMCFL, CMRSSCRL	LOWSpr, LowSpr
CM123	none	none
CM124	none	none
CM125	CMCPUFLT	CMFlt
CM126	none	none
CM127	none	none
CM128	none	none
CM129	none	MCTbl
CM130	none	none
CM131	none	Autold
CM132	none	PMCFlt

Table 8-3 Log-OM-alarm cross reference chart

Log	Associated OMs	Associated alarms
CM133	PMCNDBSY	PMCFlt
CM134	none	PMCTbl
CM135	none	
CM136	none	PMCTbl
CM137	PMCLKBSY	PMCTbl
CM138	none	none
CM139	none	none
CM140	none	none
CM141	none	none
CM142	none	PMCFlt
CM143	none	PMCTbl
CM144	none	none
CM145	CMSSCFLT	MCTbl
CM146	none	RExSch
CM147	none	PMCTbl
CM148	none	PMCTbl
CM149	none	none
CM150	none	none
CM151	none	none
CM152	none	none
CM153	none	MCTbl
CM154	none	RExSch
CM155	none	none
CM156	none	none
CM157	none	none
CM158	none	LOWSpr, LowSpr

Table 8-3 Log-OM-alarm cross reference chart

Log	Associated OMs	Associated alarms
CM159	CMDPSYNC	NoSYNC
CM160	none	CMFlt
CM162	none	CLKFlt, CMFlt
CM163	none	CMFlt
CM164	none	none
CM165	none	PrcOpt
CM166	none	none
CM167	none	none
CM168	none	SRAMFl minor
CM169	none	SRAMFl major
CM170	none	none
CM171	none	none
CM172	none	none
CM173	none	none
CM174	none	MemCfg
CM175	none	MemLim
CM176	none	none
CM177	none	none
CM178	none	SLMlim
CM179	CMREXFLT, CMRCPUFLT, CMRMEMFLT, CMRPMCFLT, CMRLNKFLT	CM Flt, REx Tst
CM180	none	SLMLIM
CM181	none	StrAlc
CMSM101	none	none

Table 8-3 Log-OM-alarm cross reference chart

Log	Associated OMs	Associated alarms
CMSM102	none	none
CMSM103	none	none
CMSM104	none	none
FP100	none	none
FP101	none	none
FP102	none	none
FP103	none	none
FP104	none	none
MFC100	none	none
MFC110	none	none
MFC111	none	MemFlt
MM100	DPSYNC	NoSYNC
MM110		MMSync
MM111		MMNoSync
MM112		MMNoSync
MM113		MMNoSync

The following table maps CM alarms to the associated logs and OMs.

Table 8-4 Alarm-log-OM cross reference chart

Alarm	Associated logs	Associated OMs
Autold	CM131	none
CBsyMC	CM105	none
CLKFlt	CM162	none
CMFlt	CM125, CM122, CM160, CM162, CM163	CMCPUFLT, CMRCPUFL, CMREXFLT, CMRLNKFL, CMRMCFL, CMRMEMFL, CMRPMCFL, CMRSSCFL
CM Mnt	CM174	none

Table 8-4 Alarm-log-OM cross reference chart

Alarm	Associated logs	Associated OMs
CMTrap	CM103, CM119	CMTRAP
E2A	CM163	none
EccOn	none	none
IMAGE	CM116	none
JInact	none	none
LowMem	CM111	none
LOWSpr	CM123, CM158	none
LowSpr	CM123, CM158	none
MBsyMC	CM106	none
MC Tbl	CM107, CM109, CM110, CM129, CM145, CM153	CMSSCFLT
MemCfg	CM174	none
MemFlt	MFC111	none
	CM112	CMMEMFLT
MemLim	CM175	none
MMnoSync	MM111, MM112, MM113	none
MMSync	MM110	none
NoBrst	none	none
NoOvr	none	none
NoSYNC	CM101, CM102, CM159	CMDPSYNC, CMMSMPXE, CMSSMPXU
NoTOD	CM115	none
PMCFlt	CM132, CM133, CM142	PMCNDBSY
PMCTbl	CM134, CM136, CM137, CM143, CM147, CM148	PMCLKBSY

Table 8-4 Alarm-log-OM cross reference chart

Alarm	Associated logs	Associated OMs
PrcOpt	CM165	none
RExSch	CM146, CM154	none
RExTst	CM102, CM179	CMDPSYNC, CMRSMXPU
SBsyMC	CM104	CMMCSBSY
SLIMLim	CM178	none
SLIMLIM	CM180	none
StrAlc	CM181	none

Memory limits and alarms

The following sections provide detailed information on CM MemLim and alarms.

Memory alarm cross reference charts

The following table describes the MemCfg alarm conditions for each platform. The report indicates that in the specified platform, the condition sets an alarm and generates a log.

Table 8-5 MemCfg conditions per platform

Config Test	SN20	SN30	SN40	SN50	SN50 MX	SN60	SN70	SNSE 20	SNSE 60	SNSE 70
Inventory problems	Report	Report	Report	Report	Report	Report	Report	Report	Report	Report
Platform does not support memory PEC	Report 9X14EA	Report 9X14EA	Report 9X14EA	Report 9X14BB (note)	Report 9X14BB	Report 9X14BB (note)	Report 9X14BB	Report 9X14BB 9X14DB	Report 9X14BB 9X14DB	Report 9X14BB 9X14DB
Empty slot by port card	N/A	N/A	N/A	N/A	Report	N/A	N/A	N/A	N/A	N/A

Note: Use inventory tables to determine the CPU PEC and count the different memory PECs. The PECS that are not known cause an inventory error. Use the present CPU and memory cards to determine the processor option. The memory rules configuration must follow the configuration rules for the processor option. If the configuration does not follow the configuration rules for the process option, the memory configuration is invalid.

Table 8-5 MemCfg conditions per platform

Config Test	SN20	SN30	SN40	SN50	SN50 MX	SN60	SN70	SNSE 20	SNSE 60	SNSE 70
Empty slots between memory cards	N/A	N/A	N/A	N/A	Report	N/A	N/A	N/A	N/A	N/A
Memory PECs inter -mixed	N/A	N/A	N/A	N/A	Report	N/A	N/A	N/A	N/A	N/A
Memory PEC blocks not ordered correctly	N/A	N/A	N/A	N/A	Report	N/A	N/A	N/A	N/A	N/A
Not enough of a given memory PEC	Report	Report	Report	Report	Report	Report	Report	Report	Report	Report
Too many of a given memory PEC	Report	Report	Report	Report	Report	Report	Report	Report	Report	Report
Invalid mix of memory PECs	N/A	N/A	N/A	N/A	Report	N/A	N/A	N/A	N/A	N/A
Platform does not support mixed memory	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Note: Use inventory tables to determine the CPU PEC and count the different memory PECs. The PECS that are not known cause an inventory error. Use the present CPU and memory cards to determine the processor option. The memory rules configuration must follow the configuration rules for the processor option. If the configuration does not follow the configuration rules for the process option, the memory configuration is invalid.

LowMem alarm

The system raises the LowMem alarm when the amount of free memory reaches the alarm threshold. This alarm triggers when the store allocator cannot configure a spare module. The failure to configure the spare module

occurs when not enough spare memory is available. The alarm triggers if the amount of memory that is not allocated reaches the alarm threshold.

StrAlc alarm

The StrAlc alarm notifies the user when the memory store allocation reaches the maximum allowed. This alarm does not depend on the switch configuration. The switch configuration is the number of memory cards and the SLM type. The StrAlc alarm rises when the the memory store allocation reaches the maximum:

- runtime image (MRTI)
- program store (PS) size
- data store (DS) size

or, 512 Mbyte of a single store type, like dstemp, is allocated.

The StrAlc triggers depend on the platform and the software release.

The StrAlc alarm triggers for BASE05 appear in the following table.

Table 8-6 StrAlc alarm triggers for BASE05

Platform	Maximum runtime image (Mbyte)	Maximum DS (Mbyte)	Maximum PS (Mbyte)
SN Series 20	212	172	64
SN Series 30	212	172	64
SN Series 40	212	172	64
SN Series 50	248	208	128
SN Series 50MX	320	256	128
SN Series 60	400	336	128
SN Series 70	400	336	128
SNSE Series 20 (NT9X14DB memory cards)	112	104	64
SNSE Series 20 (NT9X14EA memory cards)	200	168	64
SNSE Series 60	400	336	128
SNSE Series 70	400	336	128

The StrAlc alarm triggers for BASE06 appear in the following table.

Table 8-7 StrAlc alarm triggers for BASE06

Platform	Maximum runtime image (Mbyte)	Maximum DS (Mbyte)	Maximum PS (Mbyte)
SN Series 20	212	172	64
SN Series 30	212	172	64
SN Series 40	212	172	64
SN Series 50	248	208	128
SN Series 50MX	320	280 See Note.	128
SN Series 60	608	544	128
SN Series 70	736	672	128
SNSE Series 20 (NT9X14DB memory cards)	112	104	64
SNSE Series 20 (NT9X14EA memory cards)	200	168	64
SNSE Series 60	480	416	128
SNSE Series 70	704	640	128

Note: For SN Series 50MX, with some memory configurations, the maximum DS is 256 Mbyte.

The StrAlc alarm triggers for BASE07 and up, appear in the following table.

Table 8-8 StrAlc alarm triggers for BASE07 and up

Platform	Maximum runtime image (Mbyte)	Maximum DS (Mbyte)	Maximum PS (Mbyte)
SN Series 20	212	172	64
SN Series 30	212	172	64
SN Series 40	212	172	64

Note: SN and SNSE extended memory (EM) platforms are available for BASE08 and up. The StrAlc alram triggers for the EM platforms, SN and SNSE Series 70 platforms. The platforms appear in the same sequence.

Table 8-8 StrAlc alarm triggers for BASE07 and up

Platform	Maximum runtime image (Mbyte)	Maximum DS (Mbyte)	Maximum PS (Mbyte)
SN Series 50	248	208	256
SN Series 50MX	320	280	256
SN Series 60	608	544	256
SN Series 70 (See note).	736	672	256
SNSE Series 20 (NT9X14DB memory cards)	112	104	64
SNSE Series 20 (NT9X14EA memory cards)	200	168	64
SuperNode SE Series 60	480	416	256
SNSE Series 70 (See note)	704	640	256

Note: SN and SNSE extended memory (EM) platforms are available for BASE08 and up. The StrAlc alram triggers for the EM platforms, SN and SNSE Series 70 platforms. The platforms appear in the same sequence.

For more information, see the procedure Trouble Shooting a StrAlc alarm. The procedure is in the "Advanced troubleshooting procedures" chapter of this document.

LOWSpr and LowSpr alarms

The system raises the low spare memory alarms (LOWSpr and LowSpr) when the amount of spare memory is below the alarm threshold. Office parameter 1LOWSPR_ALARM_ON_CARD_SPR_BASIS in table OFCENG determines if the switch requires sparing on a card or on a module base. The default for SN is card sparing. The default for SNSE is module sparing.

One card for card sparing and one module for module sparing must be present. For card sparing, the system raises the alarm when one of the modules on the spare card is configured. For module sparing, the system raises the alarm when the spare modules configured.

MemLim alarm

The MemLim alarm indicates when the total store allocation reaches approximately 90% of the MRTI for the platform. This alarm is separate from the switch configuration.

The MemLim alarm trigger points for BASE05 and for BASE06 and up, appear in the following table.

Table 8-9 MemLim trigger points per platform

	BASE05		BASE06 and up	
Platform	**Maximum runtime image (Mbyte)**	**Trigger (Mbyte)**	**Maximum runtime image (Mbyte)**	**Trigger (Mbyte)**
SN Series 20	212	192	212	192
SN Series 30	212	192	212	192
SN Series 40	212	192	212	192
SN Series 50	248	224	248	224
SN Series 50MX	320	268	320	268
SN Series 60	400	352	608	576
SN Series 70 (See note)	400	352	736	704
SNSE Series 20 (NT9X14DB memory cards)	112	96	112	96
SNSE Series 20 (NT9X14EA memory cards)	200	180	200	180
SNSE Series 60	400	352	480	448
SNSE Series 70 (See note)	400	352	704	672

Note: SN and SNSE EM platforms are available for BASE08 and up. The MemLim alarm triggers for the EM platforms match the SN and SNSE Series 70 platforms.

SLMLIM and SLMLim alarms

The SLM limit alarms (SLMLIM and SLMLim) an SLM tape reaches the storage limit.

The capacity limits on the system load module (SLM) that will trigger the SLMLim alarm, appear in the following table.

Table 8-10 SLM capacity limits

SLM	PEC	Tape/DIsk (Mbyte)	Limit (Mbyte)	Trigger (Mbyte)	Comments
I	NT9X44AA	150/300	150	135	Limit = tape size
Ia	NT9X44AC	150/340	150	135	Limit = disk size
II	NT9X44AB	150/630	250	225	Limit = tape size
III	NT9X44AD	500/1000	500	450	Limit = tape size

The established limits for the SLM are based on the following:

- Each SLM type has a different capacity. If each plane has a separate SLM, the SLM with the smaller capacity is the trigger reference.
- The SLM tape must have enough room for the CM load.
- There must be enough room for two CM loads on the disk.
- The trigger for SLMLim minor alarm occurs at the trigger in table 90% of the limit.
- The trigger for SLMLIM major alarm occurs at the limit in table.

9 Mismatch analysis

This chapter describes mismatch problems that occur on the computing module (CM). This chapter describes:

- the types of mismatch
- the structure of mismatch logs
- the activities that operating company personnel can take to the correct mismatch

A mismatch is an error that occurs when two synchronized central processing units (CPUs) execute different instructions or operate on different data.

The write operation of a Series 60 burst mode can cause a matcher transient mismatch (MTM). The mismatch handler processes MTMs in a different way from other types of mismatches. The alarm thresholds for MTMs are different from other types of mismatches.

When the CPUs do not run in synchronization, the CPUs execute separate instructions and operate on separate data. Mismatches do not occur when CPUs do not run in synchronized mode.

Mismatch system response

The CM monitors the synchronization operation to detect a mismatch. If a mismatch occurs, the CM sends an external request for service to the CPUs through the hardware. The switch that suspends other operations activates the mismatch handler. Other operations that are suspected can include call processing.

A hardware fault can cause a mismatch. The hardware fault can be one of the following types:

- a fault that can be reproduced
- a fault that cannot be reproduced

Mismatch handler

To maintain the integrity and reliability of the system, the mismatch handler performs the following actions:

- determines if the CPUs are safe to continue to run in synchronization
- determines which CPU is active
- determines the cause of the mismatch
- recovers the system from the mismatch

> ***Note:*** If the mismatch handler performs a switch of activity (SWACT), a cold restart of switch activity does not occur.

For more details on the mismatch handler, see the "Preventative maintenance strategies" chapter in this document.

Figure 9-1, "Mismatch handler process" on page 9-3 on shows the flow of the mismatch handling process.

General mismatch thresholds

The mismatch handler does not synchronize the CPUs again when the following conditions are present:

- Three fault mismatches that require out-of-synchronization recovery occur in 1 h. The system resets the fault mismatch threshold on the hour.
- 15 memory fault correctable mismatches occurred in 1 h.

For MTMs, the default mismatch threshold of the MMsync alarm is 30 for each 24 h. The operating company can reset the default threshold to the range of 10-50 mismatches. The threshold for the MMnoSy alarm is 10 mismatches each 10 min. The operating company cannot change the threshold of the MMnoSY alarm.

Mismatch alarms

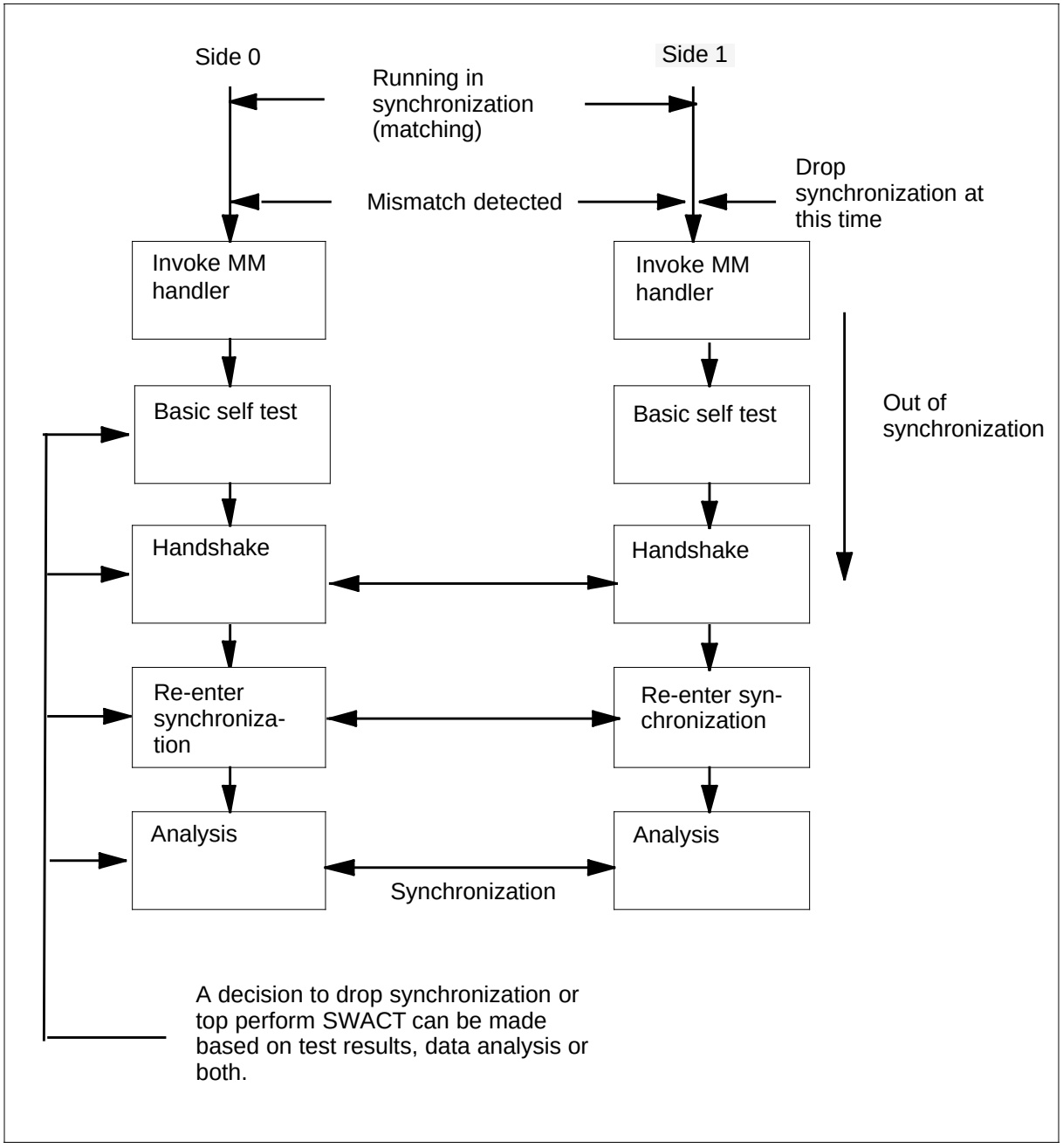
The mismatch handler raises the following alarms:

- The NOOVR alarm (M68K only) occurs when seven transient mismatches or seven memory fault correctable mismatches occur in 1 h.
- The MemFlt alarm occurs when the number of fault mismatches exceed the memory fault correctable threshold.
- The MMsync alarm occurs when the switch remains in the synchronous mode after the switch recovers from a mismatch. The mismatch is not an

MTM mismatch. The mismatch handler raises the MMsync alarm for MTMs when the number of mismatches exceeds the daily MTM threshold.

- The MMnoSy alarm occurs when the switch is not in the synchronous mode after the switch recovers from a mismatch.

Figure 9-1 Mismatch handler process



Mismatch logs

The system generates mismatch logs when the following events occur:

- the mismatch handler starts
- the handling of the mismatch is complete

Mismatch fault log

The mismatch fault log includes the activity status, the mismatch reason and the recovery action that the switch takes. The mismatch fault logs include the following:

- MFC100 INFO soft fault mismatch log
- MM100 INFO mismatch fault log
- MM101 INFO mismatch fault log
- MM102 INFO mismatch fault log (only for MTM)

Note: The system generates the MM102 INFO log on SN and SNSE Series 60 switches only.

Mismatch recovery log

The post interrupt mismatch handler generates the mismatch recovery log. The log lists the state of the switch after the recovery actions are complete. The system generates the mismatch recovery log after the fault log.

The mismatch recovery log contains a prioritized card list. The card that is the probable cause of the mismatch appears at the top of the list.

The following list describes different fault mismatch recovery logs:

- The system generates the MM110 INFO log when the mismatch handler drops synchronization and system recovery synchronizes the CPUs again.
- The system generates the MM111 INFO log when the mismatch handler drops synchronization and system recovery does not synchronize the CPUs again.
- The system generates the MM112 INFO log when the system cancels system recovery.
- The system generates the MM113 INFO log when system recovery fails.

The following list describes the reasons the system generates different memory fault correctable recovery logs

- The system generates the MFC110 INFO recovery log when the memory fault correctable mismatches do not exceed the threshold.
- The system generates the MFC111 INFO action log when the memory fault correctable mismatches exceed the threshold.

Mismatch tools

The following sections describe the MMINFO tool.

MMINFO

The MMINFO tool displays information on mismatch fault logs from the MAP terminal.

The collection of MMINFO data occurs when the mismatch handler starts. The system collects data that includes detailed data from the CM at the time of the mismatch. The system collects data that includes the progress mark after the first analysis and the recovery action of the switch.

The progress mark indicates the progress of the mismatch handler. The mismatch handler determines the type of fault that causes the mismatch. This mark indicates the type of analysis the mismatch handler runs at the point of a fault. Memory analysis marks, address analysis marks and mate analysis marks are examples of progress marks.

An analysis of fault mismatches can determine the stability of a synchronized switch or troubleshoot a switch that is not in synchronization. To analyze fault mismatches perform the following actions:

- To dump all available mismatch logs, type:

```
>logutil;open mm;back all

>MMINFO
```

For more information on the MMINFO tool and commands, refer to the "User Interface and Command" chapter.

MMSYNC command

Use the MMSYNc command to perform the following actions:

- clear the matcher transient mismatch (MTM) counts
- determine the synchronization and drop synchronization thresholds for the MTM
- determine the current MTM count
- determine if the MTM count exceeds the synchronization alarm threshold or the drop synchronization threshold for the MTM
- set the MMsync alarm threshold for MTM

The MMSYNC command is a unlisted menu command. Command MMSYNC applies only to Series 60 processors.

Use the MMSYNC command from the CM, CM;MC, CM;Memory and CM;PMC MAP levels.

For more information, refer to the MMSYNC command description in the "User Interface and Command" chapter in this document.

General analysis of mismatch logs

The DMS-core normally works in synchronization. A change from this status that is not manual causes the DMS-core to lose synchronization. The system tolerates some types of mismatches but requires immediate action to correct severe mismatches. The system attempts to synchronize the DMS-core again. If the system cannot synchronize the DMS-core again, the system leaves the DMS-core in simplex mode. The system also leaves the DMS-core in simplex mode when the system reaches mismatch thresholds. Analyze the mismatch logs before you return the DMS-core to the duplex mode of operation.

When the system exits the mismatch handler, the system specifies the reason of the exit. This reason can appear as one of many different values for the M68K or M88K BRISC processors. This section explains the values for processes. In most cases, the system deactivates the CPU at fault. This section explains the possible reasons the system does not deactivate the CPU.

Except for memory correctable mismatches, mismatches are early signs of circuit pack failure. A switch that is out of synchronization because of one or more mismatches requires maintenance. Maintenance can start at the MM logs.

Before synchronization of the CPUs begins, make sure that operating company personnel correct the mismatch before the next scheduled maintenance. Make sure that personnel correct the mismatch before a CM REX test runs.

The CPUs must remain out of synchronization until personnel can analyze the condition correctly. Personnel can perform a loadmate into the inactive CPU to act as a secondary load. If a fault occurs while the CPU is in simplex mode, the secondary load is present.

If a problem continues after the analysis of the logs and the replacement of the cards, contact the next level of support.

Mismatch analysis

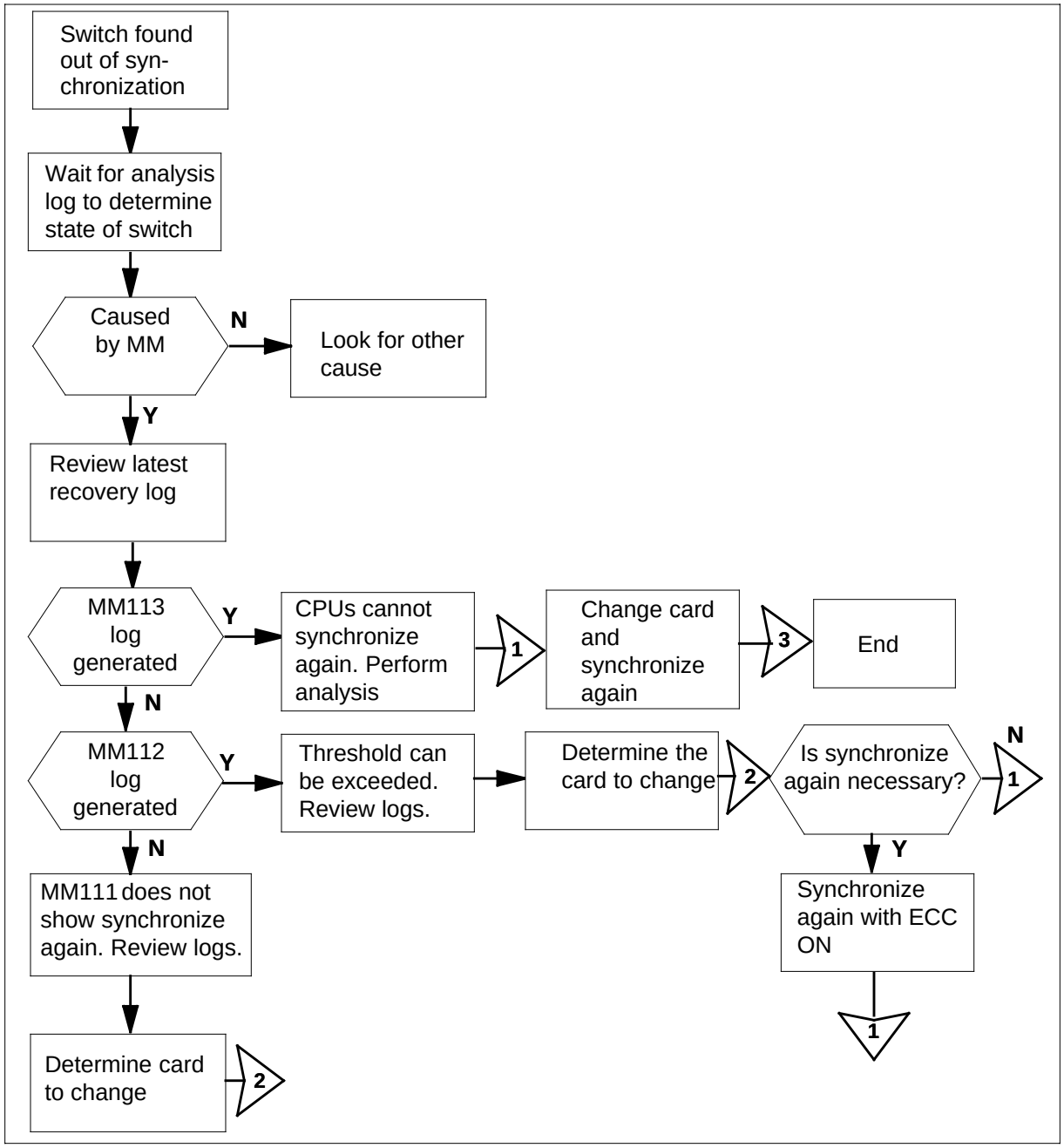
Mismatch analysis can troubleshoot or determine the stability of an out-of-specification synchronized switch. Mismatch analysis requires the following steps:

- Enter the required information into a mismatch trend analysis table. This list must include the last 30 days or more.
- Look for trends in mismatches over the last 30 days or more. A trend occurs when the mismatch reasons are identical in two or more mismatches.
- Look for a common card that appears in the card list of the recovery log.
- Begin a detailed analysis of the trends. Determine if previous mismatches indicate a trend.

Note: In some mismatch faults, the correction of the fault can require a change of more than one card in the card list. If three card replacements do not solve the fault problem, contact the next level of support

Figure 9-2, "Analysis of fault mismatch logs" on page 9-8 describes how to analyze the fault mismatch process.

Figure 9-2 Analysis of fault mismatch logs



Fault mismatch logs

Create a mismatch trend table like the example in the following table. The mismatch trend table can establish a record of fault mismatches.

Complete the table in two stages:

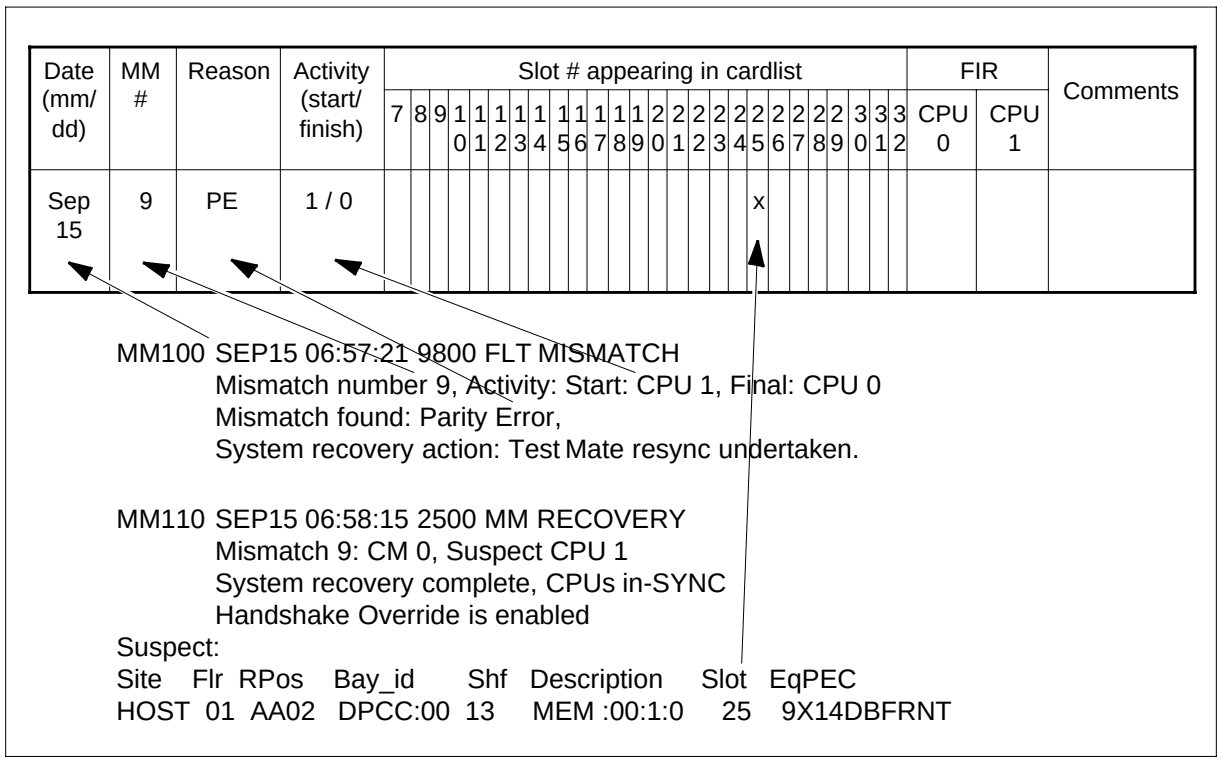
- The first stage appears in Figure 9-3, "Mismatch trend table.". This stage includes information from the first section of the MM100 log. This stage includes information from the card list of the MM110 recovery log.
- The second stage appears in Figure 9-4, "Mismatch trend table" on page 9-11 and includes information from the basic data field section and from the virtual processor registers in the MM100 log.

Mismatch trend table

The first section of the table in Figure 9-3 requires information found in the first section of MM100 log:

- The date and time that the mismatch occured
- The mismatch sequence number and the activity of the CPU at the start and end of the mismatch handler.
- The mismatch handler result and condition made at the interrupt level.
- The PEC number of the card with possible faults listed under the heading EQPEC.

Figure 9-3 Mismatch trend table

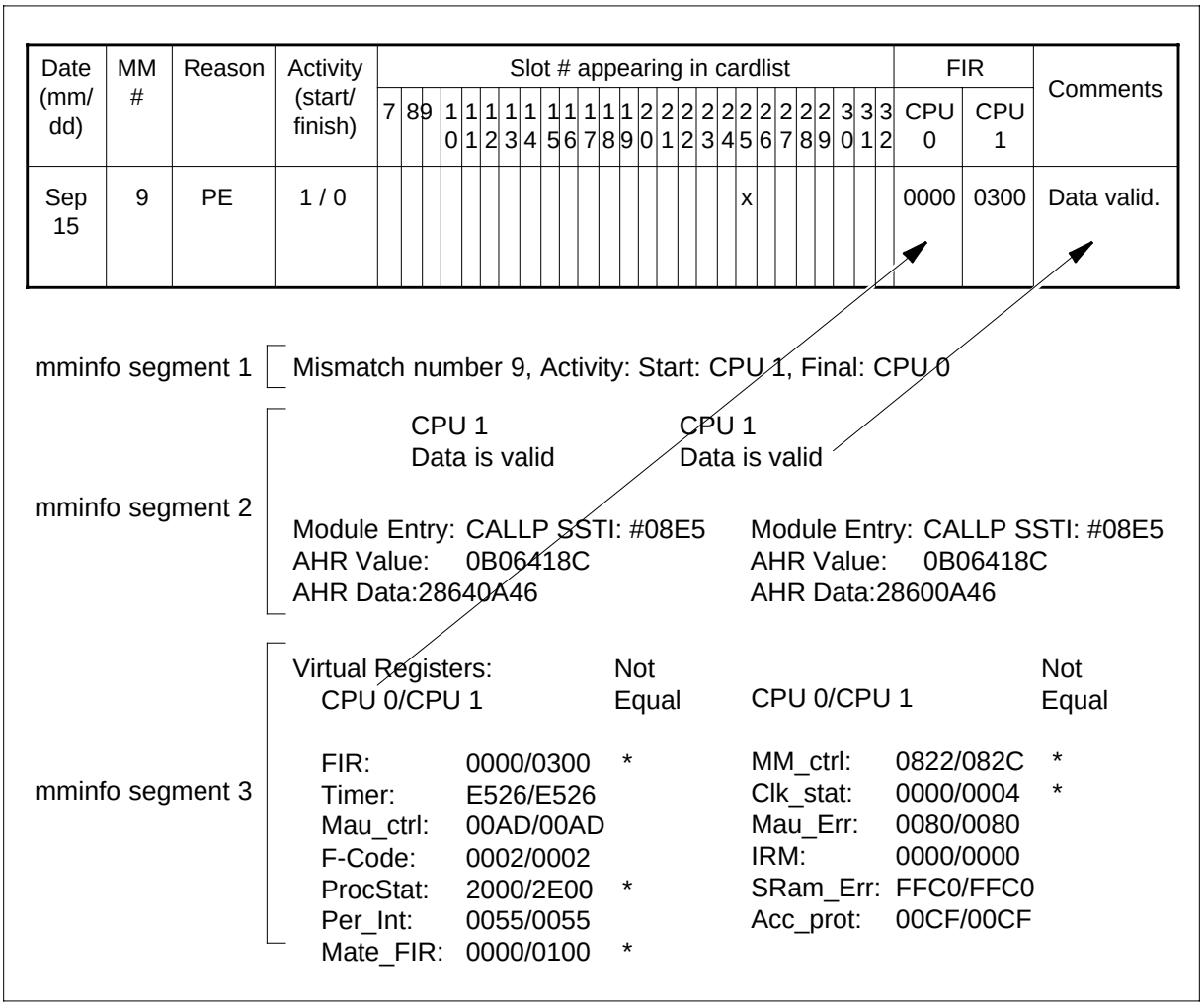


To complete the trend table, add the information from the virtual registers field of the MM100 log. The virtual registers field displays the following information:

- The CPU0/CPU1 is valid field indicates if this mismatch or a previous mismatch causes the system to display the data in this log. The data sent to the log process is from a single buffer. If the system does not collect from the mate CPU, the system displays the data from the last mismatch. The system marks the data in the log as valid when the collected data is from the current mismatch.
- The fault indication register (FIR) indicates the type of fault. The combinations of the FIRs in the two CPUs determines the type of fault.

For more information see Table 9-2, "Interpretation of mismatch fault conditions" on page 9-15, Table 9-3, "Interpretation of infrequent mismatch fault conditions" on page 9-24, and Table 9-4, "Interpretation of mismatch fault conditions" on page 9-26.

Figure 9-4 Mismatch trend table



Date (mm/ dd)	MM #	Reason	Activity (start/ finish)	Slot # appearing in cardlist																								FIR		Comments
				7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	CPU 0	CPU 1	
Sep 15	9	PE	1 / 0																			x								0000	0300	Data valid.

mminfo segment 1

Mismatch number 9, Activity: Start: CPU 1, Final: CPU 0

mminfo segment 2

	CPU 1 Data is valid	CPU 1 Data is valid
Module Entry:	CALLP SSTI: #08E5	CALLP SSTI: #08E5
AHR Value:	0B06418C	0B06418C
AHR Data:	28640A46	28600A46

mminfo segment 3

Virtual Registers: CPU 0/CPU 1		Not Equal	CPU 0/CPU 1		Not Equal
FIR:	0000/0300	*	MM_ctrl:	0822/082C	*
Timer:	E526/E526		Clk_stat:	0000/0004	*
Mau_ctrl:	00AD/00AD		Mau_Err:	0080/0080	
F-Code:	0002/0002		IRM:	0000/0000	
ProcStat:	2000/2E00	*	SRam_Err:	FFC0/FFC0	
Per_Int:	0055/0055		Acc_prot:	00CF/00CF	
Mate_FIR:	0000/0100	*			

Single bit memory fault correctable mismatches

Memory fault correctable (MFC) mismatches are normal on a DMS SN and SNSE switches that use dynamic RAM devices without error correction enabling.

The MFC mismatches affect NT9X14DB/EA memory packs in a CM with NT9X13BC/GA/HB/MA/MB and NT9X10AA processors.

The memory cards in the CM can be one of the following:

- all NT9X14DB memory cards
- all NT9X14EA memory cards
- a combination of NT9X14EA memory cards and NT9X14DB memory cards

The memory fault analysis applies to NT9X14DBC cards and NT9X14EA cards.

Soft errors in DRAMS

The *Micron Semiconductor Inc. Dynamic Memory Design 1991/1992 Data/Book/Handbook* defines a soft error as follows:

> A soft error is a single bit output error that does not recur. The most common cause of soft errors is the passage of ionizing radiation through the memory cells of semiconductor devices. The most common source of this radiation is alpha particles. Alpha particles are generated as the result of decay in radioactive substances such as thorium and uranium. These substances are present in trace amounts in the packaging material of all ceramic and plastic encapsulated integrated circuits. A soft error occurs when an alpha particle hits the memory array with enough energy to upset the stored data in a cell.

The 1Mx1 and 4Mx digital recorded announcement machine (DRAM) has a soft error rate supplied by the vendor. The soft error rate is 2000 FITS (Failure in Time) or 2000 soft errors for every one billion h. For memory cards NT9X14DB/EA, this number is 480 000 FITS (240 devices x 2000 FITS/device) or soft errors every billion h. This calculation means one error for every 86.8 days for each NT9X14DB/EA memory card configured on the computing mode.

Soft errors in a DRAM device occur randomly and the values described above are determined by use of statistics. A high number of errors in a short period of time is common. The number of errors over a long period of time will be in the predicted range.

The CM experiences soft errors for the reasons described in the *Micron Semiconductor Inc. Dynamic Memory Design 1991/1992 Data/Book/Handbook*. If the soft error occurs when the processors of the CM are in synchronization, a memory fault correctable mismatch occurs. The mismatch handler identifies the processor with the error and makes sure that processor is inactive. When the processors are not in synchronization, the active processor runs with the error correcting codes (ECC) enabled. The ECC corrects soft errors and prevents a fault.

Significance of the soft error calculation rate

The soft error calculation helps the operating company establish a method for the long-term analysis of MFC mismatches on the CM. This number does not indicate hardware with faults. The calculation gauges the how regular the MFC mismatches are over time.

The following table provides a matrix of acceptable MFC mismatches over 7 days, 28 days and 84 days. Mismatches normally occur randomly across processors and memory cards.

Table 9-1 Acceptable MFC mismatch thresholds

Number of NT9X14DB/EA configured	Maximum acceptable rate in 7 days	Maximum acceptable rate in 28 days	Maximum acceptable rate in 84 days
6	1	3	9
8	1	4	11
10	2	5	12
12	2	6	14
14	2	7	17
16	3	8	19
18	3	9	22
20	3	10	24

The configuration of a shelf determines the recommended maximum number of MFC mismatches. For example, a shelf with 20 NT9X14DB/EA memory chips must not exceed the following numbers:

- three MFC mismatches in seven days
- ten MFC mismatches in 28 days
- 24 MFC mismatches in 84 days

If four mismatches occur in a seven day period, monitor the switch. Determine if the number of MFC mismatches exceeds the 10 mismatches in 28 days. If the number of MFC mismatches does not exceed 10 in 28 days period, continue to monitor the switch. Determine if the number of MFC mismatches exceeds 24 mismatches in 84 days.

The mismatch handler analyzes the MFC mismatches over time. The mismatch handler produces a MFC 110 INFO recovery log or MFC 111 INFO action log. See Table 9-1, "Acceptable MFC mismatch thresholds," for an example of the time frame that the mismatch handler uses.

If the number of MFC mismatches exceeds the recommended rate during the monitoring period, replace a card. Contact the next level of technical support for support when one of the following occurs:

- the MFC mismatches exceed the recommended rate for the slot after the change of cards
- you cannot continue to monitor the switch
- the results are abnormal

For more information, see Table 9-5, "Interpretation of MFC mismatch conditions" on page 9-29.

Interpretation of mismatch logs

M68K/88K mismatch fault conditions

Table 9-2, "Interpretation of mismatch fault conditions" on page 9-15 lists the mismatch conditions that occur most often. This table contains the action to take to clear the problem for the following logs:

- M68K
- BRISC M88K MM100
- MM111

- MM112
- MM113

Table 9-2 Interpretation of mismatch fault conditions

Reason/condition	Possible cause and corrective action
Bad shared store	**Definition** The CPU cannot write to the variables of the mismatch handler and read the same values back. The mismatch handler attempts to drop activity. If this attempt fails, the CPU starts again with the reason Mismatch, CPU insane. **Fault isolation** The system does not diagnose a fault. An error condition occured while the system attempts to a diagnose a fault. **Location** A possible memory error in the mismatch handler occured. Like regular modules on the DMS switch, the mismatch handler owns memory. Look for the CPU and memory cards that correspond to the error. **System recovery** The system attempts to drop activity and attempts to start to load again with the reason Mismatch, CPU insane. **Manual actions** Perform a mismatch analysis to identify previous faults. The mismatch log can help the analysis. The CPU that drops activity can have faults. Replace a card.
Mate failed rendezvous	**Definition** The CPUs failed to exchange data in the mismatch handler. **Fault isolation** The system did not perform any real time diagnostics. The card list can be not exact. This type of mismatch occurs often when there is a destroyed software load on one CPU. The mismatch handler sofware only runs on one CPU and the handshake cannot occur.

Table 9-2 Interpretation of mismatch fault conditions

Reason/condition	Possible cause and corrective action
	Other causes of this mismatch can be a failed CPU or a power problem. This type of mismatch is serious. Analyze the history of mismatches. The data in the mismatch log can be invalid for the inactive CPU. The data from the active CPU is valid. The mismatch handler automatically assumes the inactive CPU caused the fault. The mismatch data from the active CPU can indicate the problem. The fault indication register (FIR) can contain this match data. If the active CPU does not contain a FIR or other indications, the mismatch is not precise. The fault can be an ECC error indicated in the FIR. Use the >Sync ECCON command to synchronize the CPUs. Perform a SWACT and change the card. Use other synchronization options under close supervision and with help from Nortel personnel. **Location** The card list lists the NT9X10/9X13 memory cards first. Any card on the list can cause the problem. **System recovery** The system attempts to test and synchronize again the CPUs, again except when resynchronization occurs while the CPU is in synchronization. **Manual actions** This mismatch is a serious mismatch. Perform corrective action. Perform a full mismatch analysis to identify previous faults. Look for indications for fault on the active FIR. If the fault is not the active side look at trends for faults on the inactive side.

Table 9-2 Interpretation of mismatch fault conditions

Reason/condition	Possible cause and corrective action
Problem with I/O port	**Definition** One or more port cards on the CM or system load module (SLM) shelf can have a fault. **Fault isolation** The address hold register (AHR) contains the address of the port card at fault. The card list normally identifies this type of mismatch. The card list for the peripheral message controller (PMC) can contain several cards that are at fault. **Location** The following cards can display a fault: • the CPU port card NT9X12 for the MC shelf • the CM bus extender NT9X27 card on the CM shelf and the cable to the SLM shelf for the PMC • the CM bus extender NT9X27 card for the SLM shelf • the CPU port card NT9X12 for the SLM shelf • the SLM NT9X44 card for the SLM shelf • the parallel port interface NT9X46 card for the SLM shelf **System recovery** When the system detects a port fault, the CPUs do not enter the synchronous mode of operation again. The system requires manual intervention to correct the fault and synchronize the CPUs again. **Manual actions recommended** A problem with I/O ports is very serious. Enter the MC or PMC level of the MAP display and type DISPCNTS to display problems in the ports. The system requires manual action to synchronize the CPU again.
Match logic broken	**Definition** A test on the matcher application specific integrated circuit (ASIC) fails. The mismatch is a not common mismatch. **Fault isolation** The system switches activity from the CPU that has faults. The card list is accurate. Transient faults can cause this type of mismatch.

Table 9-2 Interpretation of mismatch fault conditions

Reason/condition	Possible cause and corrective action
	Location The following cards can contain a fault: • the CPU card NT9X10 • the CPU card NT9X13 **System recovery** The mismatch handler attempts to switch activity from the CPU that failed the test. The system does not synchronize the switch again. **Manual actions** This mismatch is a serious mismatch. Perform a complete mismatch analysis to identify previous faults.
General FIR bits set	**Definition** The fault indication register (FIR) bits are set on the active or inactive CPU. Transient hardware can cause this rare mismatch. **Fault isolation** The address indicates the hardware accessed when the fault occurred. **Location** One of the following cards can contain a fault: • the CPU card NT9X10 • the CPU port card NT9X12 • the CPU card NT9X13 • the memory card NT9X14 **System recovery** The mismatch handler attempts to switch activity away from the CPU. **Manual actions** Transient hardware can cause this mismatch. Perform a full mismatch analysis to identify previous faults. Perform a full analysis of the logs to identify a trend of faults. If this fault persists, schedule a card change. If the analysis does not identify a card with faults, contact the next level of support.

Table 9-2 Interpretation of mismatch fault conditions

Reason/condition	Possible cause and corrective action
Could not synchronize again	**Definition** The CPU cannot synchronize again when the mismatch handler is activated to complete the analysis during the handling of a mismatch. **Fault isolation** The mismatch handler does not perform a full analysis under this condition. The card list may not be accurate. **Location** This mismatch can trigger in the mismatch handler. Any piece of equipment on the DMS core can cause this mismatch. **System recovery** See the section under mismatch thresholds. **Manual actions recommended** Perform a full mismatch analysis to identify previous faults. Change the card if necessary. The system was in the mismatch handler when the error occurred. The FIR of each CPU can indicate the type of error.
Parity error	**Definition** A memory access results in the return of data having to have bad parity for SRAM or DRAM. **Fault isolation** One or two cards in one CPU contain the fault. **Location** The following cards can contain a fault: • memory card NT9X13/ CPU card NT9X10 for SRAM • memory card NT9X14 for DRAM • CPU card NT9X10 / memory card core processor card NT9X13 for DRAM **System recovery** The system performs a SWACT, if necessary. The system leaves the switch out of synchronization. The system requires manual action to synchronize the CPU again. **Manual action** This mismatch is a serious mismatch. Change the first card on the card list before resynchronization completes.

Table 9-2 Interpretation of mismatch fault conditions

Reason/condition	Possible cause and corrective action
Data store differed	**Definition** The data store does not match and the program store does not match. The mismatch handler indicates data mismatch occured, but cannot determine the source of the fault. This mismatch is difficult to correct. **Fault isolation** The FIR does not contain errors. The system cannot determine the source of the fault. The system assigns the fault to the inactive CPU. **Location** The following cards can contain a fault: • the CPU card NT9X10 • the CPU card NT9X13 • the memory card NT9X14 See the address and card list. Potential but hidden faults on the NT9X14 memory card can cause the mismatch. **System recovery** The system synchronizes the CPUs again. Monitor the switch for more mismatches or traps. **Manual action** This mismatch is a serious mismatch. Change both NT9X14 memory cards if the trends analysis does not indicate the source of the mismatch. Perform a full mismatch analysis to identify previous faults. **Location** The following cards can contain a fault: • the CPU card NT9X10 • the CPU card NT9X13 • the memory card NT9X14 See the address and card list. Potential but hidden faults on the memory card NT9X14 can cause the mismatch. **System recovery** The mismatch handler synchronizes the CPUs again. **Manual actions** This mismatch is a serious mismatch. Perform a full mismatch analysis to identify previous faults.

Table 9-2 Interpretation of mismatch fault conditions

Reason/condition	Possible cause and corrective action
Processor registers different	**Definition** The CPU register contents differ between CPUs. The system does not detect other faults. The mismatch handler acknowledges the data mismatch occured but cannot determine the source of the fault. This mismatch is difficult to correct. **Fault isolation** The system cannot identify the CPU with faults. The system assigns the inactive CPU the fault by default.
Hardware access error	**Definition** The address of the mismatch was in one of the four hardware access ranges that follow: • the hardware ASICs • the SRAM • the invalid DRAM fault • the hard DRAM fault **Fault isolation** The hard DRAM fault is on one card. The following faults can be on one of two cards: • The SRAM fault • invalid DRAM fault • hard ASICs fault One of the cards is on the active CPU and the other cards is on the inactive CPU. The system assigns the fault to the inactive side by default. **Location** The following cards can contain a fault: • the CPU card NT9X10 • the CPU card NT9X13 • the memory card NT9X14

Table 9-2 Interpretation of mismatch fault conditions

Reason/condition	Possible cause and corrective action
	System recovery The mismatch handler attempts to switch activity from the faulty side of the inactive CPU. The mismatch handler can synchronize again. The type of fault determines if the mismatch handler synchronizes again. **Manual action** This mismatch is a serious mismatch. When the first card does not cause the fault, analyze the mismatch trends.
Transient	**Definition** The mismatch handler cannot determine the cause of the mismatch. **Fault isolation** The system assigns the fault to the inactive CPU by default. **Location** The following cards can contain a fault: • memory card NT9X14 • CPU card NT9X10 • CPU card NT9X13 • any card on the card list **System recovery** The mismatch handler synchronizes the CPUs again. **Manual action** If more than three transient mismatches occur in a week, attempt to correct the mismatch. Determine the trend of the hardware accessed at the time of the transient mismatches.
Mismatch during synchronization transition	**Definition** A mismatch occurred when the CPUs synchronized or dropped synchronization. The mismatch handler does not attempt to synchronize again. **Fault isolation** The analysis is not complete. The CPU cannot complete synchronization. The card list can list inactive cards first by default.

Table 9-2 Interpretation of mismatch fault conditions

Reason/condition	Possible cause and corrective action
	Check the FIR for an ECC error. Use the SYNC ECCON command to synchronize. Perform a SWACT and a card change. • CPU card NT9X10 • CPU card NT9X13 • memory card NT9X14 • any card on the card list **System recovery** The system does not attempt synchronization again. **Manual action** This mismatch is a serious mismatch. Take correcting action. The fault can be on either CPU. Data is correct for both CPUs in the log. The fault is usually the CPU with the FIR. ***Note:*** A failed synchronization attempt normally destroys the mate load. Perform a full mismatch analysis to identify previous faults.
Memory fault, uncorrectable	**Definition** The system cannot recover from a hard memory error. **Fault isolation** The CPU with the fault becomes inactive. The condition of the fault determines if the minimal card becomes defective (f) or ISTb. **Location** The card with faults is an NT9X14 memory card. **System recovery** The CPUs do not remain synchronized. The system can attempt to synchronize again. **Manual action** A hard ECC fault is detected and is can be reproduced. Change the memory card in the card list.

Table 9-3 describes infrequent mismatch fault conditions common to the following logs:

- M68K
- BRISC M88K MM100
- MM111

- MM112
- MM113

Table 9-3 also provides the probable cause of infrequent mismatch fault conditions and the action required to clear the problem.

Table 9-3 Interpretation of infrequent mismatch fault conditions

Reason/condition	Possible cause and corrective action
Mismatch not fully handled	This type of mismatch is rare. This type of mismatch must not occur on an active CPU. The mismatch handler attempts to start again with the reason Mismatch, CPU insane.
Could not give up activity	The mismatch handler detects a severe fault in the CPU. The mismatch handler attempts to perform a SWACT. The SWACT fails. The CPU with faults remains active. This condition can cause a COLD restart. This type of mismatch is rare. Take immediate action.
Mismatch during error condition	An error occurred that indicates a multiple fault. The mismatch handler does not always trust that its diagnosis is correct. If you see this message investigate carefully. This error message can indicate a problem within the data structure of the mismatch handler.
Mismatch during mismatch recovery	A mismatch occurred while the mismatch handler was active. This error message indicates that the mismatch handled before was not handled correctly. This error message can indicate that the fault is more severe than anticipated. A double fault condition can be present. This mismatch can occur when the post mismatch handler attempts to recover from a previous mismatch. Perform a full mismatch analysis to identify previous faults.
Mismatch in firmware	The program controller (PC) was in firmware at the time of mismatch. This fault is a severe fault. The CPUs do not attempt to synchronize again. Synchronizing again can cause the the state of one or both CPUs to become corrupt. The firmware is in an EPROM. If any bits or an access error to this chip fails in synchronization this mismatch can occur. This type of mismatch does not occur often. Take immediate action.
Mismatch handler under test	This test tests the flow of control in the mismatch analysis process. The debugger activates this test. This test does not occur in normal system operation.

Table 9-3 Interpretation of infrequent mismatch fault conditions

Reason/condition	Possible cause and corrective action
Extension shelf filter not bound in	This error message indicates that the application diagnostic and post interrupt analysis procedures are not bound into the mismatch handler tables for the extension shelf.
Invalid mismatch reason	This error message indicates a severe error condition. Report this error message to next level of support.

BRISC M88K mismatch log

The following table describes the mismatch conditions applicable to the following logs:

- BRISC #M88K MM100
- MM111
- MM112
- MM113

Table 9-4, "Interpretation of mismatch fault conditions" on page 9-26 provides the possible cause of the mismatch and the action required to clear the problem

The BRISC specific mismatches are called processor bus (P-bus) mismatches.

Table 9-4 Interpretation of mismatch fault conditions

Reason/condition	Possible cause and corrective action
Pbus-no error found	**Definition**
Pbus-transient error	The internal processor bus (P-bus) contains the fault.
Pbus-insufficient data to analyze	**Fault isolation**
	The system cannot isolate the fault to one CPU or the other.
	Location
	The processor card NT9X10 can contain a fault.
	System recovery
	The CPU remains in synchronization.
	Manual actions
	These mismatches are serious mismatches. Perform a full mismatch analysis to identify previous faults.

Table 9-4 Interpretation of mismatch fault conditions

Reason/condition	Possible cause and corrective action
Pbus-matcher broken Pbus-presynchronize environment failed Pbus-code data difference in CMMU Pbus-hard code data error in CMMU Pbus-code data difference in PCCAB Pbus-hard code data error in PCCAB Pbus-data difference in data CMMU Pbus-data difference in memory Pbus-hard data error in memory	**Definition** The internal P-bus contains a fault. **Fault isolation** The system cannot isolate the fault to one CPU or the other. **Location** The processor card NT9X10 can contain a fault. **System recovery** The mismatch handler drops synchronization of the current active CPU by default. Synchronizing again requires manual action. **Manual actions** These mismatches are serious mismatches. Perform a full mismatch analysis to identify previous faults.
Pbus-faulty CPU 0 PCCAB Pbus-faulty CPU 1 PCCAB Pbus-faulty CPU 0 PCCAB DRAM Pbus-faulty CPU 1 PCCAB DRAM Pbus-faulty CPU 0 data CMMU Pbus-faulty CPU 1 data CMMU Pbus-faulty CPU 0 code CMMU Pbus-faulty CPU 1 code CMMU Pbus-faulty CPU 0 LMS Pbus-faulty CPU 1 LMS Pbus-faulty CPU 0 processor card Pbus-faulty CPU 1 processor card Pbus-faulty CPU 0 BATC #6 Pbus-faulty CPU 1 BATC #6 Pbus-faulty CPU 0 BATC#7 Pbus-faulty CPU 1 BATC#7	**Definition** The internal P-bus contains a fault. **Fault isolation** The fault is in one CPU. The mismatch reason indicates the CPU that contains the fault. **Location** The processor card NT9X10 can contain a fault. **System recovery** The mismatch handler performs a SWACT to route activity from the CPU with the fault and drop synchronization. Synchronization of the CPU can require manual action. **Manual actions** These mismatches are serious mismatches. Perform a full mismatch analysis to identify previous faults.

Memory fault correctable mismatch log

Table 9-5, "Interpretation of MFC mismatch conditions" on page 9-29 describes the mismatch conditions that apply to the following logs:

- MFC100
- MFC110
- MFC111

Table 9-5 also describes the possible cause of the mismatch and the action required to clear the problem.

Table 9-5 Interpretation of MFC mismatch conditions

Reason/condition	Possible cause and corrective action
Memory fault, correctable	**Definition** A memory card received bad data from the location read during an attempt to access memory. The memory card sends the CPU the bad data and an interrupt signal. This action caused a mismatch. **Fault isolation** An ECC error was latched in one of the FIRs. The CPUs can recover if the system can locate the error. If the error was a single bit fault and located in a single longword, the system connects the error from the memory module. When the system repairs the error, the CPUs remain in synchronization. The system marks the memory module as in-service trouble or with faults on the MAP display. The system generates a log appropriate to the condition. The MTC suspect element for the inactive CPU also indicates the memory module, with the fault. For more information see Memory fault, correctable mismatches in this chapter. **Location** Memory card NT9X14 can contain a fault. These faults are transient. Manual tests cannot reproduce the faults. A manual test performed on a memory card that is in-service trouble or has faults can pass. **System recovery** The system isolates the CPU with a fault. In system recovery, the system copies data from the good CPU to the CPU with the fault. The mismatch handler synchronizes the CPUs again. **Manual actions** This mismatch is the least severe mismatch. This mismatch is the most common of all mismatches. The system marks a card as in-service trouble when a threshold is exceeded. Change the card, even if a manual test passes.

10 Advanced troubleshooting procedures

Task list

The following list provides the names of the procedures in this chapter, in alphabetical order. To find the correct routine maintenance procedure, look for the procedure name in the left column. Go to the page number that appears in the corresponding column. If more than one entry appears under the procedure name, check the information of the task.

Responding to a CMTrap alarm

Application

The system generates a CMTrap alarm when a trap threshold is exceeded. A trap is an interruption of the normal processing flow. In most occurrences, a hardware fault causes the interruption.

The process cannot proceed when the process attempts to use a hardware element that has faults. The hardware that has faults interrupts the normal flow of the process. The interruption causes the software to trap. Traps are filtered to determine an exact cause.

For example, a port that has faults can cause a trap. The port is taken out of service. After a specified time interval, the process tries to access the port again. The process now recognizes that port is out of service. The process searches for a redundant hardware element. This element is another port.

The process continues when the process finds a redundant hardware element. The process does not perform additional trap action. Maintenance activity starts on the component that has faults. When there is no redundant element, or the process cannot find another route, the system generates a CM119 TRAP log. The threshold counter automatically increases.

The CM119 trap log contains information that is polled from different registers on the CPU card. The registers that are polled for the 68000 series CPUs are different from the registers polled for the 88000 series (BRISC) CPUs.

The TRAPINFO tool displays the trap log data. Type the command TRAPINFO at any MAP terminal to generate a trap summary report. The report includes information about all recent traps. The report presents information in the following format:

```
>trapinfo
 Trap Summary:

 Trap 30. Bus timeout on read. At Sep-10 18:07:32.
 At 0D85CDD0 (Procname Not known). PROCID= #4502 #2004: ABEL.
 PGM= .
 Trap type count: 3.
```

To obtain more information about a trap shown in the summary, type the TRAPINFO command with the trap number. The MAP displays information about the trap, as shown on the following pages.

Operating company personnel use the information contained in the trap to analyze the root cause of the trap.

Responding to a CMTrap alarm (continued)

The flowchart on page -6 contains the steps to take in response to a CMTrap alarm.

Command input:

```
>trapinfo 30
```

MAP response:

```
Trap prior to reload of current image
 Trap number 30, Bus timeout on read.
 At 0D85CDD0 (Procname Unknown),
 PROCID= #4502 #2004: ABEL, Entry Module:  SSTI: #232A
 Current count of this trap type: 3 Traceback:


0B054044=SYSINIT.FI03:ABELCODE+#0174
 0B02FFF6=ABEL.AI01:ABELPROC+#0012
 0B049B2C=MODULES.DK02:INITIALIZEP+#0014
 0B03D7A2=PROCS.EQ05:LIVEANDD+#0012


Fault address             FDFDFDFC (Not Found)
 MAU address hold register FDFDF78C
 Access protection mask    000F
 Peripheral interrupt mask 0055
 MAU error register        00D0
 MAU ctrl register         008D
 MAU aux ctrl register     0003
 Fault Indication Register 0080
 TRAP out of SYNC on active CPU 0.

 Trap occurred at Sep-10 18:07:32.

 Interrupt Stack Prefix:
 Trap  00042B10  SR= #0000, PC= 0D85CDD0, Format= #B008

 Instructions around trapped PC:
 0D85CDC8:   4EFB 6014 A807 0002 *0001 0006 0005 0004 0003

 Process Control Block:
 Unprotect count= 0, Unsuspended slices= 0, IO ints= 0,
 Total ticks= #20DD, Total ticks locked= #0D13,
 Timeslice= 3, Saved timeslice= 0, Readyq timestamp= #369B,
 Susp2= FFFF0000 FFFF0000, Timeq= FFFF0000 FFFF0000,
 Timeq0= #C1, Timeq1= #25, Used process queue= 0063E1A8,
Mb index= #0000, Parent mb= #2201 #30FF, Pref mb= #2201 #2100,
 CP= N, Alloc= Y, Initcomplete= Y, Cannotwait= Y,
 Traceok= N, Traceon= N, Trace was on= N, Immune= N,
 Procaudit= #0000, Language= 0, Enabled= Y,
 Stack desc= ADDR=009D2330 SIZE=0646 WORDS, Semas= #FFFF,
 PPV desc=   ADDR=009D2F76 SIZE=0006 WORDS, Semav= 0,
 Prio= 7, class= SYS  , slice= 5, Being timed= N,
 Suspitem= 009D2F36, Susp failed= N, Susp type= QDMISC,
 Woken on time= N, Will be stopped= N, Status= READY,
```

Responding to a CMTrap alarm (continued)

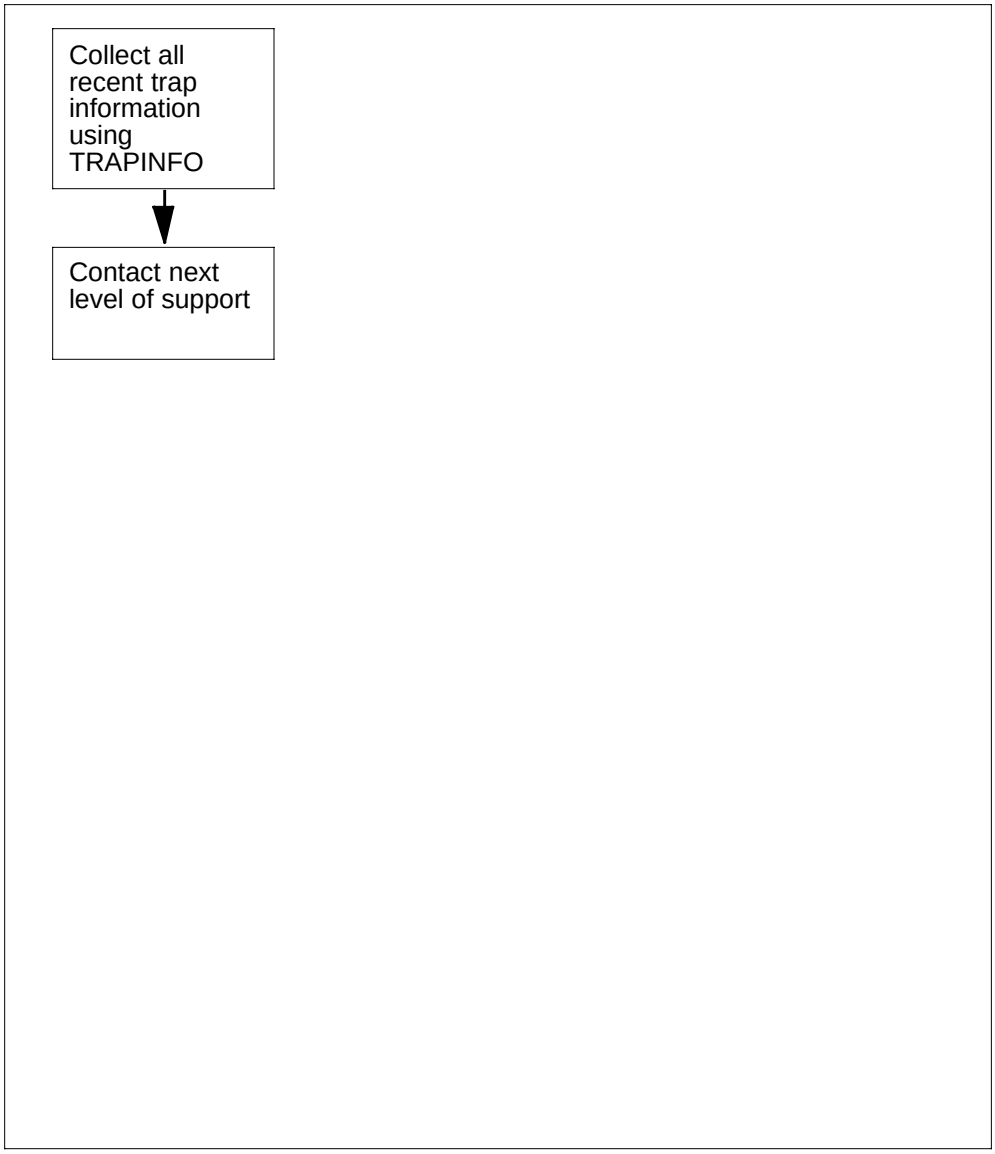
```
 Nested preempt= 0, Nested unprot= 0,
 First origid= N, Gbkgorig= #0000, Pref queue= FFFF0000.
Process Last Swapped in at 0005292A=SCHED.FA02:SCHEDULE+#005A

 Regsavearea:
 Lockcount= 0, Privcount= 0, Formato Extends= 0,
 PST register= 011FFB48, Alternate Stack= FFFF0000,
 Trace Flags= #0000, Process Time= #000000000000,
 Datareg012= FFFF0000 FFFF0000 FFFF0000.

 Permregs:
 lockintcount= #0000, suplockintcount= #0000,
 USL= 009D23B0, ISL= 00040C4C, SL= 009D23B0,
 USP= 009D2DD8, ISP= 00042B10,
 nestcount= #0001, intmask= #0000, permitmask= #007F,
 Undefined store pattern= #FDFD

 Registers:
 D0-3: #00000005 #0000000B #00000001 #00000002
 D4-7: #00000004 #0000006E #009F0006 #FFFF0000
 A0-3: #009D2DD0 #009D2D70 #041183A4 #00835A94
 A4-6: #00632A94 #009D2F2C #008AFFB0
 User Stack Traceback:
 0D85CDD0 (Procname Unknown), SB= 009D2F2C

 Corrupt or truncated stack frame. SB= 009D2F2C and stack is
from 009D2DD8 to
 009D2FBA.

 Store stack from 009D2DD8 to 009D2FBA:
 S.-000:009D2DD8: 0D85 CD80 0B6A 5BF4 0B6A 5BF4 0B6D 628C 0D85
D238 0B6A 5BF4
 S.-018:009D2DF0: 0D85 DA34 0D85 CF6C 0D85 D8D0 0D85 D504 0B6A
5BF4 0B6A 5BF4
 S.-030:009D2E08: 0B6D 6558 0B6A 5BF4 0B6A 5BF4 0B6A 5BF4 0B6A
5BF4 232A 0000
 S.-048:009D2E20: 0000 0008 011B AE6C 01AB BC74 0000 000B 000C
000C 000D 2E5C
 S.-060:009D2E38: 009D 2E60 0005 1A5E 0295 2E50 028B 57CC 01AD
56DC 009D 2E70
 S.-078:009D2E50: 009D 2E72 009D 0000 0B02 0000 0063 2FD4 009D
2E98 0005 51F0
 S.-090:009D2E68: 0B02 0000 0080 0796 0000 0004 0080 07A2 0000
0004 0005 2FD4
 S.-0A8:009D2E80: 004C D678 009D 2EBC 0B01 25DE 0D85 CCD8 009D
2E8C 0000 0003
 S.-0C0:009D2E98: 0D85 CCD8 009D 2E98 0000 0003 0080 0796 0000
0004 0080 05D0
 S.-0D8:009D2EB0: 0005 2C68 008A FFC4 0000 0003 009D 2EE0 0B04
BB8E 008A FFC4
 S.-0F0:009D2EC8: 008A FFC4 0B03 90B2 008A FFC4 0D85 CCD8 0014
0002 0D85 CCD8
 S.-108:009D2EE0: 009D 2EFC 0B04 7342 0014 0002 0D85 CCD8 009D
2F08 009D 2F76
 S.-120:009D2EF8: 01DA 5F1C 009D 2F2C 0B04 A51C 01DA 5F1C 0D85
CCD8 0000 9738
 S.-138:009D2F10: 009D 2F76 009D 2F76 0000 0005 011F FB48 0000
000F 0001 0000
```

Responding to a CMTrap alarm (continued)

```
 S.-150:009D2F28: 0001 2F74 009D 2F94 0B05 4044 0008 4502 2004
232A 0000 232A
 S.-168:009D2F40: 0099 2EFC 0B04 7342 0010 0002 0D85 84BC 009D
2F08 009D 2F76
 S.-180:009D2F58: 01DA 5F1C 009D 2F2C 0B04 A51C 01DA 5F1C 0D85
0000 0001 0000
 S.-198:009D2F70: 232A A51C 232A 009D 2320 0000 0005 232A FFFF
0001 01DA 5F1C
 S.-1B0:009D2F88: 0062 FE98 0000 0000 0004 FFFF 009D 2F9C 0B02
FFF6 009D 2FA4
 S.-1C8:009D2FA0: 0B04 9B2C 009D 2FAC 0B03 D7A2 FFFF 0000 FFFF
0000 0B04 9B18
 S.-1E0:009D2FB8: FFFF FFFF
 End of traceback.
```

Responding to a CMTrap alarm (end)

Flowchart for responding to a CMTrap alarm



Responding to a PrcOpt alarm

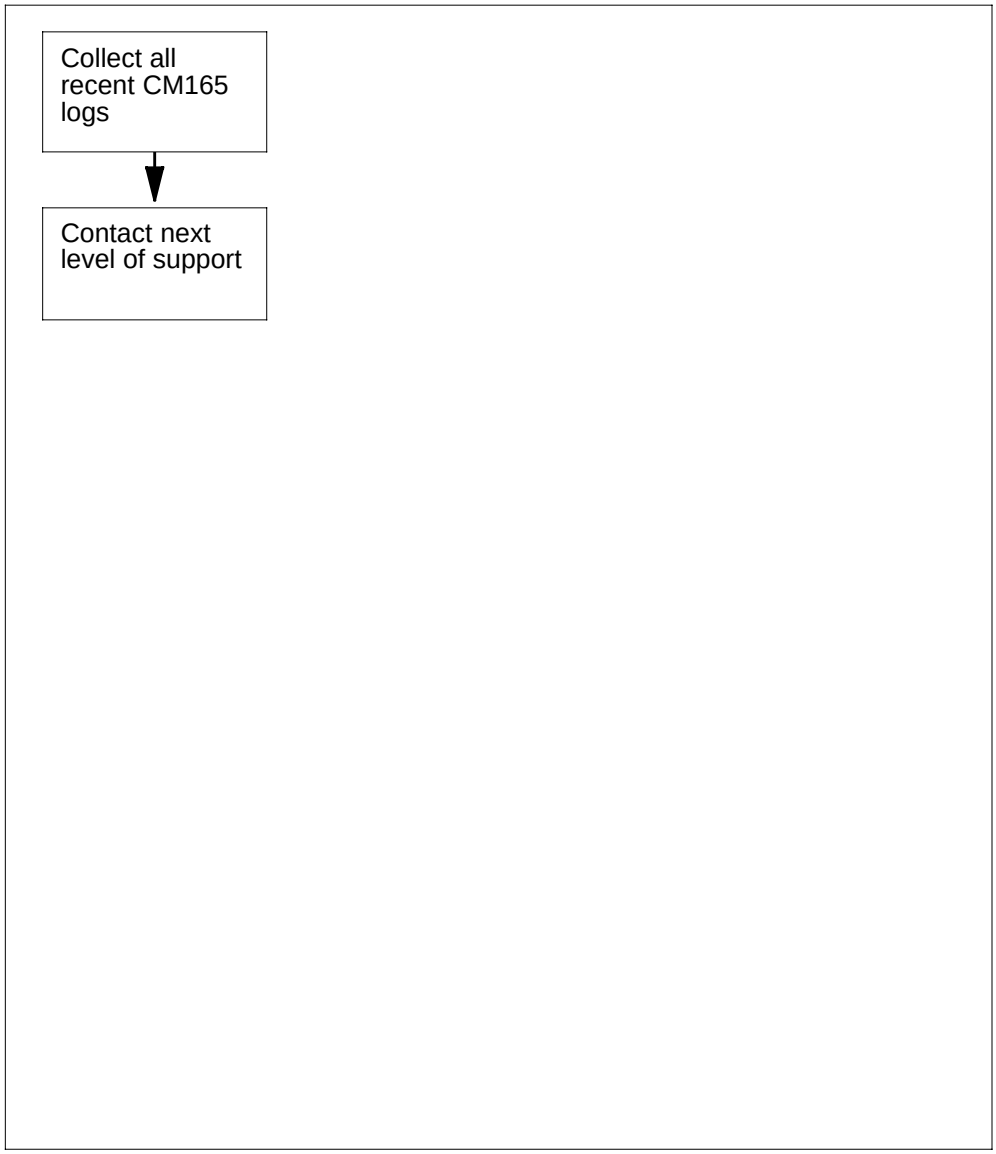
Application

The PEC numbers of the processor and memory cards installed in the switch must be the same as the processor selection datafill information. The system generates a PrcOpt alarm when the information is not the same. Nortel personnel can change this information.

Operating company personnel can install a new card to replace a card. The new card must have the same PEC and suffix as the card the operating company personnel replaced. When an upgrade occurs, contact Nortel. Nortel updates the processor option datafill.

Responding to a PrcOpt alarm (end)

Flowchart for Responding to a PrcOpt alarm



Troubleshooting a RExFlt alarm

Application

The system raises the CM RExFlt major alarm when a scheduled computing module (CM) routine exercise (REx) test does not complete.

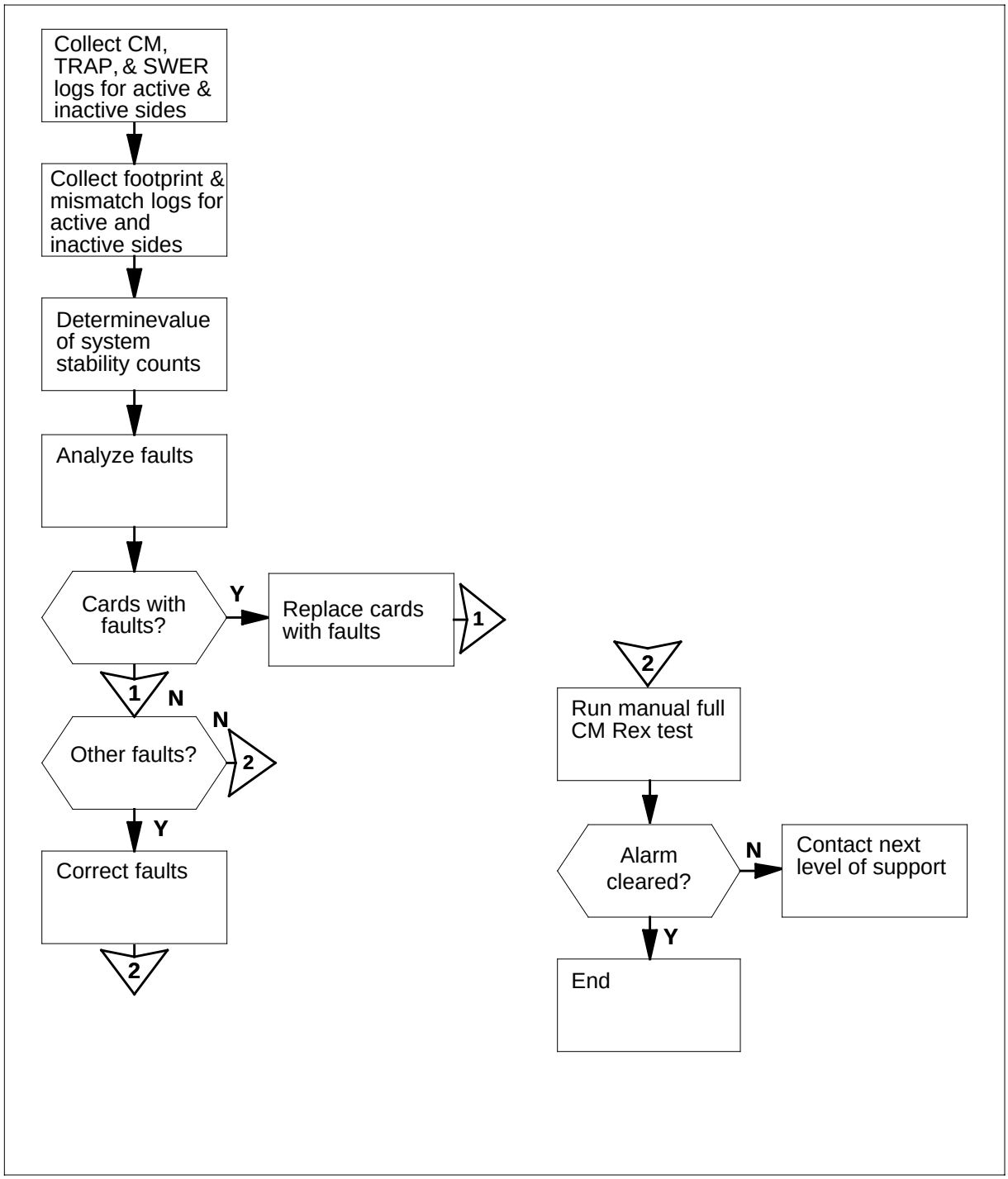
Reasons the CM REx test does not complete:

- one or more failed REx tests
- manual termination of REx testing
- one or more traps
- one or more mismatches
- one or more link closures
- an RMS timeout
- an environment error

The actions to perform to clear this alarm appear on the flowchart on the following page.

Troubleshooting a RExFlt alarm (end)

Summary of clearing a Troubleshooting a RExFlt alarm



Troubleshooting a RExSch alarm

Application

The system generates the RExSch alarm for the following reasons:

- Two consecutive automatic daily routine exercise (REx) tests are cancelled. The switch can detect conditions in the computing module (CM) that cause the REx test to fail. When this event occurs, the switch cancels the test before the test starts.
- Use datafill in table REXSCHED to disabled CMREx testing.

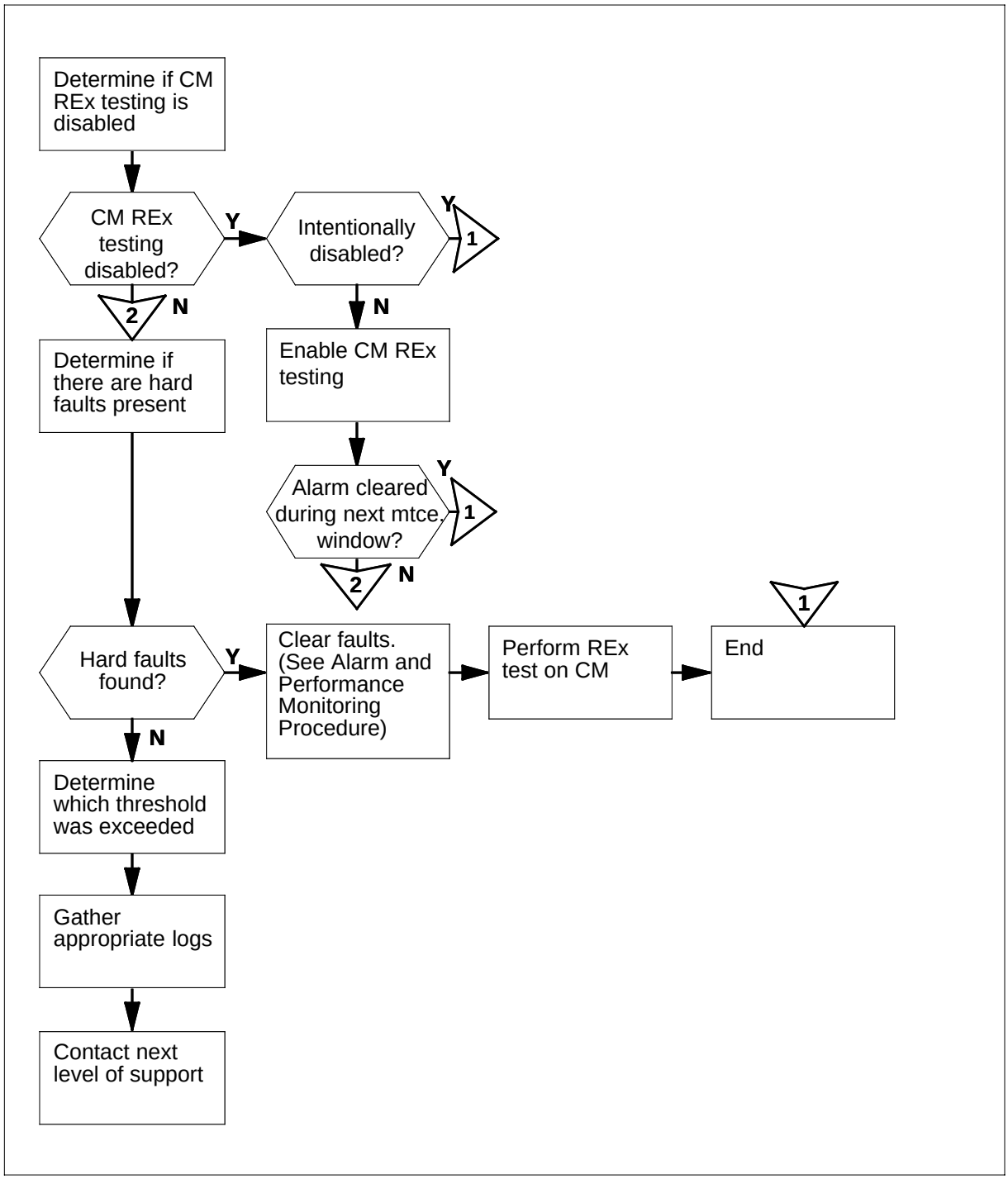
The conditions that cancel the REx test can be hard faults. The problem can be an exceeded threshold. Operating company personnel datafill the following thresholds. The thresholds to monitor the state of the CM:

- link closure count
- out-of-sync recovery mismatch count
- in-sync recovery mismatch count
- trap rate count
- processor memory fault count
- clock fault count
- canceled REx count

The steps to clear this type of alarm appear in the flowchart on the following page.

Troubleshooting a RExSch alarm (end)

Summary of troubleshooting a RExSch minor alarm



Troubleshooting an Autold alarm

Application

The system generates an Autold alarm when the correct automatic load (autold) route is not available for the computing module (CM). The path that the CM uses to access the system load module (SLM) to reload the switch does not exist.

The causes of the alarm can be hard and soft faults. Hard faults are normally problems with the SLM, or with the messaging path to the SLM. Soft faults are normally problems in datafill. The datafill does not allow the switch to determine the load route.

Personnel datafill the autoload route. If a value corresponds to an out–of–service element or hardware element that does not exist, the switch can reject the value. The switch can also generate an CM131 log. This process makes sure that the autoload route is correct when the route is set. After the load route is set, the system can raise an Autold alarm. The system raises the alarm when the device or any element in the message path to the device goes out of service.

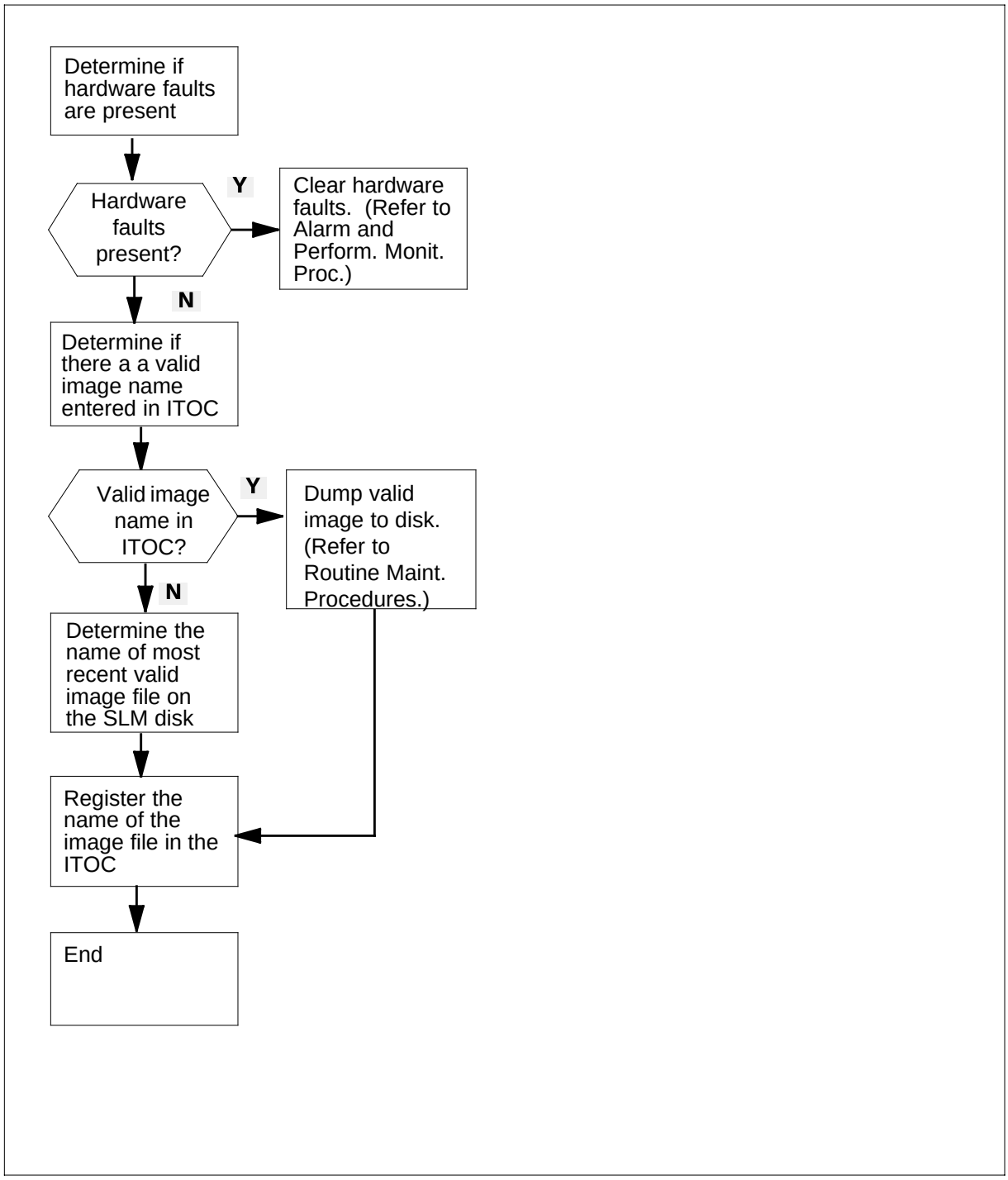
The following are soft faults that can generate the Autold alarm:

- a image that has defects on the SLM disk
- a correct image name does not exist in the image table of contents (ITOC)

The actions to clear this type of alarm appear in the flowchart on the following page.

Troubleshooting an Autold alarm (end)

Summary of troubleshooting an Autold alarm



Troubleshooting an IMAGE critical alarm

Application

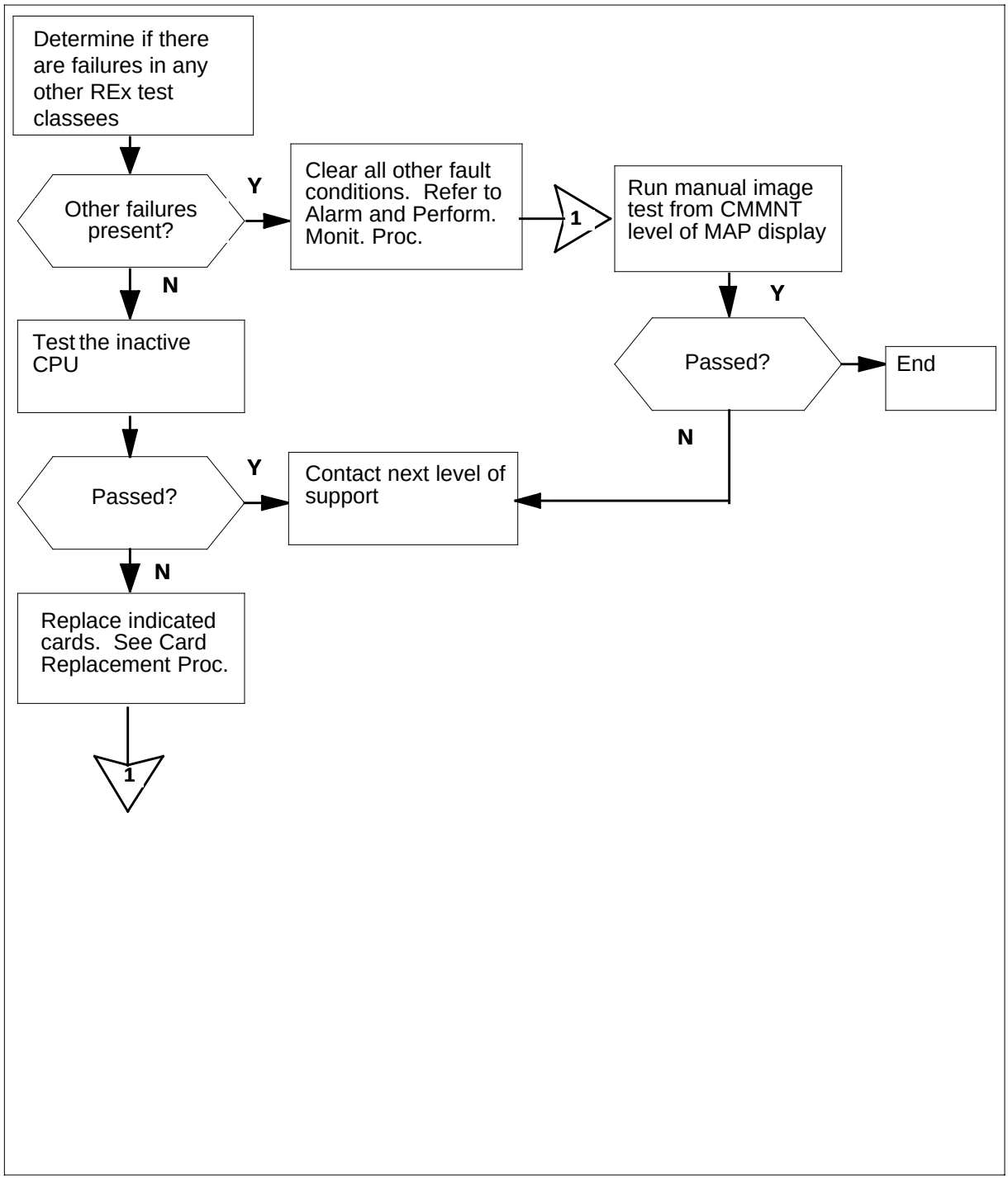
Image alarms appear after an automatic CM REx test. The CM REx test attempts to perform a restart to determine the state of the image on the inactive CPU. If the restart fails, the test fails, and the system generates the CM116 log. The system raises an IMAGE critical alarm.

When the CPU cannot perform a restart, or the restart fails, another fault can exist. Determine the root cause of the problem and clear the problem. The image alarm clears when you perform a manual image test from the CMMNT level of the MAP display.

The actions to clear this type of alarm appear on the flowchart on the following page.

Troubleshooting an IMAGE critical alarm (end)

Summary of troubleshooting an IMAGE critical alarm



Troubleshooting an StrAlc alarm

Application

The system generates the StrAlc alarm when the following conditions occur:

- a request to allocate a new data store vastarea and a maximum number of used data store vastareas is present.
- a request to locate a new program store vastarea and a maximum number of used program store vastareas is present.
- a request to allocate a new vastarea. The used data store and program store vastareas equals the maximum total number of used vastareas.
- a request to allocate a new vastarea. The total number of used requested store type vastareas, plus the requested area equals 512 Mbytes.

A threshold that causes the system to raise the alarm exists. A threshold that causes the system to lower the alarm exists. These two alarms are different. Thresholds that cause the system to lower the alarm are lower than the thresholds that cause the system to raise the alarm. The alarm remains visible until memory in the area that sets the alarm drops to ten vastareas below the threshold. The ten vastareas buffer makes sure a raised alarm remains raised under specified conditions. A raised alarm remains raised when used memory remains around a threshold value. This buffer does not allow the alarm to be toggled when number of used vastareas remain around the alarm that raises threshold.

When a different assignment decreases the number of used vast areas below a defined threshold, the system lowers the alarm. The number of used vast areas include the data store and/or the program store.

Components that can determine memory capacity include:

- SLM disk and tape capacity
- type of memory cards on a switch
- CM store allocator defined limits

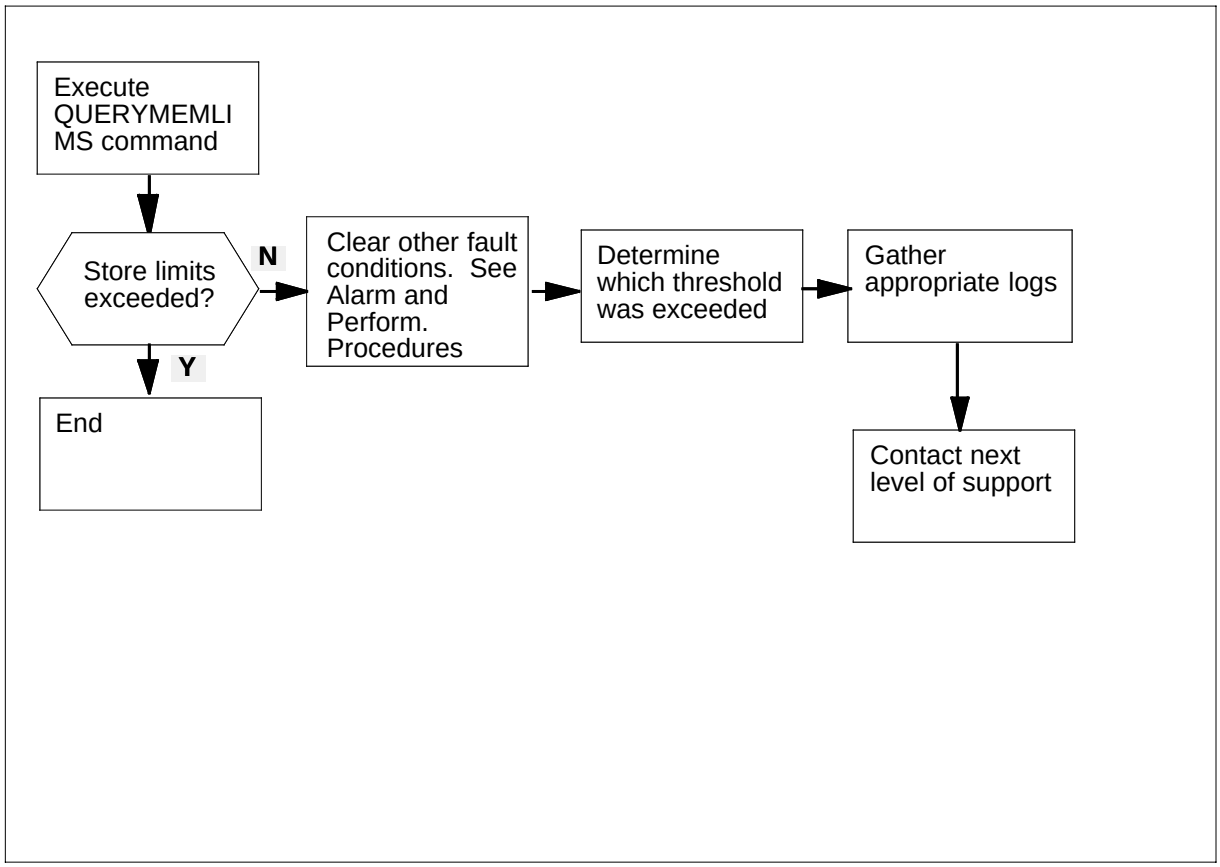
For more detailed information on memory threshold limits, see Table 8-8, "StrAlc alarm triggers for BASE07 and up" on page 8-17 in this document.

For more detailed information on the QUERYMEMLMS command, see the "User interface and commands chapter" of this document.

The steps to clear this type of alarm appear in the flowchart on the following page.

Troubleshooting an StrAlc alarm (end)

Summary of troubleshooting an StrAlc



List of terms

alarm (ALM)

An ALM is a signal that can be both visual and audible. The ALM signal alerts operating company personnel of a condition that requires attention.

application specific integrated controller (ASIC)

An ASIC is a component on the processor cards.

ASIC

See application specific integrated controller.

BAC

See bus access controller.

bus

A bus is an electrical connection that allows personnel to connect two or more wires or lines together.

bus access controller (BAC)

The BAC is the component of the CM CPU that accesses the A-bus.

cache memory management unit (CMU)

The CMU is a component of the CM CPU that manages the on-board memory.

card

A card is a plugged-in circuit pack that contains components. In a DMS switch, card is the name for a printed circuit pack or a printed circuit board.

CCITT

See Consultative Committee on International Telephony and Telegraphy (CCITT).

CCS

See common channel signaling (CCS).

CCS7

See Common Channel Signaling 7 (CCS7).

central processing unit (CPU)

A CPU is a hardware entity located in the computing module. The CPU contains the central data processor for the DMS-100 Family.

central side (C-side)

In DMS, the central side of a node faces away from the peripheral modules (PM) and toward the computing module (CM). *See* peripheral side.

clock subsystem

The clock subsystem is one of the message switch (MS) subsystems. The clock subsystem provides timing for each node in the DMS SN and SNSE systems.

CM

See computing module (CM).

CMIC

See computing module interface card (CMIC).

CMIC link

A CMIC link is the fiber optic cable that connects the message switch and the computing module.

CMMU

See cache memory management unit.

cold restart

Cold restart is an initialization phase during which the system removes and clears temporary storage. The system ends all calls and the peripheral processors (PP) clear all channel assignments.

common channel signaling (CCS)

The CCS is a signaling method in which information that relates to multiple labeled messages transmits over a single channel. This method uses time-division multiplex (TDM) digital techniques to transmit information.

Common Channel Signaling 7 (CCS7)

The CCITT defines this digital message network for signaling standards. This network separates call signaling information from voice signals. The system exchanges interoffice signaling over a separate signaling link.

computing module (CM)

The CM is the processor and memory of the dual-plane combined core (DPCC) used bythe DMS SN. Each CM consists of two CPUs with

associated memory that operate in a synchronous matched mode on two separate planes. Only one plane is active. The active plane maintains complete control of the system while the other plane is on standby.

computing module interface card (CMIC)

The CMIC is a card used by the message switch as an interface with the computing module. The CMIC uses fiber optics transmission links.

Consultative Committee on International Telephony and Telegraphy (CCITT)

The CCITT is from the French for International Telegraph and Telephone Consultative Committee (Comité Consultatif International Télégraphique et Télpéhonique).; Until March 1993, the CCITT was one of four permanent groups in the International Telecommunication Union (ITU). This committee discussed the technical issues for international telecommunications. The CCITT issued recommendations for improvement in standards and performance in the industry. The work of the CCITT continues in the ITU Telecommunication Standardization Sector (ITU-T).

CPU

See central processing unit (CPU).

C-side

See central side (C-side).

data store (DS)

The DS is one of the two elements of a DMS-100 memory. The DS is part of the central control complex (CCC). The DS contains transient information for each call. The DS also contains customer data and office parameters. The other main element of a DMS-100 memory is program store. *See* program store (PS), protected store (PROT).

DMS-bus

The DMS-bus is a messaging control component of the DMS SuperNode and DMS SuperNode SE. The DMS-bus components are two message switches (MS).

DMS-core

The DMS-core is a call management and system control part of the DMS SN and the DMS SNSE. The DMS-core consists of a computing module (CM) and a system load module (SLM).

DMS-link

The DMS-link is a networking software of the DMS SN and DMS SNSE. The DMS-link software consists of open and standard protocols that allow the switches to function in a multi vendor environment.

DMS SuperNode

The DMS SuperNode (SN) is a central control complex (CCC) for the DMS-100 switch. The main components of DMS SN are the computing module (CM) and the message switch (MS). Both components are compatible with the network module (NM), the input/output controller (IOC), and XMS-based peripheral modules (XPM).

DMS SuperNode SE

The DMS SuperNode SE (SNSE) is a smaller version of DMS SN designed to service smaller offices (maximum 20 000 lines). The DMS SNSE is based on current SN technology. All current applications of SN, including Common Channel Signaling 7 (CCS7) and international, can use the DMS SNSE. SNSE supports all SuperNode software features at a reduced call processing capacity.

DMS-X

The DMS-X is a link control protocol used with DS30A links for messaging between peripheral modules (PM).

DPCC

See dual-plane combined core (DPCC) cabinet.

DS

See data store (DS).

DS30

- The DS30 is a 10-bit 32-channel 2.048-Mb/s speech-signaling and message-signaling link. The DMS-100 Family switches use the DS30.
- The protocol by which DS30 links communicate.

DS512 fiber link

The DS512 fiber link is a fiber optic transmission link in the DMS SN and DMS SNSE. The DS512 connects the computing module to the message switch. One DS512 fiber link is equal to 16 DS30 links.

dual-plane combined core (DPCC) cabinet

The DPCC cabinet is one of the three cabinet models for the DMS SN processor. The DPCC contains a computing module (CM) shelf, two message switch (MS) shelves, and a system load module (SLM) shelf.

E2A

The E2A is telemetry equipment used to access the NT9X26 reset terminal interface paddle boards from a remote location.

ECC

See error checking and correction (ECC).

ENET

See Enhanced Network (ENET).

Enhanced Network (ENET)

The ENET is a channel-matrix time switch that provides pulse code-modulated voice and data connections between peripheral modules (PM). The ENET provides message paths to the DMS-bus components.

error checking and correction (ECC)

The ECC is a feature for CM memory that monitors the contents of the memories on both CM planes. The ECC monitors the contents of the memories on both CM planes to detect and correct single bit mismatches. The ECC does not interrupt service.

F-bus

See frame transport bus (F-bus).

fault indication register (FIR)

The FIR is a register in the fault and memory correctable mismatch logs MM100 and MFC 105. The FIR indicates the reason for the mismatch fault.

footprint (FP)

The FP is a facility that allows access to a series of buffers to gather data.

FP

See footprint (FP).

frame supervisory panel (FSP)

The FSP is a hardware device that accepts the frame battery feed and ground return from the power distribution center (PDC). The FSP distributes the battery feed to the shelves of the frame or bay where the battery feed is mounted. The FSP distributes the battery feed by secondary fuses and feeds. The FSP contains alarm circuits.

frame transport bus (F-bus)

The F-bus is an 8-bit bus that provides data communications between the message switch and the link interface units (LIU). To ensure readability the system provides 2 load-sharing F-buses. The system allocates each F-bus to either of the message switches.

FSP

See frame supervisory panel (FSP).

HMI

See human machine interface (HMI).

human machine interface

The human machine interface is a series of commands and responses used by the operating company personnel. Personnel use the human machine interface to communicate with the DMS-100 Family switches. The MAP terminal and other input/output devices (IOD) provide the human machine interface. Human machine interface, also known as man-machine interface.

ID PROM

The ID PROM is an element on each card or paddle board. Software reads these elements in order to identify the component.

input-output controller (IOC)

The IOC is an equipment shelf that provides an interface between a maximum of 36 I/O devices and the CM.

interrupt

An interrupt is a process that runs when triggered by a predetermined condition. The interrupt process will take priority over the software process.

IOC

See input-output controller (IOC).

JAM

A JAM is a state of activity for the CPU. The JAM state prevents the inactive CPU from resuming activity.

JNET

See juncture network (JNET).

junctored network (JNET)

The JNET is a time-division multiplexed system. The system allows the 1920 channels to switch for each network pair (completely duplicated). External junctors, internal junctors, and a digital network interconnecting (DNI) frame can establish more channels. The system can route channels directly or through alternative routes. The system can use other routes through junctors, a DNI frame, and software control. Capacity for a DMS-100 switch is 32 network pairs or 61 440 channels (1920 channels X 32 network pairs).

LH

See link handler (LH).

LIM

See link interface module (LIM).

link

- In a DMS switch, a connection between any two nodes.
- This four-wire group of conductors provides transmit and receive paths. A link provides transmit and receive paths for the serial speech or message data between components of DMS-100 Family switches. Speech links connect peripheral modules (PM) to the network modules (NM). Message links connect NM controllers or I/O controllers (IOC) to the central message controller (CMC).
- A logical switched virtual circuit (SVC). An X.25 communication cable carries a maximum of 256 logical SVCs.

link handler (LH)

The LH is a component of a port card used to interface with the link.

link interface module (LIM)

The LIM is a peripheral module (PM) that controls messaging between link interface units (LIU) in a link peripheral processor (LPP). The LIM controls messages between the LPP and the DMS-bus component. An LIM consists of two local message switches (LMS) and two frame transport buses (F-bus). One LMS operates in a load sharing mode with the other LMS to make sure the LIM is reliable. The LIM must be reliable in the event of an LMS failure. Each LMS has the capacity to carry the full message load of an LPP. Each LMS uses a dedicated F-bus to communicate with the LIUs in the LPP. *See* frame transport bus, link peripheral processor.

link interface shelf (LIS)

The LIS is an optional shelf in the DMS SuperNode SE that controls messaging between link interface units (LIU). Each LIS uses a dedicated F-bus to communicate with the LIUs.

link interface unit (LIU)

The LIU is a peripheral module (PM). This PM processes messages that enter and leave a link peripheral processor (LPP). Messages enter and leave an LPP through an separate signaling data link. *See* link interface unit for CCS7.

link interface unit for CCS7 (LIU7)

The LIU7 is a peripheral module (PM). This PM processes messages that enter and leave a link peripheral processor (LPP). These messages enter and leave an LPP through a single signaling data link. Each LIU7 consists of a set of cards and a paddle board provisioned from a link interface shelf. *See* link interface unit, link peripheral processor.

link peripheral processor (LPP)

The LPP is the DMS SN equipment frame for DMS-STP. The LPP that contains two types of peripheral modules (PM): a link interface module (LIM) and a link interface unit (LIU). For DMS-STP applications, link interface units for CCS7 (LIU7) are used in the LPP. *See* link interface module.

LIS

See link interface shelf (LIS).

LIU

See link interface unit (LIU).

LIU7

See link interface unit for CCS7 (LIU7).

LMS

See local message switch (LMS).

local message switch (LMS)

The LMS is a shelf in the link peripheral processor (LPP) frame or cabinet. The LMS transfers messages between application-specific units (ASU) in the LPP and provides access to the DMS-bus. Another name for the LMS is the link peripheral module (LIM).

log

A log is a message set by the DMS switch. The DMS switch sends a message when a significant event occurs in the switch or in one of the switch peripherals. A log report can include state and activity reports, reports on hardware and software errors, and test results. A log report can also includes other events or conditions that can affect the switch. The system can generate a log report in response to a system or manual action.

LPP

See link peripheral processor (LPP).

maintenance and administration position (MAP)

See MAP.

MAP

The MAP is a group of components that provides a user interface between operating company personnel and the DMS-100 Family switches. The interface consists of a visual display unit (VDU) and keyboard, a voice communications module, test facilities, and special furniture.

The MAP controls messages.

mate communication register (MCR)

The MCR is a 16-bit register. The two CM CPUs communicate through the MCR.

mate exchange bus (MEB)

The MEB is the A-32 bus that connects the two CM CPUs.

MAU

See memory access unit (MAU).

MC68000

The MC68000 is a series of CPU chips developed by the Motorola Corporation. The CPU chips are used on NT9X13 cards.

MC88100 RISC

The MC88100 RISC series of CPU chips developed by the Motorola Corporation. The CPU chips are used on NT9X10 cards.

MCR

See mate communication register (MCR).

MEB

See mate exchange bus (MEB).

memory access unit (MAU)

The MAU is a computing module (CM) CPU component. The MAU performs the following functions:

- controls and allows direct access to the static random access memory (SRAM) data cache for diagnostic purposes
- provides access protection over processor address space and parity generation
- provides access protection when the system checks for the data cache and selected backplane accesses

memory sparing

Memory sparing is the process in which the system disables a memory module that has faults. A new memory module is configured in the place of the memory module that has faults. A spare is the name of the replacement memory module.

message controller (MC)

The MC is a grouping of the hardware and software components that form the serial message links between the computing module (CM) and the message switch (MS).

message switch (MS)

The MS is a large-capacity communications facility. This facility functions as the messaging hub of the DMS SN and DMS SNSE. The MS controls messaging by MS concentrating and distributing messages and allows other nodes to communicate directly with each other.

mismatch handler

The mismatch handler is a software process initiated by a mismatch handler. The mismatch handler attempts to locate and clear any errors that occur.

mismatch interrupt

A mismatch interrupt is an interrupt the system generated by the mated processors of the DMS-100 Family switches lose synchronization.

MS

See message switch (MS).

network module (NM)

The network module is the basic building block of the DMS-100 Family switches. The NM accepts incoming calls and uses connection instructions from the CM to connect the incoming calls to the correct outgoing channels.

NM

See network module (NM).

node

A node is the terminal point of a link. A circuit can be a node in the context of another circuit in a module. The module can be a node in the context of another component of the network. Some common applications are as follows:

- in network topology, a node refers to a terminal of any branch of a network or a terminal common to a minimum of two branches of a network
- in a switched communications network, a node refers to the switching points, including patch and control facilities
- in a data network, a node refers to the location of a data station that connects between data transmission lines
- a node refers to a unit of intelligence in a system. In a DMS switch, this unit of intelligence includes the CPU, network module (NM), and the peripheral modules (PM).

OM

See operational measurements (OM).

operational measurements (OM)

The OM is the hardware and software resources of the DMS-100 Family switches. These switches control the collection and display of measurements taken from the operating system. The OM subsystem organizes the measurement data. The OM subsystem manages the transfer of the measurement data to displays and records. Operating company personnel can use this data to make decisions for maintenance, traffic, accounting, and provisioning.

paddle board (PB)

A PB is a small circuit card mounted on the back of a DMS equipment shelf. The PB carries the cable interfaces and local service functions, such as local clock sources and bus terminations.

PDC

See power distribution center (PDC).

PEC

See product engineering code (PEC).

peripheral module (PM)

The PM is any hardware module in the DMS-100 Family switches that provides an interface between external line, trunk, or service facilities. A PM contains peripheral processors (PP), which perform local routines and relieve the load on the CPU.

peripheral module controller (PMC)

The PMC is a logical grouping of the hardware and software elements used by the CM. The CM uses the PMC to communicate with the input/output devices.

peripheral side (P-side)

The P-side is the side located opposite the CM and faces the peripheral modules (PM). *See* central side.

PM

See peripheral module (PM).

PMC

See peripheral module controller (PMC).

power distribution center (PDC)

The PDC is the frame that contains the components for distributing office battery feeds to equipment frames of the DMS-100 Family switches. The PDC accepts cables A and B from the office battery and provides the protected secondary feeds to each frame or shelf. The PDC also contains

noise suppression and alarm circuits. The PDC provides a dedicated feed for the alarm battery supply.

product engineering code (PEC)

The PEC is a different eight-character identifier for each marketable hardware item manufactured by Nortel.

program store (PS)

In a DMS switch, the PS contains programmed instructions for the procedures required for processing, administration, and maintenance. The PS is one of the two elements of a DMS-100 memory. The other main element is data store. *See* data store.

protocol

A protocol is a set of rules, procedures, or standards. A protocol controls format and timing of data transmission between two devices.

PS

See program store (PS).

P-side

See peripheral side (P-side).

vastarea

Vastarea is an area of memory allocated to an exact function.

reload-restart

The reload-restart occurs when the system sets the software pointers in a program to reload the software into DMS-100 Family switches. The DMS-100 Family switches keep the office configuration and translation data and clears all the dynamic data.

reset terminal

See reset terminal interface (RTIF).

reset terminal interface (RTIF)

In a DMS SN switch, the RTIF is a user interface terminal that reboots the system. The RTIF monitors the state of the system. The RTIF can be a remote terminal connected to a modem or a local terminal. Another name for the RTIF is remote terminal interface.

restart

A restart established or executes a routine after a program error, a data error, or a machine failure. A restart normally involves returning checkpoints placed at intervals. In the event of a failure, the user can resume a job from the last checkpoint. A restart has an associated severity message that reflects the value of the reset resources. *See* cold restart, warm restart.

REx

See routine exercise (REx) test.

routine exercise (REx) test

The REx test is an automatic test performed at intervals on DMS equipment. Internal software initiates the test.

RTIF

See reset terminal interface (RTIF).

SCC

See SuperNode combined core (SCC) cabinet.

signaling transfer point (STP)

The STP is a node in a Common Channel Signaling 7 (CCS7) network that routes messages between nodes. Signaling transfer points transfer messages between incoming and outgoing signaling links. Signaling transfer points do not originate or terminate messages, with the exception of network management (NWM) information. Signaling transfer points are deployed in pairs. If one STP fails, the mate takes over. The mate makes sure that service continues without interruption.

SLM

See system load module (SLM).

STP

See signaling transfer point (STP).

SuperNode combined core (SCC) cabinet

The SCC is the DMS SuperNode SE cabinet. The SCC contains two message switches, a computing module, and system load module.

SWACT

See switch of activity (SWACT).

switch of activity (SWACT)

In a DMS fault tolerant system, the SWACT is a switch that changes the states of two identical devices. The SWACT changes the state of the two identical devices devoted to the same function. A SWACT makes an active device inactive and an inactive device active.

syslog

See system log (SYSLOG).

system load module (SLM)

The SLM is a mass storage system in a DMS SuperNode or DMS SuperNode SE that stores office images. The user can boot new loads or stored images into the computing module (CM) from the SLM.

system log (SYSLOG)

The SYSLOG is a log that contains a selection of reports from different logs after a reload-restart. The SYSLOG is the only log that remains after a reload-restart.

trap

A trap is a jump to a specified address. Hardware automatically activates a trap. The trap is not programmed, but the trap does have limits. The system makes a record of the location of the jump.

The firmware, software, or hardware detects the trap error condition and causes a trap interrupt. The process that runs stops on the instruction with the fault.

trap-interrupt

The system generates trap-interrupt when a hardware or software error occurs.

warm restart

Warm restart is an initialization phase during which the system removes and clears temporary storage. The system drops transient calls. The system allows calls in the talking state to continue.

DMS-100 Family

DMS SuperNode and DMS SuperNode SE Computing Module

CM Maintenance Guide

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