Critical Release Notice

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The content of this customer NTP supports the SN06 (DMS) software release.

Bookmarks used in this NTP highlight the changes between the LEC0015 baseline and the current release. The bookmarks provided are color-coded to identify release-specific content changes. NTP volumes that do not contain bookmarks indicate that the LEC0015 baseline remains unchanged and is valid for the current release.

Bookmark Color Legend

Black: Applies to new or modified content for LEC0015 that is valid through the current release.

Red: Applies to new or modified content for SN04 (DMS) that is valid through the current release.

Blue: Applies to new or modified content for SN05 (DMS) that is valid through the current release.

Green: Applies to new or modified content for SN06 (DMS) that is valid through the current release.

Attention!
Adobe® Acrobat® Reader™ 5.0 or higher is required to view bookmarks in color.

Publication History

June 2005

Standard release 11.03 for software release SN06 (DMS). Updates made for this release are shown below:

Volume 5

Added NTDX16AA (Q00946403)

March 2004

Standard release 11.02 for software release SN06 (DMS). Updates made for this release are shown below:

Volumes 1 – 3

No changes

Volume 4

Card NT9X30AB is Manufacture Discontinued and is replaced by new card NT9X30AC.

Volume 5

No changes

September 2003

Standard release 11.01 for software release SN06 (DMS). Updates made for this release are shown below:

Volumes 1 – 4

No changes

Volume 5

Updates were made to NT9X76AA according to CR Q00177945.

297-8991-805

DMS-100 Family

Hardware Description Manual

Volume 3 of 5

2001Q1 Standard 09.01 March 2001

NORTEL NETWORKS
How the world shares ideas.

DMS-100 Family

Hardware Description Manual

Volume 3 of 5

Publication number: 297-8991-805
Product release: 2001Q1
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Contents

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NT6X02DH through NT6X69AD (continued in Vol. 4)

NT6X02DH

Product description

The subscriber module SLC-96 (SMS) shelf provides a digital interface to remote control terminals in a digital loop carrier system. The digital loop carrier system is the subscriber loop concentrator (SLC). Business and residential applications can use the SMS shelf.

When integrated into the DMS-100 switch, the SLC-96 remote terminal is the remote carrier SLC-96 (RCS). This integrated configuration provides subscribers with the full digital resources of the DMS-100 switch. The SMS shelf does not requires separate control terminal (CT) cards for each subscriber line. The SMS shelf reduces main distribution frame (MDF) wiring and activity and saves office space. The CT serves only one remote terminal (RT). The SMS shelf can serve more than one RCS module.

The SMS shelf contains two units. One unit is active and provides the processing and control functions. The other unit is in standby mode and can take over call processing if a fault occurs in the active unit. The SMS replaces two line cards and one multiplexer to reduce the cost of the subscriber carrier.

The RCS can contain a maximum of eight digroups. The digroups provide DS-1 links to the SMS. Each digrou.. contains 24 pulse-code-modulation (PCM) channels that the time-division multiplex (TDM) assembles. Eight equipped digroups contain a total of 192 available channels (8 digroups $\times$ 24 PCM channels). Each of the two SMS message processors in the RCS uses a separate channel. A maximum of 190 channels are available for traffic.

The SMS and RCS exchange messages through a derived data link (DDL). The DDL is a 2.2-Kbps data path. The Fs framing bits from SCM superframes are replaced with DDL bits. The data path consists of these DDL bits. Two SCM superframes pass without changes by the system. The system removes the Fs bits of the next four superframes. The DDL link contains 24 DDL bits. The system removes the Fs bits from a card in the RCS or the time switch (TS) card in the SMS shelf.

The 8085 microprocessor of the A-bit/B-word DDL card sends DDL messages to the TS. The microprocessor extracts the DDL messages from incoming PCM. The DDL facility software in the signaling processor (SP) processes DDL messages.

The shelf provides an interface for RCSs. The shelf does not provide an interface to other remote systems. A standard DMS-100 single bay frame contains the SMS shelf pairs. The bay frame is the subscriber module equipment (SME) frame (NT6X01AA). The bay frame contains two pairs of shelves. Each pair of shelves is a module. The two lower shelves are both

module 0. Both of the upper shelves are module 1. Each node has a DS-1 link assigned. The node is a line appearance on a digital trunk (LDT) node.

The SMS shelf uses the SLC-96 DS-1 interface cards or filler faceplates for slots 1 to 5. Slot 13 contains an A/B interface card. Slot 14 contains a TS card. Slot 16 contains a filler faceplate or CLASS modem resource (CMR) card. Slot 18 contains a messaging card. Slot 19 contains a pad/ring card.

The SMS shelf has protection switching. Make sure communication continues between an SMS and an RCS. Protection switching makes sure communication continues if a DS-1 line that connects the SMS and the RCS fails. The RCS or SMS can initiate the protection switches. The module that detects the fault can initiate the protection switch. The switch operator can initiate the manual protection. The operator initiates the protection switch to place the switch out-of-service.

The SMS modules provide an interface to the enhanced network (ENET) through copper or optical fiber speech links. Both configurations require the NT6X69AC card. When the SMS connects to the ENET with optical fiber speech links, the SMS requires the following parts:

- the XPM DS-512 link control (NT6X40CA)
- the XPM DS-512 link card (NT6X40DA)
- the FXPM bracket assembly kit (NT6X02BU)

Parts

The SMS shelf contains the following parts:

- the NT0X50AA–Filler faceplate
- the NT2X70AE–Power converter
- the NT3X90AC–Device controller cooling interface unit
- the NT6X40BA–DS30 network interface (NI) card
- the NT6X40CA–DS30 NI card
- the NT6X40DA–DS30 NI card
- the NT6X41AA–Speech bus formatter
- the NT6X42AA–Channel supervision message (CSM) interface card
- the NT6X44AB–TS card
- the NT6X45BA–Master processor (MP) card
- the NT6X46BB–Signaling processor memory (SPM) card
- the NT6X47AC–Master processor memory (MPM) card

NT6X02DH (continued)

- the NT6X69AB–Messaging card
- the NT6X69AC–Messaging card
- the NT6X78AA–Class local area signaling service modem resource card
- the NT6X78AB–Class local area signaling service modem resource car
- the NT6X85AB–SLC-96 DS-1 interface card
- the NT6X86AA–A/B interface card

Design

The design of the NT6X02DH appears in the following table and the figure that follows the table.

The following table indicates the design of the NT6X02DH.

NT6X02DH parts (Sheet 1 of 5)

PEC	Slot	Description
NT0X50AA	1F-7F, 9F, 13F 15F-17F, 23F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the shelves. Each shelf contains a maximum of five spare card slots. Slots15 16 and 17 can access the signaling processor (SP) address bus and the parallel speech bus. Slots 13 and 19 do not have access.
NT2X70AE	25F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards in the shelf need. A power converter supplies +5 V and 12 V for the cards on the shelf. The power converters prevent loss of unduplicated cards during a power failure.
NT3X90AC	-	*Device controller cooling interface unit* The cooling inverter provides forced air for cooling.

NT6X02DH (continued)

NT6X02DH parts (Sheet 2 of 5)

PEC	Slot	Description
NT6X40BA	22F	*DS30 network interface card* The DS30 NI card is available as the NT6X40AA (8 ports) and the NT6X40AC (16 ports). The card provides a central-side (C-side) interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for defect isolation.
NT6X40CA	22F	*DS30 network interface card* The DS30 NI card is available as the NT6X40AA (8 ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for defect isolation.
NT6X40DA	22F	*DS30 network interface card* The DS30 NI card is available as the NT6X40AA (8 ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each card contains a looparound circuit for defect isolation.
NT6X41AA	21F	*Speech bus formatter* The speech bus formatter card contains a clock section and a formatting section. The clock section generates the 10.24-MHz shelf clock. The formatting section of the card provides parallel-to-serial conversion of coded voice signals. The CSM interface card sends the signals to the C-side links. The formatting section provides serial-to-parallel conversion of the coded voice signals from the C-side interface cards. The formatting section also provides network plane selection, parity error generation for test purposes and T1 clock generation.

NT6X02DH (continued)

NT6X02DH parts (Sheet 3 of 5)

PEC	Slot	Description
NT6X42AA	20F	*Channel supervision message* The CSM interface card performs several functions. The card removes the CSM bit from the C-side channels. The card assembles the CSM for each channel. The card inserts the CSM in the outgoing C-side bytes. The card performs parity checking on all incoming bytes and parity generation on all outgoing bytes.
NT6X44AB	14F	*Time switch* The TS converts between a serial stream and a parallel stream. The DS30 interface card or DS-1 interface card sends or receives the serial stream. The internal speech bus uses the parallel stream. When SP controls TS, the TS associates DS30 and DS-1 interface cards with time slots on the parallel speech bus. The TS also transfers data between the associated channel and the time slot.
NT6X45BA	8F, 12F	*Master processor card* The MP card runs the programs that operate and maintain a peripheral module. The MP card collects digits, assigns channels and reads messages for the central control complex and peripheral module.
NT6X46BB	11F	*Signaling processor memory card* The SPM card contains RAM that stores data and software applications.
NT6X47AC	9F, 10F	*Master processor memory card* The MPM card contains RAM that stores data and software applications for the MP and the SP. The SP can access a part of the MP memory with the memory management unit of the MP.

NT6X02DH (continued)

NT6X02DH parts (Sheet 4 of 5)

PEC	Slot	Description
NT6X69AB	18F	*Messaging card* The messaging card provides interface for the parallel speech bus. The messaging card extracts control messages that the control module (CM) sends on channel zero.
NT6X69AC	18F	*Messaging card* The messaging card provides interface for the parallel speech bus. The messaging card extracts control messages that the CM sends on channel zero.
NT6X78AA	16F	*Custom local area signaling service modem resource card* The CLASS modem resource (CMR) card provides residential (RES) enhanced features. Slot 16 of the SMS shelf can contain the CMR card. The calling number delivery (CND) feature requires the CMR card.
NT6X78AB	16F	*Custom local area signaling service modem resource card* The CMR card provides RES enhanced features. Slot 16 of the SMS shelf can contain the CMR card. The CND feature requires the CMR card.

NT6X02DH (continued)

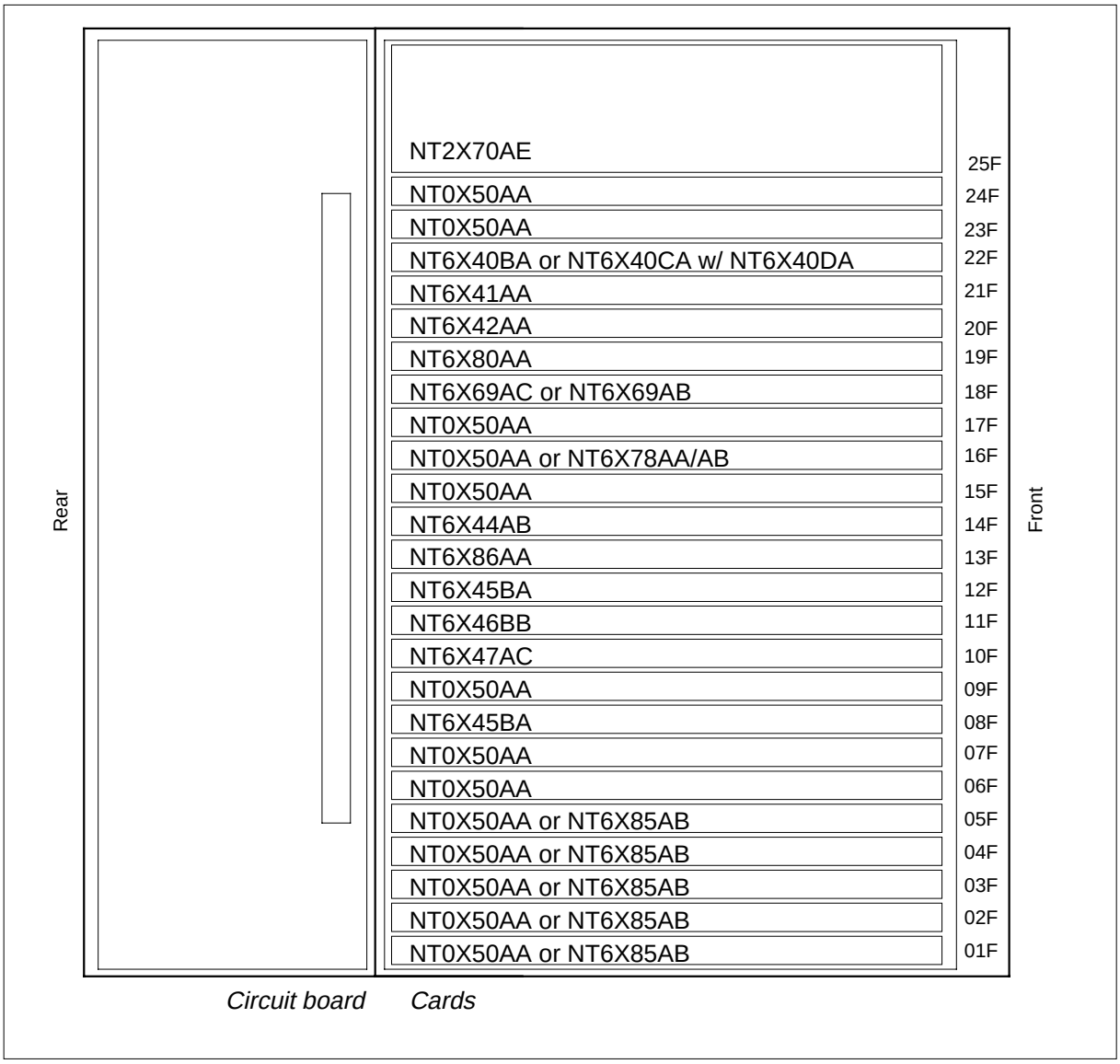
NT6X02DH parts (Sheet 5 of 5)

PEC	Slot	Description
NT6X85AB	5F	*SLC-96 DS-1 interface card* The SLC-96 DS-1 interface card contains two DS-1 ports. Each SMS module contains one to ten cards. The DS-1 interface card operates in DDL mode and non-DDL mode. In the DDL mode, the card converts transistor-transistor logic (TTL)-level PCM values of the SMS TS to bipolar levels of the DS-1 link. The card also converts the bipolar levels of the DS-1 link to the TTL-level PCM values of the SMS TS. The card also inserts DDL supervisory message bits into outgoing (network to SLC-96) DS-1 framing = bit time slots. The card extracts the corresponding bits from incoming (SLC-96 to network) frames. In non-DDL mode, DDL message capability is that same as that of a DS-1 line interface card. Each port provides a two-way voice, data, and signaling interface. The card provides looparound paths for each DS-1 port to isolate faults. The card transmits local alarm, detects remote alarms and error conditions. Error conditions include the loss of synchronization, bipolar error and slip.
NT6X86AA	13F	*A/B interface card* The A/B interface card inserts and extracts A and B bits from the PCM stream. The system uses the signaling bits for each channel to detect ringing, hook status detection and ANI and coin functions.

The following figure indicates the design of the NT6X02DH.

NT6X02DH (end)

NT6X02DH parts



NT6X02DJ

Description

The subscriber module SLC-96 (SMS) shelf that provides a digital interface to remote control terminals in a digital loop carrier system is the subscriber loop concentrator (SLC). Business and residential applications use the SMS shelf.

When integrated in the DMS-100 switch, the SLC-96 remote terminal becomes the remote carrier SLC-96 (RCS). This integrated configuration provides subscribers with the full digital resources of the DMS-100 switch. The SMS shelf does not require separate control terminal (CT) cards for each subscriber line. The SMS shelf reduces main distribution frame (MDF) wiring and activity, and saves office space. The CT serves one remote terminal (RT). The SMS shelf can serve multiple RCS modules.

The SMS shelf contains two units. One unit is active and provides the processing and control functions. The other unit is in standby mode and can take over call processing if a fault occurs in the active unit. The SMS replaces two line cards and one multiplexer to reduce the cost of the normal subscriber carrier.

Each RCS contains a maximum of eight digroups. The digroups provide DS-1 links to the SMS. Each digroup contains 24 pulse code modulation (PCM) channels assembled by time-division multiplex (TDM). Eight equipped digroups contain a total of 192 available channels (eight digroups $\times$ 24 PCM channels). Each of the two SMS message processors in the RCS uses a separate channel. A maximum of 190 channels are available for traffic.

The SMS and RDS exchange messages over a special data link called a derived data link (DDL). The DDL is a 2.2 kbit/s data path. Remove Fs framing bits from SCM superframes and replace the Fs bits with DDL bits to form the DDL. In the SMS-RCS subsystem, two SCM superframes pass without changes by the system. Remove the Fs bits of the next four superframes. Replace the Fs bits with DDL bits. A total of 24 DDL bits comprise the DDL link. The Fs bits are in a card in the RCS or the time switch (TS) card in the SMS shelf.

The 8085 microprocessor of the A-bit/B-word DDL card sends DDL messages to the timing switch(TS). The microprocessor extracts the DDL messages from incoming PCM. The DDL facility software in the signaling processor (SP) processes DDL messages.

The shelf contains an interface for RCSs only. The shelf does not provide an interface to any other remote system. A standard DMS-100 single bay frame houses the SMS shelf pairs. This bay is the subscriber module equipment (SME) frame (NT6X01AA). The bay contains two pairs of shelves, and each

pair is a module. The lower two shelves are module 0 and the two upper shelves are module 1. Each node has a DS-1 link assigned to the node the link serves. The node is a line appearance on a digital trunk (LDT) node.

The SMS shelf uses SLC-96 DS-1 interface cards or filler faceplates for slots 1 through 7. The SMS shelf uses an A/B interface card in slot 13 and a TS card in slot 14. In slot 16, the SMS shelf uses a filler faceplate or a CLASS modem resource (CMR) card. Slot 18 contains a messaging card. Slot 19 contains a pad/ring card.

The SMS shelf has protection switching to make sure communication continues between an SMS and an RCS. Protection switching makes sure communication continues when the DS-1 line that connects the SMS and RCS fails. The RCS or SMS can automatically start protection switches. The module that detects the fault failure starts the protection switch. The switch operator can also start a manual protection switch when the operator must put the switch OOS.

The SMS modules also provide an interface to the enhanced network (ENET) through copper or optical fiber speech links. Both configurations require the NT6X69AC card. When the SMS connects to the ENET with optical fiber speech links, the SMS requires the three following parts:

- the XPM DS-512 link control (NT6X40CA),
- the XPM DS-512 link card (NT6X40DA)
- the FXPM bracket assembly kit (NT6X02BU)

Parts

The SMS shelf contains the following parts:

- NT0X50AA–Filler faceplate
- NT2X70AD–Power converter
- NT2X70AE–Power converter
- NT3X90AC–Device controller cooling inverter unit
- NT6X40BA–DS30 network interface (NI) card
- NT6X40CA–DS30 NI card
- NT6X40DA–DS30 NI card
- NT6X41AA–Speech bus formatter
- NT6X42AA–Channel supervision message (CSM) interface card
- NT6X44AB–TS card

NT6X02DJ (continued)

- NT6X45AC–Master processor (MP) card
- NT6X45BA–MP card
- NT6X45CA–MP card
- NT6X46BB–Signaling processor memory (SPM) card
- NT6X47AC–Master processor memory (MPM) card
- NT6X69AB–Messaging card
- NT6X69AC–Messaging card
- NT6X78AA–Class local area signaling service modem resource card
- NT6X78AB–Class local area signaling service modem resource car
- NT6X85AB–SLC-96 DS-1 interface card
- NT6X86AA–A/B interface card

Design

The design of the NT6X02DJ appears in the following table.

NT6X02DJ parts (Sheet 1 of 6)

PEC	Slot	Description
NT0X50AA	1F-to-7F, 9F, 13F 15F-to-17F, 23F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the shelves. Each shelf contains a maximum of five spare card slots. Slots 15, 16, and 17 can access the signaling processor (SP) address bus and the parallel speech bus does not have access. Slots 13 and 19 do not have access.
NT2X70AD	25F	*Power converter* The power converter converts the -48V dc to the lower voltage that the circuit cards in the shelf require. Each power converter supplies +5V and 12V to the cards on the shelf. The power converters prevent loss of unduplicated cards during a power failure.

NT6X02DJ (continued)

NT6X02DJ parts (Sheet 2 of 6)

PEC	Slot	Description
NT2X70AE	25F	*Power converter* The power converter converts the -48V dc to the lower voltage that the circuit card in the shelf require. Each power converter supplies +5V and 12V for the cards on the shelf. The power converters supply power to prevent loss of unduplicated cards during a power failure.
NT3X90AC	–	*Device controller cooling inverter unit* The cooling inverter provides forced air cooling.
NT6X40BA	22F	*DS30 network interface card* The DS30 NI card is available in two versions. The two versions are the NT6X40AA (eight ports) and the NT6X40AC (16 ports). The card provides a central-side (C-side) interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.
NT6X40CA	22F	*DS30 network interface card* The DS30 NI card is available in two versions. The two versions are the NT6X40AA (eight ports) and the NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.
NT6X40DA	22F	*DS30 network interface card* The DS3 NI card is available in two versions. The two versions are the NT6X40AA (eight ports) and the NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.

NT6X02DJ (continued)

NT6X02DJ parts (Sheet 3 of 6)

PEC	Slot	Description
NT6X41AA	21F	*Speech bus formatter* The speech bus formatter card contains a clock section and a formatting section. The clock section generates the 10.24 MHz shelf clock. The formatting section provides parallel-to-serial conversion of the coded voice signals. The CSM interface card sends the coded voice signals to the C-side links. The formatting section provides serial-to-parallel conversion of the coded voice signals from the C-side interface cards. The formatting section also provides network plane selection, parity error generation for test purposes, and T1 clock generation.
NT6X42AA	20F	*Channel supervision message* The CSM interface card performs several functions. The functions of the CSM card are as follows: • extracts the CSM bit from the C-side channels • assembles the CSM for each channel • inserts the CSM in the outgoing C-side bytes • performs parity checks on all incoming bytes • parity generation on all outgoing bytes
NT6X44AB	14F	*Time switch* The timeswitch (TS) converts between a serial stream and a parallel stream. The DS30 interface card or the DS-1 interface card sends or receives the serial stream. The internal speech bus uses the parallel stream. When the SP controls the TS, the TS associates the DS30 interface cards and DS-1 interface cards. The TS associates the cards with the time slots on the parallel speech bus. The TS transfers data between the associated channel and the time slot.

NT6X02DJ (continued)

NT6X02DJ parts (Sheet 4 of 6)

PEC	Slot	Description
NT6X45AC	8F, 12F	*Master processor card* The MP card runs the programs that operate and maintain a peripheral module. The MP card collects digits, assigns channels, and interprets messages for the central control complex and peripheral module.
NT6X45BA	8F, 12F	*Master processor card* The MP card runs the programs that operate and maintain a peripheral module. The MP card collects digits, assigns channels, and interprets messages for the central control complex and peripheral module.
NT6X45CA	8F, 12F	*Master processor card* The MP card runs the programs that operate and maintain a peripheral module. The MP card collects digits, assigns channels, and interprets messages for the central control complex and peripheral module.
NT6X46BB	11F	*Signaling processor memory card* The SPM card contains RAM storage data and software applications.
NT6X47AC	9F, 10F	*Master processor memory card* The MPM card contains RAM storage data and software applications for the MP and the SP. The SP accesses a part of the MP memory with the memory management unit of the SP.
NT6X69AB	18F	*Messaging card* The messaging card provides interface for the parallel speech bus and extracts control messages from the control module (CM) on channel zero.
NT6X69AC	18F	*Messaging card* The messaging card provides interface for the parallel speech bus and extracts control messages from the CM on channel zero.

NT6X02DJ (continued)

NT6X02DJ parts (Sheet 5 of 6)

PEC	Slot	Description
NT6X78AA	16F	*Custom local area signaling service modem resource card* The CLASS modem resource (CMR) card provides residential (RES) enhanced features. The SMU shelf can use the CMR card in slot 16 of the SMS shelf. Use the CMR card if the calling number delivery (CND) feature requires the CMR card.
NT6X78AB	16F	*Custom local area signaling service modem resource card* The CMR card provides different RES enhanced features. The SMU shelf can use this card in slot 16 of the SMU shelf. Use the CMR card if the CND feature is provisioned.
NT6X85AB	5F	*SLC-96 DS-1 interface card* The SLC-96 DS-1 interface card contains two DS-1 ports. Each SMS module can have a supply of one to ten cards. The DS-1 interface card operates in one of two modes, DDL mode and not in DDL mode. In the DDL mode, the card converts transistor-transistor logic (TTL)-level PCM values of the SMS TS. The card converts TTL values to bipolar levels of the DS-1 link, and the bipolar level to TTL-level values. The card inserts DDL supervisory message bits to outgoing (network to SLC-96) DS-1 framing = bit time slots. The card extracts the corresponding bits from incoming (SLC-96 to network) frames. In non-DDL mode, DDL message capability is the same as a DS-1 line interface card. Each port provides a two-way voice, data and signaling interface. The card provides looparound paths for each DS-1 port to isolate faults. The card also provides local alarms and detects remote alarms and error conditions like loss of synchronization, bipolar error, and slip.

NT6X02DJ (continued)

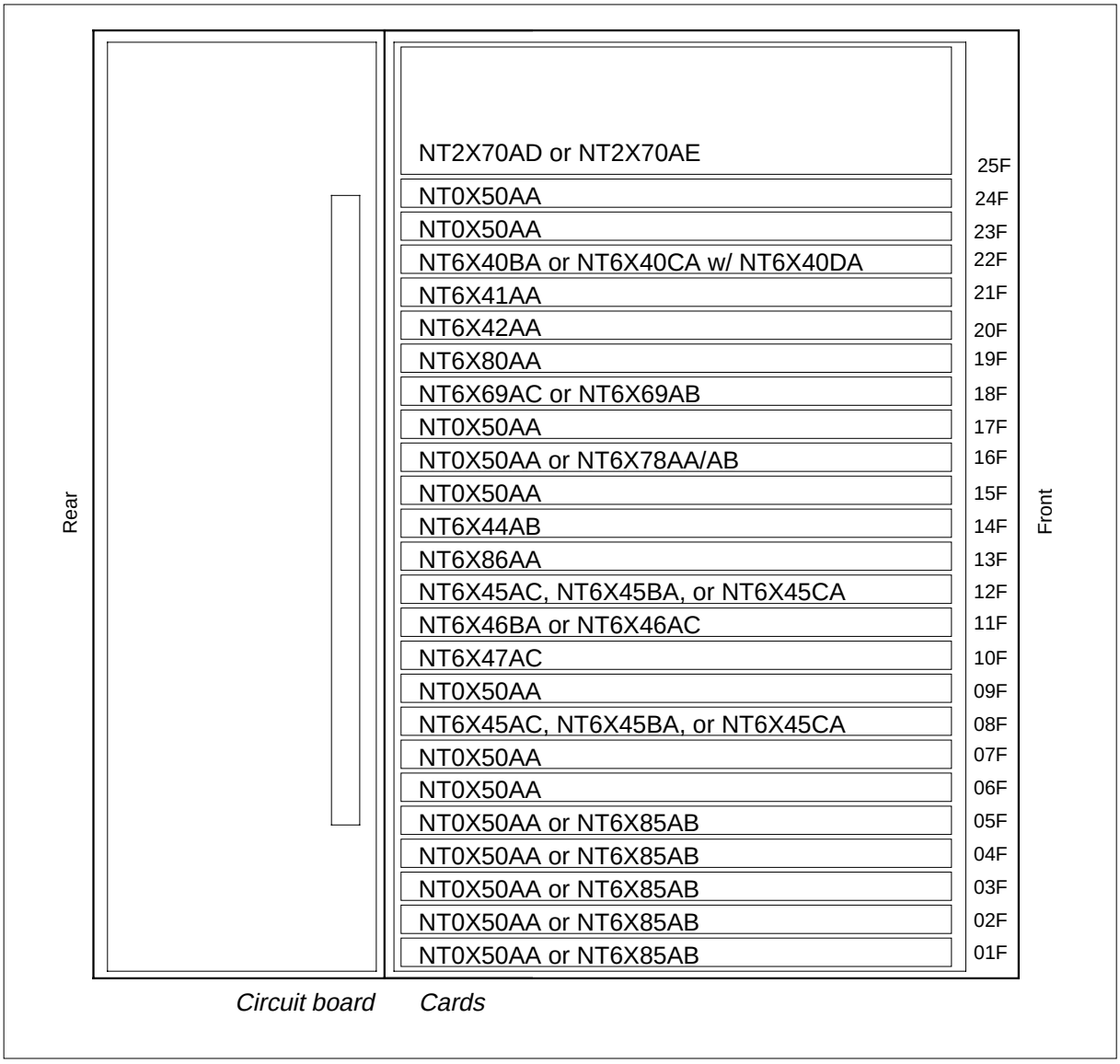
NT6X02DJ parts (Sheet 6 of 6)

PEC	Slot	Description
NT6X86AA	13F	*A/B interface card* The A/B interface card inserts and extracts A bits and B bits from the PCM stream. The system uses the signaling bits for each channel for ringing, hook status detection, and ANI and coin functions.

The design of the NT6X02DJ appears in the following figure.

NT6X02DJ (end)

NT6X02DJ parts



NT6X02EA

Description

The subscriber carrier module urban (SMU) shelf provides a digital interface to urban remote control terminals in a digital loop carrier system. The digital loop system is the subscriber loop concentrator (SLC). Business and residential applications use the SMU shelf.

When integrated in the DMS-100 switch, the DMS-1 urban remote terminal becomes the remote carrier urban (RCU) module. The DMS-100 switch offers this integrated configuration that provides subscribers with full digital resources. The SMU shelf does not require a separate control terminal (CT) card for each subscriber line. The SMU shelf reduces main distribution frame (MDF) wiring and activity. The SMU shelf saves office space. The CT serves one remote terminal (RT). The SMU shelf can serve multiple RCU modules.

The SMU shelf contains two units. One unit is active and provides the processing and control functions. The other unit is in standby mode and can take over call processing if a fault occurs in the active unit. The SMU replaces two line cards and one multiplexer to reduce the cost of the normal subscriber carrier.

Each RCS includes a maximum of eight digroups. The digroups provide DS-1 links to the SMS. Each digroup consists of 24 pulse code modulation (PCM) channels assembled by time-division multiplex (TDM). Eight equipped digroup cards contain 192 available channels (eight digroups × 24 PCM channels). Each of the two SMS message processors in the RCS uses a separate channel. A maximum of 190 channels are available for traffic.

The shelf provides an interface for RCUs only. The shelf does not provide an interface to any other remote system. A standard DMS-100 single bay frame houses the SMU shelf pairs. This bay is the subscriber module equipment (SME) frame (NT6X01AA). The bay contains two pairs of shelves, and each pair is a module. The lower two shelves are module 0 and the two upper shelves are module 1. Each module is . Each node has a DS-1 link assigned to the node the link serves. The node is a line appearance on a digital trunk (LDT) node.

The SMU shelf uses DS-1 interface cards or filler faceplates for slots 1 through 5. The SMU shelf can use filler faceplates in slots 6, 7, and 13.

The SMU modules can provide an interface to the enhanced network (ENET) by use of copper or fiber speech links. Both configurations can use the

NT6X02EA (continued)

NT6X69AC card. When the SMU uses optical fiber speech links to connect to the ENET, the following three parts are necessary for connection:

- XPM DS-512 link control (NT6X40CA)
- XPM DS-512 link card (NT6X40DA)
- FXPM bracket assembly kit (NT6X02BU)

Parts

The SMU shelf contains the following parts:

- NT0X50AA–Filler faceplate
- NT2X70AE–Power converter
- NT3X90AC–Device controller cooling inverter unit
- NT6X40AA–DS30 network interface (NI) card
- NT6X40AC–DS30 NI card
- NT6X41AA–Speech bus formatter
- NT6X42AA–Channel supervision message (CSM) interface card
- NT6X44CA–Time switch (TS)
- NT6X45AC–Master processor (MP) card
- NT6X45BA–MP card
- NT6X46BA–Signaling processor memory (SPM) card
- NT6X47AC–Master processor memory (MPM) card
- NT6X69AB–Messaging card
- NT6X78AA–Custom local area signaling service modem resource card
- NT6X78AB–Custom local area signaling service modem resource card
- NT6X80BA–Pad/ring
- NT6X85AB–DS-1 interface card

NT6X02EA (continued)

Design

The design of the NT6X02EA appears in the following table.

NT6X02EA parts (Sheet 1 of 6)

PEC	Slot	Description
NT0X50AA	1F-7F, 9F, 13F 15F-17F, 23F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the shelves. Each shelf contains a maximum of five spare card slots. Slots 15, 16, and 17 have access to the signaling processor (SP) address bus and the parallel speech bus. Slots 13 and 19 do not have access.
NT2X70AE	25F	*Power converter* The power converter converts the -48Vdc to the lower voltage that the circuit cards in the shelf require. Each power converter supplies +5V and 12V for the cards on the shelf. The power converters supply power to the DS-1 cards to prevent loss of unduplicated cards during a power failure.
NT3X90AC	-	*Device controller cooling inverter unit* The cooling inverter provides forced air cooling.
NT6X40AA	22F, 23F	*DS30 network interface card* The DS30 NI card is available in two versions. The two versions are the NT6X40AA (eight ports) and the NT6X40AC (16 ports). The card provides a central-side (C-side) interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.

NT6X02EA (continued)

NT6X02EA parts (Sheet 2 of 6)

PEC	Slot	Description
NT6X40AB	22F, 23F	*DS30 network interface card* The DS30 NI card is available in two versions. The versions are the NT6X40AA (eight ports) and the NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.
NT6X40AC	22F	*DS30 network interface card* The DS30 NI card is available in two versions. The versions are the NT6X40AA (eight ports) and the NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.
NT6X41AA	21F	*Speech bus formatter* The speech bus formatter card contains a clock section and a formatting section. The clock section generates the 10.24 MHz shelf clock. The formatting section provides parallel-to-serial conversion of the coded voice signals. The CSM interface card sends these coded voice signals to the C-side links. The card provides serial-to-parallel conversion of the coded voice signals. The formatting section provides network plane selection, parity error generation for test purposes, and T1 clock generation.

NT6X02EA (continued)

NT6X02EA parts (Sheet 3 of 6)

PEC	Slot	Description
NT6X42AA	20F	*Channel supervision message* The CSM interface card performs several functions. The functions of the CSM interface card are as follows: • extracts the CSM bit from the C-side channels • assembles the CSM for each channel • inserts the CSM in the outgoing C-side bytes • performs parity checks on all incoming bytes • parity generation on all outgoing bytes
NT6X44CA	14F	*Time switch* The timeswitch (TS) converts between a serial stream and a parallel stream. The DS30 interface card or the DS-1 interface card sends or receives the serial stream. The internal speech bus uses the parallel stream. When the SP controls the TS, the TS associates the DS30 interface cards and DS-1 interface cards. The TS associates the cards with the time slots on the parallel speech bus. The TS transfers data between the associated channel and the time slot.
NT6X45AF	8F, 12F	*Master processor card* The MP card runs the programs that operate and maintain a peripheral module (PM). The MP card collects digits, assigns channels, and interprets messages for the control central complex and peripheral module (PM).
NT6X45AC	8F, 12F	*Master processor card* The MP card runs the programs that operate and maintain a peripheral module. The MP card collects digits, assigns channels, and interprets messages for the central control complex and PM.

NT6X02EA (continued)

NT6X02EA parts (Sheet 4 of 6)

PEC	Slot	Description
NT6X45BA	8F, 12F	*Master processor card* The MP card runs the programs that operate and maintain a peripheral module. The MP card collects digits, assigns channels, and interprets messages for the central control complex and PM.
NT6X45CA	8F, 12F	*Master processor card* The MP card runs the programs that operate and maintain a peripheral module. The MP card collects digits, assigns channels, and interprets messages for the central control complex and PM.
NT6X46AC	11F	*Signaling processor memory card* The SPM card contains RAM storage data and software applications.
NT6X46BA	11F	*Signaling processor memory card* The SPM card contains RAM storage data and software applications.
NT6X47AB	9F, 10F	*Master processor memory card* The MPM card contains RAM storage data and software applications for the MP and the SP. The SP uses a part of the MP memory with the memory management unit of the SP.
NT6X47AC	10F	*Master processor memory card* The MPM card contains RAM storage data and software applications for the MP and the SP. The SP accesses a part of the MP memory with the memory management unit of the SP.
NT6X69AB	18F	*Messaging card* The messaging card provides interface for the parallel speech bus and extracts control messages from the control module (CM) on channel zero.

NT6X02EA (continued)

NT6X02EA parts (Sheet 5 of 6)

PEC	Slot	Description
NT6X69AC	18F	*Messaging card* The messaging card provides interface for the parallel speech bus and extracts control messages from the CM on channel zero.
NT6X69MA	18F	*Messaging card* The messaging card provides interface for the parallel speech bus and extracts control messages received on channel zero from the CM.
NT6X78AA	16F	*Custom local area signaling service modem resource card* The CLASS modem resource (CMR) card provides different residential (RES) enhanced features. The SMU shelf can use this card in slot 16 of the SMS shelf. Use the CMR card if the calling number delivery (CND) feature requires the CMR card.
NT6X78AB	16F	*Custom local area signaling service modem resource card* The CMR card provides different RES enhanced features. The SMU shelf can use this card in slot 16 of the SMU shelf. Use the CMR card if the CND feature is provisioned.
NT6X80BA	19F	*Pad/ring* The pad/ring card uses PCM to generate ringing frequency instructions. The TS card switches the frequencies to the DS-1 channels. The DS-1 channels are associated with the subscriber loops that must be rung.

NT6X02EA (continued)

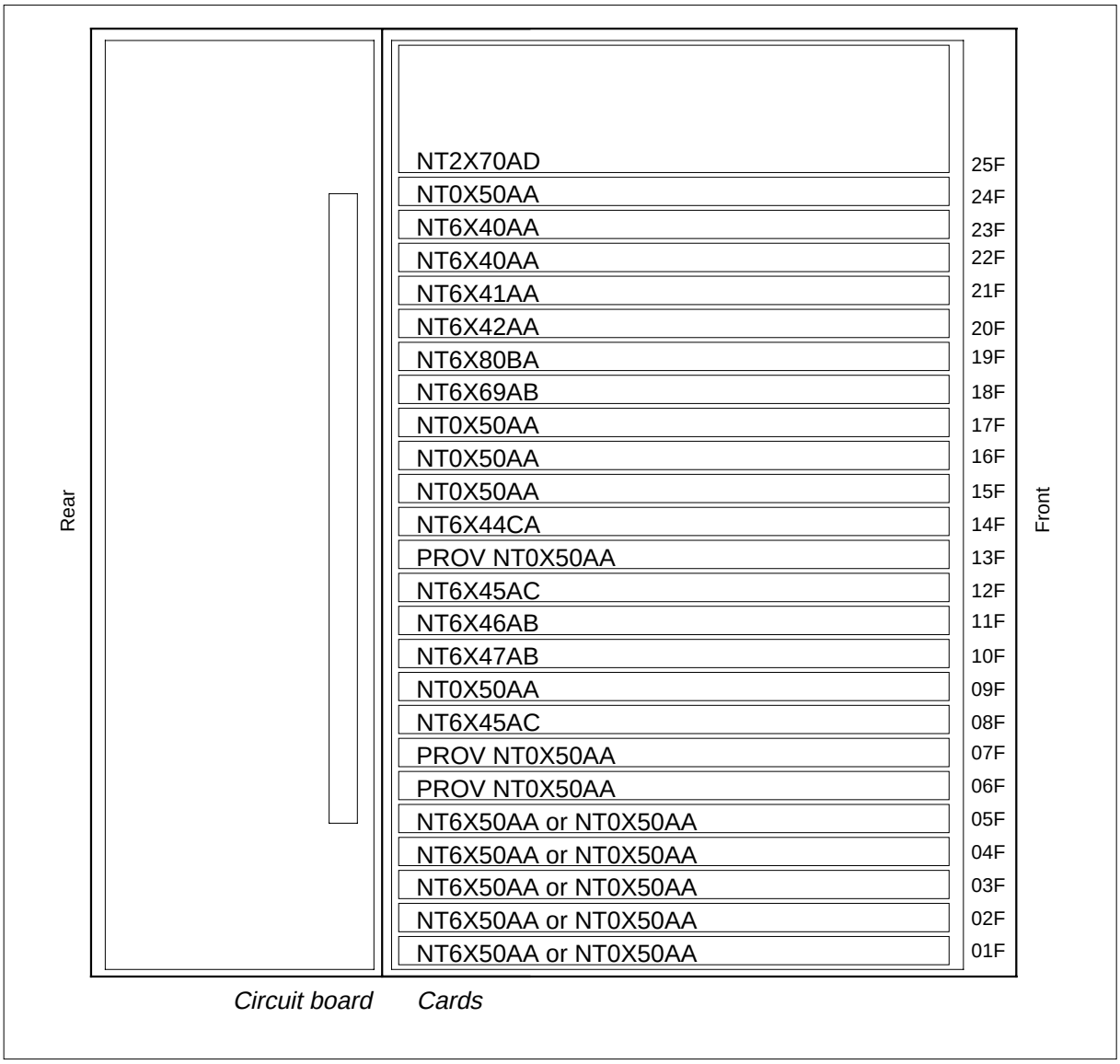
NT6X02EA parts (Sheet 6 of 6)

PEC	Slot	Description
NT6X81AA	13F	*A/B interface card* The A/B interface card inserts and extracts A-bits and B-bits from the PCM stream. The system uses these signaling bits for each channel are for ringing, hook status detection, and ANI and coin functions.
NT6X85AB	1F-5F	*DS-1 Interface card* The DS-1 interface card contains two DS-1 ports. Use one to ten cards available for each SMR module. Each port provides a two-way voice, data and signaling interface. The DS-1 interface card provides the following: • loop-around paths for each DS-1 port to allow isolation of faults • transmission of local alarms and the detection of remote alarms • detection of error conditions like loss of synchronization, bipolar error, and slip

The design of the NT6X02EA appears in the following figure.

NT6X02EA (end)

NT6X02EA parts



NT6X02EB

Description

The subscriber carrier module urban (SMU) shelf provides a digital interface to urban remote control terminals in a digital loop carrier system. The digital loop system is the subscriber loop concentrator (SLC). Business and residential application can use the SMU shelf.

When integrated in the DMS-100 switch, the DMS-1 urban remote terminal becomes the remote carrier urban (RCU) module. The DMS-100 switch offers this integrated configuration that provides subscribers with full digital resources. The SMU shelf does not require a separate control terminal (CT) card for each subscriber line. The SMU shelf reduces main distribution frame (MDF) wiring and activity. The SMU shelf saves office space. The CT serves one remote terminal (RT). The SMU shelf can serve multiple RCU modules.

The SMU shelf contains two units. One unit is active and provides the processing and control functions. The other unit is in standby mode and can take over call processing if a fault occurs in the active unit. The SMU replaces two of the three line cards and one multiplexer to reduce the cost of the subscriber carrier.

Each RCS includes a maximum of eight digroups. The digroups provide DS-1 links to the SMS. Each digroup contains 24 pulse code modulation (PCM) channels assembled by time-division multiplex (TDM). Eight equipped digroups contain 192 available channels (eight digroups × 24 PCM channels). Each of the two SMS message processors in the RCS uses a separate channel. A maximum of 190 channels are available for traffic.

The shelf provides an interface for RCUs only. The SMU shelf does not provide an interface to any other remote system. A standard DMS-100 single bay frame houses the SMU shelf pair. This bay is the subscriber module equipment (SME) frame (NT6X01AA). The bay contains two pairs of shelves, and each pair is a module. The two lower shelves are module 0 and the two upper shelves are module 1. Each module is NT6X02EB. Each node has DS-1 link assigned to the node the link serves. The node is a line appearance on a digital trunk (LDT) node.

The SMU shelf uses DS-1 interface cards or filler faceplates for slots 1 through 5. The shelf can use filler faceplates in slots 6, 7, and 13. Slots 8 and 12 can contain an XPM processor card or a master processor card. In slot 9, the SMU shelf uses a master processor memory card or a filler faceplate. Slot 16 contains a filler faceplate or a CLASS modem resource (CMR) card.

The SMU modules can also provide an interface to the enhanced network (ENET) by use of copper or fiber speech links. Both configurations can use the

NT6X69AC card. When the SMU uses the optical fiber speech links to connect to the ENET, the following three components are necessary for connection:

- the XPM DS-512 link control (NT6X40CA)
- the XPM DS-512 link card (NT6X40DA)
- the FXPM bracket assembly kit (NT6X02BU)

Parts

The SMU shelf contains the following parts:

- NT0X50AA–Filler faceplate
- NT2X70AD–Power converter
- NT2X70AE–Power converter
- NT3X90AC–Device controller cooling inverter unit
- NT6X40AA–DS30 network interface (NI) card
- NT6X40AC–DS30 NI card
- NT6X41AA–Speech bus formatter
- NT6X42AA–Channel supervision message (CSM) interface card
- NT6X44CA–Time switch (TS)
- NT6X45AF–Master processor (MP) card
- NT6X45BA–MP card
- NT6X46BA–Signaling processor memory (SPM) card
- NT6X47AB–Master processor memory (MPM) card
- NT6X69AB–Messaging card
- NT6X78AA–Custom local area signaling service modem resource card
- NT6X80BA–Pad/ring
- NT6X85AB–DS-1 interface card

NT6X02EB (continued)

Design

The design of the NT6X02EB appears in the following table.

NT6X02EB parts (Sheet 1 of 5)

PEC	Slot	Description
NT0X50AA	1F-7F, 9F, 13F 15F-17F, 23F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the shelves. Each shelf contains a maximum of five spare card slots. Slots 15, 16, and 17 have access to the signaling processor (SP) address bus and the parallel speech bus. Slots 13 and 19 do not have access.
NT2X70AD	25F	*Power converter* The power converter converts the -48V dc to the lower voltage that the circuit cards in the shelf need. Each power converter supplies +5V and 12V to the cards on the shelf. The power converters supply power to the DS-1 cards to prevent loss of unduplicated cards during a power failure.
NT2X70AE	25F	*Power converter* The power converter converts the -48V dc to the lower voltage that the circuit cards in the shelf need. Each power converter supplies +5V and 12V to the cards on the shelf. The power converters supply power to the DS-1 cards to prevent loss of unduplicated cards during a power failure.
NT3X90AC		*–DC fan cooling unit* The cooling inverter provides forced air cooling.
NT6X40AA	22F, 23F	*DS30 NI card* The DS30 NI card is available in two versions. The versions are the NT6X40AA (eight ports) and the NT6X40AC (16 ports). The card provides a central-side (C-side) interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.

NT6X02EB (continued)

NT6X02EB parts (Sheet 2 of 5)

PEC	Slot	Description
NT6X40AC	22F	*DS30 NI card* The DS30 NI card is available in two versions. The versions are the NT6X40AA (eight ports) and the NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.
NT6X41AA	21F	*Speech bus formatter* The speech bus formatter card contains a clock section and a formatting section. The clock section generates the 10.24 MHz shelf clock. The formatting section provides parallel-to-serial conversion of the coded voice signals. The CSM interface card sends these coded voice signals to the C-side links. The card provides serial-to-parallel conversion of the coded voice signals. The formatting section provides network plane selection, parity error generation for test purposes, and T1 clock generation.
NT6X42AA	20F	*Channel supervision message* The CSM interface card performs several functions. The functions of the CSM interface card are as follows: • extracts the CSM bit from the C-side channels • assembles the CSM for each channel • inserts the CSM in the outgoing C-side bytes • performs parity checking on all incoming bytes • parity generation on all outgoing bytes

NT6X02EB (continued)

NT6X02EB parts (Sheet 3 of 5)

PEC	Slot	Description
NT6X44CA	14F	*Time switch* The time switch (TS) converts between a serial stream and a parallel stream. The DS30 interface card or DS-1 interface card sends or receives the serial stream. The internal speech bus uses the parallel stream. When the SP controls the TS, the TS associates the DS30 interface cards and DS-1 interface cards. The TS associated the cards with the time slots on the parallel speech bus. The TS transfers data between the associated channel and the time slot.
NT6X45AF	8F, 12F	*Master processor card* The MP card runs the programs that operate and maintain a peripheral module (PM). The MP card collects digits, assigns channels, and interprets messages for the central control complex and PM.
NT6X45BA	8F, 12F	*Master processor card* The MP card runs the programs that operate and maintain a peripheral module that collects digits, assigns channels, and interprets messages for the central control complex and PM.
NT6X46BA	11F	*Signaling processor memory card* The SPM card contains RAM storage data and software applications.
NT6X47AB	9F, 10F	*Master processor memory card* The MPM card contains RAM storage data and software applications for the MP and the SP. The SP uses a memory management unit to gain access to a part of the MP memory.
NT6X69AB	18F	*Messaging card* The messaging card provides interface for the parallel speech bus and extracts control messages from the control module (CM) on channel zero.

NT6X02EB (continued)

NT6X02EB parts (Sheet 4 of 5)

PEC	Slot	Description
NT6X78AA	16F	*Custom local area signaling service modem resource card* The CMR card provides different residential (RES) enhanced features and the SMU shelf can use this card in slot 16. Use the CMR card if the calling number delivery (CND) feature is provisioned.
NT6X78AB	16F	*Custom local area signaling service modem resource card* The CMR card provides different RES enhanced features and the SMU shelf can use this card in slot 16. Use the CMR card if the CND feature is provisioned.
NT6X80BA	19F	*Pad/ring* Use the PCM. The pad/ring card generates ringing frequency instructions. The time switch card switches frequencies to the DS-1 channels associated with the subscriber loops that must be rung.

NT6X02EB (continued)

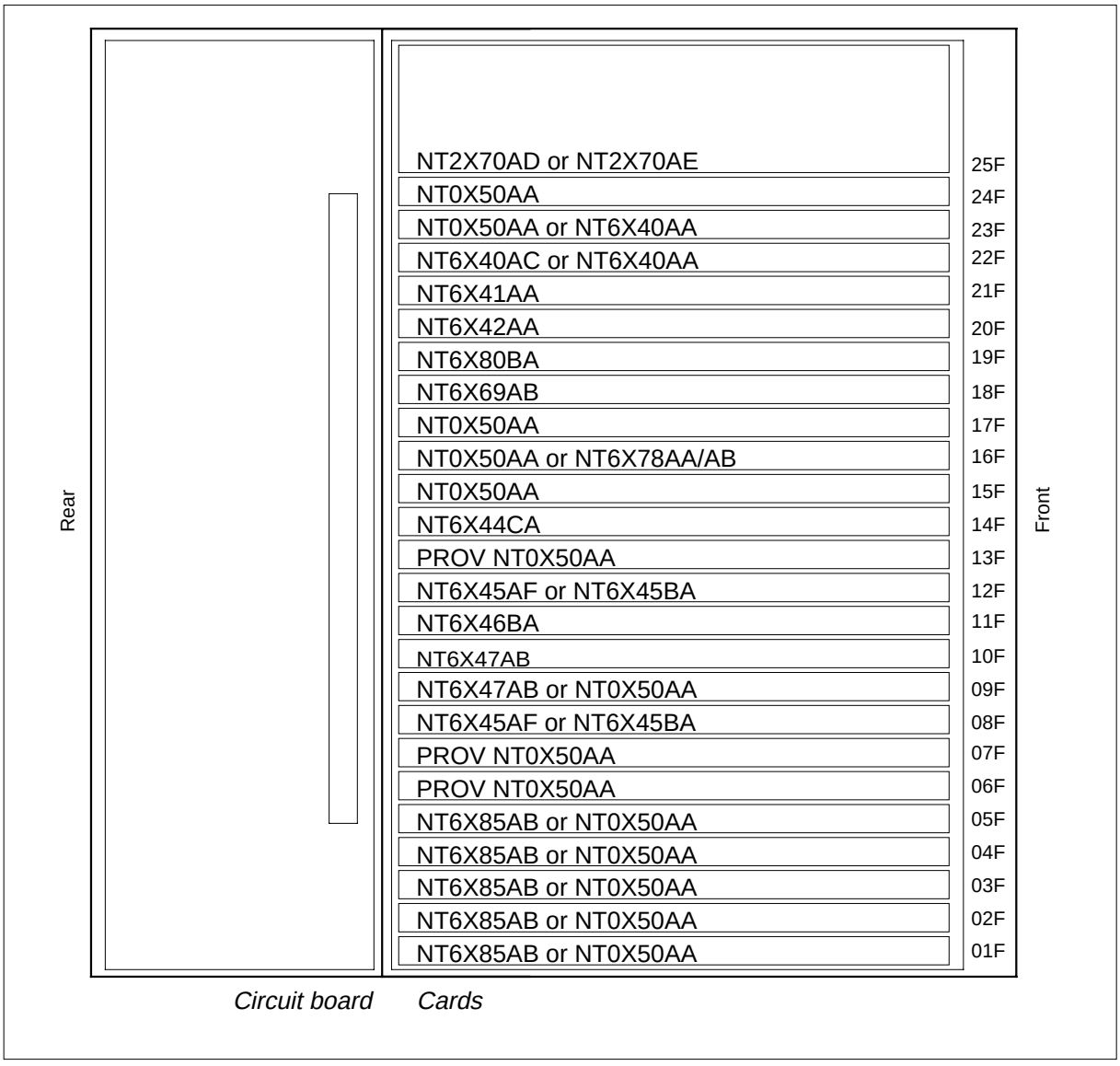
NT6X02EB parts (Sheet 5 of 5)

PEC	Slot	Description
NT6X81AA	13F	*A/B interface card* The A/B interface card inserts and extracts A bits and B bits from the PCM stream. These signaling bits for each channel are for ringing, hook status detection, and ANI and coin functions.
NT6X85AB	1F-5F	*DS-1 Interface card* The DS-1 interface card contains two DS-1 ports. Each SMR module can supply one to ten cards. Each port provides a two-way voice, data and signaling interface. The card provides the following functions: • looparound paths for each DS-1 port to allow isolation of faults • transmission of local alarms • detection of remote alarms • detection of error conditions like loss of synchronization, bipolar error and slip

The design of the NT6X02EB appears in the following figure.

NT6X02EB (end)

NT6X02EB parts



NT6X02EF

Product description

The subscriber carrier module urban (SMU) shelf provides a digital interface to urban remote control terminals in a digital loop carrier system. This system is the subscriber loop concentrator (SLC). Use the SMU shelf in business and/or residential applications.

The DMS-1 urban remote terminal becomes the remote carrier urban (RCU) module when integrated in the DMS-100 switch. This integrated configuration provides subscribers with the full digital resources that the DMS-100 switch offers. The SMU shelf reduces main distribution frame (MDF) wiring and activity, and saves office space. The SMU shelf eliminates the separate control terminal (CT) cards for each subscriber line. The CT serves one remote terminal (RT). The SMU shelf serves several RCU modules.

Divide the SMU shelf in two units. One unit is active and provides the necessary processing and control functions. One unit is in a standby mode. This unit can take over call processing if a fault occurs in the active unit. To reduce the cost of the standard subscriber carrier, the SMU replaces two of the three line cards and one multiplexer.

Each RCU has a maximum of eight digroups that provide DS-1 links to the SMU. Each digroup consists of 24 pulse-code-modulation (PCM) channels. The time-division multiplex (TDM) assembles these PCM channels. When the digroups are equipped, 192 channels are available. These channels consist of eight digroups. Each digroup has 24 PCM channels. The two SMU message processors in the RCU use a separate channel. This process leaves a maximum of 190 channels available for traffic.

The shelf provides an interface for RCUs. The shelf does not provide an interface to other remote systems. A standard DMS-100 single bay frame houses the SMU shelf pairs. This bay is the subscriber module equipment (SME) frame (NT6X01AA). This bay contains two pairs of shelves. Each pair of shelves is a module. Module 0 comprises the lower two shelves. Module 1 comprises the upper two shelves. The system designates each module NT6X02EA. The system assigns a DS-1 link to the node the module serves. This node is a line appearance on a digital trunk (LDT) node.

The SMU shelf uses DS-1 interface cards or filler faceplates for slots 1 through 5. Provision filler faceplates in slots 6, 7, and 13. Slot 8 uses an XMS-based peripheral module (XPM) processor card or a master processor card. Slot 9 uses a master processor memory card or filler faceplate. Slot 16 uses a filler faceplate or CLASS modem resource (CMR) card.

The SMU modules can use copper or fiber speech links to provide an interface to the enhanced network (ENET). The NT6X69AC card is necessary for these configurations. Two components are required when the SMU uses fiber speech links to connect to the ENET. The first required component is the XPM DS-512 link control (NT6X40CA). The second required component is the XPM DS-512 link card (NT6X40DA).

Use current shroud mounting hardware to mount the backpanel terminator (NT6X1205) in position . Use the FXPM bracket assembly kit (NT6X02BU) when you mount the XPM DS-512 link card to the backpanel terminator.

Parts

The SMU shelf contains the following parts:

- NT0X50AA–Filler faceplate
- NT2X70AD–Power converter
- NT2X70AE–Power converter
- NT3X90AC–Device controller cooling inverter unit
- NT6X40AA–DS30 network interface (NI) card
- NT6X40AC–DS30 NI card
- NT6X41AA–Speech bus formatter
- NT6X42AA–Channel supervision message (CSM) interface card
- NT6X44CA–Time switch (TS)
- NT6X45AC–Master processor (MP) card
- NT6X45BA–MP card
- NT6X45CA–MP card
- NT6X46BA–Signaling processor memory (SPM) card
- NT6X47AB–Master processor memory (MPM) card
- NT6X69AB–Messaging card
- NT6X78AA–Custom local area signaling service modem resource card
- NT6X78AB–Custom local area signaling service modem resource card
- NT6X80BA–Pad/ring
- NT6X85AB–DS-1 interface card

NT6X02EF (continued)

Design

The design of the NT6X02EF. appears in the following table.

NT6X02EF parts (Sheet 1 of 6)

PEC	Slot	Description
NT0X50AA	1F-7F, 9F, 13F 15F-17F, 23F, 24F	*Filler faceplate* Use the filler faceplate to fill empty card slots in the shelves. A maximum of five spare card slots are present in each shelf. Slots 15, 16, and 17 have access to the signaling processor (SP) address bus and the parallel speech bus. Slots 13 and 19 do not have access.
NT2X70AD	25F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards require in the shelf. The power converters supply +5 V and 12 V for the cards on the shelf. The system provides power to the DS-1 cards to prevent a loss of unduplicated cards during a power failure.
NT2X70AE	25F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards require in the shelf. The power converter supplies +5 V and 12 V for the cards on the shelf. The system provides power to the DS-1 cards to prevent a loss of unduplicated cards during a power failure.
NT3X90AC		*–DC fan cooling unit* The cooling inverter provides forced air cooling.

NT6X02EF (continued)

NT6X02EF parts (Sheet 2 of 6)

PEC	Slot	Description
NT6X40AA	22F, 23F	*DS30 NI card* The DS30 NI card is available in two version. The first version is an eight port NT6X40AA version. The second version is a 16 ports NT6X40AC version. The card provides a central-side (C-side) interface for DS30 links to the network. Each port of a DS30 NI card provide two-way voice and data interface. The ports of a DS30 NI card contain a looparound circuit for fault isolation.
NT6X40AC	22F	*DS30 NI card* The DS30 NI card is available in two versions. The first version is an eight port NT6X40AA version. The second version is an NT6X40AC version. The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides two-way voice and data interface. Each port of a DS30 NI card contains a looparound circuit for fault isolation.
NT6X41AA	21F	*Speech bus formatter* The speech bus formatter card consists of two sections. The first section is the clock section. The second section is the formatting section. The clock section generates the 10.24-MHz shelf clock. The formatting section of the card provides parallel-to-serial conversion of encoded voice signals. The card receives these signals from the CSM interface card. These signals are part of the C-side links. The card provides serial-to-parallel conversion of the encoded voice signals. The card receives these signals from the C-side interface cards and network plane selection. The card receives signals from the parity error generation for test purposes and T1 clock generation.

NT6X02EF (continued)

NT6X02EF parts (Sheet 3 of 6)

PEC	Slot	Description
NT6X42AA	20F	*Channel supervision message* The CSM interface card performs several functions. The card extracts the CSM bit from the C-side channels. The card assembles the CSM for each channel. The card inserts the CSM in the outgoing C-side bytes. The CSM interface card performs parity checking on every incoming byte. The CSM interface card performs parity generation on every outgoing byte.
NT6X44CA	14F	*Time switch* The TS converts between the serial stream and the parallel stream. The DS30, DS-1 interface card, or parallel stream receives or transmits the serial stream. The system uses parallel stream on the internal speech bus. When the SP controls the TS, the TS associates the DS30 and DS-1 interface cards with the time slots on the parallel speech bus. The TS transfers data between the associated channel and the time slot.
NT6X45AF	8F, 12F	*Master processor card* The master processor (MP) card runs the programs that control the operation and maintenance of a peripheral module (PM). The MP performs functions like digit collection and channel assignment. The MP allows for the description of messages for the central control complex and PM.
NT6X45AC	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a PM. The MP card performs functions like digit collection and channel assignment. The MP card allows for the description of messages for the central control complex and PM.

NT6X02EF (continued)

NT6X02EF parts (Sheet 4 of 6)

PEC	Slot	Description
NT6X45BA	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a PM. The MP card performs functions like digit collection and channel assignment. The MP card allows for the description of messages for the central control complex and PM.
NT6X45CA	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a PM. The MP card performs functions like digit collection and channel assignment. The MP card allows for the description of messages for the central control complex and PM.
NT6X46AC	11F	*Signaling processor memory card* The SPM card consists of RAM that the system uses to store data and software applications.
NT6X46BA	11F	*SPM card* The SPM card consists of RAM that the system uses to store data and software applications.
NT6X47AB	9F, 10F	*Master processor memory card* The MPM card consists of RAM that the system uses to store data and software applications for the MP and the SP. The SP has access to part of the MPM. The SP uses the memory management unit to gain access to the MPM.
NT6X47AC	10F	*Master processor memory card* The MPM card consists of RAM the system uses to store data and software applications for the MP and the SP. The SP has access to a part of the MPM. The SP uses the memory management unit to gain access to the MPM.

NT6X02EF (continued)

NT6X02EF parts (Sheet 5 of 6)

PEC	Slot	Description
NT6X69AB	18F	*Messaging card* The messaging card provides interface for the parallel speech bus. The messaging card extracts control messages received on channel zero from the control module (CM).
NT6X69AC	18F	*Messaging card* The messaging card provides an interface for the parallel speech bus. The messaging card extracts control messages received on channel zero from the CM.
NT6X69MA	18F	*Messaging card* The messaging card provides an interface for the parallel speech bus. The messaging card extracts control messages received on channel zero from the CM.
NT6X78AA	16F	*Custom local area signaling service modem resource card* The CMR card provides different residential enhanced (RES) features. Provision the CMR card in slot 16 of the SMU shelf. If you provision the calling number delivery (CND) feature, you require the CMR card.
NT6X78AB	16F	*Custom local area signaling service modem resource card* The CMR card provides different RES enhanced features. Provision the CMR card in slot 16 of the SMU shelf. If you provision the CND feature, you require the CMR card.
NT6X80BA	19F	*Pad/ring* The pad/ring card uses the PCM to generate ringing frequency instructions. The TS card switches the frequencies to the DS-1 channels. The DS-1 channels associate with the subscriber loops that must ring.

NT6X02EF (continued)

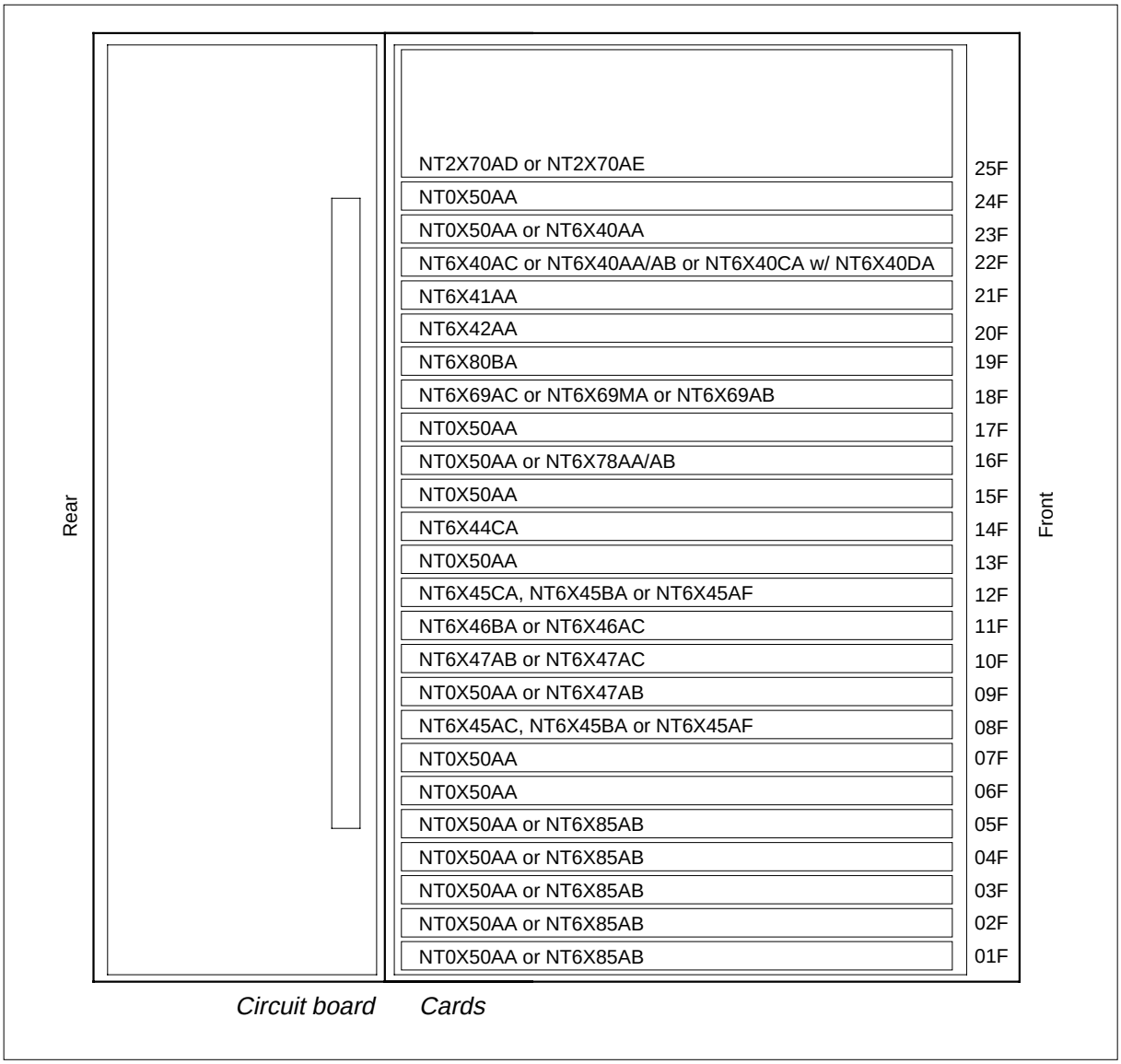
NT6X02EF parts (Sheet 6 of 6)

PEC	Slot	Description
NT6X81AA	13F	*A/B interface card* The A/B interface card inserts and extracts A and B bits from the PCM stream. Use the signaling bits for each channel to detect ringing and hook status. In some instances, the system uses these signaling bits for ANI and coin functions.
NT6X85AB	1F-5F	*DS-1 Interface card* The DS-1 interface card contains two DS-1 ports. You can provision 1 to 10 cards for each SMR module. Each port provides a two-way voice, data, and signaling interface. The card provides loop-around paths for each DS-1 port. This path allows for the isolation of faults. This path provides transmission of local alarms and the detection of remote alarms. This looparound path detects error conditions like loss of synchronization, bipolar error, and slip.

The design of the NT6X02EF. appears in the following table.

NT6X02EF (end)

NT6X02EF parts



NT6X02EG

Product description

The subscriber carrier module urban (SMU) shelf provides a digital interface to urban remote control terminals in a digital loop carrier system. This digital loop carrier system is the subscriber loop concentrator (SLC). Use the SMU shelf in business and/or residential applications.

The DMS-1 urban remote terminal becomes the remote carrier urban (RCU) module when integrated in the DMS-100 switch. This integrated configuration provides subscribers with the full digital resources that the DMS-100 switch offers. The SMU eliminates the need for separate control terminal (CT) cards for each subscriber line. This action reduces main distribution frame (MDF) wiring and activity and saves office space. The CT serves one remote terminal (RT). The SMU shelf serves several RCU modules.

The SMU shelf consists of two units. One unit is active and provides the necessary processing and control functions. The other unit is in a standby mode. This unit can take over call processing if a fault occurs in the active unit. To reduce the cost of the standard subscriber carrier, the SMU replaces two of the three line cards and one multiplexer.

Each RCU has a maximum of eight digroups. These eight digroups provide DS-1 links to the SMU. Each digroup consists of 24 pulse-code-modulation (PCM) channels that the time-division multiplex (TDM) assembles. When the digroups are equipped, 192 channels are available. These channels consist of eight digroups, each with 24 PCM channels. The two SMU message processors in the RCU use a separate channel. This condition leaves a maximum of 190 channels available for traffic.

The shelf provides an interface for RCUs. The shelf does not provide an interface to other remote systems. A standard DMS-100 single bay frame contains the SMU shelf pairs. This bay is the subscriber module equipment (SME) frame (NT6X01AA). This bay contains two pairs of shelves. Each pair of shelves is a module. Module 0 comprises the lower two shelves. Module 1 comprises the upper two shelves. Designate each module NT6X02EA. Assign a DS-1 link to the node the link serves. This node is a line appearance on a digital trunk (LDT) node.

The SMU shelf uses DS-1 interface cards or filler faceplates for slots 1 through 5. Provision filler faceplates in slots 6, 7, and 13. Slot 8 uses an XPM card or a master processor card. Slot 16 uses a filler faceplate or CLASS modem resource (CMR) card.

The SMU modules can provide an interface to the enhanced network (ENET) through the use of copper or fiber speech links. The NT6X69AC messaging

NT6X02EG (continued)

card is required with each configuration. The SMU connects to the ENET through the use of fiber speech links. This connection requires two components. The first component is the XPM DS-512 link control NT6X40CA. The second component is the XPM DS-512 link card NT6X40DA. Use the FXPM bracket assembly kit (NT6X02BU) to mount NT6X40DA to the backpanel terminator (NT6X1205).

Parts

The SMU shelf contains the following parts:

- NT0X50AA–Filler faceplate
- NT2X70AE–Power converter
- NT3X90AC–Device controller cooling inverter unit
- NT6X40AA–DS30 network interface (NI) card
- NT6X40AC–DS30 NI card
- NT6X41AA–Speech bus formatter
- NT6X42AA–Channel supervision message (CSM) interface card
- NT6X44CA–Time switch (TS)
- NT6X45BA–Master processor (MP) card
- NT6X46BB–Signaling processor memory (SPM) card
- NT6X47AC–Master processor memory (MPM) card
- NT6X69AB–Messaging card
- NT6X69AC–Messaging card
- NT6X69BA–Messaging card
- NT6X78AA–Custom local area signaling service modem resource card
- NT6X78AB–Custom local area signaling service modem resource card
- NT6X80BA–Pad/ring
- NT6X85AB–DS-1 interface card

Design

The design of the NT6X02EG appears in the following table.

NT6X02EG parts (Sheet 1 of 5)

PEC	Slot	Description
NT0X50AA	1F-7F, 9F, 13F 15F-17F, 23F, 24F	*Filler faceplate* Use the filler faceplate to fill empty card slots in the shelves. A maximum of five spare card slots are present in each shelf. Slots 15, 16, and 17 have access to the signaling processor (SP) address bus and the parallel speech bus. Slots 13 and 19 do not have access.
NT2X70AE	25F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards require in the shelf. Each power converter supplies +5 V and 12 V for the cards on the shelf. Provide power to the DS-1 cards to prevent loss of unduplicated cards during a power failure.
NT3X90AC	-	*DC fan cooling unit* The cooling inverter provides forced air cooling.
NT6X40AA	22F, 23F	*DS30 NI card* The DS30 NI card is available in two versions. The first version is the 8 port NT6X40AA. The second version is the 16 port NT6X40AC. The card provides a central-side (C-side) interface for DS30 links to the network. Every port of a DS30 NI card provides a two-way voice and data interface. Every port contains a looparound circuit for fault isolation.
NT6X40AC	22F	*DS30 NI card* The DS30 NI card is available in two versions. The first version is the 8 port NT6X40AA. The second version is the 16 port NT6X40AC. The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.

NT6X02EG (continued)

NT6X02EG parts (Sheet 2 of 5)

PEC	Slot	Description
NT6X41AA	21F	*Speech bus formatter* The speech bus formatter card consists of two sections. The first section is the clock section. The formatting section is the second section. The clock section generates the 10.24-MHz shelf clock. The formatting section of the card provides parallel-to-serial conversion of the encoded voice signals. The card receives these signals from the CSM interface card. The formatting section of the card sends these voice signals to the C-side links. The card provides serial-to-parallel conversion of the encoded voice signals from the C-side interface cards. The card provides conversion of the network plane selection, parity error generation for test purposes, and T1 clock generation.
NT6X42AA	20F	*Channel supervision message* The CSM interface card performs several functions. The card extracts the CSM bit from the C-side channels. The card assembles the CSM for each channel. The card inserts the CSM to the outgoing C-side bytes. The CSM interface card performs parity checking on each incoming byte. The CSM interface card performs parity generation on every outgoing byte.
NT6X44CA	14F	*Time switch* The TS converts between the serial stream. The TS receives or transmits this stream from the DS30 interface card or DS-1 interface card. The TS uses the parallel stream on the internal speech bus. The SP controls the TS. In this occurrence, the TS associates the DS30 interface cards and DS-1 interface cards. The TS associates these cards with the time slots on the parallel speech bus. The TS transfers data between the associated channel and the time slot.

NT6X02EG (continued)

NT6X02EG parts (Sheet 3 of 5)

PEC	Slot	Description
NT6X45AF	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a peripheral module (PM). The MP card performs functions like digit collection and channel assignment. The MP card describes messages for the central control complex and PM.
NT6X45AC	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a PM. The MP card performs functions like digit collection and channel assignment. The MP card describes messages for the central control complex and PM.
NT6X45BA	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a PM. The MP card performs functions like digit collection and channel assignment. The MP card describes messages for the central control complex and PM.
NT6X45CA	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a PM. The MP card performs functions like digit collection, channel assignment, and descriptionof messages for the central control complex and PM.
NT6X46AC	11F	*Signaling processor card* The SPM card contains RAM that stores data and software applications.
NT6X46BA	11F	*Signaling processor card* The SPM card consists of RAM that stores data and software applications.

NT6X02EG (continued)

NT6X02EG parts (Sheet 4 of 5)

PEC	Slot	Description
NT6X47AB	9F, 10F	*Master processor memory card* The MPM card contains RAM that stores data and software applications for the MP and the signaling processor. The SP has access to a part of the MP memory through the memory management unit.
NT6X47AC	10F	*Master processor memory card* The MPM card consists of RAM that stores data and software applications for the MP and the SP. The SP has access to a part of the MP memory through the memory management unit.
NT6X69AB	18F	*Messaging card* The messaging card provides interface for the parallel speech bus. The card also extracts control messages received on channel zero from the control module (CM).
NT6X69AC	18F	*Messaging card* The messaging card provides interface for the parallel speech bus. The card also extracts control messages received on channel zero from the CM.
NT6X69MA	18F	*Messaging card* The messaging card provides interface for the parallel speech bus. The card also extracts control messages received on channel zero from the CM.
NT6X78AA	16F	*Custom local area signaling service modem resource card* The CMR card provides various residential (RES) enhanced features and can be provisioned in slot 16 of the SMU shelf. The CMR card is required if the calling number delivery (CND) feature is provisioned.

NT6X02EG (continued)

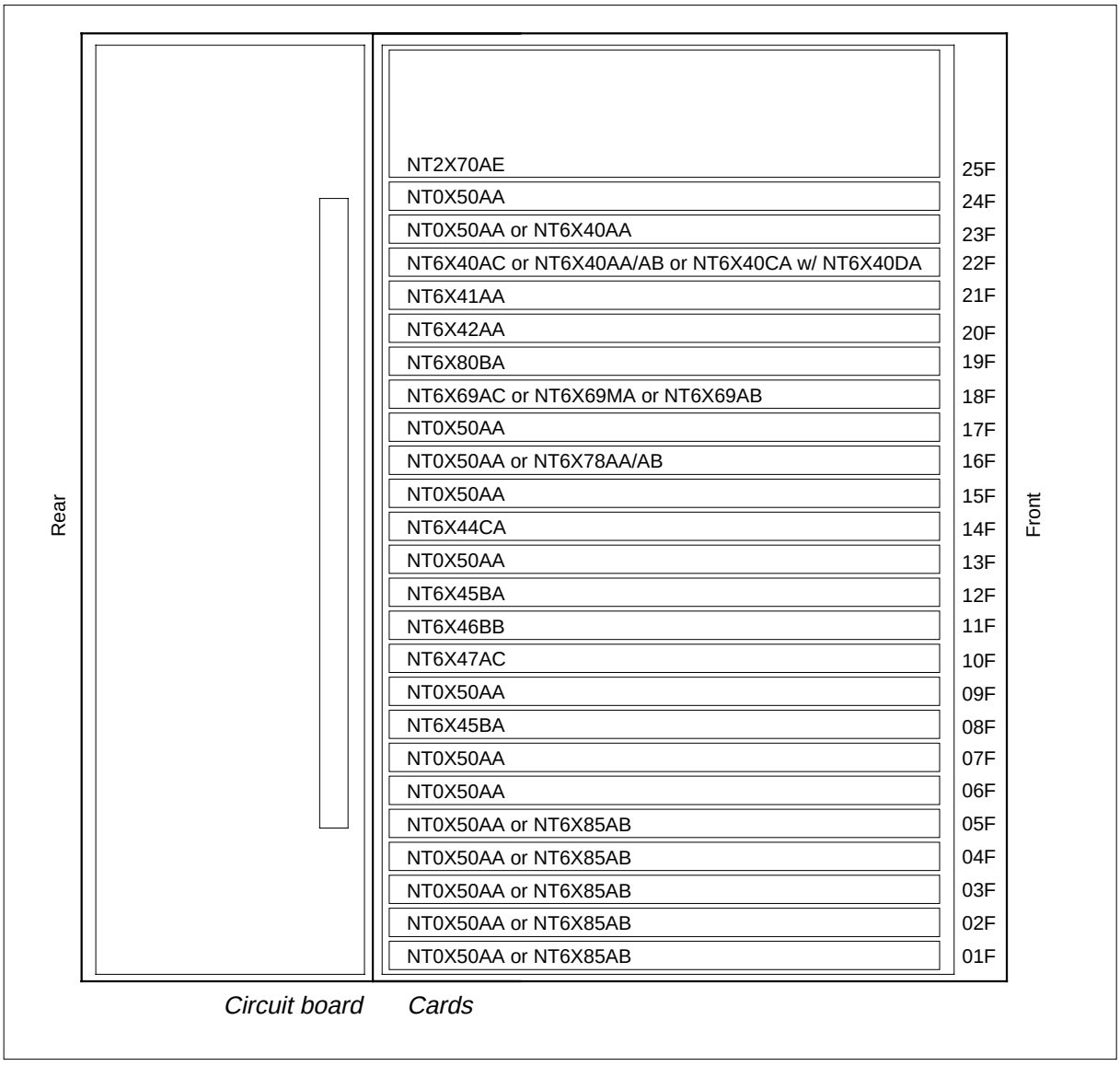
NT6X02EG parts (Sheet 5 of 5)

PEC	Slot	Description
NT6X78AB	16F	*Custom local area signaling service modem resource card* The CMR card provides various RES enhanced features and can be provisioned in slot 16 of the SMU shelf. The CMR card is required if the CND feature is provisioned.
NT6X80BA	19F	*Pad/ring* The pad/ring card generates ringing frequency instructions with the PCM. The TS switches the frequencies to the DS-1 channels. The DS-1 channels associate with the subscriber loops that must ring.
NT6X81AA	13F	*A/B interface card* The A/B interface card inserts and extracts A and B bits from the PCM stream. The signaling bits for each channel are used for ringing, and hook status detection. The signaling bits can also be used for ANI and coin functions.
NT6X85AB	1F-5F	*DS-1 Interface card* The DS-1 interface card contains two DS-1 ports. One to ten cards are provisionable for each SMR module. Each port provides a two-way voice, data, and signaling interface. The card provides loop-around paths for each DS-1 port to allow isolation of faults. The card also provides transmission of local alarms and the detection of remote alarms. The card also provides detection of error conditions like loss of synchronization, bipolar error, and slip.

The design of the NT6X02EG appears in the following table.

NT6X02EG (end)

NT6X02EG parts



NT6X02EK

Product description

The subscriber carrier module urban (SMU) shelf provides a digital interface to urban remote control terminals in a digital loop carrier system. This digital loop carrier system is the subscriber loop concentrator (SLC). Use the SMU shelf in business and/or residential applications.

When the DMS-1 urban remote terminal integrated in the DMS-100 switch, the terminal becomes the remote carrier urban (RCU) module. This integrated configuration provides subscribers with the full digital resources that the DMS-100 switch offers. The SMU shelf eliminates each control terminal (CT) cards for each subscriber line. This action reduces main distribution frame (MDF) wiring and activity and saves office space. While the CT serves one remote terminal, the SMU shelf serves several RCU modules.

The SMU shelf consists of two units. One unit is active and provides the necessary processing and control functions. The other unit is in a standby mode. This unit can take over call processing if a fault occurs in the active unit. The SMU replaces two of the three line cards and one multiplexer. This action reduces the cost of the traditional subscriber carrier.

Each RCU has a maximum of eight digroups which provide DS-1 links to the SMU. Each digroup consists of 24 pulse-code-modulation (PCM) channels that time-division multiplex (TDM) assembles. When the digroups are equipped, 192 channels are available (8 digroups, each with 24 PCM channels). Each of the two SMU message processors in the RCU uses a separate channel. This action leaves a maximum of 190 channels available for traffic.

The shelf provides an interface for RCUs. The shelf does not provide an interface to other remote systems. A standard DMS-100 single bay frame houses the SMU shelf pairs. This bay is the subscriber module equipment (SME) frame (NT6X01AA). This bay contains two pairs of shelves, and each pair is a module. Module 0 comprises the lower two shelves and module 1 comprises the upper two shelves. Each module is designated NT6X02EA. A DS-1 link is assigned to the node the link serves. The node is a line appearance on a digital trunk (LDT) node.

The SMU shelf uses DS-1 interface cards or filler faceplates for slots 1 through 5. Filler faceplates can also be provisioned in slots 6, 7, and 13. Slot 8 uses an XPM processor card or a master processor card. Slot 16 uses a filler faceplate or CLASS modem resource (CMR) card.

The SMU modules can use copper or fiber speech links to provide an interface to the enhanced network (ENET). With each configuration, the NT6X69AC

NT6X02EK (continued)

card is a requirement. When the SMU uses fiber links to connect to the ENET, three parts are required. These parts are (1) XPM DS-512 link control (NT6X40CA), (2) XPM DS-512 link card (NT6X40DA), and (3) FXPM bracket assembly kit (NT6X02BU).

Parts

The SMU shelf contains the following components:

- NT0X50AA–Filler faceplate
- NT2X70AE–Power converter
- NT3X90AC–DC fan cooling unit
- NT6X40AA–DS30 network interface (NI) card
- NT6X40AC–DS30 NI card
- NT6X41AA–Speech bus formatter
- NT6X42AA–Channel supervision message (CSM) interface card
- NT6X44CA–Time switch (TS)
- NT6X45AC–Master processor (MP) card
- NT6X45BA–MP card
- NT6X46BA–Signaling processor memory (SPM) card
- NT6X47AC–Master processor memory (MPM) card
- NT6X69AB–Messaging card
- NT6X78AA–Custom local area signaling service modem resource card
- NT6X78AB–Custom local area signaling service modem resource card
- NT6X80BA–Pad/ring
- NT6X85AB–DS-1 interface card

Design

The the design of the NT6X02EK appears in the following figure.

NT6X02EK parts (Sheet 1 of 5)

PEC	Slot	Description
NT0X50AA	1F-7F, 9F, 13F 15F-17F, 23F, 24F	*Filler faceplate* The filler faceplate is used to fill empty card slots in the shelves. A maximum of five spare card slots are available in each shelf. Three of the slots (15, 16, and 17) have access to the signaling processor (SP) address bus and the parallel speech bus. The spare slots (13 and 19) that remain do not have access.
NT2X70AE	25F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards require in the shelf. Each power converter supplies +5 V and 12 V for the cards on the shelf. Power to the DS-1 cards prevents loss of unduplicated cards when a power failure occurs.
NT3X90AC		*–DC fan cooling unit* The cooling inverter provides forced air cooling.
NT6X40AA	22F, 23F	*DS30 network interface card* The DS30 network interface card is available in two versions. These versions are NT6X40AA (eight ports) and NT6X40AC (16 ports). The card provides a central-side (C-side) interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.
NT6X40AB	22F, 23F	*DS30 network interface card* The DS30 NI card is available in two versions. These versions are NT6X40AA (eight ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.

NT6X02EK (continued)

NT6X02EK parts (Sheet 2 of 5)

PEC	Slot	Description
NT6X40AC	22F	*DS30 network interface card* The DS30 NI card is available in two versions. These versions are NT6X40AA (eight ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.
NT6X41AA	21F	*Speech bus formatter* The speech bus formatter card contains the clock section and the formatting section. The clock section generates the 10.24-MHz shelf clock. The formatting section of the card provides parallel-to-serial conversion of the encoded voice signals. These signals come from the CSM interface card and go to the C-side links. This card also provides serial-to-parallel conversion of the encoded voice signals from the C-side interface cards, and network plane selection. This card also provides parity error generation for test purposes, and T1 clock generation.
NT6X42AA	20F	*Channel supervision message* The CSM interface card performs several functions. The card extracts the CSM bit from the C-side channels, and assembles the CSM for each channel. The card inserts the CSM in the outgoing C-side bytes. The CSM interface card also performs parity checks on each incoming byte, and parity generation on each outgoing byte.

NT6X02EK (continued)

NT6X02EK parts (Sheet 3 of 5)

PEC	Slot	Description
NT6X44CA	14F	*Time switch* The TS converts between the serial stream and the parallel stream used on the internal speech bus. The DS30 interface card or DS-1 interface card sends or receives the serial stream. When the SP controls the time switch (TS), the TS also associates the DS30 interface cards and DS-1 interface cards with the time slots on the parallel speech bus. The TS transfers data between the associated channel and the time slot.
NT6X45AF	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a peripheral module (PM). The card performs functions like digit collection, channel assignment, and description of messages for the central control complex and PM.
NT6X45AC	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a PM. The card performs functions like digit collection, channel assignment, and description of messages for the central control complex and PM.
NT6X45BA	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a PM. The card functions like digit collection, channel assignment, and description of messages for the central control complex and PM.
NT6X45CA	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a PM. The card performs functions like digit collection, channel assignment, and description of messages for the central control complex and PM.

NT6X02EK (continued)

NT6X02EK parts (Sheet 4 of 5)

PEC	Slot	Description
NT6X46AC	11F	*Signaling processor memory card* The SPM card contains RAM that stores data and software applications.
NT6X46BA	11F	*Signaling processor memory card* The SPM card contains RAM that stores data and software applications.
NT6X47AB	9F, 10F	*Master processor memory card* The MPM card consists of RAM that stores data and software applications for the MP and the SP. The SP has access to a part of the MP memory through the memory management unit.
NT6X47AC	10F	*Master processor memory card* The MPM card consists of RAM that stores data and software applications for the MP and the SP. The SP has access to a part of the MP memory through the memory management unit.
NT6X69AB	18F	*Messaging card* The messaging card provides interface for the parallel speech bus. The card extracts control messages received on channel zero from the control module (CM).
NT6X69AC	18F	*Messaging card* The messaging card provides interface for the parallel speech bus. The card extracts control messages received on channel zero from the CM.
NT6X69MA	18F	*Messaging card* The messaging card provides interface for the parallel speech bus. The card extracts control messages received on channel zero from the CM.

NT6X02EK (continued)

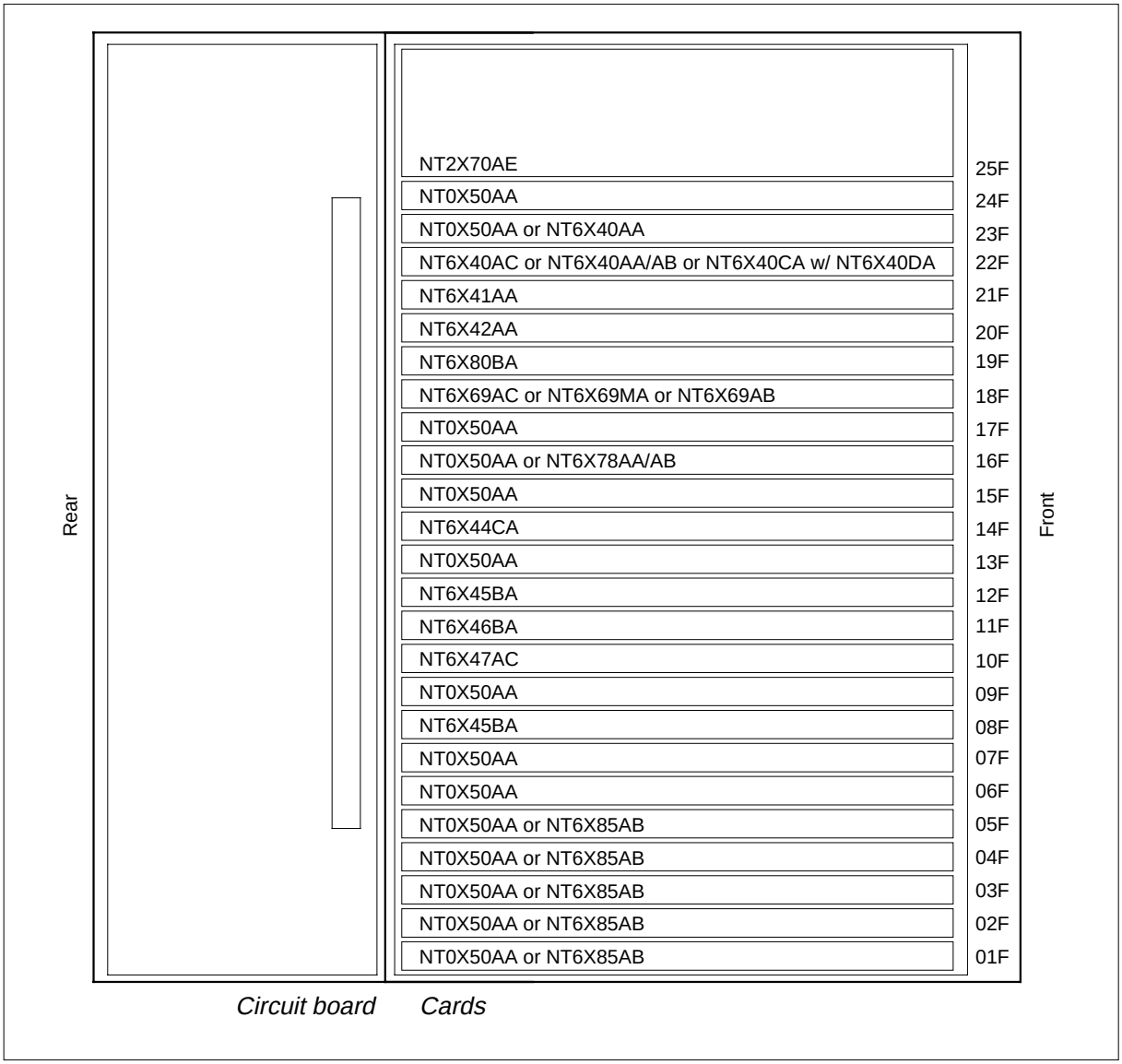
NT6X02EK parts (Sheet 5 of 5)

PEC	Slot	Description
NT6X78AA	16F	*Custom local area signaling service modem resource card* The CMR card provides several residential (RES) enhanced features. The card can be provisioned in slot 16 of the SMU shelf. The CMR card is required if the calling number delivery (CND) feature is provisioned.
NT6X78AB	16F	*Custom local area signaling service modem resource card* The CMR card provides several RES enhanced features. The card can be provisioned in slot 16 of the SMU shelf. The CMR card is required if the CND feature is provisioned.
NT6X80BA	19F	*Pad/ring* The pad/ring card generates ringing frequency instructions through the PCM. The TS switches the frequencies to the DS-1 channels that associate with the subscriber loops that must ring.
NT6X81AA	13F	*A/B interface card* The A/B interface card inserts and extracts A and B bits from the PCM stream. The signaling bits for each channel are used for ringing, and hook status detection. These signaling bits can also be used for ANI and coin functions.
NT6X85AB	1F-5F	*DS-1 Interface card* The DS-1 interface card contains two DS-1 ports. One to ten cards are provisionable for each SMR module. Each port provides a two-way voice, data, and signaling interface. The card provides looparound paths for each DS-1 port to allow isolation of faults. The card also provides transmission of local alarms and the detection of remote alarms. The card also provides detection of error conditions like loss of synchronization, bipolar error, and slip.

NT6X02EK (end)

The the design of the NT6X02EK appears in the following figure.

NT6X02EK parts



NT6X02HB

Product description

The NT6X02HB international line group controller (ILGC) shelf provides an interface. The interface is between central-side (C-side) DS30 links to the network and PCM30 links to subsidiary peripheral modules. The ILGC shelf is like the North American version of the line group controller (LGC). The ILGC uses the NT6X43BA international messaging card and firmware and supports DS30 diagnostics and not DS-1 diagnostics. The ILGC also uses the Turkish dialing plan digit analysis logic. The ILGC shelf consists of two units. One unit is active and provides the necessary processing and control functions. The other unit is in a standby mode. This unit can take over call processing if a fault occurs in the active unit. Each unit has a control complex (CC). One CC is active at a time and provides control for the two units. The NT6X01BA international common peripheral equipment (ICPCE) frame houses the ILGC shelves.

The ILGC shelf also has C-side interface. The C-side ports can support a maximum of 16 pairs of DS30 links to the network. Four DS30 interface cards support the C-side links. Each of these DS30 interface cards can handle a maximum of eight DS30 ports. The ILGC shelf distributes link assignments over the four DS30 cards so the even-numbered links connect to plane 0 of the network. The odd-numbered links must connect to plane 1. A minimum of three link pairs is required for proper interface with the network module (NM) and the CC.

Each DS30 card in the ILGC shelf powers 256 (8×32) channels for each plane to the formatter cards in units 0 and 1. Each formatter handles 512 channels (256 channels from each unit) for each plane. The two network planes combine in the formatter. The formatter selects one plane or the other for each channel. The formatter adds 512 speech channels to the 128 internal service channels. The formatter also converts the channels to a 640-channel bus to the control complex.

The ILGC shelf uses PCM30 interface cards or filler faceplates for slots 1 through 4. Filler faceplates are used in slots 5 and 6. The NT6X44AB time switch card is used in slot 7. Slots 8 and 9 use universal tone receiver (UTR) cards. The NT6X43BA messaging card is used in slot 10.

Parts

The ILGC shelf contains the following parts:

- NT0X50AA–Filler faceplate or panel
- NT2X70AE–Power converter
- NT3X90AC–Device controller cooling inverter unit

NT6X02HB (continued)

- NT6X27AA–PCM30 interface card
- NT6X27AB–PCM30 interface card
- NT6X28AA–Signaling card
- NT6X40AC–DS30 network interface (NI) card
- NT6X41AB–Speech bus formatter
- NT6X42AA–Channel supervision message (CSM) card
- NT6X43BA–Messaging card
- NT6X44AB–Time switch (TS)
- NT6X45BA–Master processor (MP) card
- NT6X45AD–Signaling processor (SP) card
- NT6X46BA–Signaling processor memory (SPM) card
- NT6X47AB–Master processor memory (MPM) card
- NT6X92CA–UTR

Design

The design of the NT6X02HB appears in the following table.

NT6X02HB parts (Sheet 1 of 5)

PEC	Slot	Description
NT0X50AA	1F-7F, 9F, 13F, 15F-17F, 19F, 23F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the CP fills. A maximum of five spare card slots is present in each fill. Three of the slots (15, 16, and 17) have access to the signaling processor (SP) address bus and the parallel speech bus. The spare slots (13 and 19) that remain do not have access.
NT2X70AE	25F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards require in the fill. Each power converter supplies + 5V and 12V for the cards in the fill. Power to the DS-1 circuit packs (CP) is provided to prevent loss of unduplicated cards during a power failure.

NT6X02HB (continued)

NT6X02HB parts (Sheet 2 of 5)

PEC	Slot	Description
NT3X90AC	-	*Device controller cooling inverter unit* The cooling inverter provides forced air cooling.
NT6X27AA	1F-to-4F	*PCM30 interface card* The pulse-code-modulation (PCM)30 interface card provides an interface. The interface is between an NT6X02 common peripheral controller (CPC) and European-standard PCM30 trunk transmission equipment. The PCM30 interface card translates PCM voice signals and signaling data between two 32-channel, 2.048-Mbps external PCM 30 trunk circuits and one 64-channel, 5.12 Mbps duplicate port in the CPC. The PCM30 interface card receives data streams from the four-wire PCM trunk transmission equipment. The PCM30 interface card converts the high-density bipolar 3 (HDB3) data to a DS30 format for transmission to the DS-60 TS card. The card receives PCM30 data from the TS card. The card converts the data to an HDB3 format for transmission to the trunk transmission equipment. A looparound function is available for testing purposes.

NT6X02HB (continued)

NT6X02HB parts (Sheet 3 of 5)

PEC	Slot	Description
NT6X27AB	4F	*PCM30 interface card* The PCM30 interface card provides an interface between an NT6X02 CPC and European-standard PCM30 trunk transmission equipment. The PCM30 interface card translates PCM voice signals and signaling data between two 32-channel, 2.048-Mbps external PCM 30 trunk circuits and one 64-channel, 5.12 Mbps duplicate port in the CPC. The PCM30 interface card receives data streams from the four-wire PCM trunk transmission equipment. The PCM30 card converts the high-density bipolar 3 (HDB3) data to a DS30 format for transmission to the DS-60 TS card. The card receives PCM30 data from the TS card. The card converts the data to an HDB3 format for transmission to the trunk transmission equipment. A looparound function is available for testing purposes.
NT6X28AA	19F	*Signaling card* The NT6X28AA signaling card is used to extract signaling information from and insert signaling information in the parallel speech buses of the IDTC. The card uses channel time slot (CTS) 16 to perform these functions. The CTS 0 is used to communicate control and status information between the processor and the PCM30 interface card.
NT6X40AC	23F	*DS30 network interface circuit pack* The DS30 NI card is available in two versions. These versions are NT6X40AA (eight ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.

NT6X02HB (continued)

NT6X02HB parts (Sheet 4 of 5)

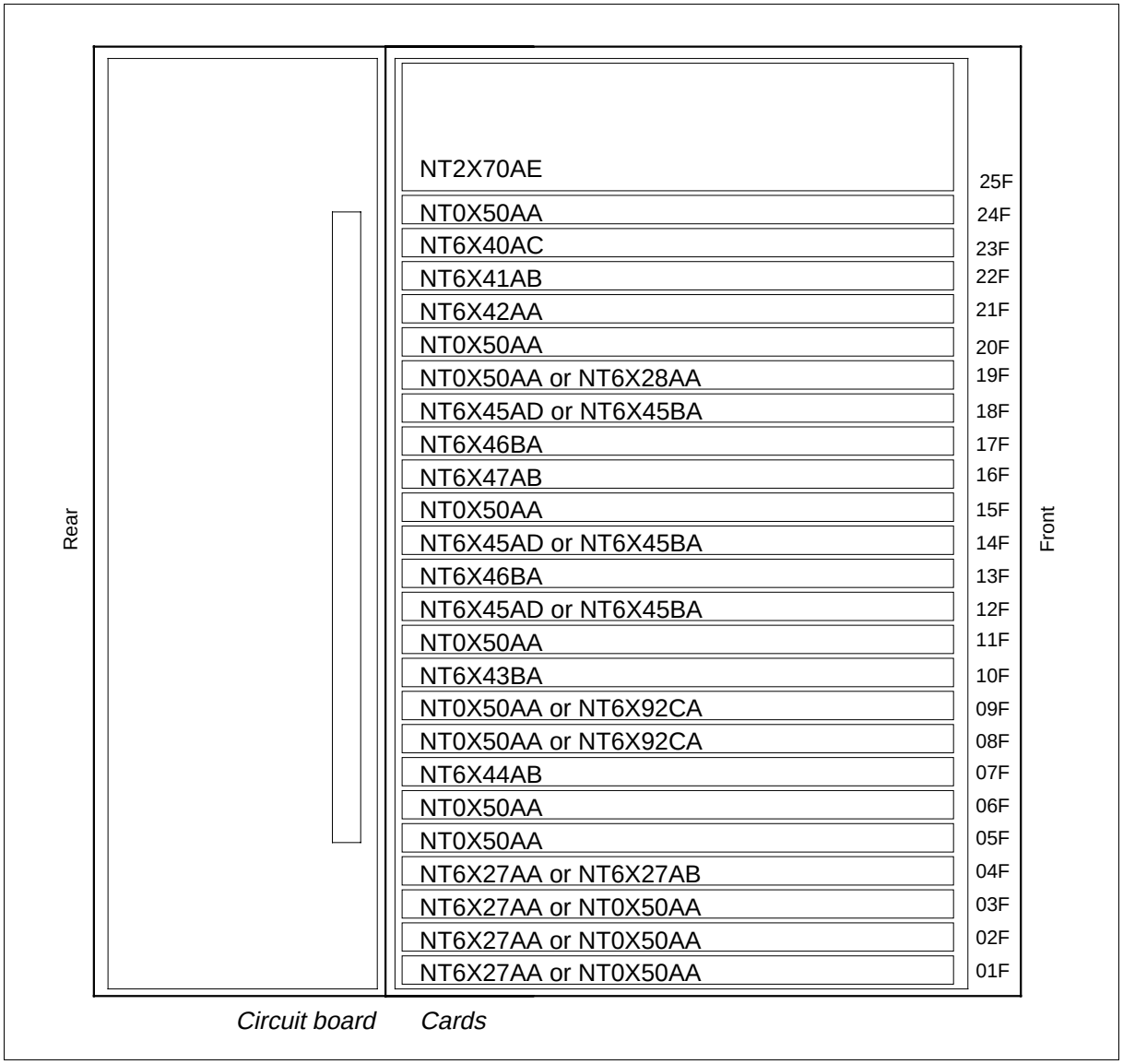
PEC	Slot	Description
NT6X41AB	22F	*Speech bus formatter* The speech bus formatter card contains two sections. These sections are the clock section and the formatting section. The clock section generates the 10.24-MHz shelf clock. The formatting section of the card provides parallel-to-serial conversion of the encoded voice signals. These signals come from the CSM interface card and must go to the C-side links. The card also provides serial-to-parallel conversion of the encoded voice signals from the C-side interface cards, and network plane selection. The card provides parity error generation for test purposes, and T1 clock generation.
NT6X42AA	21F	*Channel supervision message circuit pack* The CSM CP performs several functions. The CSM CP extracts the CSM bit from the C-side channels, and assembles the CSM for each channel. The CSM CP inserts the CSM in the outgoing C-side bytes. The CSM CP also performs parity checking on each incoming byte, and parity generation on each outgoing byte.
NT6X43BA	10F	*Messaging card* The messaging card provides interface for the parallel speech bus. The card extracts control messages from the control module (CM) that the card receives on channel zero.
NT6X44AB	7F	*Time switch* The TS converts between the serial stream that the DS30 interface card or DS-1 interface card receives or transmits, and the parallel stream used on the internal speech bus. When the SP controls the TS, the TS associates the DS30 interface cards and DS-1 interface cards with the time slots on the parallel speech bus. The DS30 interface card transfers data between the associated channel and the time slot.

NT6X02HB (end)

NT6X02HB parts (Sheet 5 of 5)

PEC	Slot	Description
NT6X45AD	12F, 14F, 18F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a peripheral module (PM). The card performs functions like digit collection, channel assignment, and description of messages for the central control complex and PM.
NT6X45BA	12F, 14F, 18F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a PM. The MP card performs functions like digit collection, channel assignment, and description of messages for the central control complex and PM.
NT6X46BA	13F, 17F	*Signaling processor memory card* The SPM card contains random access memory that stores data and software applications.
NT6X47AB	16F	*Master processor memory card* The MPM card contains RAM that stores data and software applications for the MP and the SP. The SP has access to a part of the MP memory through the memory management unit.
NT6X92CA	8F, 9F	*Universal tone receiver* The UTR is a 32-channel tone receiver that detects different tones, like dual-tone multi-frequency (DTMF) and multi-frequency (MF). The bus time switch switches tone samples to the parallel speech bus. The UTR collects tone samples at appropriate time slots. The UTR analyzes the samples and identifies the tones. The system sends the results to the SP.

NT6X02HB parts



NT6X02IA

Product description

The NT6X02IA digital trunk controller (DTC) common circuit pack (CP) fill provides an interface. This interface is between central-side (C-side) DS30 links to the network and peripheral-side (P-side) DS-1 digital trunks. The DTC common CP fill consists of two units. One unit is active and provides the necessary processing and control functions. The other unit is in standby mode. This unit can take over call processing if a fault occurs in the active unit. Each unit has a control complex (CC). One CC is active at a time and provides control for the two units.

The DTC common CP fill has C-side interface. The C-side ports can support a maximum of 16 pairs of DS30 links to the network. Four DS30 interface CPs support the C-side links. Each of these DS30 interface CPs can handle a maximum of eight DS30 ports. Link assignments are distributed over the four DS30 CPs. This distribution causes the even-numbered links to connect to plane 0 of the network, and the odd-numbered links to plane 1. A minimum of three link pairs must be present for correct interface with the network module (NM) and the CC.

Each DS30 CP in the DTC common CP fill powers 256 (8 [_Inline:Symbols:B {&0xb4;}] 32) channels for each plane to the formatter cards. These formatter cards are in units 0 and 1. Each formatter handles 512 channels (256 channels from each unit) for each plane. The two network planes combine in the formatter where selection of one of the planes occurs for each channel. The 512 speech channels are added to the 128 internal service channels. The 512 speech channels are converted to a 640-channel bus to the control complex.

The DTC common CP fill uses DS-1 interface CPs or filler faceplates for slots 1 through 5. Slot 13 uses a continuity tone detector or a filler faceplate. Slots 15 and 16 use a filler faceplate or a universal tone receiver (UTR). Slot 17 uses a specialized tone receiver (STR) or a filler faceplate. Slot 18 uses the NT6X69AB common peripheral processor (CPP) message protocol CP.

Parts

The DTC common CP fill contains the following parts:

- NT0X50AA–Filler faceplate
- NT2X70AD–Power converter
- NT2X70AE–Power converter
- NT3X90AC–Device controller cooling inverter unit
- NT6X40AA–DS30 network interface (NI)
- NT6X40AC–DS30 NI CP

- NT6X41AA–Speech bus formatter
- NT6X42AA–Channel supervision message (CSM) CP
- NT6X44AA–Time switch (TS)
- NT6X45AF–Line group controller (LGC)/DTC) processor
- NT6X45BA–XMS-based peripheral module (PM) processor
- NT6X46BA–Signaling processor memory (SPM) CP
- NT6X47AB–Master processor memory (MPM) CP
- NT6X50AA–DS-1 interface CP
- NT6X50AB–DS-1 interface CP
- NT6X55AB–DS0 interface CP
- NT6X62AA–STR
- NT6X69AB–CPP message protocol CP
- NT6X70AA–Continuity tone detector
- NT6X92BB–UTR

Design

The design of the NT6X02IA appears in the following table.

NT6X02IA parts (Sheet 1 of 6)

PEC	Slot	Description
NT0X50AA	1F-7F, 9F, 13F, 15F-17F, 19F, 23F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the CP fills. Each fill contains a maximum of five spare card slots in each fill. Three of the slots (15, 16, and 17) have access to the signaling processor (SP) address bus and the parallel speech bus. The spare slots that remain (13 and 19) do not have access.
NT2X70AD	25F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards need in the fill. Each power converter supplies +5 V and 12 V for the cards in the fill. Power to the DS-1 CPs prevents loss of cards that do not duplicate during a power failure.

NT6X02IA (continued)

NT6X02IA parts (Sheet 2 of 6)

PEC	Slot	Description
NT2X70AE	25F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards need in the fill. Each power converter supplies + 5 V and 12 V for the cards in the fill. Power to the DS-1 CPs prevents loss of cards that do not duplicate during a power failure.
NT3X90AC		*–Device controller cooling inverter unit* The cooling inverter provides forced air cooling.
NT6X40AA	22F, 23F	*DS30 network interface CP* The DS30 NI card is available in two versions. These versions are NT6X40AA (eight ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each of these ports contains a looparound circuit for fault isolation.
NT6X40AC	22F	*DS30 network interface CP* The DS30 NI card is available in two versions. These version are NT6X40AA (eight ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each of these ports contains a looparound circuit for fault isolation.

NT6X02IA (continued)

NT6X02IA parts (Sheet 3 of 6)

PEC	Slot	Description
NT6X41AA	21F	*Speech bus formatter* The speech bus formatter card contains two sections. These sections are the clock section and the formatting section. The clock section generates the 10.24-MHz shelf clock. The formatting section of the card provides parallel-to-serial conversion of the coded voice signals. These voice signals are the signals that come from the CSM interface card and that proceed to the C-side links. The formatting section of the card provides serial-to-parallel conversion of the coded voice signals. These signals come from the following processes. These processes consist of the C-side interface cards, network plane selection, T1 clock generation, and parity error generation. The parity error generation is for test purposes.
NT6X42AA	20F	*Channel supervision message CP* The CSM CP performs several functions. The CSM CP extracts the CSM bit from the C-side channels. The CSM CP assembles the CSM for each channel, and inserts the CSM in the outgoing C-side bytes. The CSM CP performs parity checking on each incoming byte, and parity generation on each outgoing byte.
NT6X44AA	14F	*Time switch* The TS converts between the serial stream, that the DS30 interface card or DS-1 interface card receives or transmits, and the parallel stream. This stream is used on the internal speech bus. When the SP controls the TS, the following two events occur. The TS associates the DS30 interface cards and DS-1 interface cards with the time slots on the parallel speech bus. The TS transfers data between the associated channel and the time slot.

NT6X02IA (continued)

NT6X02IA parts (Sheet 4 of 6)

PEC	Slot	Description
NT6X45AF	8F, 12F	*Line group controller/digital trunk controller processor* The LGC/DTC processor runs the programs that control the operation and maintenance of a PM. The LGC/DTC processor performs functions. These functions include digit collection, channel assignment, and message description for the central control complex and PM.
NT6X45BA	8F, 12F	*XMS-based peripheral module processor* The XMS-based PM (XPM) processor controls the formatter, the CSM CP, and the TS CP. The XPM processor collects the incoming control messages to the LGC/DTC processor for transmission. The LGC/DTC processor and the XPM processor use direct memory access (DMA) to communicate. The direct memory access allows the XPM processor to read and write to parts of the LGC/DTC processor memory. The LGC/DTC processor memory cannot access the XPM processor memory.
NT6X46BA	11F	*Signaling processor memory card* The SPM card contains RAM that stores data and software applications.
NT6X47AB	9F,10F	*Master processor memory card* The MPM card consists of RAM that stores data and software applications for the MP and the SP. The SP uses SP memory management unit to access a part of the MP memory.

NT6X02IA (continued)

NT6X02IA parts (Sheet 5 of 6)

PEC	Slot	Description
NT6X50AA	1F-5F	*DS-1 interface card* The DS-1 interface card contains two DS-1 ports. One to ten cards are provisionable for each LTC module. Each port provides a two-way voice, data, and signaling interface. The card provides looparound paths for each DS-1 port to allow isolation of faults. The card provides transmission of local alarms and the detection of remote alarms and error conditions. These error conditions include loss of synchronization, bipolar error, and slip.
NT6X50AB	1F-5F	*DS-1 interface card* The DS-1 interface card contains two DS-1 ports. One to ten cards are provisionable for each LTC module. Each port provides a two-way voice, data, and signaling interface. The card provides looparound paths for each DS-1 port to allow isolation of faults. The card provides transmission of local alarms and the detection of remote alarms and error conditions. These error conditions include loss of synchronization, bipolar error, and slip.
NT6X55AB	1F-5F	*DS0 interface CP* The DS0 interface CP provides physical level access for one 64-Kbps DS0 link in the DTC common CP fill. This interface CP can create CCS7 link access to a signal transfer point node for the DTC. The DS0 interface CP on a signal switching point can respond to loopback requests that the network initiates.

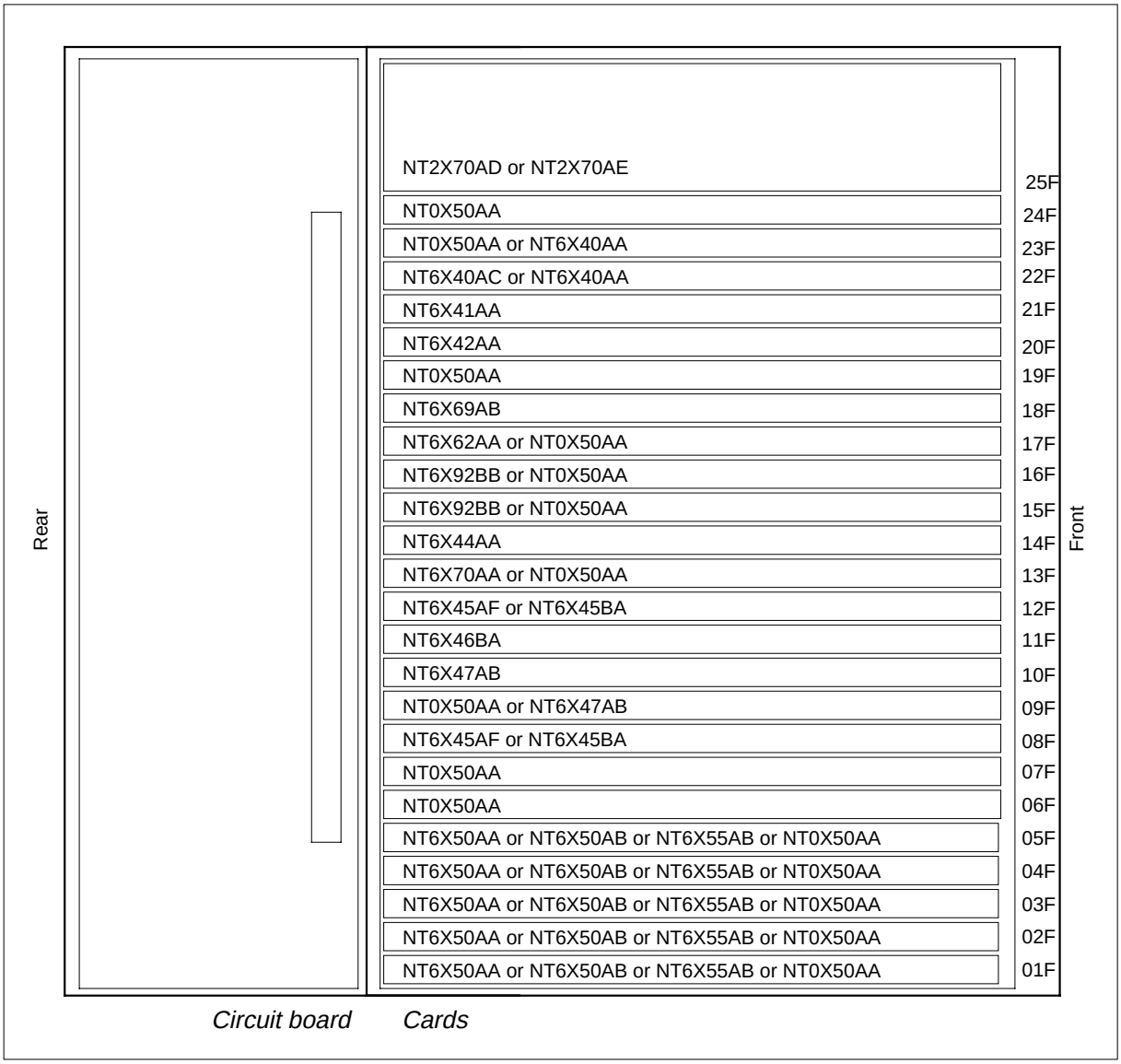
NT6X02IA (continued)

NT6X02IA parts (Sheet 6 of 6)

PEC	Slot	Description
NT6X62AA	17F	*Specialized tone receiver* The STR card allows the DTC common CP fill to detect and report specified tones on one channel or every channel. An STR can scan a maximum of 480 channels at one time. In the DMS-250, this receiver allows a subscriber in the talking state to perform the following actions. The subscriber can press # or * and dial out digits to make a new connection and not dial the carrier access and authorization codes again. The STR can be provisioned in a DTC with an extended XPM processor memory and a CPP message protocol CP.
NT6X69AB	18F	*Common peripheral processor message protocol CP* The messaging card provides interface for the parallel speech bus. The messaging card extracts control messages received on channel zero from the control module.
NT6X70AA	13F	*Continuity tone detector* The continuity tone detector detects tones used in call processing to verify the continuity of the voice/data path between DTCs. This detector monitors and records the frequency and level of the tones. The continuity tone detector retains this data for use by the XPM processor in the DTC.
NT6X92BB	15F, 16F	*Universal tone detector* The Universal tone detector (UTR) is a 32-channel tone receiver that detects different tones. These tones include dual-tone multi-frequency (DTMF) and multi-frequency (MF). The TS switches the tone samples to the parallel speech bus. The UTR collects tone samples at appropriate time slots. The UTR analyzes the samples and identifies the tones. The system sends the results to the XPM processor.

The design of the NT6X02IA appears in the following figure.

NT6S02IA parts



NT6X02LA

Product description

The NT6X02LA line group controller (LGC) common circuit pack (CP) fill provides an interface. This interface can be between central-side (C-side) DS30 links to the network and peripheral-side (P-side) DS30A links. This interface can be between C-side DS30 links to the network and DS-1 links to secondary peripheral modules (PM). The LGC common CP fill has two units. One unit is active and provides the necessary processing and control functions. The other unit is in standby mode and can take over call processing if a fault occurs in the active unit. Each unit has a control complex (CC). Only one CC is active at a time and provides control for the two units.

The LGC common CP fill has C-side interface. The C-side ports can support a maximum of 16 pairs of DS30 links to the network. Four DS30 interface CPs support the C-side links. Each of these DS30 interface CPs can handle a maximum of eight DS30 ports. Link assignments are distributed over the four DS30 CPs. This distribution causes the even-numbered links to connect to plane 0 of the network, and the odd-numbered links to plane 1. A minimum of three link pairs must be present for correct interface with the network module (NM) and the CC.

Each DS30 CP in the LGC common CP fill powers 256 x 32) channels for each plane to the formatter cards. These formatter cards are in units 0 and 1. Each formatter handles a total of 512 channels (256 channels from each unit) for each plane. The two network planes combine in the formatter. In the formatter, selection of one of the planes occurs for each channel. The 512 speech channels are added to the 128 internal service channels. The 512 speech channels convert to a 640-channel bus to the control complex.

The LGC common CP fill uses DS-1 interface CPs or filler faceplates for slots 1 through 5. Slots 6 and 7 can use the DS30A interface CPs or filler faceplates. Slots 15 and 16 use a filler faceplate or a universal tone receiver (UTR). Slot 18 uses the NT6X69AB common peripheral processor (CPP) message protocol CP. Slot 19 uses the NT6X79AA common peripheral controller equipment (CPCE) tone generator CP.

Parts

The LGC common CP fill contains the following parts:

- NT0X50AA–Filler faceplate
- NT2X70AD–Power converter
- NT2X70AE–Power converter
- NT3X90AC–Device controller cooling inverter unit

- NT6X40AA–DS30 network interface (NI)
- NT6X40AC–DS30 NI
- NT6X41AA–Speech bus formatter
- NT6X42AA–Channel supervision message (CSM) CP
- NT6X44AA–Time switch (TS)
- NT6X45AF–LGC/digital trunk controller (DTC) processor
- NT6X45BA–XMS-based PM processor
- NT6X46BA–Signaling processor memory (SPM) CP
- NT6X47AB–Master processor memory (MPM) CP
- NT6X50AA–DS-1 interface CP
- NT6X50AB–DS-1 interface CP
- NT6X69AB–CPP message protocol CP
- NT6X78AA–Custom local area signaling service modem resource CP
- NT6X78AB–Custom local area signaling service modem resource CP
- NT6X92BB–UTR

Design

The design of the NT6X02LA appears in the following table.

NT6X02LA parts (Sheet 1 of 6)

PEC	Slot	Description
NT0X50AA	1F-7F, 9F, 13F, 15F-17F, 19F, 23F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the CP fills. Each fill has a maximum of five spare card slots. Three of the slots (15, 16, and 17) have access to the signaling processor (SP) address bus and the parallel speech bus. The spare slots that remain (13 and 19) do not have access.
NT2X70AD	25F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards need in the fill. Each power converter supplies +5 V and 12 V for the cards in the fill. Power to the DS-1 CPs prevents loss of cards not duplicated during a power failure.

NT6X02LA (continued)

NT6X02LA parts (Sheet 2 of 6)

PEC	Slot	Description
NT2X70AE	25F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards need in the fill. Each power converter supplies +5 V and 12 V for the cards in the fill. Power to the DS-1 CPs prevents loss of cards not duplicated during a power failure.
NT3X90AC	-	*Device controller cooling inverter unit* The cooling inverter provides forced air cooling.
NT6X40AA	22F, 23F	*DS30 network interface CP* The DS30 NI card is available in two versions: NT6X40AA (eight ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.
NT6X40AC	22F	*DS30 network interface CP* The DS30 NI card is available in two versions: NT6X40AA (eight ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.

NT6X02LA (continued)

NT6X02LA parts (Sheet 3 of 6)

PEC	Slot	Description
NT6X41AA	21F	*Speech bus formatter* The speech bus formatter card contains two sections: the clock section and the formatting section. The clock section generates the 10.24-MHz shelf clock. The formatting section of the card provides parallel-to-serial conversion of the coded voice signals. These voice signals are signals received from the CSM interface card to proceed to the C-side links. The formatting section provides serial-to-parallel conversion of the coded voice signals received from the following processes: • C-side interface cards • network plane selection • T1 clock generation • parity error generation for test purposes
NT6X42AA	20F	*Channel supervision message CP* The CSM CP performs several functions. The CSM CP extracts the CSM bit from the C-side channels. The CSM CP assembles the CSM for each channel and inserts the CSM in the outgoing C-side bytes. The CSM CP performs parity checks on incoming bytes. The CSM CP performs parity generation on outgoing bytes.
NT6X44AA	14F	*Time switch* The TS converts between two streams. One stream is the stream received from (or transmitted to) the DS30 interface card or DS-1 interface card. The other stream is the parallel stream for use on the internal speech bus. When the SP controls the TS, the following two events occur. The TS associates the DS30 interface cards and DS-1 interface cards with the time slots on the parallel speech bus. The TS transfers data between the associated channel and the time slot.

NT6X02LA (continued)

NT6X02LA parts (Sheet 4 of 6)

PEC	Slot	Description
NT6X45AF	8F, 12F	*Line group controller/digital trunk controller processor* The LGC/DTC processor runs the programs that control the operation and maintenance of a PM. The LGC/DTC performs functions. These functions include digit collection, channel assignment, and message interpretation for the central control complex and PM.
NT6X45BA	8F, 12F	*XMS-based peripheral module processor* The XMS-based peripheral module (XPM) processor runs the programs that control the operation and maintenance of a PM. The XMS-based processor performs functions. These functions include digit collection, channel assignment, and message interpretation for the central control complex and PM.
NT6X46BA	11F	*Signaling processor memory card* The SPM card consists of RAM that stores data and software applications.
NT6X47AB	9F,10F	*Master processor memory card* The MPM card contains RAM that stores data and software applications for the MP and the SP. The SP uses SP memory management unit to access a section of the MP memory.
NT6X50AA	1F-5F	*DS-1 interface card* The DS-1 interface card contains two DS-1 ports. One to 10 cards are provisionable for each LTC module. Each port provides a two-way voice, data, and signaling interface. The card provides looparound paths for each DS-1 port to allow isolation of faults. The card provides transmission of local alarms and the detection of remote alarms and error conditions. These error conditions include loss of synchronization, bipolar error, and slip.

NT6X02LA (continued)

NT6X02LA parts (Sheet 5 of 6)

PEC	Slot	Description
NT6X50AB	1F-5F	*DS-1 interface card* The DS-1 interface card contains two DS-1 ports. One to 10 cards are provisionable for each LTC module. Each port provides a two-way voice, data, and signaling interface. The card provides looparound paths for each DS-1 port to allow isolation of faults. This card provides transmission of local alarms and the detection of remote alarms and error conditions. These error conditions include loss of synchronization, bipolar error, and slip.
NT6X69AB	18F	*Common peripheral processor message protocol CP* The messaging card provides interface for the parallel speech bus. The messaging card extracts control messages received on channel zero from the control module.
NT6X78AA	13F	*Custom local area signaling service modem resource CP* The CLASS modem resource card provides different residential (RES) enhanced features. This card can be in slot 16 of the SMU shelf. The CMR card must be present if the calling number delivery (CND) feature is present.

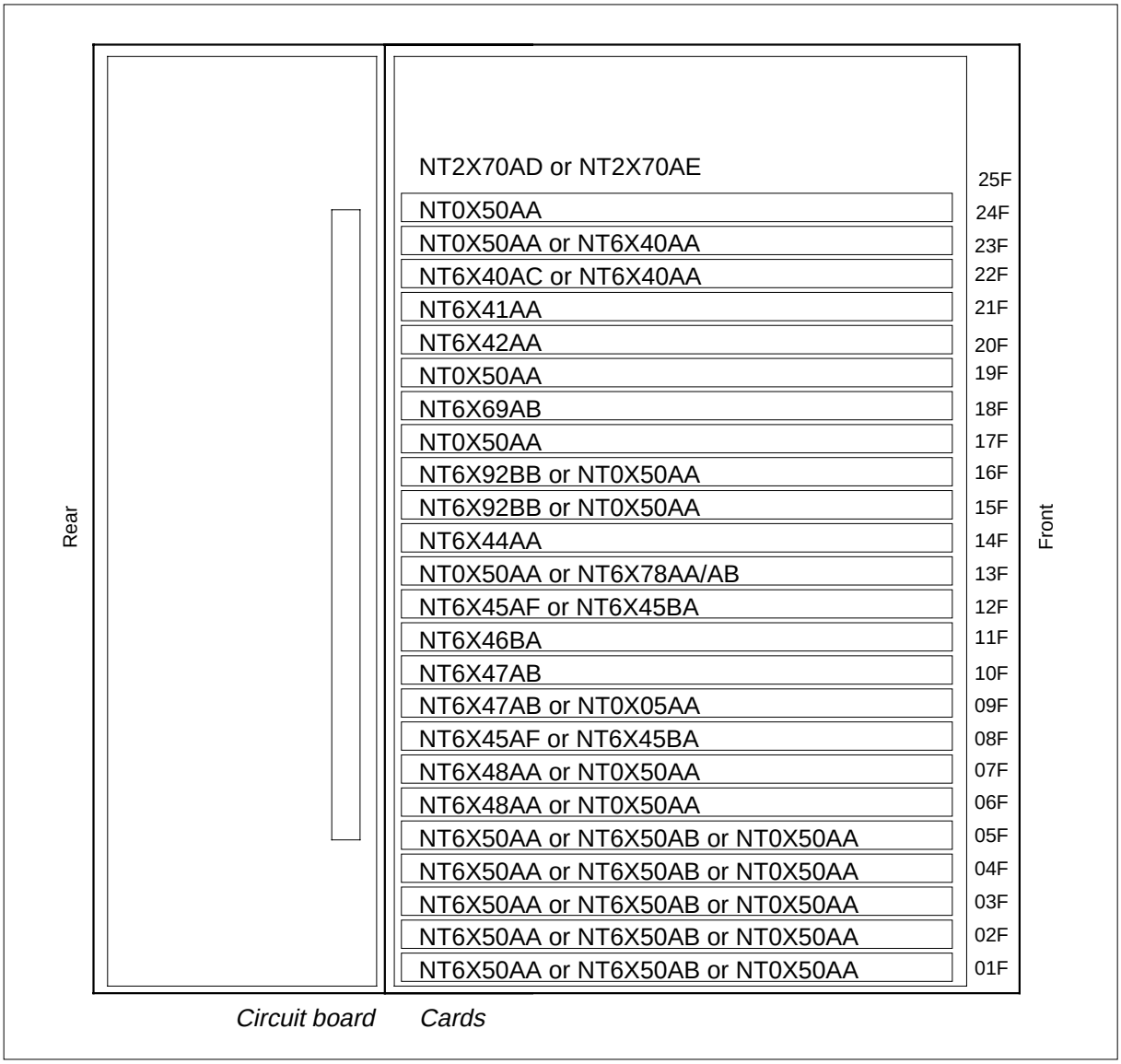
NT6X02LA (continued)

NT6X02LA parts (Sheet 6 of 6)

PEC	Slot	Description
NT6X78AB	[__.micro:caption ~bold {13F}	[__.micro:caption ~bold {} *Custom local area signaling service modem resource CP* The CMR card provides different RES enhanced features. The CMR card can be present in slot 16 of the SMU shelf. The CMR card must be present if the CND is present.
NT6X92BB	15F, 16F	*Universal tone receiver* The UTR is a 32-channel tone receiver that detects a different tones. These tones include dual-tone multifrequency (MF). The TS switches tone samples to the parallel speech bus. The UTR collects the tone samples at appropriate time slots. The UTR analyzes the samples and identifies the tones. The system sends the results to the XPM processor.

The design of the NT6X02LA appears in the following figure.

NT6X02LA parts



NT6X02MA

Product description

The NT6X02MA line trunk controller (LTC) shelf provides an interface. The interface is between central-side (C-side) DS30 links to the network and peripheral-side (P-side) DS30A links. The NT6X02MA LTC also provides an interface between the DS-1 links to subsidiary peripheral modules (PM). The LTC shelf has two units. One unit is active and provides the necessary processing and control functions. The other unit is in a standby mode and can take over call processing. The standby unit takes over call processing if a fault occurs in the active unit. Each unit has a control complex (CC). One CC is active at a time. The active CC provides control for both units. The LTC shelves are in the NT6X01AA subscriber module equipment (SME) frame.

The LTC shelf has C-side interface. The C-side ports can support a maximum of 16 pairs of DS30 links to the network. Four DS30 interface cards support the C-side links. Each DS30 interface cards can handle a maximum of eight DS30 ports. Link assignments are distributed over the four DS30 cards. The even-numbered links connect to plane 0 of the network. The odd-numbered links connect to plane 1. The system requires a minimum of three link pairs for correct interface with the network module (NM) and the CC.

Each DS30 card in the LTC shelf supplies power to 256 (8×32) channels for each plane. The cards supply power to the formatter cards in units 0 and 1. Each formatter handles a 512 channels for each plane. Each unit provides 256 channels. The combination of the two network planes occurs in the formatter. In the formatter, the system selects one plane for each channel. The system adds 512 speech channels to the 128 internal service channels. The system converts these channels to a 640-channel bus to the control complex.

The LTC shelf uses DS-1 interface cards or filler faceplates for slots 1 to 5. Slots 6 and 7 use a DS30A interface cards or filler faceplates. Slots 15 and 16 can use universal tone receiver (UTR) cards or filler faceplates. Slot 18 uses the NT6X69AB messaging card.

Parts

The LTC shelf consists of the following parts:

- NT0X50AA–Filler faceplate or panel
- NT2X70AD–Power converter
- NT2X70AE–Power converter
- NT3X90AC–Device controller cooling inverter unit
- NT6X40AA–DS30 network interface (NI)
- NT6X40AC–DS30 NI card

NT6X02MA (continued)

- NT6X41AA–Speech bus formatter
- NT6X42AA–Channel supervision message (CSM) interface card
- NT6X44AA–Time switch (TS)
- NT6X45AF–Master processor (MP) card
- NT6X45BA–MP card
- NT6X45BA–Signaling processor (SP) card
- NT6X46BA–Signaling processor memory (SPM) card
- NT6X47AB–Master processor memory (MPM) card
- NT6X48AA–DS30A interface card
- NT6X50AA–DS-1 interface card
- NT6X50AB–DS-1 interface card
- NT6X69AB–Messaging card
- NT6X70AA–Continuity card
- NT6X78AA–Custom local area signaling service modem resource
- NT6X78AB–Custom local area signaling service modem resource
- NT6X92BB–UTR

NT6X02MA (continued)

Design

The design of the NT6X02MA appears in the following table.

NT6X02MA parts (Sheet 1 of 6)

PEC	Slot	Description
NT0X50AA	1F-7F,9F, 13F, 15F-17F, 19F, 23F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the circuit pack (CP) fills. Each fill has a maximum of five spare card slots. The slots 15, 16 and 17 have access to the SP address bus and the parallel speech bus. The spare slots 13 and 19 do not have access.
NT2X70AD	25F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards need in the fill. Each power converter supplies +5 V and 12 V for the cards in the fill. The power converter provides power to the DS-1 CP to prevent loss of unduplicated cards during a power failure.
NT2X70AE	25F	*Power converter* The power converter converts the -48V dc to the lower voltages needed by the circuit cards in the fill. Each power converter supplies +5 V and 12 V for the cards in the fill. Power to the DS-1 CPs is provided to prevent loss of unduplicated cards during a power failure.
NT3X90AC	-	*Device controller cooling inverter unit* The cooling inverter provides forced air cooling.
NT6X40AA	22F, 23F	*DS30 network interface CP* The DS30 NI card is available in two versions: NT6X40AA (eight ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.

NT6X02MA (continued)

NT6X02MA parts (Sheet 2 of 6)

PEC	Slot	Description
NT6X40AC	22F, 23F	*DS30 network interface CP* The DS30 NI card is available in two versions: NT6X40AA (8 ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.
NT6X41AA	21F	*Speech bus formatter* The speech bus formatter card contains the clock section and the formatting section. The clock section generates the 10.24-MHz shelf clock. The formatting section of the card provides parallel-to-serial conversion of coded voice signals. The coded voice signals are received from the CSM interface card and will go to the C-side links. The card provides serial-to-parallel conversion of the coded voice signals received from the following: . The signals are received from the following: • the C-side interface cards • the network plane selection • the parity error generation for test purposes • the T1 clock generation
NT6X42AA	20F	*Channel supervision message CP* The CSM CP performs several functions. The CSM CP extracts the CSM bit from the C-side channels. The CSM CP assembles the CSM for each channel. The CSM CP inserts the CSM in the outgoing C-side bytes. The CSM CP performs parity check on all incoming and outgoing bytes. The CSM CP performs parity generation on all outgoing bytes.

NT6X02MA (continued)

NT6X02MA parts (Sheet 3 of 6)

PEC	Slot	Description
NT6X44AA	14F	*Time switch* The TS converts between the serial stream and the parallel stream. The serial stream is received from, or transmitted to, the DS30 interface card. The system uses the parallel stream on the internal speech bus. When the SP controls the TS, the TS associates interface cards with time slots. The TS associates the DS30 interface cards and DS-1 interface cards with time slots on the parallel speech bus. The TS transfers data between the associated channel and the time slot.
NT6X45AF	8F, 12F	*Master processor card* The MP card runs the programs that control the operation and maintenance of a PM. The MP card performs functions like a digit collection and channel assignment. The MP provides a description of messages for the central CC and PM.
NT6X45BA	8F,12F	*Signaling processor card* The SP card controls the formatter, the CSM card and the TS card. The SP collects the incoming control messages from the message protocol card (MPC). The SP passes outgoing control messages to the MPC for transmission. The MP and SP use direct memory access (DMA) to communicate. The DMA allows the SP to read and write to sections of the MP memory. The MP memory cannot access the SP memory.
NT6X46BA	11F	*Signaling processor memory card* The SPM card contains RAM used to store data and software applications.
NT6X47AB	9F,10F	*Master processor memory card* The MPM card consists of RAM used to store data and software applications for the MP and the SP. The SP can access a section of the MP memory with the memory management unit of the SP.

NT6X02MA (continued)

NT6X02MA parts (Sheet 4 of 6)

PEC	Slot	Description
NT6X48AA	6F, 7F	*DS30A interface card* The DS30A interface card contains ten separate ports. Each port provides a two-way voice and data interface and carries a 32-channel, 2.56-Mbps bit stream. Each DS30A port contains a looparound circuit for fault isolation.
NT6X50AA	1F-5F	*DS-1 interface card* The DS-1 interface card contains two DS-1 ports. One to ten cards are provisionable for each LTC module. Each port provides a two-way voice, data and signaling interface. The card provides the following features: • looparound paths for each DS-1 port to allow isolation of faults • transmission of local alarms • detection of remote alarms • detection of error conditions like a loss of synchronization, bipolar error and slip
NT6X50AB	1F-5F	*DS-1 interface card* The DS-1 interface card contains two DS-1 ports. One to ten cards are provisionable for each LTC module. Each port provides a two-way voice, data and signaling interface. The card provides the following features: • looparound paths for each DS-1 port to allow isolation of faults • transmission of local alarms • detection of remote alarms • detection of error conditions like a loss of synchronization, bipolar error, and slip

NT6X02MA (continued)

NT6X02MA parts (Sheet 5 of 6)

PEC	Slot	Description
NT6X70AA	13F	*Continuity card* The continuity card detects tones used in call processing to verify the continuity of the voice/data path between LTCs. The card monitors and records the frequency and level of the tones. The continuity card stores this data for use by the SP in the LTC.
NT6X69AB	18F	*Messaging card* The messaging card provides interface for the parallel speech bus. The messaging card extracts control messages received on channel zero from the control module.
NT6X78AA	13F	*Custom local area signaling service modem resource CP* The CLASS modem resource (CMR) card provides different residential (RES) improved features. The CMR card can be in slot 16 of the SMU shelf. The CMR card is necessary to provision a calling number delivery (CND) feature.
NT6X78AB	13F	*Custom local area signaling service modem resource CP* The CMR card provides different RES improved features. The CMR card can be in slot 16 of the SMU shelf. The CMR card is necessary to provision the CND feature.

NT6X02MA (continued)

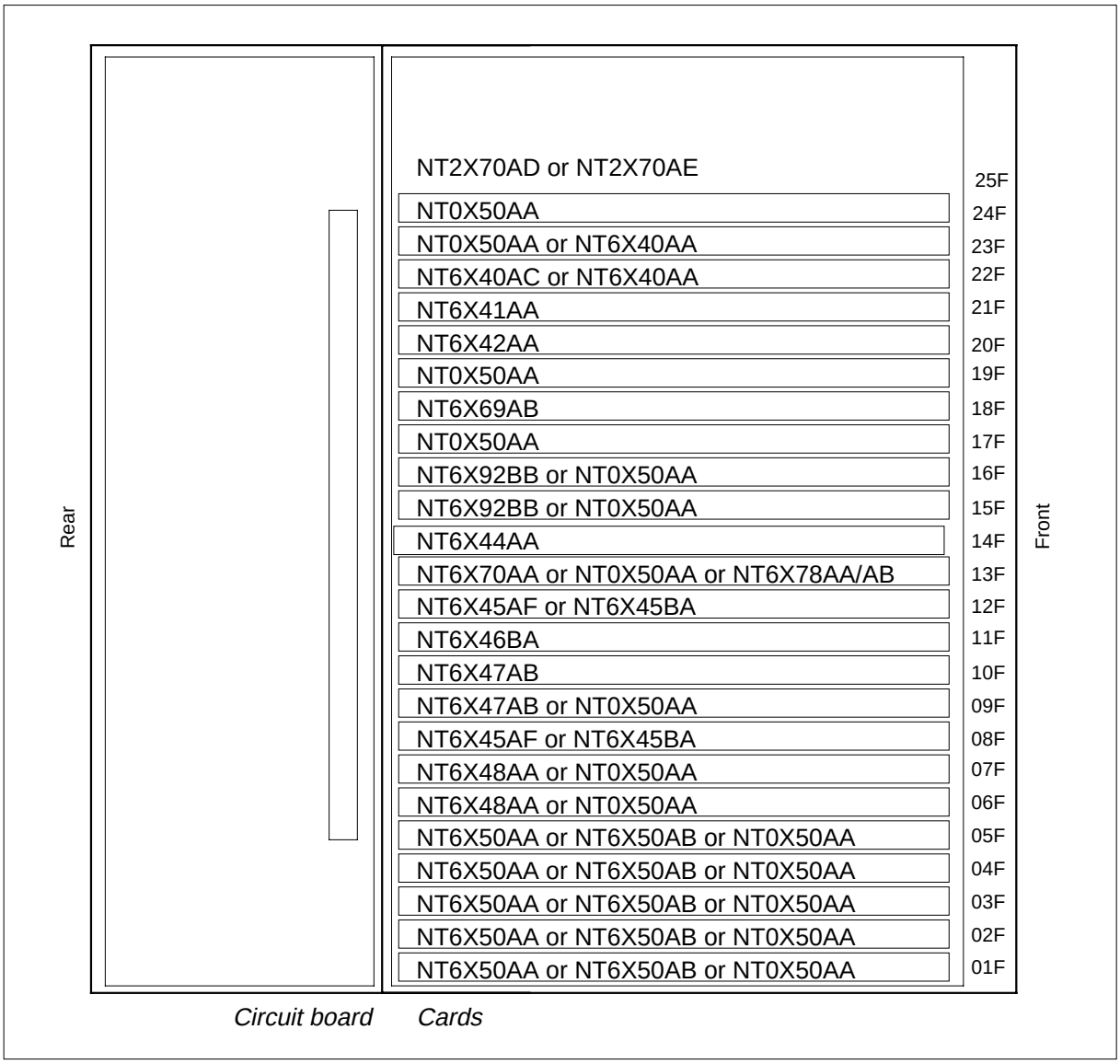
NT6X02MA parts (Sheet 6 of 6)

PEC	Slot	Description
NT6X85AB	1F-5F	*DS-1 interface CP* The DS-1 interface CP contains two DS-1 ports. One to ten cards are provisionable for each SMU. Each port provides a two-way voice, data and signaling interface. The card provides the following features: • looparound paths for each DS-1 port to allow isolation of faults • transmission of local alarms • detection of remote alarms • detection of error conditions like a loss of synchronization, bipolar error and slip
NT6X92BB	15F, 16F	*Universal tone receiver* The UTR is a 32-channel tone receiver that detects many tones. These tones include dual-tone multifrequency (DTMF) and multifrequency (MF). The TS switches the tone samples on the parallel speech bus. The UTR collects the samples at correct time slots. The UTR analyzes the samples and identifies the tones. The UTR sends the results to the SP.

The design of the NT6X02MA appears in the following figure.

NT6X02MA (end)

NT6X02MA parts



NT6X02NA

Product description

The ISDN peripheral controller applications use the ISDN common peripheral controller (ISDN CPC) common circuit pack. The NT6X02NA ISDN CPC common circuit pack (CP) provides an interface. The interface is between C-side DS30 links to the network and P-side DS-1 digital trunks.

The ISDN CPC common CP has two units. One unit is active and provides the necessary processing and control functions. The other unit is in a standby mode and can take over call processing. The standby unit takes over call processing if a fault occurs in the active unit. Each unit has a control complex (CC). One CC is active at a time. The active CC provides control for both units.

The ISDN CPC common CP has C-side interface. The C-side ports can support a maximum of 16 pairs of DS30 links to the network. Four DS30 interface cards support the C-side links. Each of these DS30 interface cards can handle a maximum of eight DS30 ports. Link assignments are distributed over the four DS30 cards. The even-numbered links connect to plane 0 of the network. The odd-numbered links connect to plane 1. The system requires a minimum of three link pairs for correct interface with the network module (NM) and the CC.

Each DS30 card in the ISDN CPC common CP supplies power to 256 (8 by 32) channels in each plane. The DS30 card supplies power to 256 channels in each plane to the formatter cards in both units 0 and 1. Each formatter handles a total of 512 channels in each plane. Each unit provides 256 channels. The formatter combines two network planes. In the formatter, the system selects one plane for each channel. The system adds the 512 speech channels to the 128 internal service channels. The system converts the channels to a 640-channel bus to the control complex.

The ISDN CPC common CP uses DS-1 interface cards, filler faceplates or D-channel handlers in slots 1-5. Slot 15 uses a universal tone receiver (UTR). Slot 16 uses an ISDN signaling preprocessor. Slot 18 uses the NT6X69AB or NT6X69AC common peripheral processor (CPP) message protocol card.

Parts

The NT6X02NA ISDN CPC common circuit pack contains the following parts:

- NTBX01AA–ISDN signaling preprocessor
- NTBX02AA–D-channel handler (DCH)
- NT0X50AA–filler face plate
- NT2X70AE–power converter

NT6X02NA (continued)

- NT6X40AC–DS30 network interface card
- NT6X40FA–DS512 network interface card
- NT6X41AA–speech bus formatter card
- NT6X42AA–channel supervision message card
- NT6X44AA–time switch card
- NT6X45BA–XMS-based peripheral module processor
- NT6X46BA–signaling processor memory card
- NT6X46BB–signaling processor memory plus card
- NT6X47AB–master processor memory plus card
- NT6X48AA–DS30A line controller module interface card
- NT6X50AB–DS-1 interface card
- NT6X69AC–CPP messaging protocol and tone card
- NT6X92BB–universal tone receiver

Design

The parts of the NT6X02NA appears in the following table. The design of the NT6X02NA appears in the following figure.

NT6X02NA parts (Sheet 1 of 5)

PEC	Slot	Description
NTBX01AA	16F	*ISDN signaling preprocessor* The ISDN signaling preprocessor (ISP) is used as a messaging link between the master processor, signaling processor and the D-channel handlers (DCH). The SP is an interface between the D-channels and the signaling processor (SP) and the master processor (MP). The ISP receives information from the D-channels through the speech bus. The system processes and transfers the information to the master processor memory (MPM) or the signaling processor memory (SPM). The the system transfers or processes the information through the signaling processor A-bus. The information flows in the same method from the processors to the D-channel. Each line group controller unit has one ISP.

NT6X02NA (continued)

NT6X02NA parts (Sheet 2 of 5)

PEC	Slot	Description
NTBX02AA	1-5F	*D-channel handler* The DCH is the main interface to all D-channels through the speech bus. The DCH facilitates communication with an ISDN terminal on request from the terminal or the line group controller (LGC) master processor (MP). The DCH can maintain a logical link with any ISDN terminal from the packet handler or the LGC MP. The DCH facilitates communication with the packet handler or LGC MP on request. The DCH maintains the connection with the packet handler while data flow over the channel. The active LGC communicates with the DCHs. The DCH can verify and route D-channel frames according to the type of the frame. The frame types are D-call control and D-packet.
NT0X50AA	1-7F, 9F, 13F, 17F, 19F, 23-24F	*Filler faceplate* The filler faceplate fills empty card slots in the card fills. Each fill has a maximum of five spare card slots. The slots 15, 16 and 17 have access to the signaling processor (SP) address bus and the parallel speech bus. The spare slots, 13 and 19, do not have access.
NT2X70AE	25F	*Power converter card* The power converter card converts the dc voltage of -48 V to the lower voltages that the cards in the fill need. Each power converter supplies +5 and 12 V for the cards in the fill. The power converter provides power to the DS-1 cards to prevent loss of unduplicated cards during a power failure.
NT6X40AC	22F	*DS30 network interface card* The DS30 network interface card is a 16-port interface. The card provides a C-side interface for DS30 links to the network. Each port of a DS30 network interface card provides a 2-way voice and data interface. Each port contains a looparound circuit for fault isolation.

NT6X02NA (continued)

NT6X02NA parts (Sheet 3 of 5)

PEC	Slot	Description
NT6X40FA	22F	*DS512 network interface card* The DS512 network interface card provides a C-side interface for DS512 links to the network. Each port of a DS512 network interface card provides a 2-way voice and data interface. Each port contains a looparound circuit for fault isolation. The interface card uses a fiber optic cable to connect the 512 pulse code modulation circuits to the extended network.
NT6X41AA	21F	*Speech bus formatter card* The speech bus formatter card contains the clock section and the formatting section. The clock section generates the 10.24-MHz shelf clock. The formatting section provides the following features: • parallel-to-serial conversion of coded voice signals received from the CSM interface card. These signals will go to the C-side links • serial-to-parallel conversion of coded voice signals received from the C-side interface cards • network plane selection • parity error generation for test purposes • T1 clock generation
NT6X42AA	20F	*Channel supervision message card* The channel supervision message (CSM) interface card performs the following functions: • extracts the CSM bit from the C-side channels • assembles the CSM for each channel • inserts the CSM into the outgoing C-side bytes The CSM card performs parity checks on incoming and outgoing bytes.

NT6X02NA (continued)

NT6X02NA parts (Sheet 4 of 5)

PEC	Slot	Description
NT6X44AA	14F	*Time switch card* The time switch card converts between the serial stream and the parallel stream. The serial stream is received from, or transmitted to the DS30, DS30A LCM, or DS-1 interface. The system uses the parallel stream on the internal speech bus. When the XPM processor controls the time switch, the time switch associates interface cards with time slots. The time switch associates the DS30, DS30A LCM or DS-1 interface cards with one of the time slots on the parallel speech bus. The time switch transfers data between the associated channel and the time slot.
NT6X45BA	8F	*XMS-based peripheral module processor* The XPM processor runs the programs that control the operation and maintenance of a peripheral module. The XPM performs functions like a digit collection and channel assignment. The XPM provides a description of messages for the central CC and PM.
NT6X46BA	11F	*Signaling processor memory card* The RAM used to store data and software applications is the signaling processor memory (SPM) card.
NT6X46BB	11F	*Signaling processor memory plus card* The RAM used to store data and software applications is the signaling processor memory (SPM) plus card.
NT6X47AB	9-10F	*Master processor memory plus card* The RAM used to store data and software applications is the master processor memory (MPM) plus card. The MPM stores data and applications for the master processor and the signaling processor. The signaling processor can access a section of the MP memory when the MPM uses the memory management unit.

NT6X02NA (continued)

NT6X02NA parts (Sheet 5 of 5)

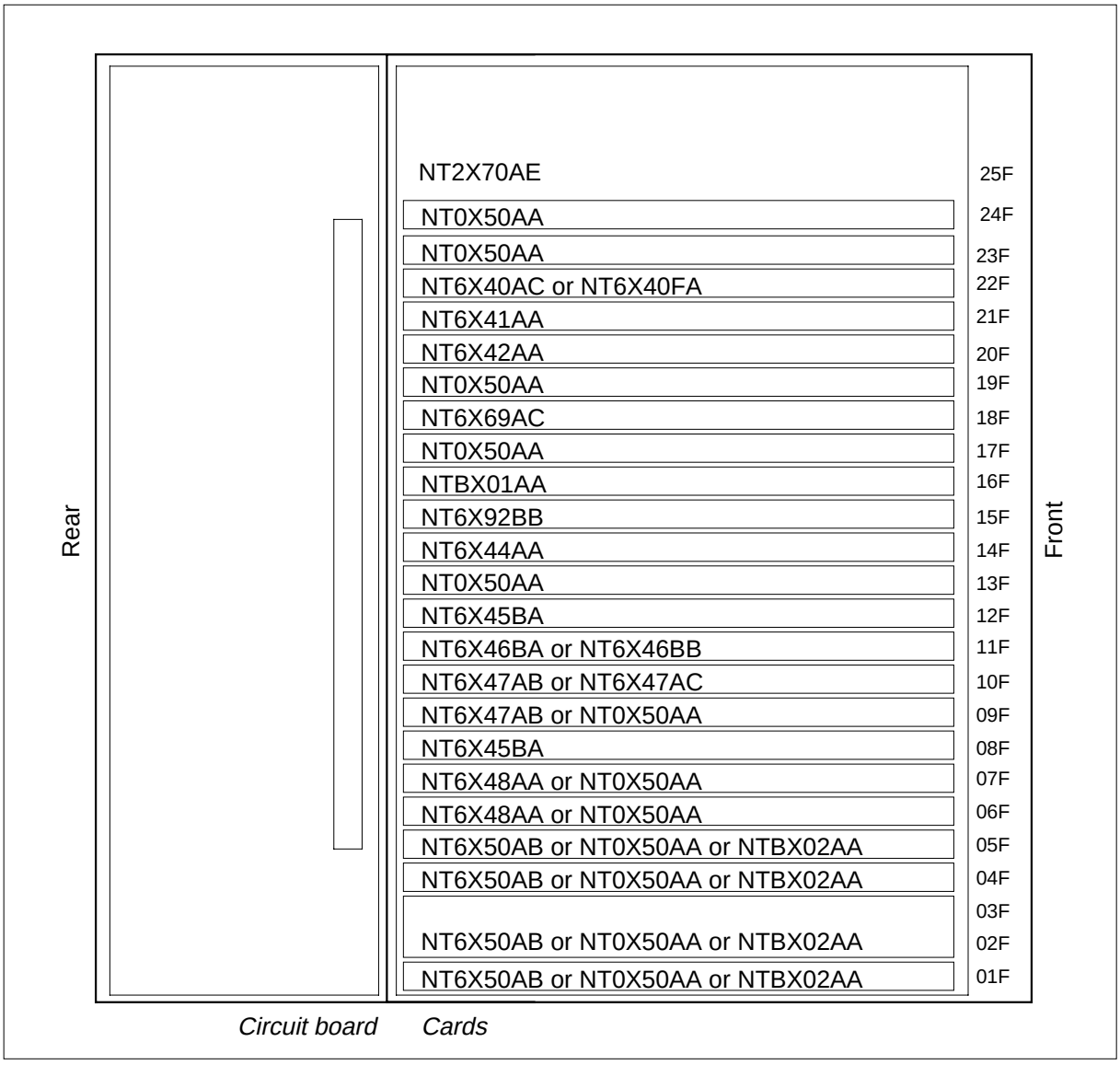
PEC	Slot	Description
NT6X48AA	6-7F	*DS30A line controller module interface card* The DS30A interface card contains ten separate ports. Each port carries a 32-channel, 2.56 Mbit/s stream and provides a 2-way voice and data interface. Each DS30A port contains a looparound circuit for fault isolation.
NT6X50AB	1-5F	*DS-1 interface card* The DS-1 interface card contains two DS-1 ports. One to ten card are provisionable for each LTC module. Each port provides a 2-way voice, data and signaling interface. The card provides the following features: • looparound paths for each DS-1 port to allow isolation of faults • transmission of local alarms • detection of remote alarms • detection of error conditions like a loss of synchronization, bipolar error and slip
NT6X69AC	18F	*Common peripheral processor messaging protocol and tone card* The messaging card provides interface for the parallel speech bus. The messaging card extracts control messages received on channel 0 from the control module.
NT6X92BB	15F	*Universal tone receiver* The UTR is a 32-channel tone receiver that detects many tones. These tones include dual-tone multifrequency (DTMF) and multifrequency (MF). The TS switches the tone samples on the parallel speech bus. The UTR collects the tone samples at correct time slots. The UTR analyzes the samples and identifies the tones. The system sends the results to the XPM processor.

NT6X02NA (end)

The following figure indicates the design of the NT6X02DH.

Note: This diagram is not drawn to scale.

NT6X02NA parts



NT6X02QA

Product description

The NT6X02QA international digital trunk controller (IDTC) shelf provides an interface. The interface exists between the central-side (C-side) DS30 links to the network and pulse-code-modulation (PCM30) digital trunks. The IDTC shelf is similar to the version from the North American DTC. The IDTC uses international digital trunks instead of the North American DS-1 digital trunks.

The IDTC shelf has two units. One unit is active and provides processing and control functions. The other unit is in a standby mode. The unit in standby mode can take over call processing if a fault occurs in the active unit. Each unit has a control complex (CC). Only one CC is active at a time. The active CC provides control for both units. The IDTC shelves are in the NT6X01BA international common peripheral equipment (ICPCE) frame.

The IDTC shelf has a C-side interface. The C-side ports can support a maximum of 16 pairs of DS30 links to the network. Four DS30 interface cards support the C-side links. Each of the DS30 interface cards can handle a maximum of eight DS30 ports. The IDTC shelf distributes link assignments over the four DS30 cards. The even-numbered links connect to plane 0 of the network. The odd-numbered links connect to plane 1 of the network. Interface with the network module (NM) and the CC requires a minimum of three link pairs.

Each DS30 card in the IDTC shelf powers 256 (8×32) channels for each plane to the formatter cards in both units. Each formatter handles a total of 512 channels for each plane. The formatter handles 256 channels from each unit. The two network planes are combined in the formatter. The formatter selects one plane or the other on a per-channel base. The 512 speech channels are added to the 128 internal service channels. The channels are converted to a 640-channel bus to the CC.

The IDTC shelf uses PCM30 interface cards or filler faceplates for slots 1 through 4. The IDTC uses filler faceplates in slots 5 and 6. The IDTC uses NT6X44AB time switch (TS) card in slot 7. The IDTC shelf uses universal tone receiver (UTR) cards for slots 8 and 9. The IDTC shelf uses the NT6X43BA messaging card in slot 10.

Parts

The IDTC shelf contains the following parts:

- NT0X50AA–Filler faceplate or panel
- NT2X70AD–Power converter
- NT3X90AC–Device controller cooling inverter unit

- NT6X27AA–PCM30 interface card
- NT6X27AB–PCM30 interface card
- NT6X28AA–Signaling card
- NT6X40AB–DS30 network interface (NI) card
- NT6X41AB–Speech bus formatter
- NT6X42AA–Channel supervision message (CSM) card
- NT6X43BA–Messaging card
- NT6X44AB–TS card
- NT6X45AD–Master processor (MP) card
- NT6X46AB–Signaling processor memory (SPM) card
- NT6X47AB–Master processor memory (MPM) card
- NT6X92AA–UTR

Design

The design of the NT6X02QA appears in the following table.

NT6X02QA components (Sheet 1 of 6)

PEC	Slot	Description
NT0X50AA	1F-7F, 9F, 13F, 15F-17F, 19F, 23F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the CP fills. Each fill can contain a maximum of five spare card slots. Slots 15, 16 and 17 have access to the signaling processor (SP) address bus and the parallel speech bus. The remaining spare slots 13 and 19 do not have access.
NT2X70AD	25F	*Power converter* The power converter converts the -48V dc to a lower voltage. In the fill, the circuit cards require lower voltages. The power converter supplies +5 V and 12 V for the cards in the fill. The power converter supplies power to the DS-1 circuit packs (CP) to prevent loss of unduplicated cards during a power failure.

NT6X02QA (continued)

NT6X02QA components (Sheet 2 of 6)

PEC	Slot	Description
NT3X90AC	-	*Device controller cooling inverter unit* The cooling inverter provides forced air cooling.
NT6X27AA	1F-4F	*PCM30 interface card* The PCM30 interface card provides an interface between an NT6X02 common peripheral controller (CPC) and European-standard PCM30 trunk transmission equipment. The PCM30 translates PCM voice signals and signaling data between two 32-channel, 2.048-Mbps external PCM 30 trunk circuits and one 64-channel, 5.12-Mbps duplicated port in the CPC. The PCM30 receives data streams from the four-wire PCM trunk transmission equipment. The PCM30 converts the high-density bipolar 3 (HDB3) data to a DS30 format. The system uses the DS30 format for data transmission to the DS-60 TS card. The card receives PCM30 data from the TS card. The card converts the data to an HDB3 format for transmission to the trunk transmission equipment. The PCM30 provides a looparound function for testing purposes.

NT6X02QA (continued)

NT6X02QA components (Sheet 3 of 6)

PEC	Slot	Description
NT6X27AB	4F	*PCM30 interface card* The PCM30 interface card provides an interface between an NT6X02 CPC and European standard PCM30 trunk transmission equipment. The PCM30 translates PCM voice signals and signaling data between two 32-channel, 2.048-Mbps external PCM 30 trunk circuits and one 64-channel, 5.12-Mbps duplicated port in the CPC. The PCM30 receives data streams from the four-wire PCM trunk transmission equipment. The PCM30 converts the high-density bipolar 3 (HDB3) data to a DS30 format. The system uses the DS30 format for data transmission to the DS-60 TS card. The card receives PCM30 data from the TS card. The card converts the data to an HDB3 format for transmission to the trunk transmission equipment. The PCM30 provides a looparound function for testing purposes.
NT6X28AA	19F	*Signaling card* The NT6X28AA signaling card uses channel time slot (CTS) 16 to extract signaling information from the parallel speech buses of the IDTC. The NT6X28AA also uses CTS 16 to insert signaling information in the parallel speech buses of the IDTC. The CTS 0 communicates control and status information between the processor and the PCM30 interface card.
NT6X40AB	22F, 23F	*DS30 network interface CP* The DS30 NI card has two versions: NT6X40AA (eight ports) and NT6X40AC (16 ports). The card provides a C-side interface for DS30 links to the network. Each port of a DS30 NI card provides a two-way voice and data interface. Each port also contains a looparound circuit for fault isolation.

NT6X02QA (continued)

NT6X02QA components (Sheet 4 of 6)

PEC	Slot	Description
NT6X41AB	22F	*Speech bus formatter* The speech bus formatter card has two sections: the clock section and the formatting section. The clock section generates the 10.24-MHz shelf clock. The formatting section provides parallel-to-serial conversion of the encoded voice signals. The formatter receives the voice signals from the CSM interface card. The voice signals are for the C-side links. The formatter also provides serial-to-parallel conversion of the encoded voice signals. The voice signals are received from the following: • C-side interface cards • network plane selection • parity error generation for test purposes • T1 clock generation
NT6X42AA	21F	*Channel supervision message CP* The CSM CP performs the following functions: • extracts the CSM bit from the C-side channels • assembles the CSM for each channel • inserts the CSM into the outgoing C-side bytes • performs parity checks on all incoming bytes • performs parity generation on all outgoing bytes
NT6X43BA	10F	*Messaging card* The messaging card provides interface for the parallel speech bus. The messaging card extracts control messages received on channel zero from the control module (CM).

NT6X02QA (continued)

NT6X02QA components (Sheet 5 of 6)

PEC	Slot	Description
NT6X44AB	7F	*Time switch* The TS converts between the serial stream and the parallel stream. The serial stream is received from or transmitted to the DS30 interface card or DS-1 interface card. The system uses the parallel stream on the internal speech bus. When the SP controls the TS, the TS associates the interface cards with the time slots. This process involves the DS30 and the DS-1 interface cards and the time slots on the parallel speech bus. The TS also transfers data between the associated channel and the time slot.
NT6X45AD	12F, 14F	*Line group controller/digital trunk controller processor* The LGC/DTC processor runs the programs that control the operation and maintenance of a peripheral module (PM). The LGC/DTC performs digit collection, channel assignment, and description of messages for the central CC and PM.
NT6X46AB	11F	*Signaling processor memory card* The SPM card contains RAM. The SPM card uses the RAM to store data and software applications.

NT6X02QA (continued)

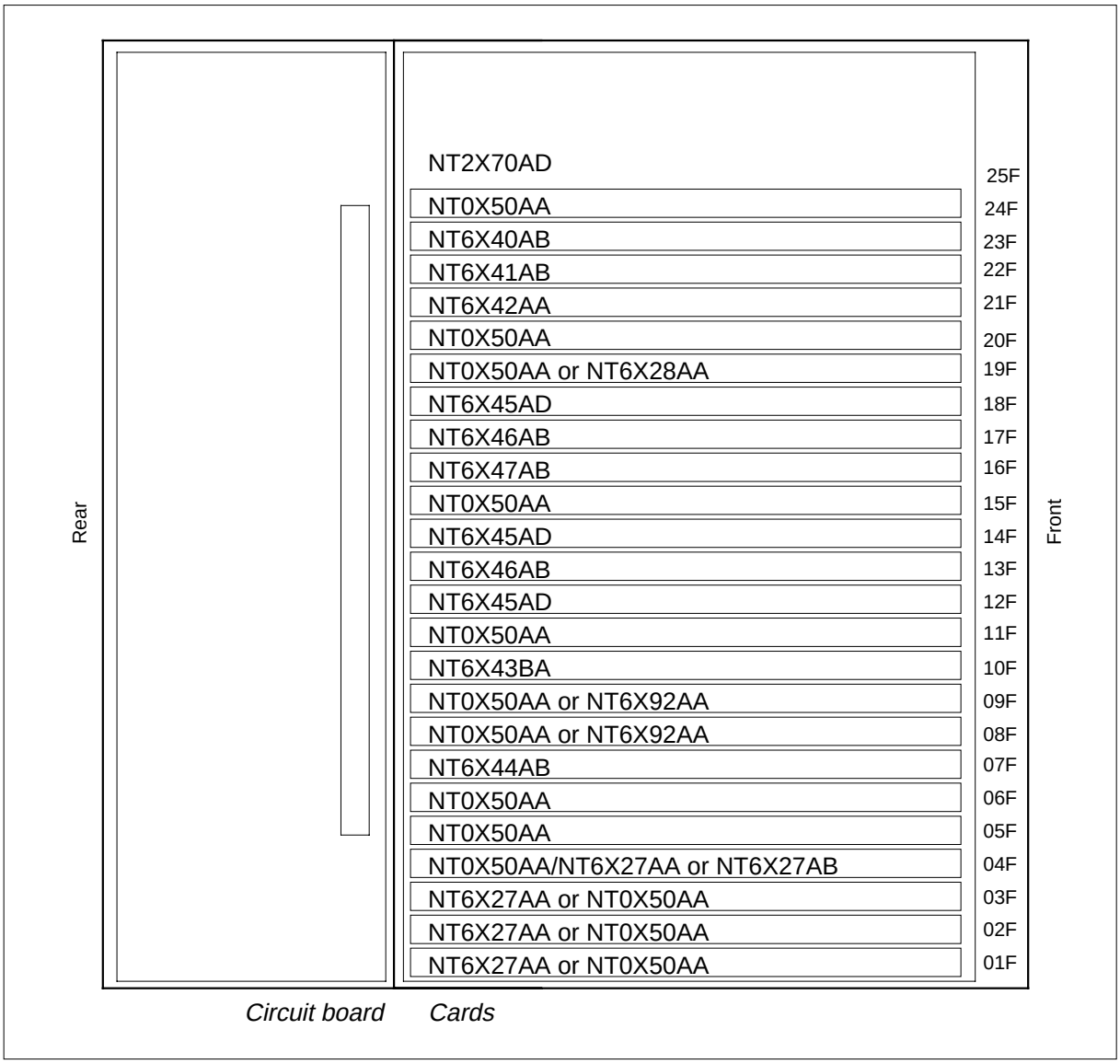
NT6X02QA components (Sheet 6 of 6)

PEC	Slot	Description
NT6X47AB	16F	*Master processor memory card* The MPM contains RAM. The MPM uses RAM to store data and software applications for both the MP and the SP. The SP uses a memory management unit to access part of the MP memory.
NT6X92AA	8F, 9F	*Universal tone receiver* The UTR is a 32-channel tone receiver. The UTR detects many tones, including dual-tone multifrequecny (DTMF) and multifrequency (MF). The TS switches the tone samples to the parallel speech bus. The UTR collects the tone samples at the correct time slots. The UTR analyzes the samples and identifies the tones. The UTR sends the results to the SP.

The design of the NT6X02QA appears in the following figure.

NT6X02QA (end)

NT6X02QA components



NT6X02UA

Product description

The NT6X02UA circuit pack is required for international applications of a PCM-30 digital trunk controller module or a PCM-30 line group controller module. The PCM-30 digital trunk controller and the PCM-30 line group controller modules have two shelves. These modules are mounted in the NT6X01AC offshore common peripheral controller equipment (CPCE) frame. The circuit cards are mounted in the NT6X0216 controller array shelf assembly international. Each module requires one common circuit pack (CP).

The common CP occupies two slots in each NT6X0216 shelf assembly international. The content of the other slots depends on the application of the modules in the CPCE frame. Applications can include the following:

- ISDN services
- connections to the Enhanced Network (ENET),
- connections to the Fiber Enhanced Network
- common channel signaling 7
- R1 signaling
- Centrex
- electronic business set
- Integrated Business Network
- plain ordinary telephone service

If the CPCE frame contains one module, the CPCE frame assigns NT6X02UA common CP to shelf positions 18 and 32. If two modules are in the frame, the CPCE assigns NT6X02UA common CP to the shelf positions 51 and 65.

The NT6X02UB replaces the NT6X02UA.

Parts

The NT6X02UA common CP contains the following parts:

- NT6X41AA–speech bus formatter card
- NT6X42AA–channel supervision message (CSM) card

Design

The parts and design of the NT6X02UA common CP appear in the following table.

NT6X02UA parts (Sheet 1 of 2)

PEC	Slot	Description
NT6X41AA	21F	*Speech bus formatter card* The NT6X41AA contains a formatting section and a clock section. The clock section generates the 10.24-MHz shelf clock signal. The clock section also generates a number of other signals that different parts of the shelf use. The formatting section handles16 DS30 ports in each direction. The main features of the NT6X41AA are: • parallel-to-serial conversion of transmit pulse code modulated data • serial-to-parallel conversion of receive pulse code modulated data • network plane selection • CSM looparound • network looparound • parity error generation • T1 clock generation

NT6X02UA (continued)

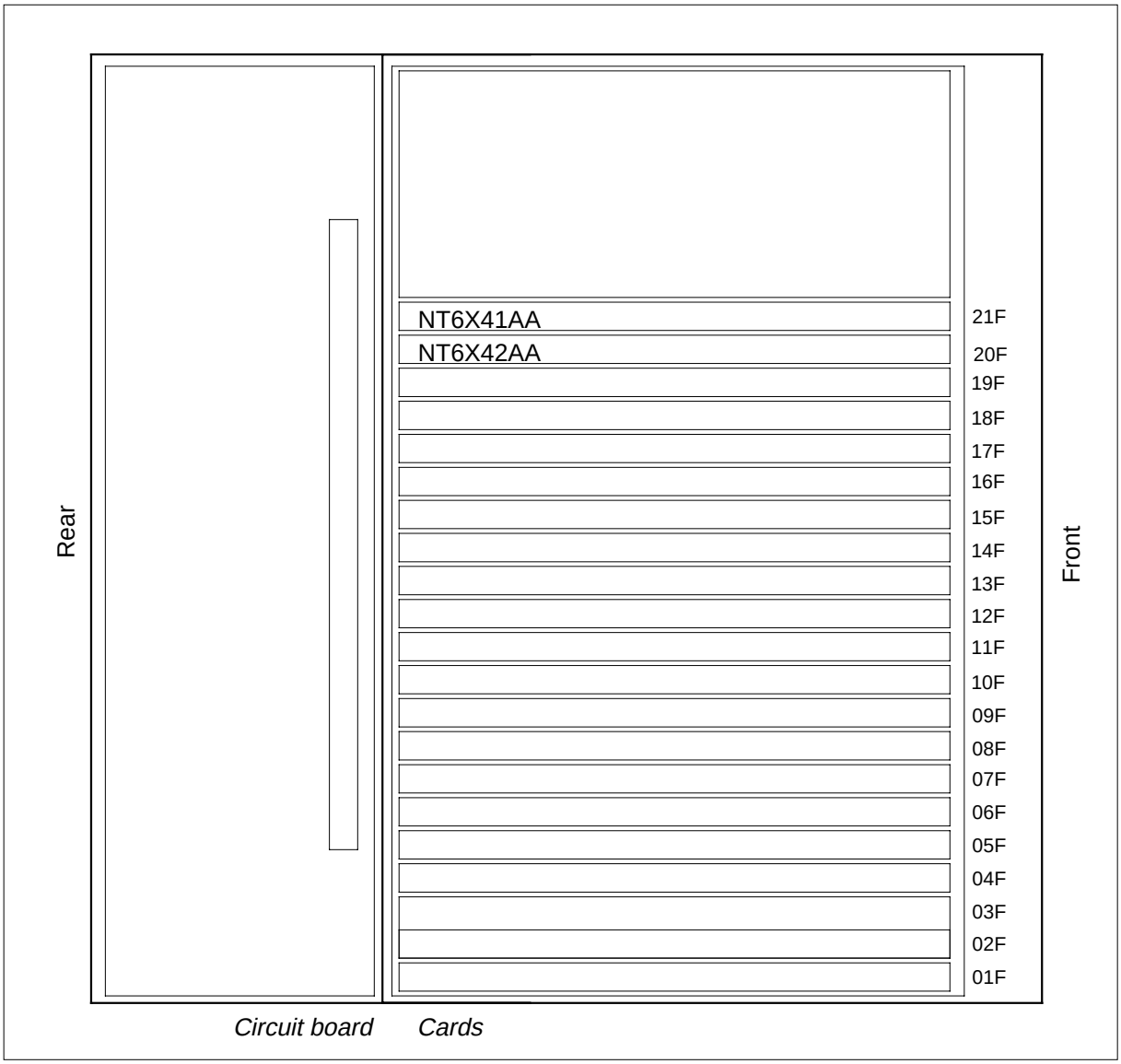
NT6X02UA parts (Sheet 2 of 2)

PEC	Slot	Description
NT6X42AA	20F	*Channel supervision message card* The NT6X42AA CSM card performs the functions required for channel supervision messaging between peripherals. The CSM can accommodate 16 network ports or 512 channels. A channel connection between two peripherals can establish a duplex path. The duplex path transmits a 10 bit byte in each direction every frame time. The parity bit maintains odd parity for each transmitted byte. The CSM bit provides a 3.2-kbit/s message link between the connected peripherals on a path by path setup. The channel data byte transmits the information required to set up, maintain, and terminate a call. The central control for every path setup gives the value of the 8 bit integrity. The integrity byte makes sure that the pulse code modulation (PCM) path setup from one peripheral to another is correct. The integrity byte also provides a means to measure the quality of the speech path in the connection. On the network side of the card, the NT6X42AA communicates with the NT6X41AA formatter card. On the peripheral side, the NT6X42AA originates the 8 bit parallel receive PCM bus. The NT6X42AA terminates the transmit PCM speech bus. The NT6X42AA performs the following functions: • extracts CSM bit from network channels • checks parity on all bytes • inserts a transmit synchronization pattern into the PCM path • counts frame and logic • checks integrity • matches integrity and reports parity error • synchronizes pattern transmission • provides a signaling processor interface

The parts and design of the NT6X02UA common CP appear in the following figure.

NT6X02UA (end)

NT6X02UA parts



NT6X02UB

Product description

International applications of a PCM-30 digital trunk controller module or a PCM-30 line group controller module must use the circuit pack. These shelves are mounted in the NT6X01AC offshore common peripheral controller equipment (CPCE) frame. The location of the circuit card is in the NT6X0216 controller array shelf assembly international. Each module requires one NT6X02UB common circuit pack (CP).

The common CP occupies two slots in each NT6X0216 shelf assembly. The content of the other slots depends on the application of the CPCE frame and module. Applications can include the following:

- ISDN services
- connections to the Enhanced Network
- connections to the Fiber Enhanced Network
- common channel signaling 7
- R1 signaling
- Centrex
- electronic business set
- Integrated Business Network
- plain ordinary telephone service (POTS)

If the CPCE frame contains only one module, the CPCE assigns common CP to shelf positions 18 and 32. If there are two modules in the frame, the CPCE assigns the common CP to shelf positions 51 and 65.

The NT6X02UB replaces the NT6X02UA.

Parts

The NT6X02UB common circuit pack contains the following parts:

- NT6X41AB–speech bus formatter card
- NT6X42AA–channel supervision message (CSM) card

Design

The parts and the position of the NT6X02UB common CP appear in the following table.

NT6X02UB parts (Sheet 1 of 3)

PEC	Slot	Description
NT6X41AB	21F	Speech bus formatter card The NT6X41AB is a new version of the NT6X41AA formatter card. The NT6X41AB is like the NT6X41AA. The NT6X41AB uses the buffers at the DS30 interface more. The NT6X41AB has a formatting section and a clock section. The clock section generates the 10.24-MHz shelf clock signal. The clock section also generates a number of other signals that different parts of the shelf use. The formatting section handles 16 DS30 ports in both directions. The main features of the NT6X41AB are: • parallel-to-serial conversion of transmit pulse code modulated data • serial-to-parallel conversion of receive pulse code modulated data • network plane selection • CSM looparound • network looparound • parity error generation • T1 clock generation

NT6X02UB (continued)

NT6X02UB parts (Sheet 2 of 3)

PEC	Slot	Description
NT6X42AA	20F	Channel supervision message card The NT6X42AA channel supervision message card performs all the functions required for channel supervision messaging between peripherals. The NT6X42AA can accommodate 16 network ports or 512 channels. Any channel connection between two peripherals establishes a duplex path. The duplex path transmits a 10-bit byte in each direction every frame time. The parity bit maintains odd parity for all transmitted bytes. The CSM bit provides a 3.2-kbit/s message link between the connected peripherals on a path by path structure. The channel data byte transmits the information required to set up, maintain and end the call. The central control for every path structure gives the value of the 8 bit integrity byte. The integrity byte makes sure that the pulse code modulation (PCM) path setup from one peripheral to another is correct. The integrity byte also provides the means to measure the quality of the speech path in the connection. On the network side of the card, the NT6X42AA communicates with the NT6X41AB formatter card. On the peripheral side, the NT6X42AA originates the 8-bit parallel receive PCM bus. The NT6X42AA ends the transmit PCM speech bus.

NT6X02UB (continued)

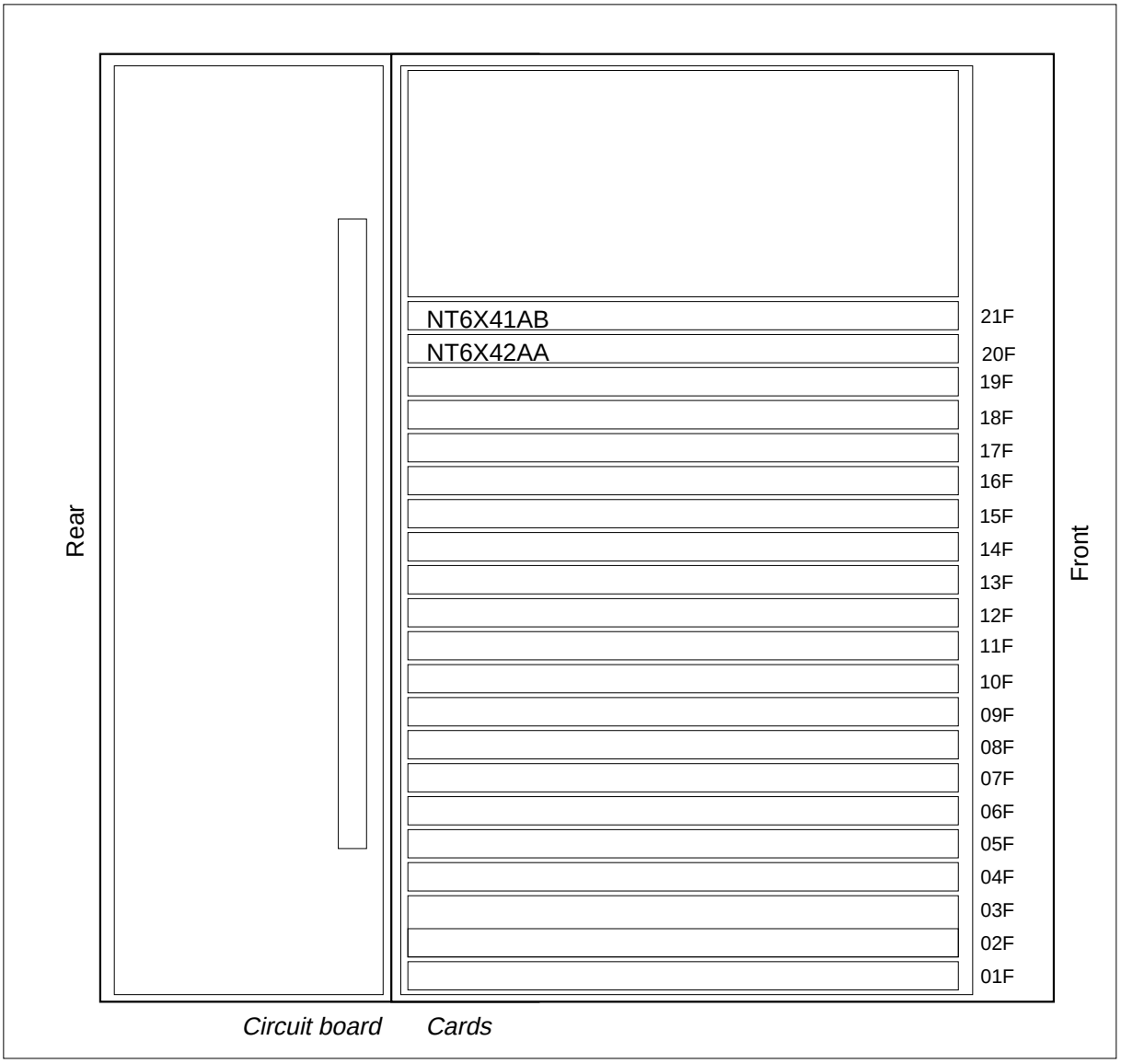
NT6X02UB parts (Sheet 3 of 3)

PEC	Slot	Description
		The NT6X42AA performs the following main functions: • extracts CSM bit from network channels • checks parity on all bytes • inserts a transmit synchronization pattern into the PCM path • counts frame and logic • checks integrity • matches integrity and reports parity errors • synchronizes pattern transmission • provides a signaling processor interface

The parts and the position of the NT6X02UB common CP appear in the following figure.

NT6X02UB (end)

NT6X02UB parts



NT6X03AA

Product description

The NT6X03AA line concentrating equipment (LCE) frame is a single-bay frame. The NT6X03AA contains the following:

- one or two NT6X04AA line concentrating module (LCM) common circuit packs (CP) or NT6X04BA international line concentrating module (ILCM) CPs
- associated frame baffle and fuse panels
- an NT6X35AA frame supervisory panel (FSP)

Each LCM contains two single-shelf line control arrays (LCA). Each LCA includes the bus interface circuit and an LCM drawer. The LCM drawer holds a maximum of 64 line circuit (LC) cards.

There are two LCMs, the LCM-0 and the LCM-1. The LCMs with a common peripheral controller (CPC) function as an interface for a maximum of 640 analog lines. The NT6X03AA uses DS30A links if the LCM is within 15 m (50 ft) of the CPC. The NT6X03AA calls the CPC a remote line concentrating module (RLCM) when the distance between the LCM and the CPC is longer. The distance can reach a maximum of 241 km (150 mi). When the NT6X03AA calls the CPC a RLCM, the NT6X03AA uses DS-1 links.

Parts

The LCE frame has the following parts:

- NT6X04AA–LCM common CP
- NT6X04BA–ILCM common CP
- NT6X35AA–LCE FSP

Line concentrating module common circuit packs

Each of the NT6X04AA LCM CP and the NT6X04BA ILCM CP contains two LCAs, LCA-0 and LCA-1. Each LCA occupies a single unit. Each LCA has a power converter. The power converter supplies the operating voltages for an LCA. One power converter can provide power for both LCAs if one power converter fails. The LCMs support a maximum of 640 plain ordinary telephone service (POTS) lines or digital data units (DDU) in any group. An LCM provides the interface for 2-6 DS30A links (60-180 channels). In remote conditions, the LCM provides the interface for 2-6 DS1 links. The digital path in each CP includes a looparound feature so that the CP can isolate single faults. Fuse and converter-failure alarm outputs are also provided for the associated FSP.

NT6X03AA (continued)

An LCA contains five LCM line drawers (NT6X05AA). Each drawer provides voice and signaling interfaces between 64 two-wire LC cards and two LCM control complexes in an LCA. The drawer also determines when to apply ringing signals to the LC cards. The drawer selects both the ringing and the ANI and coin voltages. The drawer provides digital looparound facilities for the bus interface and LC cards. The LCM also includes a cutover hold relay that allows software to cut over a selected LC.

Above each LCA are the baffle and fuse panels. The baffle and fuse panels circulate air for cooling. The baffle and fuse panels include five +5V and -48V fuse sets and a pair of fuses for the ringing voltage outputs.

Line concentrating equipment frame supervisory panel (LCE FSP)

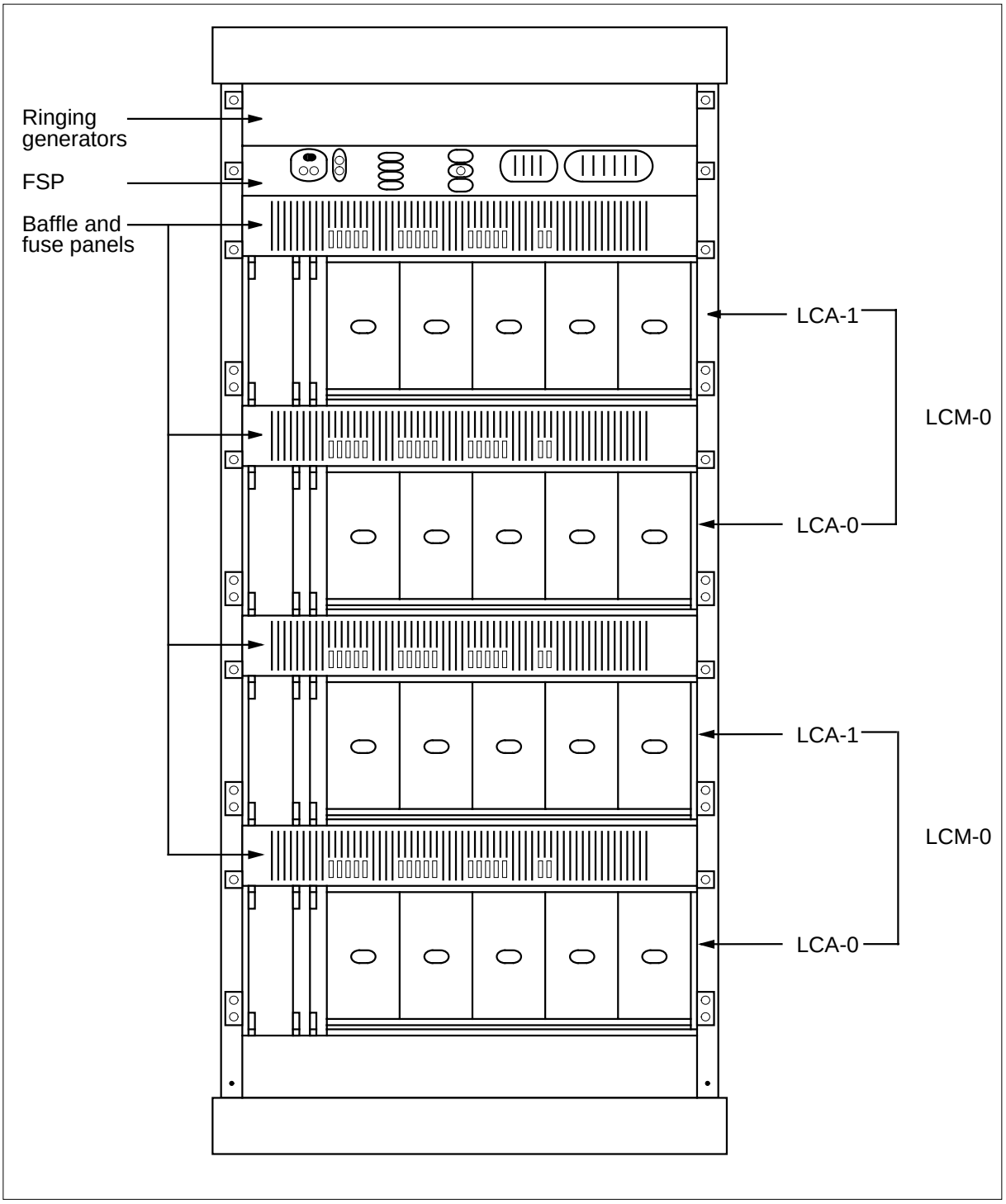
The LCE FSP contains the power control facilities, alarm facilities, and interfaces between the power distribution center (PDC) and the power converters in the LCMs. The FSP also contains two NT6X30AA ringing generators (RG). An RG generates the ringing signals and produces the dc voltages for automatic number identification (ANI) and coin functions in DMS switching system applications. Manually operated programming switches determine the amplitude and frequency of the signals. The LCE FSP sends operational signals to and receives operational signals from the LCMs.

Design

The design of the LCE frame appears in the following figure.

NT6X03AA (end)

NT6X03AA parts



NT6X03CA

Product description

The NT6X03AA line concentrating equipment (LCE) frame is a single bay frame. The NT6X03AA contains the following:

- a maximum of two NT6X04AA line concentrating module (LCM) common circuit packs (CP)
- associated frame baffle and fuse panels
- an NT6X35AA frame supervisory panel (FSP)

Each LCM contains two single-shelf line concentrating arrays (LCA). Each LCA includes the bus interface circuit and an LCM drawer. The LCM drawer holds a maximum of 64 line circuit (LC) cards.

There are two LCMs, the LCM-0 and the LCM-1. The LCMs with a common peripheral controller (CPC), function as an interface for a maximum of 640 analog lines. The NT6X03CA uses DS30A links if the LCM is in 15 m (50 ft) of the CPC. If the LCM is a maximum of 241 km (150 mi) the NT6X03CA calls the CPC a Remote Line Concentrating Module (RLCM). When the NT6X03CA calls the CPC a RLCM, the NT6X03CA uses DS-1 links. The NT6X03CA LCE frame uses a remote control and maintenance equipment (RCME) frame or retrofits to a Remote Switching Center (RSC) configuration to configure in a remote site.

Parts

The NT6X03CA line concentrating equipment frame consists of the following parts:

- NT6X04AA–LCM common CP
- NT6X0401–LCA shelf assembly
- NT6X05AA–line drawer
- NT6X30AA–ringing generator
- NT6X35AA–frame supervisory panel (FSP)

Line concentrating module common circuit pack

The NT6X04AA LCM common CP functions with a CPC as an interface for a maximum of 640 analog lines. Between an LCM and the associated CPC the connections relate to the distance between the two units. If the LCM is in 15 m (50 ft) of the CPC, the NT6X04AA uses DS30A links. The NT6X04AA uses DS-1 links for distances a maximum of 241 km (150 mi).

The LCM contains two single-unit LCAs. The LCA-0 unit is on the bottom and the LCA-1 unit is on the top. One or both of the LCMs are mounted in an

NT6X03AA LCE frame. The NT6X03AA LCE also holds the baffle and fuse panels and an NT6X35AA LCE FSP. For each LCM, the FSP includes two NT6X30AA ringing generators.

Each LCA includes a control complex (CC) that consists of an NT6X51AA LCM processor and NT6X52AA digroup controllers. The CC can handle both LCAs when the following conditions apply.

- an LCM processor or digroup controller in the associated LCA fails
- a message link to the associated LCA fails
- the line group controller (LGC) forces an activity switch

Each LCA can contain a maximum of five LCM drawers. Each drawer contains an interface circuit and a maximum of 64 LC cards. Each LCA also includes an NT6X53AA power converter. The power converter can provide the required operating voltages for both the LCAs in an LCM if the associated converter fails.

The LCM also incorporates looparound features in the digital path of each circuit card. The looparound features can isolate single faults. The LCM also sends fuse and converter failure alarm outputs to the FSP.

Line concentrating array shelf assembly

The NT6X0401 LCA shelf assembly houses five line drawers, a digroup control card, an LCM processor card, and a power converter.

Line drawer

The NT6X05AA line drawer provides signaling and voice interfaces between 64 two-way (4-wire) line circuits and the LCA CC. The LCA CC is in an LCM common CP or an international LCM (ILCM) common CP. The line drawer, is in the LCA shelf of the LCM. The line drawer also controls the application of ringing signals to the LC cards. Each LCA has a maximum of five line drawers. Each line drawer contains an NT6X54AA bus interface card (BIC) and a maximum of 64 line cards. To locate the bus interface card check behind the front panel of the line drawer. Locate the line cards mounted in the four rows behind the BIC.

Ringing generator

The NT6X30AA ringing generator generates ringing signals and dc voltages for automatic number identification (ANI) and coin functions.

Frame supervisory panel

The NT6X35AA FSP contains power control and alarm circuits. The power control and alarm circuits provide interface between the power distribution

NT6X03CA (continued)

center (PDC) and the LCE frame of the DMS-100 Family. For power control to the common peripheral control equipment (CPCE) frame the system requires all of the following:

- four circuit breakers (CB)
- one NT0X91AA converter drive and alarm
- one NT0X91AE converter drive and protection card

Each single bay equipment frame contains one FSP. The FSP monitors office battery and alarm battery supply (ABS) fuses. The FSP also monitors the cooling or inverter units. When a cooling or inverter unit fails, the system uses a variety of indications and alarms to indicate a problem. The signals can include fan fail indications, frame fail indications, and aisle alarm outputs.

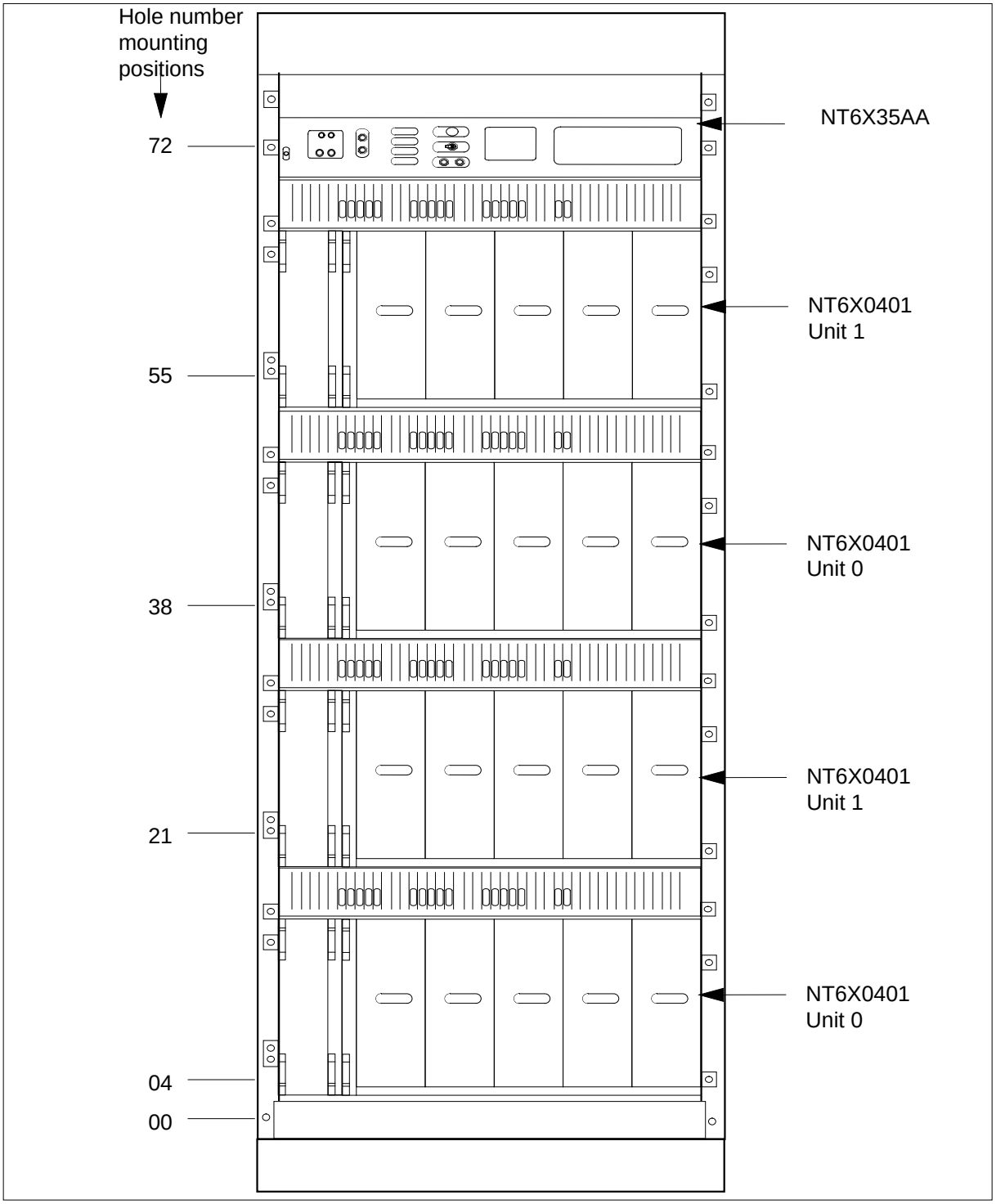
Converter fail lines are connected to the light-emitting diode (LED) indicators on the power converters in the associated frame. Frame fail indications on the FSP front panel and the aisle alarm output, monitor the converter fail lines. The converter fail lines operate an LED indicator on the front panel of the FSP below the associated power feed circuit breaker. The converter fail lines also operate the LED indicator in the shelf power converter.

Located on the front panel the four service jacks provide access. The jacks provide access to two telephone (TEL-A, TEL-B) pairs and two data (DATA-A, DATA-B) pairs. On other frames, with the FSP, the service jacks use connectors on the FSP to provide interframe and interaisle communications. The FSP also features a mechanical interlock. The mechanical interlock is a small cover that allows access to only two of the circuit breakers at a time.

Design

The design of the NT6X03CA appears in the following figure.

NT6X03CA parts



NT6X04AA

Product description

The NT6X04AA line concentrating module (LCM) common circuit pack (CP) works with a common peripheral controller (CPC). The CPC acts as an interface for a maximum of 640 analog lines. The distance between the two units determines the type of connection between the LCM nd the CPC. If the LCM is in 15 m (50 ft) of the CPC, the NT6X04AA uses DS30A links. The NT6X04AA uses DS-1 links for longer distances, to the maximum of 241 km (150 mi).

The LCM comprises two single-unit line concentrating arrays (LCA). The LCAs are designated LCA-0 and LCA-1. The LCA-0 is on the bottom and the LCA-1 is on the top. An NT6X03AA line concentrating equipment (LCE) frame can contain one or two LCMs. The LCE also holds the baffle and fuse panels and an NT6X35AA LCE frame supervisory panel (FSP). The FSP includes two NT6X30AA ringing generators for each LCM.

The LCM contains two LCAs. Each LCA includes a control complex (CC). The CC consists of an NT6X51AA LCM processor and NT6X52AA digroup controllers. The processor and controller can handle both LCAs if one of the following actions occurs:

- the LCM processor or digroup controller in the associated LCA fails
- if a message link to the associated LCA fails
- the line group controller (LGC) forces an activity switch

Each LCA also contains a maximum of five LCM drawers. Each LCM drawer contains an interface circuit and a maximum of 64 line circuit (LC) cards

Each LCA also includes a NT6X53AA power converter. The power converter can provide the operating voltages for both of the LCAs in an LCM when the associated converter fails.

The LCM incorporates looparound features in the digital path of each circuit card. The LCM can use the looparound feature to isolate single faults. The LCM also sends fuse and converter-failure alarm outputs to the FSP.

Parts

The LCM common CP consists of the following parts:

- NT6X05AA–Line drawer
- NT6X51AA–LCM processor

- NT6X52AA–Digroup controller
- NT6X53AA–Power converter

Design

The design of the NT6X04AA appears in the following table.

NT6X04AA parts (Sheet 1 of 2)

Card PEC	Slot	Description
NT6X05AA	6F-20F	*Line drawer* The line drawer provides signaling and voice interfaces between 64 two-wire LC and the two LCA control complexes in an LCM. The drawer also controls the application of ringing signals to the LC cards. Each LCA has a maximum of five line drawers. Each line drawer contains an NT6X54AA bus interface card (BIC) and a maximum of 64 line cards. Locate the BIC behind the front panel of the line drawer. Locate the line cards in the four rows behind the BIC. Use the following line cards in the NT6X05AA line drawer: • NT6X17AA–standard line card type A N • NT6X18AA–standard line card type B without +48 V • T6X18AB–standard line card type B with +48 V • NT6X21AA–standard line card type C • NT6X23AA–power converter(+48 V) • NT6X71AA–standard line card type D

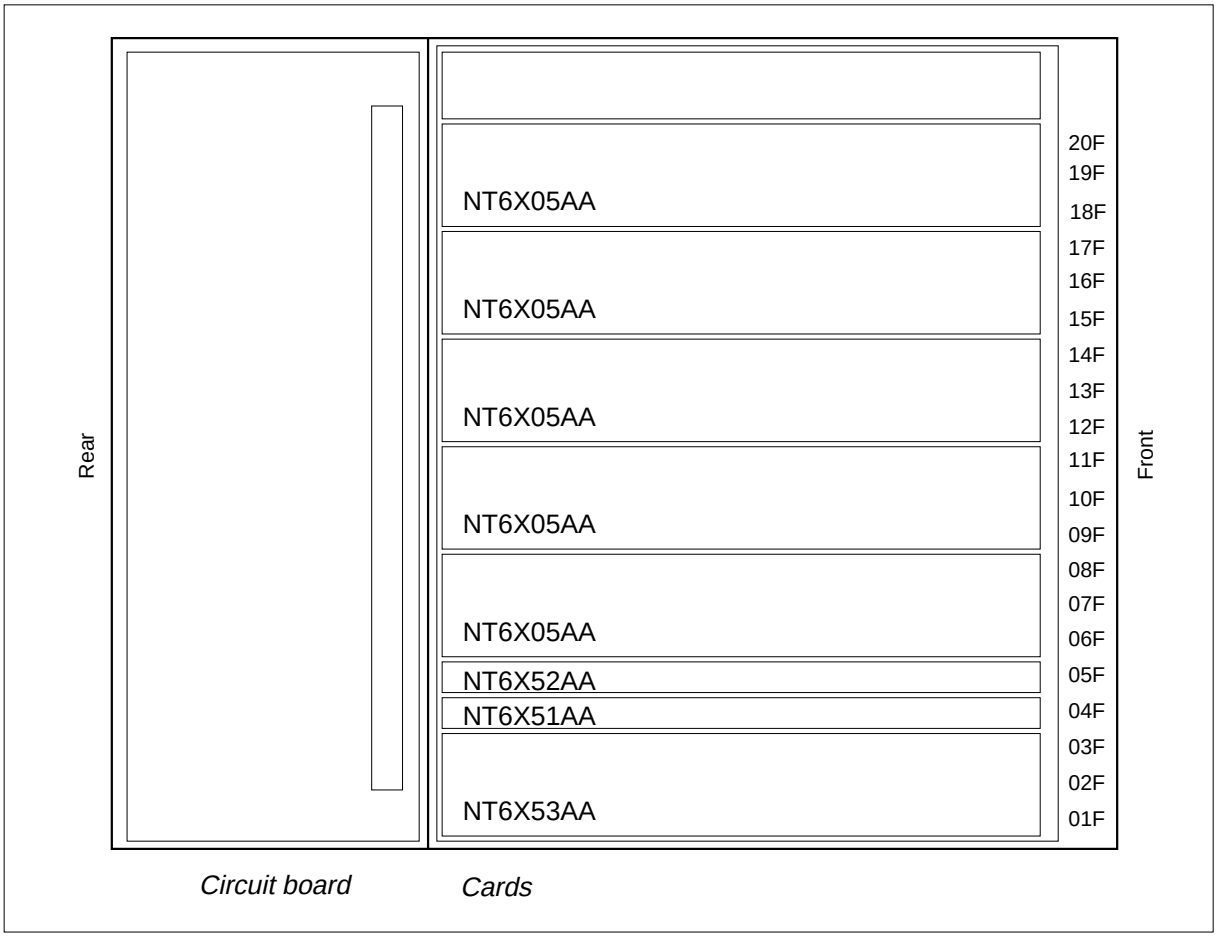
NT6X04AA (continued)

NT6X04AA parts (Sheet 2 of 2)

Card PEC	Slot	Description
NT6X51AA	4F	*Line concentrating module processor* The LCM processor controls the activity of the LCA and functions as the interface between the DS30A links and the digroup controller. The LCM processor also performs the following functions: • sanity checks • collects digits and messaging for a maximum of 640 lines • monitors power and ringing functions • recovers and generates clock signals • provides the DMSX message protocol for the line group controller
NT6X52AA	5F	*Digroup controller* The digroup controller functions as an interface for a maximum of three DS30A links and a maximum of ten LCM drawers. The digroup controller supplies time switching for both external and internal channel assignments. The digroup controller also provides the digital looparound paths used for troubleshooting.
NT6X53AA	1F-3F	*Power converter* The power converter supplies the +5V and +15V dc that the LCA circuits need. The power converter includes relay circuits. The relay circuits apply the ringing, automatic number identification (ANI), and coin voltages to the LCs in the line drawer. The ringing generators in the FSP generate the coin voltages. Each power converter also functions as a backup for the converter in the associated LCA.

The design of the NT6X04AA appears in the following figure.

NT6X04AA parts



NT6X04AB

Product description

The NT6X04AB line concentrating module (LCM) common circuit pack (CP) works with a common peripheral controller (CPC). The LCM acts as an interface to the maximum of 640 analog lines. The distance between the two units determines the type of connection between the LCM and the CPC. If the LCM is in 15 m (50 ft) of the CPC, the NT6X04AB uses DS30A links. The NT6X04AB uses DS1 links for longer distances, to a maximum of 241 km (150 mi).

The LCM contains two single-unit line concentrating arrays (LCA). The LCAs are designated LCA-0 and LCA-1. The LCA-0 is on the bottom and the LCA-1 is on the top. The system can mount one or two LCMs in an NT6X03AA line concentrating equipment (LCE) frame. The LCE also holds the baffle and fuse panels and an NT6X35AA LCE frame supervisory panel (FSP). The FSP includes two NT6X30AA ringing generators for each LCM.

The LCM contains two LCAs. Each LCA includes a control complex (CC). The CC consists of an NT6X51AA LCM processor and NT6X52AA digroup controllers. The processor and controllers can handle both LCAs when one of the following actions occur:

- the LCM processor or digroup controller in the associated LCA fails
- a message link to the associated LCA fails
- the line group controller (LGC) forces an activity switch

Each LCA also contains a maximum of five LCM drawers. Each LCM drawer contains an interface circuit and a maximum of 64 line circuit (LC) cards.

Each LCA includes a NT6X53AA power converter. The power converter can provide the operating voltages for both of the LCAs in an LCM when the associated converter fails.

The LCM incorporates looparound features in the digital path of each circuit card. The LCM can use the looparound features to isolate single faults. The LCM also sends fuse and converter-failure alarm outputs to the FSP.

Parts

The LCM common CP consists of the following parts:

- NT6X05AA–Line drawer (LD)
- NT6X51AA–LCM processor

- NT6X52AA–Digroup controller
- NT6X53AA–Power converter

Design

The design of the NT6X04AB appears in the following table.

NT6X04AB parts (Sheet 1 of 2)

Card PEC	Slot	Description
NT6X05AA	6F-20F	*Line drawer* The LD provides signaling and voice interfaces between 64 two-wire LC and the two LCA control complexes in an LCM. The drawer controls the application of ringing signals to the LC cards. Each LCA has a maximum of five LDs. Each LD contains an NT6X54AA bus interface card (BIC) and a maximum of 64 line cards. Locate the BIC behind the front panel of the LD. In the four rows behind the BIC are the line cards. Use the following line cards in the NT6X05AA LD: • NT6X17AA–standard line card type A • NT6X18AA–standard line card type B without +48 V • NT6X18AB–standard line card type B with +48 V • NT6X21AA–standard line card type C • NT6X23AA–power converter(+48 V) • NT6X71AA–standard line card type D

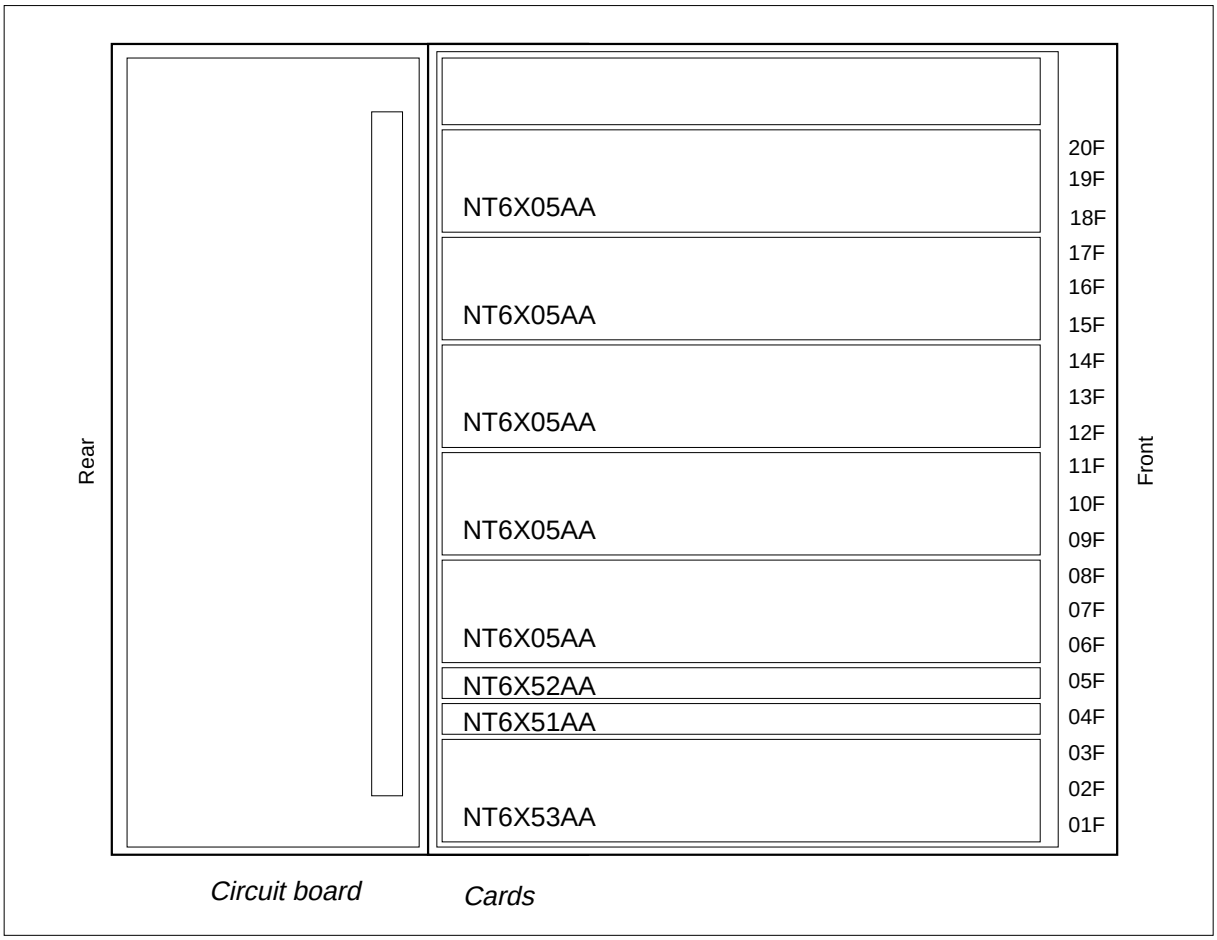
NT6X04AB (continued)

NT6X04AB parts (Sheet 2 of 2)

Card PEC	Slot	Description
NT6X51AA	4F	*Line concentrating module processor* The LCM processor controls the activity of the LCA. The LCM functions as the interface between the DS30A links and the digroup controller. The LCM processor also performs the following functions: • sanity checks • collects digits and messaging for a maximum of 640 lines • monitors power and ringing functions • recovers and generates clock signals • provides the DMSX message protocol for the LGC
NT6X52AA	5F	*Digroup controller* The digroup controller functions as an interface for a maximum of three DS30A links and a maximum of ten LCM drawers. The digroup controller supplies time switching for both external and internal channel assignments. The digroup controller also provides the digital looparound paths used for troubleshooting.
NT6X53AA	1F-3F	*Power converter* The power converter supplies the +5V and +15V dc that the LCA circuits need. The power converter includes relay circuits. The relay circuits apply the ringing, automatic number identification (ANI), and coin voltages to the LCs in the LD. The ringing generators in the FSP generate the coin voltages. Each power converter also functions as a backup for the converter in the associated LCA.

The design of the NT6X04AB appears in the following igure.

NT6X04AB parts



NT6X04BA

Product description

The NT6X04BA international line concentrating module (ILCM) common circuit pack (CP) functions with a common peripheral controller (CPC) as an interface for a maximum of 640 analog lines. The distance between an ILCM and the associated CPC determines the distance between the two units. Use the DS30A links when the ILCM is in 15 m (50 ft) of the CPC. Use the DS-1 links for distances with a maximum of 241 km (150 mi).

The ILCM has two single-unit line concentrating arrays (LCA). The two LCAs are the LCA-0 and the LCA-1. The LCA-0 is on the bottom, and the LCA-1 is on the top. An NT6X03AA international line concentrating equipment (ILCE) frame can have a maximum of two LCMs. The ILCE frame has the required baffle and fuse panels and an NT6X35AA frame supervisory panel (FSP). The FSP includes ringing generators (NT6X30AA) for each ILCM.

Each LCA in the ILCM includes a control complex (CC). The NT6X51AA LCM processor and the NT6X52AB international digroup controller make up the CC. The CC can control the LCAs when the following events occur:

- the line concentrating module (LCM) processor or digroup control card in the associated LCA fails
- a message link to the associated LCA fails
- the line group controller (LGC) forces an activity switch

Each LCA also contains a maximum of five LCM drawers. Each drawer contains an NT6X54AB international bus interface card (BIC) and a maximum of 64 line circuit (LC) cards.

Each LCA has a NT6X53AA power converter. The power converter provides the operating voltages for the LCAs in an ILCM when the companion converter fails.

The ILCM has loopback features in the digital path of each circuit card that can isolate single faults. The FSP receives fuse and converter-failure alarm outputs.

Parts

The ILCM common CP contains the following parts:

- NT6X05BA–International line drawer (LD)
- NT6X51AA–Line concentrating module (LCM) processor

- NT6X52AB–International digroup controller
- NT6X53AA–Power converter

Design

A description of the parts of the NT6X04BA appear in the following table.

NT6X04BA cards (Sheet 1 of 3)

Card PEC	Slot	Description
NT6X05BA	6F-20F	*International line drawer* The international LD provides signaling and voice interfaces. These interfaces occur between 64 two-wire line circuits and the two LCA control complexes in an LCM. The drawer also controls the application of ringing signals to the LC cards. Each LCA contains a maximum of five LDs. Each LD contains an NT6X54BA international BIC and a maximum of 64 line cards. The international BIC is behind the front panel of the LD. The line cards are in four rows behind the international BIC. The NT6X05BA international LD can use the following cards: NT6X93AA–type A line card (Turkey) NT6X94AA–type B line card (Turkey) NT6X95AA–metering tone generator NT6X98AA–scopedial United Kingdom line card The international BIC functions as the interface between the two 32-channel digroups and the 64 LC cards. The international BIC provides the following functions: • multiplexes and demultiplexes the 32-channel PCM link to 32 LC card buses • receives control messages (and responses) and stores the messages until required • watches for changes in the supervision bits of the associated 32 LC cards • writes new information to the internal ring multiplexer.

NT6X04BA (continued)

NT6X04BA cards (Sheet 2 of 3)

Card PEC	Slot	Description
		The PCM channels support looparound and address-read maintenance functions. The control channels provide loop around, activity read, and inhibit map read. A scan test message on the RPCM can test a part of the scan function of the BIC.
NT6X51AA	4F	*Line concentrating module processor* The LCM processor controls the activity of the LCA. The LCM processor provides the interface between the DS30A links and the digroup controller. The LCM processor performs the following functions: • sanity checks • collects digits and messaging for a maximum of 640 lines • monitors power and ringing functions • recovers and generates clock signals • provides the DMSX message protocol for the LGC.
NT6X52AB	5F	*International digroup controller* The international digroup controller provides an interface for a maximum of three DS30A links and a maximum of ten ILCM drawers. The controller supplies time switching for the external and internal channel assignments. The controller provides the digital looparound paths for troubleshooting use.

NT6X04BA (continued)

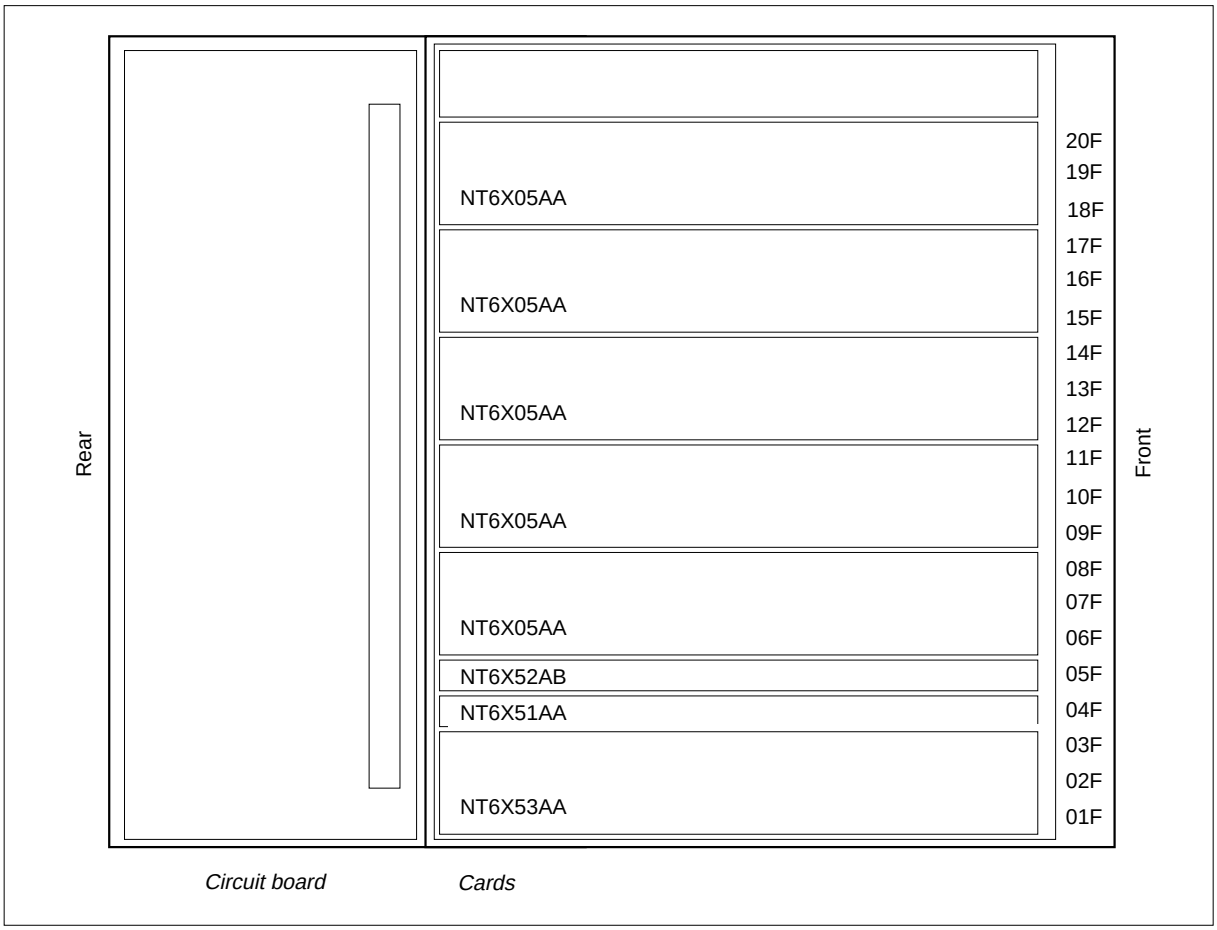
NT6X04BA cards (Sheet 3 of 3)

Card PEC	Slot	Description
NT6X53AA	1F-3F	*Power converter* The power converter supplies the +5V and +15V dc which the circuits in an LCA require. The converter also includes the following: • relay circuits that apply the ringing • automatic number identification (ANI) • coin voltages that the ringing generators generate in the FSP to the LCs in the LD. Each power converter also functions as a backup for the converter in the associated LCA.

The design of the NT6X04BA appears in the following figure.

NT6X04BA (end)

NT6X04BA parts



NT6X04BB

Product description

The NT6X04BB international line concentrating module (ILCM) common circuit pack (CP) functions with a common peripheral controller (CPC) as an interface for a maximum of 640 analog lines. The distance between an ILCM and the associated CPC determines the distance between the two units. Use the DS30A links when the ILCM common CP is in 15 m (50 ft) of the CPC. Use the DS-1 links for distances with a maximum of 241 km (150 mi).

The ILCM common CP has two single-shelf line concentrating arrays (LCA). The two LCAs are the LCA-0 and the LCA-1. The LCA-0 is on the bottom, and the LCA-1 is on the top. An NT6X03AA international line concentrating equipment (ILCE) frame can have a maximum of two LCMs. The ILCE frame has the required baffle and fuse panels and an NT6X35AA frame supervisory panel (FSP). The FSP includes two NT6X30AA ringing generators for each ILCM.

Each LCA in the ILCM common CP includes a control complex (CC). The NT6X51AA LCM processor and the NT6X52AB international digroup controller make up the CC. The CC can control the LCAs when the following events occur:

- the line concentrating module (LCM) processor or digroup control card in the associated LCA fails
- a message link to the associated LCA fails
- the line group controller (LGC) forces an activity switch

Each LCA also contains a maximum of five LCM drawers. Each drawer contains an NT6X54AB international bus interface card (BIC) and a maximum of 64 line circuit (LC) cards. The 64 line circuits are organized in two 32-channel line subgroups (LSG)

Each LCA has a NT6X53AA power converter. The power converter can provide the operating voltages for the LCAs in an ILCM common CP when the companion converter fails.

The ILCM common CP has loopback features in the digital path of each circuit card that can isolate single faults. The FSP receives fuse and converter-failure alarm outputs.

NT6X04BB (continued)

Parts

The ILCM common CP contains the following parts:

- NT6X05BA–International line drawer (LD)
- NT6X51AA–LCM processor
- NT6X52AB–International digroup controller
- NT6X53AA–Power converter

Design

A description of the parts of the NT6X04BA appear in the the following table.

NT6X04BB cards (Sheet 1 of 3)

Card PEC	Slot	Description
NT6X05BA	6F-20F	*International line drawer* The international LD provides signaling and voice interfaces. These interfaces occur between 64 two-wire line circuits and the two LCA control complexes in an LCM. The drawer also controls the application of ringing signals to the LC cards. Each LCA contains a maximum of five LDs. Each LD contains an NT6X54BA international BIC and a maximum of 64 line cards. The international BIC is behind the front panel of the LD. The line cards are in four rows behind the international BIC. The NT6X05BA international LD use the following line cards: NT6X93AA–type A line card (Turkey) NT6X94AA–type B line card (Turkey) NT6X95AA–metering tone generator NT6X98AA–scopedial United Kingdom line card The international BIC functions as the interface between the two 32-channel digroups and the 64 LC cards. The international BIC provides the following functions: • multiplexes and demultiplexes the 32-channel PCM link on to 32 LC card buses • receives control messages (and responses) and stores the messages until required • watches for changes in the supervision bits of the associated 32 LC cards • writes new information to its internal ring multiplexer.

NT6X04BB (continued)

NT6X04BB cards (Sheet 2 of 3)

Card PEC	Slot	Description
		PCM channels support looparound and address-read maintenance functions. The control channels provide looparound, activity read and inhibit map read. A scan test message on the RPCM can test a part of the scan function of the BIC.
NT6X51AA	4F	*Line concentrating module processor* The LCM processor controls the activity of the LCA. The LCM processor provides the interface between the DS30A links and the digroup controller. The LCM also performs the following functions: • sanity checks • collects digits and messaging for a maximum of 640 lines • monitors power and ringing functions • recovers and generates clock signals • provides the DMSX message protocol for the LGC.
NT6X52AB	5F	*International digroup controller* The international digroup controller provides an interface for a maximum of three DS30A links and a maximum of ten ILCM drawers. The controller supplies time switching for the external and internal channel assignments. The controller provides the digital looparound paths used for troubleshooting.

NT6X04BB (continued)

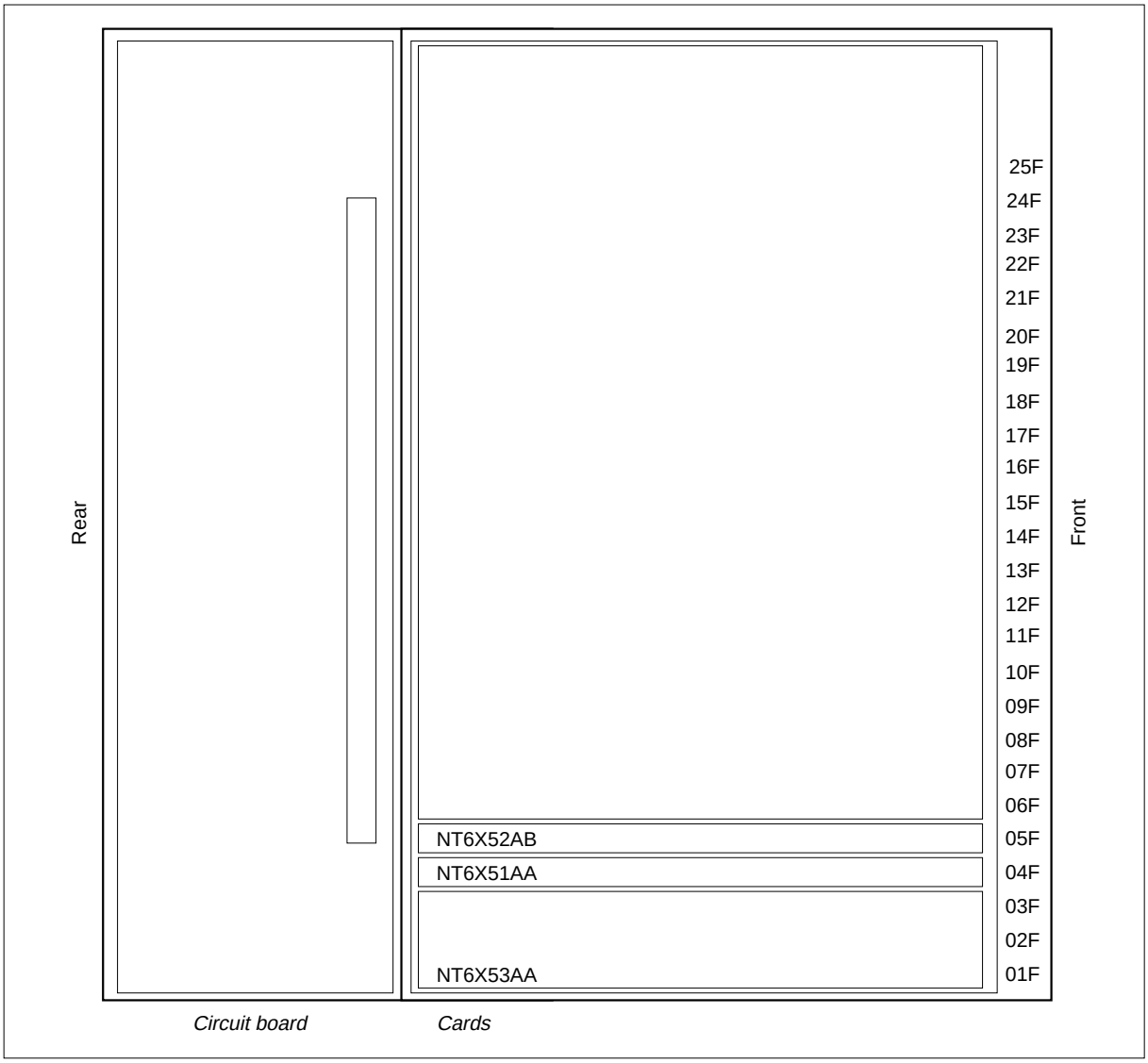
NT6X04BB cards (Sheet 3 of 3)

Card PEC	Slot	Description
NT6X53AA	1F-3F	*Power converter* The power converter supplies the +5V and +15V dc that the circuits in an LCA require. The power converter also includes the following: • relay circuits that apply the ringing, • automatic number identification (ANI) • coin voltages that the ringing generators generate in the FSP to the LCs in the LD. Each power converter also functions as a backup for the converter in the associated LCA.

The design of the NT6X04BB appears in the following figure.

NT6X04BB (end)

NT6X04BB parts



NT6X05AA

Product description

The NT6X05AA line drawer (LD) provides signaling and voice interfaces. These interfaces occur between 64 two-way (four-wire) line circuits (LC) and the line control array (LCA) control complex in a line concentrating module (LCM) common circuit pack (CP) or an international line concentrating module (ILCM) CP. The LD controls the application of ringing signals to the LC cards. The LCA shelf of the LCM contains the LD.

Each LCA has a maximum of five LDs. Each LD contains an NT6X54AA bus interface card (BIC) and a maximum of 64 line cards. The BIC is behind the front panel of the LD. The line cards are four rows behind the BIC.

Parts

The NT6X05AA LD can use the following cards:

- NT6X17AA–Standard line card type A
- NT6X18AA–Standard line card type B without +48 V
- NT6X18AB–Standard line card type B with +48 V
- NT6X21AA–Standard line card type C
- NT6X23AA–Standard line card type B with +48 V
- NT6X54AA–BIC
- NT6X71AA–Data line card

Standard line card type A

The standard line card type A operates with lines that connect to single-line analog telephone sets. This card provides an interface between a two-way analog subscriber line and one channel of the four-wire, 32-channel, 2.56-Mbps data stream. The digital switch uses this data stream. The card occupies one slot in the LD. The card includes a cutover control circuit.

Standard line card type B

The standard line card type B is like the standard line card type A in function. The card type B can also operate with the following:

- analog pay telephone sets that need coin control
- analog single-party, two-party, and multiparty telephone sets.

This card standard provides a voice and signaling interface. The card provides an interface between two-way analog subscriber lines and the four-wire, 32-channel, 2.56-Mbps digital stream. The switching system uses this data stream. This card occupies one slot in the LD.

NT6X05AA (continued)

Standard line card type C

The standard line card type C is a single-slot card. The card operates with electronic multiline telephone sets and operator consoles. The card provides an interface between the two-way analog lines that business sets use and the four-wire, 32-channel, 2.56-Mbps digital stream. The switching system uses the digital stream. The card transmits and receives 10-bit pulse-code-modulated (PCM) samples, control data, or signaling data. The card uses a bidirectional bus to link the business set to the LCM. The control module of the host office controls the card with an enable signal.

Data line card

The data line card provides an interface for lines equipped with DMS data units. The card uses a bidirectional bus and an enable signal to transfer messages between the LCM and a data unit. The card occupies two LC slots in the LD. Clock signals time the data transmission and synchronize the time-compression-multiplexing (TCM) frames for all of the data lines in the LD.

Bus interface card

The BIC provides the interface between the two 32-channel LSGs and the 64 line cards. The BIC performs the following functions:

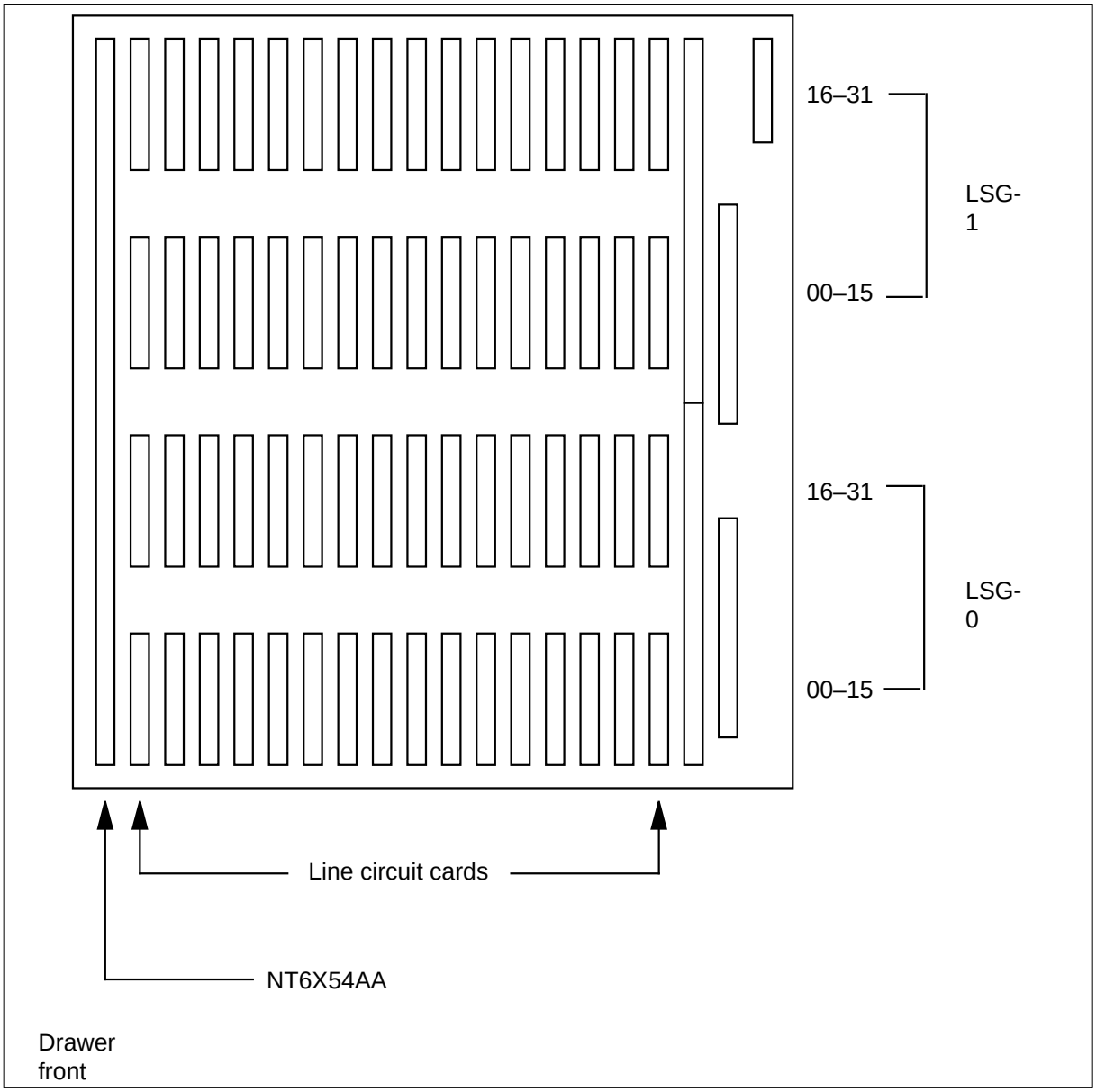
- multiplexes and demultiplexes the 32-channel PCM link on to 32-line card buses
- receives control messages and the responses
- stores the messages
- watches for changes in the supervision bits of the associated 32 line cards
- writes new information to the internal ring multiplexer.

The PCM channels support the looparound and address read maintenance functions. The control channels provide for looparound, activity read and inhibit map read. A scan test message on the RPCM bus can test a part of the scan function of the BIC.

Design

The design of the LD appears in the following figure.

NT6X05AA parts



NT6X05BA

Product description

The NT6X05BA international line drawer (LD) provides signaling and voice interfaces. These interfaces occur between 64 two-way (four-wire) line circuits (LC) and the line control array (LCA) control complex in a line concentrating module (LCM) common circuit pack (CP) or an international line concentrating module (ILCM) CP. The international LD controls the application of ringing signals to the LC cards. The LCA shelf of the LCM contains the international LD.

Each LCA has a maximum of five LDs. Each LD contains an NT6X54AA bus interface card (BIC) and a maximum of 64 line cards. The BIC is behind the front panel of the LD. The line cards are four rows behind the BIC.

Parts

The NT6X05BA LD can use the following cards:

- NT6X54BA–International BIC
- NT6X93AA–Line card Type A (Turkey)
- NT6X94AA–Line card Type B (Turkey)
- NT6X95AA–Metering tone generator
- NT6X98AA–Scopedial United Kingdom line card CP

International bus interface card

The NT6X05BA international BIC provides the interface between the two 32-channel digroups and the 64 LC cards. This card performs the following functions:

- multiplexes and demultiplexes the 32-channel pulse-code-modulation (PCM) link to 32 LC card buses
- receives and stores control messages (and the responses)
- watches for changes in the supervision bits of the associated 32 LC cards
- writes new information to the internal ring multiplexer.

The PCM channels support the looparound and address read maintenance functions. The control channels provide the looparound, activity read and inhibit map-read. A scan test message on the receive PCM (RPCM) bus can test a part of the scan function of the international BIC.

Line card type A (Turkey)

The line card type A (Turkey) provides a voice and signaling interface. This interface occurs between a two-wire analog subscriber line and a channel of

the four-wire, 32-channel, 2.56-Mbps digital link to the switching system. The design of the transmission circuits of this card can satisfy different international requirements. Changes to the values of certain parts of the card can accomplish this function.

This card has dial-pulse or Digitone operation. This card includes protection against lightning surges, short circuits and power line induction. The card also provides the following functions:

- programmable loss control in the digital-to-analog portion of the interface
- software-controlled cut off
- synchronous ring relay operation to minimize transients
- digital and analog looparound circuits for troubleshooting and maintenance
- monitors the line current for signaling and supervision functions

Line card type B (Turkey)

The line card type B (Turkey) is a voice and signaling interface. This interface occurs between a two-wire analog subscriber line and the four-wire, 32-channel, 2.56-Mbps digital stream. The switching system uses this digital stream. The card functions like the type A line card. The card type B can also operate with the following:

- interfaces for PBX and coin subscribers
- loop reversal for coin control
- a 12-KHz pulse for coin control and metering at the subscriber location.

Metering tone generator

The metering tone generator generates the sinusoidal tones that the type B line card requires. The card uses transistor-transistor logic (TTL) circuits to generate square waves and filter the square waves. This event occurs to produce the sinusoidal tones. The card includes monitor circuits that make sure that the tone is present and conforms to specifications.

Scopedial United Kingdom line card circuit pack

The scopedial United Kingdom line card CP provides a voice and signaling interface. This interface occurs between a two-wire analog subscriber and the four-wire, 32-channel, 2.56-Mbps stream. The switching system uses this stream. The card provides the following functions:

- dial-pulse and Digitone operation
- programmable receive loss control in the digital-to-analog direction

NT6X05BA (continued)

- switch-selectable loss control in the analog-to-digital direction
- software-controlled cut off
- synchronous ring relay operation to minimize transients.

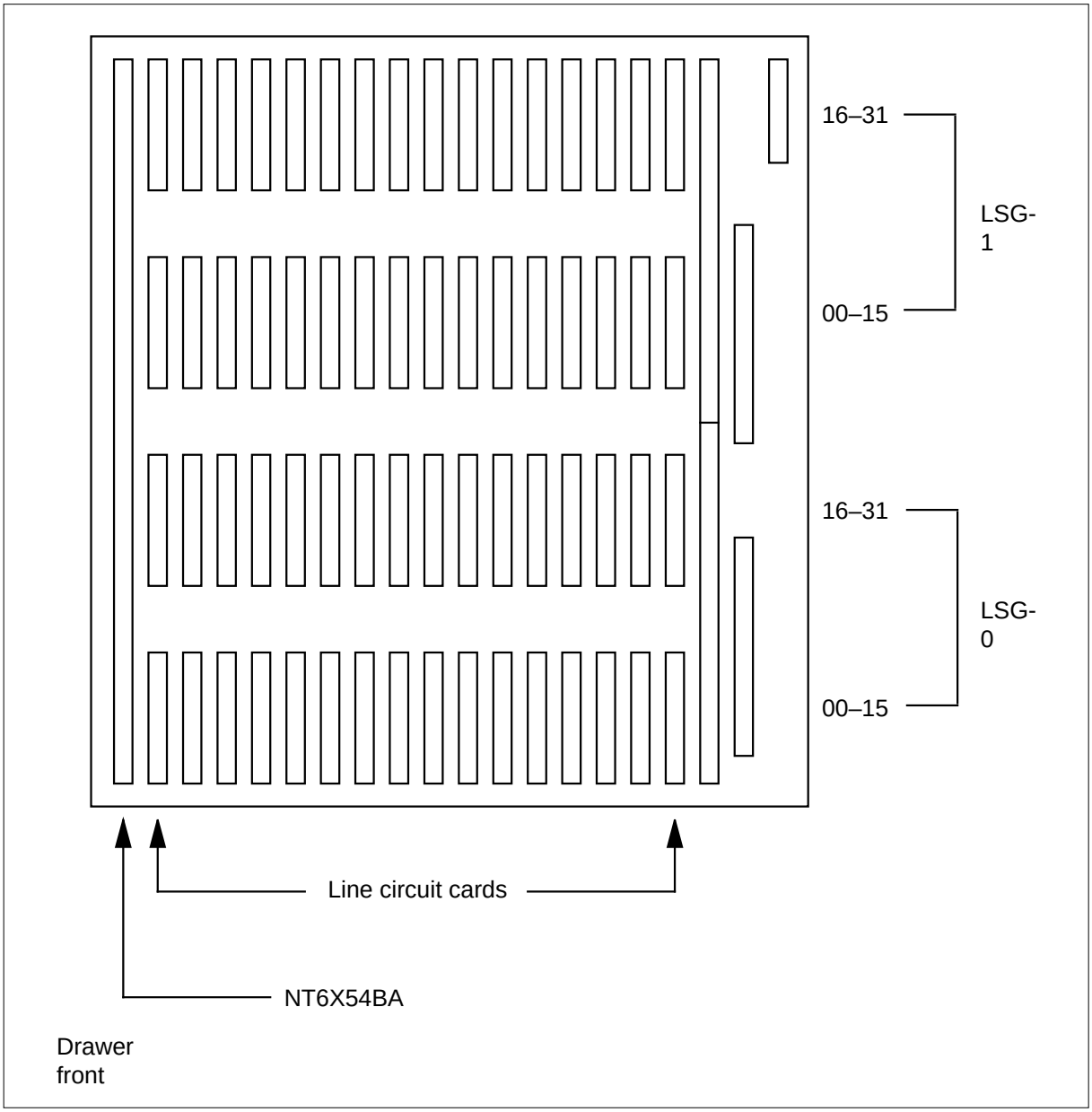
The CP has circuits that monitor the line current for the following reasons:

- signaling and supervision functions
- protection against lightning strikes
- protection against short circuits
- protection against power line induction

Design

The design of the international LD appears in the following figure.

NT6X05BA parts



NT6X05CA

Product description

The NT6X05CA pulse code modulation-30 (PCM-30) line drawer provides signaling and voice interfaces. These interfaces occur for two PCM-30 links from a type 1 line multiplexor (LMUX). The PCM-30 line drawer contains one PCM-30 interface card and one PCM-30 bus interface card. One line concentrating array (LCA) shelf can contain a maximum of five PCM-30 line drawers. Two LCAs make up a line concentrating module (LCM).

Each LCA has a maximum of five line drawers. Each line drawer contains an NT6X54CA PCM-30 line drawer bus interface card (BIC) and a maximum of 64 line cards. The bus interface card is behind the front panel of the line drawer. The line cards are in four rows behind the BIC.

Parts

The NT6X05CA PCM-30 line drawer has the following parts:

- NT6X0505–line drawer assembly
- NT6X27CA–PCM-30 interface card
- NT6X54CA–PCM-30 line drawer BIC

Design

The parts of the NT6X05CA appear in the following table.

NT6X05CA cards (Sheet 1 of 2)

Card PEC	Slot	Description
NT6X0505	–	*Line drawer assembly* The NT6X0505 line drawer assembly contains a PCM-30 interface card, a PCM-30 bus interface card and a maximum of 64 line cards.

NT6X05CA (continued)

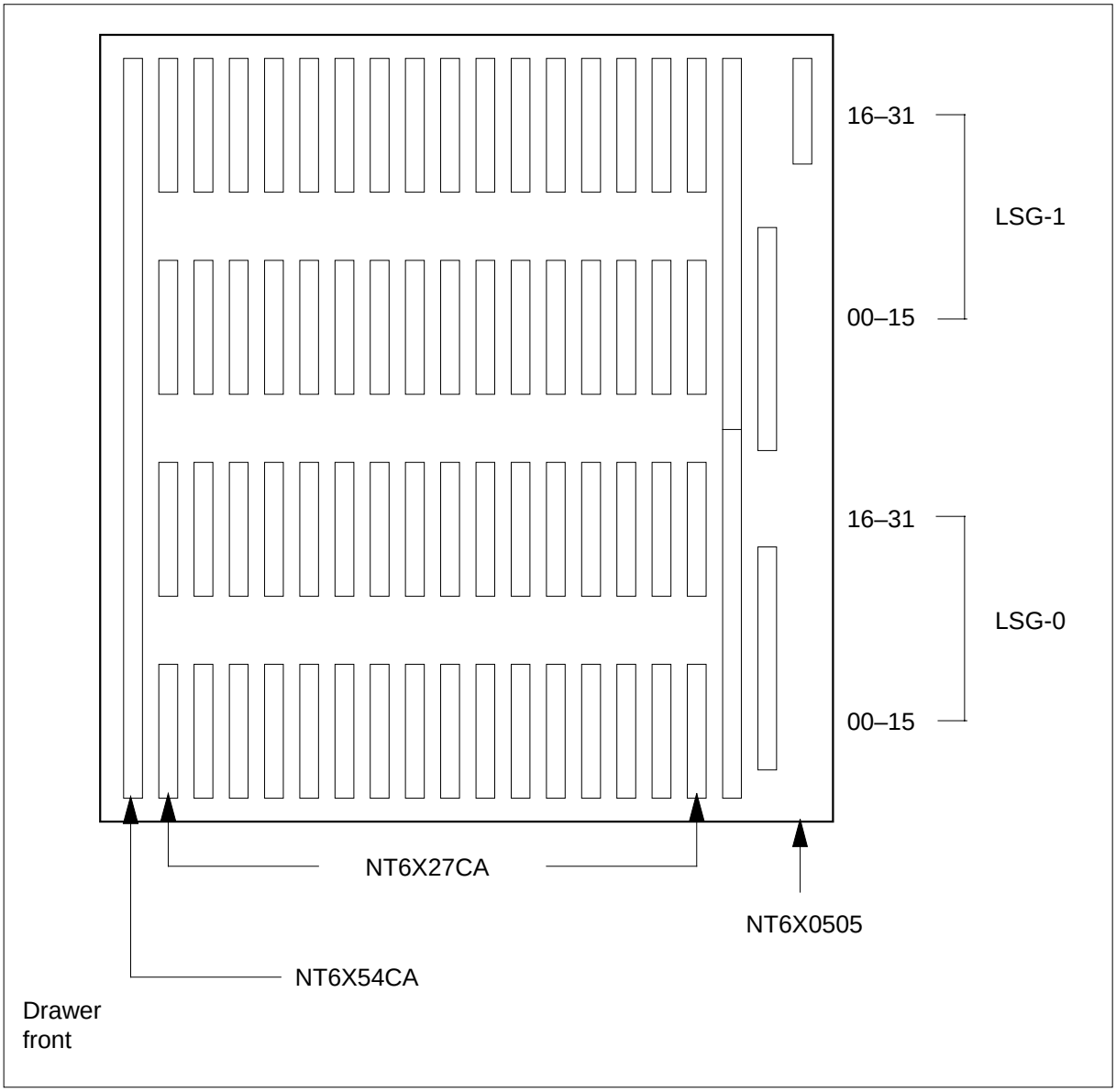
NT6X05CA cards (Sheet 2 of 2)

Card PEC	Slot	Description
NT6X27CA	–	*PCM-30 interface card* The PCM-30 interface card provides an interface between an NT6X02 common peripheral controller (CPC) and European-standard PCM-30 trunk transmission equipment. The PCM-30 interface card translates PCM voice signals and signaling data. The card translates between two 32-channel, 2.048-Mbit/s external PCM-30 trunk circuits and one 64-channel, 5.12 Mbit/s duplicated port in the CPC. The card receives data streams from the 4-wire PCM trunk transmission equipment. The card converts the high-density bipolar 3 (HDB3) data to a DS30 format for transmission to the DS60 time switch card. The card receives PCM-30 data from the time switch card. The card converts the data to an HDB3 format for transmission to the trunk transmission equipment. The card provides a looparound function for tests.
NT6X54CA	32F	*PCM -30 line drawer bus interface card* The BIC functions as the interface between the two 32-channel line subgroups and the 64 line cards. The BIC also performs the following functions: • multiplexes and demultiplexes the 32-channel PCM link onto 32 line card buses • receives and stores control messages and the responses • stores the messages until required • watches for changes in the supervision bits of the associated 32 line cards • writes new information to its internal ring multiplexer. The PCM channels support looparound and address-read maintenance functions. The control channels provide looparound, activity read, and inhibit map read. A scan test message on the RPCM bus can test a part of the BIC scan function.

The design of the appears in the followinf figure.

NT6X05CA (end)

NT6X05CA parts



Note: This illustration is not to scale.

NT6X06AC

Product description

The NT6X06AC message switching 6 equipment frame (MS6E) contains DMS Common Channel Interoffice Signaling (CCIS) hardware. The NT6X06AC also contains DMS CCITT Specifications of Signaling Number 6 (CCITT6) hardware for the DMS-300 application.

The MS6E has a message switch and buffer 6 (MSB6), signaling terminals (ST), modems and inverter units.

The STs and associated modems form two groups of eight. The MSB6 can communicate with the digital trunk controllers (DTC) through a maximum of eight network ports per plane allows the MSB6. The MSB6 switches signaling messages between the STs and the CCIS or CCITT6 trunks on the DTCs. The MSB6 uses the inter-peripheral message links (IMPL)–nailed-up connections through the network switch signalling messages. The ST provides the interface between the DMS and the signaling network.

Parts

The NT6X06AC has the following parts:

- A0367433–LaMarche inverter (provisionable)
- NT0X28AN–Frame supervisory panel (FSP)
- NT0X87AA–Inverter (provisionable)
- NT3X90AC–DC cooling unit (CU)
- NT5X08AC–Data set module
- NT6X07AB or NT6X07AC–MSB6 circuit packs (CP)

LaMarche inverter (provisionable)

Installations in the U.S. normally use two A0367433 LaMarche inverter units. The inverter units are in the NT606AC frame at shelf positions 03 and 11.

Each A0367433 inverter has an output capacity of 500 W. The A0367433 inverter converts the -48V (nominal) dc from the office battery to 110V ac. This action provides ac power to the modems on the NT5X08AC shelf. The NT5X08AC shelf is in position 19 in the frame.

Frame supervisory panel

The NT0X28AN FSP contains an NT0X91AE converter drive and protection circuit. This FSP also contains an NT0X91AA alarm and converter drive circuit. The converter drive circuit monitors and controls the power supply to

NT6X06AC (continued)

the MS6E. The power supply is from the power distribution center (PDC) in the DMS-100 system.

The NT0X28AN FSP uses four power feeds to carry the potential from the office battery, which is -48V nominal. The NT0X28AN FSP uses four circuit breakers to protect the power control and alarm circuits to the shelves in the MS6E. This set up is in contrast to some NT0X28 models that use fuses to protect the power control. This set up also contrasts some models that require two or three power feeds.

The NT0X28AN has a mechanical interlock feature. This feature contains a small sliding cover that allows access to only two circuit breakers at a time. The two circuit breakers are: CB1 and CB2, or CB4 and CB5. When all four circuit breakers are ON, the feature does not allow circuit breaker tripping in the groups.

Each pair of CBs serves an NT6X07AB/AC shelf. The CB1 and CB2 serve shelf 65. The CB4 and CB5 serve shelf 51.

Inverter

Canadian installations require two NT0X87AA inverter units. The units are in shelf positions 04 and 11 in the NT6X06AC frame.

Each NT0X87AA inverter converts -48V (nominal) input dc to 117-V, 60-Hz ac output to supply the modems in the MSE6.

The PDC supplies -48V dc input voltage.

DC cooling unit

The NT3X90AC dc cooling unit has five-fan assemblies that maintain a normal five-shelf cabinet. The fans are dc-powered at 48 V from two feeders in the PDC, fused at 5 A each.

The NT3X90AC cooling unit uses a single-fan failure detection and signaling system. The multiple-fan design has some redundancy. This redundancy allows for a single-fan failure without critical loss of cooling air.

Data set module

The NT5X08AC data set module in the frame contains A0302338 rack mounted data set modems. This data set module is also known as the ac modem shelf. The modems operate in pairs according to office requirements.

The NT6X06A frame in slots 01 and 09 in the NT5X08AC shelf contains a minimum of two A0302338 modem cards. The NT5X08AC is in shelf position 19 in the frame.

Each modem card corresponds to an NT6X65AA CCIS ST card. The A0302338 and NT6X65AA cards form a signaling link. A pair of signaling links is a signaling layer.

Message switching buffer 6 common circuit packs

The NT6X07AB or NT6X07AC message switching buffer 6 (MSB6) is the MSB type that starts procedures CCIS6 and CCITT6. This event occurs to perform the following signaling functions:

- provides and maintains a signaling path between the CCIS6/CCITT6 transmission link and the CCIS signaling terminal controllers (STC)
- performs message switching and distribution functions. These functions are between the DTC and the associated STC. The DTC handles the voice part of a call. The STC handles the signaling part of the same call.

The MSB6 has duplicates of all MSB6 contents. The duplicates increase the reliability of the system. The NT6X07AB/AC shelf can handle the complete load of the frame. One NT6X07AB/AC shelf is active, while the other shelf is inactive. The pair of MSB6 shelves makes up a single message switching buffer module 6.

In this duplication design, each NT6X65AA CCIS ST card has another card on the next MSB6 shelf. Each shelf receives power from a different power feed (A or B) to increase the reliability of the system.

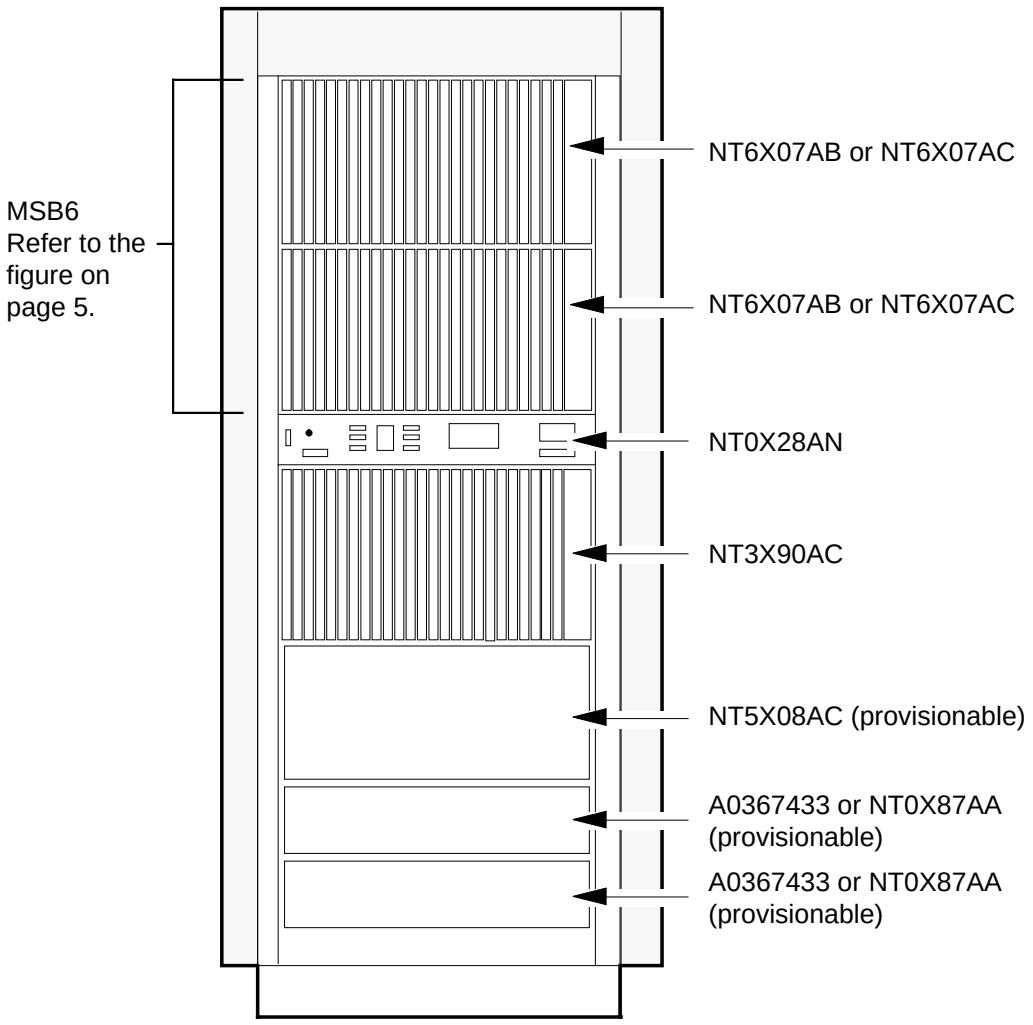
Each NT6X65AA card has a A0302338 modem card. The two NT6X65AA-A0302338 groups form a signaling layer.

Design

The design of the NT6X06AC appears in the following figure.

NT6X06AC (continued)

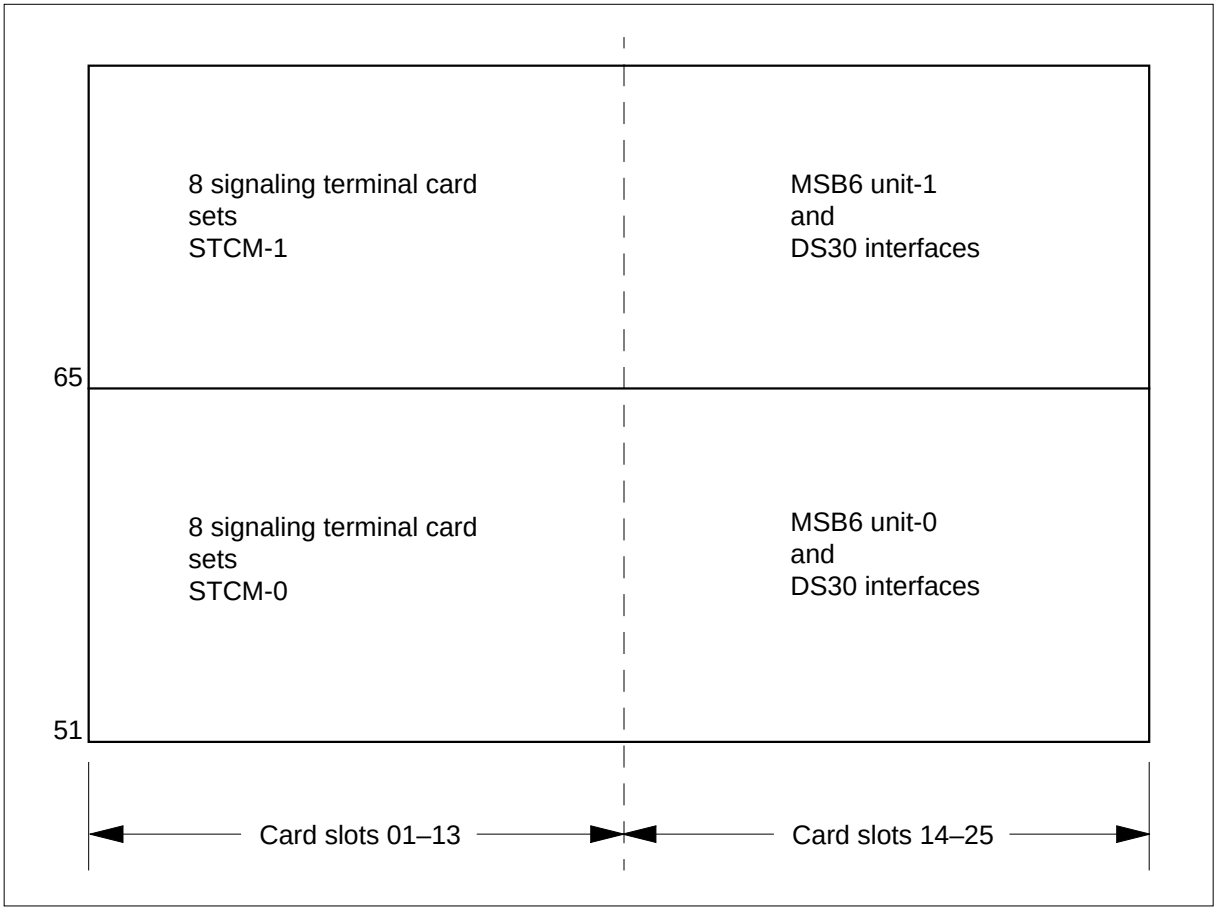
NT6X06AC card



Note: This illustration is not in scale.

A detailed view at the top two shelves of the NT6X06AC appears in the following figure.

NT6X07AB/AC design



NT6X07AB

Description

The message switch and buffer 6 (MSB6) provides and maintains a path. The path starts at the Common Channel Interoffice Signaling (CCIS)/CCITT Signaling Number 6 (CCITT6) digital signaling link. The link is switched through the network and the path ends at the CCIS6/CCITT6 signaling terminal (ST).

The NT6X07AB performs the message switching and distribution functions between the digital trunk controllers (DTC) and the correct STs.

Parts

The NT6X07AB contains of the following components:

- NT2X70AD–Power converter, &0xb1;5V/+12V circuit pack (CP)
- NT6X40AA–DS30 network interface (NI) CP
- NT6X41AA–Speech bus formatter CP
- NT6X42AA–Channel supervision message (CSM) CP
- NT6X43AA–Message interface CP
- NT6X45AC–Line group controller (LGC)/DTC processor CP
- NT6X46AB–Signal processor memory (SPM) CP
- NT6X47AB–Master processor memory (MPM) CP
- NT6X65AA–CCIS ST CP
- NT6X67AA–ST buffer CP
- NT6X68AA–ST interface CP

Design

The following table describes the components of the NT6X07AB shelf.

NT6X07AB parts (Sheet 1 of 4)

PEC	Slot	Description
NT0X50AA	16F, 4-10F *(as needed)*	*Filler faceplate .875* The NT0X50AA fills in the free card slot 16, and slots 4-10 as needed.
NT2X70AD	1F, 25F	*Power converter,*&0xb1;*5V/+12V circuit pack* The NT2X70AD provides a regulated potential of +5V and +12V to the circuit cards on the MSB6 shelf that require the potential. The office battery provides a small -48V input.
NT6X40AA	23F-24F	*DS30 network interface circuit pack* The NT6X40AA provides a DS30 interface to the network.
NT6X41AA	22F	*Speech bus formatter* The speech bus formatter contains of two sections: The formatting section handles 16 DS30 ports in both directions and features: • parallel-to-serial conversion of the transmit pulse code modulation (XPCM) data • serial-to-parallel conversion of the receive pulse code modulation (RPCM) data • network plane selection • CSM loop around • parity error generation • raw T1 clock generation The clock section generates the 10.24 MHz shelf clock and a number of other signals different other parts of the shelf use. These signals include FP, FP40, and FP48.

NT6X07AB (continued)

NT6X07AB parts (Sheet 2 of 4)

PEC	Slot	Description
NT6X42AA	21F	*Channel supervision message circuit pack* The NT6X42AA performs all of the functions CSM requires between peripherals. The NT6X42AA can accommodate 16 network ports or 512 channels. A channel connection between two peripherals establishes a duplex path that transmits a 10-bit byte in each direction every frame time. The parity bit maintains odd parity for all transmitted bytes. Main functions of the NT6X42AA include: • CSM bit extraction from network channels • parity checking on all bytes, and insertion of a transmit sync pattern and a CSM into the CSM path • frame and logic counting • call data block (CDB) and expected integrity checking • integrity match (IM) and parity error reporting • sync pattern transmission • provision of a signaling processor (SP) interface
NT6X43AA	20F	*Message interface circuit pack* The NT6X43AA provides an interface to receive and transmit messages to network modules. The NT6X43AA provides: • a channel 0 message for call processing software messages • a memory map of all bytes received or transmitted that allows DTC messaging in the speech channels • a 125 ms frame rate interrupt for message timing

NT6X07AB (continued)

NT6X07AB parts (Sheet 3 of 4)

PEC	Slot	Description
NT6X45AC	15F, 19F	*LGC/DTC processor circuit pack* The NT6X45AC provides a 68000-based microprocessor and related circuits to handle the processing tasks within the MSB6. Along with the 68000 Motorola CPU, the NT6X45AC contains four other functional circuit blocks. These circuit blocks are: • memory management unit • sanity and clock control • A-Bus interface • on-board input/output facilities
NT6X46AB	18F	*Signal processor memory circuit pack* The NT6X46AB contains 256 Kbytes of memory and direct memory access the SP card requires.
NT6X47AB	17F	*Master processor memory circuit pack* The NT6X47AB provides RAM for use by the master processor.
NT6X65AA	11F, Provisionable: 4F-10F	*CCIS signaling terminal circuit pack* The NT6X65AA transmits and receives signaling data between a DMS-100 switch and the CCIS and CCITT6 transmission links. The NT6X65AA performs the following main functions: • parallel-to-serial data conversion on messages from the MSB6 • serial-to-parallel data conversion on messages from the transmission link modem • error checking on messages between the MSB6 and the transmission link modem

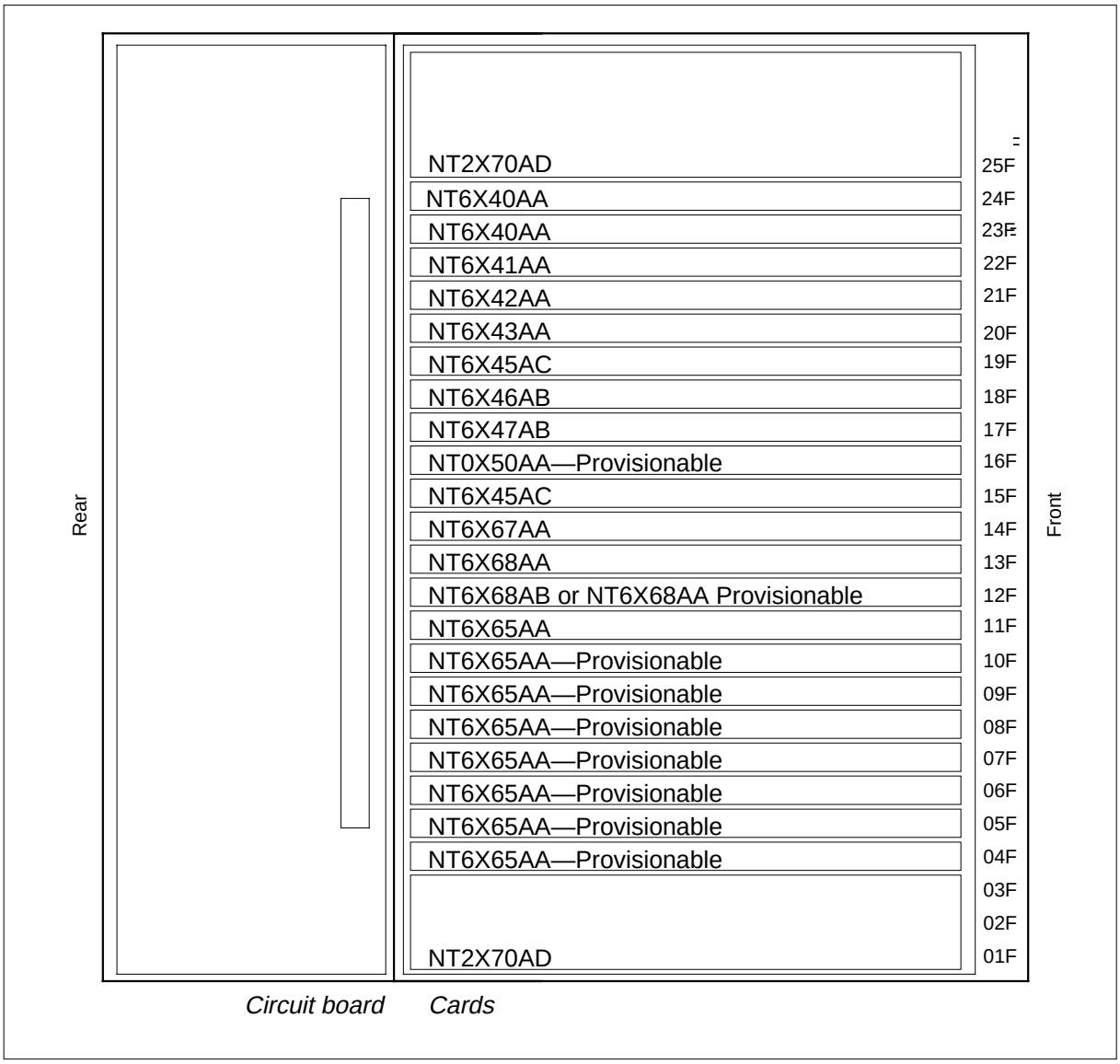
NT6X07AB (continued)

NT6X07AB parts (Sheet 4 of 4)

PEC	Slot	Description
NT6X67AA	14F	*Signaling terminal buffer circuit pack* The NT6X67AA generates and checks parity on data transmitted between the MSB6 and the ST controller (STC).
NT6X68AA	13F, Provisionable: 12F	*Signaling terminal interface circuit pack* The NT6X68AA provides latches for address, data, and control lines to the STC for fault diagnosis and maintenance.

The design of the NT6X07AB appears in the following figure.

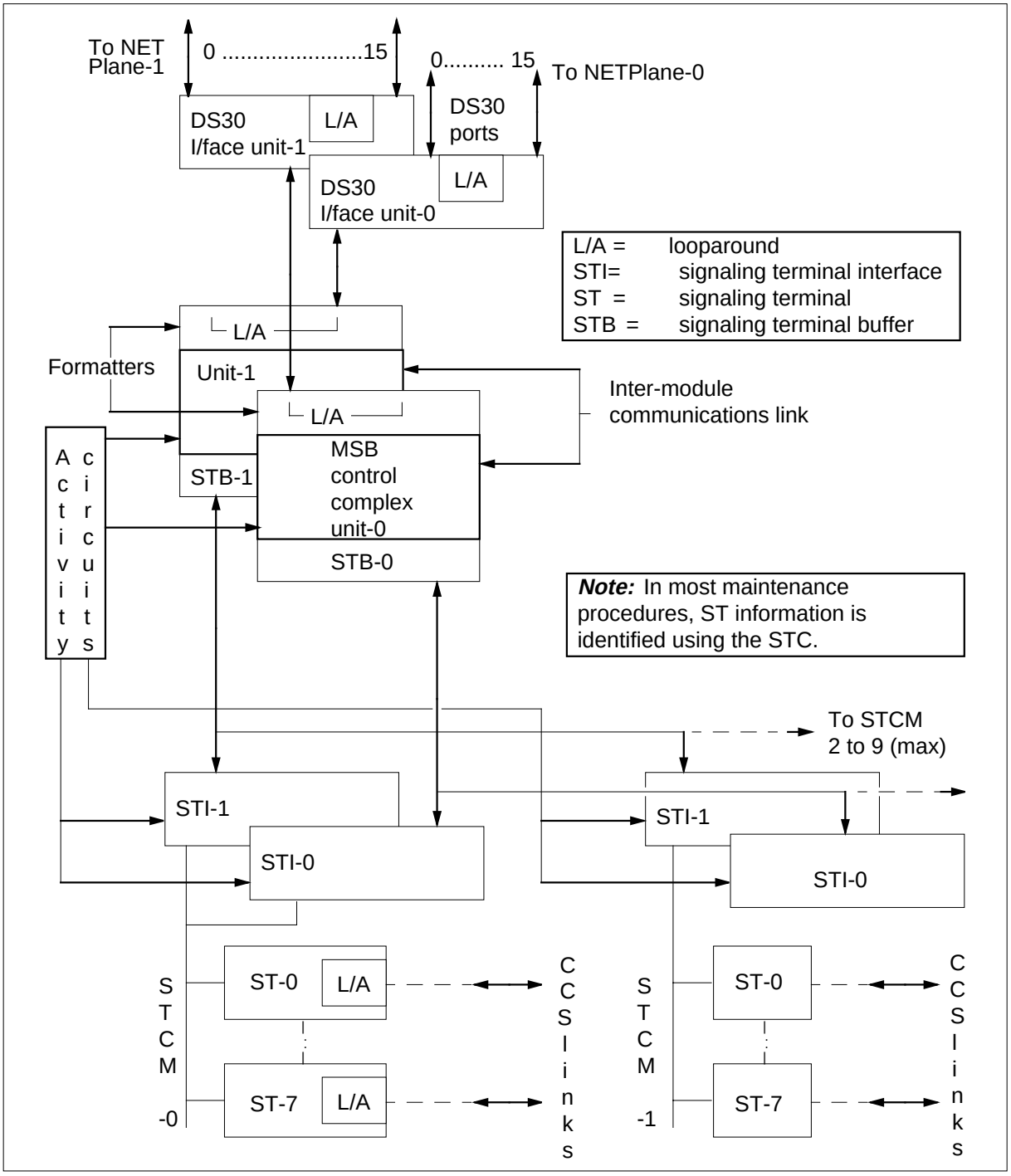
NT6X07AB design



The data flow in the NT6X07AB appears in the following figure.

NT6X07AB (end)

NT6X07AB simplified block diagram



NT6X07AC

Product description

The NT6X07AC message switching buffer 6 module (MSB6) consists of paired, matching shelves in the NT6X06AC frame.

The NT6X07AC provides and maintains a path from the Common Channel Interoffice Signaling (CCIS)/CCITT Signaling Number 6 (CCITT6) digital signaling link. The link is switched through the network and the path ends to the CCIS6/CCITT6 signaling terminal (ST).

The NT6X07AC performs the message switching and distribution functions between the digital trunk controllers (DTC) and some STs.

Parts

The NT6X07AC contains the following parts:

- NT2X70AE–Power converter
- NT6X40AA–DS-30 network interface (NI)
- NT6X41AA–Speech bus formatter circuit card (CP)
- NT6X42AA–Channel supervision message (CSM) CP
- NT6X43AA–Message interface CP
- NT6X45AC–Line group controller/digital trunk controller (LGC/DTC) processor CP
- NT6X46AB–Signal processor memory (SPM) CP
- NT6X47AB–Master processor memory (MPM) CP
- NT6X65AA–CCIS signaling terminal CP
- NT6X67AA–Signaling terminal buffer CP
- NT6X68AA–Signaling terminal interface CP

NT6X07AC (continued)

Design

The parts of the NT6X07AC appear in the following table.

NT6X07AC cards (Sheet 1 of 4)

Card PEC	Slot	Description
NT0X50AA	16F, 4-10F *(as needed)*	*Filler faceplate .875* The NT0X50AA filler face plate fills the unused used card slot 16 and slots 4-10 as required.
NT2X70AE	1F, 25F	*Power converter,±5V/12-V, 50-A CP* The NT2X70AE power converter provides a regulated potential of +5 V, -5 V, +12 V, and -12 V at 50 amps. The NT2X70AE provides the potential to the circuit cards on the MSB6 shelf as required. The office battery provides a nominal input of -48V input.
NT6X40AA	23F-24F	*DS-30 network interface CP* The NT6X40AA card provides a DS-30 interface to the network.
NT6X41AA	22F	*Speech bus formatter* The speech bus formatter has two sections: The formatting section handles 16 DS30 ports in both directions and features: • parallel-to-serial conversion of the transmit pulse code modulation (XPCM) data • serial-to-parallel conversion of the receive pulse code modulation (RPCM) data • network plane selection • CSM loop around • parity error generation • raw T1 clock generation Clock section generates the 10.24-MHz shelf clock and other signals that different parts of the shelf use. Examples of these signals are FP, FP40, and FP48

NT6X07AC cards (Sheet 2 of 4)

Card PEC	Slot	Description
NT6X42AA	21F	*Channel supervision message CP* The NT6X42AA performs all of the functions that channel supervision messaging between peripherals requires. The NT6X42AA can accommodate 16 network ports or 512 channels. Any channel connection between two peripherals establishes a duplex path that transmits a 10-bit byte in each direction every frame time. The parity bit maintains odd parity for all transmitted bytes. The NT6X42AA provides the following functions: • CSM bit extraction from network channels • parity checking on all bytes, and insertion of a transmit synchronization pattern and a CSM into the CSM path • frame and logic counting • call data block (CDB) and expected integrity checking • integrity match (IM) and parity error reporting • sync pattern transmission • provides a signaling processor (SP) interface
NT6X43AA	20F	*Message interface CP* The NT6X43AA provides an interface to receive and transmit messages to network modules. The NT6X43AA provides the following functions: • a channel 0 message interface for call processing software messages • a memory map of all bytes received or transmitted during DTC messaging in the speech channels • a 125 ms frame rate interrupt for message timing

NT6X07AC (continued)

NT6X07AC cards (Sheet 3 of 4)

Card PEC	Slot	Description
NT6X45AC	15F, 19F	*LGC/DTC processor CP* The NT6X45AC provides a 68000-based microprocessor and related circuits to handle processing tasks in the MSB6. The NT6X45AC contains the following functional circuit blocks: • the 68000 Motorola CPU • memory management unit • sanity and clock control • A-bus interface • on-board input/output (I/O) facilities
NT6X46AB	18F	*Signal processor memory CP* The NT6X46AB contains 256 Kbytes of memory and the direct memory access the SP card requires.
NT6X47AB	17F	*Master processor memory CP* The NT6X47AB provides RAM for the master processor uses.
NT6X65AA	11F, Provisionable: for 4F-10F	*CCIS signaling terminal CP* The NT6X65AA transmits and receives signaling data between a DMS-100 switch and the CCIS and CCITT6 transmission links. The NT6X65AA performs the following main functions: • parallel-to-serial data conversion on messages from the MSB6 • serial-to-parallel data conversion on messages from the transmission link modem • error checking on messages between the MSB6 and the transmission link modem

NT6X07AC (continued)

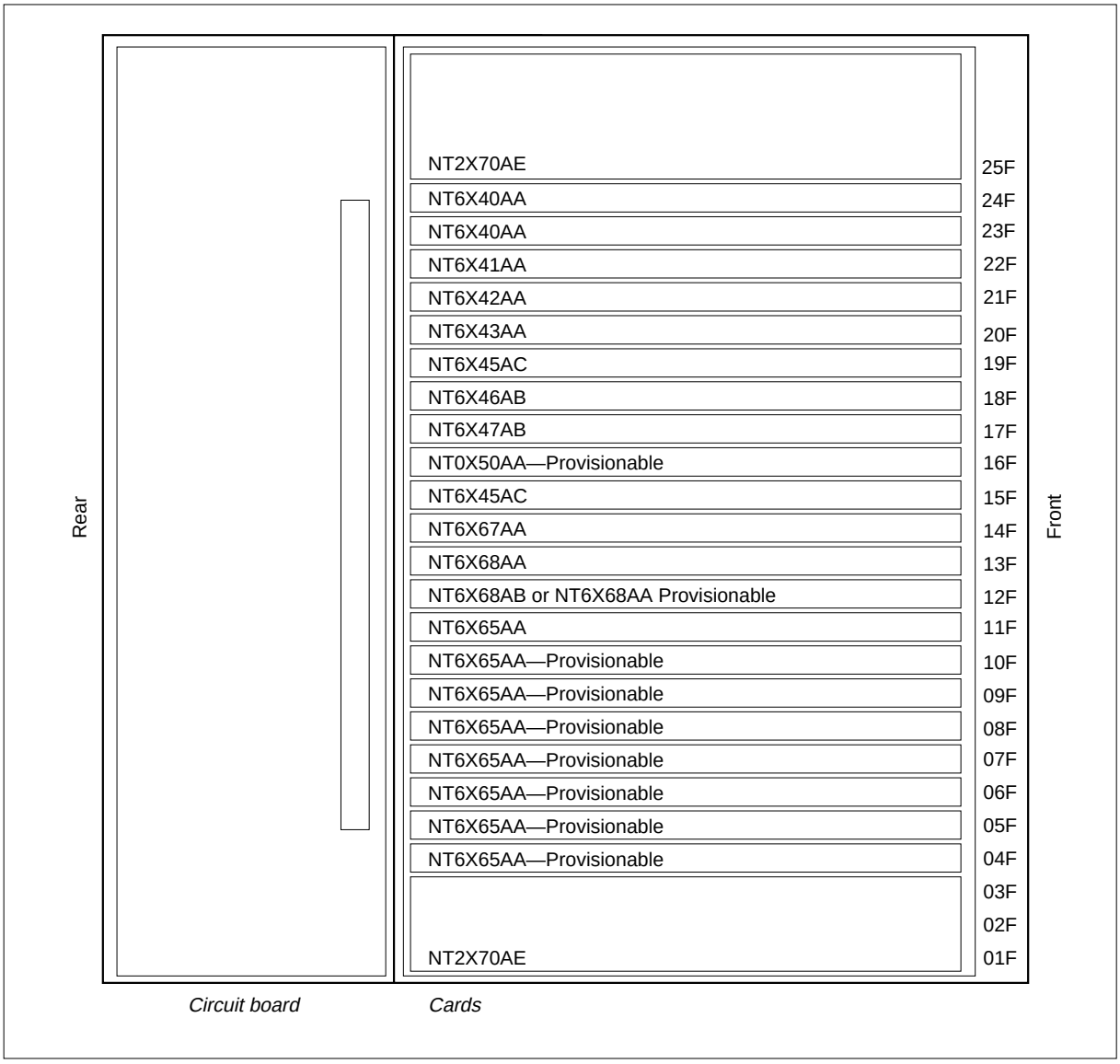
NT6X07AC cards (Sheet 4 of 4)

Card PEC	Slot	Description
NT6X67AA	14F	*Signaling terminal buffer CP* The NT6X67AA generates and checks parity on data transmitted between the MSB6 and the STC.
NT6X68AA	12F, Provisionable: 13F	*Signaling terminal interface CP* The NT6X68AA provides latches for address, data, and control lines to the STC for fault diagnosis and maintenance.
NT6X68AB	12F, Provisionable:	*Signaling terminal interface CP* The NT6X68AB provides latches for address, data, and control lines to the STC for fault diagnosis and maintenance.

The design of the NT6X07AC appears in the following figure.

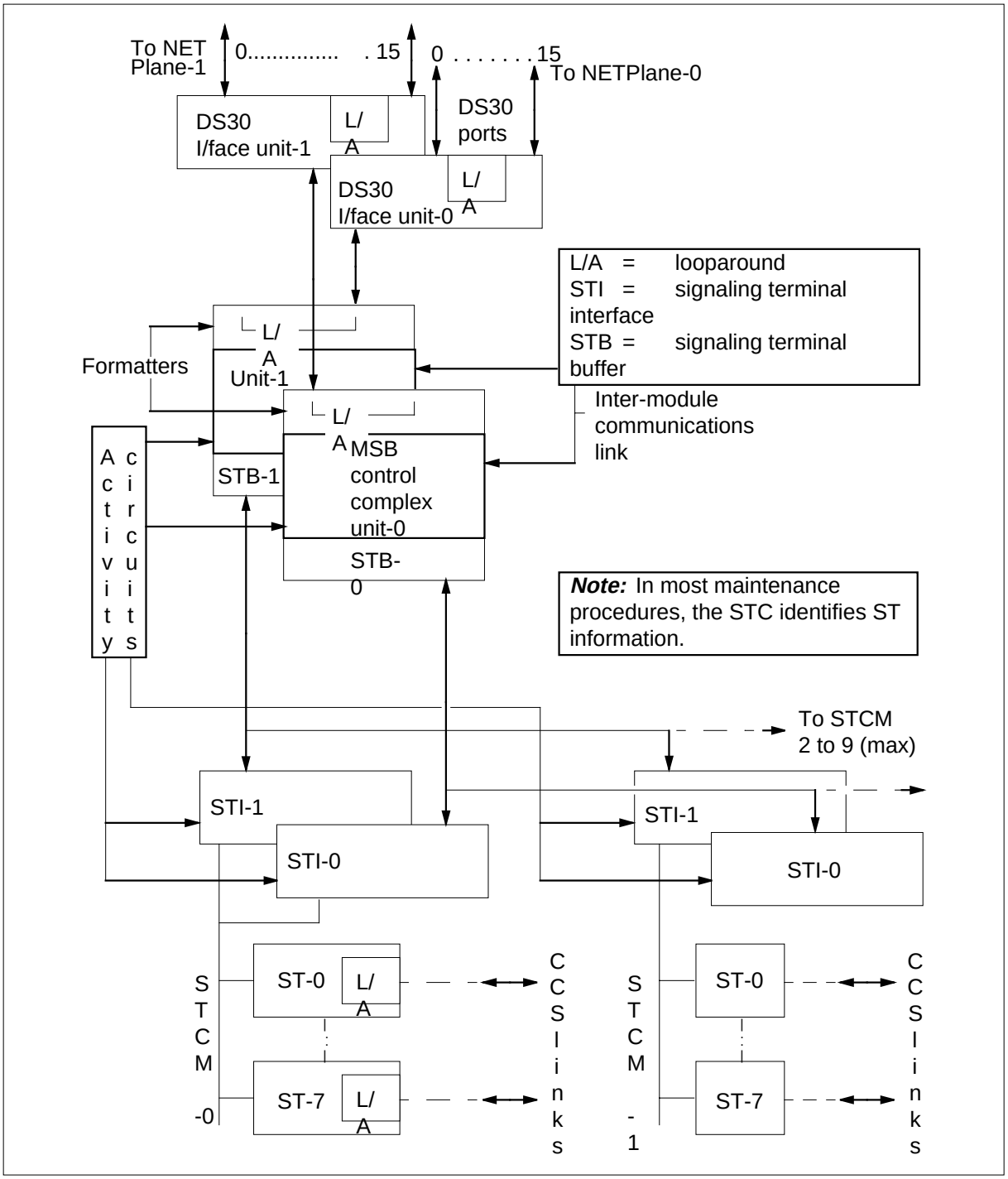
NT6X07AC (continued)

NT6X07AC layout



A simplified block diagram of data flow in the NT6X07AC appears in the following figure.

NT6X07AC simplified block diagram



NT6X08AA

Product description

The NT6X08AA signaling terminal extension shelf provides a maximum of 16 signaling terminals (ST) for each shelf. An NT6X09AA signaling terminal extension frame or NT6X31AA message switching 7 equipment frame contains the NT6X08AA shelf.

A corresponding NT6X06AB message switching 6 equipment frame or NT6X31AA frame contains 16 STs. These STs are in addition to the STs in the NT6X08AA.

An NT6X09AA frame can have a maximum of three shelves.

Parts

The NT6X08AA shelf has the following parts:

- NT0X50AA–Filler face plate .875
- NT2X70AE–Power converter, ±5 V/12 V
- NT6X65AA–CCIS signaling terminal circuit pack (CP)
- NT6X66AA–CCS7 signaling terminal CP
- NT6X66CA–DPNSS signaling terminal interface CP
- NT6X68AA–Signaling terminal interface CP
- NT6X68AB–Signaling terminal interface CP with terminator
- NT6X68AC–Signaling terminal interface CP
- NT6X68AD–Signaling terminal interface CP with terminator

Design

The design of the NT6X08AA appears in the following table.

NT6X08AA parts (Sheet 1 of 3)

PEC	Slot	Description
NT0X50AA	04-24	*Filler face plate .875* The NT0X50AA filler face plate fills unused card slots, 04-24.

NT6X08AA (continued)

NT6X08AA parts (Sheet 2 of 3)

PEC	Slot	Description
NT0X50AE	1, 25	*Filler face plate 2.62* The NT0X50AE filler face plate fills unused card slots 1 or 25 when a power converter is not present.
NT2X70AE	Provisionable: 1, 25	*Power converter,±5 V/12 V* The NT2X70AE power converter provides a regulated supply of dc potential of ±5 V/12 V to the circuit cards on the NT6X08AA shelf.
NT6X65AA	Provisionable: 17-24	*Common channel inter-office signaling No.6(CCIS) signaling terminal circuit pack* The NT6X65AA CCIS terminal card transmits and receives signaling data between a DMS-100 switch, the CCIS and CCITT6 transmission links.
NT6X66AA	Provisionable: 04-11	*Common channel signaling No. 7 (CCS7) signaling terminal circuit pack* The NT6X66AA CCS7 terminal card: • transmits and receives signaling data over CCS7 transmission links • starts the CCS7 link protocol • monitors signaling link performance
NT6X66CA	Provisionable: 12, 13, 15, 16	*DPNSS signaling terminal interface circuit pack* The NT6X66CA is a signaling terminal interface circuit pack for digital private network signaling system (DPNSS) use.
NT6X68AA	Provisionable: 12, 13, 14, 15	*Signaling terminal interface circuit pack* The NT6X68AA provides latches for address, data, and control lines to the signaling terminal controller (STC) for fault diagnosis and maintenance. See the table on page 3.

NT6X08AA (continued)

NT6X08AA parts (Sheet 3 of 3)

PEC	Slot	Description
NT6X68AB	Provisionable: 12, 13, 14, 15	*Signaling terminator interface circuit pack with terminator* The NT6X68AB provides latches for address, data, and control lines to the STC for fault diagnosis and maintenance. Refer to the table on page 3. The NT6X68AB contains built-in termination (resistors).
NT6X68AC	Provisionable: 12, 13, 15, 16	*Signaling terminal interface circuit pack* The NT6X68AC signaling terminal interface (STI) provides latches for address, data, and control lines to the STC for fault diagnosis and maintenance. See the following table. Each of the two groups of ST cards has two STIs. The figure on page 4 shows the STIs. Each group is a signaling terminal group (STG). The STI1 (for STG n and STG n+1) in slots 12 and 16, interface to MSB7 unit-1. The STI0 (for STG n and STG n+1) in slots 13 and 15 interface to MSB7 unit-0. Refer to NT6X32AA.
NT6X68AD	Provisionable: 12, and 13, or 15 and 16 (in one STG only in the NT6X09AA or NT6X31AA frames)	*Signaling terminal interface circuit pack with terminator* The highest numbered STG in the NT6X09AA or NT6X31AA frames uses NT6 X68AD circuit packs because these packs terminate data buses. The NT6X68AD provides the STC with latches for address, data, and control lines for fault diagnosis and maintenance. See the following table.

NT6X08AA (continued)

The circuit cards provisioned for the three types of applications appear in the following table.

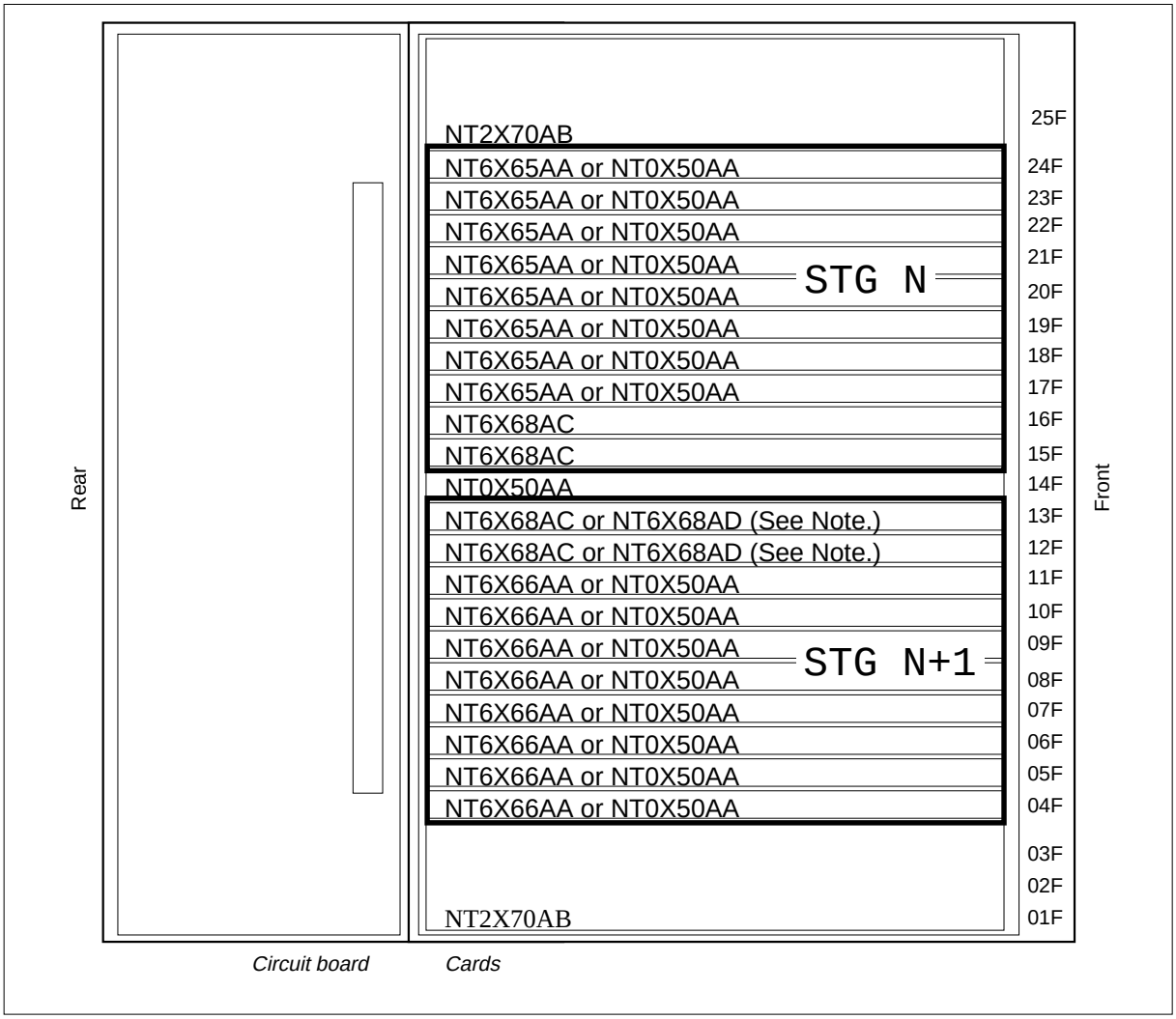
NT6X08AA provisionable circuit cards

Signaling terminal card	for ST6E	for ST7E	for DPNSS
Signaling terminal	NT6X65AA	NT6X66AA	NT6X66CA
Signaling terminal interface	NT6X68AA	NT6X68AC	NT6X68AC
Signaling terminal interface with terminator	NT6X68AB	NT6X68AD	NT6X68AD

The positions of the circuit cards on the NT6X08AA shelf appear in the following table.

NT6X08AA (end)

NT6X08AA design



Note: The highest numbered STG in the NT6X09AA or NT6X31AA frames contains a pair of NT6X68AD circuit packs to terminate the data bus.

NT6X09AA

Product description

The signaling terminal extension frame contains the following:

- CCITT signaling number 6 (CCITT6)
- common channel interoffice signaling (CCIS6)
- common channel signaling 7 (CCS7) signaling terminals (ST)

The NT6X09AA is the STE6 (signaling terminal 6 extension) frame when the NT6X09AA is an extension for CCITT No. 6 or CCIS6 applications. The NT6X09AA is the STE7 (signaling terminal 7 extension) frame under two conditions. One condition is when the NT6X09AA provides an extension for CCS7. The second condition is when the NT6X09AA extends the digital private network signaling system (DPNSS) applications.

The NT6X09AA allows the addition of a maximum of 48 STs on 3 ST extension shelves. These shelves are in positions 51, 32, and 18. These STs are in addition to:

- 16 STs on the NT6X06AB/AC MS6E frame
- 24 STs on the NT6X31AA MSE7 frame

The NT6X29 data modem extension frame must have the NT6X29 STE6 frame.

Parts

The NT6X09AA contains the following parts:

- NT0X28AP–Frame supervisory panel (FSP)
- NT0X84AA–Cage filler panel assembly
- NT3X90AA–Cooling inverter unit
- NT3X90AB–Cooling inverter unit
- NT3X90AC–DC fan cooling unit
- NT6X08AA–Signaling terminal extension shelf

Frame supervisory panel

The NT0X28AP FSP contains two NT0X91AE converter drive and protection circuits and one NT0X91AA alarm and converter drive circuit. The NT0X28AP FSP monitors and controls the power supply to the MS6E from the power distribution center (PDC) in the DMS-100 system.

NT6X09AA (continued)

The NT0X28AP FSP transmits the required potential of -48V nominal from the office battery. The NT0X28AP FSP uses five circuit breakers to protect the power control and alarm circuits to shelves in the NT06X09AA frame. The NT0X28AP uses five fuses to protect alarm battery supply (ABS) circuits.

The NT0X28AP has a mechanical interlock feature. This feature is a small sliding cover that allows access to two circuit breakers (CB) at a time. If all four circuit breakers are ON this feature prevents accidental tripping of CBs in both groups.

The CB1 and CB4 serve shelf 51. The CB5 and CB6 serve shelf 32. The CB2 and CB3 serve shelf 18.

Cage filler panel assembly

The NT0X84AA cage filler panel assembly fills in shelves that are not used in the NT6X09AA frame. This process allows the frame contents to cool correctly.

Cooling inverter unit

The NT3X90AA uses fans to provide forced-air cooling for the NT3X90AA frame. The NT3X90AA includes a built-in inverter that uses the -48V dc battery supply to provide the fans ac power.

Cooling inverter unit

The NT3X90AB uses fans to provide forced-air cooling for the frame. The NT3X90AA has an internal inverter that uses the -48 V dc battery supply to provide ac power to the fans.

DC fan cooling unit

The NT3X90AC cooling unit has five-fan assemblies that maintain a normal five-shelf cabinet. Two feeders in the PDC, fused at 5 A each, provide dc-power to the fans at 48 V each.

The NT3X90AC cooling unit uses a single-fan failure detection and signaling system. The multiple-fan design allows for a single-fan failure without critical loss of cooling air.

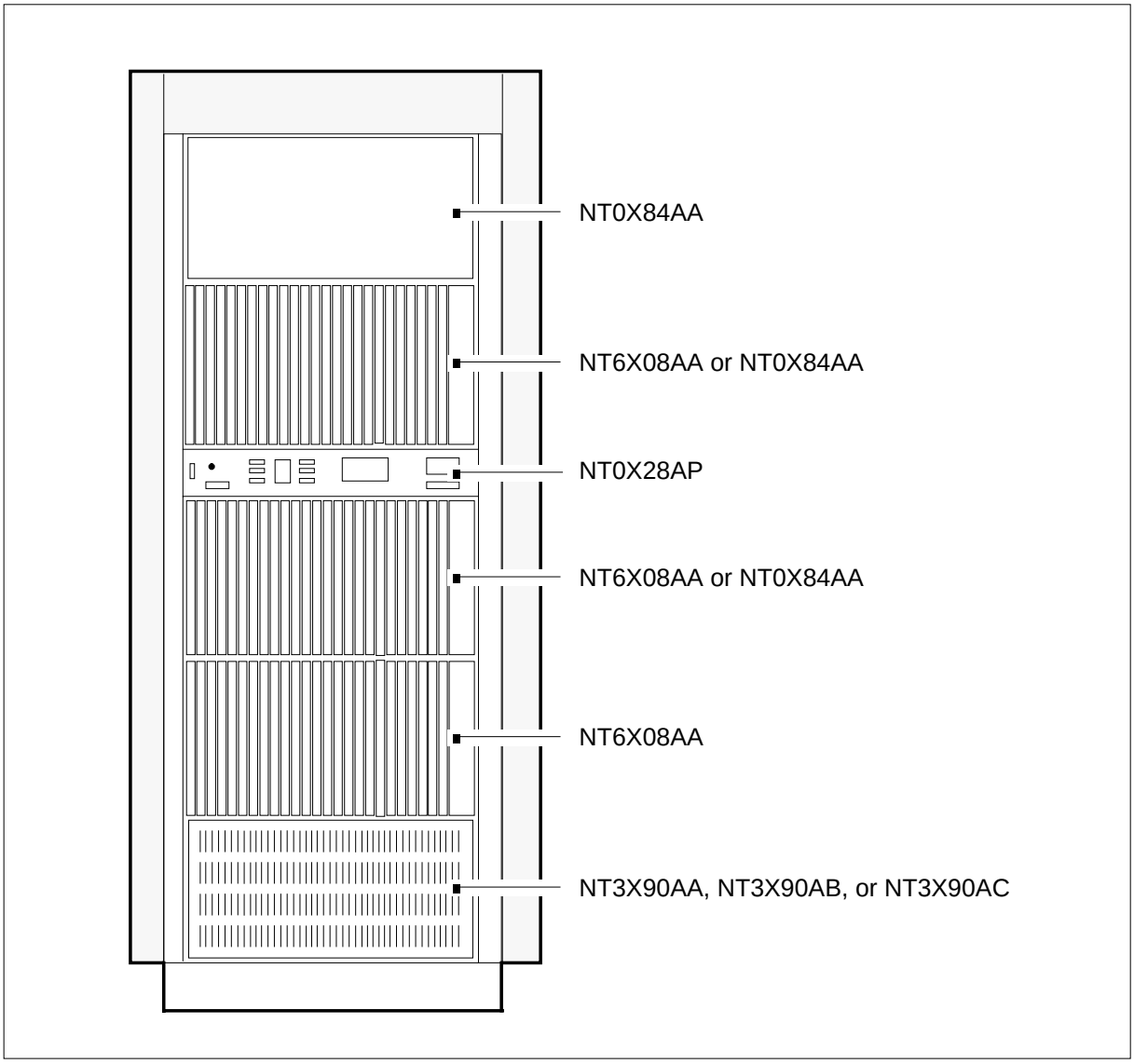
Signaling terminal extension shelf

Each NT6X08AA signaling terminal extension shelf contains a pair of signaling terminal controller modules. The application of the frame determines the type of circuit cards these modules contain. The types of circuit cards that the modules can contain are: CCIS6, CCS7 or DPNSS.

Design

The NT6X09AA design appears in the following figure.

NT6X09AA parts



Note: This illustration does not appear to scale.

NT6X10AC

Product description

The NT6X10AC remote controller equipment (RCE) frame is a standard DMS-100 single bay frame. The NT6X10CA contains a maximum of one dual-shelf remote control array shelf assembly. The NT6X10CA contains a maximum of two remote maintenance module (RMM) shelf assemblies. The bottom two shelves contain the remote control arrays (RCA) that contain the dual-shelf remote cluster controller (RCC). The top part of the RCE frame contains one or two RMMs.

The control-side (C-side) of the RCC provides an interface to the host on DS-1 links to a line group controller/line trunk controller (LGC/LTC). The RCC is in the lower part of the RCE frame. Software translations require 3 to 16 ports to link to a Remote Switching Center (RSC). Hardware requires 2 to 16 DS-1 links for a host interface and reserves a third link. All DS-1 links from an RSC must stop on the same LGC/LTC.

The peripheral-side (P-side) of the RCC contains 20 ports. These ports can support line concentrating modules (LCM), DS-1 trunks and RMMs.

The RSC is available in two configurations, mono RSC and dual RSC. The mono RSC requires only one RCE frame. The dual RSC requires two RCE frames.

Parts

The NT6X10AC remote controller equipment frame contains the following parts:

- NT0X28AS–RCE frame supervisory panel (FSP)
- NT3X90AC–cooling inverter unit
- NT6X1201–RCA shelf assembly
- NT6X1301–RMM shelf assembly

Remote control equipment frame supervisory panel

The NT0X28AS RCE FSP contains power control and alarm circuits. These circuits provide interface between the power distribution center (PDC) and the equipment frames of the DMS-100 Family. The NT0X28AS provides power control to the message switching 7 equipment (MS7E) frame, or to the

signaling terminal 6 equipment (ST6E) frame. The NT0X28AS provides power this control by use of the following:

- six circuit breakers (CB)
- one NT0X91AA converter drive and alarm
- two NT0X91AE converter drive and protection circuit packs

One FSP attaches to each single bay equipment frame. The FSP monitors office battery and alarm battery supply (ABS) fuses and cooling inverter units. If a cooling inverter unit fails, fan fail and frame fail indications, and aisle alarm outputs locate errors.

The ABS fuse 1 powers the alarm circuits of the NT0X91AA converter drive and alarm card. This condition does not directly power the frame fail lamp. Fuse 1 also powers the light-emitting diode (LED) indication next to each circuit breaker. Fuse 1 powers the converter fail LED indication on each associated power converter. Fuse 2 powers the frame fail lamp. Fuse 3 powers toll break-in (TB) 2/8, which is used for end aisle lamp power when appropriate. Fuse 4 powers TB2/10, which is used for the fan switch alarm loop. Fuse 5 powers the ABS test jacks on the front and the rear of the FSP.

Converter fail lines connect to the LED indicators on the power converters in the associated frame. A frame fail indication on the FSP front panel and an aisle alarm output monitor these lines. The lines are monitored for a converter or fuse failure. Converter fail lines operate an LED indicator on the front panel of the FSP below the associated power feed circuit breaker. The converter fail lines also operate the LED indicator in the circuit pack power converter.

Four service jacks on the front panel provide access to two telephone pairs and two data pairs. The telephone pairs are TEL-A and TEL-B and the data pairs are DATA-A and DATA-B. The service jacks provide interframe and interaisle communications through connectors on the FSP. This condition occurs when the service jacks are used with the FSP on other frames. The FSP features a mechanical interlock. The interlock is a small sliding cover that accesses three circuit breakers at a time.

Cooling inverter unit

The NT3X90AC cooling inverter provides forced-air cooling.

Remote control array shelf assembly

The NT6X1201 RCA shelf assembly contains the cards that consist of an RCA shelf.

NT6X10AC (continued)

Remote maintenance module shelf assembly

The NT6X1301 RMM shelf assembly contains the following cards:

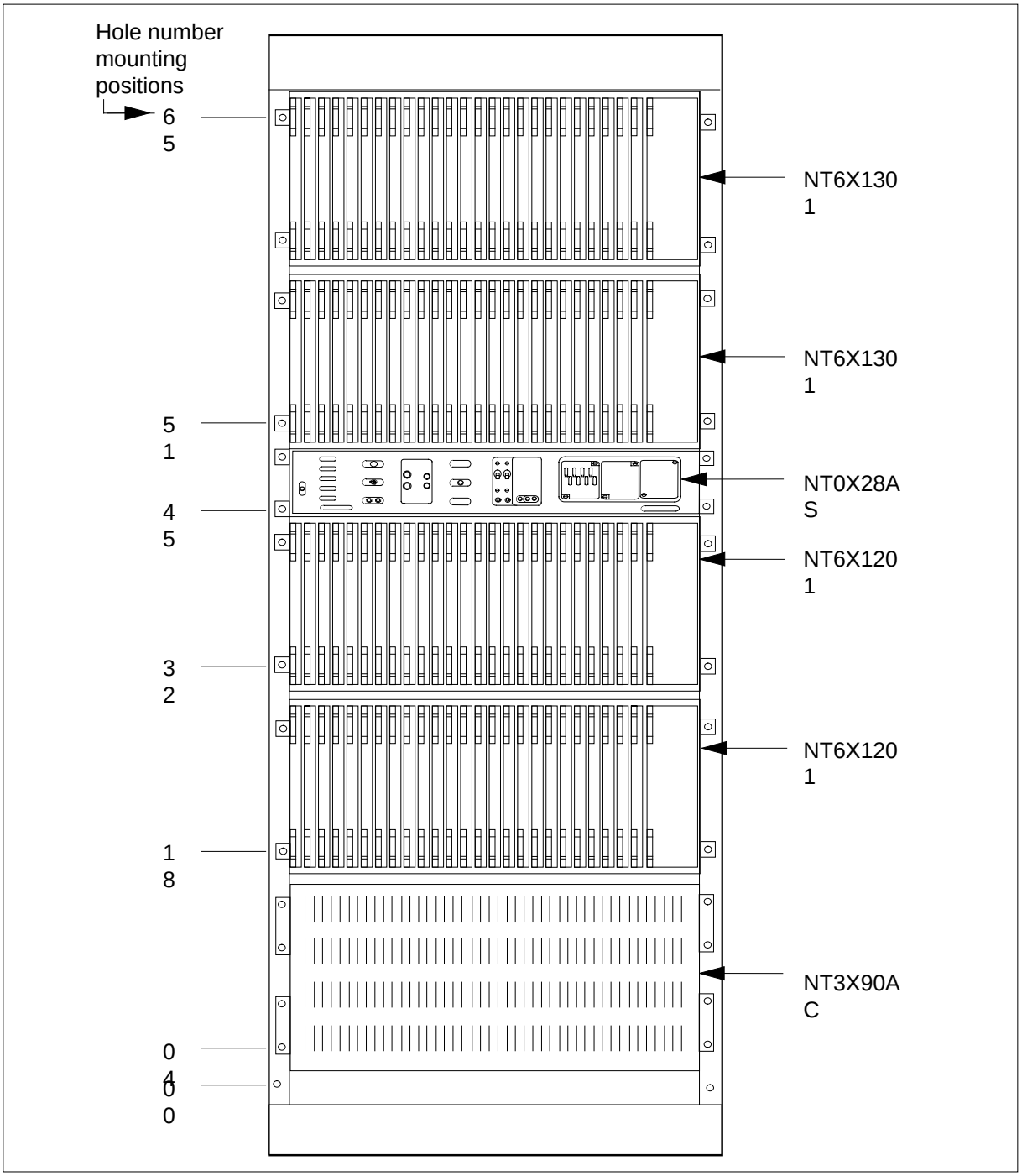
- CODEC and tones card
- RMM control card
- a maximum of 14 optional trunk and service cards

These cards consist of the RMM that provides test trunks and alarm, service, and diagnostic circuits for the RCE frame.

Design

The design of the NT6X10AC appears in the following figure.

NT6X10AC parts



NT6X10AD

Product description

The NT6X10AD ISDN remote controller equipment (RCEI) frame is a standard DMS-100 single bay frame. This NT6X10AD contains a maximum of one dual-shelf remote control array (RCA) shelf assembly. This NT6X10AD also contains a maximum of two remote maintenance module (RMM) shelf assemblies. The lower two shelves contain the remote control arrays (RCA) that contain the dual-shelf remote cluster controller (RCC). The upper part of the RCEI frame contains one or two RMMs. The RCEI frame is used for configuration in a remote site with a remote control and maintenance equipment (RCME) frame. The RCEI frame can be retrofitted to a Remote Switching Center (RSC) configuration.

The control-side (C-side) of the RCC links to the host on DS-1 links to a line group controller/line trunk controller (LGC/LTC). The C-side of the RCC is in the lower part of the RCEI frame. Software translations require 3 to 16 ports to link to an RSC. Hardware requires 2 to 16 DS-1 links for a host interface, and reserves a third link. All DS-1 links from an RSC must stop on the same LGC/LTC.

The peripheral-side (P-side) of the RCC contains 20 ports. These ports can support line concentrating modules (LCM), DS-1 trunks, and RMMs.

The RSC is available in two configurations, mono RSC and dual RSC. The mono RSC requires only one RCEI frame. The dual RSC requires two RCEI frames.

Parts

The NT6X10AD ISDN remote controller equipment frame contains the following parts:

- NT0X28EC–RCE frame supervisory panel (FSP)
- NT3X90AC–cooling inverter unit
- NT6X1206–RCA shelf assembly
- NT6X1301–RMM shelf assembly

Remote controller equipment frame supervisory panel

The NT0X28EC RCE FSP contains power control and alarm circuits. These circuits provide interface between the power distribution center (PDC) and the equipment frames of the DMS-100 Family. Power control is provided to the

message switching 7 equipment (MS7E) frame, or to the signaling terminal 6 equipment (ST6E) frame. The following parts provide power control:

- six circuit breakers (CB)
- one NT0X91AA converter drive and alarm
- two NT0X91AE converter drive and protection circuit packs

One FSP attaches to each single bay equipment frame. The FSP monitors office battery and alarm battery supply (ABS) fuses and cooling inverter units. If a cooling inverter unit fails, fan fail and frame fail indications, and aisle alarm outputs locate errors.

The ABS fuse 1 powers the alarm circuits of the NT0X91AA converter drive and alarm card. This condition does not directly power the frame fail lamp. Fuse 1 also powers the light-emitting diode (LED) indication next to each circuit breaker. Fuse 1 also powers the converter fail LED indication on each associated power converter. Fuse 2 powers the frame fail lamp. Fuse 3 powers toll break-in (TB) 2/8, which is used for end aisle lamp power when appropriate. Fuse 4 powers TB2/10, which is used for the fan switch alarm loop. Fuse 5 powers the ABS test jacks on the front and the rear of the FSP.

Converter fail lines connect to the LED indicators on the power converters in the associated frame. A frame fail indication on the FSP front panel and an aisle alarm output monitor these lines. This event occurs to locate a converter or fuse failure. Converter fail lines also operate an LED indicator on the front panel of the FSP below the associated power feed circuit breaker. Converter fail lines also operate the LED indicator in the power converter card.

Four service jacks on the front panel access two telephone pairs and two data pairs. The telephone pairs are TEL-A and TEL-B and the data pairs are DATA-A and DATA-B. The service jacks provide interframe and interaisle communications through connectors on the FSP. This condition occurs when the service jacks are used with the FSP on other frames. The FSP also features a mechanical interlock. The interlock is a small cover that slides to access three circuit breakers at a time.

Cooling inverter unit

The NT3X90AC cooling inverter provides forced-air cooling.

Remote control array shelf assembly

The NT6X1206 RCA shelf assembly contains the cards that consist of an RCC shelf. The NT6X1206 RCA shelf assembly is for use in ISDN applications.

NT6X10AD (continued)

Remote maintenance module shelf assembly

The NT6X1301 RMM shelf assembly contains the following cards:

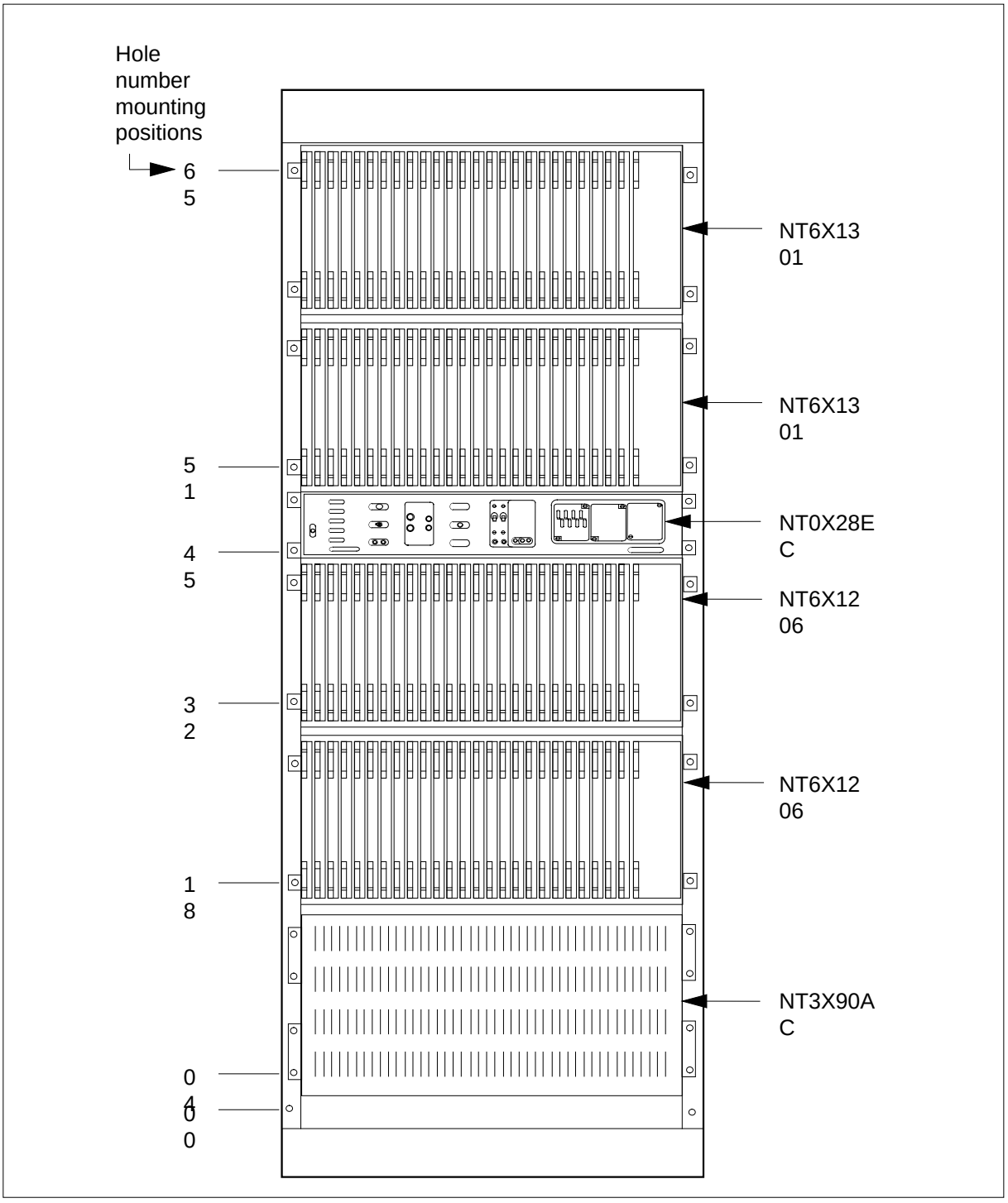
- CODEC and tones card
- RMM control card
- two power converter cards
- a maximum of 14 optional trunk and service cards

These cards contain the remote maintenance module (RMM). The RMM provides test trunks and alarm, service, and diagnostic circuits for the RCE frame.

Design

The design of the NT6X10AD appears in the following figure.

NT6X10AD parts



NT6X10AE

Product description

The NT6X10AE offshore remote controller equipment (RCE) frame is a standard DMS-100 single bay frame. The NT6X10AE contains a maximum of one dual-shelf remote controller array (RCA) shelf assembly. The NT6X10AE also contains a maximum of one remote maintenance module (RMM) shelf assembly. The lower two shelves contain the RCAs that consist of the dual-shelf PCM-30 remote cluster controller (PRCC). The upper part of the offshore RCE frame contains one or two RMMs.

The offshore RCE frame is based on the domestic NT6X10AD ISDN remote controller equipment (RCEI) frame. The offshore NT6X10AD ISDN RCEI frame is adapted for offshore markets. For remote applications, the NT6X10AD ISDN RCEI supports specific services on standard international and ISDN line concentrating modules (ILCM). These services are plain ordinary telephone service (POTS), Centrex, and limited ISDN services. The PCM-30 trunks connect the offshore RCE frame to the host peripheral controller.

The control-side or C-side of the PRCC links to the host on PCM-30 links to a line group controller/line trunk controller (LGC/LTC). The C-side of the PRCC is in the lower part of the offshore RCE frame. Software translations require 3 to 16 ports to link to a Remote Switching Center (RSC). Hardware uses a host interface requirement of 2 to 16 PCM-30 links, with a third link reserved. All PCM-30 links from an RSC must terminate on the same LGC/LTC.

The peripheral-side or P-side of the PRCC has 20 ports that can support line concentrating modules (LCM), PCM-30 trunks and RMMs.

The RSC is available in two configurations, mono RSC and dual RSC. The mono RSC requires one offshore RCE frame. The dual RSC requires two offshore RCE frames.

Parts

The NT6X10AE offshore remote controller equipment frame contains the following parts:

- NT0X0009–logic cable return assembly
- NT0X28EC–RCE frame supervisory panel (FSP)
- NT3X90AC–cooling inverter unit
- NT6X1210–RCA shelf assembly
- NT6X12DB–PRCC common circuit pack (CP)

- NT6X1301–RMM shelf assembly
- NT6X13EA–RMM common CP
- P0575239–filler panel

Logic cable return assembly

Each offshore RCE frame requires an NT0X0009 logic cable return assembly. This condition occurs when current offices not equipped with enhanced grounding are extended.

Remote controller equipment frame supervisory panel

The NT0X28EC RCE FSP contains power control and alarm circuits. The alarm circuits provide interface between the power distribution center (PDC) and the equipment frames of the DMS-100 Family. The following parts provide power control to the message switching 7 equipment (MS7E) frame, or to the signaling terminal 6 equipment (ST6E) frame:

- six circuit breakers (CB)
- one NT0X91AA converter drive and alarm
- two NT0X91AE converter drive and protection cards

One FSP attaches to each single bay equipment frame. The FSP monitors office battery and alarm battery supply (ABS) fuses, and cooling or inverter units. When a cooling or inverter unit fails, fan or frame fail indications and aisle alarm outputs identify the errors.

The ABS fuse 1 powers the alarm circuits of the NT0X91AA converter drive and alarm card. This condition powers the frame fail lamp and the light-emitting diode (LED) indication next to each circuit breaker. This condition powers the converter fail LED indication on each associated power converter. Fuse 2 powers the frame fail lamp. Fuse 3 powers toll break-in (TB) 2/8 that can power the aisle lamp. Fuse 4 powers TB2/10, which is used for the fan switch alarm loop. Fuse 5 powers the ABS test jacks on the front and the rear of the FSP.

Converter fail lines connect to the LED indicators on the power converters in the associated frame. Frame fail indication on the FSP front panel and an aisle alarm output monitor these lines for converter or fuse failure. The converter fail lines operate an LED indicator on the front panel of the FSP below the associated power feed circuit breaker. Converter fail lines also operate the LED indicator in the power converter card.

Four service jacks on the front panel provide access to two telephone pairs and two data pairs. The telephone pairs are TEL-A and TEL-B and the data pairs

NT6X10AE (continued)

are DATA-A and DATA-B. The service jacks provide interframe and interaisle communications through connectors on the FSP. This condition occurs when the service jacks operate with the FSP on other frames. The FSP features a mechanical interlock. The interlock has a small sliding cover that allows access to three circuit breakers at a time.

Cooling inverter unit

The NT3X90AC cooling inverter provides forced-air cooling.

Remote control array shelf assembly

The NT6X1210 RCA shelf assembly contains the cards that an RCC shelf requires. This RCA shelf assembly is designed for offshore applications.

PRCC common circuit pack

The NT6X12DB PCM-30 remote cluster controller (PRCC) common circuit pack contains circuit cards. These circuit cards help provide interface to PCM-30 interfaces that match from PCM-30 links.

Remote maintenance module shelf assembly

The NT6X1301 RMM shelf assembly contains the following cards:

- CODEC and tones card
- RMM control card
- two power converter cards
- a maximum of 14 optional trunk and service cards

The remote maintenance module (RMM) requires these card. The RMM provides test trunks and alarm, service, and diagnostic circuits for the RCE frame.

Remote maintenance module common circuit pack

The NT6X13EA RMM common circuit pack provides maintenance and service functions. The SL-100 UK applications uses this circuit pack. The circuit pack contains the following cards:

- CODEC and tones card
- RMM control card
- two power converter cards
- a maximum of 14 optional trunk and service cards

Filler panel

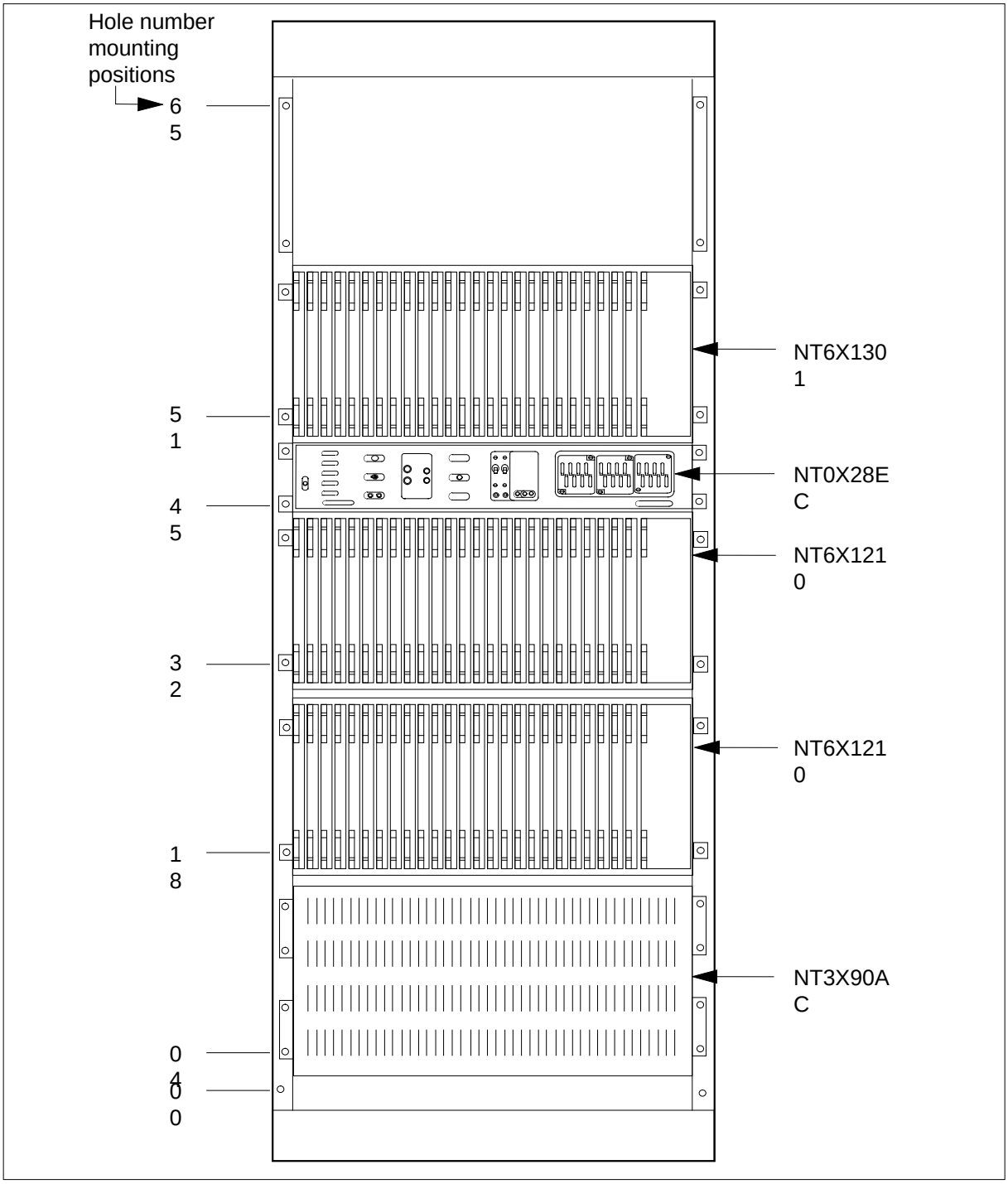
Shelf 65 of the offshore RCE frame contains the P0575239 filler panel when the offshore RCE frame does not require an RMM.

Design

The design of the NT6X10AE appears in the following figure.

NT6X10AE (end)

NT6X10AE parts



NT6X11AA

Product description

The NT6X11AA host interface equipment (HIE) common circuit pack (CP) is a part of the following modules:

- NT6X14AA remote line concentrating module (RLCM)
- NT8X01AA outside plant module (OPM)
- NT8X01BB outside plant module-256 (OPM-256)

The NT6X11AA functions as an interface between the following links:

- the DS30A links of the line concentrating arrays (LCA) in the line concentrating module (LCM) CP or the international line concentrating module (ILCM) CP
- the DS-1 links of a line group controller (LGC) or line trunk controller (LTC) in a DMS-100 central office

The NT6X11AA provides the following features:

- clock signal and ringing generators for the LCAs
- messaging interface and data rate conversion for the DS1 line cards of the circuit pack
- line concentrating arrays of the LCMs
- remote maintenance module (RMM) circuit pack (CP) fill. This circuit pack fill is also located in the RLCM or OPM.

The HIE common CP provides options on the same RLCM or OPM to be completed when the links to the host office are lost. The emergency stand-alone (ESA) operation supports the following services:

- plain ordinary telephone service (POTS)
- local dialing plans for POTS and Meridian Digital Centrex (MDC)
- hunt groups in sequence
- pulse and dual tone multifrequency (DTMF) reception
- all ringing types that the associated line concentrating module (LCM), ground and loop start lines support
- revertive calling for non-business-set party lines
- 63 automatic lines and a manual operator line

NT6X11AA (continued)

The ESA operation does not support the following services:

- attendant consoles
- vertical services
- local automatic message accounting (LAMA) and centralized automatic message accounting (CAMA) billing
- recorded announcements
- coin-control functions
- maintenance and administration functions

The ESA operation supports some MDC services such as multiple centrex customer dialing plans.

The HIE common CP contains the following cards:

- two or three NT6X50AA DS-1 interface circuit cards
- two NT6X73AA link control card CP (LCC-0 and LCC-1)
- two NT6X60AA RLCM ringing generators (RG-0 and RG-1)
- two NT2X70AA power converters

If the HIE common CP includes the ESA option, the HIE common CP also contains the following:

- NT6X45AA LGC/digital trunk controller (LGC/DTC) processor
- NT6X75AA ESA clock and tone CP
- NT6X47AB master processor (MP) memory

Parts

The HIE common CP contains the following parts:

- NT2X70AA–Power converter &0xb1;5V and 12-V CP
- NT6X45AA–LGC/DTC processor
- NT6X47AB–Master processor memory
- NT6X50AA–DS-1 interface cards
- NT6X60AA–Ringing generator
- NT6X73AA–Link control card CP
- NT6X75AA–Emergency stand-alone clock and tone CP

Design

The design of the NT6X11AA appears in the following table.

NT6X11AA parts (Sheet 1 of 5)

PEC	Slot	Description
NT2X70AA	22F-25F	*Power converter* The power converter provides the low-voltage supplies of -5V, -12V, +12V and +15V dc that the circuits in the HIE common CP require. The power converter includes a low-voltage monitor circuit, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate light-emitting diode (LED) state indicator.

NT6X11AA (continued)

NT6X11AA parts (Sheet 2 of 5)

PEC	Slot	Description
NT6X45AA	15F	*Line group controller/digital trunk controller processor* The optional LGC/DTC processor, with the optional master processor (MP) memory and the ESA clock and tone circuit cards, allow calls that originate and terminate on the same RLCM or OPM to complete. This condition occurs when the HIE common CP operates in the ESA mode. All call control messages that normally exchange with the CM of the host office now exchange with the ESA processor. The processor uses copies of the CM translation tables to identify calls between lines that the RLCM or OPM serve. The ESA memory card stores the copies of the CM translation tables. The processor enables the messaging link between the LCM processors and the LGC/DTC processor. The processor enters the ESA operating mode automatically when communications with the host office are lost for 30 s. The processor enters the ESA operating mode when the looparound messages do not receive messages for 15 min. When the system restores links to the host LGC or LTC, the CM starts a system ESA-exit or manual ESA-exit procedure. System ESA exits use a time-out period. To override the time-out interval, place the RLCM or OPM in the manual busy state. The manual ESA exits require a return to service (RTS) command after the CM reports that the links to the LGC or LTC are restored. The system loses all calls when the system enters and exits the ESA mode.
NT6X47AB	14F	*Master processor memory* The optional MP memory stores the data that the LGC/DTC processor card requires during ESA operation. The data includes copies of the control module (CM) translation tables that identify the lines the RLCM serves.

NT6X11AA (continued)

NT6X11AA parts (Sheet 3 of 5)

PEC	Slot	Description
NT6X50AA	18F, 19F, 20F	*DS-1 interface cards* Each DS-1 interface card supports two DS-1 links from the host office LGC or LTC. Each DS-1 link connects to one of the LCC cards in the HIE common CP. When both LCCs are active, signals on the even-numbered DS1 links, for example, 0, 2, and 4, are sent through LCC-0 to LCA. Signals on the odd-numbered links, 1, 3, and 5, are sent through LCC-1 to LCA-1. When an LCA becomes inactive, the system routes all traffic through the appropriate LCC to the active LCA.

NT6X11AA (continued)

NT6X11AA parts (Sheet 4 of 5)

PEC	Slot	Description
NT6X60AA	1F-8F	*Ringing generator* The ringing generators, RG-0 and RG-1, generate ringing signals and the dc voltages used for automatic number identification (ANI) and coin functions. These ringing generators operate with the NT6X25AA frame supervisory panel (FSP) in the RLCE frame. Each generator features ringing cadences, ringing frequencies and amplitudes, and dc offsets. Manually operated programming switches can set all these features. These features perform many specified applications. The units include circuits that monitor both the ringing voltage and current. The units include an internal battery supply filter and converters that produce the required operating voltages. The internal dc supplies are regulated and include circuits that limit the current. Each ringing generator also features a faceplate-mounted LED that lights when a problem occurs in the unit. The LED lights when one of the following conditions occurs: • the input current overload trips the external breaker • the external circuit breaker is tripped manually • a ringing section fails • an ANI section overvoltage condition occurs

NT6X11AA (continued)

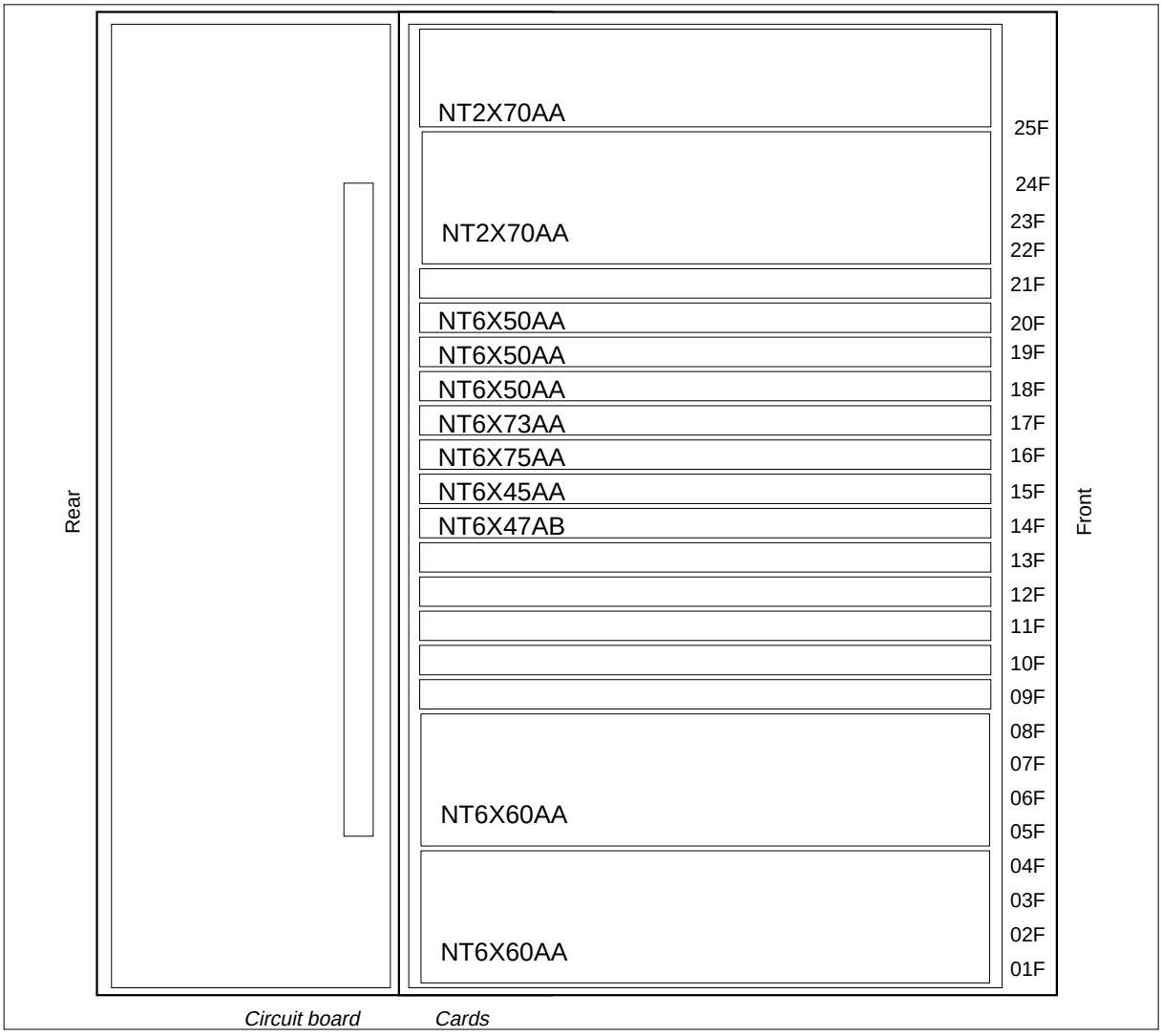
NT6X11AA parts (Sheet 5 of 5)

PEC	Slot	Description
NT6X73AA	17F	*Link control card CP* The LCC CP, LCC-0 and LCC-1 control the DS30A links to the two LCA shelves of the LCM. This condition provides intershelf connections between subscribers on different shelves of the RCLM or OPM. The LCC CP functions as the DS-1 interface between the DS-1 interface cards in the HIE CP and both the LCA and the RMM. The LCA and RMM are in the RCLM or OPM. These cards function as the messaging interface for the ESA clock and tone circuit cards and the LGC/DDTC processor when the ESA option is included. The DS30A links from LCA-0 connect to the P-side of LCC-0. The DS30A links from LCA-1 connect to the P-side of LCC-1. The C-side of each LCC card connects to each DS-1 card, the other LCC and the RMM. Each DS30A channel to and from an LCA connects to a channel in the associated LCC, a channel in a DS-1 interface card, another channel in the same LCC, or a channel in the RMM. This condition depends on the configuration parameter used when the RLCM or OPM is set up.
NT6X75AA	16F	*Emergency stand-alone clock and tone CP* The optional ESA clock and tone circuit card generates the clock signal for the LGC/DTC processor and the tones required for ESA operation. The tones include dial, busy/reorder, receiver off hook, audible ringback and electronic business set ringdown.

The design of the NT6X11AA appears in the following figure.

NT6X11AA (end)

NT6X11AA parts



NT6X11AB

Product description

The NT6X11AB host interface equipment (HIE) common circuit pack (CP) is a part of the following modules:

- NT6X14AA remote line concentrating module (RLCM)
- NT8X01AA outside plant module (OPM)
- NT8X01BB outside plant module-256 (OPM-256)

The HIE common CP functions as an interface between the following links:

- the DS30A links of the line concentrating arrays (LCA) of the line concentrating module (LCM) CP
- the DS-1 links of a line group controller (LGC) or line trunk controller (LTC) in a DMS-100 central office

The HIE common CP provides the following features:

- clock signal and ringing generators for the LCAs
- messaging interface and data rate conversion for the DS-1 line cards of the circuit pack
- line concentrating arrays in the LCMs
- remote maintenance module (RMM) CP fill in the RLCM or OPM

When the HIE common CP includes the emergency stand-alone (ESA) option, the HIE common CP provides call-processing functions. Calls that originate and terminate on the same RLCM or OPM can complete if the links to the host office are lost.

The ESA operation supports the following services:

- plain ordinary telephone service (POTS)
- local dialing plans for POTS and Meridian Digital Centrex (MDC)
- sequential hunt groups
- pulse and dual-tone multifrequency (DTMF) reception
- all ringing types supported by the LCM
- ground/loop start lines
- revertive calling for non-business-set party lines
- 63 automatic lines plus a manual operator line

NT6X11AB (continued)

The ESA operation does not support the following features:

- attendant consoles
- vertical services
- local automatic message accounting (LAMA) and centralized automatic message accounting (CAMA) billing
- recorded announcements
- coin-control functions
- maintenance and administration functions

The ESA operation supports some MDC services such as multiple centrex customer dialing plans.

The CP contains the following cards:

- two or three NT6X50AA DS-1 interface circuit cards
- two NT6X73AA link control card (LCC) CPs (LCC-0 and LCC-1)
- two NT6X60AA RLCM ringing generators (RG-0 and RG-1)
- two NT2X70AA power converters

When the CP includes the ESA option, the CP also contains an:

- NT6X45AA LGC/DTC processor
- NT6X75AA ESA clock and tone CP
- NT6X47AB master processor (MP) memory

Parts

The HIE common CP contains the following parts:

- NT2X70AA–Power converter &0xb1;5V and 12V CP
- NT6X45AA–LGC/DTC processor
- NT6X47AB–Master processor memory
- NT6X50AA–DS-1 interface card
- NT6X60AA–Ringing generator
- NT6X73AA–Link control card CP
- NT6X75AA–Emergency stand-alone clock and tone CP

Design

The design of the NT6X11AB appears in the following table.

NT6X11AB parts (Sheet 1 of 4)

PEC	Slot	Description
NT2X70AA	22F-25F	*Power converter* The power converter provides the low-voltage supplies of -5V, -12V, +12V, and +15V dc that the circuits in the HIE common CP require. The power converter includes a low-voltage monitor circuit, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate light emitting diode (LED) state indicator.

NT6X11AB (continued)

NT6X11AB parts (Sheet 2 of 4)

PEC	Slot	Description
NT6X45AA	15F	*Line group controller/digital trunk controller processor* The optional LGC/DTC processor allows calls that originate and terminate on the same RLCM or OPM to complete when the HIE common CP operates in the ESA mode. This condition occurs when the LGC/DTC processor operates with the optional MP memory and the ESA clock and tone circuit cards. All call control messages that normally exchange with the CM of the host office exchange with the ESA processor. The processor uses copies of the CM translation tables to identify calls between lines that the RLCM or OPM serve. Copies of the CM translation tables are in the ESA memory card. The processor enables the messaging link between the LCM processors and the LGC/DTC processor. The processor enters the ESA mode automatically when communications with the host office are lost for 30 s. The processor enters the ESA mode when the looparound messages do not receive messages for 15 min. When the system restores links to the host LGC or LTC, the CM starts a system ESA-exit or manual ESA-exit procedure. System ESA exits involve a time-out period. To override the time-out period, place the RLCM or OPM in the manual busy state. The manual ESA exits require a return-to-service (RTS) command after the CM reports that the system restored the links to the LGC or LTC. The system loses calls when the system enters and exits the ESA mode.
NT6X47AB	14F	*Master processor memory* The optional MP memory stores the data that the LGC/DTC processor card require during ESA operation. The data includes copies of the control module (CM) translation tables that identify the lines the RLCM serves.

NT6X11AB (continued)

NT6X11AB parts (Sheet 3 of 4)

PEC	Slot	Description
NT6X50AA	18F, 19F, 20F	*DS-1 interface cards* Each DS-1 interface card supports two DS-1 links from the host office LGC or LTC. Each DS-1 links connect to one of the LCC cards in the HIE common CP. When both LCCs are active, signals on the even-numbered DS1 links, for example, 0, 2, and 4, are sent through LCC-0 to LCA-0. Signals on the odd-numbered links, 1, 3, and 5, are sent through LCC-1 to LCA-1. When an LCA becomes inactive, the system routes all traffic through the appropriate LCC to the active LCA.
NT6X60AA	1F-8F	*Ringing generator* The ringing generators (RG-0 and RG-1) generate ringing signals and the dc voltages used for automatic number identification (ANI) and coin functions. These ringing generators must operate with the NT6X25AA frame supervisory panel (FSP) in the RLCE frame. Each generator features ringing cadences, ringing frequencies and amplitudes, and dc offsets. Manually operated programming switches can set all of these features. These features perform in many different applications. The units include circuits that monitor both the ringing voltage and current. The units include an internal battery supply filter and converters that produce the required operating voltages. The internal dc supplies are regulated and include circuits that limit current. Each ringing generator also features a faceplate-mounted LED that lights when a problem occurs in the unit. The LED lights when one of the following conditions occurs: • input current overload trips the external breaker • the external circuit breaker is tripped manually • a ringing section fails • an ANI section overvoltage condition occurs

NT6X11AB (continued)

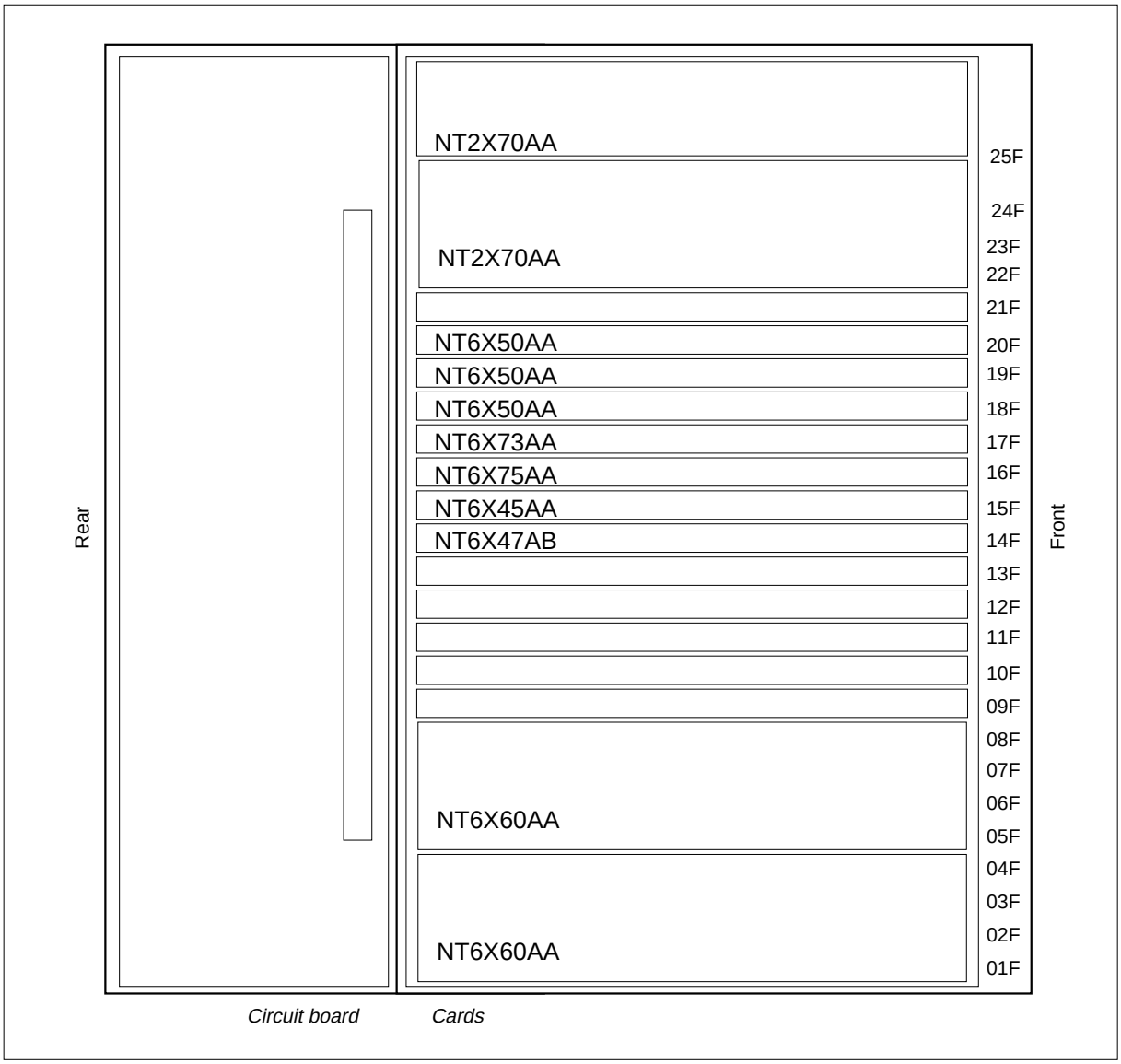
NT6X11AB parts (Sheet 4 of 4)

PEC	Slot	Description
NT6X73AA	17F	*Link control card CP* The LCC CP, LCC-0 and LCC-1, control the DS30A links to the two LCA shelves of the LCM. The LCC CP provides intershelf connections between subscribers on different shelves of the RCLM or OPM. The LCC CP functions as the DS-1 interface between the DS-1 interface cards in the HIE common CP and both the LCA and the RMM. The LCA and RMM are in the RCLM or OPM. These cards function as the messaging interface for the ESA clock and tone circuit cards and the LGC/DDTC processor when the ESA option is included. The DS30A links from LCA-0 connect to the P-side of LCC-0. The DS30A links from LCA-1 connect to the P-side of LCC-1. The C-side of each LCC card connects to each DS-1 card, the other LCC, and the RMM. Each DS30A channel to and from an LCA is connected to a channel in the associated LCC, a channel in a DS-1 interface card, another channel in the same LCC or a channel in the RMM. This condition depends on the configuration parameter used when the RLCM or OPM is installed.
NT6X75AA	16F	*Emergency stand-alone clock and tone CP* The optional ESA clock and tone circuit card generates the clock signal for the LGC/DTC processor and the tones required for ESA operation. The tones are dial, busy/reorder, receiver off hook, audible ringback and EBS ringdown.

The design of the NT6X11AB appears in the following figure.

NT6X11AB (end)

NT6X11AB parts



NT6X11BB

Product description

The international host interface equipment (HIE) shelf (NT6X11BB) is a component of the following frames:

- international remote line concentrating module (IRLCM) NT6X14AA frame
- international outside plant module (IOPM) NT8X40AA frame

The HIE shelf functions as an interface between the following components:

- DS30A links of the line concentrating arrays (LCA) of the line concentrating modules (LCM) (NT6X04 in the IRLCM frame, NT8X04 in the IOPM frame)
- the common peripheral controller (CPC) in a DMS-100 central office

This HIE shelf provides the clock signal and ringing generators for the LCAs.

This HIE shelf provides the messaging interface and data rate conversion for the following components:

- the PCM30 line cards
- the line concentrating arrays of the LCMs
- the international remote maintenance module (RMM) in the IRLCM or IOPM frame

When the emergency stand-alone (ESA) option is available, the international HIE shelf provides call-processing functions. These functions allow calls to complete if the links to the host office are lost. The calls must originate and terminate on the same IRLCM or IOPM. The ESA operation only supports specified Meridian Digital Centrex (MDC) services, like multiple centrex customer dialing plans.

The ESA operation supports the following services:

- plain ordinary telephone service (POTS)
- local dialing plans for POTS and MDC
- sequential hunt groups
- pulse and dual-tone multifrequency (DTMF) reception
- all ringing types supported by the LCM
- ground/loop start lines

- revertive calling for non-business-set party lines
- 63 automatic lines with a manual operator line

The ESA operation does not support the following services:

- attendant consoles
- vertical services
- local automatic message accounting (LAMA) billing
- centralized automatic message accounting (CAMA) billing
- recorded announcements
- coin-control functions
- maintenance and administration functions

The shelf contains the following:

- two or three PCM30 interface circuit cards (NT6X27AB)
- two link control circuit cards (LCC-0 and LCC-1) (NT6X73BA)
- two RLCM ringing generators (RG-0 and RG-1) (NT6X60AA)
- two power converters (NT2X70AE)

If the shelf has the ESA option, the shelf contains the following:

- an ESA processor (NT6X45AF)
- an ESA tone and clock card (NT6X75DA)
- an ESA memory card (NT6X47AB)

Parts

The HIE shelf consists of the following parts:

- NT2X70AA–Power converter &0xb1;5 V and 12 V circuit pack (CP)
- NT6X45AA–Line group controller/digital trunk controller processor (LGC/DTC)
- NT6X47AA–Master processor memory (MPM)
- NT6X50AA–DS-1 interface cards
- NT6X60AA–Ringing generator
- NT6X73AA–Link control card CP
- NT6X75AA–Emergency stand-alone clock and tone CP

NT6X11BB (continued)

Design

The design of the NT6X11BB appears in the following table.

NT6X11BB parts (Sheet 1 of 6)

PEC	Slot	Description
NT2X70AA	22F-25F	*Power converter* The power converter provides the following low-voltage supplies (-5 V, -12 V, +12 V, and +15 V dc) that the circuits in the HIE common CP require: • a low-voltage monitor circuit • overvoltage and overcurrent protection • faceplate test jacks • a faceplate light emitting diode (LED) status indicator

NT6X11BB (continued)

NT6X11BB parts (Sheet 2 of 6)

PEC	Slot	Description
NT6X45AA	15F	*Line group controller/digital trunk controller processor* The optional LGC/DTC processor operates with the optional master processor (MP) memory and the ESA clock and tone circuit cards. The LGC/DTC processor allows specified calls to complete when the HIE common CP operates in the ESA mode. Calls that originate and terminate on the same RLCM or OPM can complete. The common CP must be in ESA mode. In the ESA mode, all call control messages normally exchanged with the host office control module (CM) are exchanged with the ESA processor. The LGC/DTC processor uses copies of the CM translation tables to identify calls between lines that the RLCM or OPM serves. The ESA memory card stores the CM translation tables. The processor enables the messaging link between the LCM processors and the LGC/DTC processor. The processor enters the ESA operating mode. This action occurs when the processor loses communications with the host office for 30 s. This action occurs if no responses to looparound messages occur for 15 min. When the links to the host LGC or LTC are restored, the CM begins a system ESA-exit. The system can perform a manual ESA-exit procedure. System ESA-exits involve a time-out period. To override the time-out period, place the RLCM or OPM in the manual busy (ManB) state. For manual ESA exits, you must enter a return to service (RTS) command. Enter this command when the CM reports that the links to the LGC or LTC are restored. All calls are lost when the LGC/DTC processor enters and exits the ESA mode.
NT6X47AB	14F	*Master processor memory* The optional MP memory stores the data that the LGC/DTC processor card requires during ESA operation. Memory stores include copies of the CM translation tables that to identify lines the RLCM serves.

NT6X11BB (continued)

NT6X11BB parts (Sheet 3 of 6)

PEC	Slot	Description
NT6X50AA	18F, 19F, 20F	*DS-1 interface cards* Each DS-1 interface card supports two DS-1 links from the host office LGC or LTC. Each link connects to one of the LCC cards in the HIE common CP. When both LCCs are active, signals on the even-numbered DS1 links transfer through LCC-0 to LCA-0. Even-numbered links include 0, 2, and 4. Signals on the odd-numbered links, like 1, 3, and 5 transfer through LCC-1 to LCA-1. If an LCA becomes inactive for any reason, all traffic routes through the appropriate LCC to the active LCA.

NT6X11BB (continued)

NT6X11BB parts (Sheet 4 of 6)

PEC	Slot	Description
NT6X60AA	1F-8F	*Ringing generator* The ringing generators (RG-0 and RG-1) operate with the NT6X25AA frame supervisory panel (FSP) in the RLCE frame. These generators produce ringing signals and the dc voltages used for automatic number identification (ANI) and coin functions. Each generator features ringing cadences, ringing frequencies and amplitudes, and dc offsets. To set the cadences, frequencies, and amplitudes for use in specified applications, you must operate programming switches manually. The units include circuits that monitor both the ringing voltage and current. The units include an internal battery supply filter and converters that produce the required operating voltages. The internal dc supplies are regulated. The dc supplies include current-limiting circuits. Each ringing generator features a faceplate-mounted LED that lights when a problem occurs in the unit. The LED lights when one of the following conditions occurs: • input current overload trips the external breaker • the user trips the external circuit breaker • a ringing section fails • an ANI section overvoltage condition occurs

NT6X11BB (continued)

NT6X11BB parts (Sheet 5 of 6)

PEC	Slot	Description
NT6X73AA	17F	*Link control card circuit pack* The LCC-0 and LCC-1 are LCC central processors (CP). The LCC CPs control the DS30A links to the two LCA shelves of the LCM. The LCC CPs control these links to provide intershelf connections between subscribers on different shelves of the RCLM or OPM. The LCC CPs function as the DS-1 interface. The interface is between the DS-1 interface cards in the HIE common CP and both the LCA and the RMM. The LCA and the RMM are in the RCLM or OPM. These cards are the messaging interface for the ESA clock and tone circuit cards and the LGC/DDTC processor. These cards serve as an interface when the ESA option is available. The DS30A links from LCA-0 connect to the P-side of LCC-0. The DS30A links from LCA-1 connect to the P-side of LCC-1. The C-side of each LCC card connects to each DS-1 card, the other LCC and the RMM. Each DS30A channel to and from an LCA connects to one of the following channels: • a channel in the associated LCC • a channel in a DS-1 interface card • another channel in the same LCC • a channel in the RMM The configuration parameter used when the RLCM or OPM is set up determines the channel the DS30A connects to.

NT6X11BB (continued)

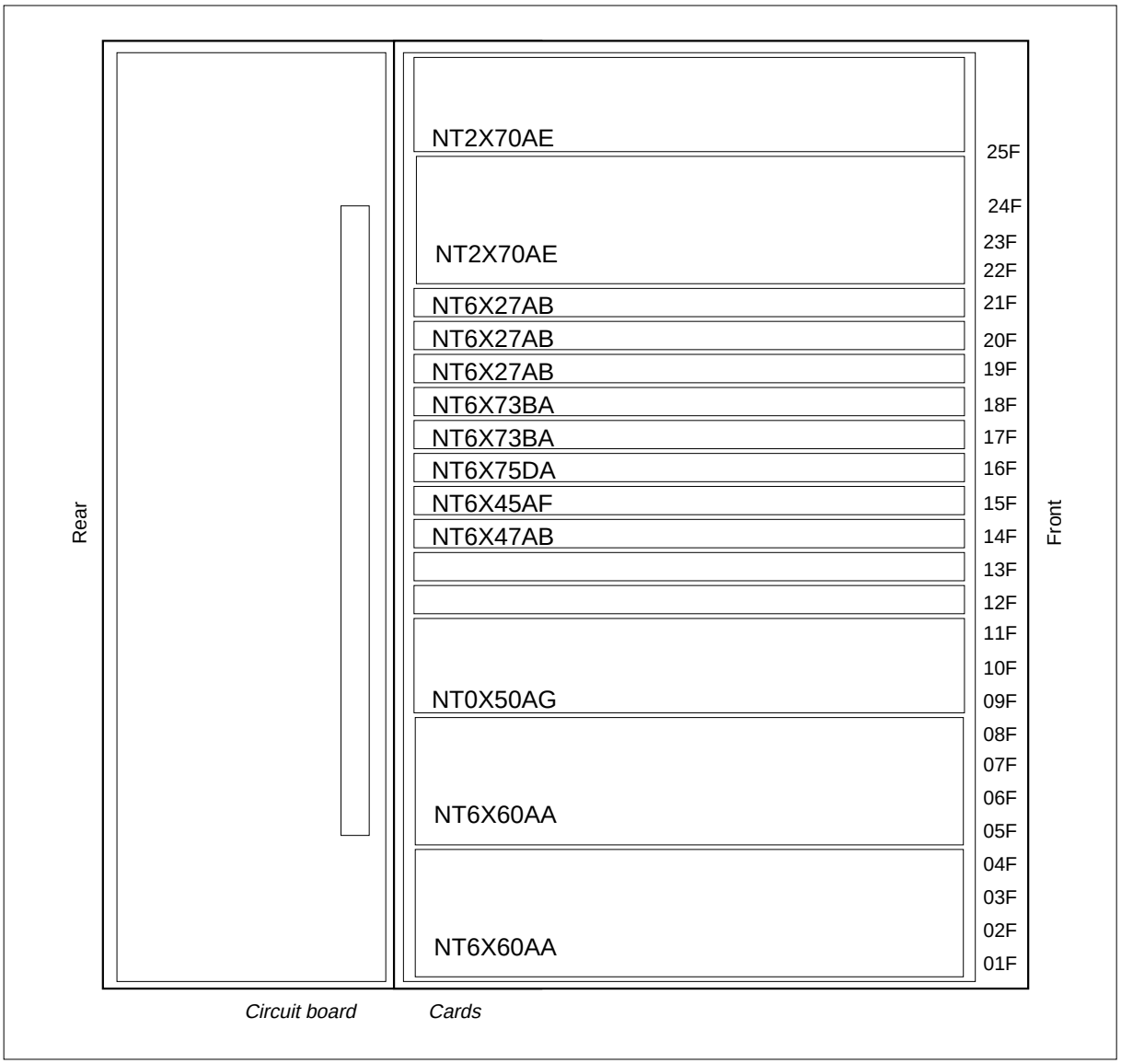
NT6X11BB parts (Sheet 6 of 6)

PEC	Slot	Description
NT6X75AA	16F	*Emergency stand-alone clock and tone circuit pack* The optional ESA clock and tone circuit card generates the clock signal for the LGC/DTC processor. The ESA clock generates the following tones required for ESA operation: • dial • busy/reorder • receiver off hook • audible ringback • EBS ringdown

The design of the NT6X11BB appears in the followin figure.

NT6X11BB (end)

NT6X11BB parts



NT6X11KA

Product description

The NT6X11KA host interface equipment (HIE) common circuit pack (China) is a part of the following frames:

- NT6X14AA international remote line concentrating module (IRLCM) frame
- NT8X40AA international outside plant module (IOPM) frame

This HIE common circuit pack functions as an interface between the following components:

- the PCM-30 links of the line concentrating arrays (LCA) of the line concentrating modules (LCM) (NT6X04 in the IRLCM, NT8X04 in the IOPM frame)
- the common peripheral controller (CPC) in a DMS-100 central office

This HIE common circuit pack (CP) uses PCM-30 interface cards instead of DS-1 interface cards. This change allows the use of the HIE CP for applications in China.

This HIE common CP provides the clock signal and ringing generators for the following components:

- LCAs and the messaging interface and data rate conversion for the PCM-30 line cards
- the line concentrating arrays of the LCMs
- the international remote maintenance module (RMM) located in the IRLCM or IOPM frame

The HIE common CP provides available emergency stand-alone (ESA) call-processing functions. These functions are necessary if the communications links to the LGC or LTC fail.

The ESA operation allows calls to complete if the links to the host office are lost. The calls must originate and terminate on the same RLCM or OPM. The ESA operation only supports specified Meridian Digital Centrex (MDC) services, like multiple Centrex customer dialing plans.

The ESA operation supports the following services:

- plain ordinary telephone service (POTS)
- local dialing plans for POTS and MDC
- sequential hunt groups

NT6X11KA (continued)

- pulse and dual-tone multifrequency (DTMF) reception
- all ringing types that the associated LCM supports
- ground and loop start lines
- revertive calling for non-business-set party lines
- 63 automatic lines with a manual operator line

The ESA operation does not support the following services:

- attendant consoles
- vertical services
- local Automatic Message Accounting (LAMA) billing
- centralized Automatic Message Accounting (CAMA) billing
- recorded announcements
- coin-control functions
- maintenance and administration functions

The HIE common CP contains two NT6X27AB PCM-30 interface cards and two NT6X73BA link control cards. These cards are LCC-0 and LCC-1.

Parts

The NT6X11KA host interface equipment (HIE) common circuit pack (China) consists of the following parts:

- NT0X50AA–filler faceplate
- NT6X27AB–PCM-30 interface cards
- NT6X73BA–link control card card

Design

The parts of the NT6X11KA appear in the following table.

NT6X11KA parts (Sheet 1 of 3)

PEC	Slot	Description
NT0X50AA	12F	*Filler faceplate* The filler faceplate fills empty card slots in the HIE common CP.

NT6X11KA (continued)

NT6X11KA parts (Sheet 2 of 3)

PEC	Slot	Description
NT6X27AB	19F, 20F	*PCM-30 interface cards* Each PCM-30 interface card supports two PCM-30 links from the host office LGC or LTC. Each link connects to one of the LCC cards in the HIE common CP. When both LCCs are active, signals on the even-numbered PCM-30 links transfer through LCC-0 to LCA-0. Signals on the odd-numbered links transfer through LCC-1 to LCA-1. If an LCA becomes inactive for any reason, all traffic routes through the appropriate LCC to the active LCA.

NT6X11KA (continued)

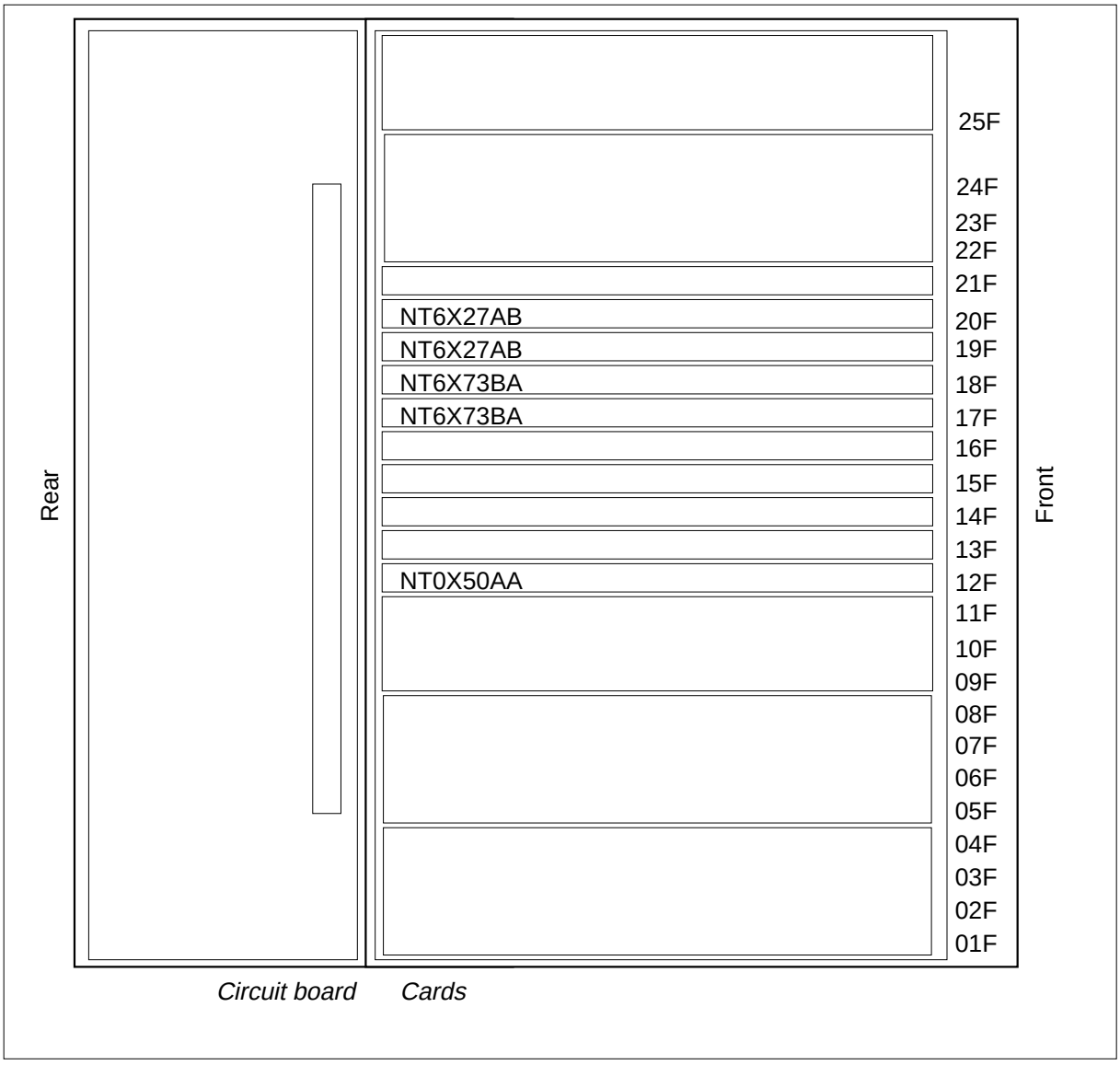
NT6X11KA parts (Sheet 3 of 3)

PEC	Slot	Description
NT6X73BA	17F, 18F	*Link control card cards* The link control card (LCC) cards are LCC-0 and LCC-1. These cards control the DS30A links to the two LCA shelves of the LCM. These cards control the links to provide intershelf connections between subscribers on different shelves of the RCLM or OPM. These cards are the DS-1 interface between the DS-1 interface cards. The DS-1 cards are in the HIE common CP and the LCA and the RMM. The LCA and the RMM are in the RCLM or OPM. These cards are the messaging interface for the ESA clock and tone circuit cards and the LGC/DDTC processor. The cards are the interface when ESA is available. The DS30A links from LCA-0 connect to the peripheral side (P-side) of LCC-0. The DS30A links from LCA-1 connect to the P-side of LCC-1. The central side (C-side) of each LCC card connects to each DS-1 card, the other LCC and the RMM. Each DS30A channel to and from an LCA connects to one of the following channels: • a channel in the associated LCC • a channel in a DS-1 interface card • another channel in the same LCC • a channel in the RMM The configuration parameter used when the RLCM or OPM is set up determines the channel to which the DS30A connects.

The design of the NT6X11KA appears in the following figure.

NT6X11KA (end)

NT6X11KA components



NT6X12AD

Product description

The Remote Switching Centers (RSC) use NT6X12AD remote cluster controller (RCC) common circuit pack. An RSC enables a line trunk controller (LTC) and the associated peripheral module of the line trunk to function from a remote site. A peripheral module that an RCC hosts can function a maximum of 161 km (100 mi) from the host central office.

The RCC common circuit pack (CP) is an LTC that stands alone in a remote location. The connections between the host LTC allow direct communication between the RCC and the central control (CC). As a result, most of the CC/LTC call processing software can be used in CC/RCC call processing. The RCC common circuit pack provides a master controller for all units at the RSC. The host LTC controls this pack. The RCC is a two-shelf peripheral module. The RCC uses many of the same components as an LTC.

The NT6X92BB universal tone receiver is used in slots 14 and 16. This tone receiver enables the RCC common circuit pack to collect and report digits.

Parts

The NT6X12AD remote cluster controller common circuit pack consists of the following parts:

- NT0X50AA–filler face plate
- NT6X44AA–time switch card
- NT6X46AC–signaling processor memory card
- NT6X47AB–master processor memory plus card
- NT6X69AA–common peripheral processor (CPP) message protocol card
- NT6X72AA–host link formatter card
- NT6X79AA–common peripheral controller equipment (CPCE) tone generator card
- NT6X92BB–universal tone receiver card

Design

The parts of the NT6X12AD appear in the following table.

NT6X12AD parts (Sheet 1 of 2)

PEC	Slot	Description
NT0X50AA	24F	*Filler faceplate* The filler faceplate fills empty card slots in the card fills.
NT6X44AA	15F	*Time switch card* The time switch converts between the serial stream and the parallel stream. The DS30 interface card or DS-1 interface card sends or receives the serial stream. The parallel stream is in use on the internal speech bus. The signaling processor (SP) can contros the time switch. In this event, the switch also associates any DS30 interface cards and DS-1 interface cards with any time slots on the parallel speech bus. This switch also transfers data between the associated channel and the time slot.
NT6X46AC	12F	*Signaling processor memory card* The signaling processor memory (SPM) card consists of random access memory. The random access memory stores data and software applications.
NT6X47AB	11F	*Master processor memory plus card* The master processor memory (MPM) card consists of RAM. The RAM stores data and software applications for both the master processor (MP) and the SP. The SP has access to a section of the MP memory using the memory management unit.
NT6X69AA	17F	*CPP message protocol card* The messaging card provides interface for the parallel speech bus. This card extracts control messages received on channel zero from the control module.

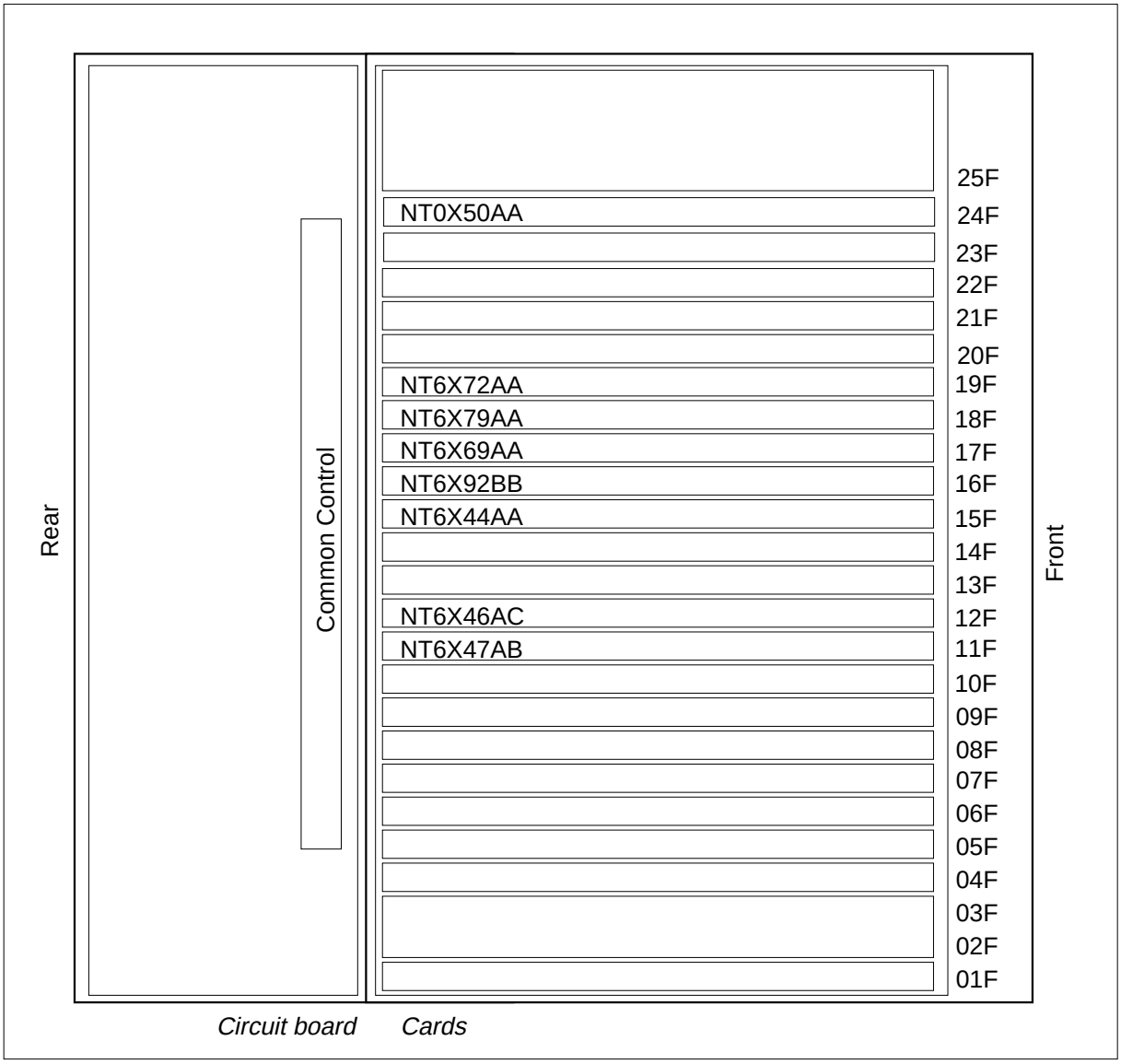
NT6X12AD (continued)

NT6X12AD parts (Sheet 2 of 2)

PEC	Slot	Description
NT6X72AA	19F	*Host link formatter card* The NT6X72AA host link formatter card provides the following: • RPCM serial-to-parallel conversion • XPCM parallel-to-serial conversion • network message interface • shelf clock generation • raw T1 clock generation • SP interface
NT6X79AA	18F	*CPCE tone generator card* The NT6X79AA CPCE tone generator card provides tones like reorder and busy.
NT6X92BB	16F	*Universal tone receiver card* The UTR is a 32-channel tone receiver that detects many tones. These tones include dual-tone multifrequency (DTMF). The time switch switches tone samples onto the parallel speech bus. The UTR collects the tone samples at correct time slots. The UTR analyzes the samples and identifies the tones. The XPM processor receives the results.

The design of the NT6X12AD appears in the following figure.

NT6X12AD parts



NT6X12AE

Product description

The NT6X12AE remote cluster controller (RCC) common circuit pack fill is used in Remote Switching Centers (RSC). An RSC enables a line trunk controller (LTC) and the peripheral module associated with the LTC to function from a remote site. A peripheral module an RCC hosts can function a maximum of 161 km (100 mi) away from the host central office.

The RCC common circuit pack (CP) fill is an LTC that stands alone in a remote location. The connections between the host LTC allow direct communication between the RCC and the central control (CC). As a result, most of the CC/LTC call processing software can be used in CC/RCC call processing. The RCC common CP fill provides a master controller for all units at the RSC. The host LTC controls the RCC common CP fill. The RCC is a two-shelf peripheral module. The RCC uses many of the same parts as an LTC.

Parts

The NT6X12AE remote cluster control common CP fill consists of the following parts:

- NT0X50AA–filler faceplate
- NT6X44AA–time switch card
- NT6X46BA–signaling processor memory plus card
- NT6X47AB–master processor memory plus card
- NT6X69AA–common peripheral processor (CPP) message protocol card
- NT6X72AA–host link formatter card
- NT6X79AA–common peripheral controller equipment (CPCE) message protocol card
- NT6X92BB–universal tone receiver (UTR) card

Design

The parts of the NT6X12AE appear in the following table.

NT6X12AE parts (Sheet 1 of 3)

PEC	Slot	Description
NT0X50AA	24F	*Filler faceplate* The filler faceplate fills empty card slots in the CP fills.

NT6X12AE (continued)

NT6X12AE parts (Sheet 2 of 3)

PEC	Slot	Description
NT6X44AA	15F	*Time switch card* The time switch converts between the serial stream and the parallel stream. The DS30 interface card or DS-1 interface card sends or receives the serial stream. The parallel stream is in use on the internal speech bus. When the signaling processor (SP) controls the time switch, this switch also associates the DS30 interface cards and DS-1 interface cards with any time slots on the parallel speech bus. The switch transfers data between the associated channel and the time slot.
NT6X46BA	12F	*Signaling processor memory plus card* The SPM plus card consists of random access memory. This memory stores data and software applications.
NT6X47AB	11F	*Master processor memory plus card* The MPM card consists of RAM. The RAM stores data and software applications for both the master processor (MP) and the SP. The memory management unit of the SP allows the SP access to a section of the MP memory.
NT6X69AA	17F	*CPP message protocol card* The messaging card provides interface for the parallel speech bus. This card extracts control messages received on channel zero from the control module.
NT6X72AA	19F	*Host link formatter card* The NT6X72AA host link formatter card provides the following: • RPCM serial-to-parallel conversion • XPCM parallel-to-serial conversion • network message interface • shelf clock generation • raw T1 clock generation • SP interface

NT6X12AE (continued)

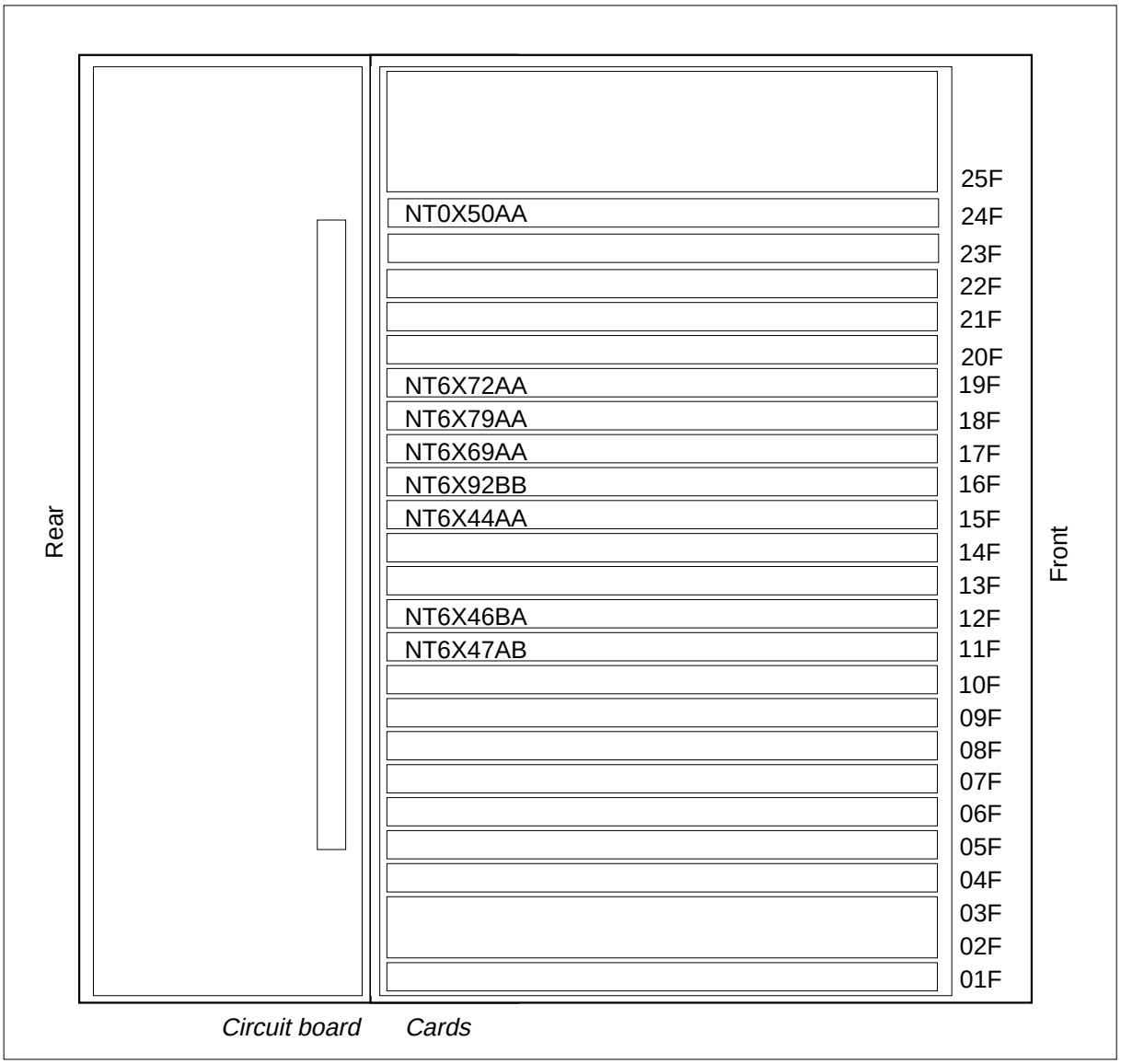
NT6X12AE parts (Sheet 3 of 3)

PEC	Slot	Description
NT6X79AA	18F	*CPCE tone generator card* The NT6X79AA CPCE tone generator card provides tones like reorder and busy.
NT6X92BB	16F	*Universal tone receiver card* The UTR is a 32-channel tone receiver that detects many tones. These tones include dual-tone multifrequency (DTMF). The time switch switches tone samples onto the parallel speech bus. The UTR collects these samples at correct time slots. The UTR analyzes the samples and identifies the tones. The XPM processor receives the results.

The design of the NT6X12AE appears in the following figure.

NT6X12AE (end)

NT6X12AE parts



NT6X12AF

Product description

The NT6XRAE Remote Switching Centers (RSC) use NT6X12AF the remote cluster controller (RCC) common circuit pack. An RSC enables a line trunk controller (LTC) and the associated peripheral module to function from a remote site. A peripheral that an RCC hosts can function a maximum of 161 km (100 mi) away from the host central office.

The RCC common circuit pack (CP) is an LTC that stands alone in a remote location. The connections between the host LTC allow direct communication between the RCC and the central control (CC). As a result, most of the CC/LTC call processing software can be used in CC/RCC call processing. The RCC common CP provides a master controller for all units at the RSC. The host LTC controls the RCC common CP. The RCC is a two-shelf peripheral module that uses many of the same parts as an LTC.

Parts

The NT6X12AF remote cluster control common circuit pack consists of the following parts:

- NT0X50AA–filler faceplate
- NT6X44AA–time switch card
- NT6X46AC–signaling processor memory card
- NT6X47AB–master processor memory plus card
- NT6X69AB–common peripheral processor (CPP) message protocol and tones card
- NT6X72AA–host link formatter card
- NT6X92BB–universal tone receiver (UTR) card

Design

The parts of the NT6X12AF appear in the following table.

NT6X12AF parts (Sheet 1 of 3)

PEC	Slot	Description
NT0X50AA	24F	*Filler faceplate* The filler faceplate fills empty card slots in the CP fills.

NT6X12AF (continued)

NT6X12AF parts (Sheet 2 of 3)

PEC	Slot	Description
NT6X44AA	15F	*Time switch card* The time switch converts between the serial stream and the parallel stream. The DS30 interface card or DS-1 interface card sends or receives this parallel stream. The parallel stream is in use on the internal speech bus. The signaling processor (SP) can control the time switch. In this event, the time switch also associates any DS30 interface cards and DS-1 interface cards with any time slots on the parallel speech bus. The time switch transfers data between the associated channel and the time slot.
NT6X46AC	12F	*Signaling processor memory card* The signaling processor memory (SPM) card consists of random access memory. This memory stores data and software applications.
NT6X47AB	11F	Master processor memory plus card The master processor memory (MPM) plus card consists of RAM. The RAM stores data and software applications for both the master processor (MP) and the SP. The memory management unit of the SP allows the SP to access a section of the MP memory.
NT6X69AB	17F	*CPP message protocol and tones card* The messaging card provides interface for the parallel speech bus. This card extracts control messages received on channel zero from the control module. This card also provides tones, like reorder and busy.

NT6X12AF (continued)

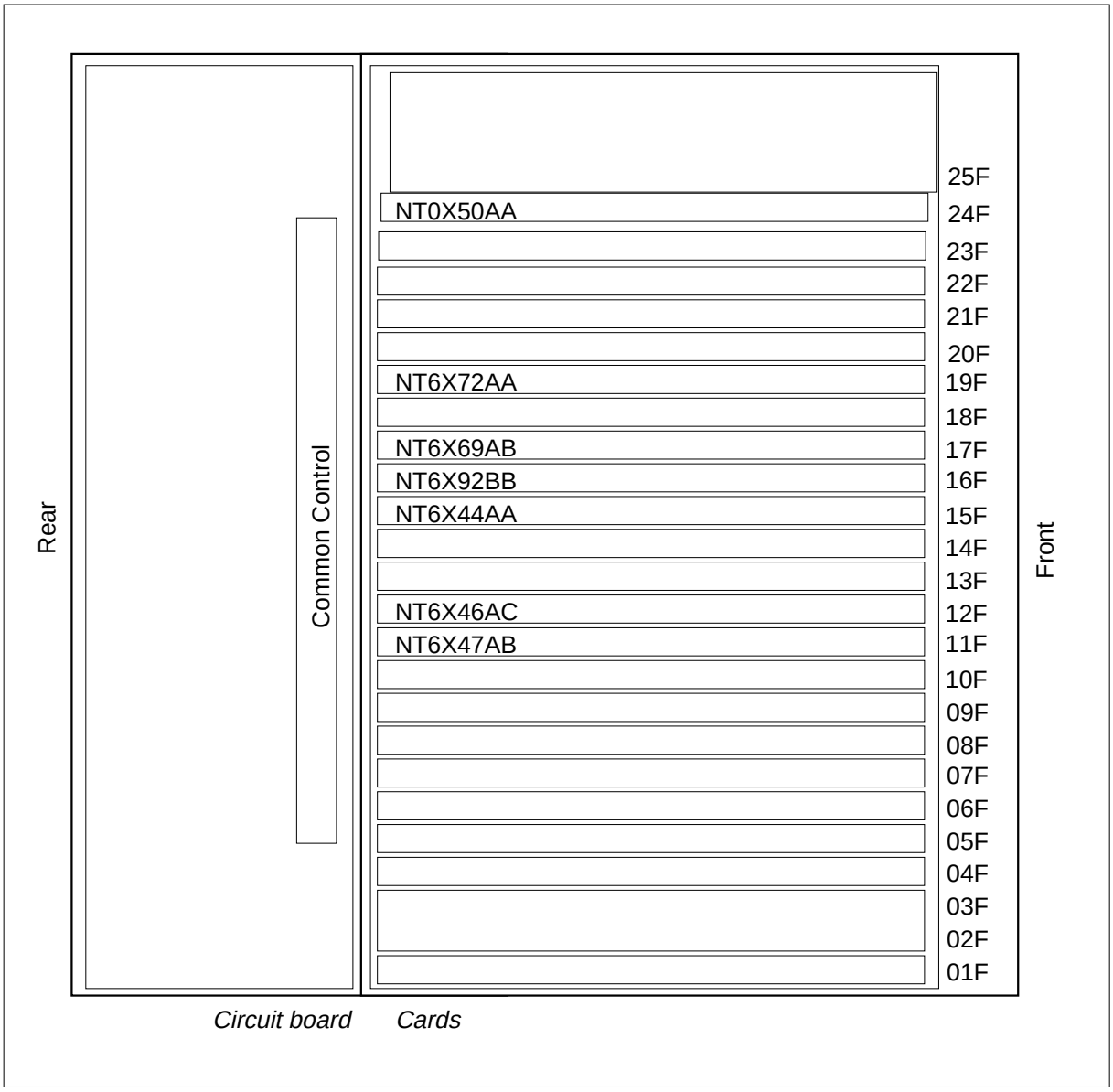
NT6X12AF parts (Sheet 3 of 3)

PEC	Slot	Description
NT6X72AA	19F	*Host link formatter card* The NT6X72AA host link formatter card provides the following: • RPCM serial-to-parallel conversion • XPCM parallel-to-serial conversion • network message interface • raw T1 clock generation • SP interface
NT6X92BB	16F	*Universal tone receiver* The UTR is a 32-channel tone receiver that detects many tones. These tones include the dual-tone multifrequency (DTMF). The time switch switches tone samples onto the parallel speech bus. The UTR collects these samples at the correct time slots. The UTR analyzes the samples and identifies the tones. The XPM processor receives the results.

The design of the NT6X12AF appears in the following figure.

NT6X12AF (end)

NT6X12AF parts



NT6X12AG

Product description

The NT6X12AG remote cluster controller (RCC) common circuit pack fill is used in Remote Switching Centers (RSC). An RSC enables a line trunk controller (LTC) and the associated peripheral module to function from a remote site. A peripheral module an RCC hosts can function a maximum of 161 km (100 mi) away from the host central office.

The RCC common circuit pack (CP) is an LTC that stands alone in a remote location. The connections between the host LTC allow direct communication between the RCC and the central control (CC). As a result, most of the CC/LTC call processing software can be used in CC/RCC call processing. The RCC common CP provides a master controller for all units at the RSC. The host LTC controls the RCC common CP. The RCC is a two-shelf peripheral module that uses many of the same components as an LTC.

Parts

The NT6X12AG remote cluster control common CP consists of the following parts:

- NT0X50AA–filler faceplate
- NT6X44AA–time switch card
- NT6X46BB–signaling processor memory card
- NT6X47AC–4-MB master processor memory plus card
- NT6X72AB–host link formatter card
- NT6X92BB–universal tone receiver (UTR) card

Design

The parts of the appear in the following table.

NT6X12AG parts (Sheet 1 of 3)

PEC	Slot	Description
NT0X50AA	9F, 10F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the CP fills.

NT6X12AG (continued)

NT6X12AG parts (Sheet 2 of 3)

PEC	Slot	Description
NT6X44AA	15F	*Time switch card* The time switch converts between the serial stream and the parallel stream. The DS30 interface card or DS-1 interface card sends or receives the serial stream. The parallel stream is in use on the internal speech bus. The signaling processor can control the time switch. In this event, the switch also associates the DS30 interface cards and DS-1 interface cards with the time slots on the parallel speech bus. This switch transfers data between the associated channel and the time slot.
NT6X46BB	12F	*Signaling processor memory card* The signaling processor memory (SPM) card consists of random access memory (RAM). This RAM stores data and software applications.
NT6X47AC	11F	*4-MB master processor memory plus card* The master processor memory (MPM) plus card consists of RAM. This RAM stores data and software applications for both the master processor (MP) and the signaling processor (SP). The memory management unit of the SP allows the SP access to a section of the MP memory.
NT6X72AB	19F	*Host link formatter card* The NT6X72AB host link formatter card provides the following; • RPCM serial-to-parallel conversion • XPCM parallel-to-serial conversion • network message interface • shelf clock generation • raw T1 clock generation • SP interface

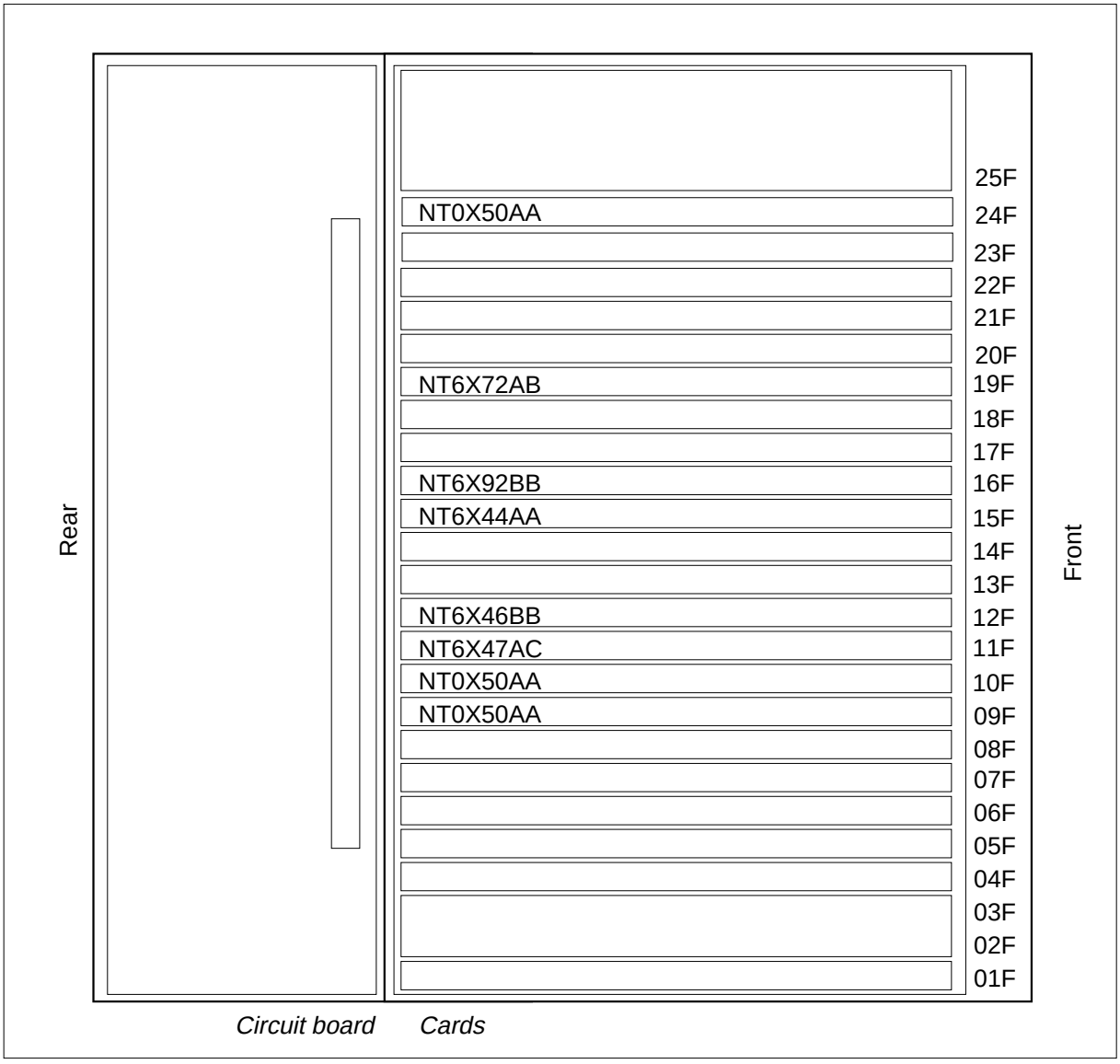
NT6X12AG (continued)

NT6X12AG parts (Sheet 3 of 3)

PEC	Slot	Description
NT6X92BB	16F	*Universal tone receiver card* The UTR is a 32-channel tone receiver that detects many tones. These tones include dual-tone multifrequency (DTMF). The time switch switches tone samples onto the parallel speech bus. The UTR collects these samples at the correct time slots. The UTR analyzes the samples and identifies the tones. The XPM processor receives the results.

The design of the appears in the following figure.

NT6X12AG parts



NT6X12CA

Product description

The NT6X12CA remote cluster controller (RCC) common circuit pack fill is used in Remote Switching Centers (RSC). An RSC enables a line trunk controller (LTC) and the associated peripheral module to function from a remote site. A peripheral module an RCC hosts can function a maximum of 161 km (100 mi) away from the host central office.

The RCC common circuit pack (CP) is an LTC that stands alone in a remote location. The connections between the host LTC allow direct communication between the RCC and the central control (CC). As a result, most of the CC/LTC call processing software can be used in CC/RCC call processing. The RCC common CP provides a master controller for all units at the RSC. The host LTC controls this RCC common CP. The RCC is a two-shelf peripheral module that uses many of the same components as an LTC.

Parts

The NT6X12CA remote cluster control common CP fill consists of the following parts:

- NT0X50AA–filler faceplate
- NT6X44AA–time switch card
- NT6X45BA–signaling processor memory plus card
- NT6X47AB–master processor memory plus card
- NT6X69AB–common peripheral processor (CPP) message protocol and tones card
- NT6X72AA–host link formatter card
- NT6X92BB–universal tone receiver (UTR) card

Design

The parts of the NT6X12CA appear in the following table.

NT6X12CA parts (Sheet 1 of 3)

PEC	Slot	Description
NT0X50AA	24F	*Filler faceplate* The filler faceplate fills empty card slots in the CP fills.

NT6X12CA (continued)

NT6X12CA parts (Sheet 2 of 3)

PEC	Slot	Description
NT6X44AA	15F	*Time switch card* The time switch converts between the serial stream and the parallel stream. The DS30 interface card or DS-1 interface card sends or receives the serial stream. The parallel stream is in use on the internal speech bus. The signaling processor can control the time switch. In this event, the switch also associates any of the DS30 interface cards and DS-1 interface cards with any of the time slots on the parallel speech bus. The switch transfers data between the associated channel and the time slot.
NT6X45BA	12F	*Signaling processor memory plus card* The signaling processor memory (SPM) card consists of random access memory (RAM). The RAM stores data and software applications.
NT6X47AB	11F	*Master processor memory plus card* The master processor memory (MPM) plus card consists of RAM. This RAM stores data and software applications for both the master processor (MP) and the signaling processor (SP). The memory management unit of the SP allows the SP access to a part of the MP memory.
NT6X69AB	17F	*CPP message protocol and tones card* The messaging CP provides interface for the parallel speech bus. This CP extracts control messages received on channel zero from the control module. This circuit pack also provides tones, like reorder and busy.

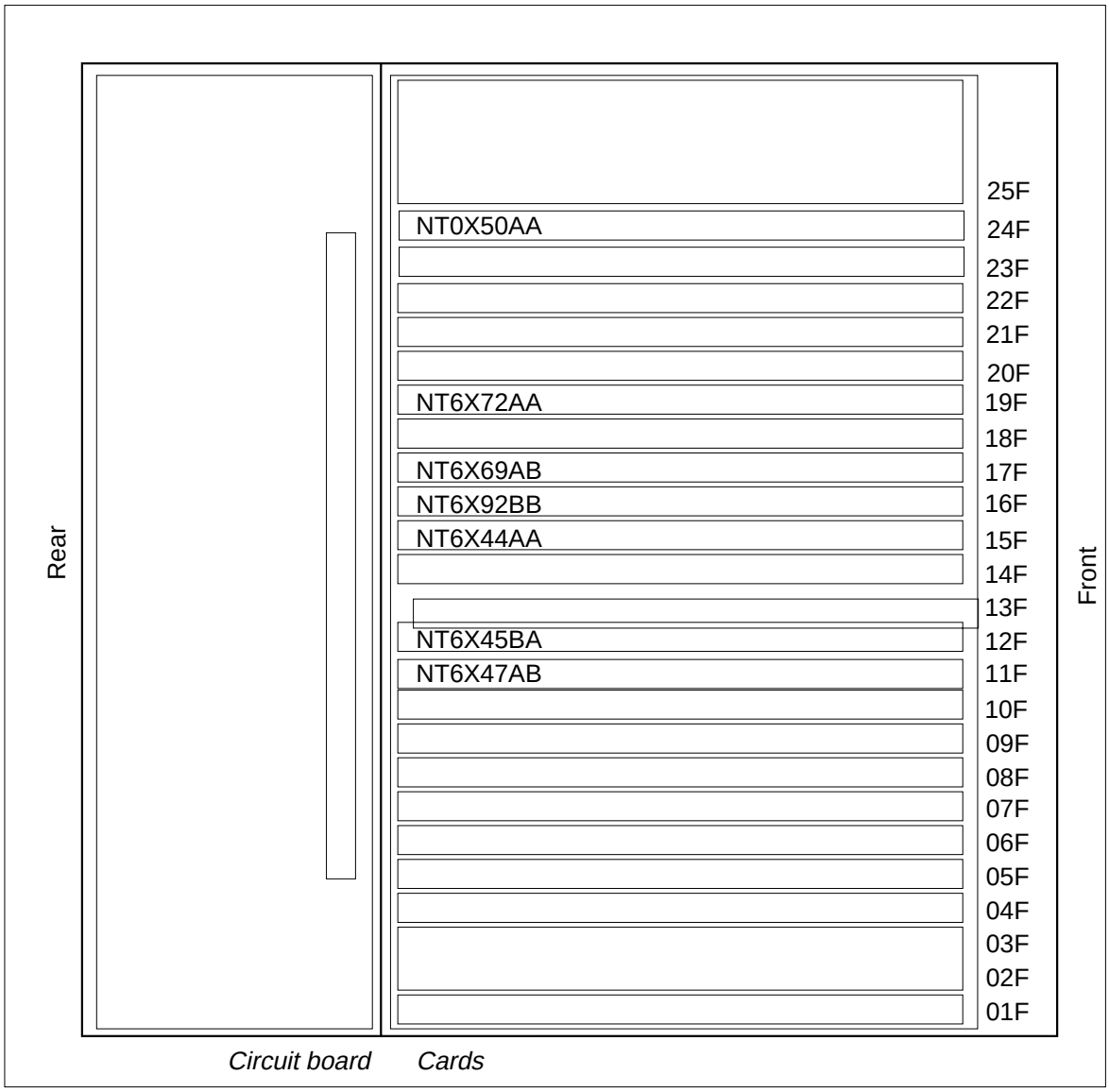
NT6X12CA (continued)

NT6X12CA parts (Sheet 3 of 3)

PEC	Slot	Description
NT6X72AA	19F	*Host link formatter card* The NT6X72AA host link formatter card provides the following: • RPCM serial-to-parallel conversion • XPCM parallel-to-serial conversion • network message interface • shelf clock generation • raw T1 clock generation • SP interface
NT6X92BB	16F	*Universal tone receiver card* The UTR is a 32-channel tone receiver that detects many tones. These tones include dual-tone multifrequency (DTMF). The time switch switches tone samples onto the parallel speech bus. The UTR collects these samples at the correct time slots. The UTR analyzes the samples and identifies the tones. The XPM processor receives the results.

The design of the NT6X12CA appears in the following figure.

NT6X12CA parts



NT6X12DA

Product description

The NT6X12DA ISDN remote cluster controller (RCC) common circuit pack fill is used in Remote Switching Centers (RSC). An RSC enables a line trunk controller (LTC) and the associated peripheral module to function from a remote site. A peripheral module an RCC hosts can function a maximum of 161 km (100 mi) away from the host central office.

The RCC common circuit pack (CP) is an LTC that stands alone in a remote location. The connections between the host LTC allow direct communication between the RCC and the central control (CC). As a result, most of the CC/LTC call processing software can be used in CC/RCC call processing. The RCC common circuit pack provides a master controller for all units at the RSC. The host LTC controls the RCC common circuit pack. The RCC is a two-shelf peripheral module that uses many of the same components as an LTC.

Parts

The NT6X12DA ISDN remote cluster control common CP consists of the following parts:

- NT0X50AA–filler face plate
- NT6X44AA–time switch card
- NT6X45BC– line group controller/digital trunk controller (LGC/DTC) processor card
- NT6X46BA–signaling processor memory plus card
- NT6X47AB–master processor memory plus card
- NT6X50AB–DS-1 extended frame format (EFF) card
- NT6X69AB–common peripheral processor (CPP) message protocol and tones card
- NT6X72AB–host link formatter card
- NT6X92BB–universal tone receiver (UTR) card
- NTBX01AA–ISDN signaling preprocessor card

Design

The parts of the NT6X12DA appear in the following table.

NT6X12DA parts (Sheet 1 of 3)

PEC	Slot	Description
NT0X50AA	9F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the CP fills.
NT6X44AA	15F	*Time switch card* The time switch converts between the serial stream and the parallel stream. The DS30 interface card or DS-1 interface card sends or receives the serial stream. The parallel stream is in use on the internal speech bus. The signaling processor can control the time switch. In this event, the switch associates any of the DS30 interface cards and DS-1 interface cards with any of the time slots on the parallel speech bus. This switch also transfers data between the associated channel and the time slot.
NT6X45BC	8F, 13F	*LGC/DTC processor card* The NT6X45BC LGC/DTC is a Motorola 68000-based processor card. This card is for use in most extended multiprocessor (XMS)-based peripheral modules (XPM) of the DMS-100. This card is not for use with applications that require the NT6X45CA. The external bus structure conforms with the XMS address bus (A-bus) interface specification.
NT6X46BA	12F	*Signaling processor memory plus card* The SPM plus card consists of random access memory used to store data and software applications.

NT6X12DA (continued)

NT6X12DA parts (Sheet 2 of 3)

PEC	Slot	Description
NT6X47AB	10F, 11F	*Master processor memory plus card* The MPM plus card consists of RAM. The RAM stores data and software applications for both the master processor and the signaling processor. The memory management unit of the signaling processor allows the signalling processor access to a section of the MP memory.
NT6X50AB	20F	*DS-1 extended frame format card* The DS-1 EFF card provides a 2-way voice, data, and signaling interface between the common peripheral controller (CPC) and one 2-way port. The CPC is in the DMS-100 and the 2-way port is in standard DS-1 systems. The card contains two circuits that perform separate, but by the same method.
NT6X69AB	17F	*CPP message protocol and tones card* The messaging card provides interface for the parallel speech. This card extracts control messages received on channel zero from the control module. This card also provides tones, like reorder and busy.
NT6X72AB	19F	*Host link formatter card* The NT6X72AB host link formatter card provides the following: • RPCM serial-to-parallel conversion • XPCM parallel-to-serial conversion • network message interface • shelf clock generation • raw T1 clock generation • signaling processor (SP) interface

NT6X12DA (continued)

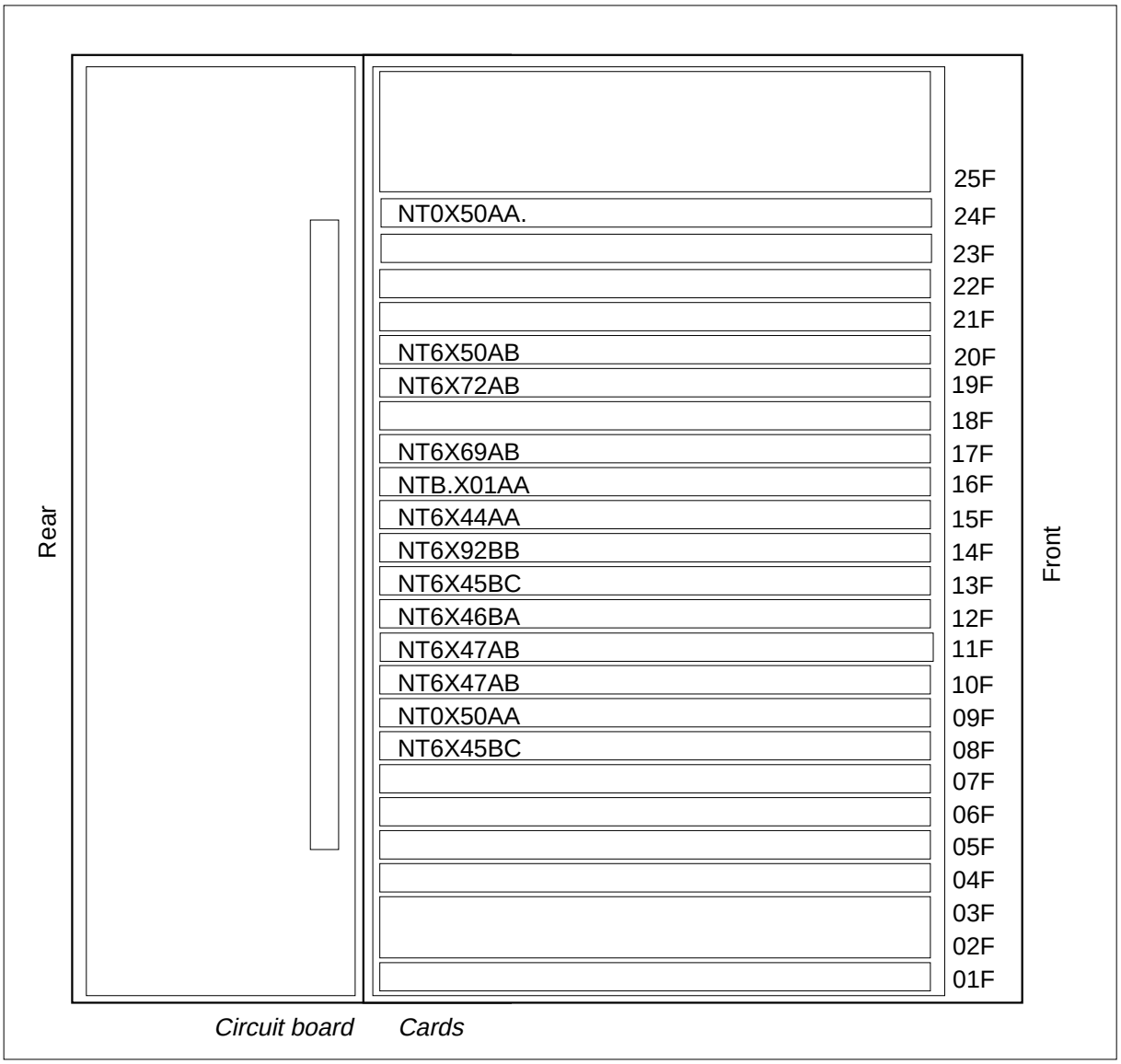
NT6X12DA parts (Sheet 3 of 3)

PEC	Slot	Description
NT6X92BB	14F	*Universal tone receiver* The UTR is a 32-channel tone receiver that detects many tones. These tones include dual-tone multifrequency (DTMF). The time switch switches tone samples onto the parallel speech bus. The UTR collects these samples at the correct time slots. The UTR analyzes the samples and identifies the tones. The XPM processor receives the results.
NTBX01AA	16F	*ISDN signaling preprocessor* The ISDN signaling preprocessor (ISP) card provides interface to both the SP and the speech bus. The NTBX01AA terminates a single messaging link for each D-channel handler (DCH), and processes layer-3 information. The ISP sends the signaling information that the DCH extracts to the master processor (MP).

The design of the NT6X12DA appears in the following figure.

NT6X12DA (end)

NT6X12DA parts



NT6X12DB

Product description

The Remote Switching Centers (RSC) uses the NT6X12DB offshore remote cluster controller (RCCO) common circuit pack fill. An RSC allows a line trunk controller (LTC) and the associated peripheral module to function from a remote site. A peripheral module that an RCCO hosts can function from a maximum of 161 km (100 mi) from the host central office.

The offshore RCC common circuit pack (CP) is an LTC that stands alone in a remote location. The connections between the host LTC allow direct communication between the RCCO and the central control (CC). This condition allows the CC/RCC call processing to use most of the CC/LTC call processing software. The offshore RCC common circuit pack provides a master controller for all units at the RSC. The host LTC controls the offshore RCC common circuit pack. The RCCO is a dual-shelf peripheral module that uses many of the same parts as an LTC.

Parts

The NT6X12DB RCCO common circuit pack fill contains the following parts:

- NT0X50AA–filler faceplate
- NT6X27AC–PCM-30 trunk interface card
- NT6X44EA–time switch card
- NT6X45BC–line group controller/digital trunk controller (LGC/DTC) processor card
- NT6X46BA–signaling processor memory plus card
- NT6X47AC–4-MB master processor memory plus card
- NT6X69LA–common peripheral processor (CPP) message protocol card
- NT6X72BA–host link formatter card
- NT6X92CA–universal tone receiver (UTR) card
- NTBX01AA–ISDN signaling preprocessor card

NT6X12DB (continued)

Design

The parts of the NT6X12DB appear in the following table.

NT6X12DB parts (Sheet 1 of 3)

PEC	Slot	Description
NT0X50AA	9F, 11F, 18F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the CP.
NT6X27AC	20F	*PCM-30 trunk interface card* The NT6X27AC PCM-30 trunk interface card is like the NT6X27AB. The NT6X27AC is grounded in a different method. On the AA and AB versions, the outside ring of the coaxial cable grounds to the logic ground. On the AC version, the outer ring grounds to the frame ground. The AA card does not require the peripheral-side (P-side) looparound on the inactive side. Versions AB and AC do not have the P-side looparound. The NT6X27AC provides an interface between new DMS-100 peripherals and standard PCM-30 plant equipment. The card accepts common channel or channel-associated signaling techniques according to CCITT recommendation G.732. The card translates between one internal dual port multiplexed DS60 signal and two external PCM-30 lines. The card inverts each even bit automatically. The duplicated DS60 system interface contains embedded control data.

NT6X12DB parts (Sheet 2 of 3)

PEC	Slot	Description
NT6X44EA	15F	*Time switch card* The time switch (TS) converts between the serial and the parallel stream. The switch receives the serial stream from, or transmits the serial stream to the DS30 or DS-1 interface card. The internal speech bus uses the parallel stream. When the signaling processor controls the time switch, the switch compares the DS30 interface cards and DS-1 interface cards. The switch compares these cards with the time slots on the parallel speech bus. The switch transfers data between the associated channel and the time slot.
NT6X45BC	8F, 13F	*LGC/DTC processor card* The NT6X45BC LGC/DTC processor card is a Motorola 68000-based processor card. All extended multiprocessor (XMS)-based peripheral modules (XPM) of the DMS-100 use this card. Applications that require the NT6X45CA do not use this card. The external bus structure conforms with the XMS address bus (A-bus) interface specification.
NT6X46BA	12F	*Signaling processor memory plus card* The SPM plus card contains random access memory that stores data and software applications.
NT6X47AC	10F	*Master processor memory plus card* The MP memory plus card provides dynamic RAM (DRAM) to extended multiprocessor system (XMS)-based peripheral modules (XPM). The NT6X47AC does not require two NT6X47AB cards. The NT6X47AC reduces power use. The NT6X47AC allows a minimum of 2 MB of MP memory in emergency stand-alone (ESA) and message switch and buffer (MSB7) XPMs.

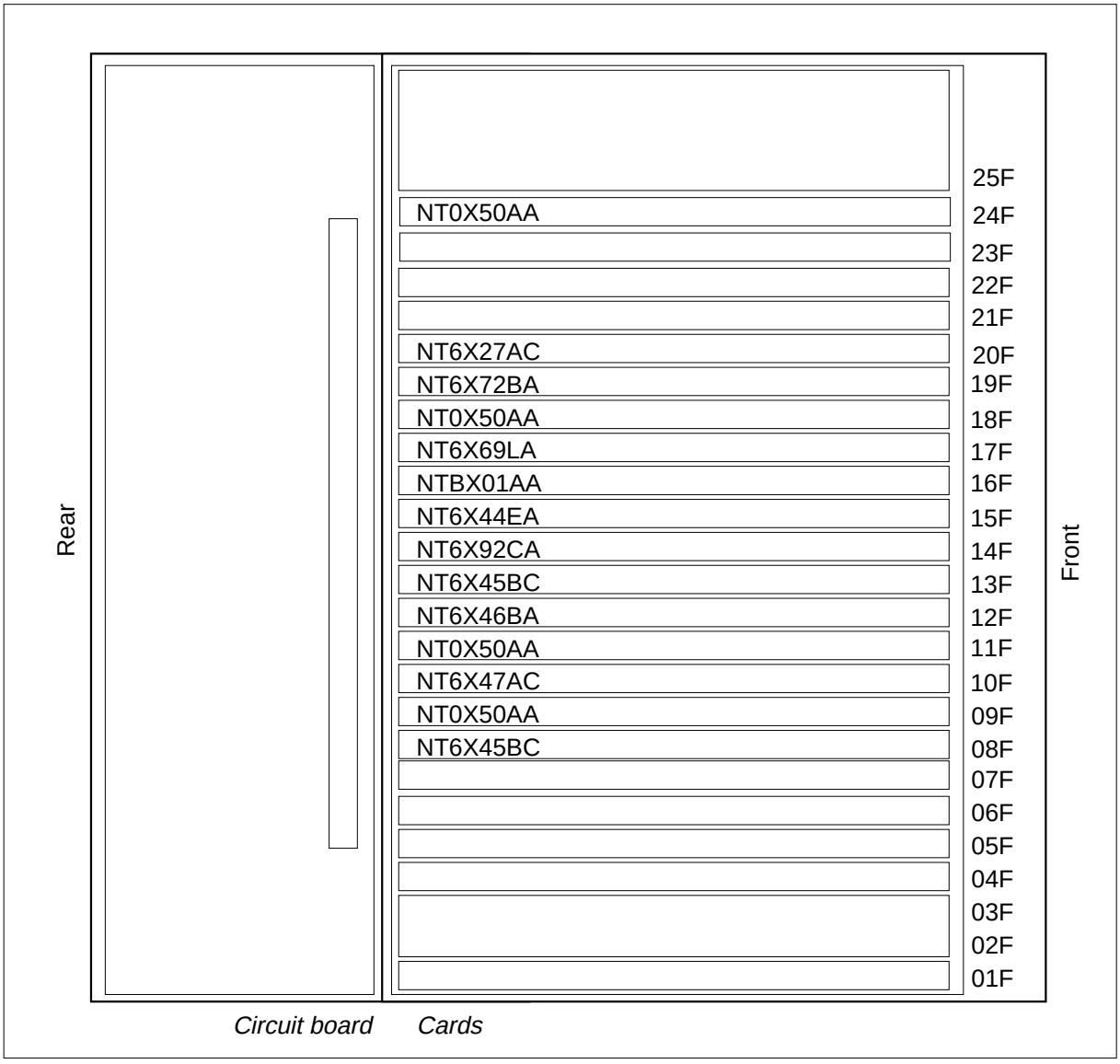
NT6X12DB (continued)

NT6X12DB parts (Sheet 3 of 3)

PEC	Slot	Description
NT6X69LA	17F	*CPP message protocol card* The messaging card provides interface for the parallel speech bus. This card also removes control messages received on channel zero from the control module.
NT6X72BA	19F	*Host link formatter card* The NT6X72BA host link formatter card provides RPCM serial-to-parallel conversion and XPCM parallel-to-serial conversion. This card provides network message interface, shelf clock generation, raw T1 clock generation, and signaling processor (SP) interface.
NT6X92CA	14F	*Universal tone receiver card* The UTR is a 32-channel tone receiver that detects different tones that include dual-tone multifrequency (DTMF). The time switch switches tone samples to the parallel speech bus. The UTR collects tone samples at correct time slots. The UTR analyzes the samples and identifies the tones. The UTR sends the results to the XPM processor.
NTBX01AA	16F	*ISDN signaling preprocessor card* The ISDN signaling preprocessor (ISP) card provides interface to both the signaling processor (SP) and the speech bus. The NTBX01AA terminates a single messaging link for each D-channel handler (DCH), and processes layer-3 information. The DCH removes the signaling information. The ISP sends this information to the MP.

The design of the NT6X12DB appears in the following figure.

NT6X12DB Parts



NT6X12DC

Product description

The Remote Switching Centers (RSC) use the NT6X12DC integrated services digital network (ISDN) remote cluster controller (RCC) common circuit pack fill. An RSC allows a line trunk controller (LTC) and the associated peripheral module to function from a remote site. A peripheral module that an RCC hosts can function a maximum of 161 km (100 mi) from the host central office.

The RCC common circuit pack (CP) is an LTC that stands alone in a remote location. The connections between the host LTC allow direct communication between the RCC and the central control (CC). This condition allows the CC/RCC call processing to use most of the CC/LTC call processing software. The RCC common circuit pack provides a master controller for all units at the RSC. The host LTC controls the RCC common circuit pack. The RCC is a dual-shelf peripheral module that uses many of the same parts as an LTC.

Parts

The NT6X12DC remote cluster controller common circuit pack fill contains the following parts:

- NT0X50AA–filler face plate
- NT6X44AA–time switch card
- NT6X45BC–line group controller/digital trunk controller (LGC/DTC) processor card
- NT6X50AB–DS-1 extended frame format (EFF) card
- NT6X72AB–host link formatter card
- NT6X92BB–universal tone receiver (UTR) card
- NTBX01AA–ISDN signaling preprocessor card

Design

The parts of the NT6X12DC appear in the following table.

NT6X12DC parts (Sheet 1 of 3)

PEC	Slot	Description
NT0X50AA	9F, 24F	*Filler faceplate* The filler faceplate fills empty card slots in the CP.

NT6X12DC (continued)

NT6X12DC parts (Sheet 2 of 3)

PEC	Slot	Description
NT6X44AA	15F	*Time switch card* The time switch converts between the serial stream and the parallel stream. The switch receives serial stream from, or transmits serial stream to the DS30 or DS-1 interface card. The internal speech bus uses the parallel stream. When the signaling processor controls the time switch, the switch associates the DS30 and DS-1 interface cards with the time slots on the parallel speech bus. The switch also transfers data between the associated channel and the time slot.
NT6X45BC	8F, 13F	*LGC/DTC processor card* The NT6X45BC LGC/DTC is a Motorola 68000-based processor card. All extended multiprocessor (XMS)-based peripheral modules (XPM) of the DMS-100 use this card. Applications that require the NT6X45CA do not use this card. The external bus structure applies to the XMS address bus (A-bus) interface requirements.
NT6X50AB	20F	*DS-1 EFF card* The DS-1 EFF card provides a 2-way voice, data, and signaling interface between the common peripheral controller (CPC) in the DMS-100. This card also provides one 2-way port in standard DS-1 systems. The card contains two circuits that perform in the same method but separate of each other.
NT6X72AB	19F	*Host link formatter card* The NT6X72AB host link formatter card provides RPCM serial-to-parallel conversion and XPCM parallel-to-serial conversion. This card also provides network message interface, shelf clock generation, raw T1 clock generation, and signaling processor (SP) interface.

NT6X12DC (continued)

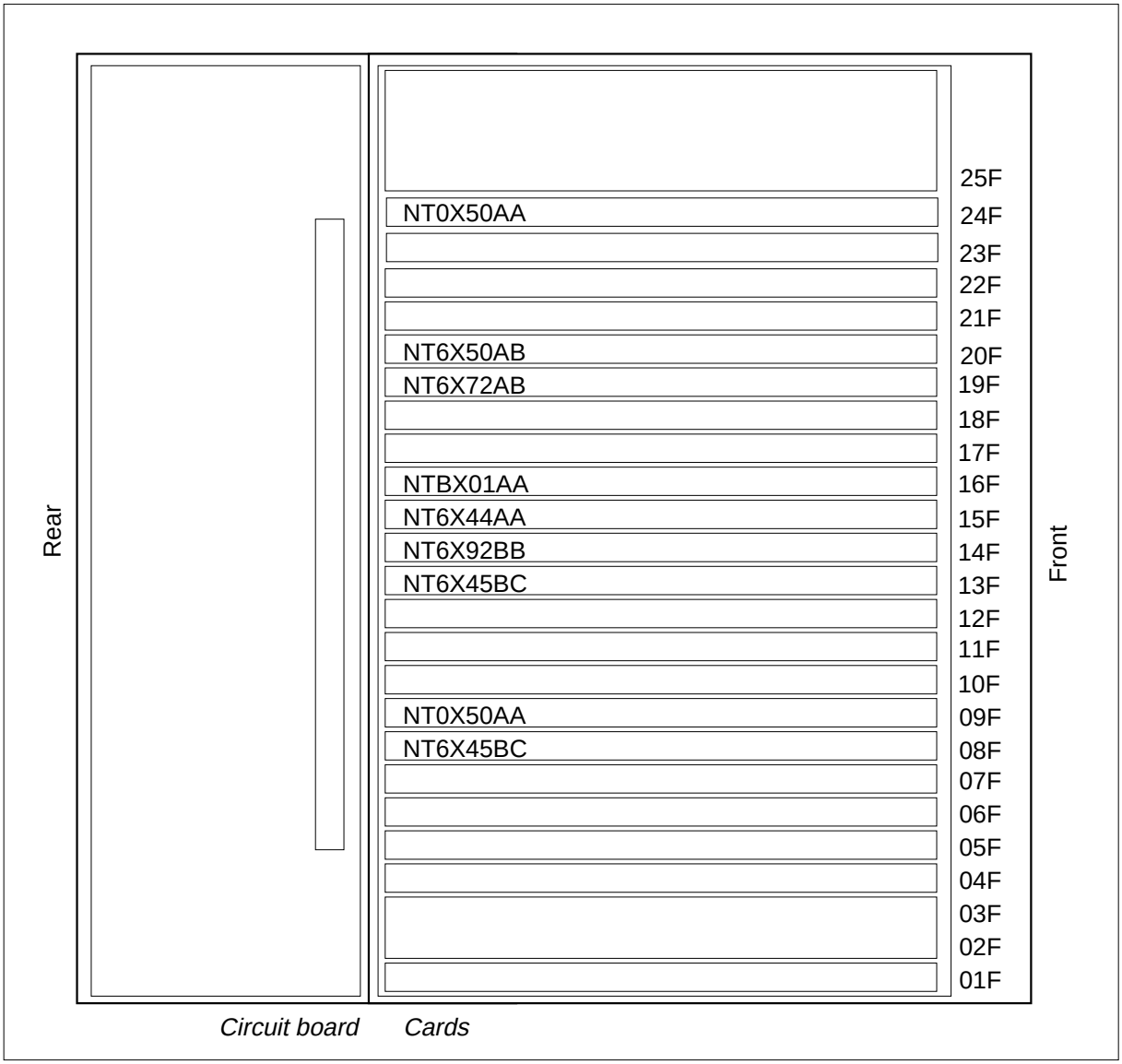
NT6X12DC parts (Sheet 3 of 3)

PEC	Slot	Description
NT6X92BB	14F	*Universal tone receiver card* The UTR is a 32-channel tone receiver that detects different tones that include dual-tone multifrequency (DTMF). The time switch moves tone samples to the parallel speech bus. The UTR collects tone samples at appropriate time slots. The UTR analyzes the samples and identifies the tones. The UTR sends the results to the XPM processor.
NTBX01AA	16F	*ISDN signaling preprocessor card* The ISDN signaling preprocessor (ISP) card provides interface to both the SP and the speech bus. The NTBX01AA terminates one messaging link for each D-channel handler (DCH), and processes layer-3 information. The DCH removes the signaling information. The ISP sends this information to the master processor.

The design of the NT6X12DC appeasr in the following figure.

NT6X12DC (end)

NT6X12DC parts



NT6X13AA

Product description

The remote maintenance module (RMM) shelf (NT6X13AA) is a modified version of the maintenance trunk module (MTM) (NT2X58) shelf. The NT6X13AA provides maintenance and operational support for remote offices connected to a DMS-100 central office. Use of the shelf can occur in the following frames:

- remote line concentrating module (RLCM) (NT6X14AA) frames
- outside plant module (OPM) frames (NT8X01AA and NT8X01AB)
- remote controller equipment (RCE) frames (NT6X10AC) in a remote switching center (RSC)

The shelf supports the following features:

- metallic test access (MTA)
- incoming/outgoing test trunks
- line test units (LTUs)
- scan and signal distribution (SD) points
- digitone receivers if the emergency stand-alone (ESA) option is included

The RMM shelf contains the following parts:

- control circuit card (NT6X74AA)
- group coder-decoder (CODEC) and tone circuit card (NT2X59AA)
- two power converters (NT2X06AB and NT6X09AA)
- a maximum of 14 service circuit cards. Office requirements determine the types of cards.

Some of the service cards used in the RMM are for MTA functions.

RLCM and OPM operation

When the RMM is in an RLCM or an OPM, the RMM decreases the amount of traffic on the DS-1 links. An example of this condition occurs when an OPM is an RLCM in an environmentally controlled cabinet. The RMM allows the line control module (LCM) (NT6X04) in the RLCM or OPM to test and service circuit cards at the remote site. The DS30A links connect C-side interface of the RMM shelf to each of the two line control cards (LCC) (NT6X50AA) in the host interface shelf (HIE) (NT6X11). The RMM connects to both LCCs to make sure that the shelf continues to operate if one LCC is active. If the RLCM does not include the ESA option, a minimum of one RLCM at a remote site can share one RMM. If the RLCM does not include the

ESA option, each RLCM must have a specified RMM. In addition, the RMM must include a digitone receiver card.

The selection and test of a line circuit and the display of test results occurs through the DS30A links. The DS30A links to the LCC and from the LCC to the host office. All test procedures follow the maintenance administration position (MAP) as described in the *DMS-100 Menu Commands Reference Manual* (297-1001-801).

RSC operation

When the RMM is at a remote switching center, the RMM provides test trunks, service circuits, and alarm circuits for the RSC. The RSC supports the RMM as a separate node off of the P-side of the remote cluster controller (RCC) (NT6X12AB). The RMM functions as a stand-alone peripheral for messaging and maintenance. Two RSCs can share an RMM if the RSCs connect to the same host. An RSC and an RLCM at the same location can share an RMM when the RLCM is not equipped for ESA operation.

The line trunk controller (LTC) (NT6X02) or line group controller (LGC) (NT6X02) of the host office communicates with the RMM. The LTC or LGC of the NT6X02 communicate with the RMM at an RSC through the DS-1 link to the RCC. The LTC or LGC of the NT6X02 communicate with the RMM at an RCC through the DS30A link.

Parts

The RMM shelf contains the following parts:

- NT6X74AA–Control circuit card
- NT2X59AA–Group CODEC and tone circuit card
- NT2X06AB–Power converter
- NT2X09AA–Power converter
- Service circuit cards

Service circuit cards

The international RMM shelf can have the following service cards:

- NT3X09AA–Remote metallic test access card
- NT0X10AA–Miscellaneous scan card
- NT2X55AA, NT2X57AA–Signal distribution card
- NT2X10AA–Analog line test unit
- NT2X11AA–Digital line test unit

NT6X13AA (continued)

- NT2X48AA–Multifrequency (MF) receiver card
- NT2X48AB–Digitone receiver card
- NT2X90–Incoming/outgoing test trunk card
- NT3X04AA–Incoming test trunk card
- NT3X82, NT3X83AA–Office alarm unit (OAU) circuit card

Design

The design of the NT6X13AA appears in the following table. The service circuit cards in use depends on the application of the shelf.

NT6X13AA parts (Sheet 1 of 4)

PEC	Slot	Description
NT0X10AA	13F	*Miscellaneous scan card* The miscellaneous scan card (NT0X10AA) detects external alarms like the aisle alarm on a frame supervisory panel (FSP). This card sends the information to the host office. The card monitors the condition of contacts at the remote site. The card sends the information to the host office through the service shelf interface card, the remote line controller (RLC), and the DS-1 message channel.
NT2X06AB	20F	*Power converter* The NT2X06AB produces a 5-V, 40-A output. The NT2X06AB includes low-voltage monitor circuits, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.
NT2X09AA	17F,18F	*Power converter* The NT2X09AA converter produces -5V, -15V, +5V, +12V, and +24V dc. The NT2X09AA includes low-voltage monitor circuits, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate LED status indicator.

NT6X13AA (continued)

NT6X13AA parts (Sheet 2 of 4)

PEC	Slot	Description
NT2X10AA	7F	*Analog line test unit* The analog (NT2X10AA) and digital (NT2X11AA) LTUs function together and appear side by side in card slots. The analog LTU is in an odd-numbered slot. The digital LTU is in an even-numbered slot. Both cards provide test conditions to test line circuits. The RLC controls both LTUs through the service shelf interface card.
NT2X11AA	8F	*Digital line test unit* The analog (NT2X10AA) and digital (NT2X11AA) LTUs function together and appear side by side in card slots. The analog LTU is in an odd-numbered slot. The digital LTU is in an even-numbered slot. Both cards provide test conditions for testing line circuits. The RLC controls both LTUs through the service shelf interface card.
NT2X48AA	9F, 10F	*Multifrequency (MF) receiver card* The digital four-channel MF receiver (NT2X48AA) and the digitone receiver (NT2X48AB) cards detect and decode tones in pulse-code-modulation (PCM) data. The NT2X48AA and NT2X48AB monitor a maximum of four channels and generate 8-bit binary codes to indicate the received tones.
NT2X48AB	9F, 10F	*Digitone receiver card* The digital four-channel MF receiver (NT2X48AA) and the digitone receiver (NT2X48AB) cards detect and decode tones in PCM data. The NT2X48AA and NT2X48AB monitor a maximum of four channels and generate 8-bit binary codes to indicate the received tones.

NT6X13AA (continued)

NT6X13AA parts (Sheet 3 of 4)

PEC	Slot	Description
NT2X57AA	15F	*Signal distribution card* The signal distribution card (NT2X57AA) functions as an interface. This card is an interface between digital circuits in the RLM and a maximum of 14 external, relay-controlled devices at the remote site. A message from the CM at the host office can activate any relay in the SD card. The activation messages reach the SD card through the DS-1 message channel, digroup 19 of the RLC, and the service shelf interface card. The NT2X57AA SD card is like the NT2X55AA SD card but contains small, flat-spring, board-mounted relays. These relays are for applications that require lower output contact ratings and resistive loads.
NT2X59AA	1F	*Group CODEC and tone circuit card* The group CODEC and tone circuit card (NT2X59AA) encodes analog samples from the RLCM lines to PCM code words. The card decodes PCM samples from the host to analog samples. The card generates the digital tones required for dialing and signaling.
NT2X90AB	4F-6F	*Incoming/outgoing test trunk card* The incoming/outgoing test trunk card (NT2X90) is normally next to an LTU pair. This card can accommodate one trunk circuit and functions as an interface between the RMM and different test units. These test units include the 14 local test desk (14 LTD), 3 local test cabinet (3 LTC), centralized automated loop reporting system (CALRS) test desk, mechanized loop tester (MLT). The incoming/outgoing test trunk card is required for MTA.

NT6X13AA (continued)

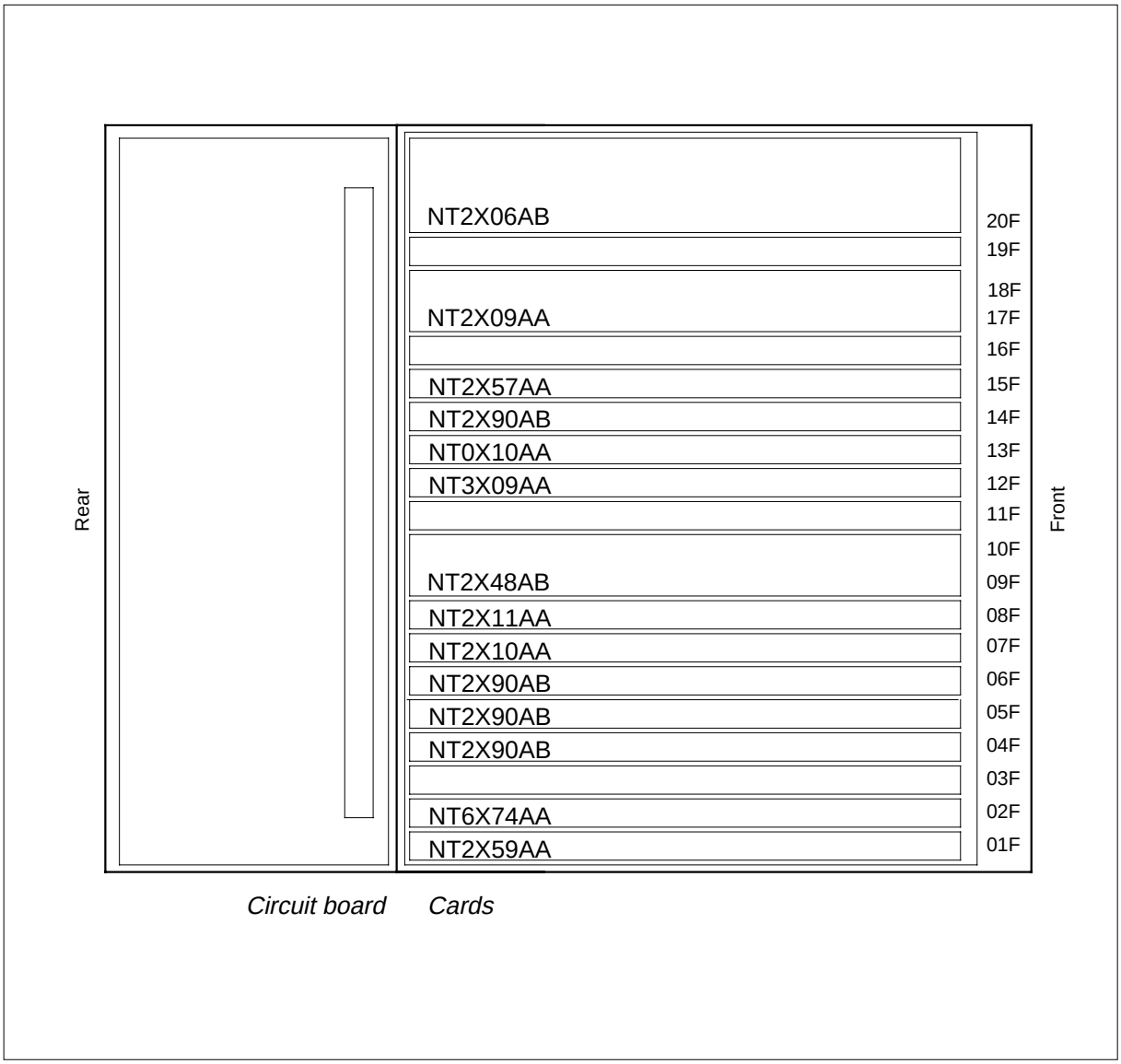
NT6X13AA parts (Sheet 4 of 4)

PEC	Slot	Description
NT3X09AA	12F	*Remote metallic test access card* The remote MTA card (NT3X09AA) provides metallic dc connections between test circuits and line circuits. Each remote MTA card can install four 2-wire paths at the same time.
NT6X74AA	2F	*Control circuit card* The control circuit card (NT6X74AA) functions as the link between the line control arrays (LCA) of the LCM and the test trunks, service circuits, and alarm circuits of the RMM. This card also processes DMSX messages, trunk messages, and PCM data.

The design of the NT6X13AA appears in the following figure. The design of accurate shelves can be different than the following figure.

NT6X13AA (end)

NT6X13AA parts



NT6X13AB

Product description

The NT6X13AB remote maintenance module (RMM) common circuit pack (CP) fill provides maintenance and operational support. The NT6X13AB provides this support for remote offices connected to a DMS-100 central office (CO). The RMM CP fill supports the following features:

- metallic test access (MTA)
- incoming-outgoing test trunks
- line test units (LTU)
- scan and signal distribution (SD) points
- digitone receivers when the available emergency stand-alone (ESA) is included

The RMM CP fill contains the following parts:

- an NT6X74AB control circuit card
- an NT2X59AA group coder-decoder (CODEC) circuit card
- an NT2X06AB power converter

In the Remote Line Concentrating Module (RLCM), the RMM reduces traffic on the DS-1 links. The RMM allows the line concentrating module (LCM) to test and service circuit cards at the remote site. The DS30A links connect the central-side (C-side) interface of the RMM CP fill to the two NT6X50AA line control cards in the host interface equipment (HIE) CP fill. This condition does not occur for the maintenance trunk module (MTM) common CP fill. The RMM connects to both line control cards (LCC) to make sure that the CP continues to operate when only one LCC is active. If the available ESA is not included, more than one RLCM can share a RMM at a remote site. If the ESA is included, each RLCM must have a specified RMM. The RMM must include a Digitone receiver card.

The selection and test of line circuits and the display of test results occur through DS30A links. The DS30A links to the LCC and from the LCC to the host office. All test procedures occur at the MAP (maintenance and administration position) terminal as described in the *Commands Reference Manual* , 297-1001-821.

In the NT6X14AA RLCM, the RMM common CP is assigned to shelf position 56. In the NT6X10AC remote controller equipment (RCE), the RMM common CP is assigned to shelf position 51 and position 65 if required. In the outside plant module (OPM), the RMM common CP assigns to shelf position 5. In the

NT6X13AB (continued)

remote control and maintenance equipment (RCME), the RMM common CP assigns to position 21.

Parts

The NT6X13AB RMM common CP fill contains the following parts:

- NT0X50AA–filler faceplate
- NT2X06AB–power converter common feature card
- NT2X09AA–multioutput power converter card
- NT2X59AA–group CODEC DMS100/200 card
- NT6X74AB–RMM control card

Design

The parts of the NT6X13AB appear in the following table.

NT6X13AB parts (Sheet 1 of 2)

PEC	Slot	Description
NT0X50AA	19F	*Filler faceplate* The filler faceplate occupies empty card slots in the CP fills.
NT2X06AB	20F	*Power converter common feature card* The NT2X06AB produces a 5-V, 40-A output. The NT2X06AB includes low-voltage monitor circuits, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.
NT2X09AA	17F	*Multioutput power converter card* The NT2X09AA power converter card produces dc voltages of -5, -15, +5, +12, and +24 V. The NT2X09AA includes low-voltage monitor circuits, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate LED status indicator.

NT6X13AB (continued)

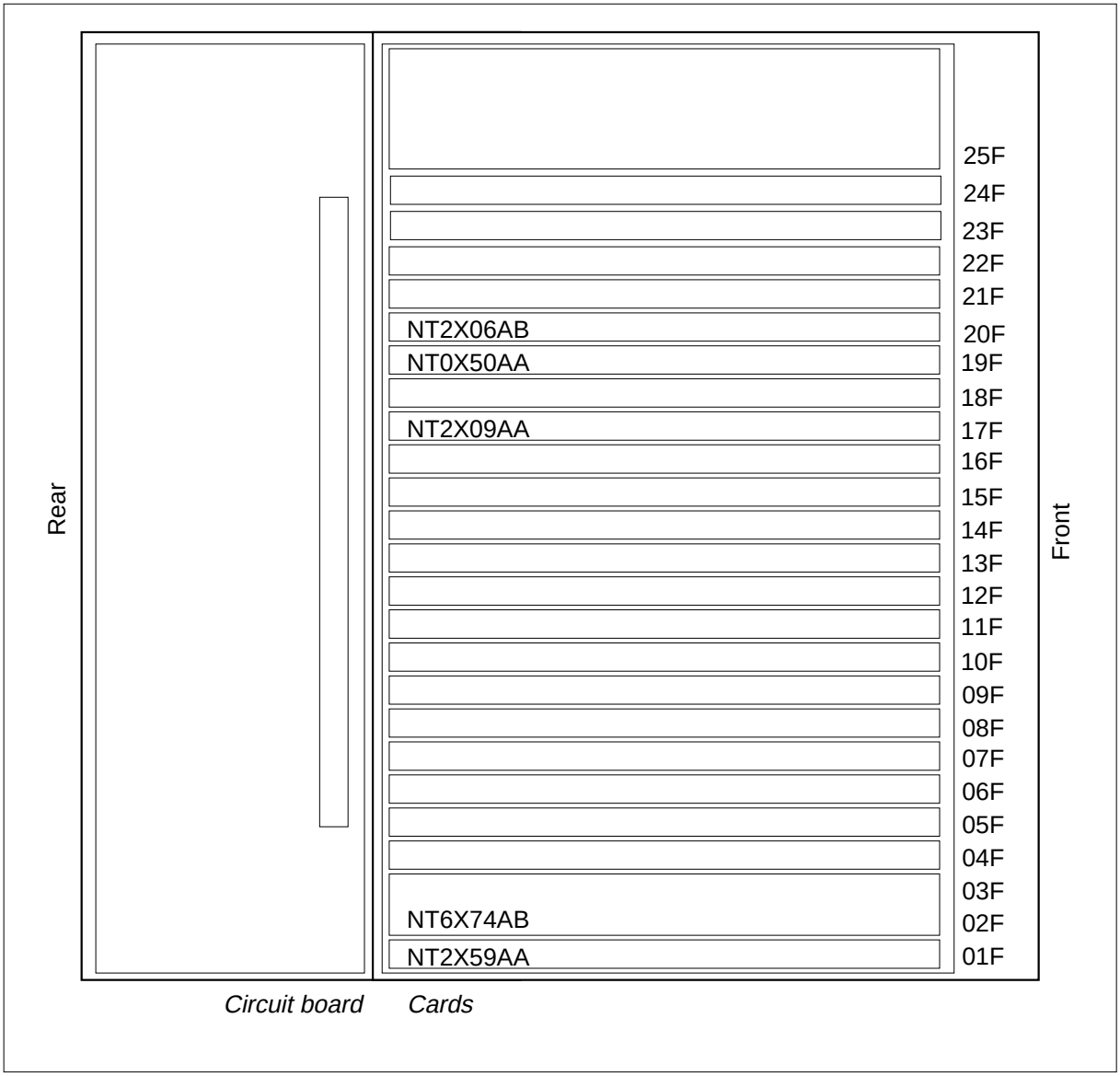
NT6X13AB parts (Sheet 2 of 2)

PEC	Slot	Description
NT2X59AA	1F	*Group CODEC DMS100/200 card* The NT2X59AA group CODEC DMS100/200 card encodes analog samples from the RLCM lines to pulse code modulation (PCM) words. This card decodes PCM samples from the host to analog samples. The card generates the digital tones required for dialing and signaling.
NT6X74AB	2F	*RMM control card* The NT6X74AB control circuit card functions as the link between the line control arrays (LCA) of the LCM and the test trunks, service circuits, and alarm circuits of the RMM. This card processes DMS-X messages, trunk messages, and PCM data.

The design of the NT6X13AB appears in the following figure.

NT6X13AB (end)

NT6X13AB parts



NT6X13BA

Product description

The NT6X13BA remote maintenance module (RMM) common fill is a modified version of the NT2X58 maintenance trunk module (MTM) fill. The NT6X13BA provides maintenance and operational support for remote offices connected to a DMS-100 central office. The RMM fill supports the following features:

- metallic test access (MTA)
- incoming and outgoing test trunks
- line test units (LTU)
- scan and signal distribution (SD) points
- Digitone receivers if the emergency stand-alone (ESA) option is included

The RMM fill contains the following:

- an NT6X74AB control card
- an NT2X59BA A-law CODEC and tones card
- a power converter (NT2X06AB)

In the Remote Line Concentrating Module (RLCM), the RMM decreases the traffic on the DS-1 links. The RMM allows the line concentrating module (LCM) to test and service cards at the remote site. The DS30A links connect the central-side (C-side) interface of the RMM fill to the two NT6X50AA line control cards in the host interface equipment (HIE) fill. The RMM connects to both line control cards (LCC) so the fill continues to operate when only one LCC is active. If the ESA is not included, more than one RLCM at a remote site can share a RMM. If ESA is included, each RLCM must have a specified RMM. The RMM must include a Digitone receiver card.

The selection and test of line circuits and the display of test results occur through DS30A links. The DS30A links to the LCC and from the LCC to the host office. All test procedures occur at the MAP (maintenance and administration position) terminal as described in the *Commands Reference Manual*, 297-1001-821.

Parts

The NT6X13BA RMM common fill contains the following parts:

- NT0X50AA–filler faceplate
- NT2X06AB–power converter common feature card
- NT2X09AA–multioutput power converter card

NT6X13BA (continued)

- NT2X59BA–A-law CODEC and tones card
- NT6X74AB–RMM control card

Design

The parts of the NT6X13BA appear in the following table.

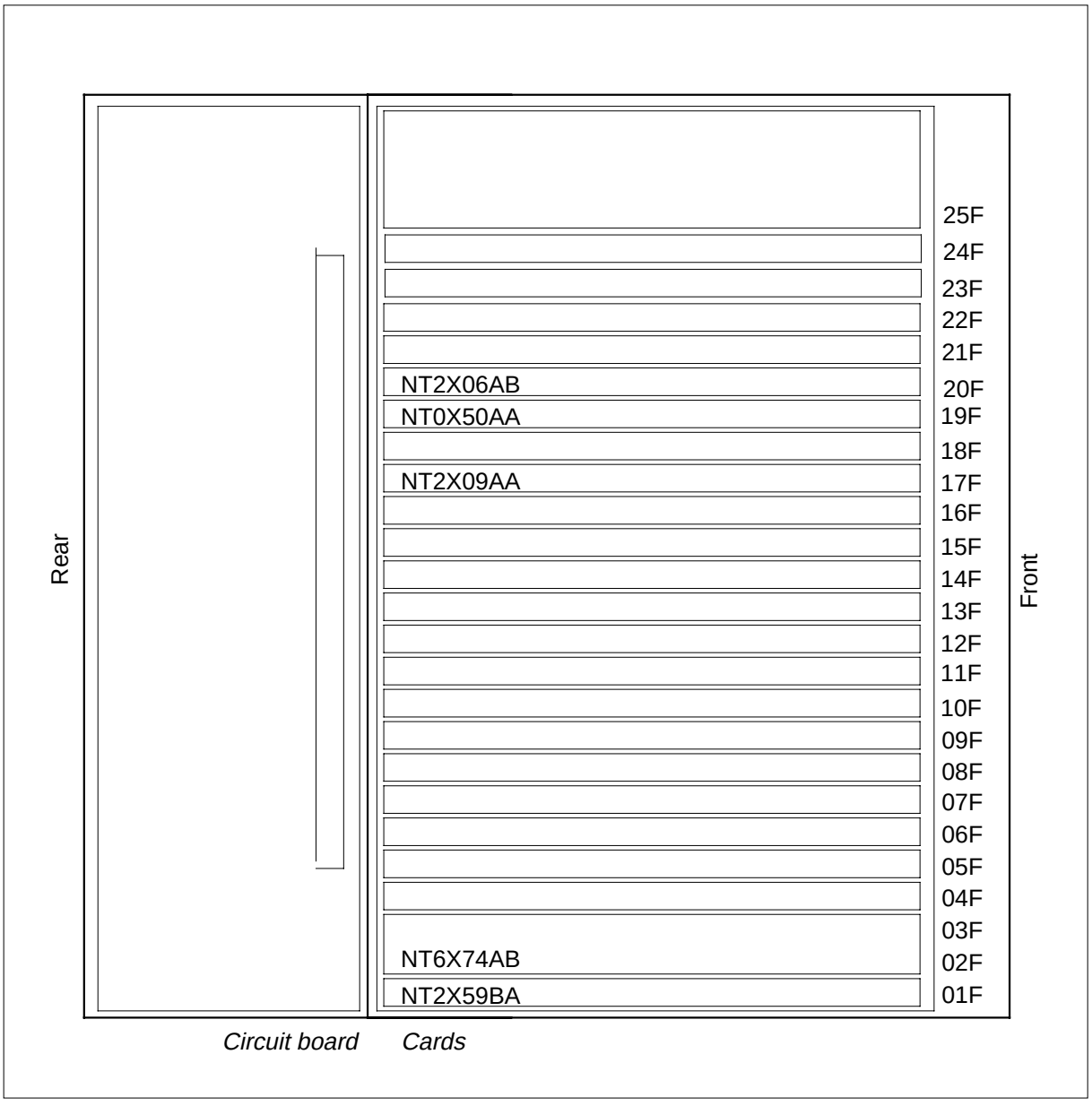
NT6X13BA parts

PEC	Slot	Description
NT0X50AA	19F	*Filler faceplate* The filler faceplate occupies empty card slots in the fills.
NT2X06AB	20F	*Power converter common feature card* The NT2X06AB produces a 5-V, 40-A output. The NT2X06AB includes low-voltage monitor circuits, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.
NT2X09AA	17F	*Multioutput power converter card* The NT2X09AA converter produces dc voltages of -5, -15, +5, +12, and +24 V. The NT2X09AA includes low-voltage monitor circuits, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate LED status indicator.
NT2X59BA	1F	*A-law CODEC and tones card* The NT2X59BA A-law CODEC and tones card encodes analog samples from the RLCM lines to pulse code modulation (PCM) words. The card decodes PCM samples from the host to analog samples. The card generates the digital tones required for dialing and signaling.
NT6X74AB	2F	*RMM control card* The NT6X74AB control card is the link between the line control arrays (LCA) of the LCM and the test trunks, service circuits, and alarm circuits of the RMM. This card processes DMS-X messages, trunk messages, and PCM data.

NT6X13BA (end)

The design of the NT6X13BA appears in the following figure.

NT6X13BA parts



NT6X13DA

Product description

The international remote maintenance module (RMM) shelf (NT6X13DA) is a modified version of the maintenance trunk module (MTM) (NT2X58) shelf. The NT6X13DA provides maintenance and operational support for remote offices connected to a DMS-100 central office. The shelf can function in the following frames:

- international remote line concentrating module (IRLCM) (NT6X14AA) frames
- international outside plant module (IOPM) frames (NT8X40AA)
- remote controller equipment (RCE) frames (NT6X10AC) in a remote switching center (RSC)

The NT6X13DA supports the following features:

- metallic test access (MTA)
- incoming/outgoing test trunks
- line test units (LTU)
- scan and signal distribution (SD) points
- digitone receivers if the emergency stand-alone (ESA) option is included

The international RMM shelf contains the following cards:

- control circuit card (NT6X74AA)
- group coder-decoder (CODEC) and tone circuit card (NT2X59AA)
- two power converters (NT2X06AB and NT6X09AA) cards
- a maximum of 14 service circuit cards. Office requirements determine the types of cards.

Some of the service cards used in the international RMM are for MTA functions.

RLCM and OPM operation

When the international RMM is in an IRLCM or an IOPM, the RMM decreases the traffic on the PCM30 links. An IOPM is a remote line concentrating module (RLCM) in an environmentally controlled cabinet. The RMM allows the line control module (LCM) (NT6X04) in the IRLCM or IOPM to test and service circuit cards at the remote site. The DS30A connects the C-side interface of the international RMM shelf to each of the two line control cards (LCC) (NT6X50AA) in the host interface shelf (HIE) (NT6X11). The international RMM connects to both LCCs so the shelf continues to

operate when only one LCC is active. If the ESA option is not included, more than one IRLCM at a remote site can share an international RMM. If the ESA option is included, each IRLCM must have a dedicated international RMM. This international RMM must include a digitone receiver card.

The selection and test of a line circuit and the display of test results occur through the DS30A links. The DS30A links to the LCC and from the LCC to the host office. All test procedures occur at the maintenance administration position (MAP).

RSC operation

When the RMM is at a remote switching center, the international RMM provides test trunks, service circuits, and alarm circuits for the RSC. The system supports the international RMM as a separate node off of the P-side of the remote cluster controller (RCC) (NT6X12AB). The RMM functions as a stand-alone peripheral for messaging and maintenance. Two RSCs can share an international RMM if the RSCs connect to the same host. An RSC and an RLCM can share an RMM at the same location if the RLCM is not equipped for ESA operation.

The common peripheral controller (CPC) (NT6X02) of the host office communicates with the international RMM at an RSC through the link to the RCC. The NT6X02 communicates with the international RMM through the DS30A link at the RCC.

Parts

The international RMM shelf contains the following parts:

- NT6X74AB–Control circuit card
- NT2X59DA–Group CODEC and tone circuit card
- NT2X06AB–Power converter
- NT2X09AA–Power converter
- Service circuit cards

Service circuit cards

The international RMM shelf can have the following service cards:

- NT3X09AA–Remote metallic test access card
- NT0X10AA–Miscellaneous scan card
- NT2X55AA, NT2X57AA–Signal distribution card
- NT2X10AA–Analog line test unit
- NT2X11AA–Digital line test unit

NT6X13DA (continued)

- NT2X48AA–Multifrequency (MF) receiver card
- NT2X48AB–Digitone receiver card
- NT2X90–Incoming/outgoing test trunk card
- NT3X04AA–Incoming test trunk card
- NT3X82AB, NT3X83AA–Office alarm unit (OAU) circuit card

Design

The design of the NT6X13DA appears in the following table. Service circuit cards used depend on the application of the NT6X13DA.

NT6X13DA parts (Sheet 1 of 4)

PEC	Slot	Description
NT0X10AA	13F	*Miscellaneous scan card* The miscellaneous scan card (NT0X10AA) detects external alarms like the aisle alarm on a frame supervisory panel (FSP). This card sends the information to the host office. The card monitors the condition of contacts at the remote site. The card sends the information to the host office through the service shelf interface card, the remote line controller (RLC), and the DS1 message channel.
NT2X06AB	20F	*Power converter* The NT2X06AB produces a 5-V, 40-A output. The NT2X06AB includes low-voltage monitor circuits, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.
NT2X09AA	17F,18F	*Power converter* The NT2X09AA converter produces -5V, -15V, +5V, +12V, and +24V dc. The NT2X09AA includes low-voltage monitor circuits, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate LED status indicator.

NT6X13DA (continued)

NT6X13DA parts (Sheet 2 of 4)

PEC	Slot	Description
NT2X10AA	7F	*Analog line test unit* The analog (NT2X10AA) and digital (NT2X11AA) LTUs function together and appear side by side in card slots. The analog LTU is in an odd-numbered slot. The digital LTU is in an even-numbered slot. Both cards provide test conditions to test line circuits. The RLC controls both cards through the service shelf interface card.
NT2X11AA	8F	*Digital line test unit* The analog (NT2X10AA) and digital (NT2X11AA) LTUs function together and appear side by side in card slots. The analog LTU is in an odd-numbered slot. The digital LTU is in an even-numbered slot. Both cards provide test conditions to test line circuits. The RLC controls both cards through the service shelf interface card.
NT2X48AA	9F, 10F	*Multifrequency receiver card* The digital four-channel MF receiver (NT2X48AA) and the digitone receiver (NT2X48AB) cards detect and decode tones in pulse-code- modulation (PCM) data. The NT2X48AA and NT2X48AB monitor a maximum of four channels and generate 8-bit binary codes to indicate the received tones.
NT2X48AB	9F, 10F	*Digitone receiver card* The digital four-channel MF receiver (NT2X48AA) and the digitone receiver (NT2X48AB) cards detect and decode tones in PCM data. The NT2X48AA and NT2X48AB monitor a maximum of four channels and generate 8-bit binary codes to indicate the received tones.

NT6X13DA (continued)

NT6X13DA parts (Sheet 3 of 4)

PEC	Slot	Description
NT2X57AA	15F	*Signal distribution card* The signal distribution card (NT2X57AA) functions as an interface. The card is an interface between digital circuits in the RLM and a maximum of 14 external, relay-controlled devices at the remote site. A message from the CM at the host office can activate any relay in the SD card. The activation messages reach the SD card through the DS1 message channel, digroup 19 of the RLC, and the service shelf interface card. The NT2X57AA SD card is like the NT2X55AA SD card but contains small, flat-spring, board-mounted relays. These ralys are for applications that require lower output contact ratings and resistive loads.
NT2X59AA	1F	*Group CODEC and tone circuit card* The group CODEC and tone circuit card (NT2X59AA) encodes analog samples from the RLCM lines to PCM code words. The card decodes PCM samples from the host to analog samples. The card generates the digital tones required for dialing and signaling.
NT2X90AB	4F-6F	*Incoming/outgoing test trunk card* The incoming/outgoing test trunk card (NT2X90) is normally next to two LTUs. This card can accommodate one trunk circuit. This card functions as an interface between the RMM and different test units. These test units include the14 local test desk (14 LTD), 3 local test cabinet (3 LTC), centralized automated loop reporting system (CALRS) test desk, and mechanized loop tester (MLT). The MTA feature requires the incoming/outgoing test trunk card.

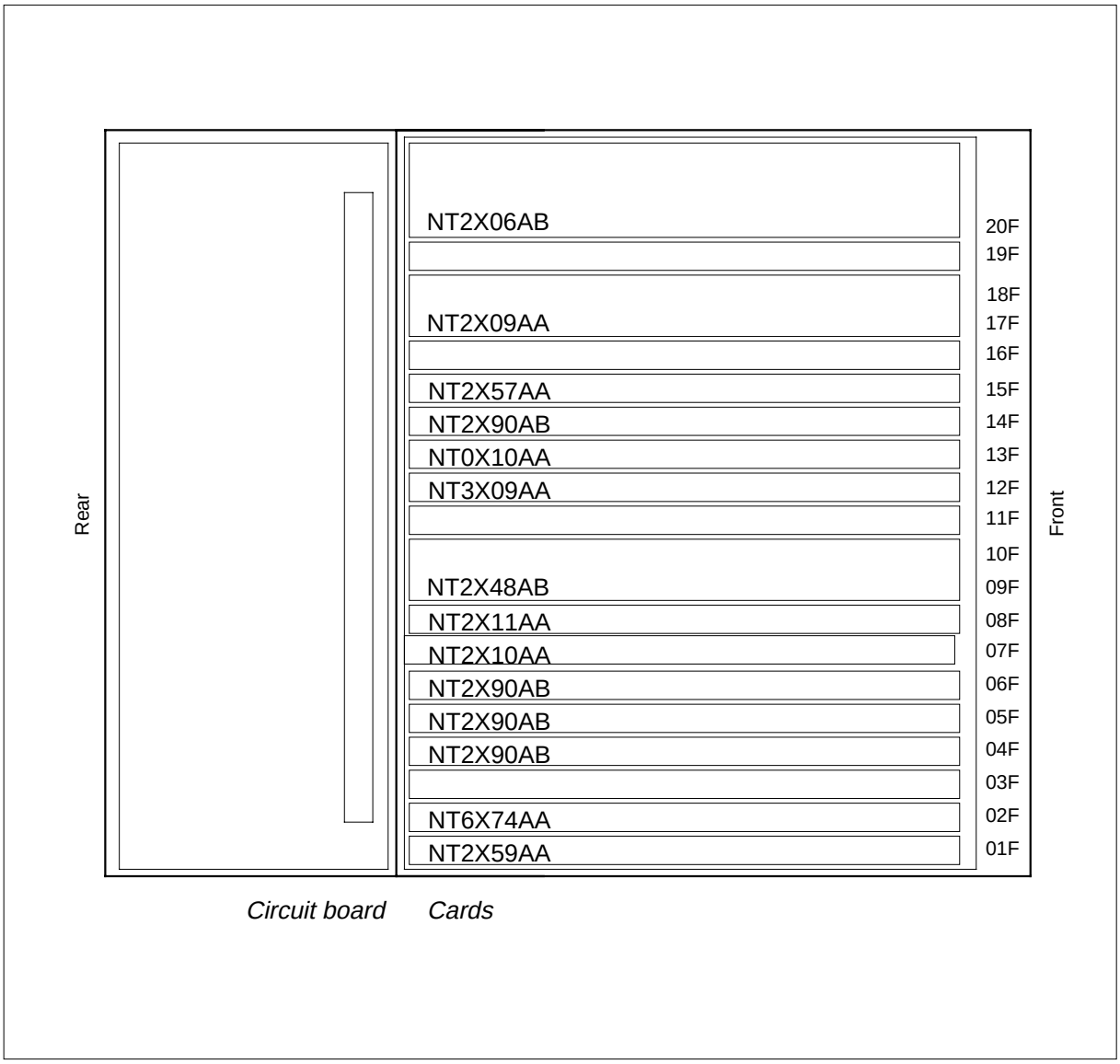
NT6X13DA parts (Sheet 4 of 4)

PEC	Slot	Description
NT3X09AA	12F	*Remote metallic test access card* The remote MTA card (NT3X09AA) provides metallic dc connections between test circuits and line circuits. Each remote MTA card can install four 2-wire paths at the same time.
NT6X74AA	2F	*Control circuit card* The control circuit card (NT6X74AA) functions as the link between the line control arrays (LCA) of the LCM and the test trunks, service circuits, and alarm circuits of the RMM. The card processes DMSX messages, trunk messages, and PCM data.

The design of the NT6X13DA appears in the following figure. The design of accurate shelves can be different from the design in the figure.

NT6X13DA (end)

NT6X13DA parts



NT6X13EA

Product description

The NT6X13EA remote maintenance module (RMM) common fill is a modified version of the NT2X58 maintenance trunk module (MTM) fill. The NT6X13EA provides maintenance and operational support for remote offices connected to a DMS-100 central office (CO). The RMM fill supports the following features:

- metallic test access (MTA)
- incoming/outgoing test trunks
- line test units (LTU)
- scan and signal distribution (SD) points
- Digitone receivers if the emergency stand-alone (ESA) option is included

The RMM fill contains the following:

- an NT6X74AB control card
- an NT2X59CA A-law TM CODEC and tones card
- a power converter (NT2X06AB)

In the Remote Line Concentrating Module (RLCM), the RMM decreases the traffic on the DS-1 links. The RMM allows the line concentrating module (LCM) to test and service cards at the remote site. The DS30A links connect the central-side (C-side) interface of the RMM fill to the two NT6X50AA line control cards in the host interface equipment (HIE) fill. The RMM connects to both line control cards (LCC) so the RMM operates when only one LCC is active. If the ESA option is not included, more than one RLCM at a remote site can share an RMM. If the ESA option is included, each RLCM must have a dedicated RMM. This RMM must include a Digitone receiver card.

The selection and test of line circuits and the display of test results occurs through DS30A links. The DS30A links to the LCC and from the LCC to the host office. All test procedures occur at the MAP (maintenance and administration position) terminal.

Parts

The NT6X13EA contains the following parts:

- NT0X50AA–filler faceplate
- NT2X06AB–power converter common feature card
- NT2X09AA–multi output power converter card

NT6X13EA (continued)

- NT2X59CA–A-law TM CODEC and tones card
- NT6X74AB–RMM control card

Design

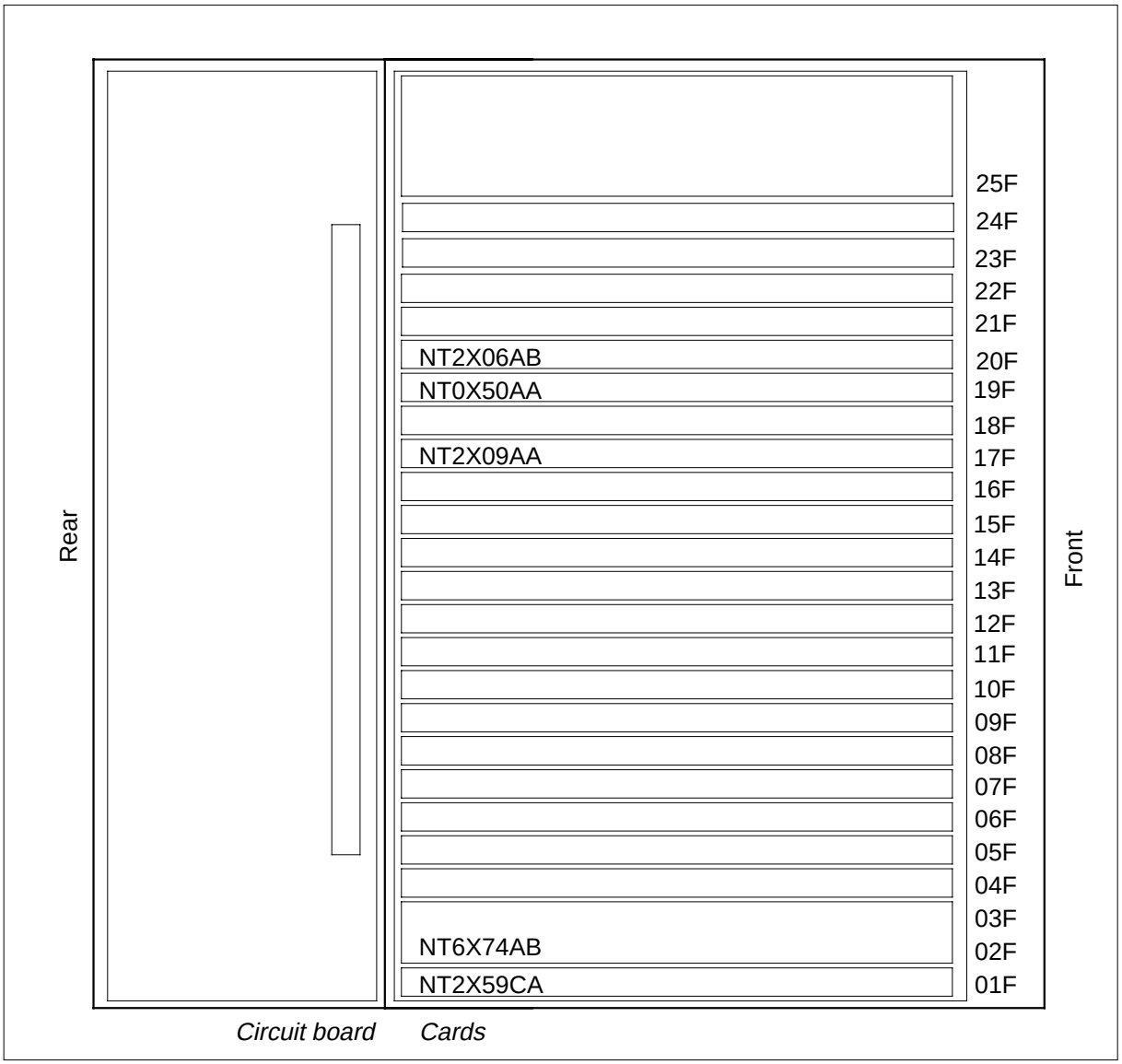
The parts of the NT6X13EA appear in the following table.

NT6X13EA parts

PEC	Slot	Description
NT0X50AA	19F	*Filler faceplate* The filler faceplate occupies empty card slots in the fills.
NT2X06AB	20F	*Power converter common feature card* The NT2X06AB produces a 5-V, 40-A output. The NT2X06AB includes low-voltage monitor circuits, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.
NT2X09AA	17F	*Multi output power converter card* The NT2X09AA converter produces dc voltages of -5, -15, +5, +12, and +24 V. The NT2X09AA includes low-voltage monitor circuits, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate LED status indicator.
NT2X59CA	1F	*A-law TM CODEC and tones card* The NT2X59CA A-law TM CODEC and tones card encodes analog samples from the RLCM lines to pulse code modulation (PCM) words. The card decodes PCM samples from the host to analog samples. The card generates the digital tones required for dialing and signaling.
NT6X74AB	2F	*RMM control card* The NT6X74AB control card is the link between the line control arrays (LCA) of the LCM and the test trunks, service circuits, and alarm circuits of the RMM. The card processes DMS-X messages, trunk messages, and PCM data.

The design of the NT6X13EA appears in the following figure.

NT6X13EA parts



NT6X14AA

Product description

The NT6X14AA remote line concentrating module (RLCM) contains the following parts. These parts connect a maximum of 640 subscriber lines to a common peripheral controller (CPC). The CPC connects to the central switch. The RLCM has the following parts:

- an NT6X04AA or NT6604BA line concentrating module (LCM)
- an NT6X11AA host interface equipment (HIE) shelf
- an NT6X13AA remote maintenance module (RMM)
- an NT6X25AA frame supervisory panel (FSP)

The central-side (C-side) of the LCM connects to the CPC through DS30A links. The CPC can be a line group controller (LGC), a line trunk controller (LTC), or a remote cluster controller (RCC). When the LCM receives instructions from the CPC, the LCM links a DS30A channel to a subscriber line. This link allows incoming and outgoing calls to complete. The LCM supports digital and analog lines. All signals between the RLCM and the CPC are digital. The LCM performs the digital-to-analog and analog-to-digital conversion. This conversion connects the CPC and the central switch to analog subscriber lines.

Parts

The RLCM contains the following parts:

- an NT6X04AA–line concentrating module (LCM)
- an NT6X04BA–line concentrating module (LCM)
- an NT6X11AA–host interface equipment (HIE) common circuit pack (CP) fill
- an NT6X13AA–remote maintenance module (RMM)
- an NT6X25AA–frame supervisory panel (FSP)

Line concentrating module

The NT6X14AA or NT6X04BA LCM has two single-shelf line concentrating arrays (LCA) designated LCA-0 and LCA-1. The LCA-0 is on the bottom. The LCA-1 is on the top. Each LCA includes a control complex that has an NT6X51AA LCM processor card and an NT6X52AA digroup control. The

control complex can handle both LCAs when one of the following conditions occurs:

- the LCM processor or digroup control card in the associated LCA fails
- a message link to the associated LCA fails
- the common peripheral controller fails

Each LCA also contains a maximum of five NT6X05AA LCM drawers. Each drawer contains an NT6X54AA bus interface card (BIC) and a maximum of 64 line circuit (LC) cards.

Each LCA has an NT6X53AA power converter, which can provide the required operating voltages for both LCAs if the other converter fails. The power converter also incorporates looparound features in the digital path of each circuit card that can isolate single faults. Fuse and converter-failure alarm outputs go to the FSP.

Host interface equipment common CP fill

The NT6X11AA host interface equipment common CP fill is an interface between the LCA DS30A links and the CPC DS-1 links. The common CP fill provides the following:

- the clock signal for the LCAs
- ringing generators for the LCAs
- the messaging interface and data rate conversion for the DS-1 line cards, the LCAs, and the RMM of the CP fill

The HIE common CP fill also provides optional emergency stand-alone (ESA) call-processing functions if the communications links to the CPC fail. Calls that originate and terminate on the same RLCM can complete if loss of links to the host office occurs. The ESA operation allows these calls to completes.

The ESA operation supports the following:

- plain ordinary telephone service (POTS)
- local dialing plans for POTS and Meridian Digital Centrex (MDC)
- sequential hunt groups
- pulse and dual tone multifrequency (DTMF) reception
- all ringing types that the associated LCM supports
- ground and loop start lines

NT6X14AA (continued)

- revertive calling for party lines that are not business-set
- a manual operator line plus 63 automatic lines

The ESA operation does not support the following:

- attendant consoles
- vertical services
- local automatic message accounting (LAMA)
- centralized automatic message accounting (CAMA) billing
- recorded announcements
- coin-control functions
- maintenance and administration functions
- most MDC services. An exception is multiple centrex customer dialing plans.

The HIE common CP fill contains the following:

- two or three NT6X50AA DS-1 interface CPs
- two NT6X73AA link control circuit cards, LCC-0 and LCC-1
- two NT6X60AA RLCM ringing generators (RG)
- two NT2X70AA power converters

If the ESA option is present, the HIE common CP fill also contains the following:

- an NT6X45AA ESA processor
- an NT6X75AA ESA tone and clock card
- an ESA memory card

Remote maintenance module

The NT6X13AA RMM CP fill is a modified version of the NT2X58 maintenance trunk module (MTM) CP fill. The NT6X13AA RMM CP fill provides maintenance and operational support for remote offices connected to a DMS-100 central office.

The NT6X13AA RMM CP fill supports the following:

- metallic test access (MTA)
- incoming/outgoing test trunks
- line test units (LTU)

- scan and signal distribution (SD) points
- Digitone receivers, when the ESA option is present

The RMM CP fill contains the following:

- an NT6X74AA control circuit card
- an NT2X59AA group coder-decoder (CODEC) and tone circuit card
- a pair of power converters, NT2X06AB and NT6X09AA
- a maximum of 14 service circuit cards

The needs of the office determine the types of service circuit cards used. Some of the service cards the RMM uses are for MTA functions.

In the RLCM, the RMM gives the LCM access to test and service circuit cards at the remote site. This process reduces traffic on the DS-1 links. The C-side interface of the RMM CP fill connects to each NT6X50AA line control card in the HIE CP fill. This connection occurs through DS30A links. The RMM connects to both LCCs to make sure the CP is operational. The operation does not depend on which LCC is active. If the ESA option is not present, more than one RLCM at a remote site can share a single RMM. If the ESA option is present, each RLCM must have a dedicated RMM. The RMM must include a Digitone receiver card.

Selecting and testing line circuits occurs through the DS30A links to the LCC and from the LCC to the host office. The display of test results also occurs in this way. Test procedures are performed at the MAP terminal.

Frame supervisory panel

The NT6X25AA FSP applies power to and provides the power control and alarm circuits for parts in the RLCM frame. The following provide power control:

- seven circuit breakers
- an NT6X35AA alarm circuit card (CD1)
- an NT0X91AA converter drive and alarm circuit card (CD2)
- an NT0X91AE converter drive and protection circuit card (CD3)

The FSP also contains two talk battery filters and eight fuses.

Converter-fail lines from the power converters in the RLCM connect to light-emitting diode (LED) frame-fail indicator on the FSP front panel. The converter-fail lines operate fail LEDs located below the associated power-feed circuit breakers on the FSP front panel. The front panel also contains four test

NT6X14AA (continued)

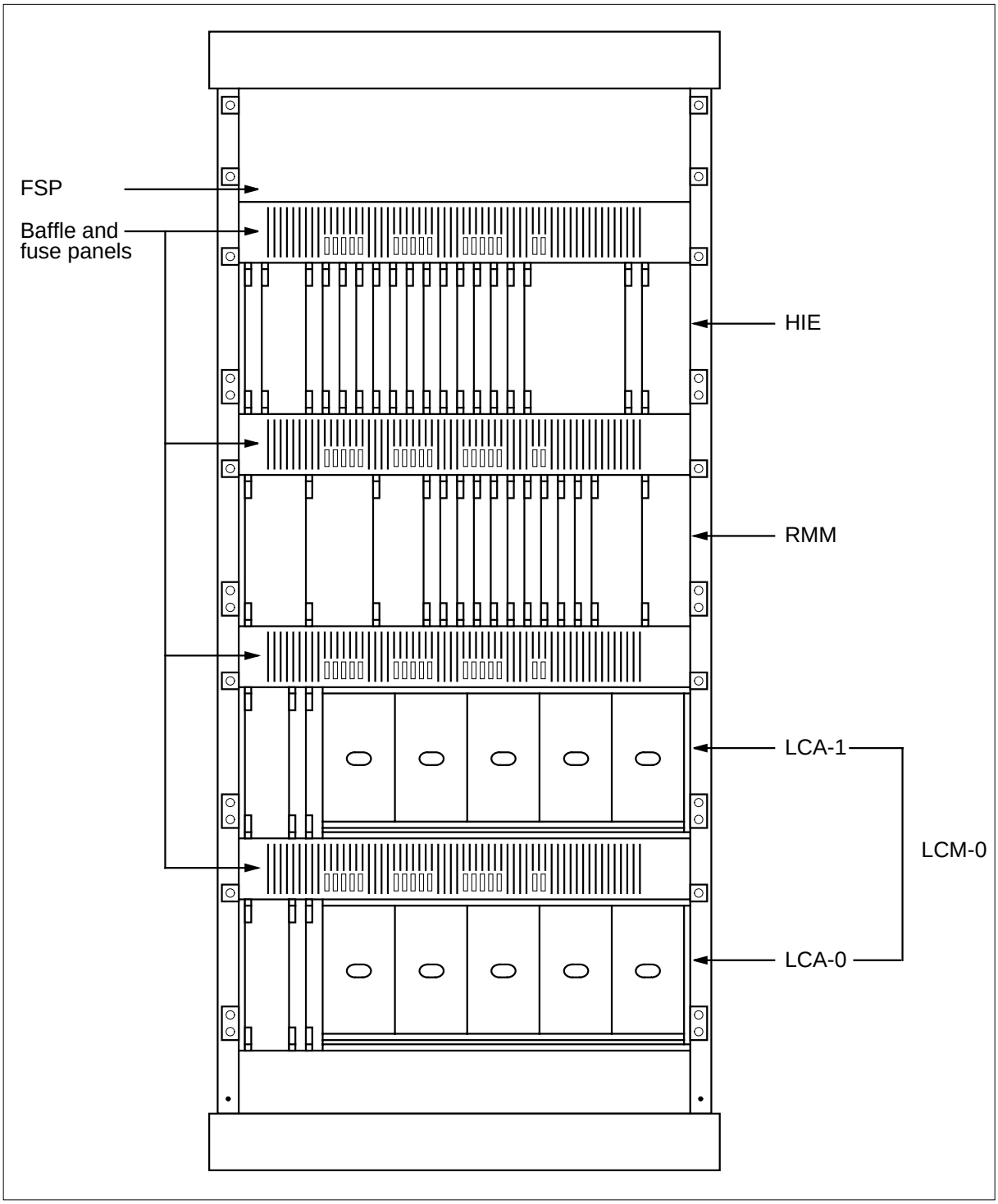
jacks, two telephone pairs and two data pairs. The telephone pairs are TEL-A and TEL-B. The data pairs are DATA-A and DATA-B. The FSP features a mechanical interlock, a small cover that slides to provide access to two circuit breakers at a time.

Design

The RLCM design appears in the following figure.

NT6X14AA (end)

The NT6X14AA parts



NT6X14CA

Product description

The NT6X14CA remote control and maintenance equipment (RCME) frame contains the following:

- a maximum of three NT6X11AA host interface equipment (HIE) common fills
- an NT6X13AB remote maintenance module (RMM) fill
- an NT6X25AA frame supervisory panel (FSP)

Baffles permit air circulation for convection cooling. The FSP provides power control and alarm circuits for the three HIE shelves and one RMM shelf.

Parts

The RCME contains the following parts:

- an NT6X11AA–host interface equipment (HIE) common fill
- an NT6X13AB–remote maintenance module (RMM) fill
- an NT6X25AA–frame supervisory panel (FSP)

Host interface equipment common fill

The NT6X11AA HIE common fill provides the clock signal and ringing generators. The common fill also provides messaging interface and data rate conversion for DS-1 line cards of the common fill and the RMM. The HIE common fill also provides available emergency stand-alone (ESA) call-processing functions if the communications links fail. If loss of links to the host office occurs, calls that originate and terminate on the same RCME on can complete. The ESA operation allows completion of these calls

The ESA operation supports the following functions:

- plain ordinary telephone service (POTS)
- local dialing plans for POTS and Meridian Digital Centrex (MDC)
- sequential hunt groups
- pulse and dual-tone multifrequency (DTMF) reception
- all ringing types that the associated line concentrating module (LCM) supports
- ground and loop start lines,
- revertive calling for party lines that are not business sets
- a manual operator line plus 63 automatic lines

The ESA operation does not support the following functions:

- attendant consoles
- vertical services
- local Automatic Message Accounting (LAMA)
- centralized Automatic Message Accounting (CAMA) billing
- recorded announcements
- coin-control functions
- maintenance and administration functions
- most MDC services. An exception is multiple Centrex customer dialing plans.

The HIE common fill contains

- two or three NT6X50AA DS-1 interfaces
- one NT6X73AA link control card
- two NT6X60AA RCME ringing generators (RG)
- two NT2X70AA power converters

If the available ESA is present, the common fill also contains an NT6X45AF ESA processor and NT6X75AA ESA clock and tone card.

Remote maintenance module fill

The NT6X13AB RMM fill provides maintenance and operational support for remote offices connected to a DMS-100 central office. The RMM fill supports the following:

- metallic test access (MTA)
- incoming and outgoing test trunks
- line test units (LTU)
- scan and signal distribution (SD) points
- Digitone receivers, when ESA is present

The RMM fill contains the following:

- an NT6X74AB control card
- an NT2X59AA group coder-decoder (CODEC) and tones card
- an NT2X06AB power converter

NT6X14CA (continued)

In the RCME, the RMM gives the LCM access to test and service cards at the remote site. This process reduces the traffic on the DS-1 links. The central-side (C-side) interface of the RMM fill connects to each NT6X50AA DS-1 interface card in the HIE fill. This connection occurs through DS30A links. The RMM connects to the DS-1s to maintain operation. Operation does not depend on which DS-1 is active. If the available ESA is not present, more than one RCME at a remote site can share a single RMM. If the ESA is present, each RCME must have a dedicated RMM. The RMM must include a Digitone receiver card.

Frame supervisory panel

The NT6X25AA FSP applies power and provides the power control and alarm circuits for the the RCME frame components. The following provide power control:

- seven circuit breakers
- an NT0X91AA converter drive and alarm card
- an NT0X91AE converter drive and protection card

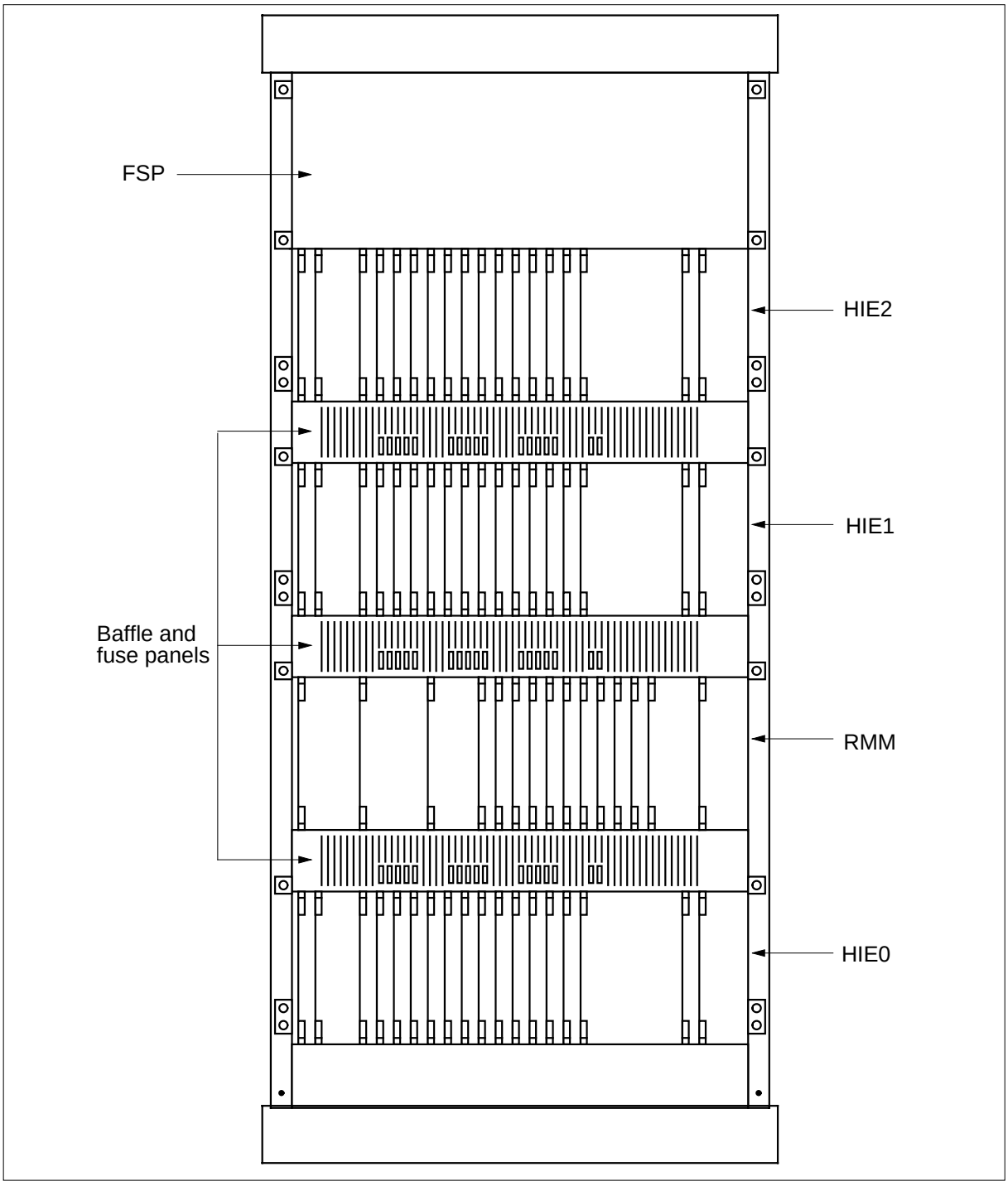
The FSP also contains two talk battery filters and eight fuses.

Converter fail lines from the power converters in the RCME connect to light-emitting diode (LED) frame fail indicators on the front panel of the FSP. The converter fail lines also operate fail LEDs located below the associated power feed circuit breakers on the FSP front panel. The front panel also contains four test jacks that provide access to two telephone pairs and two data pairs. The telephone pairs are TEL-A and TEL-B. The two data pairs are DATA-A and DATA-B. The FSP features a mechanical interlock, a small cover that slides to provide access to two circuit breakers at a time.

Design

The RCME design appears in the following figure.

The NT6X14CA parts



Note: This illustration is not drawn to scale.

NT6X17AC

Product description

The NT6X17AC type-A line card provides voice and signaling interface between the following:

- a single-party, two-wire loop
- the digital network of DMS-100 switches

The card also provides both analog and digital looparound for diagnostics.

The card provides access to the subscriber loop with or without the line card circuits connected for loop and card tests. The card also provides software-controlled cutover.

Functional description

The NT6X27AC converts analog signals to digital signals.

Functional blocks

The NT6X17AC has the following functional blocks:

- loop detection
- ringing supervision
- flux balance
- transmission
- line circuit card (LCC) functions
- voltage regulator
- cutover hold
- test access relay

Loop detection

Talk battery and battery return connect to tip and ring through a matched pair of 200ω resistors and a transformer primary winding. A resistive bridge and the associated amplifier of the bridge monitor a loop current that flows through the feed resistors.

The supervision amplifier (SVA) produces an output voltage related to the loop current. A comparison of the output of the SVA with the reference voltage determines the loop status. A voltage at the supervision amplifier output lower than the reference voltage indicates an off-hook condition.

Ringing supervision

During ringing, a large amount of ac current flows through the feed resistors. The supervision amplifier also detects this current. When detection occurs, ac voltage superimposes on the nominal dc level at the supervision amplifier.

To prevent off-hook detection that is not reliable, a low-pass filter filters the ac component of the SVA signal out. The low-pass filter uses with a cutoff frequency of 2 Hz.

Flux balance

Flux balance keeps the transformer from saturation because of high current that flows in the primary winding.

A current source, controlled to produce 20% of the loop current, connects to the flux balance winding. This winding has five times the number of turns of the combined primary windings. The current in the flux balance winding flows in a direction opposite to that in the primary winding. This flow balances the flux that loop current causes.

Level shifting and simplification translates the logic control voltage to the -48V talk battery. This translation has enough voltage swing to control the current source. A 1000Ω resistor monitors the current source. A zener diode clamp protects the current source from foreign potentials on the loop.

Transmission

In the receive direction, the LCC decodes and filters the pulse code modulation (PCM) data from the bidirectional bus. Two 415Ω resistors couple the output of the LCC to the secondary side of the transformer. The middle capacitor completes the voice frequency (VF) path for the split primary windings of the transformer. The receive signal appears on the tip and ring.

In the transmit direction, VF signals from the tip and ring couple to the secondary transformer. The signal feeds into the LCC. The LCC filters the VF signal and codes the signal into PCM data. The data goes to the network through the bidirectional bus.

The LCC provides two balance networks under software control, one for loaded loops and one for loops that are not loaded. The LCC also provides gain pads under software control for the receive path. Zener diodes (D3 and D4) on the secondary side of the transformer protect the LCC from foreign potentials on the loop.

NT6X17AC (continued)

Line circuit card functions

The bidirectional bus helps perform the software control and PCM transmission. The master clock that the line drawer supplies clocks data into the LCC.

Control messages can affect the following functions:

- the value of the receive gain pad
- relay operations
- read and write operations to the test register
- setting the balance network to use

Volt regulator

The 12 V that the LCC requires is from a series-pass regulator connected to the 15-V logic supply. The base of the transistor (Q6) connects to the 12.7 V drawer reference through a resistor-capacitor (RC) filter. This arrangement provides an accurate low-impedance supply for the LCC and other associated circuits.

Cutover hold

The cutover relay (K2) activates under software control. Application of a ground to the cutover (CUTO) hold line holds the relay on after removal of the relay drive. This process reduces the power that the line card dissipates while in CUTO hold.

The bus interface card (NT6X54) controls the ground on the CUTO pin. This control allows a complete drawer go into service at the same time.

Test access relay

The test access relay (K1) allows bridging access to the tip and ring leads for test purposes. The test access relay is on the loop side of the CUTO relay to allow loop testing with the line card circuits removed.

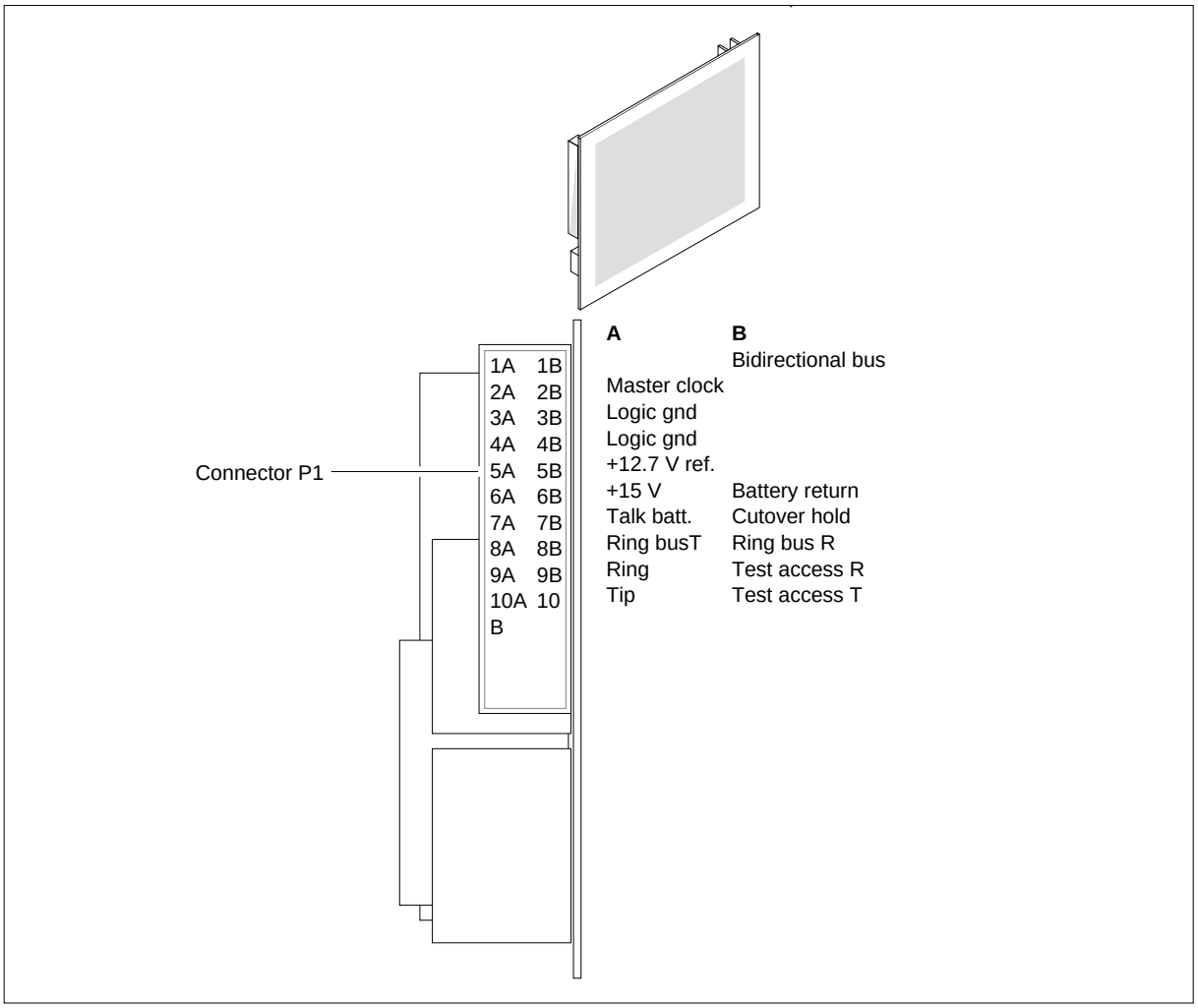
Signaling

The NT6X17AC card receives supply voltages and control signals from the line concentrating module (LCM) through the back panel of the line drawer.

Pin numbers

The NT6X17AC pin numbers appear in the following figure.

The NT6X17AC pin numbers



The card has short circuit protection. The 60-Hz induction is normal with a maximum 20 mA for each conductor. The signaling characteristics of the card appear in the following table.

Signaling characteristics parts (Sheet 1 of 2)

Characteristics	Value
Talk battery voltage	-42.75 V to -55.8 V
Normal talk battery range (float charge)	-49 V to -53.5 V
Maximum talk battery discharge (no charge)	-42.75 V

NT6X17AC (continued)

Signaling characteristics parts (Sheet 2 of 2)

Characteristics	Value
Maximum talk battery charge (equalizing)	-55.8 V
Lightning surge protection	1 kV (10 × 1000 µs)
Total loop resistance, including 500-type set for 21 mA: residential	1900 Ω
Conductor leakage resistance: residential	10 kΩ

Transmission specifications

The NT6X17AC has a 900 Ω + 2.16 µF input impedance. The transmission frequency responses and relative losses appear in the following table.

Transmission frequency responses

Frequency response (Hz)	Relative loss (dB)	
	Minimum	Maximum
60	20.0	-
200	0.0	4.0
300	-0.5	1.0
3000	-0.5	1.0
3200	-0.5	1.5
3400	0.0	3.0

The input return loss is as follows: echo return loss (ERL) is ≥20 dB; singing return loss (SRL) is ≥14 dB. A D/A loss range of 0 to 7 dB in 1-dB increments that can be programmed is provided. The line equipment level nominal loss of the A/D path and the D/A path is 0 dBm.

The card has an idle channel noise level of <20 dBrnC. The card transhybrid echo return loss (ERL) loss is ≥21 dB, and the transhybrid singing return loss (SRL) is ≥16 dB.

The envelope delay distortion frequencies and delays appear in the following table.

Envelope delay distortion

Frequency (Hz)	Maximum delay distortion (μs)
400	700
600	500
800	350
1004	190
1150	150
2300	150
2500	190
2700	350
3000	500
3200	700

The quantization distortion level and signal/delay distortion ratios appear in the following table.

Quantization distortion

Input level at 1004 Hz	Signal/distortion ratio (dB) C-message weighted, line-to-line
0 to -30 dBm0	≥33
0 to -40 dBm0	≥27
0 to -45 dBm0	≥22

The signal longitudinal balance appears in the following table.

Longitudinal balance (Sheet 1 of 2)

Frequency (Hz)	Minimum balance (dB)
204	≥53

NT6X17AC (end)

Longitudinal balance (Sheet 2 of 2)

Frequency (Hz)	Minimum balance (dB)
1004	≥58
3004	≥53

Dimensions

The dimensions of the NT6X17AC are as follows:

- height: 73 mm (2.875 in.)
- depth: 22 mm (0.875 in.)
- width: 89 mm (3.5 in.)

Power requirements

The card requires 165 mW. The converter voltage has a power requirement of +15 V ±0.5 V. The reference voltage in the bus interface card has a power requirement of +12.7 V ±1%.

NT6X17BA

Product description

The NT6X17BA type-A world line card (WLC) provides a plain ordinary telephone service (POTS) interface. The interface meets the requirements of all Nortel Networks markets. The software controls transmission and signaling characteristics of the card, including loop current limit and automatic loss equalization.

Location

The NT6X17BA occupies one card position in a line concentrating module (LCM) drawer.

Functional description

Functional blocks

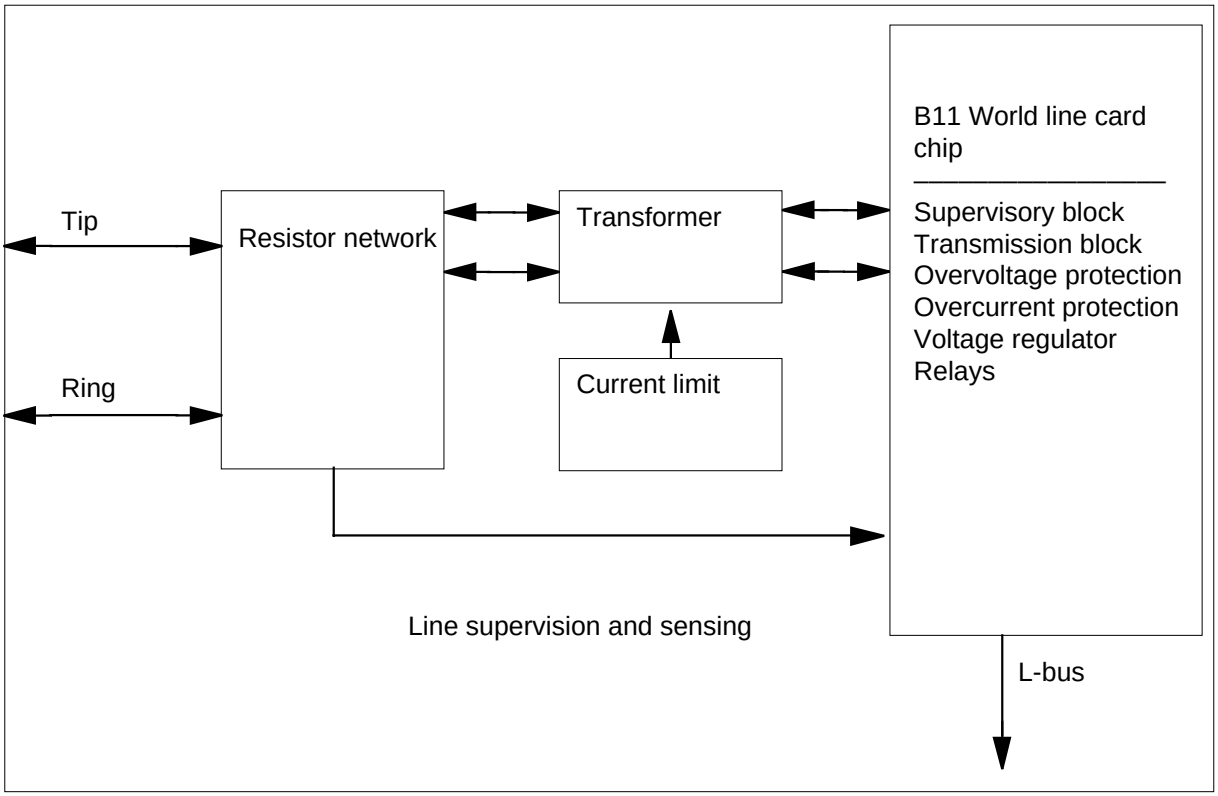
The NT6X17BA has the following functional blocks:

- supervisory block
- transmission block
- overvoltage protection
- overcurrent protection
- voltage regulator
- relays

The relationship between these functional blocks appears in the following figure.

NT6X17BA (continued)

The NT6X17BA functional blocks



Supervisory block

The supervisory block performs the following functions:

- loop detection
- ringing supervision
- loop current limiting

The network and the B11 chip monitor a loop current that flows through the WLC transformer and the battery feed network. The B11 compares the output voltage of the amplifier with a software-selectable supervision threshold. The B11 chip determines if the line is on-hook or off-hook.

Two external low-pass filters and the loop detection comparator (in the B11 chip) provide ringing supervision.

The B11 chip in the NT6X17BA allows the software to select the loop current limit.

Transmission block

The transmission block performs the following functions:

- generation of input impedances
- code and decode of voice signals
- establishment of hybrid balance

The differential loop current and the voltage between the tip and ring leads have a specified relationship. Establishment of the required relationship creates the input impedance.

To establish the voice path, the B11 coder-decoder (CODEC) decodes and filters the receive signal and the transmit signal. The receive signal is digital-analog and the transmit signal is analog-digital. The B11 CODEC makes frequency response corrections when the terminating impedance differs from the input impedance, as in two-element input impedances.

The balance filter accomplishes hybrid balance. The transmit signal contains parts of the receive signal. Removal of these parts must occur before coding of the transmit signal and position on the bidirectional bus.

Overvoltage protection

The tip and ring leads of the NT6X17BA are monitored for overvoltage occurrences. When overvoltage occurs, operation of the cutover relay isolates the line circuit. System software releases the relay after removal of the fault condition.

Overcurrent protection

The NT6X17BA has automatic protection against ground faults on the ring lead. The automatic protection function of the NT6X17BA senses the condition and limits the current that can flow in the ring lead. The function limits the current to a value that cannot damage the card.

Voltage regulator

The B11 chip in the NT6X17BA includes a 5-V regulator. The regulator takes a reference signal from the line card power supply and scales the signal. This process allows the regulator to make sure of an accurate power source of 5 V.

NT6X17BA (continued)

Relays

The NT6X17BA has the following relays:

- cutover
- test access
- ring

A cutover relay isolates the NT6X17BA line card from the subscriber loop. The relay has several purposes, including diagnostics, office installation, and protection of the line card from potential hazards.

A test access relay connects the A and B leads (tip and ring) of the NT6X17BA to the LCM test access bus during tests.

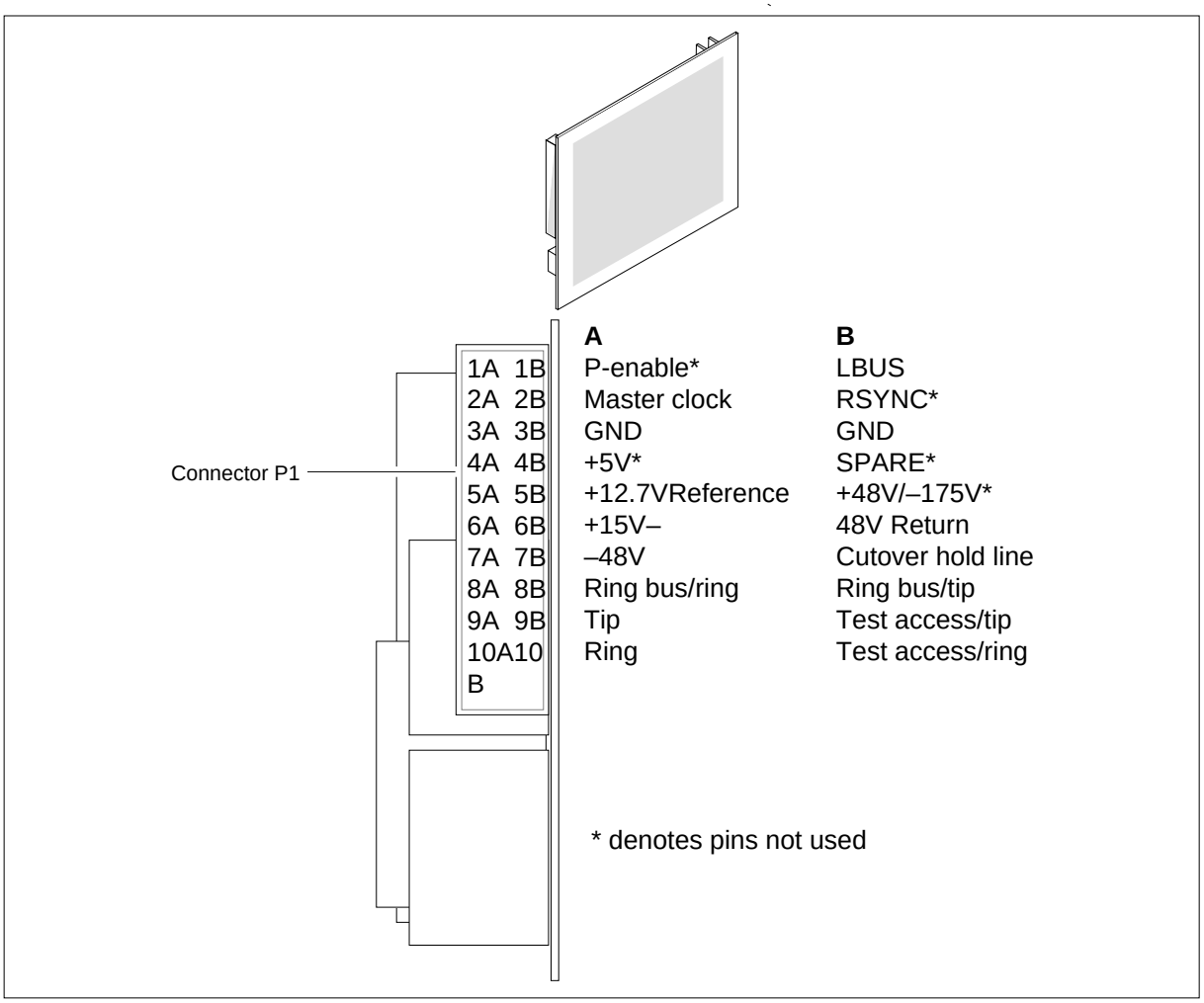
A ring relay connects the LCM ring bus to the NT6X17BA in order to ring the near-end telephone.

Signaling

Pin numbers

The pin numbers for the NT6X17BA appear in the following figure.

The NT6X17BA pin numbers



The card has short circuit protection. The 60-Hz induction is normal with a maximum of 20 mA for each conductor. The signaling characteristics of the card appear in the following table.

Signaling characteristic parts (Sheet 1 of 2)

Characteristic	Value
Talk battery voltage	-42.75 V to -55.8 V
Normal talk battery range (float charge)	-49 V to -53.5 V
Maximum talk battery discharge (no charge)	-42.75 V

NT6X17BA (continued)

Signaling characteristic parts (Sheet 2 of 2)

Characteristic	Value
Maximum talk battery charge (equalizing)	-55.8 V
Lightning surge protection	1 kV (10 × 1000 µs)
Total loop resistance, including 500-type set for 21 mA: residential	1900 Ω
Conductor leakage resistance: residential	10 kΩ

Transmission specifications

The has a 900 Ω+ 2.16 µF input impedance. The transmission frequency responses and relative losses appear in the following table.

Transmission frequency responses

Frequency response (Hz)	Relative	loss (dB)
	Minimum	Maximum
60	20.0	-
200	0.0	4.0
300	-0.5	1.0
3000	-0.5	1.0
3200	-0.5	1.5
3400	0.0	3.0

The input return loss is echo return loss (ERL) is ≥20 dB, singing return loss (SRL) is ≥14 dB. A D/A loss range of 0 to 7 dB in 1-dB increments that can be programmed is provided. The nominal loss of the A/D path and the D/A path of the line equipment level is 0 dBm.

The card has an idle channel noise level of <20 dBrnC. The transhybrid echo return loss (ERL) loss of the card is ≥21 dB. The transhybrid singing return loss (SRL) of the card is ≥16 dB.

The envelope delay distortion frequencies and delays appear in the following table.

Envelope delay distortion

Frequency (Hz)	Maximum delay distortion (μs)
400	700
600	500
800	350
1004	190
1150	150
2300	150
2500	190
2700	350
3000	500
3200	700

The quantization distortion level and signal/delay distortion ratios appear in the following table.

Quantization distortion

Input level at 1004 Hz	Signal/distortion ratio (dB) C-message weighted, line-to-line
0 to -30 dBm0	≥33
0 to -40 dBm0	≥27
0 to -45 dBm0	≥22

The longitudinal balance of the signal appears in the following table.

Longitudinal balance (Sheet 1 of 2)

Frequency (Hz)	Minimum balance (dB)
204	≥53

NT6X17BA (end)

Longitudinal balance (Sheet 2 of 2)

Frequency (Hz)	Minimum balance (dB)
1004	≥58
3004	≥53

Dimensions

The dimensions of the NT6X17BA are as follows:

- height: 73 mm (2.875 in.)
- depth: 22 mm (0.875 in.)
- width: 89 mm (3.5 in.)

Power requirements

The card requires 165 mW. The converter voltage has a power requirement of +15 V ±0.5 V. The reference voltage in the bus interface card has a power requirement of +12.7 V ±1%.

NT6X18AA

Product description

The NT6X18AA line card type B provides voice and signaling interfaces. The interface is between 2-wire analog subscriber lines and the 4-wire, 32-channel, 2.56 Mbit/s digital bit stream of the DMS-100 switch.

The card interacts with subscriber lines, coin private automatic branch exchange (PABX) and coded ringing circuits. The card provides a single-party, two-party or multiparty interface with one channel of the DMS.

Location

The card occupies one position in a line concentrating module (LCM) drawer.

Functional description

The NT6X18AA communicates between the line card (LC) and the LCM drawer. The card uses 10 bit digital receive and transmit pulse code modulation (PCM) and control data samples on a bidirectional bus for communication. The card uses a clock signal from the LCM drawer to transfer samples at the appropriate channel. The card supervises onhook, offhook and dial pulsing signals from the subscriber line.

Functional blocks

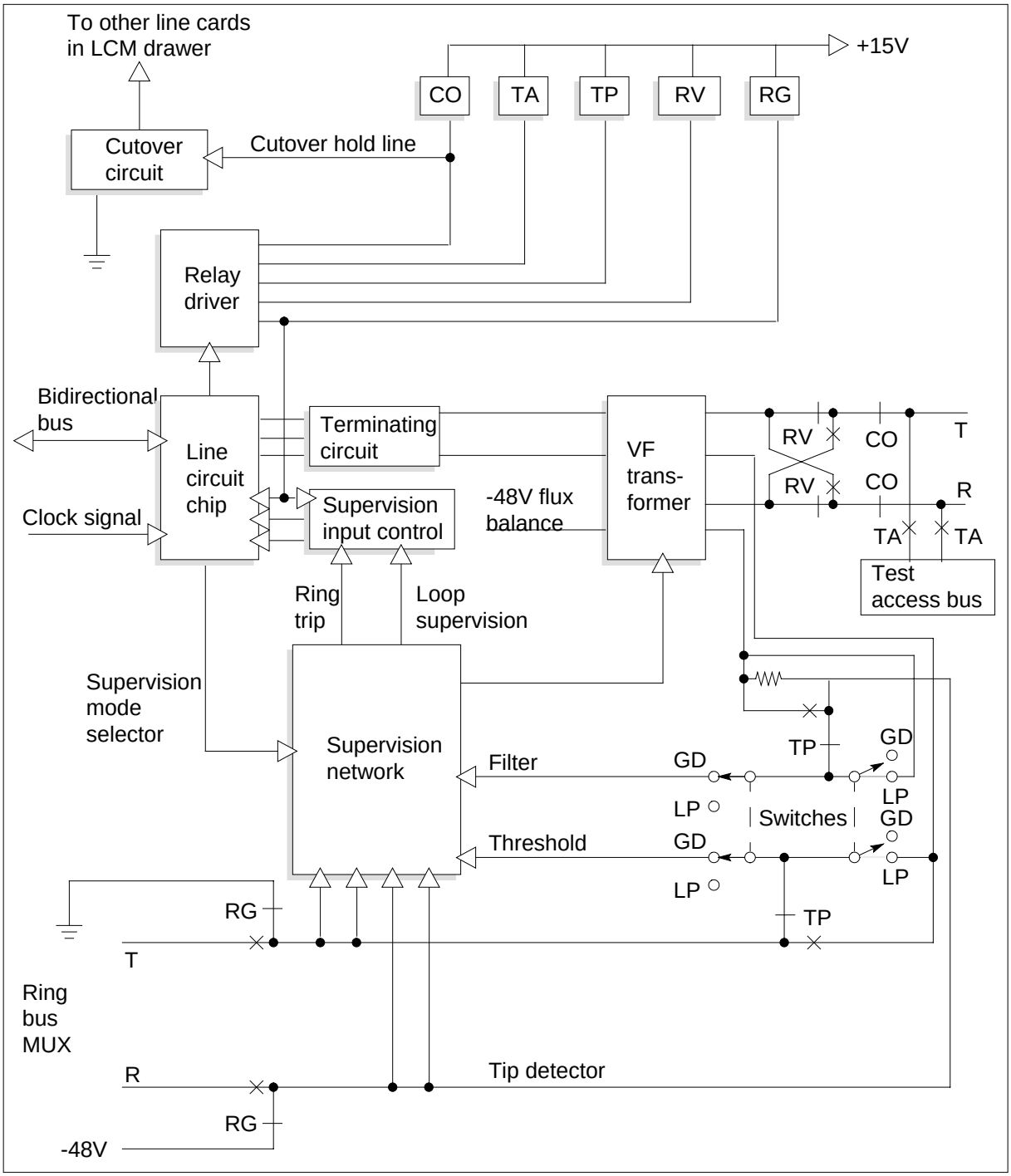
The NT6X18AA consists of the following functional blocks:

- line circuit (LC) chip
- supervision network
- supervision input control
- terminating circuit
- voice frequency (VF) transformer
- relay driver
- relay circuits
- cutover circuit

The following figure describes the relationship between the functional blocks.

NT6X18AA (continued)

NT6X18AA functional blocks



LC chip

The LC chip uses a bidirectional bus to receive and transmit PCM samples. In the receive direction, the circuit decodes the received PCM samples to analog voice frequency signals to reconstruct the original analog VF signal. The signal passes through the VF transformer to the analog line of the subscriber.

In the transmit direction, the LC chip receives analog VF signals from the equipment of the subscriber. The LC chip converts the signals to PCM samples, and transmits these samples to the bus interface in the LCM drawer. The chip filters the analog signals to limit bandwidth, and samples the signals at an 8 kHz rate.

The chip also selects the source of card supervision (loop detection or tip detection). The chip uses a 2.56 MHz clock to transfer data at the appropriate channel time.

The chip contains balancing networks that you can program to balance nonloaded and loaded cables. The nonloaded cable has a resistance of 800Ω, with a capacitance of 0.005 µF. The loaded cable has a resistance of 1650ω, with a capacitance of 0.005 µF.

Supervision network

The supervision network uses tip and loop detectors to determine onhook and offhook conditions from the subscriber equipment. The network uses control messages from the LC chip and tip detectors in coin mode supervision. The network uses loop detectors in residential mode supervision. The network also detects dial pulsing on the tip (T) and ring (R) leads of the analog line of the subscriber.

The network filters a sampled loop current during ringing. The network performs this action to determine if a dc component that indicates a ring trip condition is present.

Supervision input control

The supervision input control circuit receives signals from the supervision network. The supervision input control provides supervision signals to the LCM drawer and the RG relay.

Terminating circuit

The terminating circuit receives and transfers Digitone signaling to the LC chip.

NT6X18AA (continued)

VF transformer

The VF transformer provides an interface between the LC chip in the card and the analog facilities. In the receive direction, the transformer converts the signals on the T and R leads to one signal. The receive circuit must process this signal. In the transmit direction, the transformer receives the signal from the transmit circuit. The transformer sends the converted signals over the T and R leads.

The transformer uses a flux balance winding to cancel flux that line currents, that flow in the supervision circuits, produce. The transformer cancels flux to improve the performance of the transformer for speech transmission.

Relay driver

The relay driver receives coded messages from the LC and decodes the messages. The relay driver sends signaling messages to the appropriate relay circuits.

Cutover circuit

The cutover circuit receives a signal from the CO relay circuit and provides cutover that the software controls. The circuit uses the bidirectional bus to address specified line circuits. The circuit activates the CO relay circuit in the addressed LC.

Relay circuits

Five relay circuits receive signals from the relay driver and provide testing and supervision enabling. The relays and associated functions appear in the following table.

Relay operation (Sheet 1 of 2)

Relay	Operated	Released
CO, TA	CO operated, TA released: T and R leads isolated VF transformer unbalanced VF signals on the receive path appear on the transmit path with almost zero loss. TA operated, CO released: Bridged monitor access provided to the T and R leads of the subscriber and to the VF transformer.	CO and TA released, normal operation

Relay operation (Sheet 2 of 2)

Relay	Operated	Released
	TA and CO operated with TA contacts closed and CO contacts open: Subscriber loop tests are applied to the T and R leads through the TA, by isolation of the subscriber loop from the LC.	
TP	If the LC switches set to GD, normal operation.	If the LC switches are set to GD, a ground start is enabled.
	If the LC switches are set to LD, disables ac filter in the supervision network to allow detection of dial pulses.	If the LC switches are set to LD, normal operation.
RV	Reverses polarity of the signaling voltage on the T and R leads. Disables the digitone termination pad in the telephone set to prevent generation of false coin signaling tones.	Normal operation
RG	Supervision voltages disconnected. Ringing bus connects to the supervision network.	Normal operation

Technical data

The card has short circuit protection. The 60 Hz induction is normal with a maximum 20mA for each conductor. The signaling characteristics of the card appear in the following table.

Signaling characteristics (Sheet 1 of 2)

Characteristic	Value
Talk battery voltage	-42.75V to -55.8V
Normal talk battery range (float charge)	-49V to -53.5V
Maximum talk battery discharge (no charge)	-42.75V
Maximum talk battery charge (equalizing)	-55.8V
Ground potential	±3V
Ground resistance	50 Ω(max)
Lightning surge protection	1kV (10 × 100 μs)

NT6X18AA (continued)

Signaling characteristics (Sheet 2 of 2)

Characteristic	Value
Total loop resistance (like 500-type set for 21mA)	
Residential:	1900 Ω
Coin:	1500 Ω
Ground start ring lead resistance	1040 Ω
Conductor leakage resistance	
Residential:	10 kΩ
PABX/coin:	30 kΩ

Transmission specifications

The NT6X18AA card has a 0 dBm transmission level point (TLP) at the main distribution frame (MDF) and an overload level of +3 dBm. The transmission frequency responses and the relative losses of the card appear in the following table.

Transmission frequency responses

Frequency response	Relative loss
200-250 Hz	4.00 dB
251-300 Hz	2.00 dB
301-2400 Hz	0.75 dB
2401-3000 Hz	2.00 dB
3001-3400 Hz	4.00 dB

The echo return loss of the transmission is 20 dB. The structural return loss of the echo is 14 dB. The structural return loss has a programmable digital-to-analog loss range of 0 through 7 dB in 1 dB increments.

Physical dimensions

The physical dimensions of the NT6X18AA are:

- height: 73 mm (2.875 in.)
- depth: 22 mm (0.875 in.)
- width: 89 mm (3.5 in.)

Power requirements

The NT6X18AA consumes 150mW of power and converts voltages of +15V ±0.5V and +12.7V ± 1%.

NT6X18AB

Product description

The NT6X18AB line card type B with +48V provides voice and signaling interfaces. The interface is between 2-wire analog subscriber lines and the 4-wire, 32-channel, 2.56 Mbit/s digital bit stream of the DMS-100 switch.

The card interacts with subscriber lines, coin private automatic branch exchange (PABX) and coded ringing circuits. The card provides a single-party, two-party or multiparty interface with one channel of the DMS.

Location

The card occupies one position in a line concentrating module (LCM) drawer.

Functional description

The NT6X18AB communicates between the line card (LC) and the LCM drawer. The card uses 10 bit digital receive and transmit pulse code modulation (PCM) and control data samples on a bidirectional bus for communication. The card uses a clock signal from the LCM drawer to transfer samples at the appropriate channel. The card supervises onhook, offhook and dial pulsing signals from the subscriber line.

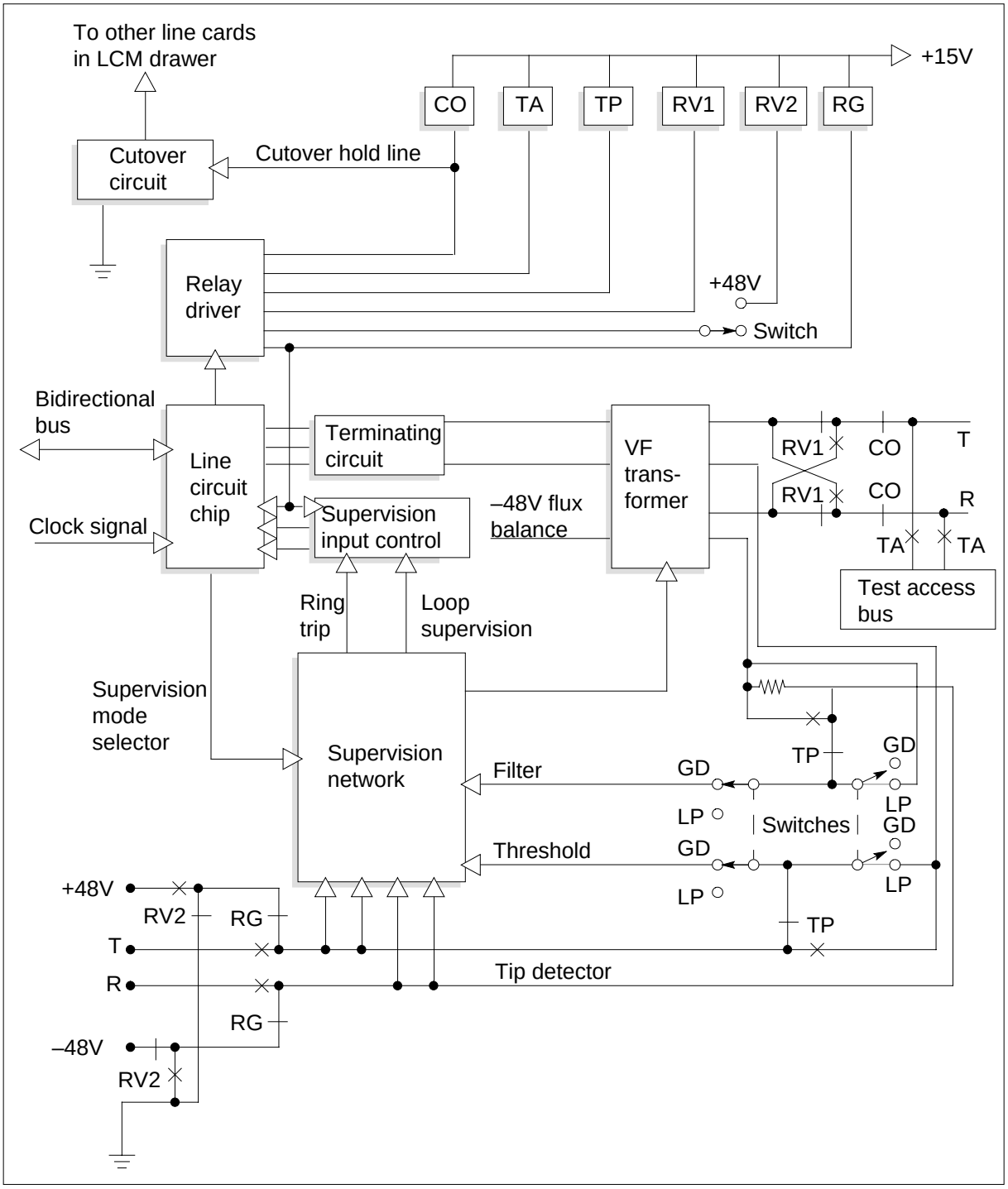
Functional blocks

The NT6X18AB contains the following functional blocks:

- LC chip
- supervision network
- supervision input control
- terminating circuit
- voice frequency (VF) transformer
- relay driver
- relay circuits
- cutover circuit

The following figure displays the relationship between the functional blocks.

NT6X18AB functional blocks



NT6X18AB (continued)

LC chip

The LC chip uses a bidirectional bus to receive and transmit PCM samples. In the receive direction, the circuit decodes the received PCM samples to analog voice frequency signals. The circuit performs this action to reconstruct the original analog VF signal. The signal passes through the VF transformer to the analog line of the subscriber.

In the transmit direction, the LC chip receives analog VF signals from the equipment of the subscriber. The LC chip converts the signals to PCM samples. The LC chip transmits these samples to the bus interface in the LCM drawer. The chip filters the analog signals to limit bandwidth and samples the signals at an 8 kHz rate.

The chip selects the source of card supervision, loop detection or tip detection. The chip uses a 2.56 MHz clock to transfer data at the appropriate channel time.

The chip contains balancing networks that you can program to balance nonloaded and loaded cables. The nonloaded cable has a resistance of 800Ω with a capacitance of 0.050 µF. The loaded cable has a resistance of 1650Ω with a capacitance of 0.005 µF.

Supervision network

The supervision network uses tip and loop detectors to determine onhook and offhook conditions from the subscriber equipment. With control messages from the LC chip, the network uses tip detectors in coin mode supervision. The network uses loop detectors in residential mode supervision. The network detects dial pulsing on the tip (T) and ring (R) leads of the analog line of the subscriber.

The network filters a sampled loop current during ringing. The network performs this action to determine if a dc component indicates that a ring trip condition is present.

Supervision input control

The supervision input control circuit receives signals from the supervision network. The supervision control circuit provides supervision signals to the LCM drawer and the RG relay.

Terminating circuit

The terminating circuit receives and transfers Digitone signaling to the LC chip.

VF transformer

The VF transformer provides an interface between the LC chip in the card and the analog facilities. In the receive direction, the transformer converts the signals on the T and R leads to one signal. The receive circuit processes this signal. In the transmit direction, the transformer receives the signal from the transmit circuit. The transformer sends the converted signals over the T and R leads.

The transformer uses a flux balance winding to cancel flux line currents produce. The line currents flow in the supervision circuits. The transformer cancels flux to improve the performance of the transformer for speech transmission.

Relay driver

The relay driver receives coded messages from the LC and decodes the messages. The relay driver sends signaling messages to the appropriate relay circuits.

Cutover circuit

The cutover circuit receives a signal from the CO relay circuit and provides cutover that software controls. The circuit uses the bidirectional bus to address specified line circuits. The circuit activates the CO relay circuit in the addressed LC.

NT6X18AB (continued)

Relay circuits

Six relay circuits receive signals from the relay driver and provide testing and supervision enabling. The relays and associated functions appear in the following table.

Relay operation

Relay	Operated	Released
CO,TA	CO operated, TA released: T and R leads isolated VF transformer unbalanced VF signals on the receive path appear on the transmit path with almost zero loss. TA operated, CO released: Bridged monitor access provided to the T and R leads of the subscriber and to the VF transformer. TA and CO operated with TA contacts closed and CO contacts open: Subscriber loop tests are applied to the T and R leads through the TA, by isolation of the subscriber loop from the LC.	CO and TA released, normal operation
TP	If the LC switches are set to GD, normal operation. If the LC switches are set to LD, the TP relay bypassed	If the LC switches are set to GD, a ground start is enabled.
RV1, RV2	RV1 operated, RV2 released: Reverses the T and R leads of the subscriber. Disables the digitone termination pad in the telephone set to prevent generation of false coin signaling tones. RV1 operated, RV2 operated: Reverses polarity of the signaling voltage on the T and R leads from ground on T and -48V on R to ground on T and +48V on R	RV1 and RV2 released, normal operation
RG	Supervision voltages disconnected, and ringing bus connected to the supervision network	Normal operation

Technical data

The card has short circuit protection, and the 60 Hz induction is normal with a maximum 20mA for each conductor. The signaling characteristics of the card appear in the following table.

Signaling characteristics

Characteristic	Value
Talk battery voltage	-42.75V to -55.8V
Normal talk battery range (float charge)	-49V to -53.50V
Maximum talk battery discharge (no charge)	-42.75V
Maximum talk battery charge (equalizing)	-55.8V
Ground potential	±3V
Ground resistance	50 ω(max)
Lightning surge protection	1kV (10 × 100 μs)
Total loop resistance (like 500-type set for 21mA)	
Residential:	1900 Ω
Coin:	1500 Ω
Ground start ring lead resistance	1040 Ω
Conductor leakage resistance	
Residential:	10k Ω
PABX/Coin:	30k Ω

Transmission specifications

The card has a 0 dBm transmission level point (TLP) at the main distribution frame (MDF) and an overload level of +3 dBm. The transmission frequency responses and the relative losses of the card appear in the following table.

Transmission frequency responses (Sheet 1 of 2)

Frequency response	Relative loss
200-250 Hz	4.00 dB
251-300 Hz	2.00 dB
301-2400 Hz	0.75 dB

NT6X18AB (end)

Transmission frequency responses (Sheet 2 of 2)

Frequency response	Relative loss
2401-3000 Hz	2.00 dB
3001-3400 Hz	4.00 dB

The echo return loss of the transmission is 20 dB. The structural return loss of the transmission is 14 dB. The structural return loss has a programmable digital-to-analog loss range of 0 through 7 dB in 1 dB increments.

Physical dimensions

The physical dimensions of the NT6X18AB are:

- height: 73 mm (2.875 in.)
- depth: 22 mm (0.875 in.)
- width: 89 mm (3.5 in.)

Power requirements

The consumes 150mW of power and converts voltages of +15V ±0.5V and +12.7V ± 1%.

NT6X18BA

Product description

The NT6X18BA Type-B world line card (WLC) is a subscriber line interface that provides a type-B plain ordinary telephone service (POTS) interface. The NT6X18BA can generate many different input and balance impedances. These impedances allow many telephone systems around the world to use the card.

Different transmission and signaling parameters can be selected in software, like the loop feed current limit. Electronic overvoltage protection improves the strength of the line card in hostile electrical environments.

The NT6X18BA also supports loop start, ground start, A and B lead (tip and ring) reversals. The card supports 12 to 16 kHz metering at different amplitudes and pulse periods. The cards also supports loss of A (tip) current detection for coin operation and register recall earth for United Kingdom application.

The NT6X18BA does not support:

- the message-waiting ability of the NT6X19AA line card
- the 30kΩ loop feature
- the synchronous optical network DMS (S/DMS) access node

Location

The NT6X18BA line card occupies one position in a line concentrating module (LCM) drawer.

Functional description

The NT6X18BA provides a voice and signaling interface. The interface is between a 2-wire analog subscriber line and one channel of the 4-wire, 32-channel, 2.56 Mbit/s stream of the DMS Family of switching systems.

Functional blocks

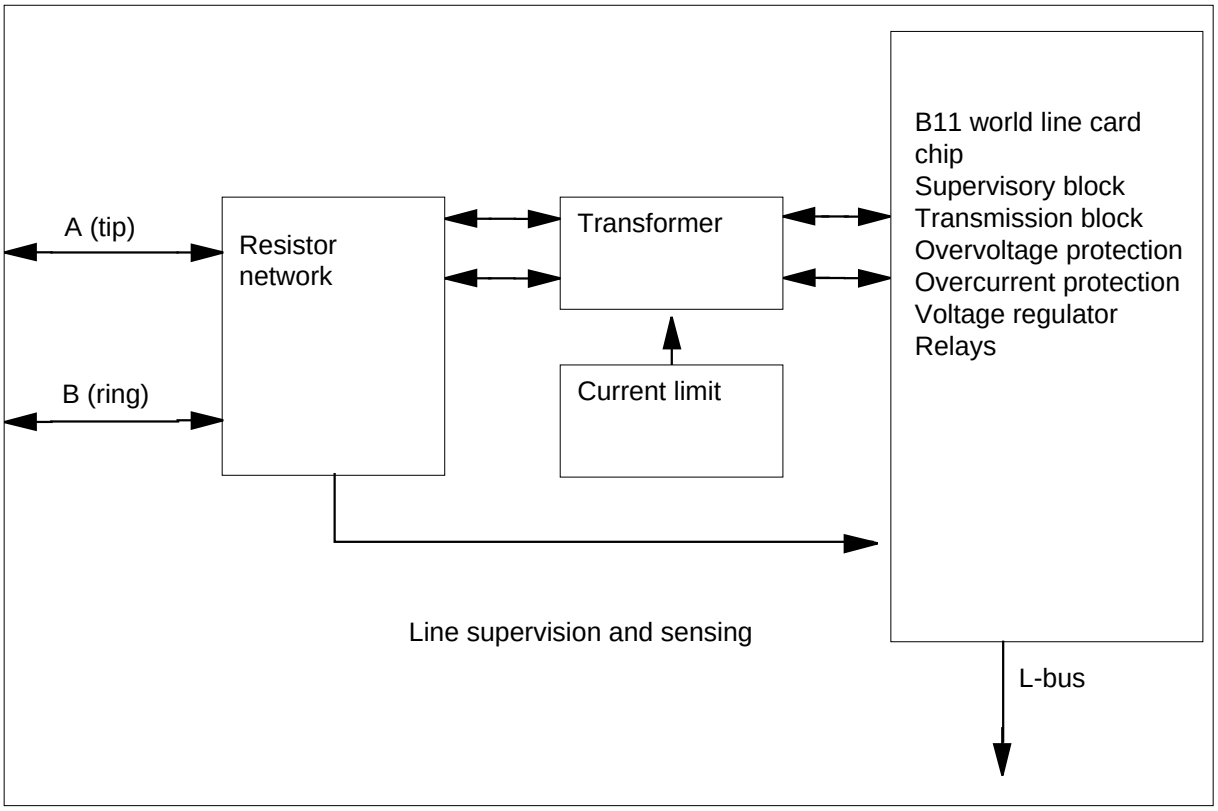
The NT6X18BA consists of the following functional blocks:

- supervisory block
- transmission block
- overvoltage protection
- overcurrent protection
- voltage regulator
- relays

NT6X18BA (continued)

The relationship between these functional blocks appears in the following table.

NT6X18BA functional blocks



Supervisory block

The supervisory block performs the following functions:

- loop start or ground start detection
- ringing supervision
- loop current limiting

The network and the B11 chip monitor a loop current that flows through the WLC transformer and the battery feed network. The network compares the output voltage of the amplifier with a software-selectable supervision threshold. The B11 chip determines if the line is on-hook or off-hook.

Two low-pass filters and the loop detection comparator (in the B11 chip) work to provide ringing supervision.

The B11 chip in the allows the loop current limit and the automatic loss equalization you to select in software.

Transmission block

The transmission block performs the following functions:

- generates input impedance
- establishes a voice path
- establishes hybrid balance
- enables loss equalization

The transmission block creates input impedance through the establishment of a required relationship. The differential loop current and the differential loop voltage between the A and B leads (tip and ring) require a relationship.

To establish the voice path, the B11 coder-decoder (CODEC) decodes and filters the receive signal and the transmit signal. The receive signal is digital-analog. The transmit signal is analog-digital. The B11 CODEC makes frequency response corrections when the terminating impedance is different from the input impedance, two-element input impedances.

The balance filter accomplishes hybrid balance. The transmit signal contains components of the receive signal that the system must remove. The system must remove these components before the system encodes the transmit signal. The system must perform this action before the system puts the signal on the bidirectional bus.

Set the equalization enable (EQE) bit in the B11 CODEC to select the loss equalization function.

Overvoltage protection

The NT618BA system monitors the A and B leads (tip and ring) of the for overvoltage. When overvoltage occurs, the system isolates the line circuit from the loop through the operation of the cutover relay. The system software releases the relay after the removal of the fault condition.

Overcurrent protection

The self protects against ground faults on the B lead (ring). The card detects the condition. The card limits the current to a level that cannot damage the card.

NT6X18BA (continued)

Voltage regulator

The B11 chip in the NT618BA has a 5V regulator. The regulator takes a reference signal from the line card power supply to stabilize the power source at 5V.

Relays

The NT6X18BA has the following relay types:

- cutover
- test access
- ring
- reversal
- ground start

A cutover relay isolates the NT6X18B line card from the subscriber loop. Features like diagnostics, office installation, and protection of the line card from potential hazards uses the relay.

A test access relay connects the NT618BA A and B leads (tip and ring) of the to the LCM test access bus during testing.

A ring relay connects the LCM ring bus to the NT618BA to ring the near-end telephone.

The reversal relay reverses the A and B lead (tip and ring) connections. Type-A Japan service requires this reversal. The type-B WLC provides the type-A Japan service. North American type-B functions use the type-B WLC.

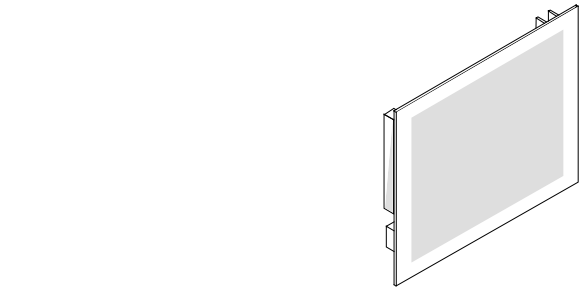
The ground start relay disconnects the A lead (tip) from the line for ground start detection.

Signaling

Pin numbers

The following figure displays the pin numbers for the NT6X18BA.

NT6X18BA pin numbers



Connector P1

	A	B
1A 1B	P-enable*	Lbus
2A 2B	Master clock	RSYNC*
3A 3B	Ground	Ground
4A 4B	+5 V*	Meter
5A 5B	+12.7 V Reference	+48 V/–175 V*
6A 6B	+15 V	–48V Return
7A 7B	–48 V	Cutover hold line
8A 8B	Ring bus/B	Ring bus/A
9A 9B	A	Test access/A
10A 10B	B	Test access/B

* denotes pins that are not used on this card

NT6X19AA

Product description

The NT6X19AA message waiting line card provides an interface. The interface is between a 2-wire analog line of the subscriber and 1 channel of the 4-wire, 32 channel, 2.56 Mbps bit stream of DMS-100 equipment.

The card contains circuits to flash the neon lamp in a message waiting telephone set. The card provides features like the Type-A line card but does not provide multiparty ability.

Location

The card occupies one position in the line drawer (LD) of a line concentrating module (LCM).

Functional description

The NT6X19AA communicates between the analog line of the subscriber and the LCM drawer. The card uses a bidirectional bus to receive and transmit 10 bit pulse code modulation (PCM) samples or control and signaling data. The card contains relays to control ringing, message waiting, testing and maintenance functions.

Functional blocks

The NT6X19AA consists of the following functional blocks:

- line circuit (LC) chip
- supervision network
- message waiting circuit
- VF transformer
- relay driver
- relays
- cutover circuit

LC chip

The LC chip uses a bidirectional bus to receive and transmit PCM samples or signaling and control data. In the receive direction, the circuit decodes the received PCM samples to analog voice frequency (VF) signals. The circuit performs this action to reconstruct the original analog VF signal. The signal passes through the VF transformer to the analog line of the subscriber.

In the transmit direction, the LC chip receives analog VF signals from the equipment of the subscriber. The LC chip converts the signals to PCM samples, and transmits these samples to the bus interface in the LCM drawer.

The LC chip filters the analog signals to limit bandwidth and samples the signals at an 8 kHz rate.

The LC chip uses two balancing networks. One balancing network is for loaded loops and one for nonloaded loops. The LC chip uses these networks to achieve the required singing margin. The chip uses a 2.56 MHz clock to transfer data at the appropriate channel time.

Supervision network

The supervision network detects dial pulse (DP). The supervision network detects on-hook or off-hook supervision signals on the tip (T) and ring (R) leads. The supervision network detects current changes in the loop. The network transmits the signals to the LC chip in digital format.

The network improves the performance of the speech transmission of the VF transformer. The network cancels flux dc line currents produce. The dc line currents produce the flux in the flux balance winding of the VF transformer.

Message waiting circuit

The message waiting circuit receives a 175V supply voltage from the LD. The circuit applies part of the voltage to the T and R leads to turn on the neon message waiting lamp. The circuit uses an oscillator to gate the 175V supply to flash the lamp on and off.

VF transformer

The VF transformer provides an interface between analog facilities and the LC chip in the card. In the receive direction, the transformer converts the signals on the T and R leads to one signal. The receive circuit must process this signal. In the transmit direction, the transformer receives the signal from the transmit circuit. The transformer sends the converted signals out over the T and R leads. The transformer operates with the balancing network to provide four-wire to two-wire conversion.

The transformer functions with the supervision network to cancel flux line currents that flow in the supervision circuits produce. The network and the transformer cancel flux to improve the performance of the transformer for speech transmission.

Relay driver

The relay driver receives coded messages from the LC chip and decodes the messages. The relay driver sends signaling messages to the appropriate relay circuits.

NT6X19AA (continued)

Relays

Four relays are available for ringing, message waiting, testing, and maintenance purposes. The following table lists the relays and associated operated and released functions.

Relay Operation

Relay	Operated	Released
CO,TA	CO operated, TA released: • T and R leads isolated • VF signals on the receive path appear on the transmit path with almost zero loss. TA operated, CO released: • Bridged monitor access is provided to the T and R leads of the subscriber and to the VF transformer Both TA and CO operated with TA contacts closed and CO contacts open: • Subscriber loop tests are applied to the T and R leads through the TA, by the isolation of the subscriber loop from the LC	CO and TA released: • Normal operation
RG	Supervision voltages are disconnected. Signals on the ringing bus replace the supervision voltages.	Normal operation
MSG	Message waiting circuit is enabled. A 150V current is applied to the T and R leads to turn on the neon message waiting lamp.	Normal operation
CO,TA	CO operated, TA released TA operated, CO released TA and CO operated with TA contacts closed and CO contacts open	CO and TA both released
RG	Supervision voltages disconnected. Signals on the ringing bus replace the supervision voltages.	Normal operation
MSG	Message waiting circuit is enabled. A 150V current is applied to the T and R leads to turn on the neon message waiting lamp	Normal operation

Cutover circuit

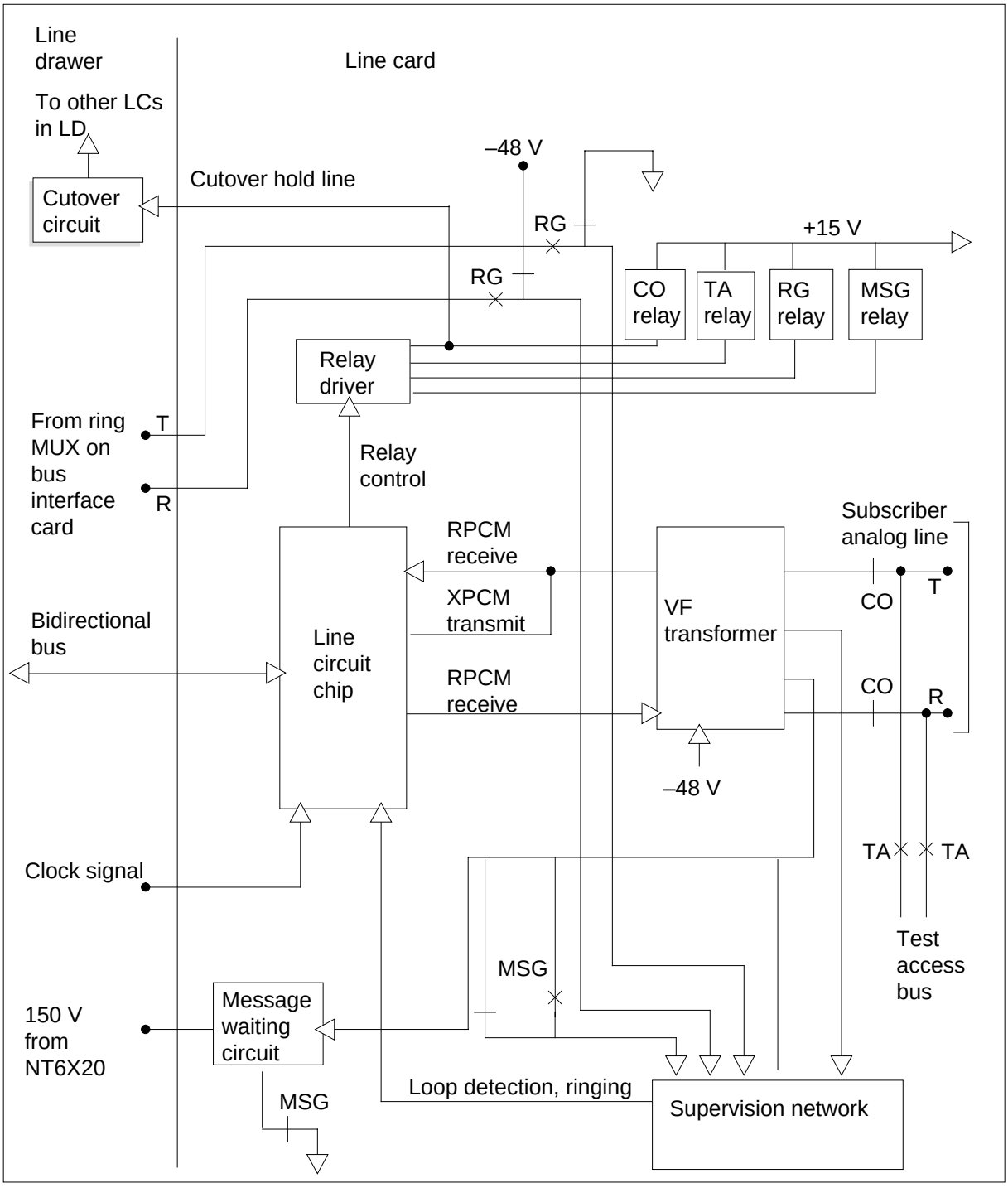
The cutover circuit receives a signal from the CO relay circuit and provides cutover that software controls. The circuit uses the bidirectional bus to address

specific LCs through the bidirectional bus. The circuit activates the CO relay circuit in the addressed LC.

The relationship between the functional blocks appears in the following figure.

NT6X19AA (continued)

NT6X19AA functional blocks



Technical data

The card has short circuit protection. The card is not affected by 60 Hz induction. The signaling characteristics of the card appear in the following tables.

Signaling characteristics

Characteristic	Value
Talk battery nominal voltage	-48.00V
Talk battery extreme range	-42.75V to -55.80V
Normal talk battery range (float charge)	-48.00V to -53.50V
Maximum talk battery discharge (no charge)	-42.75V
Maximum talk battery charge (equalizing)	-55.80V
Ground resistance	50 Ω maximum
Lightning surge protection	1kV (10 y 1000μs)
60-Hz longitudinal or metallic transients	600V rms for 5 s 700V rms for 183 ms
Total loop resistance	1900 Ω maximum
Conductor leakage resistance (minimum)	1M Ω

Transmission specifications

The NT6X19AA has a 900ω, 2.16 μF input impedance. The transmission frequency responses and relative losses appear in the following table.

Transmission frequency responses (Sheet 1 of 2)

Frequency response (Hz)	Relative loss (dB)	
	Min	**Max**
60	20.0	
200	0.0	4.0
300	-0.5	
3000	-0.5	1.0

NT6X19AA (continued)

Transmission frequency responses (Sheet 2 of 2)

Frequency response (Hz)	Relative loss (dB)	
	Min	**Max**
3200	-0.5	1.5
3400	0.0	3.0

The echo return loss (ERL) is 20dB. The singing return loss (SRL) is 14dB. A programmable digital-to-analog (D/A) loss range of 0 to 7 dB in 1 dB increments is available. The line equipment level nominal loss of the analog-to-digital (A/D) path. The D/A path is 0 dBm.

The card has an idle channel noise level of £20 dBrnC. The transhybrid ERL loss of the card is 21 dB. The transhybrid SRL is 14 dB.

The following table lists the envelope delay distortion frequencies and delays.

Envelope delay distortion

Frequency (Hz)	Max. delay distortion (µs)
400	700
600	500
800	350
1004	190
1150	150
2300	150
2500	190
2700	350
3000	500
3200	700

The quantization distortion level and signal/delay distortion ratios appear in the following table.

Quantization distortion

Input level (dBm0)	Signal/distortion ratio (dB) C-message weighted, line-to-line
0 to -30	≥33
0 to -40	≥27
0 to -45	≥22

The longitudinal balance of the signal appears in the following table.

Longitudinal balance

Frequency (Hz)	Minimum balance (dB)
60	≥47
204	≥53
1004	≥58
3004	≥53

The lamp interface has -130V minimum open circuit voltage, a nominal flash rate of 75 interruptions per minute (IPM), and a nominal 38% duty cycle.

Physical dimensions

The physical dimensions of the NT6X19AA are:

- height: 73 mm (2.875 in.)
- depth: 22 mm (0.875 in.)
- width: 89 mm (3.5 in.)

Power requirements

The converter voltage has a power requirement of +15V ±300mV. The reference voltage in the bus interface card has a power requirement of +12.7V ±50mV. The message waiting voltage from the NT6X20 converter has a -175V nominal power requirement.

NT6X20AA

Product description

The NT6X20AA message waiting (MWT) power converter line card (LC) provides the voltages that light MWT lamps. The message center uses the MWT lamp and the call request features. The message center uses these features to indicate to a user station that the system receives a message. The state of the lamp informs the user station that the system queues a message. The state of the lamp is flashing or off. The NT6X20AA provides a -150V synchronized pulse for the MWT lamp circuit.

Location

The NT6X20AA occupies two vertical slots in the add line subgroup (LSG) in the line drawer (LD). Slots 0 and 16 must contain the NT6X20AA.

For BCS-28, the must be in LSG1 in each drawer. Each drawer is logical drawers 1, 4, 7, 10, 13, 16, 19 and 22. In BCS-29, this restriction is not present. The converter can be in any logical drawer.

Note: An LSG that contains ISDN line cards cannot contain type E line cards or the NT6X20AA.

Functional description

The system routes an incoming trunk call or an internal call automatically to a message center. This event occurs if the original destination does not answer the call. The MWT lamp flashes on the telephone unit at the original destination. The MWT flashes to indicate that the system receives a message and waits. The lamp is off if messages are not in a queue for the station. The station is on-hook or off-hook in this occurrence. If messages are in the queue for the station and the station is on-hook, the lamp is on. The lamp flashes at 60 interruptions per minute (IPM). The lamp follows the ringing pattern to provide a visual indication of the station ringing.

Stations with the MWT lamp capability require a special LC on a line concentrating module (LCM). Each telephone that uses an MWT lamp must have a standard type E MWT LC (NT6X19AA). The NT6X19AA provides features like LC type A and a single- or two-party interface. This interface is between a two-wire analog line of the subscriber and one channel of the four-wire, 32-channel, 2.56 Mbit/s stream. The switching system uses this stream. Refer to the NT6X19AA hardware description for more information about the MWT LC.

The type E standard LC works with the NT6X20AA and requires the NT6X20AA to function. Each drawer with an MWT LC must have an NT6X20AA for the lamp power supply. The monitoring circuits use neon

lamps. The NE-500-YR and the NE-2500YQA sets use these lamps. These lamps operate according to NT specification NPS25008. The NT link telephone sets can accommodate an MWT lamp.

To use 500 or 2500 sets with neon lamps of other manufacturers, check the lamps. Make sure the lamps perform the following functions:

- the lamps light and extinguish correctly when the lamps connect to the NT6X20AA and NT6X19AA circuits.
- the lamps draw enough current to provide the correct limiting resistor value in the lit state. The limiting resistor value must satisfy the lamp fail monitor circuit conditions.

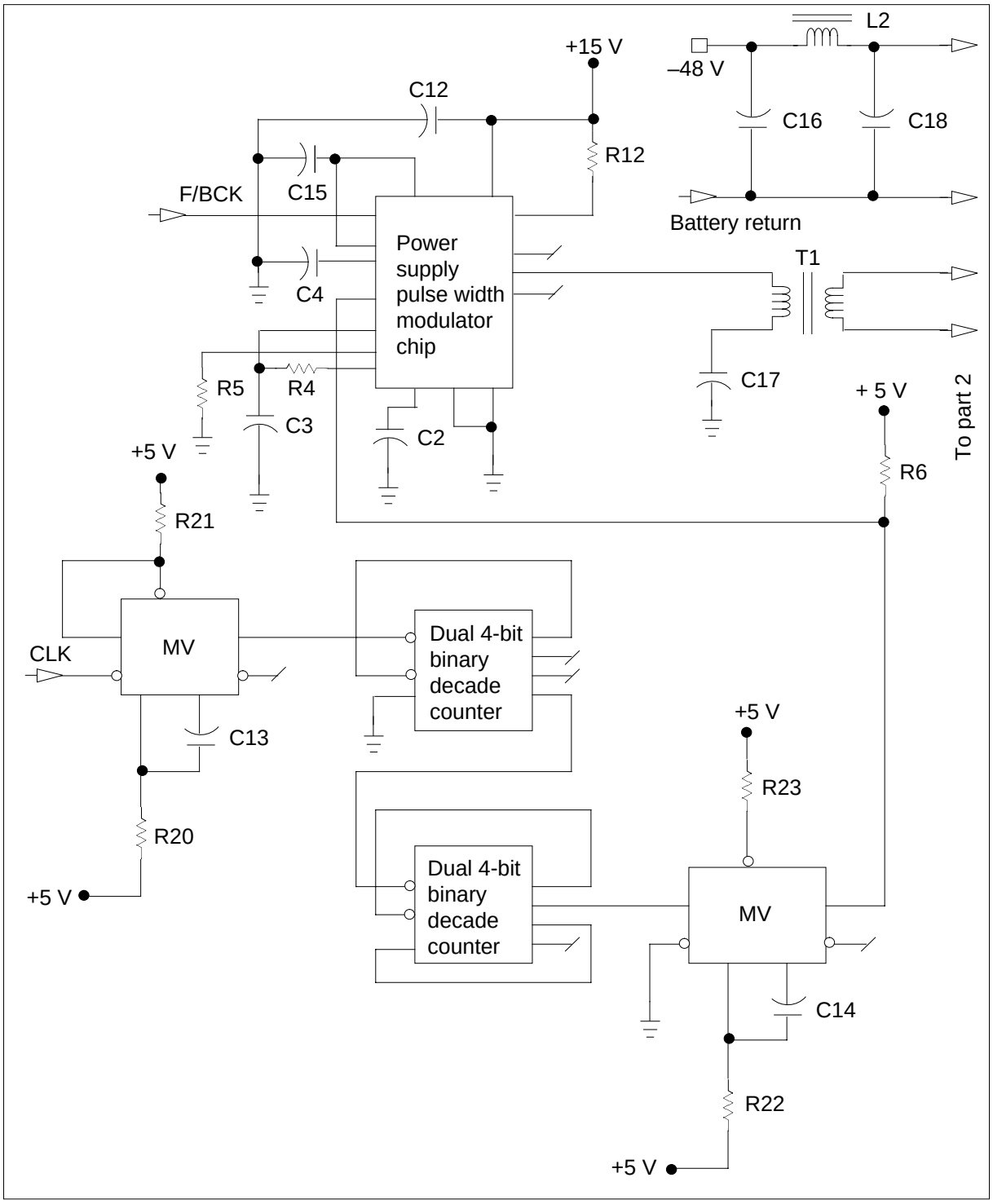
Each LD can have one NT6X20AA assigned. An LD cannot contain the LC type E that requires message waiting and the LC type B that requires fraud prevention feature.

The lamp driver hardware requires two adjacent LC slots in a drawer. Stations that require the MWT lamp capability must be in a drawer with the lamp driver package. Each drawer has one lamp driver package. Drawers that have the lamp driver hardware can have 62 LCs and not 64. The drawers can have 62 LCs because of the NT6X20AA.

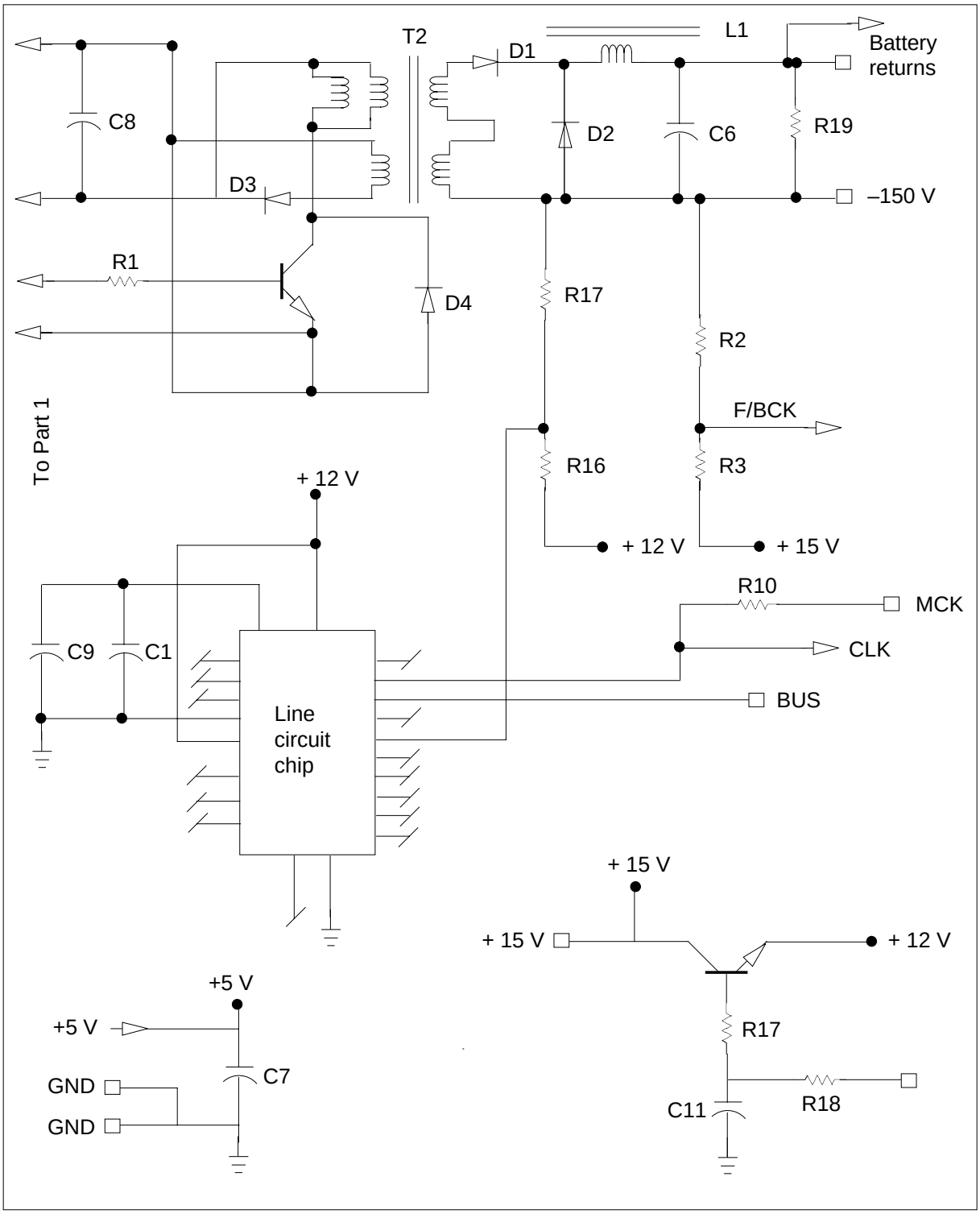
The NT6X20AA circuits appear in the following figures.

NT6X20AA (continued)

NT6X20AA circuit diagram (Part 1)



NT6X20AA circuit diagram (Part 2)



NT6X20AA (continued)

Technical data

The technical data section provides specifications for the following parts of NT6X022AA:

- power requirements
- equipment dimensions
- environmental conditions
- specifications for connections

Power requirements

The NT6X022AA input specifications appear in the following table.

Power requirements

Input	Minimum	Nominal	Maximum
Voltage (Vdc)	-42	-48	-56
Current (Adc)	-----	-----	0.75

The NT6X022AA output specifications appear in the following table.

Power requirements

Output	Minimum	Nominal	Maximum
Voltage (V)	-165.0	-175.0	-185.0
Current (A)	-----	-----	0.075

Equipment dimensions

The NT6X20AA dimensions are 89.74 mm (3.5 in.) high, 22.84 mm (0.9 in.) wide, and 152.28 mm (6.0 in.) deep. The approximate weight of the NT6X20AA is 881 g (0.4 lb).

Environmental conditions

The NT6X20AA performs under limited environmental controls. These controls appear in the following table.

Ambient conditions

Condition	Operating range	Short-term range
Temperature	0°C to 55°C (50°F to 86°F)	0°C to 65°C (41°F to 120.2°F)
Airflow	Natural	Natural
Relative humidity	20% to 55%	20% to 80%

Connections

There are no electrical connections applied to the P1 connector. The NT6X20AA P2 connector pin assignments appear in the following table.

Connections

Row	Column A	Column B
1	N/C	BUS
2	MCK	N/C
3	GND	GND
4	+5V	N/C
5	+12.7 V	-175 V
6	+15V	-48 VR
7	-48 V	N/C
8	N/C	N/C
9	N/C	N/C
10	N/C	N/C

NT6X21AC

Product description

The NT6X21AC P-phone line card 15 kft provides voice and signaling interfaces. The card provides interfaces between two-wire analog subscriber lines that use business sets and the digital bit stream. The stream is four-wire, 32 channel, 2.56 Mbit/s digital bit stream. The stream is from of the DMS-100 switch.

Each card supports one business set and three addressable add-on units. The voice and the signaling paths can be active at the same time. The card contains a set presence detector that generates an absence report when a set is not present. The detector prevents error messages in the maintenance system.

Location

The card occupies one position in a line concentrating module (LCM) drawer.

Functional description

The NT6X21AC communicates between the business set line card and the LCM drawer. The NT6X21AC uses a bidirectional bus to receive and transmit 10 bit pulse code modulation (PCM) samples or control or signaling data. The system sends data that the DMS-100 central control (CC) selects. An enable signal controls the data transmission. The signal sends the data tone to the following:

- the signaling chip for a signaling transfer
- the line circuit (LC) chip for speech or control transfer

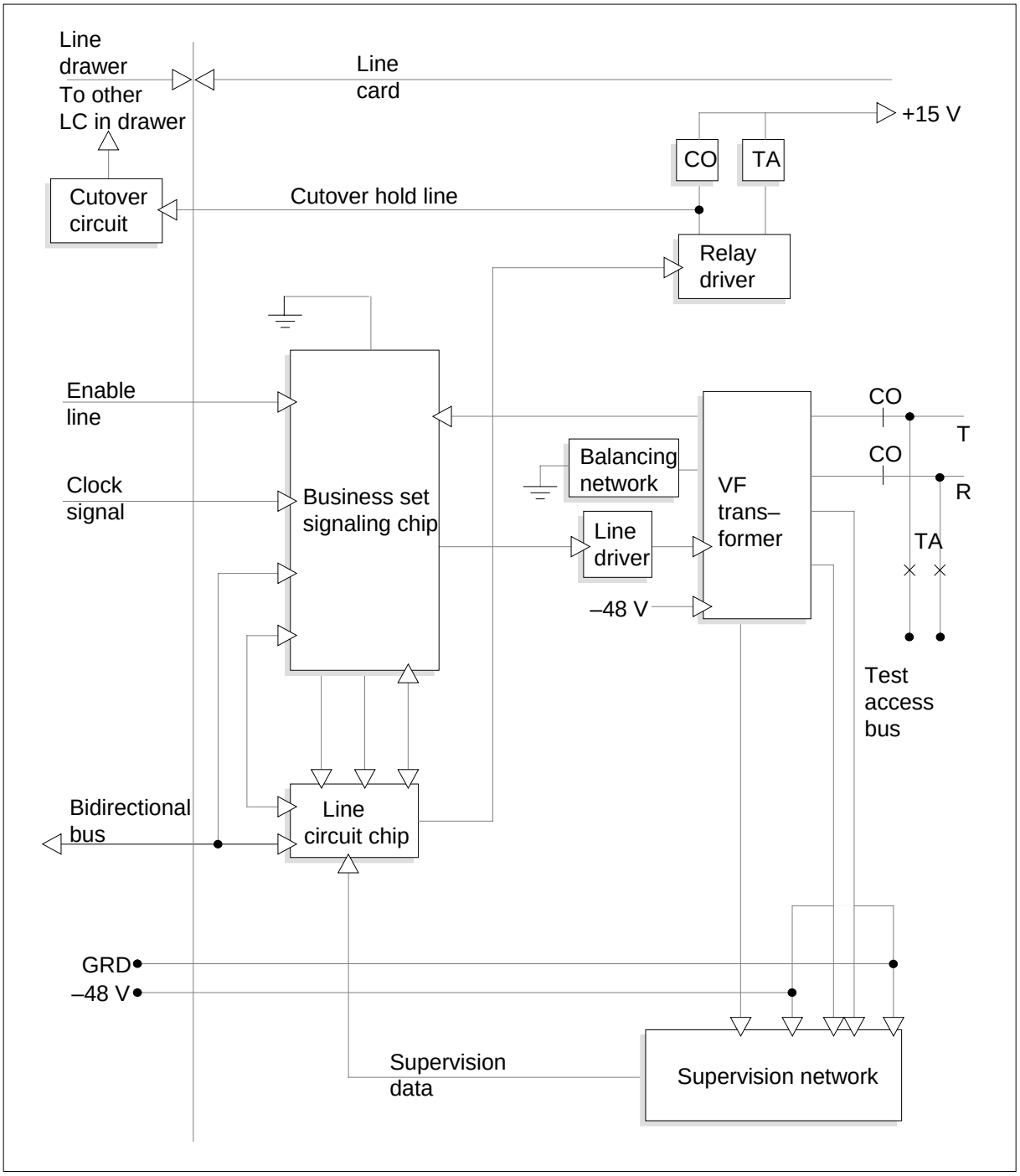
Functional blocks

The NT6X21AC contains the following functional blocks:

- line circuit (LC) chip
- business set signaling chip
- supervision network
- voice frequency (VF) transformer
- line driver
- balancing network
- relay driver
- relays
- cutover circuit

The relationship between the functional blocks appears in the following figure.

NT6X21AC functional blocks



NT6X21AC (continued)

LC chip

The LC chip receives and transmits PCM samples with a bidirectional bus. In the receive direction, the circuit decodes the received PCM samples to analog voice frequency signals. The circuit decodes the samples to construct the original analog VF signal again. The system passes the signal through the business set signaling chip and the VF transformer. The system passes the signal to the analog line of the subscriber.

In the transmit direction, the LC chip receives analog VF signals from the equipment of the subscriber. The LC chip converts the signals to PCM samples. The LC chip transmits the samples to the bus interface in the LCM drawer. The chip filters the analog signals to limit the bandwidth of the signals. The chip samples the signals at an 8-kHz rate.

The LC chip accepts PCM samples from the NT6X79 tone generator card when ringing is a requirement. The LC chip uses a 2.56 MHz clock to transfer data at the correct channel time.

Business set signaling chip

The signaling chip filters VF signals and modulated signals. The system uses voice-band low-pass filters to filter VF signals. The system uses band-limiting filters to filter the demodulator and modulator. This chip provides the following:

- a digital interface compatible with the serial bus configuration.
- a digital interface to the amplitude shift keying (ASK) modem.
- an analog interface compatible with the four-wire interface of the LC chip.

The signaling chip uses a looparound feature to check the accuracy of the signaling protocol. The chip checks the accuracy at the subscriber loop side and the bidirectional bus side of the circuit.

Supervision network

The supervision network reads current changes in the loop to detect if a P-phone set is present on the loop. The network controls the current in the flux balance winding of the VF transformer.

VF transformer

The VF transformer provides an interface between the LC chip in the card and the analog facilities. In the receive direction, the transformer converts the signals on the tip (T) and ring (R) leads to one signal. The receive circuit processes this signal. In the transmit direction, the transformer receives the signal from the transmit circuit. The transformer sends the converted signals

over the T and R leads. The transformer works with the balancing network to provide four-wire to two-wire conversion.

The transformer works with the supervision network to cancel any flux. Line currents that flow in the supervision circuits produce flux. Line currents that flow in the supervision circuits improve the quality of the transformer for speech transmission.

Line driver

The line driver receives signals from the business set chip. The driver sends the signals to the VF transformer for transmission to the T and R lines of the subscriber.

Balancing network

The balancing network provides the required singing margin on all subscriber loops. The network works with the VF transformer to provide four-wire to two-wire conversion.

Relay driver

The relay driver receives coded messages from the LC chip. The relay driver decodes the messages and sends signaling messages to relay circuits.

NT6X21AC (continued)

Relays

This feature provides two relays for test purposes. The relays and the operated and released functions of the relays appear in the following table.

Relay Operatio

Relay	Operated	Released
CO,TA	CO operated, TA released: • T and R leads are isolated • VF signals on the receive path appear on the transmit path with approximately zero loss TA operated, CO released: • The system provides bridged monitor access to the T and R leads of the subscriber and to the VF transformer Both TA and CO operated with TA contacts closed and CO contacts open: • Subscriber loop tests use the TA to apply the tests to the T and R leads. The TA isolates the loop of the subscriber from the LC.	CO and TA both released, normal operation

Cutover circuit

The cutover circuit receives a signal from the CO relay circuit and provides software-controlled cutover. The circuit uses the bidirectional bus to address a specified LC and activate the CO relay circuit in the addressed LC.

Technical data

The card has short-circuit protection. The 60-Hz induction is normal with a maximum 20 mA for each conductor. The card has two ringing tones that alternate alternate at 9 Hz ±2 Hz. The tones are a 516 Hz ±10 Hz tone and a

649 Hz ±10 Hz tone. Both tones have -4 dBm ±5dB level. The signaling characteristics of the card appear in the following table.

Signaling characteristics

Characteristic	Value
Talk battery nominal voltage	-48.00 V
Talk battery extreme range	-42.50 V to -55.80 V
Normal talk battery range (float charge)	-48.00 V to -53.50 V
Maximum talk battery discharge (no charge)	-42.50 V
Maximum talk battery charge (equalizing)	-55.80 V
Lightning surge protection	1 kV (10 x 1000 µs)
60-Hz longitudinal or metallic transients	480 Vrms for 183 ms 600 Vrms for 5 s
Maximum loop range (nonloaded loop)	4.5 km (15 kft) of 26 AWG
Insertion loss limit	24 dB at 8 kHz
Conductor leakage resistance (maximum)	10 M Ω

Transmission specifications

The NT6X21AC card uses a different bidirectional bus for each business set line. The NT6X21AC card uses an enable signal common to all business set line cards in a line drawer. The card uses the signal to receive and transmit signals. The transmission characteristics of the card appear in the following table.

Transmission characteristics (Sheet 1 of 2)

Characteristic	Value
Modulation technique	ASK, half-duplex
Carrier frequency	8 kHz ±2%
Bit length	1 ms
Message length	16 ms
Message interval	23 ms
Maximum carrier transmit level	730 mVp

NT6X21AC (continued)

Transmission characteristics (Sheet 2 of 2)

Characteristic	Value
Minimum carrier transmit level	540 mVp
Minimum carrier receive level	24 mVp

The NT6X21AC has a 3.5-dBm transmission level point (TLP) at the main distribution frame (MDF) and an overload level of +3.17 dBm0. The transmission frequency responses and relative losses appear in the following table.

Transmission frequency responses

Frequency responses (Hz)	Relative loss (dB)	
	Min	**Max**
60	20.0	-
200	-0.0	4.0
300	-0.5	1.0
3000	-0.5	1.0
3200	-0.5	1.0
3400	0.0	3.0

The transmission echo return loss (ERL) is ≥20 dB and the singing return loss is ≥14 dB. The programmable D-A loss range is 0 through 7 dB in 1-dB increments. The nominal loss level of the line equipment level of A through D path is 0 dBm. The nominal loss of D through A path is 3.5 dBm.

The card has an idle channel noise level of ≦23dBrnC and a transhybrid ERL loss of ≥21 dBSRL.

The envelope delay distortion frequencies and delays appear in the following table.

Envelope delay distortion

Frequency (Hz)	Maximum delay distortion (µs)
400	700
600	500
800	350
1004	190
1150	150
2300	150
2500	190
2700	350
3000	500
3200	700

Quantization distortion level and signal/delay distortion ratios appear in the following table.

Quantization distortion

Input level (dBm0)	Signal/delay distortion ratio (dB)
0 to -30	≥33
0 to -40	≥27
0 to -45	≥22

Dimensions

The dimensions of the NT6X21AC are as follows:

- height: 73 mm (2.875 in.)
- depth: 22 mm (0.875 in.)
- width: 89 mm (3.5 in.)

NT6X21AC (end)

Power requirements

WARNING

Damage to equipment or loss of service

Use only on telephone wiring protected by a Nortel Networks protector, catalog number 303M-12AIKE. Use with a 26-AWG copper wire with thermoplastic insulation. The maximum fusing wire to use in series with the protector is 26 AWG.

The consumes 300 mW of power and converts voltages of +15 V ±0.5 V and +12.7 V ± 1%.

NT6X21AD

Product description

The NT6X21AD line card provides a voice and signaling interface. The interface occurs between two-wire analog subscriber lines with business sets and the four-wire, 32 channel, 2.56 Mb/s digital bit stream of the DMS-100 switch

This line card is the same as the NT6X21AC line card except for the following differences:

- lower messaging noise.
- the 900 Ω +2.16 µF balance impedance option.
- the 0 or -3.5 dB gain option in the digital to analog (D/A) path.

Each card supports one business set and three add-on units that can be addressed. The voice and the signaling paths can be active at the same time. The card contains a set presence detector that generates an absence report when a set is not available. The detector prevents error messages in the maintenance system.

Location

The card occupies one position in a drawer of one of the following peripherals:

- Line concentrating module (LCM)
- ISDN line concentrating module enhanced (LCME)
- ISDN line concentrating module (LCMI)
- International line concentrating module (ILCM)
- Remote line concentrating module (RLCM)
- Outside plant module (OPM)
- Small remote unit (SRU)
- Remote switching center (RSC)
- ISDN remote switching center (RSCI)
- Sonet remote switching center (SRSC)
- Extended memory line concentrating module (XLCM)
- Remote extended memory line concentrating module (XRLCM)

Functional description

The NT6X21AD communicates between the business set line card and the LCM drawer. The NT6X21AD uses a 2-directional bus to receive and transmit

NT6X21AD (continued)

10-bit pulse code modulation (PCM) samples or control or signaling data. The DMS-100 central control (CC) selects data. An enable signal controls the data. The system sends data to the signaling chip for a signaling transfer. The system can also send data to the line circuit (LC) chip for speech or control transfer.

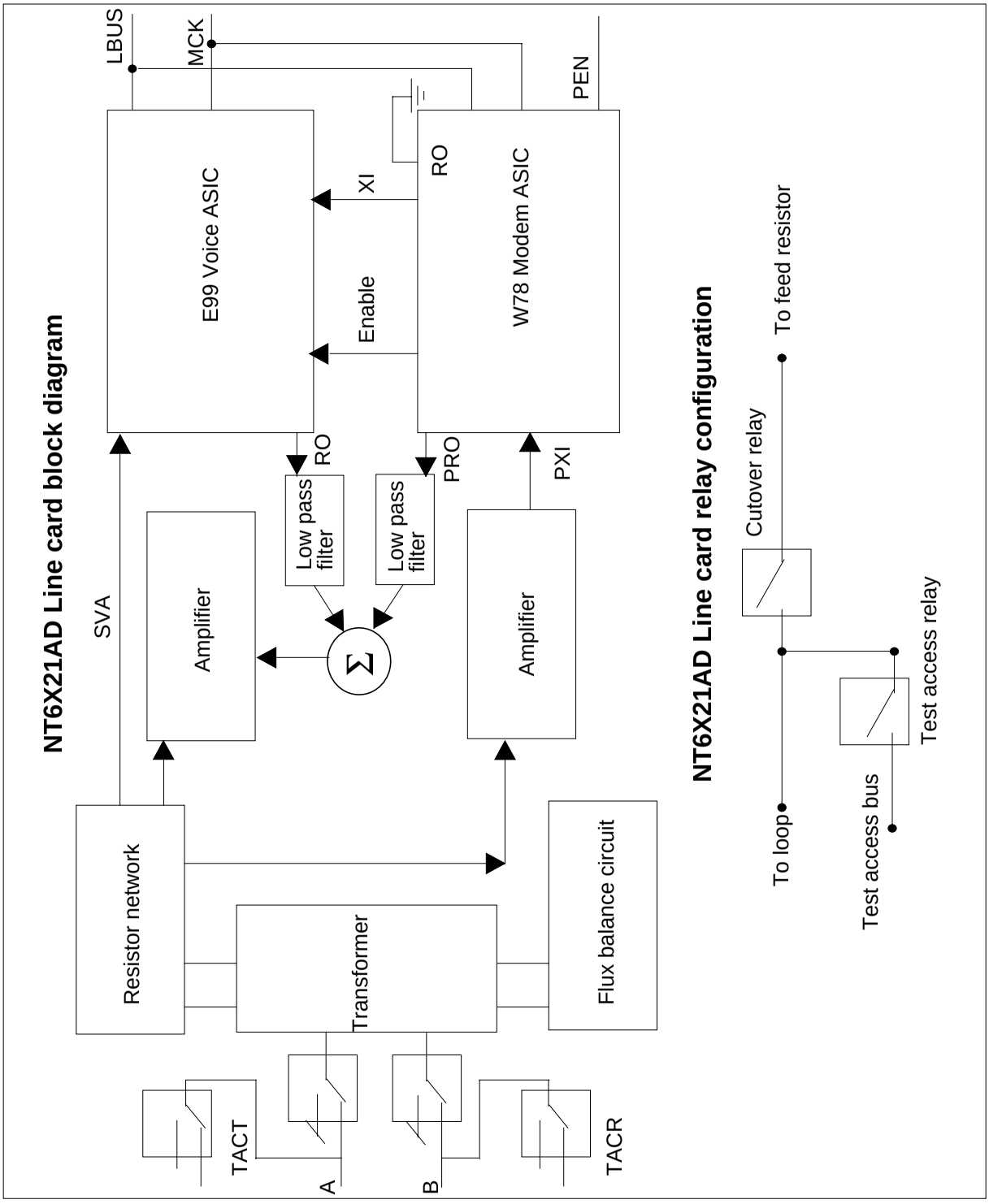
Functional blocks

The NT6X21AD has the following functional blocks:

- E99 voice ASIC
- W78 modem ASIC
- resistor network
- flux balance circuit
- high pass filter
- low pass filter

The relationship between the functional blocks appears in the following figure.

NT6X21AD functional blocks



NT6X21AD (continued)

Supervision

The W78 (modem chip) or the E99 (voice chip) can supply supervision (SV0 and SV1) on the LBUS. The supply of supervision depends on the state of PEN (P-enable), pin 1A on the line card connector. The state of PEN for this supply occurs during the start bit of an LBUS transaction. When PEN is low during the start bit, the LBUS transaction communicates with the W78. The SV0 and SV1 from the W78 indicate message transmission or reception status. The SV0 from E99 indicates when the loop current is above the set-presence threshold.

Loop detection

The talk battery of the NT6X21AD connects to the subscriber A and B leads. The connection is through a pair of feed resistors on the battery feed thick film resistor network and the transformer. The total resistance of the feed resistors and the transformer is normally 440 Ω.

A voltage measurement bridge performs the loop detection. A voltage measurement bridge compares two voltages. For loop detection, one voltage is at the exact center point between tip (T) and battery (-48V). The second voltage is at the exact center point between ring (R) and battery return (-48V rtn). This difference is amplified, and biased to new dc levels for ordinary electronic components.

The loop current threshold indicates set presence. The phone set draws a minimum of 4.5mA. The exception to this rule is the ACD set with a headset. When the headset is unplugged, the phone set loop current becomes less than 2mA.

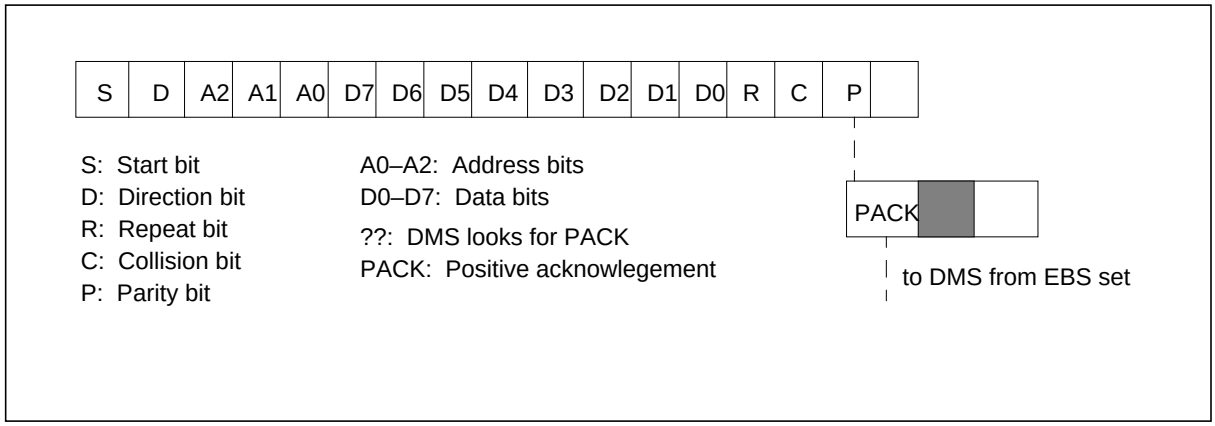
Loop current limit

The phone set is a current sink that limits loop current to less than 38 mA.

Signaling

The W78 provides the amplitude shift keying (ASK) signaling interface between the EBS business feature set and the DMS switch. The loop (tip-ring) side of the device provides an 8 kHz carrier. A 1 kb/s signal that uses ASK modulates the 8 kHz carrier. The ASK turns on the 8 kHz for 1 bit and turns off the 8 kHz for 0 bit. The ASK is an asynchronous protocol and has a specified addressing structure which appears in the following figure.

Asynchronous protocol



The PRO is the signaling output of the W78 chip. The PXI is the signaling and voice input to the W78 chip.

Voice frequency transmission

Loop termination

A resistor and capacitor on the center tap of the secondary of the transistor combines the NT6X21AD input impedance. The input impedance required of the NT6X21AD is 900 Ω + 2.16 µF.

Voice path

The E99 chip receives the receive (D-A) signal on the LBUS. The E99 chip decodes and filters the signal. The E99 chip transmits the signal out the RO+ and RO- outputs. Additional gain and filtering occurs outside the E99 before the sum of the voice path occurs with the signaling path.

A set of software controlled bits and a DIP switch controls the D-A gain. The software control provides a nominal gain in the D-A path. The range of this gain is 0 to -7 dB in 1 dB steps. The bits DAG3, DAG2 and DAG1 set this nominal gain. The Call Processing Software alters these bits. This process depends on how the specific call is routed. This functionality is an internal part of the DMS-100 call processing software. The NT6X21AD provides DIP switch selection of 0 or -3.5 dB D/A levels. The -3.5 dB selection maintains backward compatibility. As a result, the D/A levels that the DAG3-DAG1 and the DIP switch controls can be from 0 to -10 dB.

NT6X21AD (continued)

Hybrid balance

The transmit signal contains components of the receive signal. Removal of components must occur before the transmit signal can be encoded and put on the two way bus. This function is a hybrid balance. The balance filter accomplishes this function. There are two DIP switch-selectable balance filters on the NT6X21AD. The line card meets the balance impedance specifications.

The NT6X21AD balance impedance is set to 900 Ω + 2.16 µF or 800 Ω //(100 Ω+ 50 nF).

Power supplies

A 15V rail and a 12.7V precise high-impedance reference are supplied to the line card. The 10V, 12V and 7.5V supplies derive from the 15V rail and 12.7V precise high-impedence reference. An AGND (analog ground, at 5V) regulator is an integral part into the W78 chip.

Relays

Cutover relay

The cutover relay isolates the line card from the loop. Use the cutover relay for diagnostics and office installation.

Test access

The NT6X21AD line card test access relay allows bridged access to the A and B leads for testing purposes. Operation of this relay connects the A and B leads of the subscriber loop on the LCM test access bus. Operation of the cutover relay at the same time as the test access relay can occur. This action separates the line card from the subscriber loop and from the test access bus. This action

allows the maintenance equipment to test the loop alone, and the loop with the line card that drives the loop.

	D/A voice (S1)		Balance (S2)		Signaling level (S3)			
	On	Off	On	Off	Both On	Only S4 On	Only S3 On	Both Off
Application	**0 dB**	**-3.5 dB**	**NL**	**9+2**	**1.3Vpp**	**0.8Vpp**	**0.6Vpp**	**0.14Vpp**
MBS phone sets long loops: 21-24 dB EML	x		x		x			
MBS phone sets medium loops: 17-21 dB EML	x		x			x		
MBS phone sets medium loops: 4-17 dB EML		x		x			x	
MBS phone sets short loops: 0-4 dB EML		x		x				x
Northern Telecom UDLCs		x	x					x
Other vendor UDLCs	x			x			x	
NT6X21AC equivalent		x	x		x			

Note: NL = non-loaded, Vpp = voltage peak to peak, EML = estimated measured loss, UDLC = universal digital loop carrier

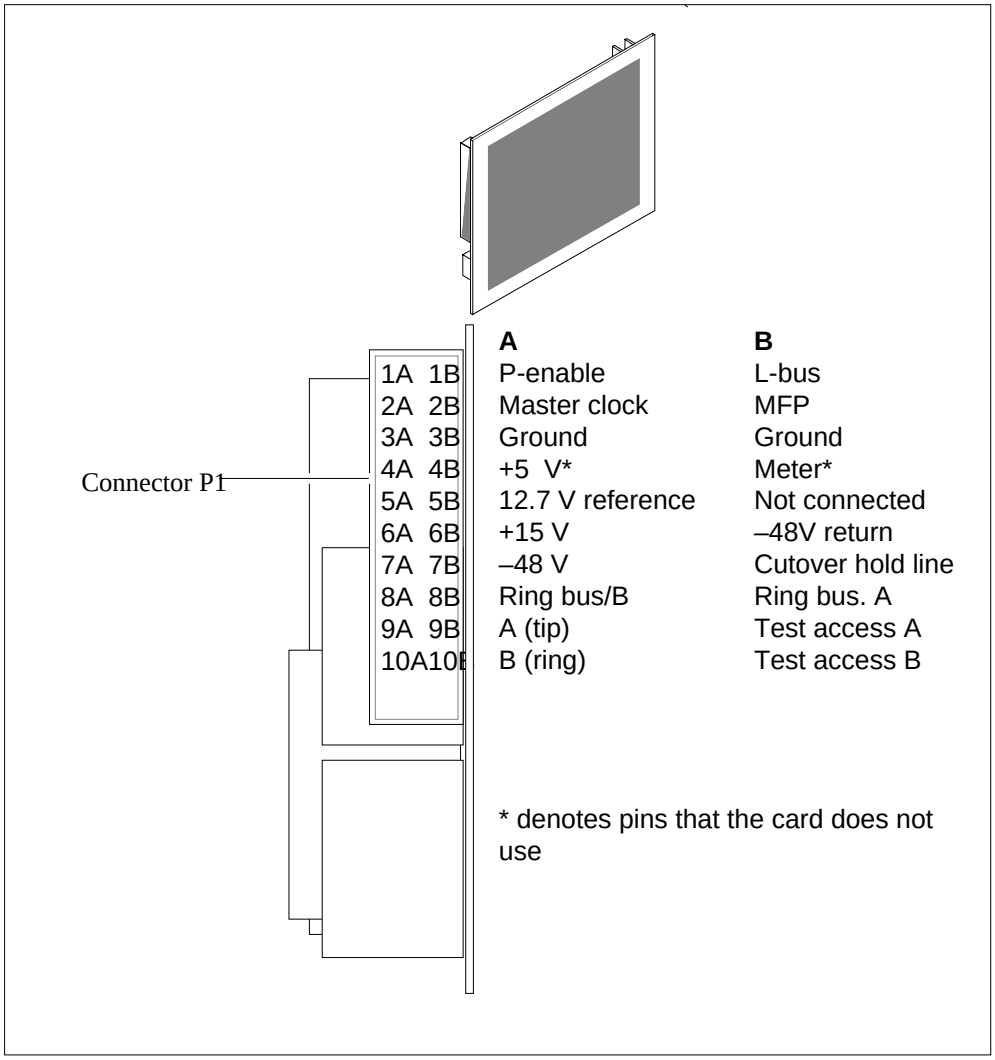
Signaling

Pin numbers

The pin numbers for the NT6X21AD appear in the following figure.

NT6X21AD (continued)

NT6X21AD P1 pin numbers



P1 Pin number description (Sheet 1 of 2)

Pin	Signal	Description
1A	P-enable	Directs 2-directional, 1-wire serial communications link (LBUS) message to application specific integrated circuit (ASIC) W78 when low during start bit.
2A	Master clock	Clock for LBUS.
3A	Ground	

P1 Pin number description (Sheet 2 of 2)

Pin	Signal	Description
4A	+5 V	The card does not use this pin
5A	12.7V reference	ASIC E99 precision reference
6A	+15 V	Line card supply: creates +10V and +12V rails
7A	-48 V	Talk battery low
8A	Ring bus/B	Ring signal low
9A	A (tip)	Subscriber interface high
10A	B (ring)	Subscriber interface low
1B	LBUS	MSG & PCM digital interface
2B	MFP	Multi-function protector
3B	Ground	
4B	Meter	The card does not use this pin
5B	NC	Not connected
6B	-48V return	Talk battery high
7B	Cutover hold line	For cutover of all lines at the same time
8B	Ring bus/A	Ring signal high
9B	Test access A	Test bus high (tip)
10B	Test access B	Test bus low (ring)

Technical data

Transmission specifications

The NT6X21AD card uses a two way bus unique to each business set line to receive and transmit signals. The NT6X21AD card also uses an enable signal common to all business set line cards in a line drawer. The NT6X21AD card

NT6X21AD (continued)

uses this signal to receive and transmit signals. The transmission characteristics of the card appear in the following table.

Transmission characteristics

Characteristic	Value
Modulation technique	ASK, half-duplex
Carrier frequency	8 kHz ±2%
Bit length	1 ms
Message length	16 ms
Message interval	23 ms
Maximum carrier transmit level (long loop)	770 mVp
Minimum carrier transmit level (long loop)	630 mVp
Maximum carrier transmit level (short loop)	77.5 mVp
Minimum carrier transmit level (short loop)	67.5 mVp
Maximum carrier receive level	560 mVp
Minimum carrier receive level	25 mVp

The transmission gain/frequency distortion for an analog to digital path appears in the following table. Measurements are subject to 1000 Hz @ 0 dBm0.

Transmission gain/frequency distortion

Frequency response (Hz)	Gain (dB)	
	Min	Max
60		<-20.0
300	-1.5	0.4
1700	-0.5	0.4
2800	-1.0	0.3
3000	-1.0	0.3
3400	-2.0	0.0

The transmission gain/frequency distortion for a digital path to an analog path appears in the following table. Measurements are subject to 1000 Hz @ 0 dBm0.

Transmission gain/frequency distortion

Frequency response (Hz)	Gain (dB)	
	Min	**Max**
300	-0.96	0.3
1700	-0.5	0.4
2800	-1.0	0.4
3000	-1.0	0.5
3400	-2.40	0.0

The transmission echo return loss (ERL) is ≥24.5 dB. The singing return loss is ≥19 dB, with a programmable D-A loss range of 0 through 7 dB in 1-dB increments. The line equipment level nominal loss of A through D path is 0 dBm. The nominal loss of D through A path is 3.5 dBm.

The card has an idle channel noise level of <20 dBrnC.

The group delay distortion frequencies and delays appear in the following table.

Group delay distortion

Frequency (Hz)	Max. delay distortion (ms)
400 - 3200	0.35
600 - 3000	0.25
800 - 2800	0.175
1000 - 2600	0.095
1150 - 2300	0.075

NT6X21AD (continued)

The total distortion appears in the following table. The total distortion includes the quantization distortion level ratios.

Quantization distortion

Input level (dBm0)	Minimum signal to total distortion ratio (dB)
-45	24
-40	28
-30	35
0	35

Signaling and supervision

The talk battery limits appear in the following table.

Talk battery limits

52 V battery	Characteristic
Normal	-48V to -53.5V
Extreme	-42.75V to -55.8V

Front end dc feed characteristics

The NT6X21AD provides a dc feed resistance of 440 Ω. This parameter cannot be selected. The feed resistance is present during all line card states and cannot change.

Loop range

The loop range is as follows:

1. 4572 m (15 000 ft) or 24 dB insertion loss. This event occurs at 8 kHz and 1240 Ω loop resistance for direct connection to EBS terminal equipment, or
2. <100 Ω dc resistance or <3.3 dB cable loss at 8 kHz for connection to EBS active line unit UDLC transport systems.

Loop leakage resistance

The minimum conductor leakage resistance is 120 kΩ tip to ring, tip to ground or ring to ground.

Induction

The NT6X21AD meets signaling and supervision requirements with 20 mA rms for each conductor of induced 60 Hz ac.

Extended signaling and supervision

The proprietary interface sends the following messages to the NT6X21AD:

- on/off hook supervision
- dial information
- special feature activation from/to the subscriber

The system transmits the ASK, half-duplex signaling on an 8-khz carrier at 1 kb/s, 16 bits for each message.

Addressing

The MBS set provides addressing information encoded in the ASK signaling design. The XPM on the C-side of the LCM holds the MBS line card. The XPM decodes the addressing information. The XPM provides the correct route information to the DMS computing module (CM). Dual tone multi-frequency (DTMF) and dial pulse (DP) are not valid addressing designs for MBS loops.

Ringing

To provide ringing on the MBS set, turn on the speaker. The ringing on the MBS set requires a voice frequency voice-level signal on the T and R. This signal acts as the alerting signal.

Messaging description

The NT6X21AD supplies MBS messaging at 8 kHz ± 2% carrier and 1 kb/s ± 2 % ASK modulation.

ASK messaging level

To set the messaging level, use the DIP switch. The messaging level follows:

- 1.5± .2Vpp for loops over 100Ω dc (external copper loop type)
- 130 to 150 mVpp for loops less than 100Ω dc (internal central office and very short loops),
- 1Vpp or 600Vpp for use with EBS equipment with limited receiver sensitivity.

Impulse noise during messaging

The impulse noise measured during the metering tone does not exceed -35 dBm0. The NT6X21AD terminates in the nominal impedance for the MBS set at 900Ω +2.16 µF.

NT6X21AD (end)

Dimensions

The dimensions of the NT6X21AD are as follows:

- height: 76 mm (2.994 in.)
- depth: 22 mm (0.875 in.)
- width: 89 mm (3.5 in.)

Power requirements

The NT6X21AD consumes 300mW of power and converts voltages of +15V ±0.5V and +12.7V ± 1%.

NT6X21BC

Product description

The P-phone line card (NT6X21BC) provides a voice and signaling interface between two-wire analog subscriber lines with business sets and the four-wire, 32 channel, 2.56 Mb/s digital bit stream of the Digital Multiplex System (DMS).

The NT6X21BC line card is the identical to the NT6X21AC line card except for the following differences:

- lower messaging noise.
- the 900 Ω +2.16 µF balance impedance option.
- -3.5 dB gain option in the digital to analog path from pulse code modulation (PCM) to tip and ring
- 5.2 dB gain option in the analog to digital path from tip and ring to PCM.
- used in the United Kingdom (UK).

The NT6X21BC line card supports one business set and addresses three add-on units. Voice and signaling paths can be active at the same time. The NT6X21BC line card contains a set presence detector that generates an absence report when a set is not available. The detector prevents error messages in the maintenance system.

Location

The NT6X21BC line card is in one position in a drawer of the next peripherals:

- Line concentrating module (LCM)
- ISDN line concentrating module enhanced (LCME)
- ISDN line concentrating module (LCMI)
- International line concentrating module (ILCM)
- Remote line concentrating module (RLCM)
- Outside plant module (OPM)
- Small remote unit (SRU)
- Remote switching center (RSC)
- ISDN remote switching center (RSCI)
- Sonet remote switching center (SRSC)
- Extended memory line concentrating module (XLCM)
- Remote extended memory line concentrating module (XRLCM)

NT6X21BC (continued)

Functional description

The NT6X21BC line card provides an interface between the business set line card and the LCM drawer. The NT6X21BC line card uses a 2-directional bus to receive and transmit 10-bit PCM samples, or control or signaling data. The central control (CC) of the DMS switch selects data and an enable signal controls the data selected. The DMS switch sends data to the signaling chip for a signaling transfer. The DMS switch can send data to the line circuit chip for speech or control transfer.

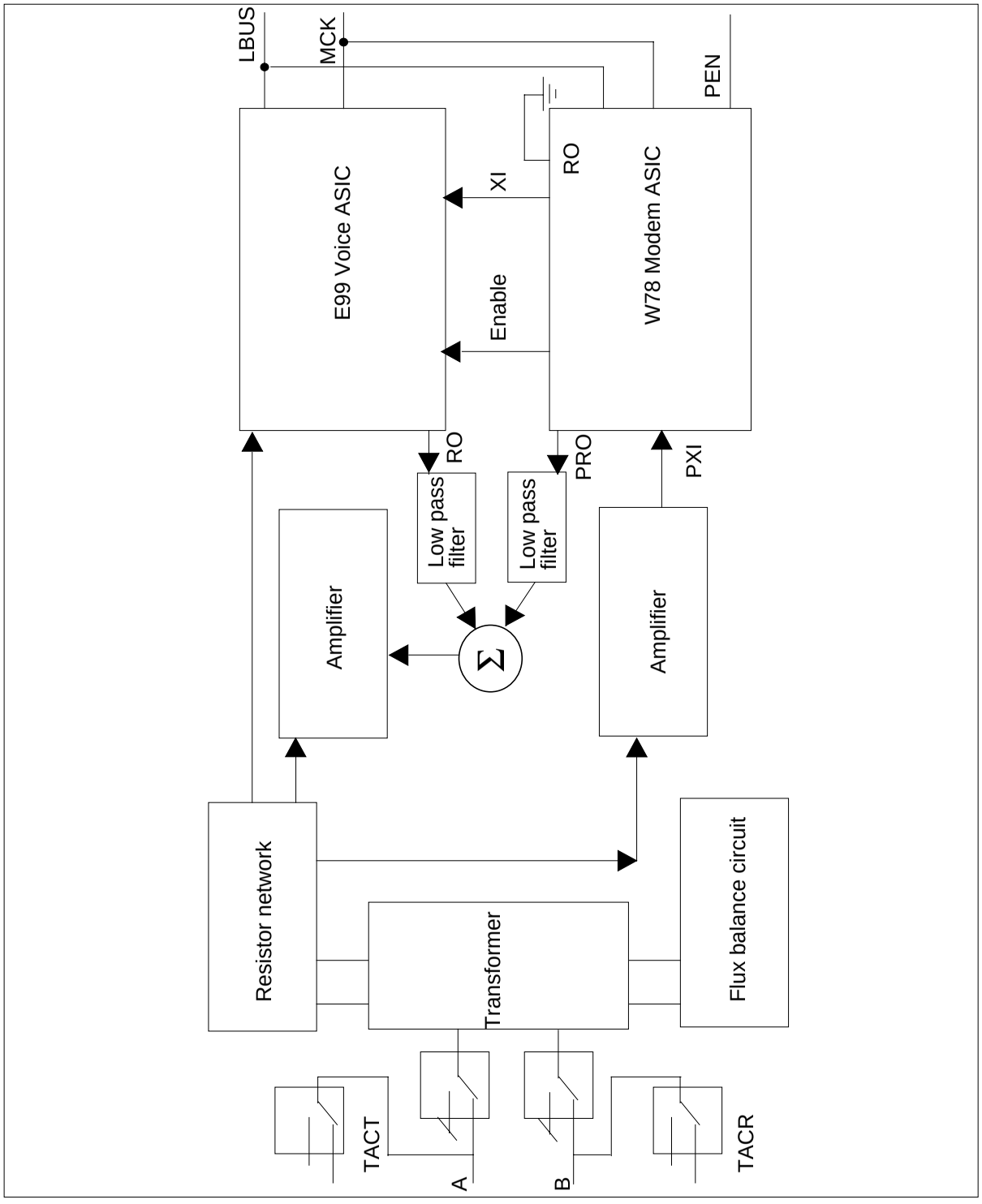
Functional blocks

Functional blocks of the NT6X21BC line card are:

- E99 voice ASIC
- W78 modem ASIC
- resistor network
- flux balance circuit
- high pass filter
- low pass filter
- voice frequency (VF) transformer

The relationship between the functional blocks of the NT6X21BC line card appear in the next figure.

NT6X21BC functional blocks



NT6X21BC (continued)

Supervision

The W78 (signaling chip) or the E99 (voice chip) can supply supervision (SV0) on the local bus (L-BUS). The supply of supervision depends on the state of pin 1A, which is P-enable (PEN) on the line card connector. The state of the PEN for this supply occurs during the start bit of an L-BUS transaction. When the PEN is low during the start bit, the L-BUS transaction communicates with the W78. The SV0 from the W78 indicates message transmission or reception status. The SV0 from the E99 indicates the loop current is above the set presence threshold.

Loop detection, current limit and termination

This section discusses loop detection, current limit and termination.

Loop detection

A voltage measurement bridge performs the loop detection. A voltage measurement bridge compares two voltages. For loop detection, one voltage is at the exact center point between tip and battery (-48V). The second voltage is at the exact center point between ring and battery return (-48V rtn). This difference is amplified, and biased to new dc levels for standard electronic components.

The loop current threshold indicates set presence. The business set draws a minimum of 4.5 mA. The exception to this rule is the ACD set with a headset. When the headset is unplugged, the business set loop current becomes less than 2 mA.

Loop current limit

The business set is a current sink that limits loop current to less than 38 mA.

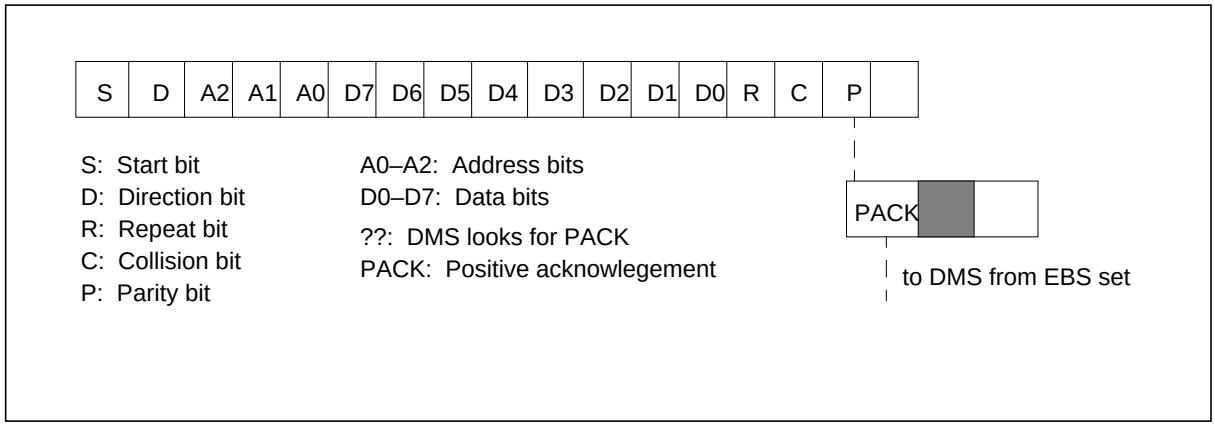
Loop termination

A resistor and capacitor on the center tap of the secondary of the transistor combines the NT6X21BC input impedance. The input impedance required of the NT6X21BC line card is 900 Ω + 2.16 μF.

Signaling

The W78 provides the amplitude shift keying (ASK) signaling between the business set and the DMS switch. The loop (tip-ring) side of the device provides an 8 kHz carrier. A 1 kb/s signal that uses ASK modulates the 8 kHz carrier. The ASK turns on the 8 kHz for 1 bit and turns off the 8 kHz for 0 bit. The PRO is the signaling output of the W78 chip. The PXI is the signaling and voice input to the W78 chip. The ASK is an asynchronous protocol and has a defined addressing structure which appears in the next figure.

Asynchronous protocol



Voice path

The E99 chip receives the receive digital to analog signal on the L-BUS and decodes and filters the signal. The E99 chip transmits the signal out of the RO+ and RO- outputs. Additional gain and filtering occurs before the sum of the voice path occurs with the signaling path.

Hybrid balance

The transmit signal contains components of the receive signal. Removal of components must occur before the transmit signal can be encoded and put on the two way bus. This function is a hybrid balance. The balance filter does this function. There are two DIP switch selectable balance filters on the NT6X21BC line card.

The NT6X21BC hybrid balance impedance is set to 800 Ω + .05 µF.

Power supplies

A 15V rail and a 12.7V precise high impedance reference are supplied to the NT6X21BC line card. The 10V, 12V, 9V and 5V supplies originate from the 15V rail and 12.7V precise high impedance reference.

Cut-over relay

The cut over relay isolates the NT6X21BC line card from the loop. The cutover relay is used for diagnostics and office installation.

Test access

The NT6X21BC test access relay allows bridged access to the A and B leads for testing purposes. Operation of the test relay connects the A and B leads of the subscriber loop on the LCM test access bus. Operation of the cutover relay

NT6X21BC (continued)

at the same time as the test access relay can occur. This action separates the NT6X21BC line card from the subscriber loop and from the test access bus. This action also allows the maintenance equipment to test the loop alone, or the loop with the line card that drives the loop.

Voice frequency transformer

The VF transformer provides an interface between the E99 in the N6X21BC circuit card and the analog facilities. In the receive direction, the transformer converts the signals on the tip and ring leads to one signal. The receive circuit processes this signal.

In the transmit direction, the transformer receives the signal from the transmit circuit. The transformer sends the converted signals over the tip and ring leads. The transformer works with the balancing network to provide four-wire to two-wire conversion

The transformer works with the supervision network to cancel any flux. Line currents that flow in the supervision circuits produce flux. Line currents that flow in the supervision circuits improve the quality of the transformer for speech transmission.

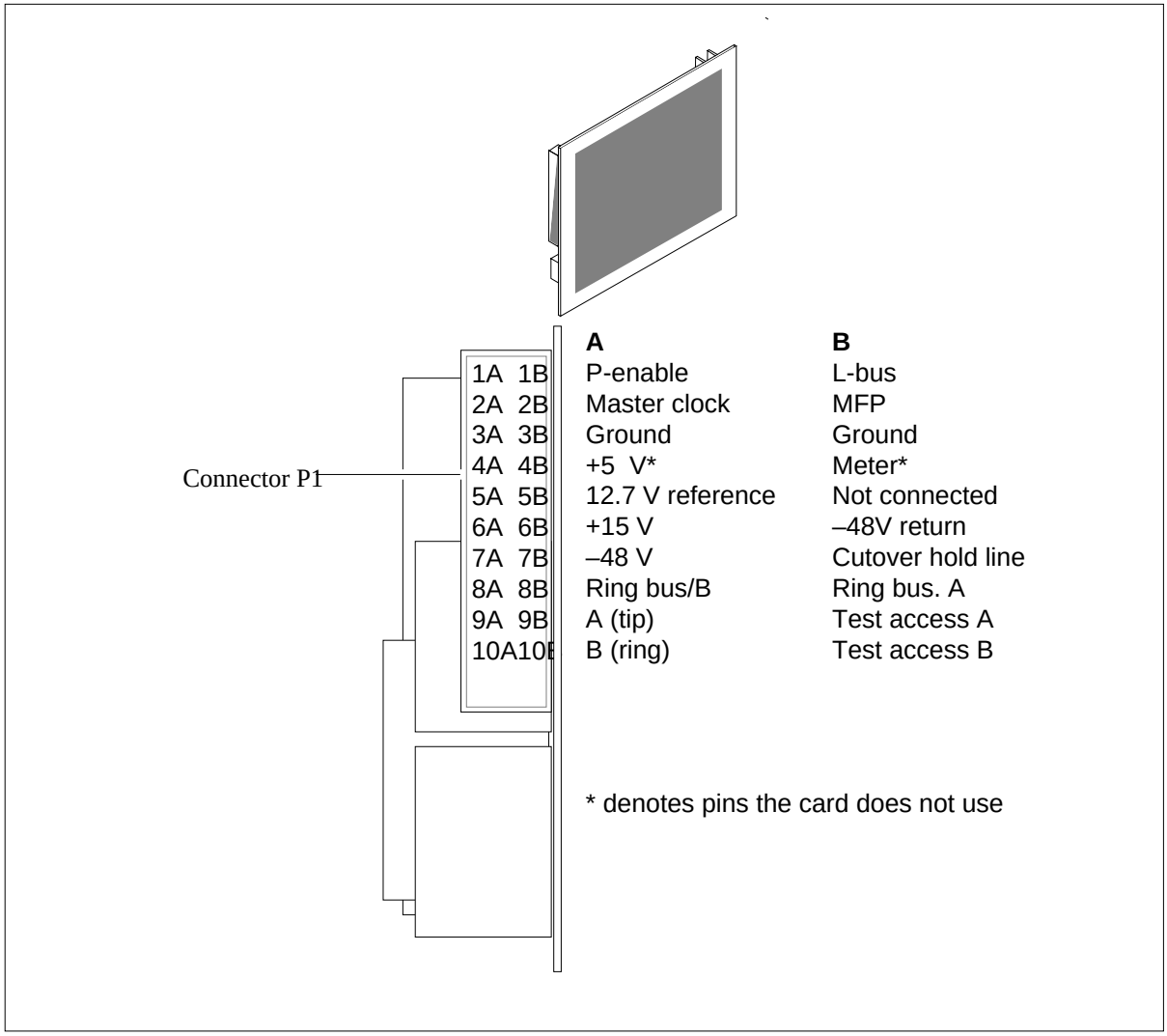
Flux balance circuit

Flux balance is provided by a current source, which is done by controlling the voltage across a 619 Ω resistor. DC loop current can absorb the core of the transformer. The flux balance circuit prevents the loop current from absorbing the transformer magnetically.

Pin numbers

The P1 pin numbers for the NT6X21AD appear in the next figure.

NT6X21BC P1 pin numbers



A description of P1 pin numbers is in the next table.

P1 Pin number description (Sheet 1 of 2)

Pin	Signal	Description
1A	P-enable	Sets 2-directional, 1-wire serial communications link (LBUS) message to application specific integrated circuit (ASIC). PEN is low during start bit.
2A	Master clock	Clock for LBUS.

NT6X21BC (continued)

P1 Pin number description (Sheet 2 of 2)

Pin	Signal	Description
3A	Ground	
4A	+5 V	The card does not use this pin
5A	12.7V reference	ASIC E99 precision reference
6A	+15 V	Line card supply: creates +10V and +12V rails
7A	-48 V	Talk battery low
8A	Ring bus/B	Ring signal low
9A	A (tip)	Subscriber interface high
10A	B (ring)	Subscriber interface low
1B	LBUS	MSG & PCM digital interface
2B	MFP	Multi-function protector
3B	Ground	
4B	Meter	The card does not use this pin
5B	NC	Not connected
6B	-48V return	Talk battery high
7B	Cutover hold line	For cutover of all lines at the same time
8B	Ring bus/A	Ring signal high
9B	Test access A	Test bus high (tip)
10B	Test access B	Test bus low (ring)

Technical data

This section contains technical data referring the NT6X21BC line card.

Transmission specifications

The NT6X21BC line card uses a two way bus to receive and transmit signals. The NT6X21BC line card also uses an enable signal to receive and transmit

signals. The transmission characteristics of the NT6X21BC line card appear in the next table.

Transmission characteristics

Characteristic	Value
Modulation technique	ASK, half-duplex
Carrier frequency	8 kHz ±2%
Bit length	1 ms
Message length	16 ms
Message interval	23 ms

The transmission gain/frequency distortion for an analog to digital path appears in the next table. Measurements are subject to 1000 Hz @ 0 dBm0.

Transmission gain/frequency distortion (analog to digital)

Frequency response (Hz)	Gain (dB)	
	Min	Max
60		<-20.0
300	-1.5	0.4
1700	-0.5	0.4
2800	-1.0	0.3
3000	-1.0	0.3
3400	-2.0	0.0

NT6X21BC (continued)

The transmission gain/frequency distortion for a digital path to an analog path appears in the following table. Measurements are subject to 1000 Hz @ 0 dBm0.

Transmission gain/frequency distortion

Frequency response (Hz)	Gain (dB)	
	Min	**Max**
300	-0.96	0.3
1700	-0.5	0.4
2800	-1.0	0.4
3000	-1.0	0.5
3400	-2.40	0.0

The transmission echo return loss (ERL) is 20 dB. The singing return loss is 14dB, with a programmable digital to analog loss range of 0 through 7 dB in 1-dB increments.

Quantization distortions (digital to analog) appear in the next table.

Quantization distortion (digital to analog)

Input level (dBm0)	Minimum signal to total distortion ratio (db)
0.0 dBm	35 dB
-30.0 dBm	35 dB
-40.0 dBm	29 dB
-45.0 dBm	25 dB

Quantization distortions (analog to digital) appear in the next table

Quantization distortion (analog to digital)

Input level (dBm0)	Minimum signal to total distortion ratio (db)
-5.2 dBm	35 dB
-35.2 dBm	35 dB
-45.2 dBm	26 dB
-40.2 dBm	23 dB

Dimensions

The dimensions of the NT6X21BC are as follows:

- height: 76 mm (2.994 in.)
- depth: 22 mm (0.875 in.)
- width: 89 mm (3.5 in.)

Power requirements

The NT6X21BC line card uses 300mW of power and converts voltages of +15V ±0.5V and +12.7V ± 1%.

NT6X25AA

Product description

The NT6X25AA frame supervisory panel (FSP) contains power control and alarm circuits. These circuits provide an interface between the power distribution center (PDC) and the equipment frames of the DMS-100 Family digital switching system. The following components provide power control to the remote line concentrating equipment (RLCE) frame:

- one NT0X91AE converter drive and protection circuit pack (CP)
- one NT0X91AA converter drive and alarm
- one NT6X36AA alarm circuit
- seven circuit breakers (CB)

One FSP mounts on each single-bay equipment frame. The FSP includes two talk battery filters and eight QFF1 fuses.

The NT6X25AA provides power for the following converters and generators:

- NT2X06AB–Power converter common feature
- NT2X06BB–Power converter (5 V/40 A)
- NT2X09AA–Multi outside plant power converter CP
- NT2X09BA–Multi outside plant power converter electromagnetic interference shield
- NT2X70AA–Power converter ±5V and ±12 V
- NT2X70AB–Power converter ±5V and ±12 V
- NT2X70AD–Power converter ±5V and ±12 V CP
- NT2X70AE–Power converter CP ±5V and ±12 V
- NT2X70AZ–Power converter primary center kit
- NT2X70BA–Power converter
- NT2X70CA–Power converter
- NT6X53AA–Power converter
- NT6X53BA–Power converter
- NT6X53CA–Line concentrating module (enhanced) power converter
- NT6X53EA–Power converter
- NT6X60AB–Ringing generator CP
- NT6X60DA–Ringing generator CP (China)

- NT6X60EA–Ringing generator (Australia)
- NT6X60GA–Ringing generator (United Kingdom)

The FSP monitors office battery and alarm battery supply (ABS) fuses and cooling or inverter units. If a cooling or inverter unit fails, fan fail indications, frame fail indications and aisle alarm outputs indicate problems.

Converter fail lines connect to the light-emitting diode (LED) indicators on the power converters in the associated frame. A frame fail indication on the FSP front panel and an aisle alarm output monitor these lines. The frame fail indication and aisle alarm output monitor the line to detect a converter or fuse failure. The converter fail lines operate a LED indicator on the front panel of the FSP below the associated power feed CB. The fail lines also operate the LED indicator in the shelf power converter.

The front panel includes four service jacks. These service jacks provide access to two telephone pairs and two data pairs. The telephone pairs are TEL-A and TEL-B. The data pairs are DATA-A and DATA-B. The use of service jacks with the FSP on other frames provides interframe and interaisle communication. This communication uses connectors on the FSP.

The FSP includes a mechanical interlock. This feature contains a small cover that slides. The small cover allows access to only two CBs at one time.

Parts

The FSP contains a mechanical interlock, a front panel control and indicators and the following parts:

- NT0X91AA–Alarm and converter drive CP.
- NT0X91AE–Alarm drive and protective circuit network.
- NT6X36AA–Frame supervisory panel alarm card.

Mechanical interlock

Each frame includes a mechanical interlock. The mechanical interlock surrounds all feeds for power converters from the FSP. The FSP provides a block interlock for feeds to shelves 65 and 18 with feeds to shelves 51 and 04.

Front panel control and indicators

You can operate the breakers manually from the front panel. The location of the associated converter fail LED indicator is below the CB that feeds that converter. If a converter fails, a signal on the associated converter fail lead causes the LED to light. The ABS test jacks appear on the front and rear panels of the FSP. Four jacks allow connection to other frames through a connector

NT6X25AA (continued)

on the rear of the FSP. Two jacks are for data and two jacks are for telephone. Fuses F01 to F04 each have a mechanical indicator. The mechanical indicators are visible from the front of the panel after the operation of a guard contact. Dummy fuses occupy the fuse positions that are not in use.

Alarm and converter drive CP

The FSP uses this CP to monitor all CBs and fuse alarms. The converter drive part of the CP controls the -48 V feeds to two power converters. The NT0X91AE converter drive does not drive these power converters. The alarm part of the NT0X91AA CP can receive input. The alarm receives inputs from the converter fail bus and the guard contacts of fuses F02 through F04. When the alarm circuit receives input, the frame fail lamp lights up and aisle alarm 1 connects to aisle alarm 2. Aisle alarm 2 also provides a connection for an end-aisle alarm lamp.

Alarm drive and protective circuit network

The FSP uses this CP to provide power control and protection to the shelves of the RLCE frame. When a CB is closed, application of the -48 V feed to the converter in shelf position 65 cannot occur. The application occurs only if the correct power-up sequence occurs. Application of the correct sequence must occur through the ON/OFF, RESET and CONVERTER DRIVE leads. Some of the printed circuit board (PCB) connecting fingers on the NT0X91AE are shortened. This change protects the CBs associated with drive circuits in the NT0X91AA when you remove and replace the NT0X91AE. The change makes sure that the CBs do not trip because of transients.

Frame supervisory panel alarm card

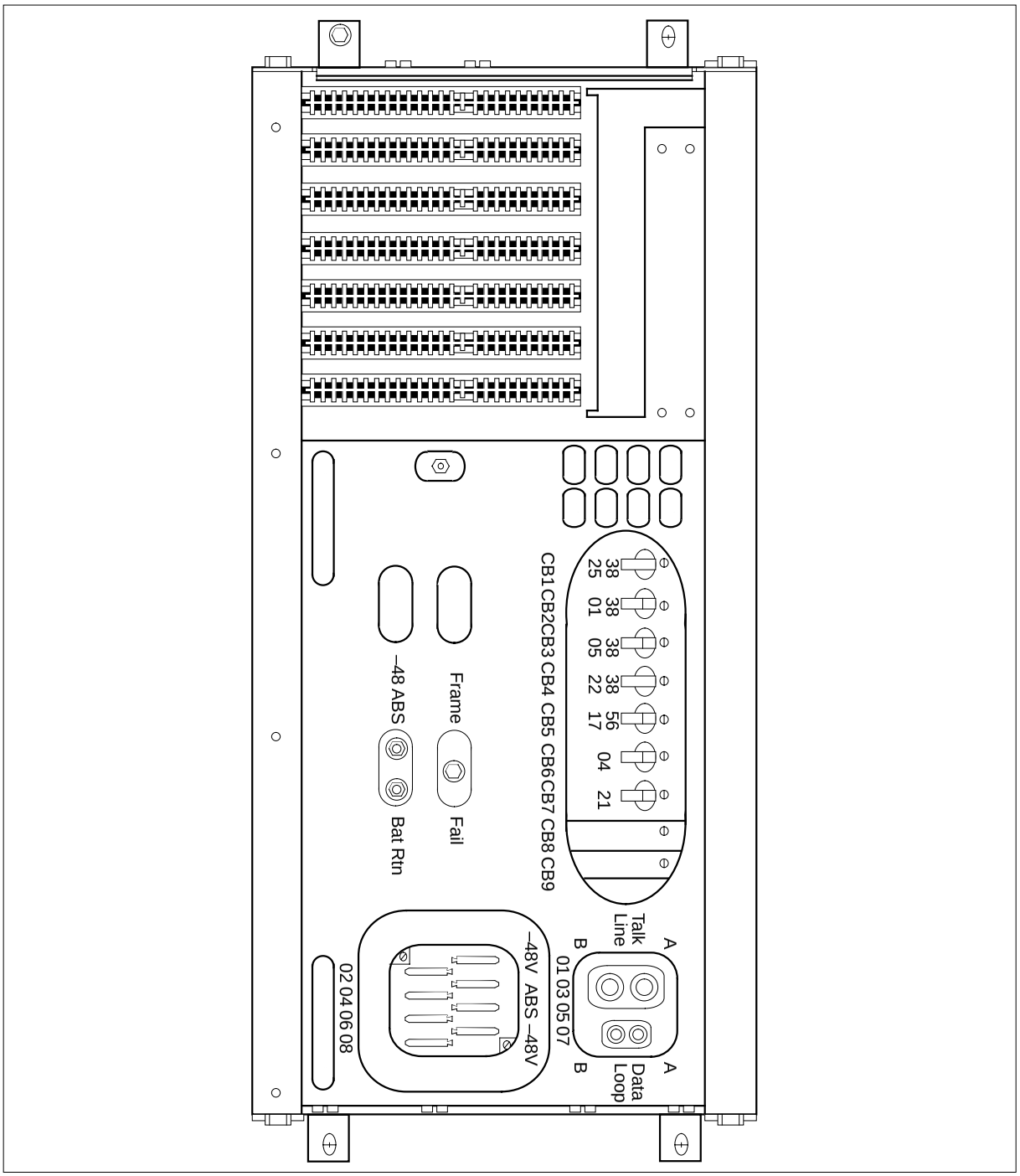
The FSP uses this card to indicate the occurrence of conditions that are dangerous or that threaten the power system. When the aisle alarm loop closes, the frame fail lamp and the end aisle lamp light up. The lamps light up in response to an alarm condition. These alarm conditions include fan fail, fuse fail, tripped CBs CB8 and CB9 and T1 alarms. If the problem occurs in a power converter or ringing generator, the alarm LED lights up in response.

Design

The design of the FSP appears in the following figure.

NT6X25AA (end)

NT6X25AA parts



NT6X25AB

Product description

The NT6X25AB frame supervisory panel (FSP) contains power control and alarm circuits. These circuits provide an interface between the power distribution center (PDC) and the equipment frames of the DMS-100 Family digital switching system. The following provide power control to the remote control and maintenance equipment (RCME) frame:

- one NT0X91AE alarm drive and protective circuit network (NET)
- one NT0X91AA alarm and converter drive circuit pack (CP)
- one NT6X36AA FSP alarm card
- seven circuit breakers (CB)

One FSP mounts on each single-bay equipment frame. The FSP features two talk battery filters and eight QFF1 fuses.

The NT6X25AB provides power for the following converters and generators:

- NT2X06AB–Power converter common feature
- NT2X06BB–Power converter (5 V/40 A)
- NT2X09AA–Multi outside plant power converter CP
- NT2X09BA–Multi outside plant power converter electromagnetic interference shield
- NT2X70AA–Power converter ±5V, ±12 V
- NT2X70AB–Power converter ±5V and ±12 V
- NT2X70AD–Power converter ±5V and ±12 V CP
- NT2X70AE–Power converter CP ±5V and ±12 V
- NT2X70AZ–Power converter primary center kit
- NT2X70BA–Power converter
- NT2X70CA–Power converter
- NT6X53AA–Power converter
- NT6X53BA–Power converter
- NT6X53CA–Line concentrating module (enhanced) power converter
- NT6X53EA–Power converter
- NT6X60AB–Ringing generator CP
- NT6X60DA–Ringing generator CP (China)

- NT6X60EA–Ringing generator (Australia)
- NT6X60GA–Ringing generator (United Kingdom)

The FSP monitors office battery and alarm battery supply (ABS) fuses and cooling or inverter units. If a cooling or inverter unit fails, fan fail indications, frame fail indications and aisle alarm outputs indicate problems.

Converter fail lines connect to the light-emitting diode (LED) indicators on the power converters in the associated frame. A frame fail indication on the FSP front panel and an aisle alarm output monitors these lines. The frame fail indication and aisle alarm output can indicate converter or fuse failure. The converter fail lines operate the LED indicator on the front panel of the FSP below the associated power feed CB. The converter fail lines also operate the LED indicator in the shelf power converter.

The front panel includes four service jacks. These jacks provide access to two telephone pairs and two data pairs. The telephone pairs are TEL-A and TEL-B. The data pairs are DATA-A and DATA-B. The use of service jacks with the FSP on other frames provides interframe and interaisle communication. This communication uses connectors on the FSP.

The FSP includes a mechanical interlock. This feature contains a small cover that slides. This cover allows access to only two CBs at one time.

Parts

The FSP contains a mechanical interlock, a front panel control and indicators and the following parts:

- NT0X91AA–Alarm and converter drive CP
- NT0X91AE–Alarm drive and protective circuit network
- NT6X36AA–Frame supervisory panel alarm card

Mechanical interlock

Each frame includes a mechanical interlock. The mechanical interlock surrounds all feeds for power converters from the FSP. The FSP provides a block interlock for feeds to shelves 65 and 18 with feeds to shelves 51 and 04.

Front panel control and indicators

You can operate the breakers manually from the front panel. The location of the associated converter fail LED indicator is below the CB that feeds that converter. If a converter fails, a signal on the associated converter fail lead causes the LED to light up. The ABS test jacks appear on the front and rear panels of the FSP. Four jacks allow connections to other frames through a

NT6X25AB (continued)

connector on the rear of the FSP. Two jacks are for data and two are for telephone. Fuses F01 to F04 each have a mechanical indicator. The mechanical indicator is visible from the front of the panel after the operation of a guard contact. Dummy fuses occupy the fuses positions that are not in use.

Alarm and converter drive CP

The FSP uses the alarm and converter drive CP to monitor all CBs and fuse alarms. The converter drive part of the CP controls the -48 V feeds to two power converters. The NT0X91AE converter drive does not drive these power converters. The alarm part of the NT0X91AA CP can receive input. The alarm receives input from the converter fail bus and the guard contacts of fuses 2 through 4. When the alarm circuit receives input, the frame fail lamp lights and aisle alarm 1 connects to aisle alarm 2. Aisle alarm 2 also provides a connection for an end-aisle alarm lamp.

Alarm drive and protective CP

The FSP uses the alarm drive and protective CP to provide power control and protection to the shelves of the RCME frame. When a CB is closed, application of the -48 V feed to the converter in shelf position 65 cannot occur. Application of the feed to the shelf requires the application of the correct power-up sequence. The correct application of this sequence must occur through the ON/OFF, RESET, and CONVERTER DRIVE leads. When you remove and replace the NT0X91AE, transients can cause the drive circuits in the NT0X91AA to trip. Some of the printed circuit board (PCB) connecting fingers on the NT0X91AE are shortened. This change makes sure that the CBs associated with drive circuits in the NT0X91AA do not trip.

Frame supervisory panel alarm card

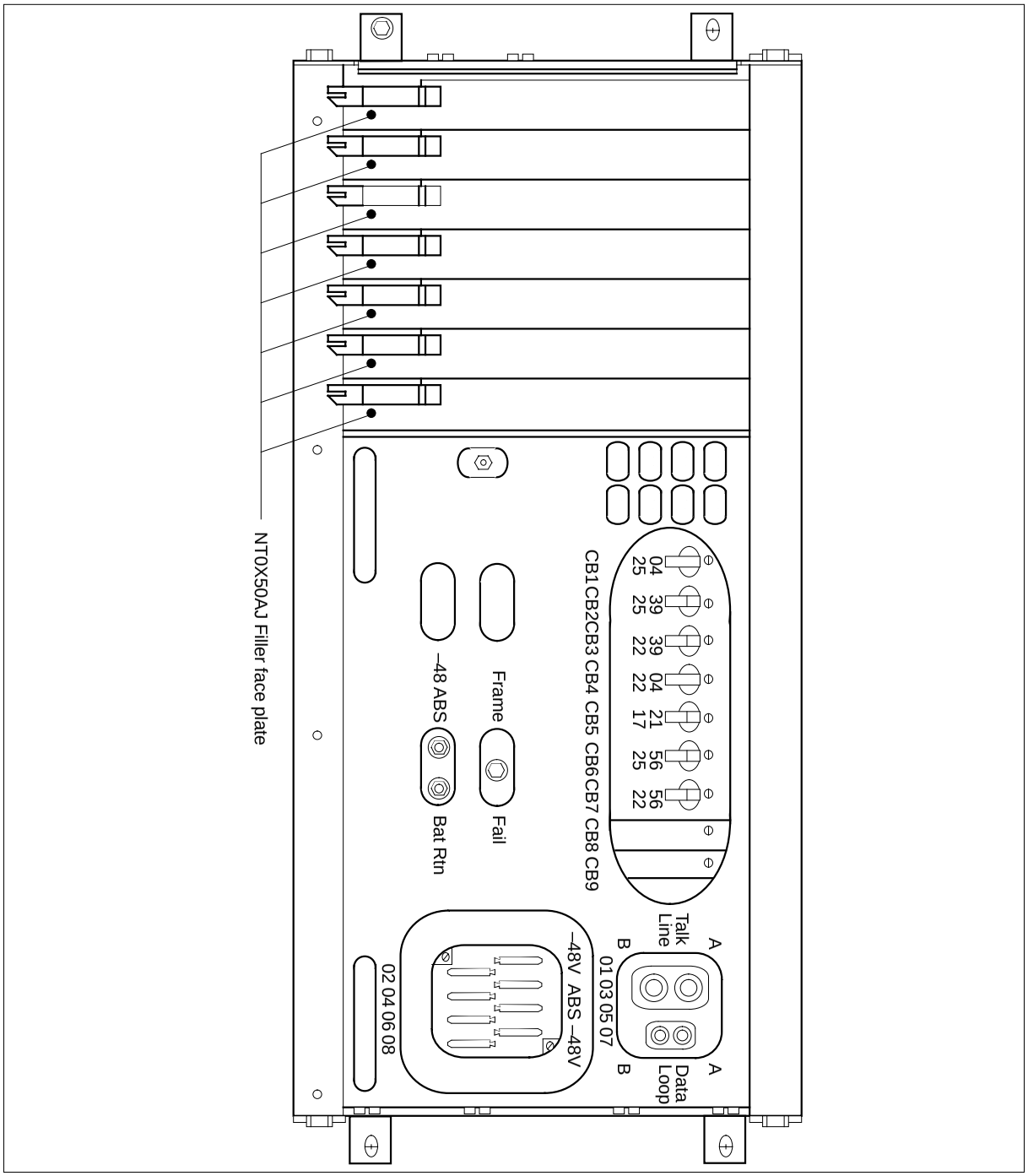
The FSP uses the FSP alarm card to indicate the occurrence of conditions that are dangerous or that threaten the power system. When the aisle alarm loop closes, the frame fail lamp and the end aisle lamp light up. The lamps light up in response to an alarm condition. These alarm conditions include fan fail, fuse fail, tripped CBs CB8 and CB9 and T1 alarms. If the problem occurs in a power converter or ringing generator, the alarm LED lights in response.

Design

The design of the FSP appears in the following figure.

NT6X25AB (end)

NT6X25AB parts



NT6X25BA

Product description

The NT6X25BA frame supervisory panel (FSP) is a component of the remote line concentrating module (RLCM) (NT6X14AA) frame. The FSP is also a component of the outside plant module (OPM) (NT8X01AA and NT8X01BB) frame. The FSP provides power control circuits to power converters (NT2X06, NT2X09, and NT2X70) and ringing generators (RG) (NT6X60AA). The power converters are on separate shelves. The FSP includes frame-fail indicators, a fuse-fail alarm output, front and rear alarm battery supply (ABS) test jacks. The FSP includes four front-panel service jacks. Two service jacks are telephone pairs (TEL-A and TEL-B). Two service jacks are data pairs (DATA-A and DATA-B).

The FSP has two talk battery filters, nine circuit breakers (CB1-CB9) and eight fuses (F01-F08). The FSP contains the following plug-in cards (CD1-CD3):

- an alarm and converter drive circuit card (NT0X91AA)
- a converter drive protection circuit card (NT0X91AE)
- an alarm circuit card (NT6X36AA)

The FSP monitors the condition of the power converters and ringing generators in the shelves of the frame. The FSP also monitors the input voltage from the power distribution center (PDC). The two separate inputs are -48 V (A) and -48 V (B).

Parts

The FSP contains the following parts:

- NT0X91AA–Alarm and converter drive circuit card.
- NT0X91AE–Converter drive protection circuit card.
- NT6X36AA–Alarm circuit card.

Alarm and converter drive circuit card

The alarm and converter drive circuit card controls -48 V dc supplies to the power converters. The converter drive protection circuit card does not control these power supplies. The alarm and converter drive circuit card can receive input. The card receives input from the converter-fail bus and the guard contacts of fuses F02 through F04. When a fail indication occurs the alarm and converter drive circuit card controls light the frame-fail indicator. The alarm and converter drive circuit card completes the connection between aisle alarm 1 and aisle alarm 2. Aisle alarm 2 also provides a connection to the end aisle alarm lamp.

Converter drive and alarm circuit card

The converter drive and protection circuit pack (CP) provides power control and protection for the shelves in the RLCM or OPM frames. The circuits only apply -48 V dc to the power converters when the correct power-up sequence is complete. The card includes shortened fingers. This change makes sure that power surges and transients do not trip the circuit breakers associated with the drive circuits. You can remove the card for maintenance. This action does not disrupt the supply of power to the shelves in the associated frame.

Alarm circuit card

The alarm circuit card monitors operational conditions and produces indications of failures and dangerous operational conditions. A cooling fan failure, a tripped circuit breaker or a T1 alarm can cause the alarm-loop to close. These events cause the alarm circuit card to light the frame-fail lamp. The alarm light-emitting diode (LED) lights if a problem occurs in a power converter or RG in the frame.

Front panel controls and indicators

The front panel includes nine circuit breakers and associated LEDs, eight fuses, test jacks and the frame-fail LED. You can operate the circuit breakers manually. A problem in the associated power converter can trip the circuit breakers. The location of the associated converter-fail LED is below each circuit breaker. The fuses have a mechanical indicator that is visible when a guard contact closes.

The circuit breakers and fuses and associated voltages and supplies appear in the following table. Dummy fuses occupy the fuse positions not in use.

Circuit breaker and fuse functions (Sheet 1 of 2)

Designation	Function	Size
CB1	-48 V (A) from PDC	10 A
CB2	-48 V (A) from PDC	10 A
CB3	-48 V (B) from PDC	10 A
CB4	-48 V (B) from PDC	10 A
CB5	-48 V (A) from PDC	10 A
CB6	-48 V (A) from PDC	10 A
CB7	-48 V (B) from PDC	10 A
CB8	-48 V (A) from PDC, -48 V talk	10 A

NT6X25BA (continued)

Circuit breaker and fuse functions (Sheet 2 of 2)

Designation	Function	Size
CB9	-48 V (B) from PDC, -48 V talk	10 A
F01	-48 V talk	1.3 A
F02	ABS	1.3 A
F03	ABS	1.3 A
F04	ABS	1.3 A
F05	ABS	1.3 A
F06	1.3 A	ABS
F07	Not used	--
F08	Not used	--

The front panel includes the following test jacks: TALK-A, TALK-B, DATA-A, DATA-B, -48 ABS, and BAT RET. Two talk line jacks and the two data line jacks at the rear of the panel can connect to other frames.

Mechanical interlock

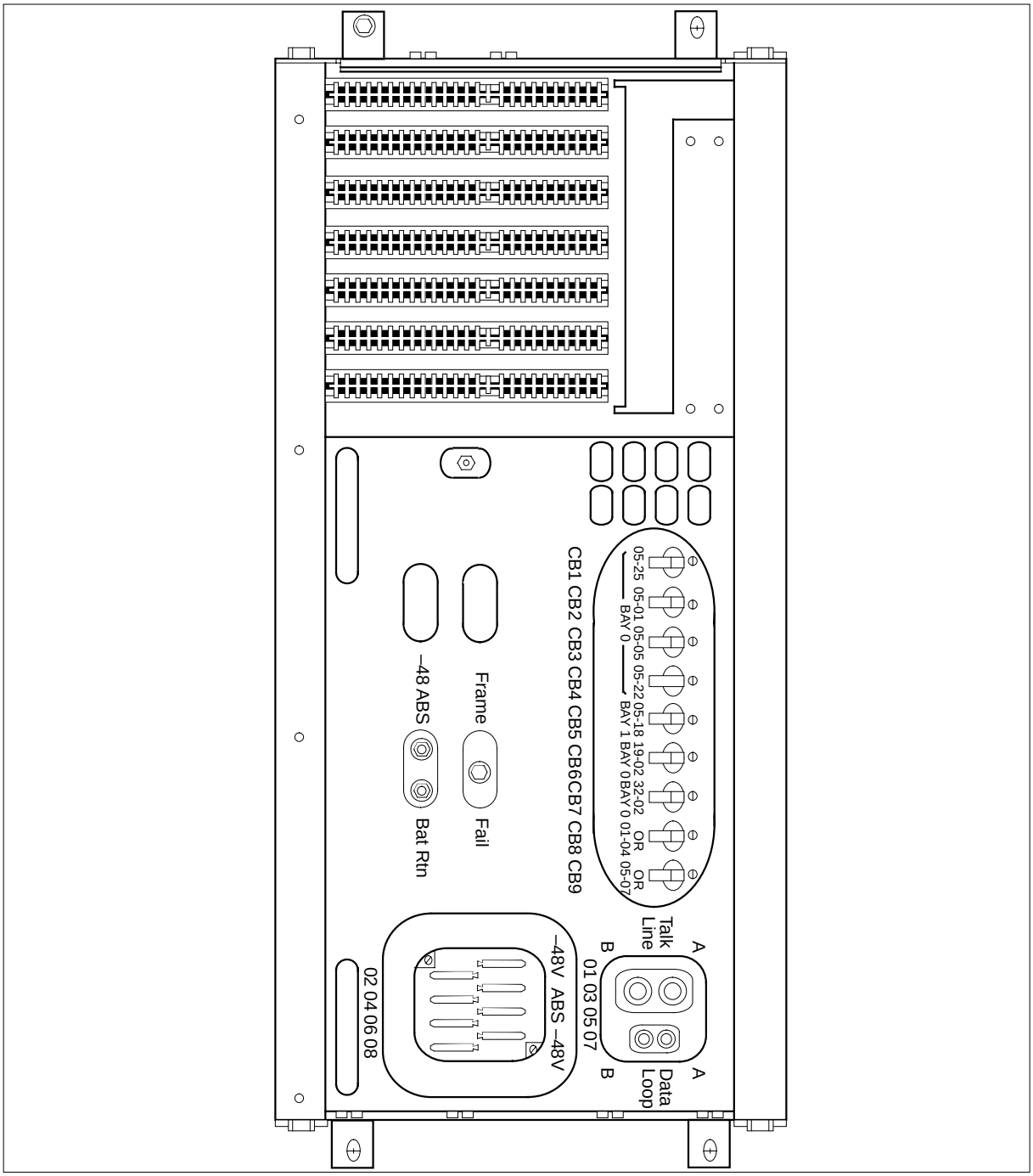
The NT6X25BA FSP includes a mechanical interlock. The mechanical interlock is a small cover that slides. The mechanical interlock allows access to only two circuit breakers at one time. For example, the mechanical interlock can allow access to CB1 and CB2, or CB4 and CB5. The FSP includes the interlock to prevent an accidental trip of the circuit breakers.

Design

The design of the FSP appears in the following figure.

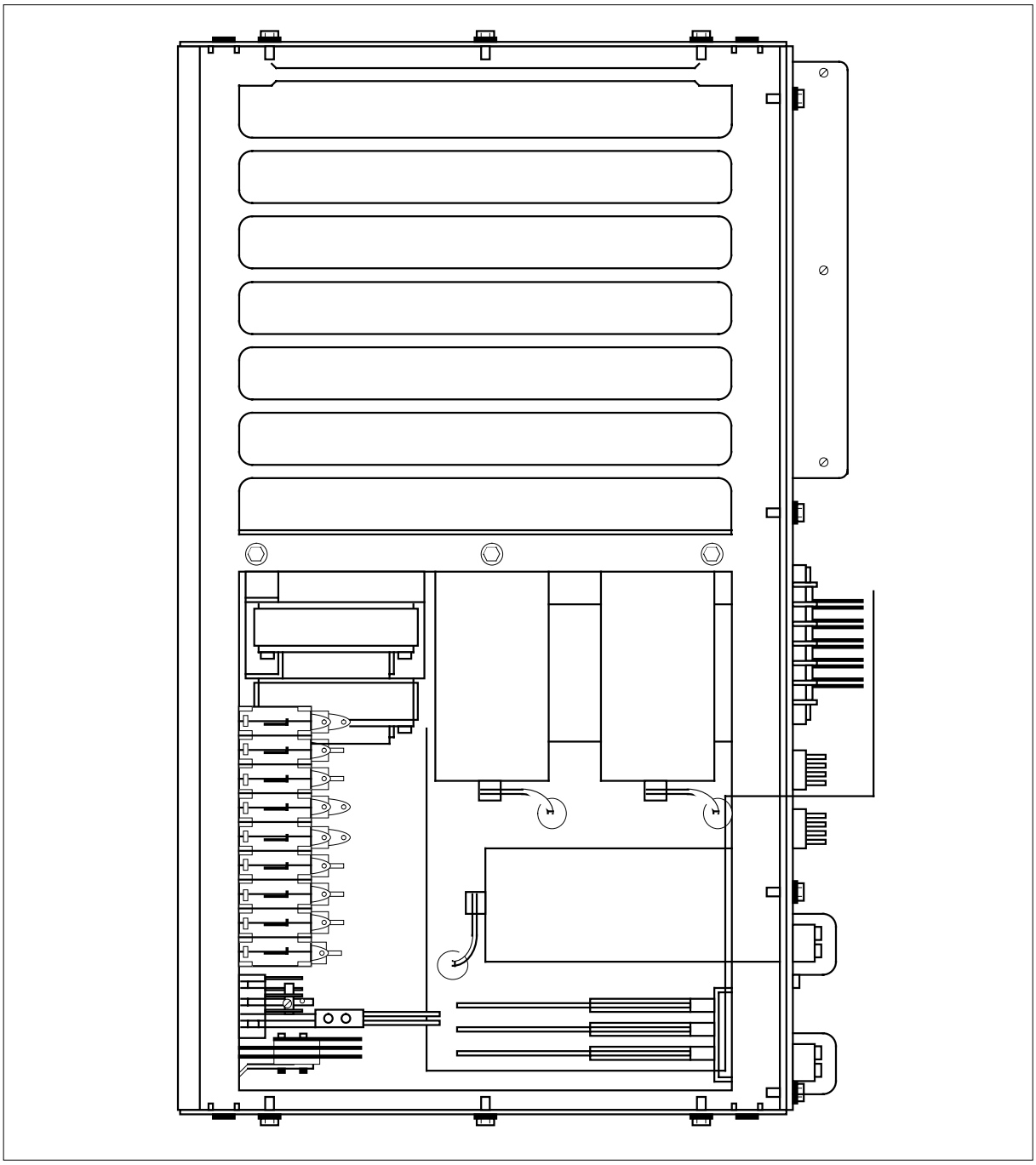
NT6X25BA (continued)

NT6X25BA front view



NT6X25BA (end)

NT6X25BA top view



NT6X25BB

Product description

The NT6X25BB frame supervisory panel (FSP) is a component of the remote line concentrating module (RLCM) NT6X14AA and outside plant module (OPM) NT8X01AA and NT8X01BB frames. The NT6X25BB provides the power control circuits needed by the power converters NT2X06, NT2X09, and NT2X70 and ringing generators (RG) NT6X60AA. These power converters and ringing generators are in separate shelves.

The FSP includes the following:

- frame-fail indicators
- a fuse-fail alarm output
- front and rear alarm battery supply (ABS) test jacks
- four front-panel service jacks that consist of two telephone pairs (TEL-A and TEL-B) and two data pairs (DATA-A and DATA-B)

The panel includes the following:

- two talk battery filters
- nine circuit breakers (CB1-CB9)
- eight fuses (F01-F08)
- three plug-in cards (CD1-CD3)
- an alarm and converter drive circuit card (NT0X91AA)
- a converter drive protection circuit card (NT0X91AE)
- an alarm circuit card (NT6X36AA)

The panel monitors the condition of the power converters and RGs in the shelves belonging to the frame. The panel monitors the input voltage from the power distribution center (PDC). The two separate inputs in an RLCM frame are -48 V (A) and -48 V (B). An OPM frame uses a single -48 V input for both the A and B supplies.

Parts

The NT6X25BB consists of the following parts:

- NT0X91AA–Alarm and converter drive circuit card
- NT0X91AE–Converter drive protection circuit card
- NT6X36AA–Alarm circuit card

NT6X25BB (continued)

Alarm and converter drive circuit card

The alarm and converter drive circuit card (NT0X91AA) controls the -48 V dc supplies to the power converters. The converter drive protection circuit card (NT0X91AE) does not control these power converters. The NT0X91AA receives inputs from the converter-fail bus and the guard contacts of fuses F02-F04.

When a fail indication occurs, the NT0X91AA

- lights the frame-fail indicator
- completes the connection between aisle alarm one and aisle alarm two

Aisle alarm two provides a connection to the end aisle alarm lamp.

Converter drive and alarm circuit card

The converter drive and protection circuit pack (CP) provides power control and protection for the shelves in the RLCM or OPM frames. The circuits apply -48 V dc to the power converters when the correct power-up sequence has occurred. The circuits apply -48dc to the power converters when the card includes shortened fingers. The card includes shortened fingers to make sure that power surges and transients trip the circuit breakers. The circuit breakers associate with the drive circuits. You can remove the card for maintenance without disrupting the power applied to the shelves in the associated frame.

Alarm circuit card

The alarm circuit card monitors different conditions and produces indications of failures and dangerous operating conditions. If the alarm-loop closes because of the following conditions, the alarm circuit card lights the frame-fail lamp. These conditions include a cooling fan failure, a tripped circuit breaker, or a T1 alarm. If a problem occurs in a power converter or ringing generator in the frame, the following action occurs. The card lights the alarm light-emitting diode (LED).

Front panel controls and indicators

The front panel includes nine circuit breakers and associated LEDs, eight fuses, test jacks, and the frame-fail LED. The circuit breakers can operate manually or tripped by a problem in the associated power converter. The associated converter-fail LED is below each circuit breaker. The fuses have a mechanical indicator visible when a guard contact closes.

The circuit breakers and fuses and the voltages and supplies associated with the front panel controls and indicators are given in the following table. Fuse positions that are not used have dummy fuses.

Circuit breaker and fuse functions

Designation	Function	Size
CB1	-48 V (A) from PDC	10 A
CB2	-48 V (A) from PDC	10 A
CB3	-48 V (B) from PDC	10 A
CB4	-48 V (B) from PDC	10 A
CB5	-48 V (A) from PDC	10 A
CB6	-48 V (A) from PDC	10 A
CB7	-48 V (B) from PDC	10 A
CB8	-48 V (A) from PDC, -48 V talk	10 A
CB9	-48 V (B) from PDC, -48 V talk	10 A
F01	-48 V talk	1.3 A
F02	ABS	1.3 A
F03	ABS	1.3 A
F04	ABS	1.3 A
F05	ABS	1.3 A
F06	1.3 A	ABS
F07	Not used	--
F08	Not used	--

The front panel also includes a number of test jacks: TALK-A, TALK-B, DATA-A, DATA-B, -48 ABS, and BAT RET. Two talk line jacks and the two data line jacks at the rear of the panel can connect to other frames.

Mechanical interlock

The NT6X25BB FSP also includes a mechanical interlock. A mechanical interlock is a small sliding cover. A mechanical interlock allows access to only two of the circuit breakers at a time. An example of the access is: CB1 and

NT6X25BB (continued)

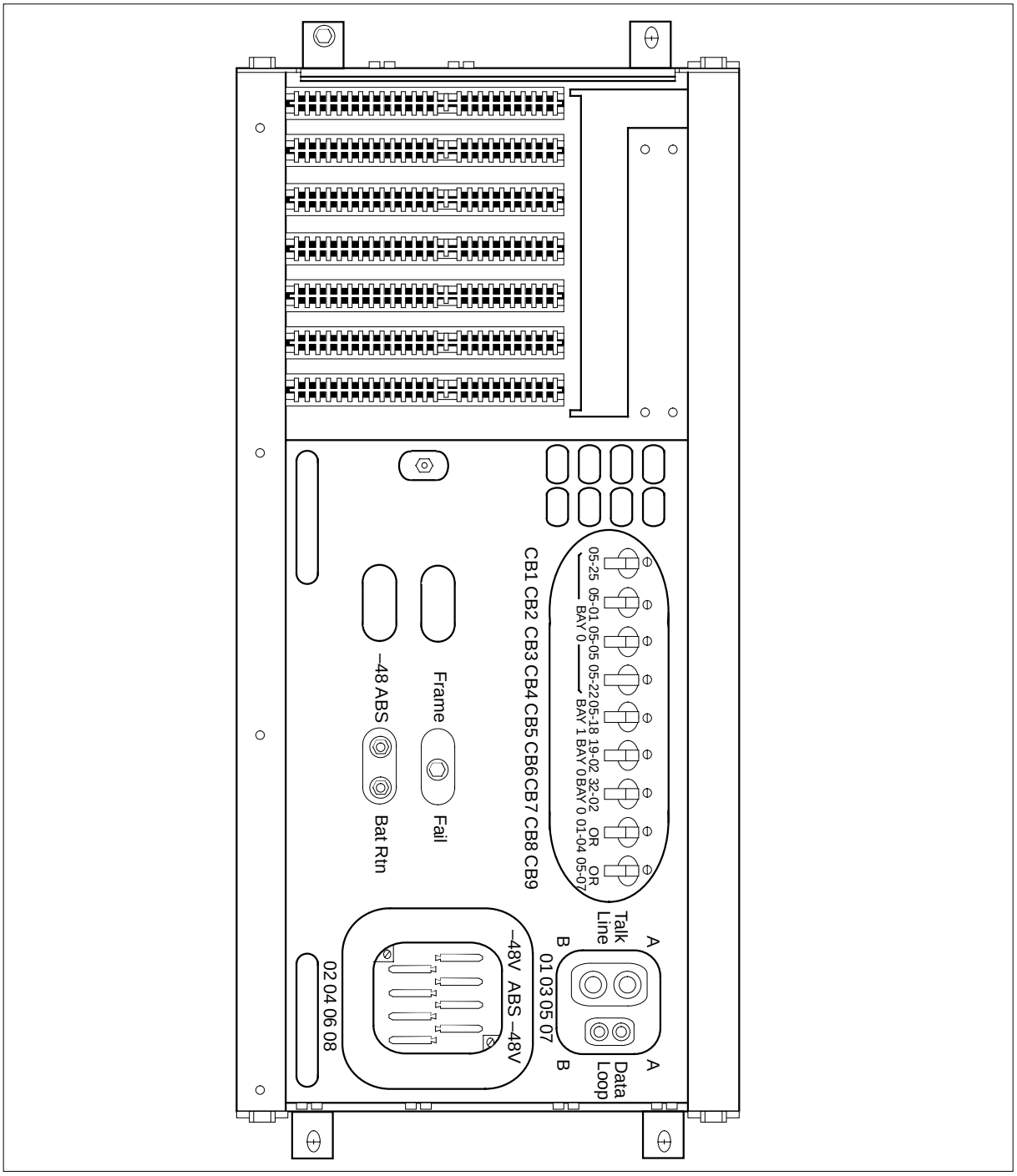
CB2, CB4 and CB5. This interlock is present so that circuit breakers cannot trip by accident.

Design

The design of the FSP appears in the following figures.

NT6X25BB (continued)

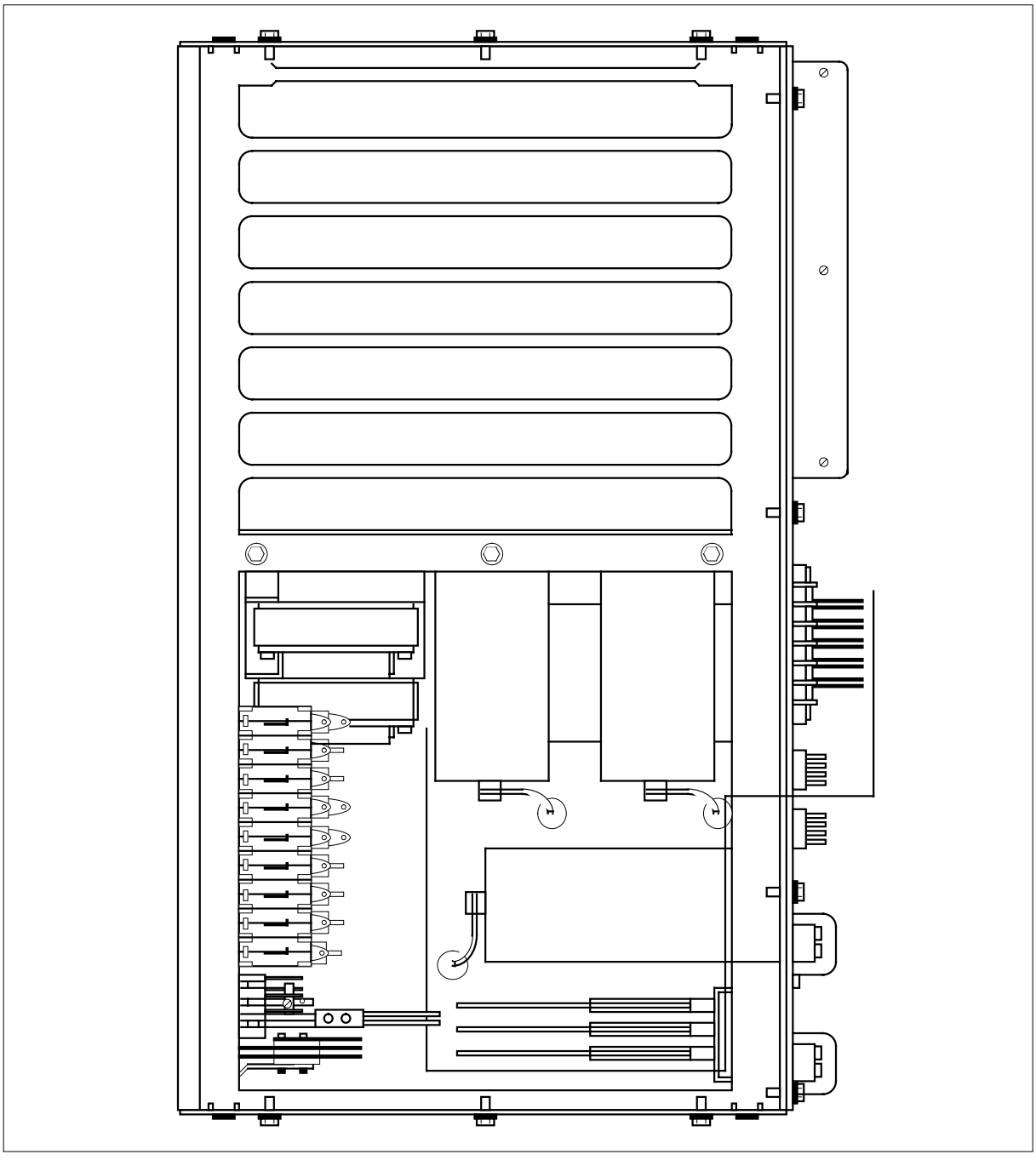
NT6X25BB front view



Note: This diagram is not drawn to scale.

NT6X25BB (end)

NT6X25BB top view



Note: This diagram is not drawn to scale.

NT6X25BC

Product description

The NT6X25BC frame supervisory panel (FSP) provides the power control circuits needed by the power converters (NT2X06, NT2X09, and NT2X700) and ringing generators (RG) (NT6X60AA) located in separate shelves. The FSP is a component of the NT6X14AA remote line concentrating module (RLCM) and the NT8X01AA and NT8X01BB outside plant module (OPM) frames. The FSP includes the following:

- frame-fail indicators,
- a fuse-fail alarm output
- front and rear alarm battery supply (ABS) test jacks
- four front-panel services jacks. The service jacks are two telephone pairs (TEL-A and TEL-B) and two data pairs (DATA-A and DATA-B).

The panel has two talk battery filters, nine circuit breakers (CB1-CB9), eight fuses (F01-F08), and three plug-in cards (CD1-CD3). The three plug-in cards consist of an alarm and converter drive circuit card (NT0X91AE), and an alarm circuit card (NT6X36AA). The FSP monitors the condition of the power converters and RGs in the frame shelves. The FSP monitors the input voltage from the power distribution center (PDC). There are two separate inputs in an RLCM frame: -48 V (A) and -48 V (B). In an OPM frame, a single -48 V input is for the A and B supplies.

Parts

The NT6X25BC consists of the following parts:

- NT0X91AA–alarm and converter drive circuit card
- NT0X91AE–converter drive protection circuit card
- NT6X36AA–alarm circuit card
- Front panel controls and indicators
- Mechanical interlock

Alarm and converter drive circuit card

The alarm and converter drive circuit card controls the -48V dc supplies to the power converters. The card controls the supplies to the power converters not controlled by the converter drive protection circuit card. The circuit card receives inputs from the converter-fail bus and the guard contacts of fuses F02-F04. When a fail indication occurs, the alarm and converter drive circuit card lights the frame-fail indicator. The circuit card completes the connection between aisle alarm one and aisle alarm two. Aisle alarm two provides a connection to the end aisle alarm lamp.

NT6X25BC (continued)

Converter drive and alarm circuit card

The converter drive and protection circuit pack (CP) provides power control and protection for the shelves in the RLCM or OPM frames. The circuits apply -48V dc to the power converters when the correct power-up sequence occurs. The card must include shortened fingers to make sure that power surges and transients trip the circuit breakers associated with the drive circuits. You can remove the card for maintenance without disrupting the power applied to the shelves in the associated frame.

Alarm circuit card

The alarm circuit card monitors different conditions and produces indications of failures and dangerous operating conditions. If the alarm loop closes because of a cooling fan failure, a tripped circuit breaker, or a T1 alarm, the alarm circuit card lights the frame-fail lamp. If a problem occurs in a power converter or ringing generator in the frame, the card lights the frame light-emitting diode (LED).

Front panel controls and indicators

The front panel includes nine circuit breakers and associated LEDS, eight fuses, test jacks, and the frame-fail LED. The circuit breakers can operate manually or tripped by a problem in the associated power converter. The associated converter-fail LED is below each circuit breaker. The fuses have a mechanical indicator that is visible when a guard contact closes.

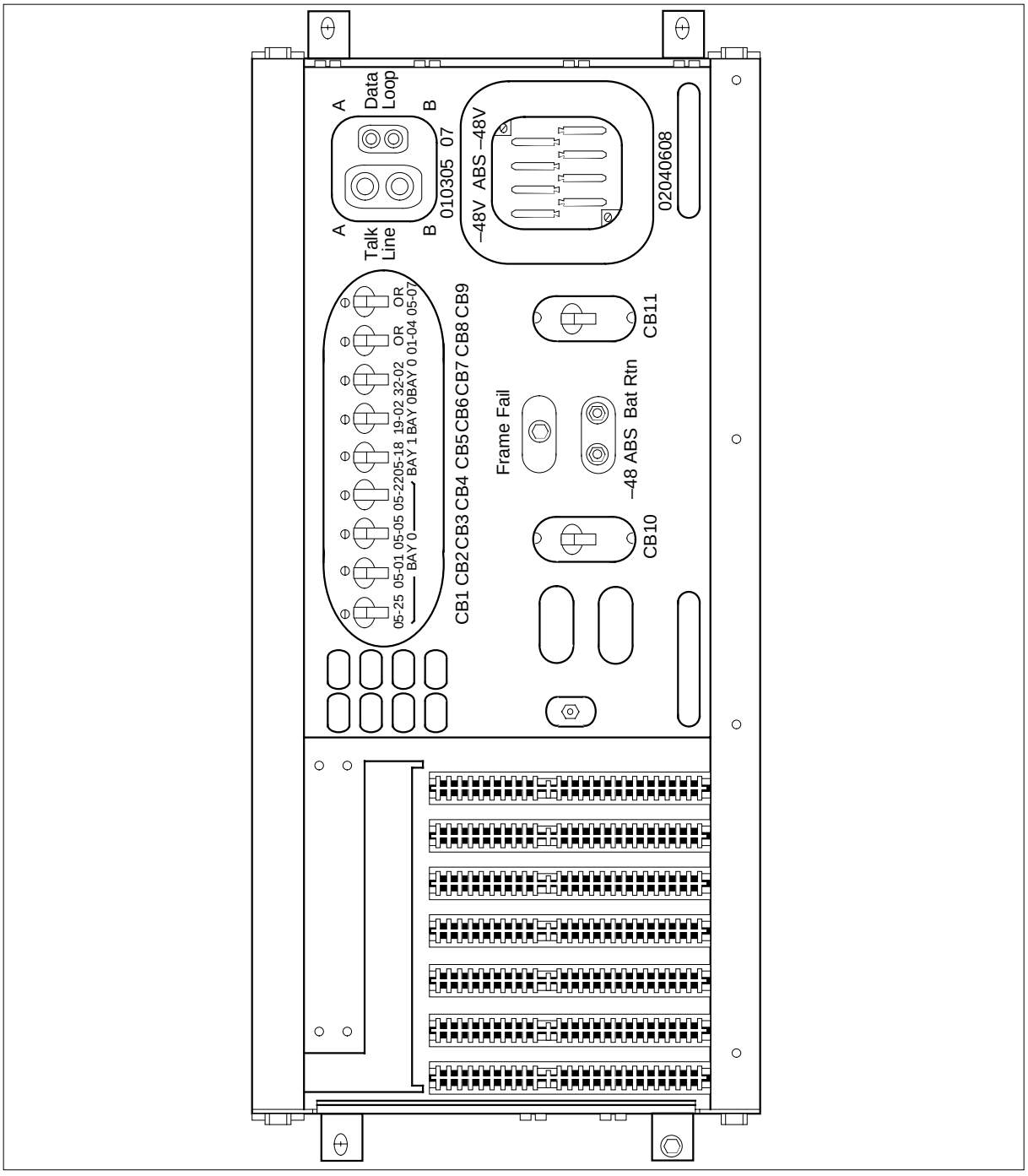
Mechanical interlock

The FSP also includes a mechanical interlock. A mechanical interlock is a small sliding cover. The mechanical interlock allows access to only two of the circuit breakers at a time. An example of the access is CB1 and CB2, and CB4 and CB5. This interlock is present so that circuit breakers cannot trip by accident.

Design

The design of the FSP appears in the following figure.

NT6X25BC front view



Note: This diagram is not drawn to scale.

NT6X27AA

Product description

The NT6X27AA pulse code modulation (PCM) 30 interface circuit card provides an interface between an NT6X02 common peripheral controller (CPC) and European-standard PCM30 trunk transmission equipment.

The card translates PCM voice signals and signaling data. The card translates the data between two 32-channel, 2.048 Mbps external PCM30 trunk circuits and one 64-channel, 5.12 Mbps duplicated port in the CPC. The card meets the transmission and signaling standards of the CCITT.

Location

The card occupies one position in an international CPC (ICPC) shelf. The ICPC contains two shelves. One shelf is active the other shelf is standby. Each shelf can hold a maximum of eight cards.

Functional description

The NT6X27AA receives data streams from the four-wire PCM trunk transmission equipment. The converts the high-density bipolar 3 (HDB3) data to a DS-30 format for transmission to the DS-60 ports time switch interface. The card receives PCM30 data from the DS-60 time switch interface. The card converts the data to an HDB3 format for transmission to the trunk transmission equipment. The NT6X27AA provides a looparound function for test purposes.

Functional blocks

The NT6X27AA consists of the following functional blocks:

- receive interface
- looparound multiplexer (MUX)
- clock extractor
- decoder
- frame slip buffer
- channel 16 buffer
- channel control and status register
- input MUX
- control circuit and read counter
- channel input control data register
- activity select/port split
- signaling MUX

- two alignment delay circuits
- insert channel PCM30 signaling circuit
- clock converter
- encoder
- transmit interface
- serial-to-parallel converter
- frame alignment symbol/multiframe alignment symbol (FAS/MFAS) search circuit
- write counter
- port loop

Receive interface

The receive interface accepts data from the four-wire PCM30 trunk transmission equipment. The receive interface sends the data through the looparound MUX to the decoder.

If a digroup loop is in operation the loop connects to the decoder. The looparound MUX does not allow data from the receive interface to enter the decoder.

Looparound MUX

The looparound MUX receives PCM30 data from the receive interface and transmits the data to the decoder. If a digroup loop is in operation, the MUX connects the loop to the decoder. The MUX does not allow entry of data from the receive interface to enter the decoder.

Clock extractor

The clock extractor uses the incoming PCM30 bitstream to generate a 2.048 MHz clock signal to synchronize the card.

Decoder

The decoder converts the PCM30 data from a CCITT HDB3 format to a DS-30 format. The decoder transmits the data to the frame slip buffer.

Frame slip buffer

The frame slip buffer removes or adds 32 channel frames. The difference between the two clock signals determines if the frame slip buffer adds or removes frames. This process controls synchronization between the PCM input and PCM output. The frame slip buffer receives data at a rate of 2.048 Mbps. The buffer transmits data at a rate of 2.56 Mbps.

NT6X27AA (continued)

Channel 16 buffer

The channel 16 buffer sends channel 16 data from the decoder output to the input MUX at the correct time.

Channel control and status register

The channel control and status register contains status information for the NT6X27AA and transmits the data to the input MUX.

Input MUX

The input MUX combines data received from the following into one outgoing DS60 data stream:

- frame slip buffer
- channel 16 buffer
- two alignment delay circuits
- channel control and status register

Control circuit and read counter

The control circuit and read counter synchronizes the internal timing of the card with the external equipment timing. The counter uses the 10.24 MHz DMS-100 system clock, the 2.048 MHz PCM30 clock, and the MFAS 500 Hz timer.

Channel input control data register

The channel input control data register receives control data on the DS-60 channel 0. The channel input control data register provides access to data for the following:

- control looparound
- alarm signals
- national and international signaling use selection

Activity select/port split

The activity select/port split uses the state of the ACTIVITY signal to select the correct DS-60 port. The activity select/port split divides the incoming data into two 2.56 Mbps bit streams. The activity select/port split captures and deciphers the control byte found in time slot 0. The circuit loops the inactive port to the input MUX and loops four ports back to the ICPC.

Signaling MUX

The signaling MUX receives data from the activity select/port split. The signaling MUX uses the insert channel PCM30 signaling circuit to add the

PCM30 signaling data on channel 0. An alignment delay circuit can loop the data from the signaling MUX to the input MUX.

Alignment delay circuits

The two alignment delay circuits perform delay functions. The delay functions align the transmitted data stream and the data stream looped to the input MUX.

Insert channel PCM30 signaling circuit

The insert channel PCM30 signaling circuit sends the PCM signaling data to the signaling MUX for insertion on channel 0.

Clock converter

The clock converter changes the signaling data bit rate from 2.56 Mbps to the PCM30 bit rate of 2.048 Mbps.

Encoder

The encoder circuit converts bit stream data that the clock converter sends. The encoder circuit converts the data to an HDB3 CCITT format and transmits the data to the PCM30 transmit interface.

Transmit interface

The PCM30 transmit interface sends the PCM data to the four-wire PCM30 trunk transmission equipment.

Serial-to-parallel converter

The serial-to-parallel converter accepts channel 0 and channel 16 serial data from the decoder. The serial-to-parallel converter converts the data to a parallel format. The serial-to-parallel converter transmits the data to the FAS/MFAS search circuit.

FAS/MFAS search circuit

The FAS/MFAS search circuit checks channel 0 and channel 16 data. The FAS/MFAS search circuit checks for the number of frame alignment and multiframe alignment symbols.

If the circuit does not detect multiframe alignment symbols, common channel signaling (CCS) is in use.

Write counter

The write counter records the number of channel 0 and channel 16 frame alignment and multiframe alignment symbols. The write counter records the number of channel 0 and channel 16 frame alignment from the FAS/MFAS search circuit. The write counter records multiframe alignment symbols from the FAS/MFAS search circuit.

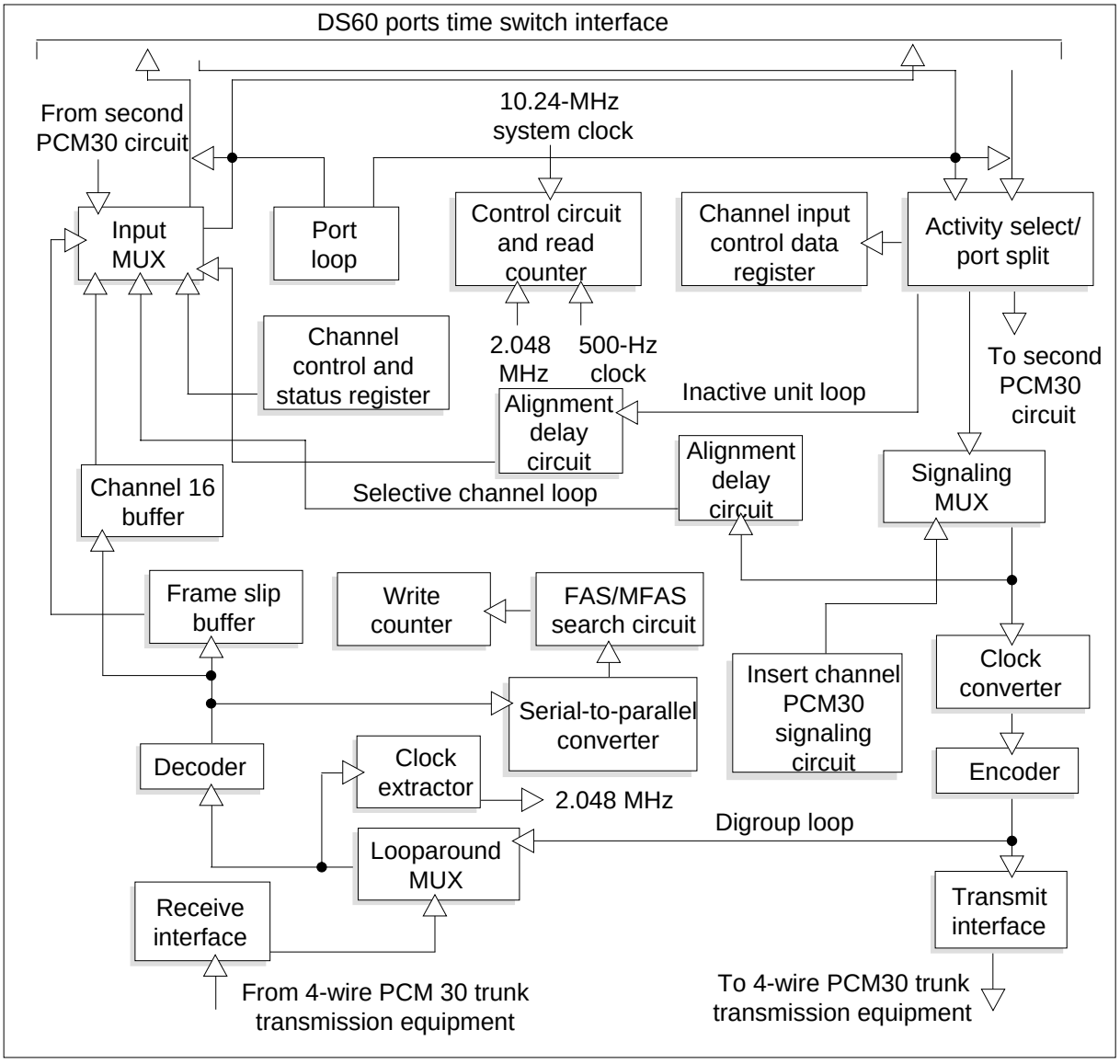
NT6X27AA (continued)

Port loop

The port loop provides test functions. The port loop loops the DS60 incoming data stream to the outgoing data stream. The port loop loops the outgoing data stream to the incoming data stream.

The following figure describes the relationship between the functional blocks.

NT6X27AA functional blocks



Technical data

The uses 64 10 bit time slots at 5.12 Mbps. The NT6X27AA uses a 10.24 MHz clock with the time switch. The PCM30 interface specifications appear in the following table.

PCM30 interface specifications

Characteristic	Value
Electrical interface	Specifications CCITT G703, G712 75- Ω coaxial pair or 120- Ω symmetrical pairs
PCM data stream format	High-density bipolar 3
Frame time	125 μs (8 kHz)
Frame format	Specification CCITT G732 32 8-bit channel time slots at 2.048 Mbps
Channel assignment	Specification CCITT G732 Channel 0 - signaling and framing Channels 1-15 - PCM telephony Channel 16 - signaling Channels 17-31 - PCM telephony

Channel 0 uses FAS framing with a repetition rate of μs (4 kHz). The channel signaling uses 1 bit for international signaling if FAS is present. The channel signaling uses 8 bits for national, international, and remote alarm indication if FAS is not present.

Channel 16 uses CCS with a 64 Kbps clear channel. The channel signaling of channel 16 has the following features:

- 16 multiframe sequences
- two 4 bit signaling words for each multiframe sequence
- 4-bit MFAS
- a repetition rate of 2 ms (500 Hz)

NT6X27AA (end)

Physical dimensions

The physical dimensions of the NT6X27AA are as follows:

- height: 353 mm (13.9 in).
- depth: 277 mm (10.9 in).
- width: 20 mm (0.78 in).

Power requirements

The NT6X27AA requires input voltages from the NT2X70AC power converter in the ICPC of +5V, +12V, and -12V.

NT6X27AC

Product description

The NT6X27AC is based on the NT6X27AB. The NT6X27AC grounding is different than the NT6X27AB grounding. On the AA and AB versions, the outer ring of the coaxial cable grounds to the logic ground. On the AC card the outer ring grounds to the frame ground.

The inactive side on the AA card does not require a peripheral side (P-side) looparound. Versions AB and AC do not have the P-side looparound.

The NT6X27AC provides an interface between new DMS-100 peripherals and standard PCM30 plant equipment. The card accepts common channel or channel-associated signaling techniques. These signaling techniques correspond to CCITT recommendation G.732. The NT6X27AC translates between one internal dual-port multiplexed DS60 signal and two external PCM30 lines. The system inverts every even bit. The duplicated DS60 system interface has embedded control data for the card. This feature improves reliability.

Location

The location of the card is between two external PCM30 lines and one internal system DS60 port.

Functional description

On the internal system face, the NT6X27AC must meet the DS60 standard. On the external face, the card must meet the PCM30 standard.

System interface

The system interface contains of the following main parts:

- DS60 signal specification
  - — frame format
  - — polarity
  - — multiplexing
  - — channel assignment
  - — channel skew
- system clock requirements
  - — signals terminating on a card
  - — clock signals from a card
- system reliability interface

NT6X27AC (continued)

DS60 signal specification

The DS60 interface contains two 32-channel incoming and outgoing ports multiplexed together. The system inverts the B2, B4, B6, and B8 on all voice channels automatically. Data for the two PCM30 lines is bit interleaved on the C390+ bus. The PCM30 data advances 37.5 bits (390 ns) in relation to a DSOUT signal. The following table defines the mapping between DS60 system timeslots, channel timeslots, and telephone channels.

System timeslot assignment (Sheet 1 of 2)

DS60 system timeslot	Incoming to card		Outgoing from card	
0	Card control		Card status	
1	Telephone channel	1	Telephone channel	1
2		2		2
3		3		3
4		4		4
5		5		5
6		6		6
7		7		7
8		8		8
9		9		9
10		10		10
11		11		11
12		12		12
13		13		13
14		14		14
15	Telephone channel	15	Telephone channel	15
16	Signaling		Signaling	
17	Telephone channel	16	Telephone channel	16
18		17		17

System timeslot assignment (Sheet 2 of 2)

DS60 system timeslot	Incoming to card		Outgoing from card	
19		18		18
20		19		19
21		20		20
22		21		21
23		22		22
24		23		23
25		24		24
26		25		25
27		26		26
28		27		27
29		28		28
30		29		29
31	Telephone channel	30	Telephone channel	30

System clock requirements

The basic system clock (C97+) and internal C390+ clocks have positive-going edges. Superframe pulse 48 frames (FP48) synchronize the edges. The system derives frame pulse from the incoming PCM30 data stream (RECFP) to synchronize one site clock to another site clock.

System reliability interface

The system for which the PCM30 line card provides an interface operates in a standby state. To make sure the system is reliable, each half of the reliability pair has an equivalent ACTIVITY signal. This signal selects the reliability pair for the DS60 interface. This signal selects the system clock.

Each NT6X27AC line card interfaces with two PCM30 lines. These PCM30 lines conform to an 8-bit, 32-channel timeslot serial transmission medium. The PCM30 lines operate at a rate of 2048 Kbps standard.

NT6X27AC (continued)

PCM30 interface

The PCM30 interface contains of the following main parts:

- electrical interface specification.
- PCM30 frame format.

Electrical interface specification

The NT6X27AC is switch compatible with the 75 Ω coaxial cable or the 120 Ω balanced pair electrical interconnection technique.

PCM30 frame format

The CCITT recommendation G.732 defines the PCM30 frame format. Of the 32 channel timeslots (CTS), 30 are for telephone channels. The 32 timeslots are 1 to 15 and 17 to 31. The CTS 0 functions include signaling and framing. The description of CTS 0 changes on alternate frames.

The CTS 16 is a signaling channel that allows for the following types of signaling:

- common channel signaling that uses CTS 16 as a 64 Kbps clear channel to transmit signaling information.
- channel-associated signaling that uses a sequence of 16 consecutive CTS 16s with a defined multiframe structure.

Functional blocks

The NT6X27AC contains of the following functional blocks:

- activity select and port split
- signaling multiplexer
- clock conversion
- clock extraction
- line interface
- slip buffer
- frame alignment circuitry
- channel-16 elastic store
- control timeslot
- status timeslot

Activity select and port split

The activity select and port split performs the following functions:

- selects the DS60 port based on the state of the ACTIVITY signal
- separates the incoming data stream in two separate ports for each card
- captures and deciphers the control byte that timeslot 0 contains
- loops the inactive port back to that inactive port
- loops four ports back to the international line trunk controller to provide additional looparound channels

Signaling multiplexer

The signaling multiplexer replaces the control information for the line card in system timeslot 0 with CTS 0 data. The signaling multiplexer replaces the information before the card transmits pulse code modulation (PCM) data. Output of the signaling mutiplexer loops around to the input mutiplexer to align the two data streams. The CTS 16 selective loop contains bit-inverted data because of the even bit inversion on the PCM30 card.

Clock conversion

The clock conversion changes the rate of data transmission after the establishment of the frame contents.

Clock extraction

The system establishes a clock associated with the incoming PCM30 data stream before the card can process channel data.

Line interface

The data stream receives code and bipolar conversion before transmission. After the bipolar conversion process, the card transmits the PCM stream. The system provides a set of relays to the digroup looparound path. The outgoing PCM30 data stream connects to the receive path on the digroup looparound path.

After the card translates incoming data from the bipolar format, the card decodes the data. The process is a high-density bipolar 3 decoding process. The card transmits the data to the retiming circuitry. The system maintains an error count based on the reception of data.

Slip buffer

The slip buffer synchronizes the PCM stream the retiming circuitry receives to the locally generated clock. The slip buffer does not synchronize the PCM stream to the system clock. The data and the clock that results are subject to jitter. A slip buffer removes or introduces complete frames of PCM to handle

NT6X27AC (continued)

jitter. The slip buffer adds or removes frames based on the immediate difference in receive and system clocks.

Frame alignment circuity

The frame alignment circuitry establishes a frame reference before the PCM30 card handles the incoming PCM for each channel. The frame alignment symbol (FAS) and multiframe alignment symbol (MFAS) define the frame.

Channel-16 elastic store

An external card in the system, receives a multiframe-aligned view of CTS 16. This card handles channel-associated channel-16 signaling.

Control timeslot

The byte in status timeslot 0 goes to one of four registers in the NT6X27AC. The state of B0 and B1 determine the destination of the byte. Refer to the following table.

Control timeslot

	B0	B1	B2	B3	B4	B5	B6	B7	System #
			National use						
Nat. signal	0	0	N8	N7	N6	N5	N4	X	
			International use						
Int. signal	0	1	IN0	I1	X	X	X	X	
					Digital	CAS			
Link control	1	0	Alarm	Reset	loop	dis.	X	X	
					Loop channel				
Loop control	1	1	L0	L1	L2	L3	L4	X	

Status timeslot

The byte output in status timeslot 0 from the NT6X27AC on the DS60 side contains status information. The state of B0 and B1 determines the description

of the status byte. The control register accessed last determines the status register selected for status timeslot 0. Refer to the following table.

Status timeslot

	B0	B1	B2	B3	B4	B5	B6	B7	System #
Nat. signal &			National use						
slip	0	0	N8	N7	N6	N5	N4	Slip *	
Int. signal &			International use		Alarm	Alarm	R. MF	R. MF	
link Tx status	0	1	IN0	I1	Rx	Rx *	loss	loss *	
			AIS	AIS	Frame	Frame	L. MF	L. MF	
Link Rx status	1	0	Rx	Rx *	loss	loss *		loss *	
			Error count						
Error count	1	1	E0	E1	E2	E3	E4	E5	

Note 1: An asterisk (*) indicates latched status bits. A 0 to 1 transition on the control reset bit resets these status bits.

Note 2: An AIS Rx indication is low active (0 indicates a received AIS). The latched version is high active.

NT6X27BA

Product description

The enhanced PCM30 interface card replaces previous versions of the pulse code modulation (PCM) interface card for transmission of PCM data at 2.048 Mbps (European standards). The NT6X27BA provides interface functions, diagnostics and maintenance for the PCM interface according to two interface standards. The NT6X27BA uses DS60 for PCM data at 5.12 Mbps and PCM30 for PCM data at 2.048 Mbps.

Location

The NT6X27BA is in all extended multiprocessor system peripheral modules (XPM).

Functional description

Functional blocks

The NT6X27BA contains the following functional blocks:

- PCM interface
- digroup loop
- selective channel loop
- DS60 interface

Each functional block is present in duplicate because the NT6X27BA supports two PCM interfaces.

PCM interface

The PCM interface contains of a PCM line interface integrated circuit, CS61574, with a transmit and a receive section. Each section functions separately from the other. The PCM interface receives and transmits data between the peripheral side (P-side) PCM30 ports and the DS60 interface.

The receive section of the CS61574 recovers the clock and data from the incoming PCM30 stream and outputs clock and synchronized data.

The transmit section of the CS611574 takes formatted data from the DS60 interface. The transmit sections produces pulses of the appropriate shape to transmit back to the P-side.

Digroup loop

The digroup loop is a diagnostic feature. The feature can be activated to loop all 32 time slots back through the receive circuitry of the application-specific integrated circuit (ASIC). The 32 time slots are already formatted for

transmission. This action allows diagnostic software to perform a complete hardware evaluation of the NT6X27BA.

Selective channel loop

The selective channel group is a diagnostic feature that can select a single channel and loop a channel back to the central side (C-side). This feature allows diagnostic software to do a limited hardware evaluation of the NT6X27BA.

DS60 interface

The DS60 interface contains an ASIC, S46, with a transmit and a receive section. Each section functions separately from the other. The DS60 interface receives and transmits data between the PCM interface and the C-side interface.

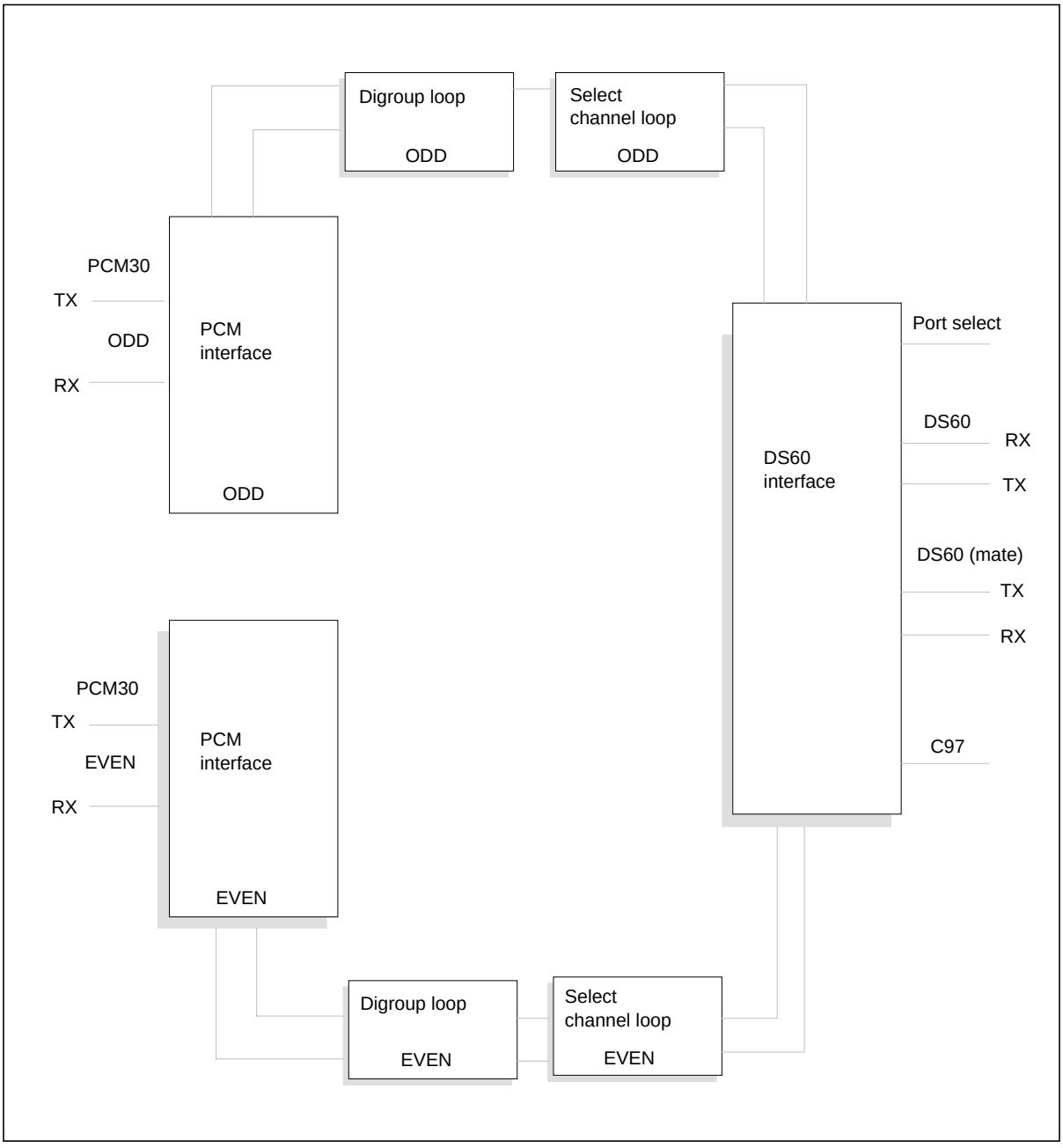
The receive section of the ASIC takes the synchronized clock and data from the PCM interface. The receive section performs a code and bipolar conversion process. The receive section multiplexes two DS30 streams of formatted data into one DS60 data stream. The DS60 data stream goes to the C-side interface.

The transmit section of the ASIC reverses the actions of the receive section. The transmit activity begins when ASIC accepts the C-side DS60 data stream. The activity ends when ASIC transmits formatted data to the PCM interface.

The relationship between the functional blocks appears in the following figure.

NT6X27BA (continued)

NT6X27BA functional blocks



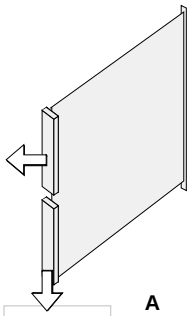
Signaling

Pin numbers

The pin numbers for NT6X27BA appear in the following figure.

NT6X27BA (continued)

NT6X27BA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	PWR+5	PWR+5
3A 3B	PWR+5	PWR+5
4A 4B	+5–M	+5–M
5A 5B	GND	GND
6A 6B		C97+
7A 7B	GND	GND
8A 8B	ACTY–	
9A 9B	GND	GND
10A 10B	FP48–	FP48–M
11A 11B	SENDT0	SENDR0
12A 12B	SENDT1	SENDR1
13A 13B		
14A 14B		
15A 15B		
16A 16B		
17A 17B	C97+M	
18A 18B	GND	
19A 19B	DSOUT	DSOUTM
20A 20B		
21A 21B	ETS	ETSM
22A 22B		
23A 23B		
24A 24B		
25A 25B		
26A 26B		
27A 27B		
28A 28B		
29A 29B		
30A 30B		
31A 31B		
32A 32B		
33A 33B		
34A 34B		
35A 35B		
36A 36B		
37A 37B		
38A 38B		
39A 39B		
40A 40B		

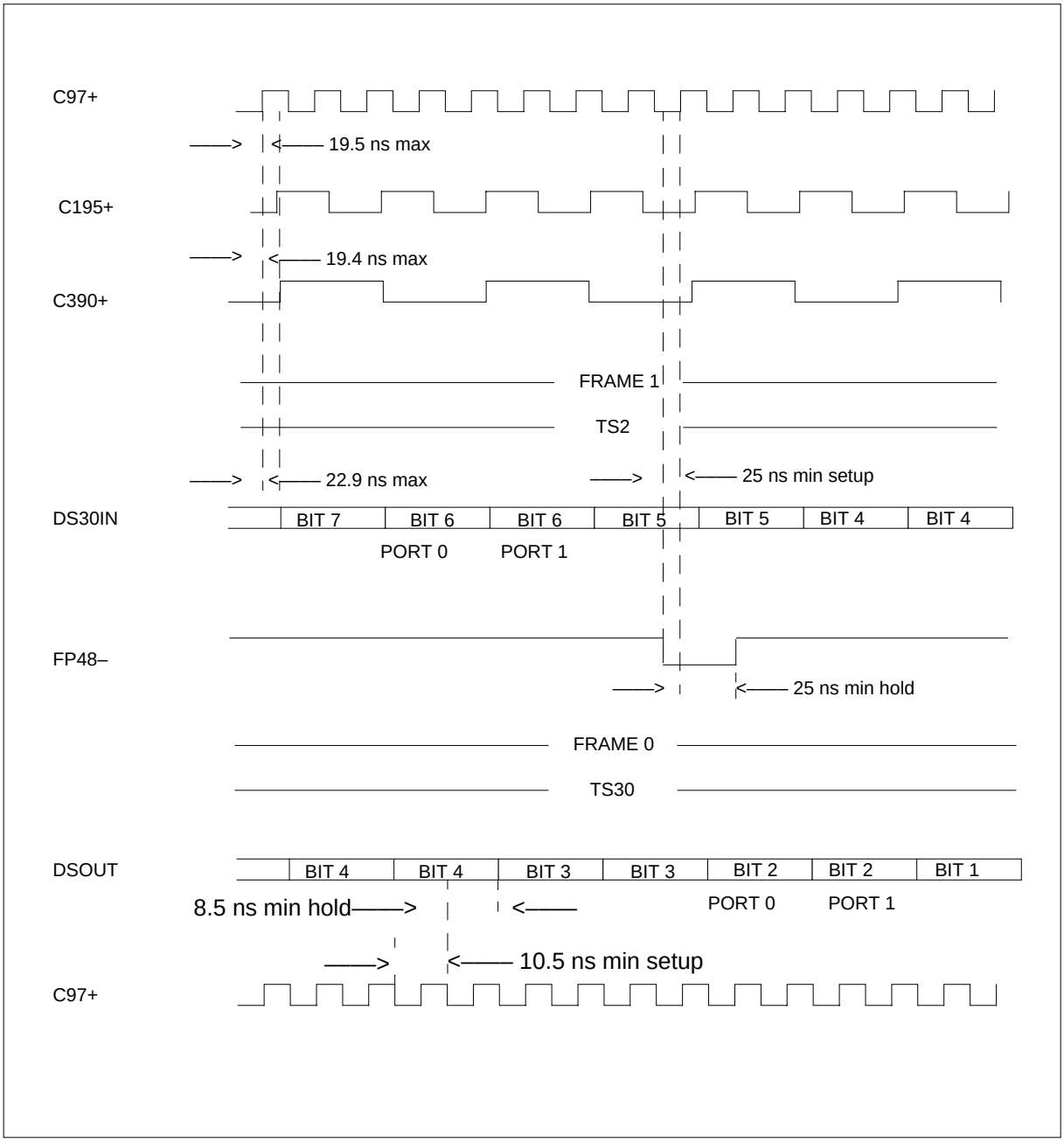
	A	B
41A 41B		
42A 42B		
43A 43B		
44A 44B		
45A 45B		
46A 46B		
47A 47B		
48A 48B		
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B		
58A 58B		
59A 59B		
60A 60B		
61A 61B		
62A 62B		
63A 63B		
64A 64B		
65A 65B		
66A 66B		
67A 67B		
68A 68B		
69A 69B	C	CM
70A 70B	RECFPR	
71A 71B	+12–M	
72A 72B	RECT0	RECR0
73A 73B	RECT1	RECR1
74A 74B	RECFP	RECFP–M
75A 75B	PCM30IN	PCM30IN–M
76A 76B	GND	GND
77A 77B	PWR+12	PWR+12
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

NT6X27BA (continued)

Timing

The worst case timing for hardware interfaces for the NT6X27BA appears in the following figure.

NT6X27BA hardware interface timing



Technical data

Power requirements

The supply voltage for the NT6X27BA is as follows:

- minimum 4.75 V
- nominal 5.0 V
- maximum 5.5 V

The nominal supply current is 350 mA.

NT6X27BB

Product description

The enhanced PCM30 interface card replaces previous versions of the pulse code modulation (PCM) interface card for transmission of PCM data at 2.048 Mbps (European standards). The NT6X27BB provides interface functions, diagnostics and maintenance for the PCM interface according to two interface standards. The NT6X27BB uses DS60 for PCM data at 5.12 Mbps and PCM30 for PCM data at 2.048 Mbps.

Location

The NT6X27BB resides in all extended multiprocessor system peripheral modules (XPM).

Functional description

Functional blocks

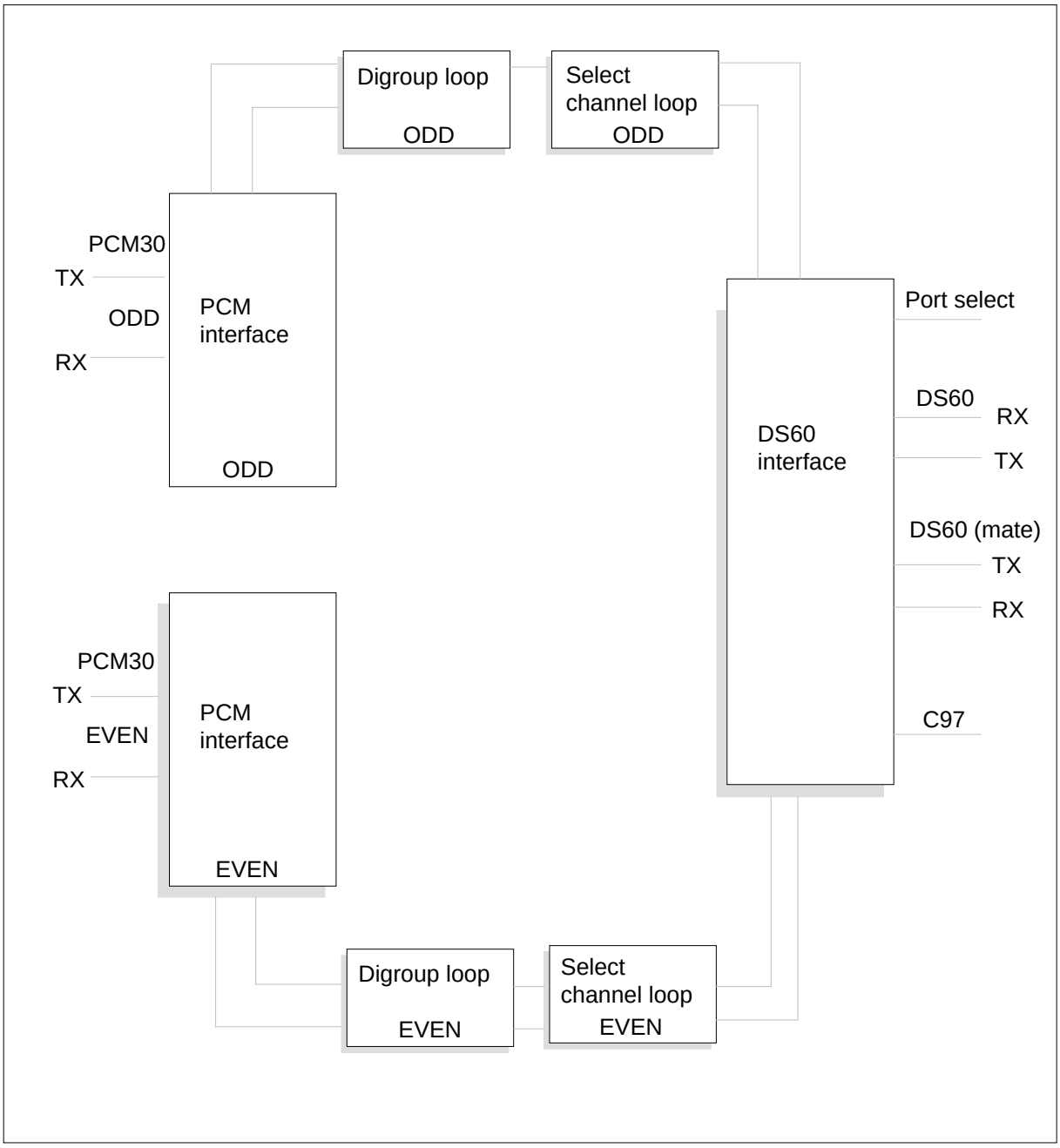
The NT6X27BB contains the following functional blocks:

- PCM interface
- digroup loop
- selective channel loop
- DS60 interface

The functional blocks are present in duplicate because the NT6X27BB supports two PCM interfaces.

The relationship between the functional blocks appears in the following figure.

NT6X27BB functional blocks



PCM interface

The PCM interface contains a PCM line interface integrated circuit, CS61574, with a transmit and a receive section. Each section functions separately from

NT6X27BB (continued)

the other. The PCM interface receives and transmits data between the peripheral side (P-side) PCM30 ports and the DS60 interface.

The receive section of the CS61574 recovers the clock and data from the incoming PCM30 stream and outputs clock and synchronized data.

The transmit section of the CS61574 takes formatted data from the DS60 interface. The transmit section produces pulses of the appropriate shape to transmit back to the P-side.

Digroup loop

The digroup loop is a diagnostic feature. The feature can loop all 32 time slots back through the receive circuitry of the application-specific integrated circuit (ASIC) when activated. The 32 time slots are already formatted for transmission. This action allows diagnostic software to perform a complete hardware evaluation of the NT6X27BB.

Selective channel loop

The selective channel loop is a diagnostic feature that can select a single channel and loop it back to the central side (C-side). This feature allows diagnostic software to do a limited hardware evaluation of the NT6X27BB.

DS60 interface

The DS60 interface contains an ASIC, S46, with a transmit and a receive section. Each section functions separately. The DS60 interface receives and transmits data between the PCM interface and the C-side interface.

The receive section of the ASIC takes the synchronized clock and data from the PCM interface. The receive section performs a code and bipolar conversion process. The receive section multiplexes two DS30 streams of formatted data into one DS60 data stream. The DS60 data stream goes to the C-side interface.

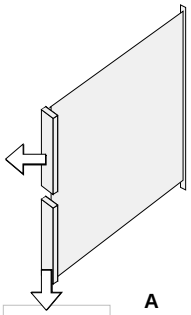
The transmit section of the ASIC reverses the actions of the receive section. The transmit activity begins when ASIC accepts the C-side DS60 data stream. The activity ends when ASIC transmits formatted data to the PCM interface.

Signaling

Pin numbers

The pin numbers for NT6X27BB appear in the following figure.

NT6X27BB pin numbers



	A	B
1A 1B	GND	GND
2A 2B	PWR+5	PWR+5
3A 3B	PWR+5	PWR+5
4A 4B	+5–M	+5–M
5A 5B	GND	GND
6A 6B		C97+
7A 7B	GND	GND
8A 8B	ACTY–	
9A 9B	GND	GND
10A 10B	FP48–	FP48–M
11A 11B	SENDT0	SENDR0
12A 12B	SENDT1	SENDR1
13A 13B		
14A 14B		
15A 15B		
16A 16B		
17A 17B	C97+M	
18A 18B	GND	
19A 19B	DSOUT	DSOUTM
20A 20B		
21A 21B	ETS	ETSM
22A 22B		
23A 23B		
24A 24B		
25A 25B		
26A 26B		
27A 27B		
28A 28B		
29A 29B		
30A 30B		
31A 31B		
32A 32B		
33A 33B		
34A 34B		
35A 35B		
36A 36B		
37A 37B		
38A 38B		
39A 39B		
40A 40B		

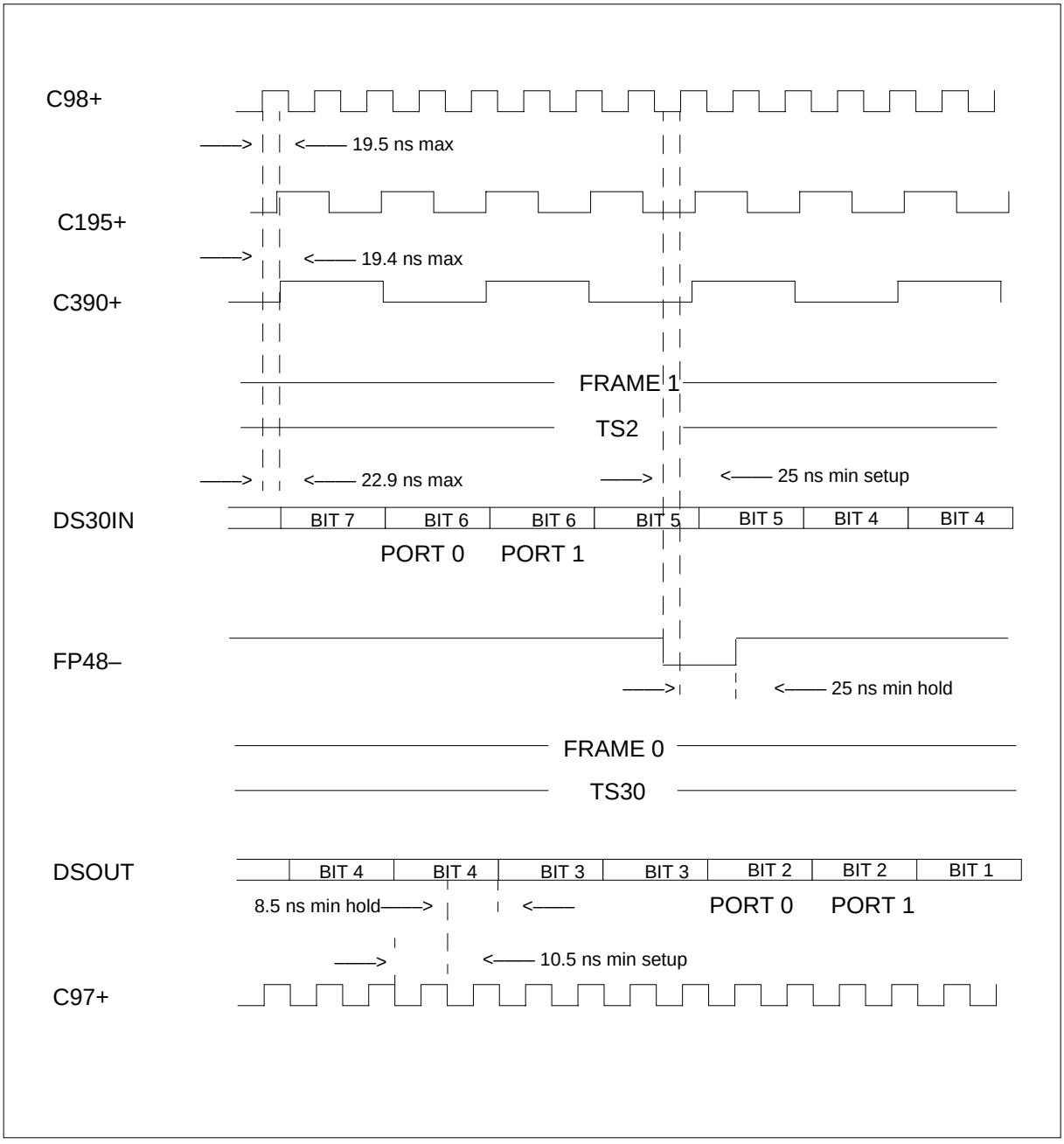
	A	B
41A 41B		
42A 42B		
43A 43B		
44A 44B		
45A 45B		
46A 46B		
47A 47B		
48A 48B		
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B		
58A 58B		
59A 59B		
60A 60B		
61A 61B		
62A 62B		
63A 63B		
64A 64B		
65A 65B		
66A 66B		
67A 67B		
68A 68B		
69A 69B	C	CM
70A 70B	RECFPR	
71A 71B	+12–M	
72A 72B	RECT0	RECR0
73A 73B	RECT1	RECR1
74A 74B	RECFP	RECFP–M
75A 75B	PCM30IN	PCM30IN–M
76A 76B	GND	GND
77A 77B	PWR+12	PWR+12
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

NT6X27BB (continued)

Timing

The worst case timing for hardware interfaces for the appears in the following figure.

NT6X27BB hardware interface timing



Technical data

Power requirements

The supply voltage for the NT6X27BB is as follows:

- minimum 4.75 V
- nominal 5.0 V
- maximum 5.5 V

The nominal supply current is 350 mA.

NT6X27BD

Product description

The enhanced PCM30 interface card replaces previous versions of the pulse code modulation (PCM) interface card for transmission of PCM data at 2.048 Mbps (European standards). The NT6X27BD provides interface functions, diagnostics and maintenance for the PCM interface according to two interface standards. The NT6X27BD uses DS60 for PCM data at 5.12 Mbps and PCM30 for PCM data at 2.048 Mbps.

Location

The NT6X27BD resides in all extended multiprocessor system peripheral modules (XPM).

Functional description

Functional blocks

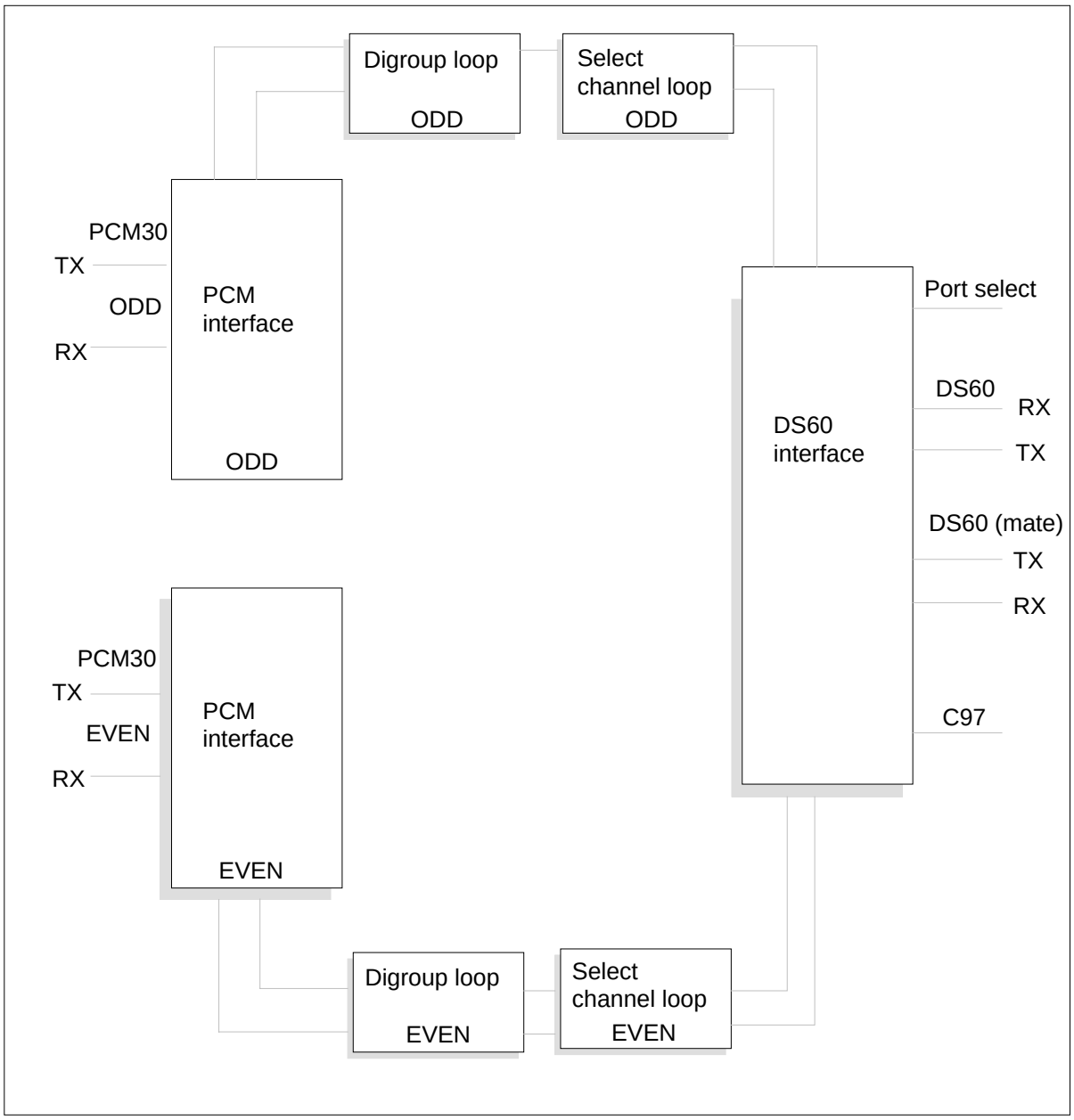
The NT6X27BD contains the following functional blocks:

- PCM interface
- digroup loop
- selective channel loop
- DS60 interface

The functional blocks are present in duplicate because the NT6X27BD supports two PCM interfaces.

The relationship between the functional blocks appears in the following figure.

NT6X27BD functional blocks



PCM interface

The PCM interface contains a PCM line interface integrated circuit, CS61574, with a transmit and a receive section. Each section functions separately from the other. The PCM interface receives and transmits data between the peripheral side (P-side) PCM30 ports and the DS60 interface.

NT6X27BD (continued)

The receive section of the CS61574 recovers the clock and data from the incoming PCM30 stream and outputs clock and synchronized data.

The transmit section of the CS61574 takes formatted data from the DS60 interface. The transmit section produces pulses of the appropriate shape to transmit back to the P-side.

Digroup loop

The digroup loop is a diagnostic feature. The feature can loop all 32 time slots back through the receive circuitry of the application-specific integrated circuit (ASIC) when activated. The 32 time slots are already formatted for transmission. This action allows diagnostic software to perform a complete hardware evaluation of the NT6X27BD.

Selective channel loop

The selective channel loop is a diagnostic feature that can select a single channel and loop it back to the central side (C-side). This feature allows diagnostic software to do a limited hardware evaluation of the NT6X27BD.

DS60 interface

The DS60 interface contains an ASIC, S46, with a transmit and a receive section. Each section functions separately. The DS60 interface receives and transmits data between the PCM interface and the C-side interface.

The receive section of the ASIC takes the synchronized clock and data from the PCM interface. The receive section performs a code and bipolar conversion process. The receive section multiplexes two DS30 streams of formatted data into one DS60 data stream. The DS60 data stream goes to the C-side interface.

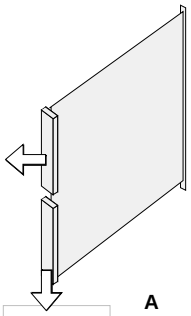
The transmit section of the ASIC reverses the actions of the receive section. The transmit activity begins when ASIC accepts the C-side DS60 data stream. The activity ends when ASIC transmits formatted data to the PCM interface.

Signaling

Pin numbers

The pin numbers for NT6X27BD appear in the following figure.

NT6X27BD pin numbers



	A	B
1A 1B	GND	GND
2A 2B	PWR+5	PWR+5
3A 3B	PWR+5	PWR+5
4A 4B	+5–M	+5–M
5A 5B	GND	GND
6A 6B		C97+
7A 7B	GND	GND
8A 8B	ACTY–	
9A 9B	GND	GND
10A 10B	FP48–	FP48–M
11A 11B	SENDT0	SENDR0
12A 12B	SENDT1	SENDR1
13A 13B		
14A 14B		
15A 15B		
16A 16B		
17A 17B	C97+M	
18A 18B	GND	
19A 19B	DSOUT	DSOUTM
20A 20B		
21A 21B	ETS	ETSM
22A 22B		
23A 23B		
24A 24B		
25A 25B		
26A 26B		
27A 27B		
28A 28B		
29A 29B		
30A 30B		
31A 31B		
32A 32B		
33A 33B		
34A 34B		
35A 35B		
36A 36B		
37A 37B		
38A 38B		
39A 39B		
40A 40B		

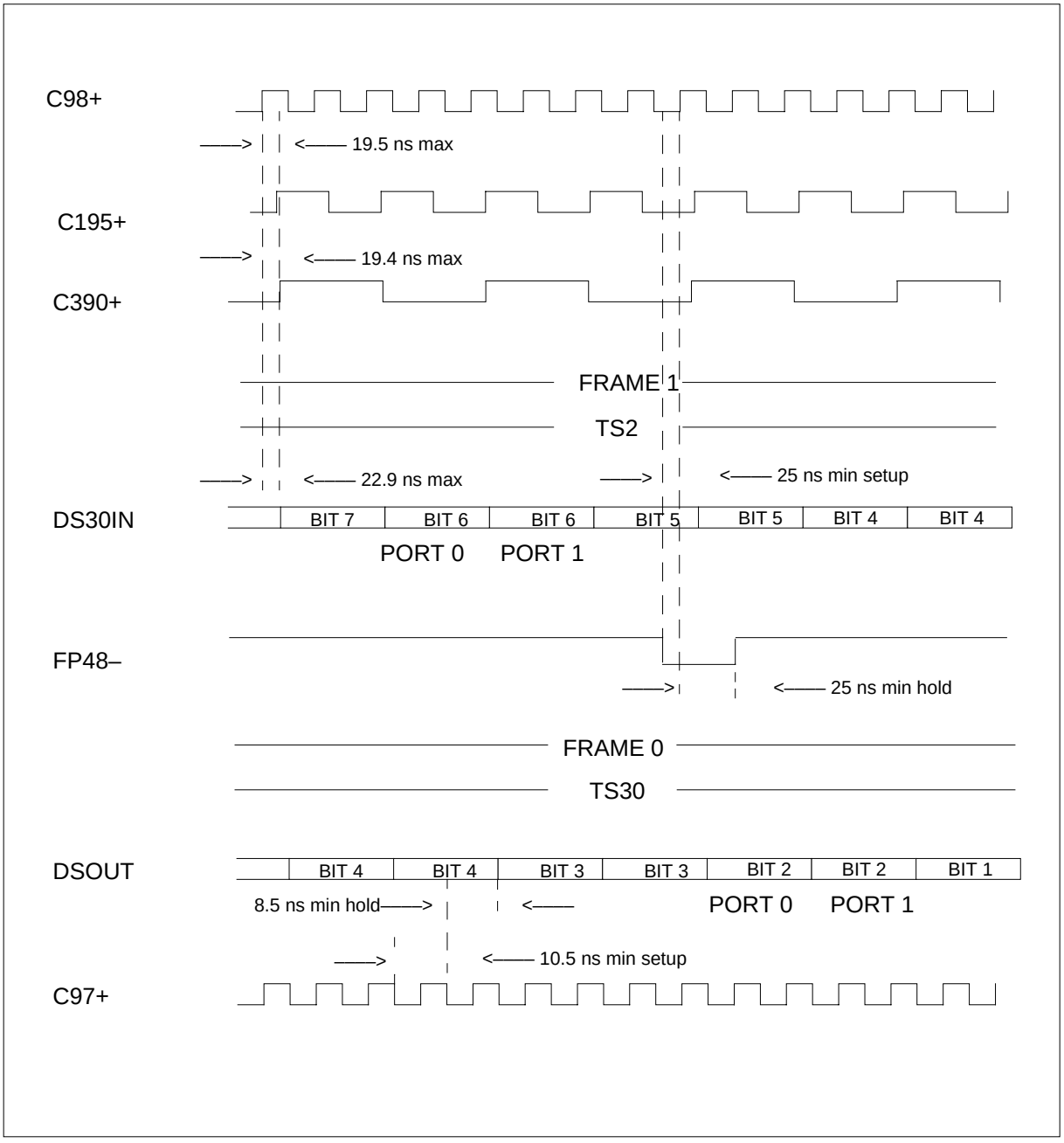
	A	B
41A 41B		
42A 42B		
43A 43B		
44A 44B		
45A 45B		
46A 46B		
47A 47B		
48A 48B		
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B		
58A 58B		
59A 59B		
60A 60B		
61A 61B		
62A 62B		
63A 63B		
64A 64B		
65A 65B		
66A 66B		
67A 67B		
68A 68B		
69A 69B	C	CM
70A 70B	RECFPR	
71A 71B	+12–M	
72A 72B	RECT0	RECR0
73A 73B	RECT1	RECR1
74A 74B	RECFP	RECFP–M
75A 75B	PCM30IN	PCM30IN–M
76A 76B	GND	GND
77A 77B	PWR+12	PWR+12
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

NT6X27BD (continued)

Timing

The worst case timing for hardware interfaces for the appears in the following figure.

NT6X27BD hardware interface timing



Technical data

Power requirements

The supply voltage for the NT6S27BD is as follows:

- minimum 4.75 V
- nominal 5.0 V
- maximum 5.5 V

The nominal supply current is 350 mA.

NT6X27JA

Product description

The NT6X27JA M20 interface card connects external M20 links or TTC links with the host PCM30 digital trunk controller (PDTC). This connection occurs over a DS60 interface.

The NT6X27JA is between two external M20 or TTC links and one internal DS60 port. This positioning indicates that the NT6X27JA meets the following interface standards:

- M20
- TTC
- DS60

The M20 and TTC are the Japanese standards for the transmission of pulse code modulated (PCM) data at 2.048 Mbps.

The DS30 is time-division multiplexed (TDM) PCM data transmitted at 2.560 Mbps.

The DS60 is TDM PCM data transmitted at 5.120 Mbps.

Location

The NT6X27JA fits in slots 2 to 5 in both shelves of a PDTC, in a DMS switch.

Functional description

The NT6X27JA has the following functions:

- connects M20/TTC links with the host PDTC over a DS60 interface
- provides incoming elastic buffering to control wandering of the DMS clock system relative to the digital clock system (DCS)
- connects with the M20/TTC interface at 2.048 Mbps
- extracts and inserts signaling bits for each of the 30 speech/data channels, in time slot 0 (TS0)
- reports performance errors
- reports alarm conditions

The M20/TTC standard transmits serial data at 2.048 Mbps.

The DS60 standard transmits serial data at 5.120 Mbps. The DS60 standard acts as host for the NT6X27JA for internal use on the PDTC.

Functional blocks

The NT6X27JA duplicates the following to support the M20/TTC interfaces:

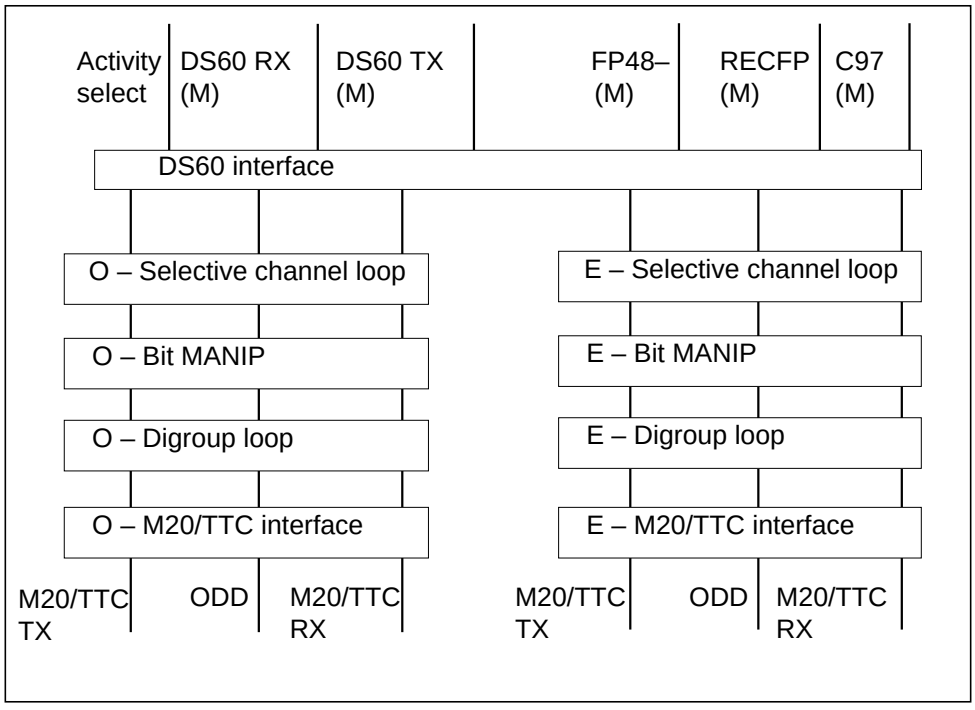
- selective channel loop
- bit manipulator
- digroup loop

The NT6X27JA has the following functional blocks:

- DS60 interface
- selective channel loop
- bit manipulator (MANIP)
- digroup loop
- M20/TTC interface

The relationship between the functional blocks appears in the following figure.

NT6X27JA functional blocks



Note: M indicates that the signals are duplicated

NT6X27JA (continued)

DS60 interface

The DS60 interface buffers signals to and from the central side (C-side). Each DS60 link contains two bit-interleaved DS30 data streams. Each link carries the data for one of the M20/TTC interfaces. The DS60 interfaces are duplicated within the PDTC system for security.

Selective channel loop

The selective channel loop is a feature used to loop a selected voice channel back toward the C-side DS60 interface.

Bit manipulator

The bit manipulator moves signaling bits (A-bits). The manipulator moves the bits from TS16 of the C-side DS30 data stream to TS0 of the processor side (P-side) of the M20/TTC interface. This action also occurs along the same route in the opposite direction. The manipulator extracts control information from TS0 of the received C-side data. The manipulator also inserts status information into TS0 and TS16 of the transmitted C-side data.

Digroup loop

The digroup loop is a feature that loops all 32 time slots formatted for M20/TTC transmission back through the receive circuitry. This loopback allows the software to perform a complete hardware evaluation of the NT6X27JA. When data is looped, the transmits all ones (1) at the M20/TTC interface.

M20/TTC interface

The M20/TTC interface is a transformer-coupled line interface that handles M20/TTC data at 2.048 Mbps.

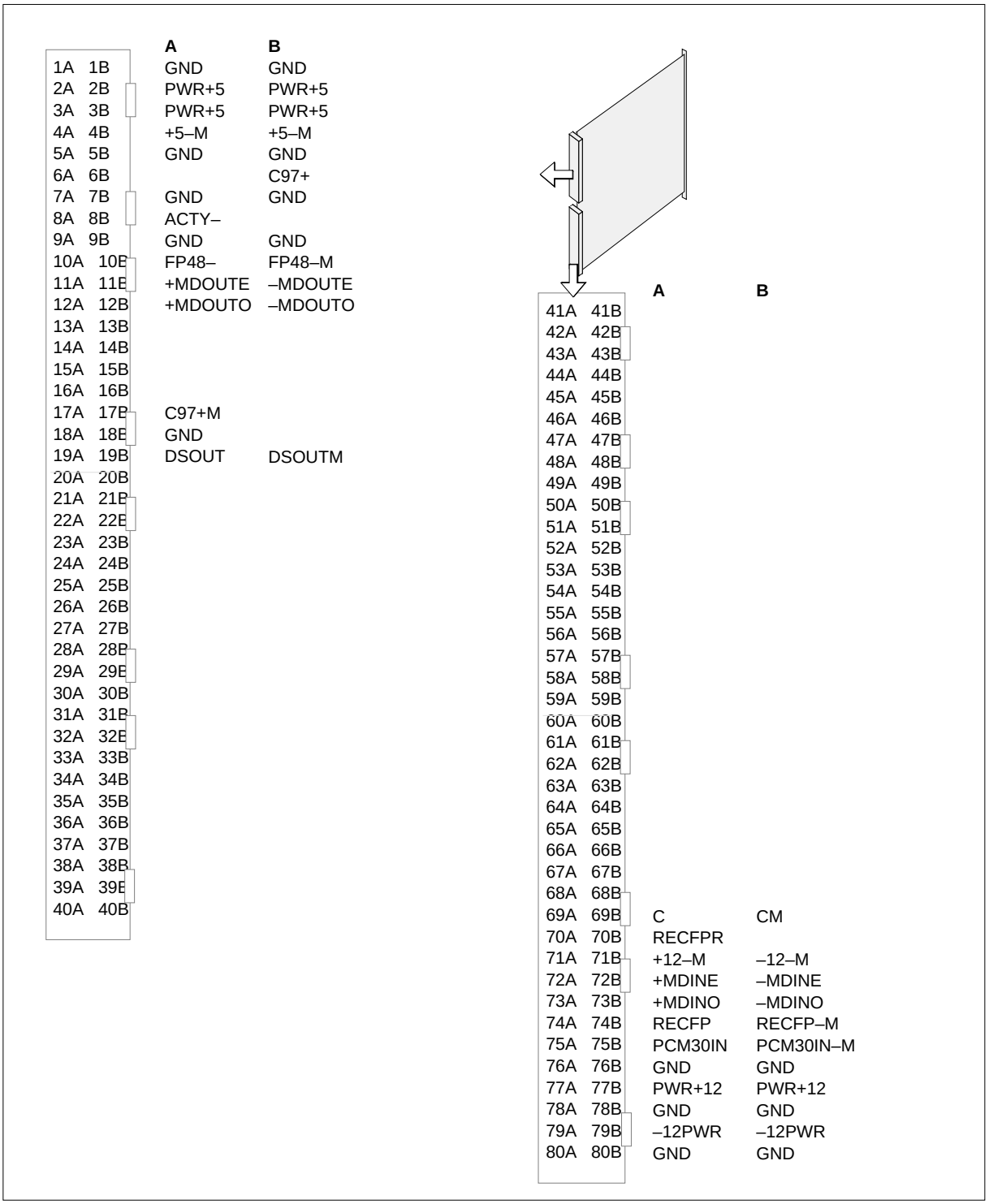
Signaling

Pin numbers

The pin numbers for the NT6X27JA appear in the following figure.

NT6X27JA (continued)

NT6X27JA pin numbers



NT6X27JA (end)

Technical data

Physical description

The NT6X27JA is a standard two-layer printed circuit board that does not require special manufacturing processes.

Technology

The NT6X27JA uses two ASIC devices (U17 and 35) developed for the Japan project. The ASICs are packaged as 68-pin pin grid arrays (PGA), on an 11 by 11 grid.

Power requirements

The NT6X27JA uses the following power supply voltages:

- -12 V
- -12 V backup
- +12 V
- +12 V backup
- +5 V
- +5 V backup
- GND

The power requirements for the NT6X27JA appear in the following table.

Power requirements of the NT6X27JA

Parameter	Minimum	Nominal	Maximum	Units
Supply voltage	+4.75	+5.00	+5.25	volts
		+12		volts
		-12		volts
Supply ripple	–	–	–	
Supply current	–	860	–	milliamperes

NT6X28AA

Product description

The NT6X28AA extracts signaling information from and insert signaling information into the parallel speech buses of the international digital trunk controller (IDTC). The NT6X28AA uses channel time slot (CTS) 16. The CTS 0 communicates control and status information between the processor and the PCM30 interface card.

Functional description

Functional blocks

The NT6X28AA contains the following functional blocks:

- CTS 16 signaling receive interface
- FIFO interface
- CTS 16 signaling transmit interface
- bit-to-bit-9 mapping
- control and status register interface
- processor interface
- timing generation

CTS 16 signaling receive interface

The interface extracts signaling information from the PCM30 links during CTS 16 of the incoming parallel speech bus (SPIN 0-7). Each CTS 16 contains signaling information for two channels for the 16 ports. The information for the 32 channels (for each port) is sent during 16 frames. Each channel has 4 signaling bits. The signaling bits are A, B, C, and D.

The system extracts signaling information for the two channels from the speech bus at the same time. Two RAMs store this information separately. The system enables both RAMs together and uses the same address for separate storage. The separate storage allows for storage of the ABCD values for the two channels in the same location. The storage of the ABCD values occurs on different RAMs.

Address bit 9 selects one of the two RAMs because the processor accesses signaling information for only one channel at a time.

The other RAMs store mask information, which masks bits for channels that do not directly affect the software. These RAMs are addressed in the same method as the receive RAMs (address bit 9). You must write a zero in the appropriate location of the mask to mask a bit.

NT6X28AA (continued)

If the FIFO is not full, the system updates receive RAM with the new ABCD information.

FIFO interface

The new ABCD value from the speech bus is the CID value. The CID and the XOR values latched in the receiver are written in the FIFO at one location. The system generates the write if a mismatch is present and an overflow is not present.

The FIFO contains a series of five 16X4 RAMs. The processor or a local counter can address the FIFO. The processor provides the read address and the counter provides the write address. A multiplexer selects the processor or the counter. During CTS 16, the counter address or the processor address is chosen. Each time the system performs a write, the write address increases by one. During processor access, two separate read instructions read the address information stored in each location. A word-read accesses the CID, and a byte-read compares the value and the XOR value. For each location, a word read must be performed before a byte read. The read address increases after the byte read. The read address and the write address are compared. The current and previous values of these addresses determine the overflow and empty status of the FIFO.

CTS 16 signaling transmit interface

The system inserts the signaling information the processor supplies into the outgoing parallel speech bus (SPOUT 0-7). The insertion occurs during CTS 16 use of this circuit. When the processor accesses the RAMs, address bit 9 selects one of the two RAMs. When the local counter addresses the RAMs, both RAMs are selected.

A buffer interfaces the signaling information to the speech bus. The buffer is enabled during CTS. The speech enable signals control of the buffer. The connection memory of the message interface card provides the signals.

CTS 0 control and status register interface

This circuit exchanges the following control and status information between the processor and the PCM30 interface card:

- international signaling
- loopback controls
- maintenance commands

Two RAMs are used for this exchange. The lower half of the RAMs stores the command bytes. The upper half of the RAMs stores the status bytes.

During CTS 0, the status bytes are extracted from the incoming speech bus. The command bytes are inserted in to the outgoing speech bus. This action occurs for all 16 ports during one CTS 0 time. Each CTS 0 contains control and status bytes for one register. Four registers are on each port. Sixty-four command bytes and 64 status bytes correspond to the 16 ports. The command and status byte locations are rewritten every four frames.

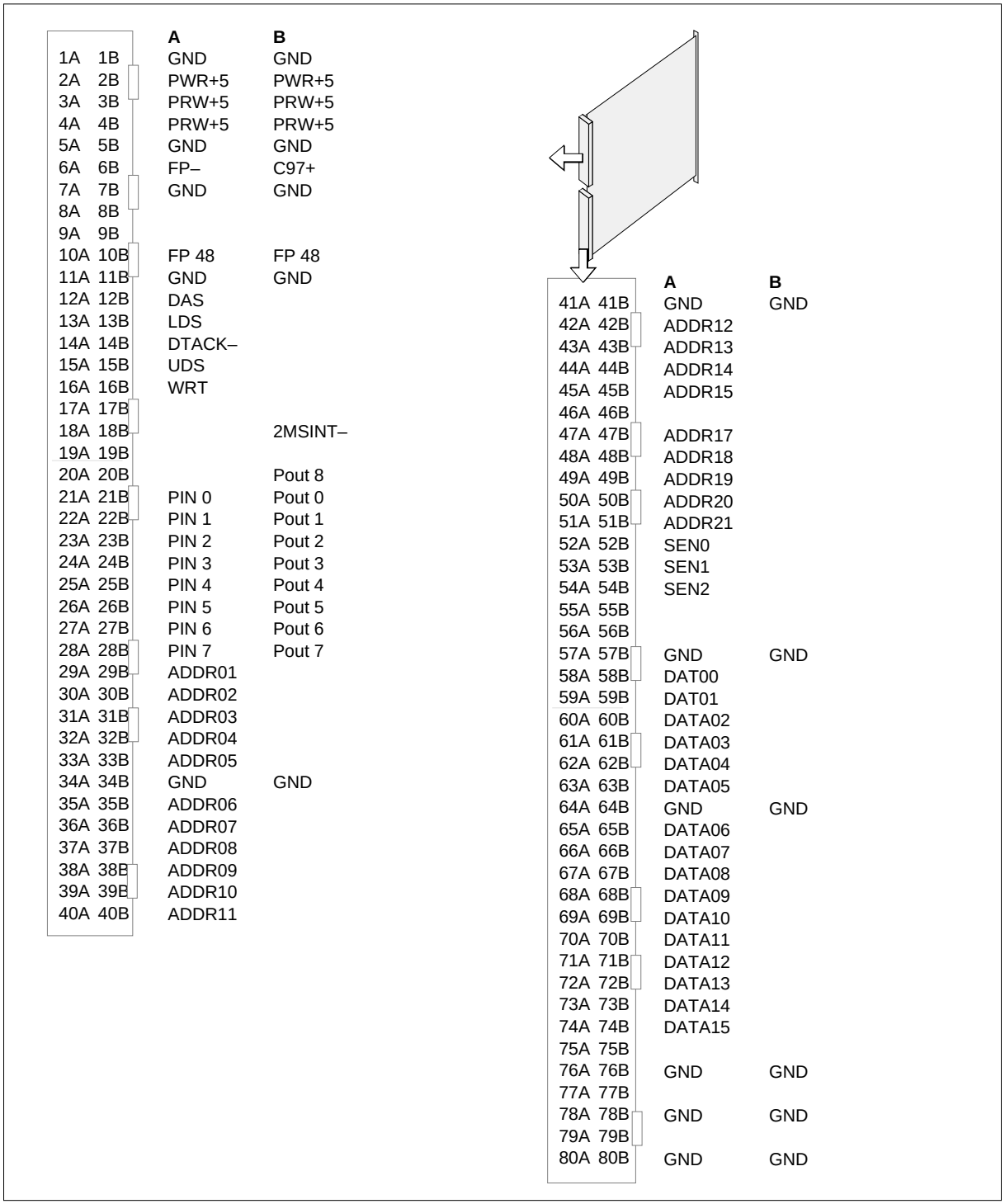
Signaling

Pin numbers

The pin numbers for the NT6X28AA appear in the following figure.

NT6X28AA (end)

NT6X28AA pin numbers



NT6X28AB

Product description

The NT6X28AB extracts and inserts signaling information to and from the parallel speech buses of the international digital trunk controller (IDTC). The NT6X28AB uses channel time slot (CTS) 16 to perform this procedure. The CTS 0 communicates control and status information between the processor and the PCM30 interface card.

Functional description

Functional blocks

The NT6X28AB contains the following functional blocks:

- CTS 16 signaling receive interface
- FIFO interface
- CTS 16 signaling transmit interface
- CTS 0 PCM30 control and status register interface
- metering bit (MBIT) insertion
- speech bus interface
- timing and control logic
- processor interface

CTS 16 signaling receive interface

The NT6X28AB extracts signaling information that comes from the PCM30 links. The NT6X28AB extracts this information during CTS 16 of the incoming parallel speech bus (SPIN 2-9). Each CTS 16 contains signaling information for two channels of the 16 ports. The system sends information for the 32 channels or two channels for each port during 16 frames. Each channel has 4 signaling bits: A, B, C and D.

The system uses two RAMs to store information for two channels separately. The NT6X28AB extracts signaling information for two channels at the same time from the speech bus. The NT6X28AB enables both RAMs and uses the same address. Two different RAMs store the ABCD values for the two channels. The two RAMs are at the same location.

The system uses address bit 9 to select one of the two RAMs. This procedure occurs because the processor accesses signaling information for one channel at a time.

Two other RAMs store mask information. This information masks out bits for any channel not related to the software. These RAMs are addressed like the

NT6X28AB (continued)

receive RAMs. To mask out a specified bit, the system writes a 0 in to the appropriate location of the mask.

The system updates the receive RAM with the new ABCD information if the FIFO is not full.

FIFO interface

The following are written into the FIFO at one location:

- terminal ID (TID)
- new ABCD value
- XOR logic value that the system latches in the receiver

The write operation occurs if there is a mismatch and there is no overflow.

The FIFO contains a series of five 16X4 RAMs that the processor or a local counter can address. The counter provides the write address and the processor provides the read address. A multiplexer selects the counter or the processor. During CTS 16, the multiplexer selects the counter address. The rest of the time, the multiplexer selects the processor address. Each time a write occurs, the write address increases by 1. During processor access, two separate read instructions read the address information stored in each location. A word read accesses the TID and a byte read compares this value and the XOR logic value. For each location, a word read must occur before a byte read. The read address increases after the byte read. The read address and the write address are compared. The current and previous values of the addresses determine the overflow and empty status of the FIFO.

An overflow status bit and an empty status bit provide information about the queue to the processor. The system provides an interrupt to the processor at the beginning of every multiframe. The interrupt is a flag for the processor to read the status register (SR). Reading the SR clears the interrupt flag.

During initialization of the card, an access to location 1A5000 must occur. An access to location 1A5000 sets the FIFO read and write counters to 0. An access to location 1A5000 sets the SR to empty condition. This procedure makes sure that the processor does not read the FIFO until a valid entry is written in after initialization.

CTS 16 signaling transmit interface

The NT6X28AB uses this circuit to insert signaling information that the processor supplies. This circuit inserts information in to the outgoing parallel speech bus (SPOUT 2-9) during CTS 16. When the processor accesses the

RAMs, the system uses address bit 9 to select one of the two RAMs. When the local counter addresses the RAMs, both RAMs are selected.

The system uses a buffer to interface the signaling information to the speech bus. The buffer is enabled during CTS 16. The speech enable signals control the buffer. The connection memory of the message interface card provides these signals.

CTS 0 PCM30 control and status register interface

This circuit card allows the exchange of control and status information between the processor and the PCM30 interface card. Control and status information includes international signaling, loopback controls and maintenance commands. The system uses two RAMs for this purpose. The lower half of the RAMs stores the command bytes. The upper half of the RAMs stores the status bytes.

During CTS 0, the NT6X28AB extracts status bytes for all 16 ports from the incoming speech bus. The NT6X28AB inserts the command bytes in to the outgoing speech bus. Each CTS 0 contains control and status bytes for one register. There are 64 command bytes and 64 status bytes that correspond to the 16 ports. Four registers are present for each port. These locations are written again every four frames.

Metering bit insertion

During the PCM timeslots, the system uses B1 to give metering information on each timeslot to the subscriber. The processor uses the A bit to write the metering information on the signaling card. The card stores this information in a separate RAM. The system reads this information out of RAM and inserts this information in B1 of the outgoing speech bus in sequence.

Speech bus interface

The speech bus interface contains the logic required to access the speech bus at the correct time. The incoming bus is enabled during CTS 16 and CTS 0 with use of separate latched buffers. The system disables incoming bus in looparound mode and RAM disable mode. The outgoing speech bus is enabled during CTS 0 and CTS 16 with use of the speech bus connection memory enable signal.

Timing and control logic

Logic for timing and control includes the following:

- synchronized clock generation
- address generation
- gating and timing signals

NT6X28AB (continued)

- counter that generates a 2-ms interrupt to the processor with use of superframe pulse 48 frames (FP48)
- card control register that uses 3 bits of the byte:
  - least significant bit (bit 0) = looparound, enable high
  - bit 1 = interrupt disable, active high
  - message (bit 2) = RAM disable, active low

Processor interface

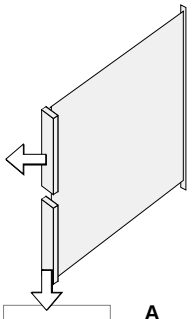
A comparator selects the card when the processor generates the correct address. An inhibit signal does not allow the processor to access the card during CTS 0 and CTS 16. The system sends a data transfer acknowledge (DTACK) signal back to the processor to indicate successful access. The circuits contain a series of buffers for the different RAMs to access the processor data bus.

Signaling

Pin numbers

The pin numbers for the NT6X28AB appear in the following figure.

NT6X28AB pin numbers



	A	B
1A 1B	GND	GND
2A 2B	PWR+5	PWR+5
3A 3B	PRW+5	PRW+5
4A 4B	PRW+5	PRW+5
5A 5B	GND	GND
6A 6B	FP-	C97+
7A 7B	GND	GND
8A 8B		
9A 9B		
10A 10B	FP 48	FP 48
11A 11B	GND	GND
12A 12B	DAS	
13A 13B	LDS	
14A 14B	DTACK-	
15A 15B	UDS	
16A 16B	WRT	
17A 17B		
18A 18B		2MSINT-
19A 19B		
20A 20B		POUT 8
21A 21B	PIN 0	POUT 0
22A 22B	PIN 1	POUT 1
23A 23B	PIN 2	POUT 2
24A 24B	PIN 3	POUT 3
25A 25B	PIN 4	POUT 4
26A 26B	PIN 5	POUT 5
27A 27B	PIN 6	POUT 6
28A 28B	PIN 7	POUT 7
29A 29B	ADDR01	
30A 30B	ADDR02	
31A 31B	ADDR03	
32A 32B	ADDR04	
33A 33B	ADDR05	
34A 34B	GND	GND
35A 35B	ADDR06	
36A 36B	ADDR07	
37A 37B	ADDR08	
38A 38B	ADDR09	
39A 39B	ADDR10	
40A 40B	ADDR11	

	A	B
41A 41B	GND	GND
42A 42B	ADDR12	
43A 43B	ADDR13	
44A 44B	ADDR14	
45A 45B	ADDR15	
46A 46B		
47A 47B	ADDR17	
48A 48B	ADDR18	
49A 49B	ADDR19	
50A 50B	ADDR20	
51A 51B	ADDR21	
52A 52B	SEN0	
53A 53B	SEN1	
54A 54B	SEN2	
55A 55B		
56A 56B		
57A 57B	GND	GND
58A 58B	DATA00	
59A 59B	DATA01	
60A 60B	DATA02	
61A 61B	DATA03	
62A 62B	DATA04	
63A 63B	DATA05	
64A 64B	GND	GND
65A 65B	DATA06	
66A 66B	DATA07	
67A 67B	DATA08	
68A 68B	DATA09	
69A 69B	DATA10	
70A 70B	DATA11	
71A 71B	DATA12	
72A 72B	DATA13	
73A 73B	DATA14	
74A 74B	DATA15	
75A 75B		
76A 76B	GND	GND
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

NT6X28AC

Product description

The NT6X28AC is a version of the NT6X28AA with changes to the card memory addressing. These modifications allow the NTCX50, NT6X28AC and NT6X69 to function correctly in the XPM Plus.

Like the NT6X28AA, the NT6X28AC extracts and inserts signaling information. This signaling information is for each of the 30 voice channels to and from the parallel speech buses. The parallel speech buses are part of the international digital trunk controller (IDTC). The signaling information uses channel time slot (CTS) 16. The CTS 0 communicates control and status information between the signal processor and the PCM30 interface card (NT6X27BB).

Location

The NT6X28AC plugs in the front of the shelf at slot position 19.

Functional description

Functional blocks

The NT6X28AC contains the following functional blocks:

- CTS 16 signaling receive interface
- FIFO interface
- CTS 16 signaling transmit interface
- CTS 0 PCM30 control and status register interface
- metering bit (MBIT) insertion
- speech bus interface
- miscellaneous timing and control logic
- processor interface

CTS 16 signaling receive interface

The system extracts signaling information from the PCM30 links during CTS 16 of the incoming parallel speech bus (SPIN 2-9). Each CTS 16 contains signaling information for two channels of the 16 ports. The system sends information for the 32 channels or two channels for each port during 16 frames. Each channel has 4 signaling bits: A, B, C and D.

The system uses two RAMs to store information for two channels separately. The NT6X28AC extracts signaling information for two channels at the same time from the speech bus. The NT6X28AC enables both RAMs together uses

the same address to perform this procedure. The NT6X28AC stores the ABCD values for the two channels in the same location on different RAMs.

Address bit 9 is used to select one of the two RAMs. This procedure occurs because the processor accesses signaling information for one channel at a time.

Two other RAMs store mask information. Mask information masks out bits for any channel that the software wants to scan. These RAMs are addressed like the receive RAMs. To mask out a specified bit, the system writes a 0 in to the correct location of the mask RAM.

The system updates the receive RAM with the new ABCD information if the receive FIFO is not full.

FIFO interface

The system generates the FIFO write if a mismatch occurs and the FIFO is not full. A new ABCD value and X-ored value are written in to the FIFO at the current pointer location. The X-ored value is latched in the receiver. This procedure occurs with a mismatch of the terminal identifier (TID). The FIFO contains five 256 x 4 RAMs. These RAMs are configured like a 17 x 16 FIFO. The system uses three data bits and the first 16 locations. Counters control the FIFO. One counter provides the write address and the other counter controls the read address. A MUX is used to select one of these counters. Each time a write is done, the write address increases by one. During processor access, two separate read instructions read the above information stored in each location. A word read accesses the TID. The TID is nine bits. Three of the FIFO devices store the TID. A byte read accesses the compare value and the X-ored value. The other two FIFO devices store these values. The two reads for each location are performed in the order that appears earlier in this document. After the second read (byte read), the read address increases. The read address and write address are compared. The present and the past values of these addresses to determine the FIFO full and empty status.

NT6X28AC (continued)

The processor accesses FIFO when the processor uses the following address:

1A3000

The information that the processor extracts has the following format:

BIT 876543210 BIT 7654 3210

(TID) (X-ored value) (ABCD value)

There are two status bits that form a FIFO status register (read only). The two bits are overflow (F) and Empty (E). These bits provide the following information to the processor:

FIFO status register

E	F	Condition
0	0	Queue is empty
1	0	Queue is not empty
1	1	Queue is full
Note: The status register (SR) has the address 1A4000.		

An interrupt status is provided to the processor at the beginning of every multiframe (1 MF = 16 frames = 125 µsec * 16 = 2 ms). This information is a flag for the processor to read the status register. When the processor reads the SR, the interrupt flag clears.

During initialization of the card, an access (read or write) to location 1A5000 occurs. This action resets the FIFO. When the address 1A5000 is decoded, the FIFO is reset if the FIFO is read or write. Access of this location sets the FIFO read and write counters to zero and sets the SR to an empty condition. This action makes sure that the processor does not read the FIFO until a valid entry is written in after initialization.

CTS 16 signaling transmit interface

The NT6X28AC uses this circuit to insert signaling information that the processor supplies. The processor supplies this signaling information into the outgoing parallel speech bus (SPOUT 2-9) during CTS 16. When the processor accesses the RAMs, address bit 9 is used to select one of the two RAMs. When the local counter addresses the RAMs, both RAMs are selected.

The NT6X28AC uses a buffer to interface the signaling information to the speech bus. The buffer is enabled during CTS 16. The speech enable signals

that the connection memory of the message interface card provides control the buffer.

CTS 0 PCM30 control and status register interface

The NT6X28AC uses this path to exchange control and status information between the processor and the PCM30 interface card. Control and status information include international signaling, loopback controls and maintenance commands. The system uses two RAMs for this purpose. The lower half of the RAMs stores command bytes. The upper half of the RAMs stores status bytes.

During CTS 0, the NT6X28AC extracts status bytes for all 16 ports from the incoming speech bus. The NT6X28AC inserts the command bytes in to the outgoing speech bus. Each CTS 0 contains control and status bytes for one register. Four registers are present for each port. There are 64 command bytes and 64 status bytes that correspond to the 16 ports. These locations are written again every four frames.

Metering bit insertion

During the PCM timeslots, the NT6X28AC uses bit 1 to give metering information on each subscriber timeslot. The processor uses the A bit to write the metering information to the signaling card. The card stores this information in a separate RAM. This information is read out of RAM. The system inserts this information in bit 1 of (0-9) of the outgoing speech bus in order.

Speech bus interface

The speech bus interface contains the logic required to access the speech bus at the correct time. The incoming bus is enabled during CTS 16 and CTS 0 with separate latched buffers. The system disables the incoming bus in loop-around mode and in RAM disable mode. The speech bus connection memory enable signal is used to enable the outgoing speech bus connection. This procedure occurs during CTS 0 and CTS 16.

Miscellaneous timing and control logic

Logic for timing and control includes the following:

- synchronized clock generation
- address generation
- gating and timing signals

NT6X28AC (continued)

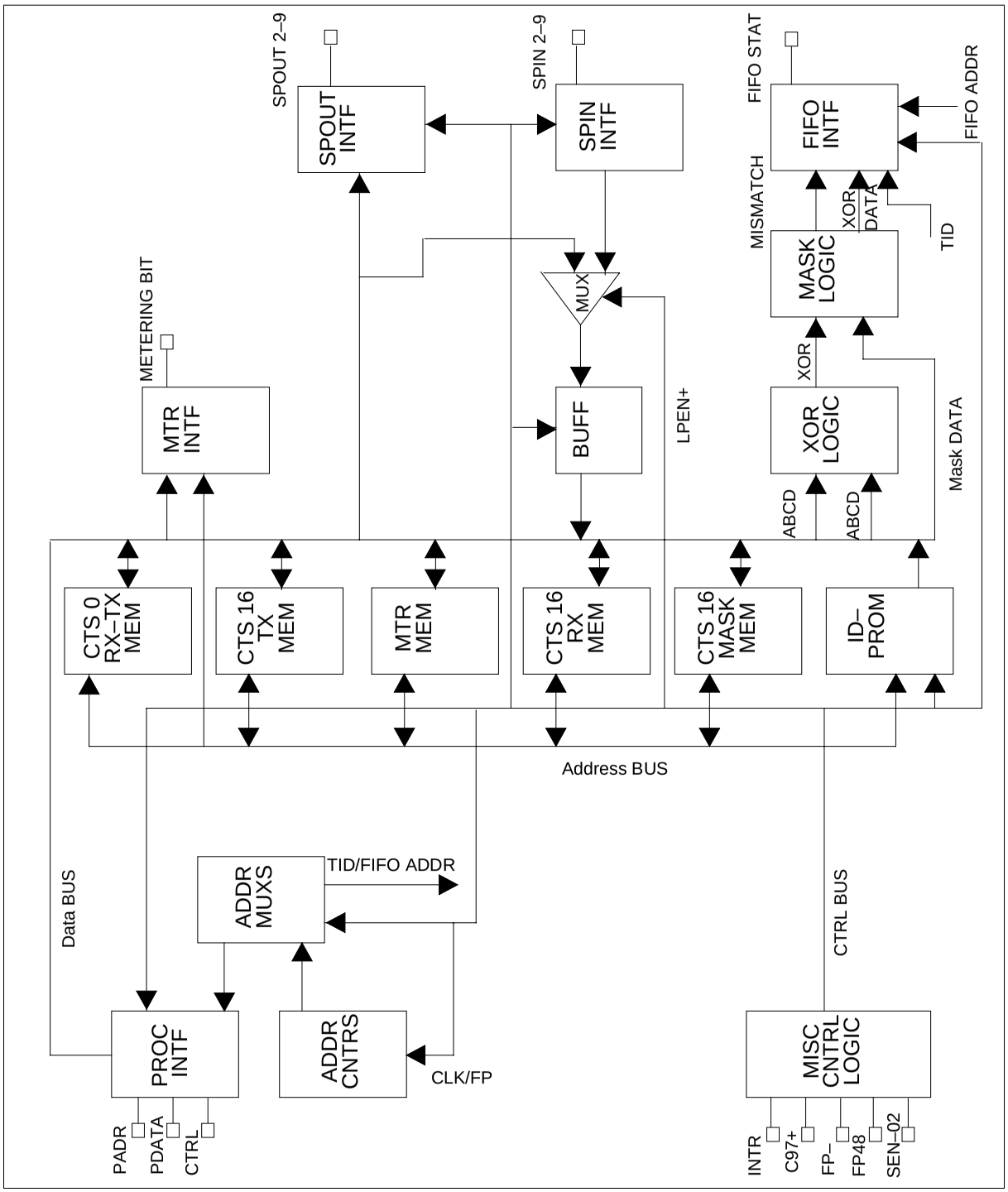
- counter that generates a 2 ms interrupt to the processor with use of superframe pulse 48 frames (FP48)
- card control register that uses 3 bits of the byte:
  - — least significant bit (bit 0) = loop-around, enable high
  - — bit 1 = interrupt disable, active high
  - — message (bit 2) = RAM disable, active low

Processor interface

The NT6X28AC interfaces to the XPM and XPM Plus backplane through a 160 pin connector (P1). A comparator selects the card when the processor generates the correct address. An inhibit signal does not allow the processor to access the card during CTS 0 and CTS 16. The system sends a data transfer acknowledge (DTACK) signal back to the processor to indicate successful access. The circuits contains a series of buffers for the different RAMs to access the processor data bus.

The relationship between the functional blocks appears in the following figure.

NT6X28AC simplified block diagram



NT6X28AC (continued)

Power requirements

The power requirements for the NT6X28AC appear in the following figure.

Power requirements

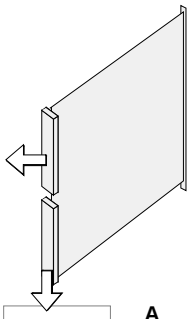
Parameter	Minimum	Nominal	Maximum
Supply voltage	4.75 V	5 V	5.25 V
Supply ripple			
Supply current		1.85 A	

Signaling

Pin numbers

The pin numbers for the NT6X28AC appear in the following figure.

NT6X28AC pin numbers



		A	B
1A	1B	GND	GND
2A	2B	PWR+5	PWR+5
3A	3B	PRW+5	PRW+5
4A	4B	PRW+5	PRW+5
5A	5B	GND	GND
6A	6B	FP-	C97+
7A	7B	GND	GND
8A	8B		
9A	9B		
10A	10B	FP 48–	FP 48
11A	11B	GND	GND
12A	12B	DAS–	
13A	13B	LDS–	
14A	14B	DTACK-	
15A	15B	UDS–	
16A	16B	WRT–	
17A	17B		
18A	18B		2MSINT-
19A	19B		
20A	20B		POUT 8
21A	21B	PIN 0	POUT 0
22A	22B	PIN 1	POUT 1
23A	23B	PIN 2	POUT 2
24A	24B	PIN 3	POUT 3
25A	25B	PIN 4	POUT 4
26A	26B	PIN 5	POUT 5
27A	27B	PIN 6	POUT 6
28A	28B	PIN 7	POUT 7
29A	29B	ADDR01	
30A	30B	ADDR02	
31A	31B	ADDR03	
32A	32B	ADDR04	
33A	33B	ADDR05	
34A	34B	GND	GND
35A	35B	ADDR06	
36A	36B	ADDR07	
37A	37B	ADDR08	
38A	38B	ADDR09	
39A	39B	ADDR10	
40A	40B	ADDR11	

		A	B
41A	41B	GND	GND
42A	42B	ADDR12	
43A	43B	ADDR13	
44A	44B	ADDR14	
45A	45B	ADDR15	
46A	46B	ADDR16	
47A	47B	ADDR17	
48A	48B	ADDR18	
49A	49B	ADDR19	
50A	50B	ADDR20	
51A	51B	ADDR21	
52A	52B	SEN0	
53A	53B	SEN1	
54A	54B	SEN2	
55A	55B		
56A	56B		
57A	57B	GND	GND
58A	58B	DATA00	
59A	59B	DATA01	
60A	60B	DATA02	
61A	61B	DATA03	
62A	62B	DATA04	
63A	63B	DATA05	
64A	64B	GND	
65A	65B	DATA06	
66A	66B	DATA07	
67A	67B	DATA08	
68A	68B	DATA09	
69A	69B	DATA10	
70A	70B	DATA11	
71A	71B	DATA12	
72A	72B	DATA13	
73A	73B	DATA14	
74A	74B	DATA15	
75A	75B		
76A	76B	GND	GND
77A	77B		
78A	78B	GND	GND
79A	79B		
80A	80B	GND	GND

NT6X29AA

Description

The NT6X29AA data modem extension frame (DME) houses analog 2400-baud modems. These modems modulate and demodulate serial binary data (in dibits) to and from phase shift keying (PSK). Phase shift keying is the method of modulation used to transmit serial binary data over analog channels. An alternating current (ac) modem is dedicated to each signaling terminal. The NT5X08AC ac modem shelf accommodates a maximum of 16 ac modem cards (A0302338). A maximum of three ac modem shelves are in any or all of the following positions of the NT6X29AA frame. The positions are 33, 52 and 66.

The DME frame is provisioned in conjunction with the NT6X09AA signaling terminal 6 extension (ST6E) frame.

Parts

The NT6X29AA contains the following parts:

- NT0X87AA–inverter unit
- NT0X88AB–miscellaneous frame equipment frame supervisory panel
- NT5X08AC–ac modem shelf

Inverter unit

The NT0X87AA inverter unit converts office battery to ac power for the cooling unit to use.

Miscellaneous frame equipment frame supervisory panel

The NT0X88AB miscellaneous frame equipment frame supervisory panel (FSP) receives feeder cables from the power distribution center (PDC) fuse. The FSP distributes dc power by local fuses to the shelves in the frame. The NT0X88AB receives the alarm battery supply (ABS) multiple feeder from the ABS fuse in the PDC. The NT0X88AB routes the ABS through internal fuses to the frame alarm circuits. The NT0X88AB FSP is at shelf position 45 in the frame.

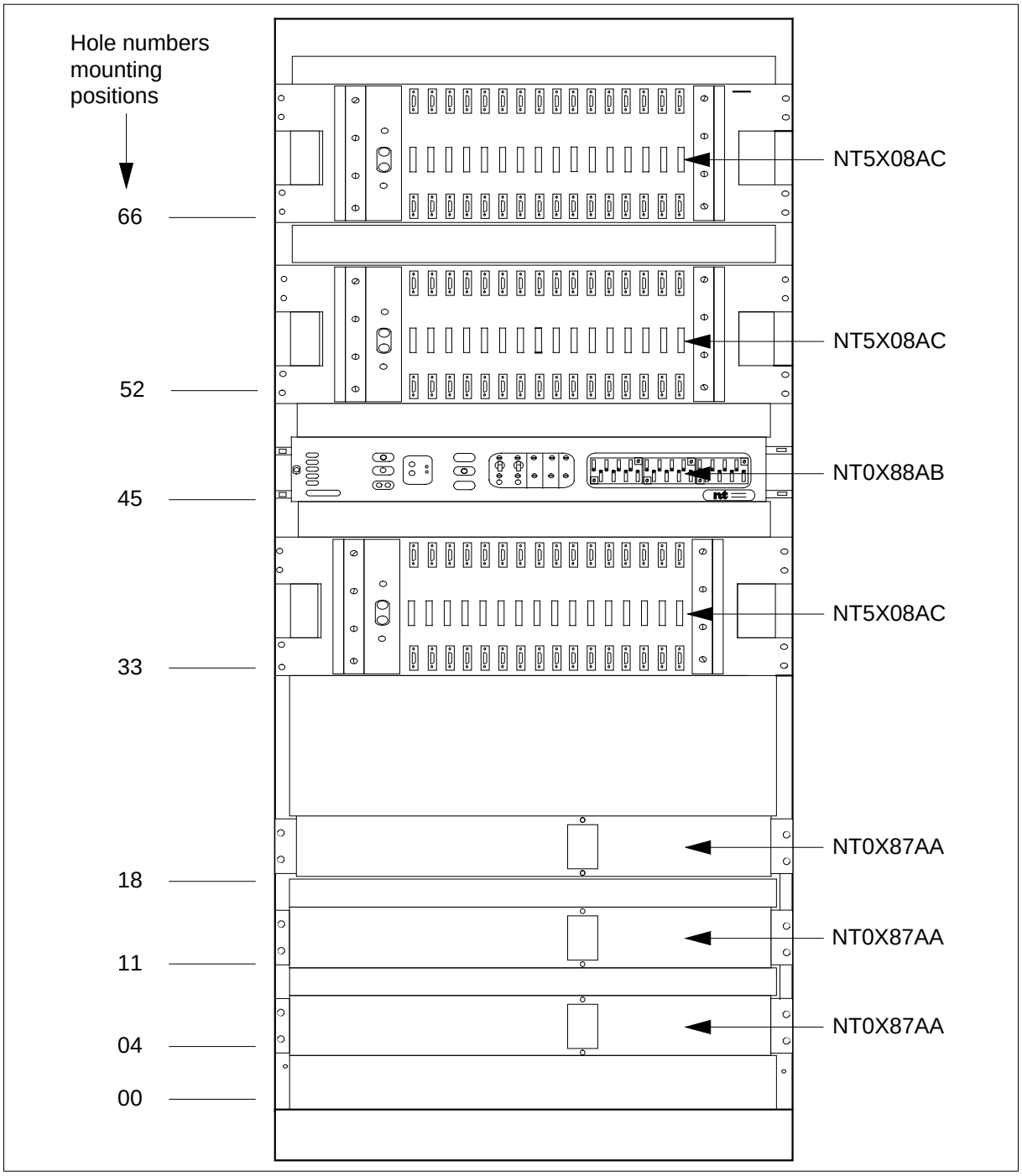
AC modem shelf

Each NT5X08AC ac modem shelf has a maximum of 16 ac modem cards (A0302338).

Design

The design of the NT6X29AA appears in the following figure.

NT6X29AA parts



Note: This diagram is not drawn to scale.

NT6X30

Product description

The NT6X30 contains the NT6X38 ringing control card and the NT6X37 ringing amplifier card. Ringing signals originate in the NT6X38. The NT6X37 amplifies the signals to the required output.

Functional description

The NT6X30 generates ringing signals and dc voltages for automatic number identification (ANI) and coin functions. The DIP switches or straps allow the frequencies and amplitudes of ringing waveform to be set. Frequencies and amplitudes are set to meet telephone company requirements.

Ringing control NT6X38

The NT6X38 performs the following functions:

- generates ringing signal
- provisions ANI and coin outputs
- monitors the ring bus output
- synchronizes dc-to-dc converters
- provisions auxiliary supply

Generating ringing signal

The waveform store PROM holds a digital model of a single cycle of each ringing waveform. The control logic selects the correct timing, frequency, and amplitude. The manual settings determine the selections. The output from the waveform store passes through the digital-to-analog converter and low-pass filter. This action provides the analog input signal for the ringing amplifier card.

Provisioning ANI and coin outputs

A single dc-to-dc converter provides *+48 V and +130 V outputs for ANI and coin functions.*

Monitoring ring bus outputs

The NT6X38 monitors the ring bus output from the NT6X37 for output voltage and current. If the NT6X38 detects overvoltage, the system sends a signal to the NT6X37 to shut down the amplifier. If the NT6X38 detects an ANI or coin overvoltage, the system shuts down the appropriate converter.

The monitor circuit provides transistor-transistor logic (TTL)-level status signals to the line concentrating module (LCM) processor. These signals indicate ringing voltage (RMS), ringing current (CUR) and low ANI or coin voltage. These signals combine with three status bits from the control logic and

travel through a serial data link. This group provides isolation of the ground reference.

Synchronizing dc-to-dc converters

The dc-to-dc converters in the NT6X37 must be synchronized to the LCM system clock. The converter requires 48 kHz synchronization, and the LCM provides 64 kHz, a phase-lock loop converts the frequency. The system provides dc isolation of the grounds between the LCM synchronization feed and the NT6X37 synchronization input.

Provisioning auxiliary supply

A small dc-to-dc converter supplies +15 V and +5 V for the internal circuits of NT6X38. The +15 V is for the control circuits on the NT6X37.

Ringing amplifier NT6X37

The NT6X37 amplifier is a dc-coupled class-B type. The NT6X37 amplifier uses power field-effect transistors (FET) as output devices. Two dc-to-dc converters power the amplifier. This condition allows a feedback signal from the ring bus output to control supply voltages. The feedback signal from the ring bus output controls the positive and negative supply voltages.

If ringing output is not present, the supply voltages are at a minimum of approximately +20 V. Under normal operation, the feedback from the ringing output causes the positive and negative supply voltages to increase alternately. This condition causes sufficient voltage to be available to produce the required output.

NT6X30AA

Product description

The NT6X30AA contains the NT6X38 ringing control card and the NT6X37 ringing amplifier card. The NT6X38 originates ringing signals and NT6X37 amplifies the signals to the required output level.

Functional description

The NT6X30AA generates ringing signals and dc voltages for automatic number identification (ANI) and coin functions. Frequencies and amplitudes of ringing waveform are set manually with dual in-line package (DIP) switches or straps. The settings meet the telephone company requirements.

Ringing control NT6X38

The NT6X38 performs the following functions:

- generation of ringing signal
- the ANI and coin outputs
- monitoring the ring bus output
- synchronization of dc-to-dc converters
- auxiliary supply

Generating ringing signal

The waveform store PROM holds a digital model of a single cycle of each ringing waveform. The control logic selects the correct timing, frequency, and amplitude. Manual settings determine the selections. The system passes the output from the waveform store through the digital-to-analog (D-to-A) converter and low-pass filter. This action provides the analog input signal for the ringing amplifier card.

Provisioning ANI and coin outputs

A single dc-to-dc converter provides +48V outputs and +130V outputs for ANI and coin functions.

Monitoring ring bus outputs

The NT6X38 monitors the ring bus output from the NT6X37 for output voltage and current. If the NT6X38 detects a ringing overvoltage, the system sends a signal to the NT6X37 to shut down the amplifier. If the NT6X38 detects an ANI or coin overvoltage, the system shuts down the converter that applies.

The monitor circuit also provides transistor-transistor logic (TTL)-level status signals to the line concentrating module (LCM) processor. These signals indicate ringing voltage (RMS), ringing current (CUR) and low ANI or coin

voltage. These signals combine with three status bits from the control logic. The system sends the signals through a serial data link to provide isolation of the ground reference.

Synchronizing dc-to-dc converters

The dc-to-dc converters in the NT6X37 must synchronize with the LCM system clock. The converter requires 48-kHz synchronization, and the LCM provides 64 kHz. A phase-lock loop converts the frequency. The system provides dc isolation of the grounds between the LCM synchronization feed and the NT6X37 synchronization input.

Provisioning auxiliary supply

A small dc-to-dc converter supplies +15 V and +5 V for the internal circuits of NT6X38. The +15 V is also for the control circuits on the NT6X37.

Ringing amplifier NT6X37

The NT6X37 amplifier is a dc-coupled class-B type. The NT6X37 uses power field-effect transistors (FET) as output devices. Two dc-to-dc converters power the amplifier. This condition allows a feedback signal from the ring bus output to control supply voltages. The signal from the ring bus output controls the positive and negative supply voltages.

If ringing output is not present, the supply voltages are at a minimum of approximately 20 V. Under normal operation, the feedback from the ringing output causes the positive and negative supply voltages to increase in alternate order. This condition causes enough voltage to be available to produce the required output.

NT6X30AA (continued)

Technical data

The following tables provide information about NT6X30AA ringing.

Ringing type applications that use NT6X30AA (Sheet 1 of 2)

Ring type	User	Switches	Table	Line
Coded ringing	Bell Canada U.S. Bell operating companies (BOC)			
• 20 Hz		1 to 4	"Coded ringing"	1, 5, 6, 7
• 30 Hz		1 to 4		2, 3, 4
Superimposed ringing	BOC (U.S.)			
• BCS15 or earlier		1 & 2 3 & 4	"Superimposed ringing"	1 2
• BCS16 and later (non-revertive)		1 & 2 3 & 4	"Superimposed ringing"	3 4
• BCS16 and later (revertive) (See Note 1)		1 & 2 3 & 4	"Superimposed ringing"	5 6
• BCS16 and later (revertive) (See Note 2)		1 & 2 3 & 4	"Superimposed ringing"	7 8
Superimposed ringing	Rural Electrification Administration (REA)			
• BCS16 and later (non-revertive) (See Note 3)			"Superimposed ringing"	11 12

Note 1: Do not change any DIP switch setting while power is ON. Set the correct circuit breaker on the NT6X35 FSP to OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.

Note 2: Release numbers: OE, OF, OG, OH, OJ, OK, OL, or ON. If a release number is not present, the card is release OE or earlier.

Note 3: Release numbers: OP through OZ, and AE or later.

Note 4: Release number: CC or later.

Ringing type applications that use NT6X30AA (Sheet 2 of 2)

Ring type	User	Switches	Table	Line
• BCS16 and later (revertive) (See 3)			"Superimposed ringing"	9 10
Frequency selective ringing				
• Synchromonic	BOC (U.S.)		"Synchromonic ringing (BOC)"	
• Harmonic	BOC (U.S.)		"Harmonic ringing (BOC)"	
• Decimonic	BOC (U.S.)		"Decimonic ringing (BOC)"	
• Synchromonic	REA		"Synchromonic ringing (REA)"	
• Harmonic	REA		"Harmonic ringing (REA)"	
• Decimonic	REA		"Decimonic ringing (REA)"	
	International	1 to 4	"International ringing"	
	Japan	1 to 4	"International ringing"	
	U.K.	1 to 4	"International ringing"	

Note 1: Do not change any DIP switch setting while power is ON. Set the correct circuit breaker on the NT6X35 FSP to OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.

Note 2: Release numbers: OE, OF, OG, OH, OJ, OK, OL, or ON. If a release number is not present, the card is release OE or earlier.

Note 3: Release numbers: OP through OZ, and AE or later.

Note 4: Release number: CC or later.

NT6X30AA (continued)

Coded ringing

Line	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
1	86 -52	20	2 2 1 1	1 to 4	00000000
2	95 -52	30	2 2 1 1	1 to 4	00010100
3	110 -52	30	2 2 1 1	1 to 4	01010100
4	120 -52	30	2 2 1 1	1 to 4	00110100
5	90 -52	20	2 2 1 1	1 to 4	00011000
6	105 -52	20	2 2 1 1	1 to 4	01011000
7	120 -52	20	2 2 1 1	1 to 4	00111000

Note: The symbols under the settings heading are 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

Superimposed ringing (Sheet 1 of 2)

Line	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
1	86 -38	20	2 2 1 1	1 & 2	01000000
2	86 +38	20	2 2 1 1	3 & 4	00100000
3	86 -38	20	2 2 1 1	1 & 2	00011110
4	86 +38	20	2 2 1 1	3 & 4	01011110
5	86 -38	20	2 2 1 1	1 & 2	10011110
6	86 +38	20	2 2 1 1	3 & 4	11011110
7	86 -52	20	1.84 1.84 1.84 0.48	1 & 2	10011110
8	86 +52	20	1.84 1.84 1.84 0.48	3 & 4	11011110
9	105 -52	20	1.84 1.84 1.84 0.48	1 & 2	11101100

Note: The symbols under the settings heading are 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

Superimposed ringing (Sheet 2 of 2)

Line	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
10	105 +52	20	1.84 1.84 1.84 0.48	3 & 4	11100010
11	105 -52	20	2 2 1 1	1 & 2	01101100
12	105 +52	20	2 2 1 1	3 & 4	01100010

Note: The symbols under the settings heading are 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

Synchromonic ringing (BOC) (Sheet 1 of 2)

	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
Low	90 -52	16	2 2 1 1	1	00010000
	90 -52	20	2 2 1 1	1	00011000
	95 -52	30	2 2 1 1	2	00010100
	100 -52	42	2 2 1 1	3	00000010
	110 -52	54	2 2 1 1	4	00001010
	125 -52	66	2 2 1 1	opt	00000110
Medium	105 -52	16	2 2 1 1	1	01010000
	105 -52	20	2 2 1 1	1	01011000
	110 -52	30	2 2 1 1	2	01010100
	115 -52	42	2 2 1 1	3	01000010
	125 -52	54	2 2 1 1	4	01001010
	140 -52	66	2 2 1 1	opt	01000110
High	120 -52	16	2 2 1 1	1	00110000

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

NT6X30AA (continued)

Synchromonic ringing (BOC) (Sheet 2 of 2)

	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
	120 -52	20	2 2 1 1	1	00111000
	120 -52	30	2 2 1 1	2	00110100
	130 -52	42	2 2 1 1	3	00100010
	140 -52	54	2 2 1 1	4	00101010
	155 -52	66	2 2 1 1	opt	00100110

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

Decimonic ringing (BOC) (Sheet 1 of 2)

	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
Low	90 -52	20	2 2 1 1	1	00011000
	95 -52	30	2 2 1 1	2	00010100
	100 -52	40	2 2 1 1	3	00011100
	110 -52	50	2 2 1 1	4	00010010
	125 -52	60	2 2 1 1	opt	00011010
Medium	105 -52	20	2 2 1 1	1	01011000
	110 -52	30	2 2 1 1	2	01010100
	115 -52	40	2 2 1 1	3	01011100
	125 -52	50	2 2 1 1	4	01010010
	140 -52	60	2 2 1 1	opt	01011010
High	120 -52	20	2 2 1 1	1	00111000

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

Decimonic ringing (BOC) (Sheet 2 of 2)

	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
	120 -52	30	2 2 1 1	2	00110100
	130 -52	40	2 2 1 1	3	00111100
	140 -52	50	2 2 1 1	4	00110010
	155 -52	60	2 2 1 1	opt	00111010

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

Synchromonic ringing (REA) (Sheet 1 of 2)

	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
Low	90 -52	16	1.95 1.35 1.35 1.35	1	10010000
	90 -52	20	1.95 1.35 1.35 1.35	1	10011000
	95 -52	30	1.95 1.35 1.35 1.35	2	10010100
	100 -52	42	1.95 1.35 1.35 1.35	3	10000010
	110 -52	54	1.95 1.35 1.35 1.35	4	10001010
	125 -52	66	1.95 1.35 1.35 1.35	opt	10000110
Medium	105 -52	16	1.95 1.35 1.35 1.35	1	11010000
	105 -52	20	1.95 1.35 1.35 1.35	1	11011000
	110 -52	30	1.95 1.35 1.35 1.35	2	11010100
	115 -52	42	1.95 1.35 1.35 1.35	3	11000010
	125 -52	54	1.95 1.35 1.35 1.35	4	11001010
	140 -52	66	1.95 1.35 1.35 1.35	opt	11000110

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

NT6X30AA (continued)

Synchromonic ringing (REA) (Sheet 2 of 2)

	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
High	120 -52	16	1.95 1.35 1.35 1.35	1	10110000
	120 -52	20	1.95 1.35 1.35 1.35	1	10111000
	120 -52	30	1.95 1.35 1.35 1.35	2	10110100
	130 -52	42	1.95 1.35 1.35 1.35	3	10100010
	140 -52	54	1.95 1.35 1.35 1.35	4	10101010
	155 -52	66	1.95 1.35 1.35 1.35	opt	10100110

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

Harmonic ringing (REA) (Sheet 1 of 2)

	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
Low	90 -52	16-2/3	1.95 1.35 1.35 1.35	1	10001000
	95 -52	25	1.95 1.35 1.35 1.35	2	10000100
	100 -52	33-1/3	1.95 1.35 1.35 1.35	3	10001100
	110 -52	50	1.95 1.35 1.35 1.35	4	10010010
	125 -52	66-2/3	1.95 1.35 1.35 1.35	opt	10010110
Medium	105 -52	16-2/3	1.95 1.35 1.35 1.35	1	11001000
	110 -52	25	1.95 1.35 1.35 1.35	2	11000100
	115 -52	33-1/3	1.95 1.35 1.35 1.35	3	11001100
	125 -52	50	1.95 1.35 1.35 1.35	4	11010010
	140 -52	66-2/3	1.95 1.35 1.35 1.35	opt	11010110

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

Harmonic ringing (REA) (Sheet 2 of 2)

	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
High	120 -52	16-2/3	1.95 1.35 1.35 1.35	1	10101000
	120 -52	25	1.95 1.35 1.35 1.35	2	10100100
	130 -52	33-1/3	1.95 1.35 1.35 1.35	3	10101100
	140 -52	50	1.95 1.35 1.35 1.35	4	10110010
	155 -52	66-2/3	1.95 1.35 1.35 1.35	opt	10110110

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

Decimonic ringing (REA) (Sheet 1 of 2)

	Voltage ac dc	Frequency (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
Low	90 -52	20	1.95 1.35 1.35 1.35	1	10011000
	95 -52	30	1.95 1.35 1.35 1.35	2	10010100
	100 -52	40	1.95 1.35 1.35 1.35	3	10011100
	110 -52	50	1.95 1.35 1.35 1.35	4	10010010
	125 -52	60	1.95 1.35 1.35 1.35	opt	10011010
Medium	105 -52	20	1.95 1.35 1.35 1.35	1	11011000
	110 -52	30	1.95 1.35 1.35 1.35	2	11010100
	115 -52	40	1.95 1.35 1.35 1.35	3	11011100
	125 -52	50	1.95 1.35 1.35 1.35	4	11010010
	140 -52	60	1.95 1.35 1.35 1.35	opt	11011010
High	120 -52	20	1.95 1.35 1.35 1.35	1	10111000

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

NT6X30AA (continued)

Decimonic ringing (REA) (Sheet 2 of 2)

	Voltage ac dc	Frequency (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
	120 -52	30	1.95 1.35 1.35 1.35	2	10110100
	130 -52	40	1.95 1.35 1.35 1.35	3	10111100
	140 -52	50	1.95 1.35 1.35 1.35	4	10110010
	155 -52	60	1.95 1.35 1.35 1.35	opt	10111010

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

International ringing

	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
Low	67 -52	25	1.95 1.35 1.35 1.35	1 to 4	10001110
Medium	75 -52	25	1.95 1.35 1.35 1.35	1 to 4	11001110
High	82 -52	25	1.95 1.35 1.35 1.35	1 to 4	10101110
Low	67 -52	25	2 2 1 1	1 to 4	00001110
Medium	75 -52	25	2 2 1 1	1 to 4	01001110
High	82 -52	25	2 2 1 1	1 to 4	00101110
Japan	75 0	16	2 2 1 1	1 to 4	11101110
U.K.	75 -52	25	1 1 0.4 0.6	1 to 4	01101110

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

Harmonic ringing (BOC)

	Voltage ac dc	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
Low	90 -52	16-2/3	2 2 1 1	1	00001000
	95 -52	25	2 2 1 1	2	00000100
	100 -52	33-1/3	2 2 1 1	3	00001100
	110 -52	50	2 2 1 1	4	00010010
	125 -52	66-2/3	2 2 1 1	opt	00010110
Medium	105 -52	16-2/3	2 2 1 1	1	01001000
	110 -52	25	2 2 1 1	2	01000100
	115 -52	33-1/3	2 2 1 1	3	01001100
	125 -52	50	2 2 1 1	4	01010010
	140 -52	66-2/3	2 2 1 1	opt	01010110
High	120 -52	16-2/3	2 2 1 1	1	00101000
	120 -52	25	2 2 1 1	2	00100100
	130 -52	33-1/3	2 2 1 1	3	00101100
	140 -52	50	2 2 1 1	4	00110010
	155 -52	66-2/3	2 2 1 1	opt	00110110

Note: The symbols under the settings heading are 0 = ON, 1 = OFF, X opt = the specified setting can be for any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

The following tables provide information about NT6X30AA tolerances.

The NT6X30AA Frequency and dc voltage tolerances (Sheet 1 of 2)

Frequency/dc voltage	Tolerances
16 to 33-1/3 Hz	±1/3 Hz
40 to 66-2/3 Hz	±1%
25 Hz international	±1/3 Hz

NT6X30AA (continued)

The NT6X30AA Frequency and dc voltage tolerances (Sheet 2 of 2)

Frequency/dc voltage	Tolerances
-52V dc	-49.75 to -52.5V dc
-38V dc	±2V dc
+ 38V dc	±2V dc

The NT6X30AA ac voltage tolerances

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8
100	97	103
105	101.9	108.1
110	106.7	113.3
115	111.6	118.4
120	116.4	123.6
125	121.2	128.7
130	126.1	133.9
140	135.8	144.2
155	150.3	159.6

The following table provides information about ANI and coin voltages.

The NT6X30AA ANI and coin voltages

Output	Limits
+48 V	+52, ±2.5 V
-48 V	-52, ±5 V
+130 V	+130, ±5 V
-130 V	-130, ±5 V

Power requirements

The NT6X30AA requires -42 V to -56 V, and nominally 3.5 A, to a maximum of 5 A. The NT6X30AA consumes 180 W of power.

NT6X30AE

Product description

The NT6X30AE contains the NT6X38 card for ringing control and the NT6X37 card for ringing amplification. The NT6X38 originates ringing signals. The NT6X37 amplifies the signals to the required output level.

The NT6X30AE operates with the NT6X35 power control circuit frame supervisory panel (FSP) in the DMS-100 line concentrating module (LCM) for application in Australia.

Functional description

The NT6X30AE generates ringing signals and dc voltages for automatic number identification (ANI) and coin functions. Dual in-line package (DIP) switches or straps are used to set the frequency and amplitude of ringing waveforms manually. Frequency and amplitude are set to meet telephone operating company requirements.

The NT6X30AE contains two printed circuit cards. The cards are the NT6X38AE for ringing control and the NT6X37AA for ringing amplification. The NT6X38AE originates ringing signals. The NT6X37AA amplifies the signals to the required output level.

Ringing control

The NT6X38 performs the following functions:

- generation of ringing signal
- provision of ANI and coin outputs
- monitoring of ring bus output
- synchronization of dc-to-dc converters
- auxiliary supply

Generating ringing signal

The waveform store PROM holds a digital model of a single cycle of each ringing waveform. The control logic selects the correct timing, frequency, and amplitude. The manual settings determine the selections. The system passes the output from the waveform store through the digital-to-analog converter and the low-pass filter. This action provides the analog input signal for the ringing amplifier card.

Provisioning ANI and coin outputs

A single dc-to-dc converter provides ±52V output for ANI functions and ±130V output for coin functions.

Monitoring ring bus output

The NT6X38AE monitors ring bus output from the NT6X37AA for output voltage and current. If the NT6X39AE detects a ringing overvoltage, the system sends a signal to the NT6X37AA to shut down the amplifier. If the NT6X39AE detects an ANI or coin overvoltage, the system shuts down the correct converter. If both types of overvoltage occur, the FSP disconnects primary power.

The monitor circuit also provides transistor-transistor logic (TTL)-level status signals to the LCM processor. These signal indicate ringing voltage (RMS), ringing current (CUR), and low ANI or coin voltage (ACT). These signals combine with three status bits from the control logic. These status bits are AFO, AF1, and XOVER. The system sends the signals through a serial data link to provide isolation of the ground reference.

Synchronizing dc-to-dc converters

The dc-to-dc converters in the NT6X37AA must synchronize with the LCM system clock. The converter requires 48-kHz synchronization, and the LCM provides 64-kHz synchronization. A phase-lock loop converts the frequency. The dc isolation of the grounds occurs between the LCM synchronization feed and the NT6X37AA synchronization input.

Provisioning auxiliary supply

A small dc-to-dc converter supplies ±15 V and 5 V for the internal circuits of the NT6X38AE. The ±15 V is also for the control circuits on the NT6X37AA.

Ringing amplification

The NT6X37 amplifier is a dc-coupled class-B type, which uses power field effect transistors (FET) as output devices. Two dc-to-dc converters power the amplifier. This condition allows a feedback signal from the ring bus output to control the supply voltages. The feedback signal from the ring bus output controls positive and negative supply voltages.

If ringing output is not present, the supply voltages are at a minimum of approximately ±20 V. Under normal operation, the feedback from the ringing output causes the positive and negative supply voltages to increase in alternate order. This action causes sufficient available voltage to produce the required output.

NT6X30AE (continued)

Signaling

Pin numbers

The following table provides pin number information for the NT6X30AE finger connector (P3).

The NT6X30AE pin number

Pin	Signal	Pin	Signal
1	AF0	19	-48 V
2	LOGIC GND	20	BR
3	AF1	21	ABS-48
4	LOGIC GND	22	FSPMON
5	ACT	23	LOGIC GND
6	LOGIC GND	24	SYNC 64
7	XOVER	25	RRING
8	LOGIC GND	26	RTIP
9	RMS	27	RRING
10	LOGIC GND	28	RTIP
11	CUR	29	-52 V
12	LOGIC GND	30	ABS BR
13	LOGIC GND	31	
14	FSPLINK	32	+52 V
15	-48 V	33	
16	BR	34	-130 V
17	-48 V	35	
18	BR	36	+130 V

Technical data

The following tables contain information on voltages.

International

Voltage ac dc offset	Frequency (Hz)	Cadence (s)	Switch (SW1-4)	Setting 12345678
90 -52	25	1.00 1.00 0.40 0.60	1 to 4	0111111X
Note: The symbols under the settings heading are: 0=ON, 1=OFF, X=ON or OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.				

The NT6X30AE frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
25 Hz international	±;0.33 Hz
-52V dc	-49.75 to -52.5V dc

Ac voltage tolerances

Nominal	Low	High
90	88	92

The NT6X30AE ANI/coin voltages

Output	Limits
+48 V	+52 V ±2.5 V
-48 V	-52 V ±5 V
+130 V	+130 V ±5 V
-130 V	-130 V ±5 V

Power requirements

The NT6X30AE requires -42 V to -56 V, and nominally 3.5 A to a maximum of 4 A. The NT6X30AE uses a maximum of 208 W of power.

NT6X30BA

Product description

The NT6X30BA ringing generator for Japan contains two cards. These cards are the NT6X38BA ringing control and the NT6X37CA ringing amplifier. The NT6X38BA originates the ringing signals. The NT6X37CA amplifies the signals to the required output level.

Location

The NT6X30BA that fits in the NT6X35AA frame supervisory panel (FSP) is part of the line concentrating module (LCM) cabinet.

Functional description

The NT6X30BA generates ringing signals. Use dual inline package (DIP) switches or straps to set the frequencies and amplitudes of ringing waveforms manually. For Japan, the output ringing waveform is 76V ringing voltage (RMS) at 16 Hz. The output ringing waveform, placed over the input battery voltage, is externally fused.

NT6X38BA ringing control

The NT6X38BA performs the following functions:

- ringing signal generation
- ring bus output monitoring
- auxiliary power supply

Generating ringing signal

The waveform store PROM holds a digital image of one cycle of each ringing waveform. According to the manual settings, the control logic selects the correct timing, frequency and amplitude. The output from the waveform store transfers through the digital-to-analog (D-to-A) converter. The output transfers through the low-pass filter to provide the analog input signal for the ringing amplifier card.

Monitoring ring bus output

The NT6X38BA monitors the ring bus output from the NT6X37CA for output voltage and current. If a ringing overvoltage is present, the NT6X38BA sends a signal to the NT6X37CA to shut down the amplifier.

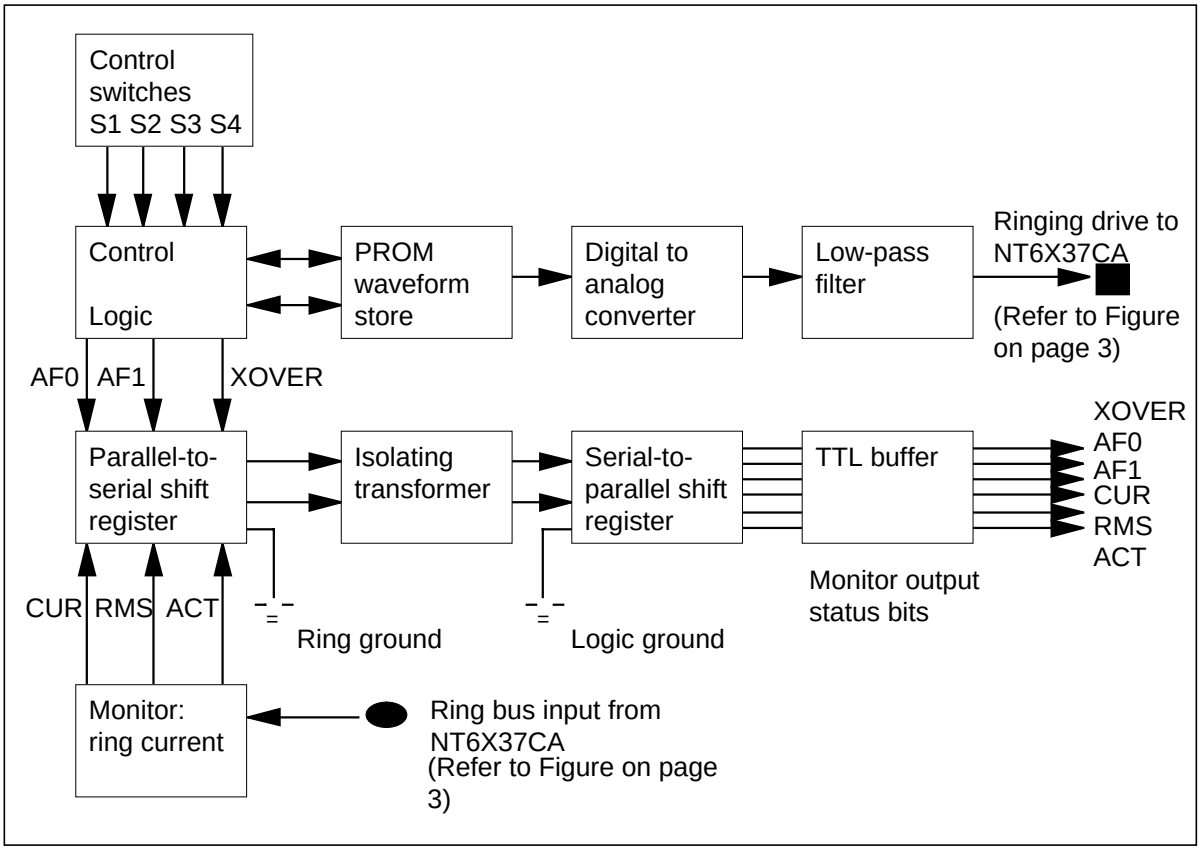
The monitor circuit provides transistor-to-transistor logic (TTL)-level status signals to the LCM processor. The status signals indicate RMS and ringing current (CUR). The status signals combine with three status bits from the control logic. The signals and bits are through a serial data link to isolate the ground reference.

Auxiliary power supply

A small dc-to-dc converter supplies *plusmn;15V and 5V for the internal circuits of the NT6X38BA. You use the +15V for the control circuits on the NT6X37CA.

The relationship with the components of the NT6X38BA appear in the following figure.

NT6X38BA Ringing control block diagram



Ringing amplifier NT6X37CA

The NT6X37CA is a dc-coupled class-B type ringing amplifier that uses power field-effect transistors (FET) as the output devices. Two dc-to-dc converters power the amplifier. These converters allow a feedback signal from the ring bus output to independently control the positive and negative supply voltages.

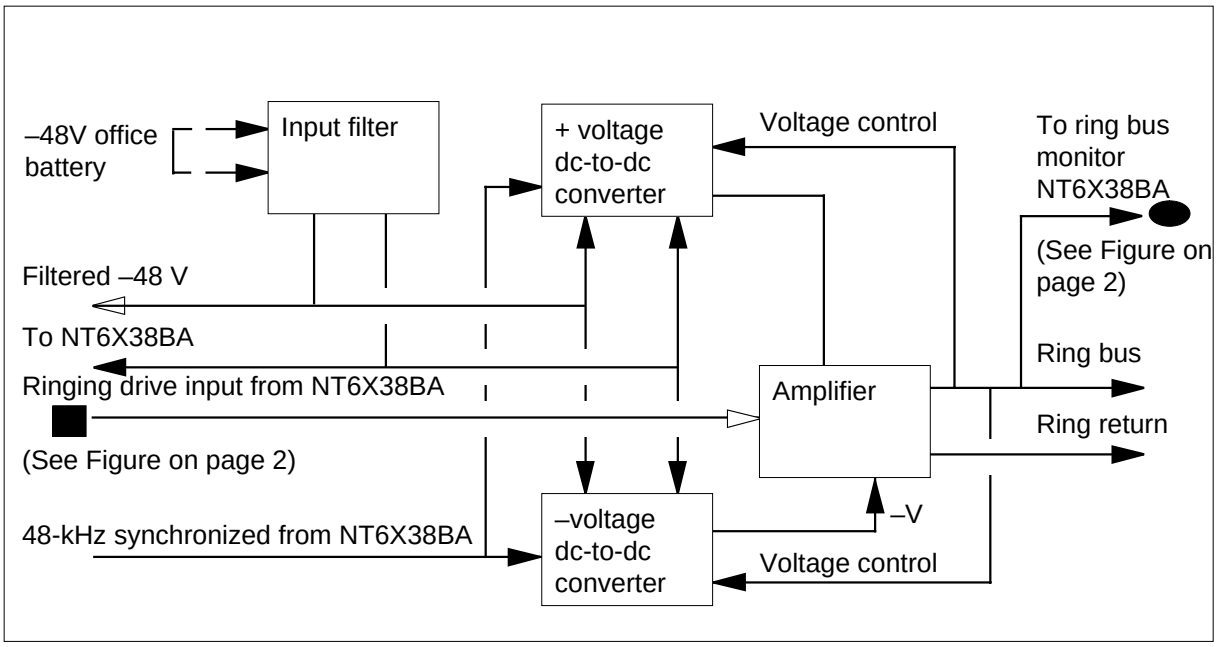
Without a ringing output, the supply voltages are at minimum. The minimum is approximately 20V. Under normal operation, the feedback from the ringing output causes the positive and negative supply voltages to alternately increase.

NT6X30BA (continued)

This action occurs so that enough voltage is available to produce the required output.

The relationship between the parts of the NT6X37CA appears in the following figure.

NT6X37CA Ringing amplifier block diagram



Signaling

Pin numbers

The pin numbers for the NT6X30BA appear in the following table.

NT6X30BA pin number (Sheet 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	AF0	1	LOGICGND	19	-48V	28	RTIP
2	LOGICGND	11	CUR	20	BR	29	-52V(N/C ON BA)
3	AF1	12	LOGICGND	21	ABS-48	30	ABSBR
4	LOGICGND	13	LOGICGND	22	FSPMON	31	N/C
5	ACT	14	FSPLINK	23	LOGICGND	32	+52V(N/C ON BA)
6	LOGICGND	15	-48V	24	SYNC64	33	N/C

NT6X30BA pin number (Sheet 2 of 2)

Pin Signal	Pin Signal	Pin Signal	Pin Signal
7 XOVER	16 BR	25 RRING	34 -130V(N/C ON BA)
8 LOGICGND	17 -48V	26 RTIP	35 N/C
9 RMS	18 BR	27 RRING	36 +130V(N/C ON BA)

Technical data

Power requirements

The NT6X30BA requires 42V to 56V and a nominal current of 3.5A, to a maximum of 5A. The card consumes 180W of power.

NT6X30BB

Product description

The NT6X30BB ringing generator is a horizontal mount version of the ringing generator for the Japanese market. The contains one card that provides required functionality. Two cards in the NT6X30BA provide required functionality. The is backwards compatible with the NT6X30BA.

Location

The NT6X30BB fits in the NT6X35AA frame supervisory panel (FSP). The FSP is part of the line concentrating equipment (LCE) frame.

Functional description

The NT6X30BB generates ringing signal voltages. Use the four dual inline package (DIP) switches during installation to set the ring output frequency and amplitude manually. Use the four dual inline package (DIP) switches during installation to meet Japanese requirements,

Functional blocks

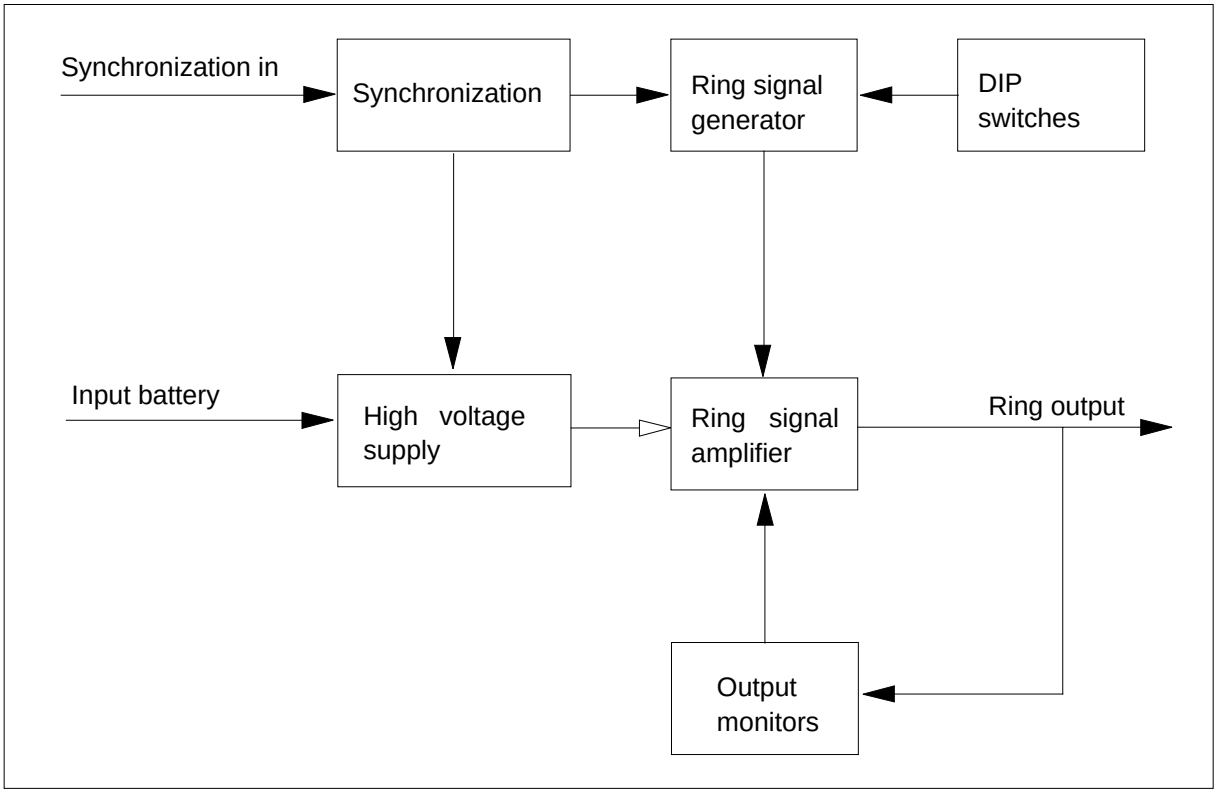
The ringing signal is ground backed. Ground backed means that the ringing is centered about ground. The input battery, through a fuse, provides the dc-offset for this market. Apply the output battery to the tip side of the bus.

The NT6X30BB has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X30BB functional blocks



High voltage supply

The raw battery input voltage (-48V) is filtered and fed to a single-transistor isolated boost converter topology. These actions switch the input voltage to a square wave across the primary of a flyback transformer. The primary is where the secondary is rectified and filtered to produce a regulated floating 300V supply. An isolated output produces the voltages required to power the ringing control and monitor circuits.

Ring signal generator

A digital image of the ringing waveform is in the programmable read-only memory (PROM) of the microcontroller of the card. The microcontroller responds to the DIP switch settings on the card. This response sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. This information produces a low voltage sinusoidal waveform of the right frequency and reference amplitude. This information includes dc offset to the ring signal amplifier. The microcontroller provides additional information, like zero-crossing detect (XOVER) and subcycle cadence information AF0 and AF1.

NT6X30BB (continued)

Ring signal amplifier

The ringing signal from the ring signal generator is fed to a class D amplifier circuit. The circuit modulates the pulse width to a full bridge switch configuration. This configuration switches the high voltage floating supply alternately to ground on one side for each half cycle of the output waveform. This action creates a train of different width pulses. When the width pulses are filtered, these pulses produce the required sinusoidal ringing output voltage and dc-offset. The voltage and dc-offset are fed from the ring generator. To regulate this output, compare a sample of the filtered output to the input reference signal from the ring signal generator circuit.

Output monitors

The ringing output and dc-offset are monitored for ac overvoltage and undervoltage. In an undervoltage condition, the current must be less than the current limit point to allow shutdown.

The monitor circuits provide electrically isolated transistor-to-transistor logic (TTL) level signals to the (LCM) processor. These signals indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the LCM synchronizes the dc-dc converters and the ringing amplifier on this card. The integer multiple is 8 kHz. This synchronization is electrically isolated from the clock signal that the LCM provides. The synchronization is isolated between the different converters on this card.

Signaling

Pin numbers

The pin numbers for the NT6X30BB appear in the following tables.

Pin numbers for the P1 Connector (Sheet 1 of 2)

1 AF0	10 LOGICGND	19 -48V	28 RTIP
2 LOGICGND	11 CUR	20 BR	29 (N/C)
3 AF1	12 LOGICGND	21 ABS-48	30 ABSBR
4 LOGICGND	13 LOGICGND	22 FSPMON	31 N/C
5 ACT	14 FSPLINK	23 LOGICGND	32 (N/C)
6 LOGICGND	15 -48V	24 SYNC64	33 N/C
7 XOVER	16 BR	25 RRING	34 (N/C)

Pin numbers for the P1 Connector (Sheet 2 of 2)

8 LOGICGND	17 -48V	26 RTIP	35 Fuse Alarm
9 RMS	18 BR	27 RRING	36 (N/C)

Technical data

The card has an output of 16 Hz, with an amplitude of 76 V (rms). The correct setting of the DIP switches is 11101110.

The following table indicates the ringing characteristics and DIP switch setting for the NT6X30BB.

Japan ringing characteristics and switch setting

Voltage AC DC offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
76 0	16	2 2 1 1	1 to 4	11101110
Note: Interpret the symbols under the heading as 0=ON, 1=OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.				

The information about voltages appears in the following tables.

Japan frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
16 Hz	+ or - 1 Hz
0V (dc)	+ or - 2V (dc)
-48V (dc)	+ or - 2V (dc)

Japan ac voltage tolerances

Nominal	Low	High
76	69	83

Power requirements

The NT6X30BB requires -39.5V to -75V, and a nominal current of 1 A, to a maximum of 2 A. The card consumes 75 W of power.

NT6X30CA

Product description

The NT6X30CA ringing generator is a horizontal mount version of the ringing generator for the North American market. The NT6X30CA contains one card that provides the required functionality. The NT6X30AA ringing generator requires two cards to provide all functionality. The NT6X30CA is backwards compatible with the NT6X30AA.

Location

The NT6X30CA fits in the NT6X35AA frame supervisory panel (FSP) in the line concentrating equipment (LCE) frame. The fits in the NTB37AB FSP integrated services digital network line concentrating equipment (LCEI).

Functional description

The NT6X30CA generates ringing signals and the dc voltages that the automatic number identification (ANI) and coin functions require. Use the four dual inline package (DIP) switches during installation to set the ring output frequency and amplitude manually. Use the DIP switches during installation to meet North American requirements.

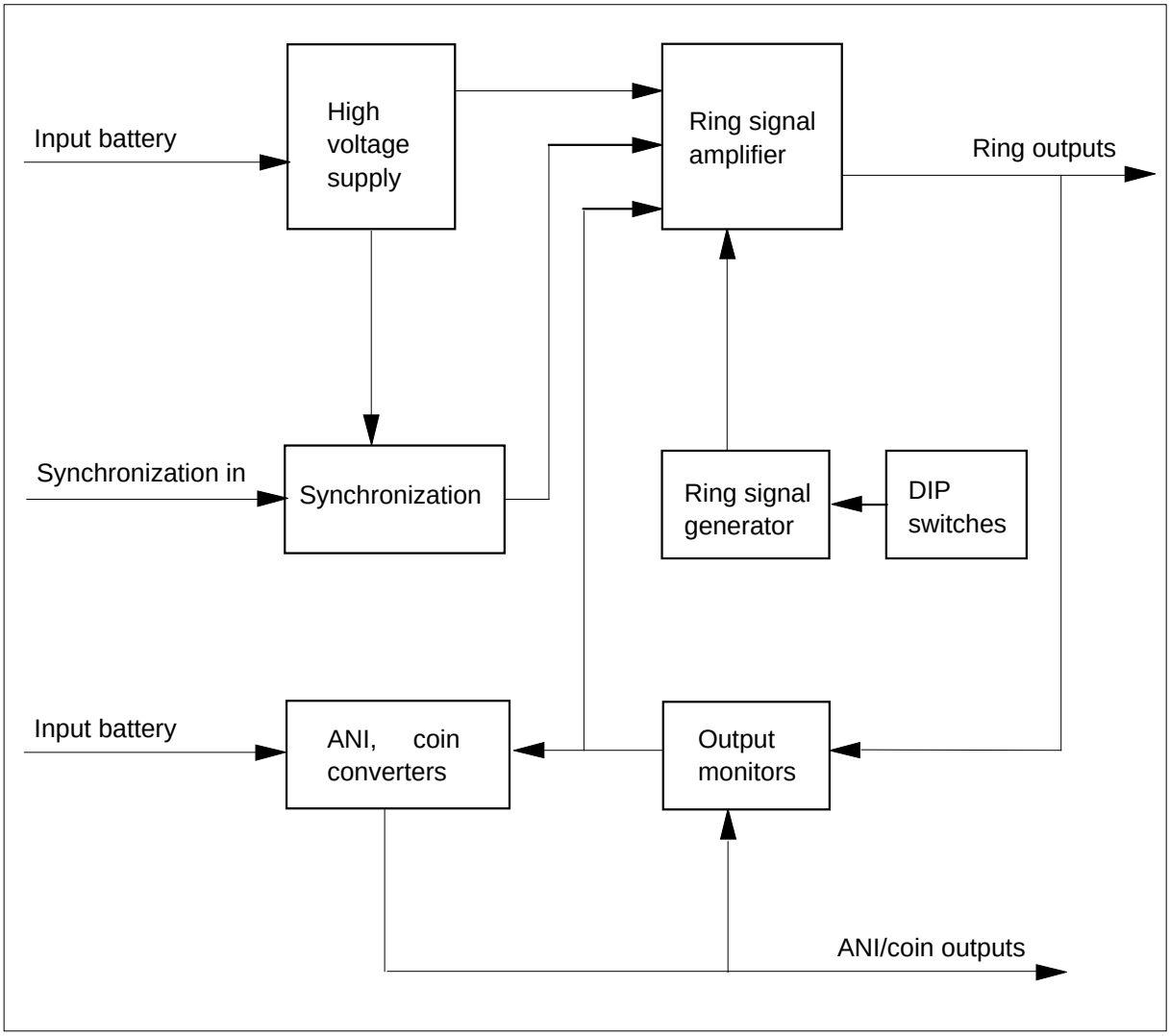
Functional blocks

The NT6X30CA has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- ANI, coin converters
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X30CA functional blocks



High voltage supply

The raw battery input voltage, -48V, is filtered and fed to a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of the flyback transformer. The secondary of the flyback transformer is rectified and filtered to produce a regulated floating 300 V supply. An isolated output that produces the voltages required to power the ringing control and monitor circuits is available.

NT6X30CA (continued)

Ring signal generator

A digital image of the ringing waveform is in the programmable read-only memory (PROM) of the micro controller of the card. The micro controller responds to the DIP switch settings on the card to send the correct stream of digital information. The micro controllers sends the digital information to the digital-to-analog converter (DAC) circuit. The DAC circuit produces a low voltage sinuosity waveform of the right frequency and reference amplitude. This waveform includes dc-offset to the ring signal amplifier. The micro controller provides additional information, like zero-crossing detect (XOVER) and subcycle cadence information (AF0 and AF1).

Ring signal amplifier

The ringing signal from the ring signal generator is fed to a class D amplifier circuit. The circuit modulates the pulse width to a full bridge switch configuration. This configuration switches the high voltage floating supply alternately to ground on one side for each half cycle of the output waveform. This action creates a train of different width pulses. When filtered, these pulses produce the required sinusoidal ringing output voltage and dc-offset. The voltage and dc-offset are fed from the ring generator. To regulate this output, compare a sample of the filtered output to the input reference signal from the ring signal generator circuit.

ANI, coin converters

Two separate single-transistor isolated flyback converters provide the dc outputs. The dc outputs are required for the ANI feature (one converter) and the coin feature (the other converter). Linear post-regulator regulates these outputs.

Output monitors

The ringing output and dc-offset are monitored for ac overvoltage and low voltage. In a low voltage condition, the current must be less than the current limit point to allow shutdown.

Monitor the ANI/Coin outputs for overvoltage and low voltage conditions. If an overvoltage condition is present, the system disables the correct converter. If an low voltage condition is present, the system raises an alarm. The card does not shut down unless the ringing output is low.

The monitor circuits provide electrically isolated transistor-transistor logic (TTL) level signals to the LCM processor. These signals indicate low ringing voltage (RMS-bit), excess ringing output current (CUR-bit), and ANI/Coin status (ACT-bit).

Synchronization

A phase-lock loop to the clock frequency of the LCM synchronizes the dc-dc converters and the ringing amplifier on this card. The integer multiple is 8 kHz. This synchronization is electrically isolated from the clock signal from the LCM and between the different converters on this card.

Technical data

Information about ringing appears in the following tables.

Ringing type applications that use NT6X30CA (Sheet 1 of 2)

Ring type	User	Switches	Table	Line
Coded ringing	Bell Canada U.S. Bell operating companies (BOC)			
• 20 Hz		1-4	"NT6X30CA coded ringing"	1, 4, 5, 6
• 30 Hz		1-4		2, 3, 4
Superimposed ringing	BOC (U.S.)			
• BCS15 or earlier		1 & 2 3 & 4	"NT6X30CA superimposed ringing"	1 2
• BCS16 and later (non-revertive)		1 & 2 3 & 4	"NT6X30CA superimposed ringing"	3 4
• BCS16 and later (revertive)		1 & 2 3 & 4	"NT6X30CA superimposed ringing"	5 6
Superimposed ringing	Rural Electrification Administration (REA)			
• BCS16 and later (non-revertive)		1 & 2 3 & 4	"NT6X30CA superimposed ringing"	9 10

Note: Do not change DIP switch setting while power is ON. Set the correct circuit breaker on the NT6S35 FSP to OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.

NT6X30CA (continued)

Ringing type applications that use NT6X30CA (Sheet 2 of 2)

Ring type	User	Switches	Table	Line
• BCS16 and later (revertive)		1 & 2 3 & 4	"NT6X30CA superimposed ringing"	7 8
Frequency selective ringing				
• Synchromonic	BOC (U.S.)		"NT6X30CA synchromonic ringing (BOC)"	
• Harmonic	BOC (U.S.)		"NT6X30CA harmonic ringing (BOC)"	
• Decimonic	BOC (U.S.)		"NT6X30CA decimonic ringing (BOC)"	
• Synchromonic	REA		"NT6X30CA synchromonic ringing (REA)"	
• Harmonic	REA		"NT6X30CA harmonic ringing (REA)"	
• Decimonic	REA		"NT6X30CA decimonic ringing (REA)"	
	International	1-4	"NT6X30CA international ringing"	
	Japan	1-4	"NT6X30CA international ringing"	
	U.K.	1-4	"NT6X30CA international ringing"	

Note: Do not change DIP switch setting while power is ON. Set the correct circuit breaker on the NT6S35 FSP to OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.

NT6X30CA coded ringing

Line	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
1	86	-52	20	2 2 1 1	1 to 4	00000000
2	110	-52	30	2 2 1 1	1 to 4	01010100
3	120	-52	30	2 2 1 1	1 to 4	00110100
4	90	-52	20	2 2 1 1	1 to 4	00011000
5	105	-52	20	2 2 1 1	1 to 4	01011000
6	120	-52	20	2 2 1 1	1 to 4	00111000

Note: Interpret the symbols under the heading settings as 0=ON, 1=OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. SW1a and SW4s not in use must have all eight sections set to OFF.

NT6X30CA superimposed ringing

Line	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
1	86	-38	20	2 2 1 1	1 & 2	01000000
2	86	+38	20	2 2 1 1	3 & 4	00100000
3	86	-38	20	2 2 1 1	1 & 2	00011110
4	86	+38	20	2 2 1 1	3 & 4	01011110
5	86	-52	20	1.84 1.84 1.84 0.48	1 & 2	10011110
6	86	+52	20	1.84 1.84 1.84 0.48	3 & 4	11011110
7	105	-52	20	1.84 1.84 1.84 0.48	1 & 2	11101100
8	105	+52	20	1.84 1.84 1.84 0.48	3 & 4	11100010
9	105	-52	20	2 2 1 1	1 & 2	01101100
10	105	+52	20	2 2 1 1	3 & 4	01100010

Note: Interpret the symbols under the heading settings as 0=ON, 1=OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. SW1a and SW4s not in use must have all eight sections set to OFF.

NT6X30CA (continued)

NT6X30CA synchromonic ringing (BOC)

Line	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	16	2 2 1 1	1	00010000
	90	-52	20	2 2 1 1	1	00011000
	95	-52	30	2 2 1 1	2	00010100
	100	-52	42	2 2 1 1	3	00000010
	110	-52	54	2 2 1 1	4	00001010
	125	-52	66	2 2 1 1	opt	00000110
Medium	105	-52	16	2 2 1 1	1	01010000
	105	-52	20	2 2 1 1	1	01011000
	110	-52	30	2 2 1 1	2	01010100
	115	-52	42	2 2 1 1	3	01000010
	125	-52	54	2 2 1 1	4	01001010
	140	-52	66	2 2 1 1	opt	01000110
High	120	-52	16	2 2 1 1	1	00110000
	120	-52	20	2 2 1 1	1	00111000
	120	-52	30	2 2 1 1	2	00110100
	130	-52	42	2 2 1 1	3	00100010
	140	-52	54	2 2 1 1	4	00101010
	145	-52	66	2 2 1 1	opt	00100110

Note: Interpret the symbols under the heading settings as 0=ON, 1=OFF, opt=the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. SW1s to SW4s not in use must have all eight sections set to OFF.

NT6X30CA decimonic ringing (BOC)

Line	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	20	2 2 1 1	1	00011000
	95	-52	30	2 2 1 1	2	00010100
	100	-52	40	2 2 1 1	3	00011100
	110	-52	50	2 2 1 1	4	00010010
	125	-52	60	2 2 1 1	opt	00011010
Medium	105	-52	20	2 2 1 1	1	01011000
	110	-52	30	2 2 1 1	2	01010100
	115	-52	40	2 2 1 1	3	01011100
	125	-52	50	2 2 1 1	4	01010010
	140	-52	60	2 2 1 1	opt	01011010
High	120	-52	20	2 2 1 1	1	00111000
	120	-52	30	2 2 1 1	2	00110100
	130	-52	40	2 2 1 1	3	00111100
	140	-52	50	2 2 1 1	4	00110000
	145	-52	60	2 2 1 1	opt	00111010

Note: Interpret the symbols under the heading settings as 0=ON, 1=OFF, opt=the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. SW1s to SW4s not in use must have all eight sections set to OFF.

NT6X30CA (continued)

NT6X30CA synchromonic ringing (REA)

Line	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	16	1.95 1.35 1.35 1.35	1	10010000
	90	-52	20	1.95 1.35 1.35 1.35	1	10011000
	95	-52	30	1.95 1.35 1.35 1.35	2	10010100
	100	-52	42	1.95 1.35 1.35 1.35	3	10000010
	110	-52	54	1.95 1.35 1.35 1.35	4	10001010
	125	-52	66	1.95 1.35 1.35 1.35	opt	10000110
Medium	105	-52	16	1.95 1.35 1.35 1.35	1	11010000
	105	-52	20	1.95 1.35 1.35 1.35	1	11011000
	110	-52	30	1.95 1.35 1.35 1.35	2	11010100
	115	-52	42	1.95 1.35 1.35 1.35	3	11000010
	125	-52	54	1.95 1.35 1.35 1.35	4	11001010
	140	-52	66	1.95 1.35 1.35 1.35	opt	11000110
High	120	-52	16	1.95 1.35 1.35 1.35	1	10110000
	120	-52	20	1.95 1.35 1.35 1.35	1	10111000
	120	-52	30	1.95 1.35 1.35 1.35	2	10110100
	130	-52	42	1.95 1.35 1.35 1.35	3	10100010
	140	-52	54	1.95 1.35 1.35 1.35	4	10101010
	145	-52	66	1.95 1.35 1.35 1.35	opt	10100110

Note: Interpret the symbols under the heading settings as 0=ON, 1=OFF, opt=the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. SW1s to SW4s not in use must have all eight sections set to OFF.

NT6X30CA harmonic ringing (REA)

Line	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	16-2/3	1.95 1.35 1.35 1.35	1	10001000
	95	-52	25	1.95 1.35 1.35 1.35	2	10000100
	100	-52	33-1/3	1.95 1.35 1.35 1.35	3	10001100
	110	-52	50	1.95 1.35 1.35 1.35	4	10010010
	125	-52	66-2/3	1.95 1.35 1.35 1.35	opt	10010110
Medium	105	-52	16-2/3	1.95 1.35 1.35 1.35	1	11001000
	110	-52	25	1.95 1.35 1.35 1.35	2	11000100
	115	-52	33-1/3	1.95 1.35 1.35 1.35	3	11001100
	125	-52	50	1.95 1.35 1.35 1.35	4	11010010
	140	-52	66-2/3	1.95 1.35 1.35 1.35	opt	11010110
High	120	-52	16-2/3	1.95 1.35 1.35 1.35	1	10101000
	120	-52	25	1.95 1.35 1.35 1.35	2	10100100
	130	-52	33-1/3	1.95 1.35 1.35 1.35	3	10101100
	140	-52	50	1.95 1.35 1.35 1.35	4	10110010
	145	-52	66-2/3	1.95 1.35 1.35 1.35	opt	10110110

Note: Interpret the symbols under the heading settings as 0=ON, 1=OFF, opt=the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. SW1s to SW4s not in use must have all eight sections set to OFF.

NT6X30CA (continued)

NT6X30CA decimonic ringing (REA)

Line	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	20	1.95 1.35 1.35 1.35	1	10011000
	95	-52	30	1.95 1.35 1.35 1.35	2	10010100
	100	-52	40	1.95 1.35 1.35 1.35	3	10011100
	110	-52	50	1.95 1.35 1.35 1.35	4	10010010
	125	-52	60	1.95 1.35 1.35 1.35	opt	10011010
Medium	105	-52	20	1.95 1.35 1.35 1.35	1	11011000
	110	-52	30	1.95 1.35 1.35 1.35	2	11010100
	115	-52	40	1.95 1.35 1.35 1.35	3	11011100
	125	-52	50	1.95 1.35 1.35 1.35	4	11010010
	140	-52	60	1.95 1.35 1.35 1.35	opt	11011010
High	120	-52	20	1.95 1.35 1.35 1.35	1	10111000
	120	-52	30	1.95 1.35 1.35 1.35	2	10110100
	130	-52	40	1.95 1.35 1.35 1.35	3	10111100
	140	-52	50	1.95 1.35 1.35 1.35	4	10110010
	145	-52	60	1.95 1.35 1.35 1.35	opt	10111010

Note: Interpret the symbols under the heading settings as 0=ON, 1=OFF, opt=the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. SW1s to SW4s not in use must have all eight sections set to OFF.

NT6X30CA international ringing

Line	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	67	-52	25	1.95 1.35 1.35 1.35	1 to 4	10001110
Medium	75	-52	25	1.95 1.35 1.35 1.35	1 to 4	11001110
High	82	-52	25	1.95 1.35 1.35 1.35	1 to 4	10101110
Low	67	-52	25	2 2 1 1	1 to 4	00001110
Medium	75	-52	25	2 2 1 1	1 to 4	01001110
High	82	-52	25	2 2 1 1	1 to 4	00101110
Japan	75	0	16	2 2 1 1	1 to 4	11101110
U.K.	75	-52	25	1 1 0.4 0.6	1 to 4	01101110

Note: Interpret the symbols under the heading settings as 0=ON, 1=OFF, opt=the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. SW1s to SW4s not in use must have all eight sections set to OFF.

NT6X30CA harmonic ringing (BOC) (Sheet 1 of 2)

Line	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	16-2/3	2 2 1 1	1	00001000
	95	-52	25	2 2 1 1	2	00000100
	100	-52	33-1/3	2 2 1 1	3	00001100
	110	-52	50	2 2 1 1	4	00010010
	125	-52	66-2/3	2 2 1 1	opt	00010110
Medium	105	-52	16-2/3	2 2 1 1	1	01001000
	110	-52	25	2 2 1 1	2	01000100
	115	-52	33-1/3	2 2 1 1	3	01001100

Note: Interpret the symbols under the heading settings as 0=ON, 1=OFF, opt=the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. SW1s to SW4s not in use must have all eight sections set to OFF.

NT6X30CA (continued)

NT6X30CA harmonic ringing (BOC) (Sheet 2 of 2)

Line	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
	125	-52	50	2 2 1 1	4	01010010
	140	-52	66-2/3	2 2 1 1	opt	01010110
High	120	-52	16-2/3	2 2 1 1	1	00101000
	120	-52	25	2 2 1 1	2	00100100
	130	-52	33-1/3	2 2 1 1	3	00101100
	140	-52	50	2 2 1 1	4	00110010
	145	-52	66-2/3	2 2 1 1	opt	00110110

Note: Interpret the symbols under the heading settings as 0=ON, 1=OFF, opt=the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. SW1s to SW4s not in use must have all eight sections set to OFF.

The information about NT6X30CA tolerances appears in the following tables.

NT6X30CA frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
16 to 33-1/3 Hz	±1/3 Hz
40 to 66-2/3 Hz	±1%
25 Hz international	±1/3 Hz
-52V (dc)	-49.75 to -52.5V (dc)
-38V (dc)	±2V (dc)
+38V (dc)	±2V (dc)

NT6X30CA ac voltage tolerances (Sheet 1 of 2)

Nominal	Low	High
67	65	69
75	73	77
82	80	84

NT6X30CA ac voltage tolerances (Sheet 2 of 2)

Nominal	Low	High
86	84	88
90	87.3	92.7
95	92.1	97.8
100	97	103
105	101.9	108.1
110	106.7	113.3
115	111.6	118.4
120	116.4	123.6
125	121.2	128.7
130	126.1	133.9
140	135.8	144.2
145	140.7	149.3

The information about ANI and coin voltages appears in the following table.

NT6X30CA ANI and coin voltage

Output	Limits
+48V	+52V, ±2.5V
-48V	-52V, ±2.5V
+130V	+130V, ±5V
-130V	-130V, ±5V

NT6X30CA (end)

Signaling

Pin numbers

The following table provides pin number information for the NT6X30CA finger connector (P1).

NT6X30CA pin number

Pin	Signal	Pin	Signal
1	AF0	19	-48V
2	LOGIC GND	20	BR
3	AF1	21	ABS-48
4	LOGIC GND	22	FSPMON
5	ACT	23	LOGIC GND
6	LOGIC GND	24	SYNC 64
7	XOVER	25	RRING
8	LOGIC GND	26	RTIP
9	RMS	27	RRING
10	LOGIC GND	28	RTIP
11	CUR	29	-52V
12	LOGIC GND	30	ABS BR
13	LOGIC GND	31	
14	FSPLINK	32	+52V
15	-48V	33	
16	BR	34	-130V
17	-48V	35	Fuse Alarm
18	BR	36	+130V

Power requirements

The NT6X30CA requires -39.5V to -75V, and nominally 2.5 A, to a maximum of 4 A. The card consumes 140 W of power.

NT6X30DA

Product description

The NT6X30DA contains two cards. These cards are the NT6X38 ringing control and the NT6X37 ringing amplifier. Ringing signals start in NT6X38. The NT6X37 amplifies ringing signals to the required output level.

The NT6X30DA operates using power control circuits in the DMS-100 line concentrating module (LCM) FSP (NT6X35). This card applies in Australia. This card applies in the DMS-10 in China.

Functional description

The NT6X30DA generates ringing signals and dc voltages for automatic number identification (ANI) and coin functions. To meet telephone company requirements, use dual inline package (DIP) switches or straps manually set frequencies and amplitudes of ringing waveform. Do not change a DIP switch setting when power is ON. Set the correct circuit breaker on the NT6X35 FSP to OFF.

The NT6X30DA contains two printed circuit boards: the ringing control NT6X38DA and the ringing amplifier NT6X37AA. Ringing signals start in the NT6X38DA. The NT6X37AA amplifies the ringing signals to the required output level.

Ringing control NT6X38

The NT6X38 performs the following functions:

- generates a ringing signal
- provides ANI and coin outputs
- monitors the ring bus output
- synchronizes the dc-to-dc converters
- provides an auxiliary supply

Generating ringing signal

The waveform store PROM holds a digital representation of a single cycle of each ringing waveform. According to the manual settings, the control logic selects the correct timing, frequency, and amplitude. The output from the waveform store passes through the digital-to-analog converter and low-pass filter. This action provides the analog input signal for the ringing amplifier card.

Providing ANI and coin outputs

A single dc-to-dc converter provides 52Vand ±130V outputs for ANI and coin functions, in this order.

NT6X30DA (continued)

Monitoring ring bus outputs

The NT6X38DA monitors the ring bus output from the NT6X37AA for output voltage and current. If a ringing overvoltage is present, the system sends a signal to the NT6X37AA to shut down the amplifier. If an ANI or coin overvoltage is present, the system shuts down the correct converter. If both events occur, the FSP disconnects the primary power.

The monitor circuit provides transistor-transistor logic (TTL)-level status signals to the LCM processor. These signals indicate ringing voltage (RMS), ringing current (CUR) and low ANI or coin voltage. These conditions combine with three status bits from the control logic. The bits are sent through a serial data link to isolate the ground reference.

Synchronizing dc-to-dc converters

The dc-to-dc converters in the NT6X37AA must be synchronized to the LCM system clock. A phase-lock loop converts the frequency because the converter requires 48 kHz synchronization and the LCM provides 64 kHz. The LCM synchronization feed and the NT6X37AA synchronization input provide the dc isolation of the grounds.

Providing auxiliary supply

A small dc-to-dc converter supplies ±15V and ±5V for the internal circuits of NT6X38DA. The ±15V is used for the control circuits on the NT6X37AA.

Ringing amplifier NT6X37

The NT6X37 amplifier is a dc-coupled class-B type that uses power field-effect transistors (FET) as the output devices. Two dc-to-dc converters power the amplifier. This power allows a feedback signal from the ring bus output to independently control the positive and negative supply voltage.

If a ringing output is available, the supply voltages are at a minimum. This minimum is approximately ±20V. Under normal operation, the feedback from the ringing output causes the positive and negative supply voltages to increase alternately. This action indicates that enough voltage is available to produce the required output.

Technical data

Information about NT6X30AA ringing appears in the following tables.

Ringing type applications that use NT6X30DA

Ring type	User	DIP switch setting
Switches 1 to 4	China	Refer to the table below.
Switches 1 to 4	Australia	Refer to the table below.
Note: Release numbers: OE, OF, OG, OH, OJ, OK, OL, or ON. If a release number is not available, the card is release OE or earlier. Release numbers: OP through OZ, and AE or later. Release number: CC or later.		

International

	Voltage		Freq		Switch	Setting
	ac	dc	(Hz)	Cadence (seconds)	(1-4)	12345678
China	86	-52	25	1.25 1.25 1.25 1.25	1 to 4	0011111X
Australia	86	-52	25	1.25 1.25 1.25 1.25	1 to 4	0011111X
Note: Interpret the symbols under the heading settings as 0 = ON, 1 = OFF, X = ON or OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Use switch settings for Japan with Lcrls modified for Japanese ringing only. Pull the ringing generator card completely from the shelf to change DIP switch settings.						

Ringing characteristics and DIP switch settings

Voltage				Setting
AC	DC	Freq (Hz)	Cadence (seconds)	12345678
86	-49.75	25	1.25 1.25 1.25 1.25	0011111X
Note: Interpret the symbols under the heading settings as 0 = ON, 1 = OFF, X = ON or OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Use switch settings for Japan with Lcrls modified for Japanese ringing only. Pull the ringing generator card completely from the shelf to change DIP switch settings.				

NT6X30DA (continued)

Information about NT6X30DA voltages appears in the following tables.

NT6X30DA Frequency and DC voltage tolerances

Frequency/dc voltage	Tolerances
16 to 33.33 Hz	±33 Hz
40 to 66.66 Hz	±1 %
25 Hz international	±.33 Hz
-52 Vdc	-49.75 to -52.5 Vdc
-38 Vdc	±2 Vdc
+ 38 Vdc	±2 Vdc

NT6X30DA ac voltage tolerances

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8
100	97	103
105	101.9	108.1
110	106.7	113.3
115	111.6	118.4
120	116.4	123.6
125	121.2	128.7
130	126.1	133.9
140	135.8	144.2
155	150.3	159.6

NT6X30DA ANI/coin voltage

Output	Limits
+48V	+ 52, ±2.5 V
- 48V	- 52, ±5V
+130 V	+ 130, ±5V
-130V	-130 V, ±5V

Power requirements

The NT6X30DA requires 42 to 56V, and nominally 3.5 A to a maximum of 5 A. The card consumes 180 W of power.

NT6X30DB

Product description

The NT6X30DB ringing generator is a horizontal mount version of the ringing generator for international markets. The contains a single card. This card provides functionality in the NT6X30DA (China) and NT6X30AE (Australia) ringing generators. A previous version of this functionality required two cards. The is backwards compatible with the NT6X30DA and NT6X30AE.

Location

The NT6X30DB operates in with power control circuits in the DMS-100 line concentrating equipment (LCE) FSP (NT6X35) for application in Australia. The operates in with power control circuits in the DMS-10 for application in China.

Functional description

The NT6X30DB generates the ringing signals that international markets require. These markets include China and Australia.

Functional blocks

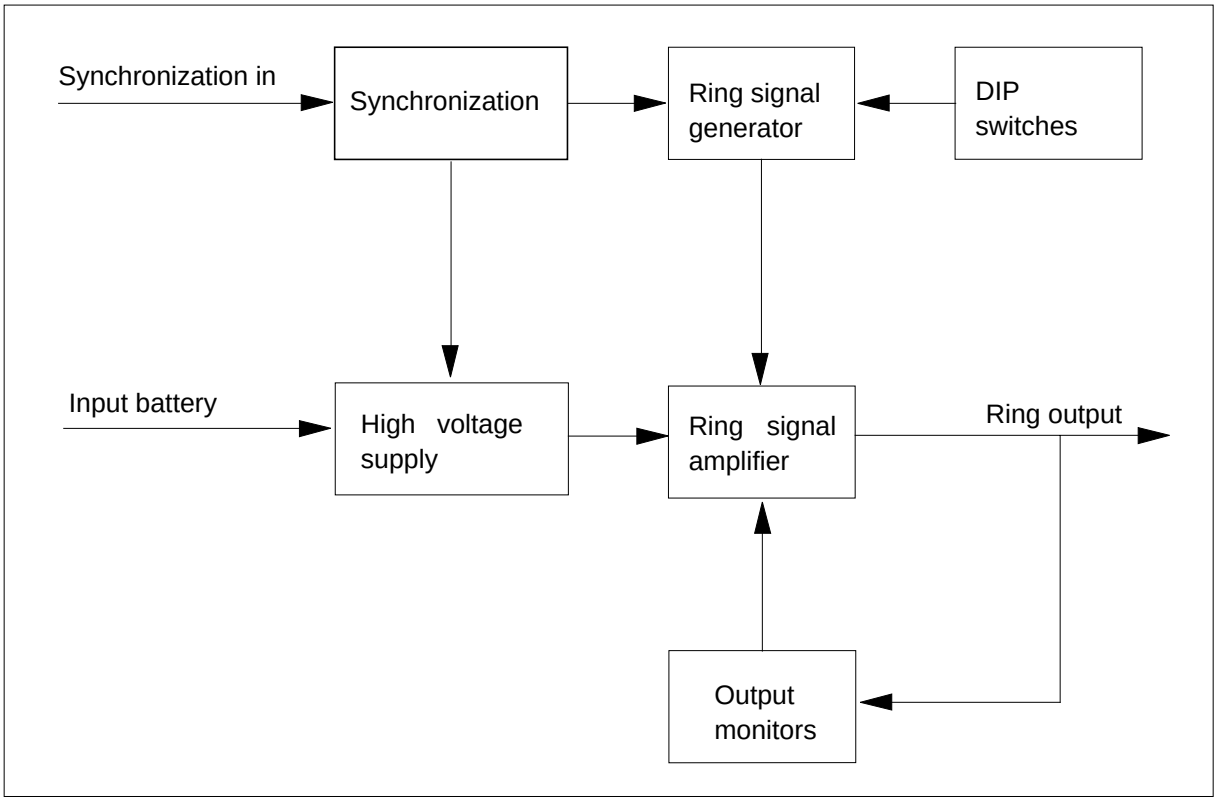
Operating company personnel set ring output frequency and amplitude manually. This process occurs during installation. Operating company personnel use the four dual inline package (DIP) switches to meet international requirements.

The NT6X30DB has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X30DB functional blocks



High voltage supply

The system filters raw battery input voltage (-48 V) and feeds the voltage into a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of a flyback transformer. The system rectifies and filters the secondary of this transformer to produce a regulated 300 V supply that floats. An isolated output produces voltages. The ringing control and monitor circuits require these voltages for power.

Ring signal generator

The programmable read-only memory (PROM) of the card microcontroller stores a digital image that represents the ringing waveform. The microcontroller sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. The microcontroller performs this action in response to the setting of the DIP switches of the card. The DAC produces a low voltage sinusoidal waveform to the ring signal amplifier. This waveform is the correct frequency and reference amplitude. The reference amplitude includes dc offset. The microcontroller provides additional

NT6X30DB (continued)

information, like zero-crossing detect (XOVER) and subcycle cadence information (AF0 and AF1).

Ring signal amplifier

The system feeds the ringing signal from the ring signal generator into a class D amplifier circuit. This circuit modulates the pulse width to a full-bridge switch configuration. This configuration switches the high voltage supply that floats alternately to ground on one side for each half cycle of the output waveform. This process creates a train of variable width pulses. The filtered pulses produce the necessary sinusoidal ringing output voltage and dc offset. The sinusoidal ringing output voltage and dc offset is fed out of the ringing generator. A comparison of the filtered output to the input reference signal from the ring signal generator circuit occurs. This comparison to regulate this output.

Output monitors

Monitor circuits monitor the ringing output and dc offset for ac over- and undervoltage. When an overvoltage condition occurs, the system disables the ringing amplifier. When an undervoltage condition occurs, the current must be less than the current limit point to allow shutdown.

The monitor circuits provide electrically isolated transistor-transistor logic (TTL) level signals to the LCM processor. These signals indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the line concentrating module synchronizes all dc-dc converters and the ringing amplifier on this card. The phase-lock loop synchronizes the converters and amplifier at an integer multiple of 8 kHz. The system electrically isolates this synchronization from the clock signal that the LCM provides. The system isolates this synchronization between the various converters on this card.

Signaling

Pin numbers

Pin number information for the finger connector (P1) appears in the following table.

NT6X30DBpin numbers (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	AF0	19	-48 V
2	LOGIC GND	20	BR

NT6X30DBpin numbers (Sheet 2 of 2)

Pin	Signal	Pin	Signal
3	AF1	21	ABS-48
4	LOGIC GND	22	FSPMON
5	ACT	23	LOGIC GND
6	LOGIC GND	24	SYNC 64
7	XOVER	25	RRING
8	LOGIC GND	26	RTIP
9	RMS	27	RRING
10	LOGIC GND	28	RTIP
11	CUR	29	NC
12	LOGIC GND	30	ABS BR
13	LOGIC GND	31	
14	FSPLINK	32	NC
15	-48 V	33	
16	BR	34	NC
17	-48 V	35	Fuse Alarm
18	BR	36	NC

Technical data

Information on voltages appears in the following tables.

NT6X30DB (continued)

Power requirements

The NT6X30DB requires -39.5 V to -75 V and a nominal current of 1 A to a maximum of 2 A. The consumes 75 W of power.

NT6X30DB international ringing

	Voltage		Freq	Subcycle cadence	Switch	Setting
	ac	dc	(Hz)	(seconds)	(SW1-4)	12345678
Low	67	-52	25	1.95 1.35 1.35 1.35	1 to 4	10001110
Med	75	-52	25	1.95 1.35 1.35 1.35	1 to 4	11001110
High	82	-52	25	1.95 1.35 1.35 1.35	1 to 4	10101110
Low	67	-52	25	2 2 1 1	1 to 4	00001110
Med	75	-52	25	2 2 1 1	1 to 4	01001110
High	82	-52	25	2 2 1 1	1 to 4	00101110
Japan	76	0	16	2 2 1 1	1 to 4	11101110
U.K.	75	-52	25	1 1 0.40. 6	1 to 4	01101110
China	86	-52	25	1.25 1.25 1.25 1.25	1 to 4	00111110
Brazil	86	-52	25	1.25 1.25 1.25 1.25	1 to 4	00111110
Australia	90	-52	25	1 1 0.40 0.60	1 to 4	01111110
Morroco	80	-52	50	1.70 1.70 0.80 0.80	1 to 4	10111110
Germany	65	-60	25	2 2 1 1	1 to 4	11111110
Phillipines	90	-52	20	1.25 1.25 1.25 1.25	1 to 4	11110110

Note: The interpretation of the symbols under the heading settings is 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.

NT6X30DB international coded and superimposed ringing (Sheet 1 of 2)

	Voltage		Freq		Switch	Setting
Line	ac	dc	(Hz)	Cadence (seconds)	(SW1-4)	12345678
1	86	-52	20	2 2 1 1	1 to 4	00000000
2	86	-38	20	2 2 1 1	1 & 2	01000000

NT6X30DB international coded and superimposed ringing (Sheet 2 of 2)

Line	Voltage ac	dc	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
3	86	+38	20	2 2 1 1	3 & 4	00100000
4	86	-38	20	2 2 1 1	1 & 2	00011110
5	86	+38	20	2 2 1 1	3 & 4	01011110

NT6X30DB international frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
16 to 33-1/3 Hz	+ or - 1/3 Hz
40 to 66-2/3 Hz	+ or - 1 %
25 Hz international	+ or - 1/3 Hz
-52 V (dc)	-49.5 to -53.5 V (dc)
-38 V (dc)	+ or - 2 V (dc)
+ 38 V (dc)	+ or - 2 V (dc)

NT6X30DB international ac voltage tolerances

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8

NT6X30EA

Product description

The NT6X30EA ringing generator is a low profile horizontal mount version of the ringing generator for international markets. The contains a single card. This card provides the required functionality.

Location

The NT6X30EA mounts in the cabinetized DMS-100 product, above the modular supervisory panel (MSP). The MSP is part of the line concentrating module (LCM) frame.

Functional description

The NT6X30EA generates the ringing signals that international markets require. These markets include China and Australia.

Functional blocks

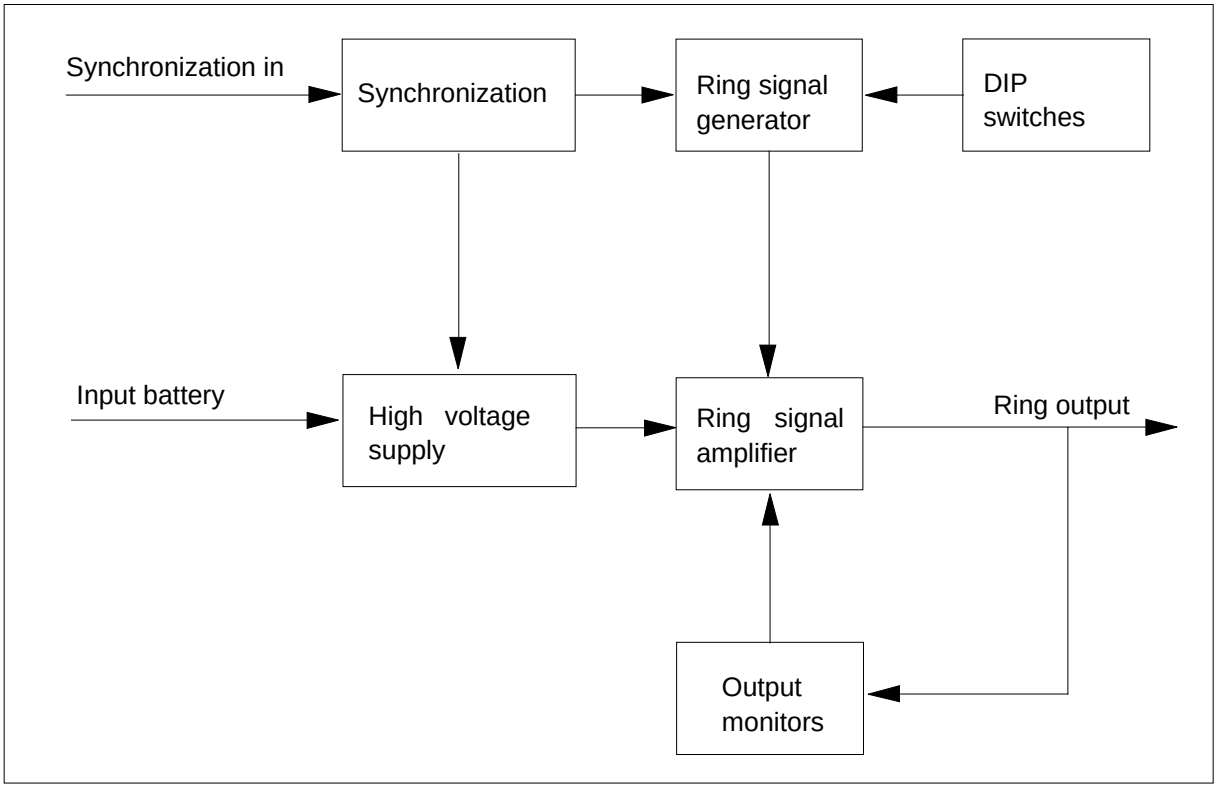
Operating company personnel set ring output frequency and amplitude during installation. Operating company personnel use the four dual inline package (DIP) switches to meet international requirements.

The NT6X30EA has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X30EA functional blocks



High voltage supply

The system filters raw battery input voltage (-48 V) and feeds this voltage into a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of a flyback transformer. The system rectifies and filters the secondary of this transformer to produce a regulated 300V supply that floats. Ringing control and monitor circuits require voltages for power. An isolated output produces these voltages.

Ring signal generator

The programmable read-only memory (PROM) of the card microcontroller stores a digital image that represents the ringing waveform. The microcontroller sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. The microcontroller performs this action in response to the setting of the DIP switches of the card. The DAC provides a low voltage sinusoidal waveform to the ring signal amplifier. This waveform is the correct frequency and reference amplitude. The reference amplitude includes dc offset. The microcontroller provides additional

NT6X30EA (continued)

information like zero-crossing detect (X-OVER) and subcycle cadence information (AF0 and AF1).

Ring signal amplifier

The system feeds the ringing signal from the ring signal generator into a class D amplifier circuit. This circuit modulates the pulse width to a full-bridge switch configuration. This configuration switches the high voltage supply that floats alternately to ground on one side for each half cycle of the output waveform. This process creates a train of variable width pulses. The filtered pulses produce the necessary sinusoidal ringing output voltage and dc offset. The sinusoidal ringing output voltage and dc offset fed out of the ringing generator. A comparison of a sample of the filtered output to the input reference signal from the ring signal generator circuit occurs. This comparison occurs to regulate this output.

Output monitors

The monitor circuits monitor the ringing output and dc offset for ac overvoltage and undervoltage. When an overvoltage condition occurs, the system disables the ringing amplifier. When an undervoltage condition occurs, the current must be less than the current limit point to allow shutdown.

The monitor circuits also provide electrically isolated transistor-transistor logic (TTL) level signals to the LCM processor. These signals indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the LCM synchronizes the dc-dc converters and the ringing amplifier on this card. The phase-lock loop synchronizes the dc-dc converters and the ringing amplifier at an integer multiple of 8 kHz. The system electrically isolates this synchronization from the clock signal that the LCM provides. The system isolates this synchronization between the various converters on this card.

Signaling

Pin numbers

Pin number information for the NT6X30EA finger connector (P1) appears in the following figure.

NT6X30EA pin numbers (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	AF0	19	-48 V
2	LOGIC GND	20	BR

NT6X30EA pin numbers (Sheet 2 of 2)

Pin	Signal	Pin	Signal
3	AF1	21	ABS-48
4	LOGIC GND	22	FSPMON
5	ACT	23	LOGIC GND
6	LOGIC GND	24	SYNC 64
7	XOVER	25	RRING
8	LOGIC GND	26	RTIP
9	RMS	27	RRING
10	LOGIC GND	28	RTIP
11	CUR	29	-52 V
12	LOGIC GND	30	ABS BR
13	LOGIC GND	31	
14	FSPLINK	32	+52 V
15	-48 V	33	
16	BR	34	-130 V
17	-48 V	35	Fuse Alarm
18	BR	36	+130 V

Technical data

Information on NT6X30EA voltages appears in the following tables.

NT6X30EA (continued)

Power requirements

The NT6X30EA requires -39.5 V to -75 V, and a nominal current of 2 A to a maximum of 3 A. The NT6X30EA consumes 100 W of power.

NT6X30EA international ringing

	Voltage ac dc	Freq (Hz)	Subcycle cadence (seconds)	Switch (SW1-4)	Setting 12345678
Low	67 -52	25	1.95 1.35 1.35 1.35	1 to 4	10001110
Med	75 -52	25	1.95 1.35 1.35 1.35	1 to 4	11001110
High	82 -52	25	1.95 1.35 1.35 1.35	1 to 4	10101110
Low	67 -52	25	2 2 1 1	1 to 4	00001110
Med	75 -52	25	2 2 1 1	1 to 4	01001110
High	82 -52	25	2 2 1 1	1 to 4	00101110
Japan	76 0	16	2 2 1 1	1 to 4	11101110
U.K.	75 -52	25	1 1 0.4 0.6	1 to 4	01101110
China	86 -52	25	1.25 1.25 1.25 1.25	1 to 4	00111110
Brazil	86 -52	25	1.25 1.25 1.25 1.25	1 to 4	00111110
Australia	90 -52	25	1 1 0.40 0.60	1 to 4	01111110
Morocco	80 -52	50	1.70 1.70 0.80 0.80	1 to 4	10111110
Germany	65 -60	25	2 2 1 1	1 to 4	11111110
Philippines	90 -52	20	1.25 1.25 1.25 1.25	1 to 4	11110110

Note: The interpretation of the symbols under the heading setting is 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.

NT6X30EA international coded and superimposed ringing

Line	Voltage ac dc	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
1	86 -52	20	2 2 1 1	1 to 4	00000000
2	86 -38	20	2 2 1 1	1 & 2	01000000
3	86 +38	20	2 2 1 1	3 & 4	00100000
4	86 -38	20	2 2 1 1	1 & 2	00011110
5	86 +38	20	2 2 1 1	3 & 4	01011110

NT6X30EA international frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
16 to 33-1/3 Hz	+ or - 1/3 Hz
40 to 66-2/3 Hz	+ or - 1 %
25 Hz international	+ or - 1/3 Hz
-52 V (dc)	-49.75 to -52.5 V (dc)
-38 V (dc)	+ or - 2 V (dc)
+ 38 V (dc)	+ or - 2 V (dc)

NT6X30EA international ac voltage tolerances

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8

NT6X30FA

Product description

The NT6X30FA ringing generator is a horizontal mount version of the ringing generator for the United Kingdom market. The contains a single card. This card provides functionality for the NT6X30FA. A previous version of this functionality earlier required two cards in the NT6X30AB ringing generator. The NT6X30FA is backwards compatible with the NT6X30AB.

Location

The NT6X30FA fits into the NT6X35AA frame supervisory panel (FSP). The FSP is part of the line concentrating equipment (LCE) frame.

Functional description

The NT6X30FA generates the ringing signals that the United Kingdom requires.

Functional blocks

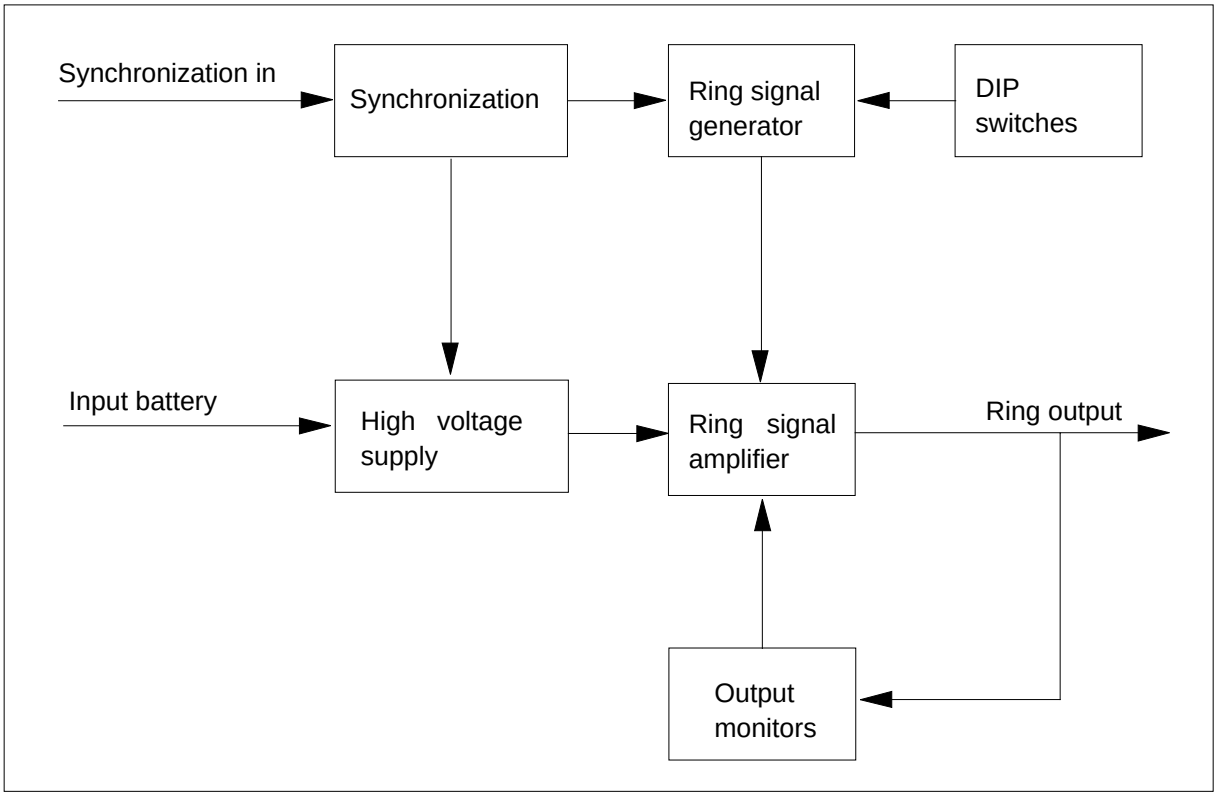
Ring output frequency and amplitude are set at the factory to meet United Kingdom requirements.

The NT6X30FA has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figures.

NT6X30FA functional blocks



High voltage supply

The system filters raw battery input voltage (-48 V) and feeds the voltage into a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of a flyback transformer. The system rectifies and filters the secondary of this transformer to produce a regulated 300 V supply that floats. The ringing control and monitor circuits require voltages for power. An isolated output produces these voltages.

Ring signal generator

The programmable read-only memory (PROM) of the card microcontroller stores a digital image that represents the ringing waveform. The microcontroller sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. The microcontroller performs this action in response to the setting of the DIP switches of the card. The DAC produces a low voltage sinusoidal waveform to the ring signal amplifier. This low voltage sinusoidal waveform is the correct frequency and reference amplitude. The reference amplitude includes dc offset. The microcontroller provides additional information like zero-crossing detect (XOVER) and subcycle cadence information (AF0 and AF1).

NT6X30FA (continued)

Ring signal amplifier

The system feeds the ringing signal from the ring signal generator into a class D amplifier circuit. This circuit modulates the pulse width to a full-bridge switch configuration. This configuration switches the high voltage supply that floats alternately to ground on one side for each half cycle of the output waveform. This process creates a train of variable width pulses. The filtered pulses produce the necessary sinusoidal ringing output voltage and dc offset. The sinusoidal ringing output voltage and dc offset are fed out of the ringing generator. A comparison of a sample of the filtered output to the input reference signal from the ring signal generator circuit occurs. This comparison occurs to regulate this output.

Output monitors

The monitor circuits monitor the ringing output and dc offset for ac over- and undervoltage. When an overvoltage condition occurs, the system disables the ringing amplifier. When an undervoltage condition occurs, the current must be less than the current limit point to allow shutdown.

The monitor circuits provide electrically isolated transistor-transistor logic (TTL) level signals to the LCM processor. These signals indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the LCM synchronizes dc-dc converters and the ringing amplifier on this card. The phase-lock loop synchronizes dc-dc converters and the ringing amplifier at an integer multiple of 8 kHz. The system electrically isolates this synchronization from the clock signal that the LCM provides. The system isolates this synchronization between the various converters on this card.

Signaling

Pin numbers

Pin number information for the NT6X30FA finger connector (P1) appears in the following table.

NT6X30FA pin numbers (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	AF0	19	-48 V
2	LOGIC GND	20	BR
3	AF1	21	ABS-48

NT6X30FA pin numbers (Sheet 2 of 2)

Pin	Signal	Pin	Signal
4	LOGIC GND	22	FSPMON
5	ACT	23	LOGIC GND
6	LOGIC GND	24	SYNC 64
7	XOVER	25	RRING
8	LOGIC GND	26	RTIP
9	RMS	27	RRING
10	LOGIC GND	28	RTIP
11	CUR	29	-52 V
12	LOGIC GND	30	ABS BR
13	LOGIC GND	31	
14	FSPLINK	32	+52 V
15	-48V	33	
16	BR	34	-130 V
17	-48V	35	Fuse Alarm
18	BR	36	+130 V

Technical data

Information on NT6X30FA voltages, ringing and tolerances appears in the following tables.

NT6X30FA (end)

Power requirements

The NT6X30FA requires -39.5 V to -75 V, and a nominal current of 2 A to a maximum of 3 A. The NT6X30FA consumes 100 W of power.

NT6X30FA international ringing

	Voltage		Freq	Subcycle cadence	Switch	Setting
	ac	**dc**	**(Hz)**	**(seconds)**	**(SW1-4)**	**12345678**
U.K.	75	-52	25	1 1 0.4 0.6	1 to 4	01101110
Note: The interpretation of the symbols under the heading settings is 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.						

NT6X30FA international frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
25 Hz international	+ or -1/3 Hz
-52 V (dc)	-49.75 to -52.5 V (dc)

NT6X30FA international ac voltage tolerances

Nominal	Low	High
75	73	77

NT6X30GA

Product description

The NT6X30GA ringing generator is a low profile horizontal mount version of the ringing generator for international markets. The contains a single card, which provides the required functionality.

Location

The NT6X30GA mounts in the cabinetized DMS-100 product, above the modular supervisory panel (MSP). The MSP is part of the cabinetized line concentrating equipment (CLCE) frame.

Functional description

The NT6X30GA generates the ringing signals that the United Kingdom requires.

Functional blocks

Ring output frequency and amplitude are set at the factory to meet the requirements of the United Kingdom.

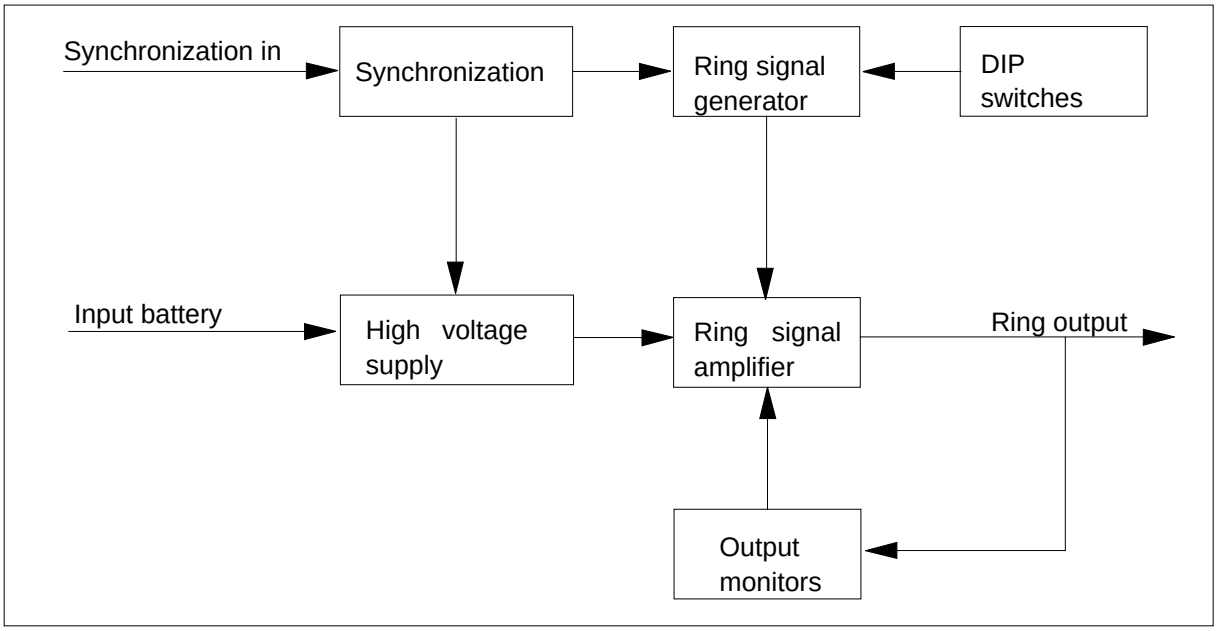
The NT6X30GA has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X30GA (continued)

NT6X30GA functional blocks



High voltage supply

The system filters raw battery input voltage (-48V) and feeds the voltage into a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of a flyback transformer. The system rectifies and filters the secondary of this transformer to produce a regulated 300 V supply that floats. The ringing control and monitor circuits require voltages for power. An isolated output produces these voltages.

Ring signal generator

The programmable read-only memory (PROM) of the card microcontroller stores a digital image that represents the ringing waveform. The microcontroller sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. The DAC produces a low voltage sinusoidal waveform to the ring signal amplifier. This low voltage sinusoidal waveform is the right frequency and reference amplitude. The reference amplitude includes dc offset. The microcontroller provides additional information like zero-crossing detect (XOVER) and subcycle cadence information (AF0 and AF1).

Ring signal amplifier

The ringing signal from the ring signal generator is fed into a class D amplifier circuit. This circuit modulates the pulse width to a full-bridge switch configuration. This configuration switches the high voltage supply that floats

alternately to ground on one side for each half cycle of the output waveform. This process creates a train of variable width pulses. The filtered pulses produce the necessary sinusoidal ringing output voltage and dc offset. The sinusoidal ringing output voltage and dc offset is fed out of the ringing generator. A comparison of a sample of filtered output to the input reference signal from the ring signal generator circuit occurs. This comparison occurs to regulate this output.

Output monitors

The monitor circuits monitor the ringing output for ac over- and undervoltage. The monitor circuits monitor the dc-offset for over- and undervoltage. When an overvoltage condition occurs, the system disables the ringing amplifier. When an undervoltage condition occurs, the current must be less than the current limit point to allow shutdown.

The monitor circuits provide electrically isolated transistor-transistor logic (TTL) level signals to the LCM processor. These signals indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the line concentrating module synchronizes all dc-dc converters and the ringing amplifier on this card. The phase-lock loop synchronizes dc-dc converters and the ringing amplifier at an integer multiple of 8 kHz. The system electrically isolates this synchronization from the clock signal that the LCM provides. The system isolates this synchronization between the various converters on this card.

Signaling

Pin numbers

Pin number information for the NT6X30GA finger connector (P1) appears in the following table.

NT6X30GA pin numbers (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	AF0	19	-48 V
2	LOGIC GND	20	BR
3	AF1	21	ABS-48
4	LOGIC GND	22	FSPMON
5	ACT	23	LOGIC GND

NT6X30GA (continued)

NT6X30GA pin numbers (Sheet 2 of 2)

Pin	Signal	Pin	Signal
6	LOGIC GND	24	SYNC 64
7	XOVER	25	RRING
8	LOGIC GND	26	RTIP
9	RMS	27	RRING
10	LOGIC GND	28	RTIP
11	CUR	29	-52 V
12	LOGIC GND	30	ABS BR
13	LOGIC GND	31	
14	FSPLINK	32	+52 V
15	-48 V	33	
16	BR	34	-130 V
17	-48 V	35	Fuse Alarm
18	BR	36	+130 V

Technical data

Information on NT6X30GA voltages appears in the following tables.

Power requirements

The NT6X30GA requires -39.5 V to -75 V, and a nominal current of 2 A to a maximum of 3 A. The NT6X30GA consumes 100 W of power.

NT6X30GA international ringing (Sheet 1 of 2)

	Voltage ac dc	Freq (Hz)	Subcycle cadence (seconds)	Switch (SW1-4)	Setting 12345678
Low	67 -52	25	1.95 1.35 1.35 1.35	1 to 4	10001110
Med	75 -52	25	1.95 1.35 1.35 1.35	1 to 4	11001110

Note: The interpretation of the symbols under the heading settings is 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.

NT6X30GA international ringing (Sheet 2 of 2)

	Voltage ac dc	Freq (Hz)	Subcycle cadence (seconds)	Switch (SW1-4)	Setting 12345678
High	82 -52	25	1.95 1.35 1.35 1.35	1 to 4	10101110
Low	67 -52	25	2 2 1 1	1 to 4	00001110
Med	75 -52	25	2 2 1 1	1 to 4	01001110
High	82 -52	25	2 2 1 1	1 to 4	00101110
Japan	76 0	16	2 2 1 1	1 to 4	11101110
U.K.	75 -52	25	1 1 0.4 0.6	1 to 4	01101110
China	86 -52	25	1.25 1.25 1.25 1.25	1 to 4	00111110
Brazil	86 -52	25	1.25 1.25 1.25 1.25	1 to 4	00111110
Australia	90 -52	25	1 1 0.40 0.60	1 to 4	01111110
Morroco	80 -52	50	1.70 1.70 0.80 0.80	1 to 4	10111110
Germany	65 -60	25	2 2 1 1	1 to 4	11111110
Phillipines	90 -52	20	1.25 1.25 1.25 1.25	1 to 4	11110110

Note: The interpretation of the symbols under the heading settings is 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.

NT6X30GA international coded and superimposed ringing

Line	Voltage ac dc	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
1	86 -52	20	2 2 1 1	1 to 4	00000000
2	86 -38	20	2 2 1 1	1 & 2	01000000
3	86 +38	20	2 2 1 1	3 & 4	00100000
4	86 -38	20	2 2 1 1	1 & 2	00011110
5	86 +38	20	2 2 1 1	3 & 4	01011110

NT6X30GA (end)

NT6X30GA international frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
16 to 33-1/3 Hz	+ or -1/3 Hz
40 to 66-2/3 Hz	+ or -1 %
25 Hz international	+ or -1/3 Hz
-52 V (dc)	-49.75 to -52.5 V (dc)
-38 V (dc)	+ or - 2 V (dc)
+ 38 V (dc)	+ or - 2 V (dc)

NT6X30GA international ac voltage tolerances

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8

NT6X30GB

Product description

The NT6X30GB ringing generator is a low-profile, horizontal-mount version of the ringing generator intended for the European market. The NT6X30GB contains a single card, which provides the required functionality.

Location

The NT6X30GB mounts in the cabinetized DMS-100 MMP product, above the modular supervisory panel (MSP). The MSP is part of the cabinetized line concentrating equipment (CLCE) frame.

Functional description

The NT6X30GB generates a single continuous ringing waveform from a selection of ringing signals that meet the European market requirements.

Functional blocks

Ring output frequency and amplitude are set at the factory to meet the requirements of the United Kingdom.

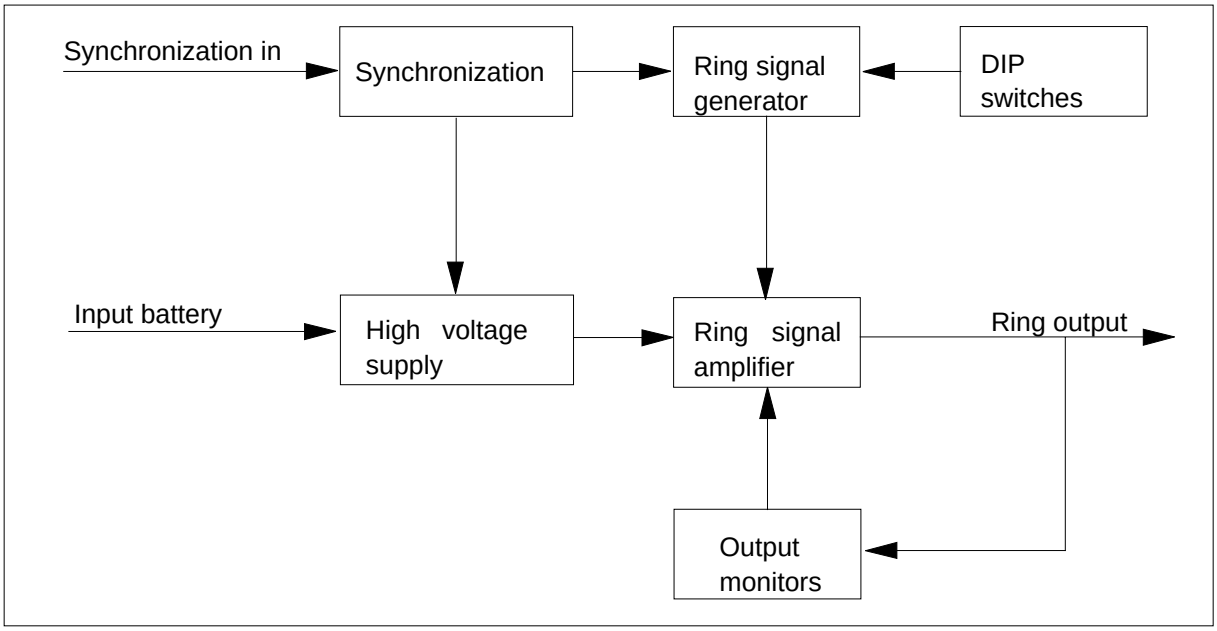
The NT6X30GB has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X30GB (continued)

NT6X30GB functional blocks



High-voltage supply

This circuit filters the raw battery voltage (-48 V dc nominal) and feeds this voltage into a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of a flyback transformer. The system rectifies and filters the secondary of this transformer to produce a regulated 300 V supply that floats. The ringing control and the monitor circuits require separate low voltages for power. Isolated outputs on this supply provide these voltages.

Ring-signal generator

The programmable read-only memory (PROM) of the card's microcontroller stores a digital image that represents the ringing waveform, along with information that allows interpretation of the settings of the on-board dual in-line package (DIP) selection switches. Based on the switch settings, the microcontroller sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. The DAC produces a low voltage sinusoidal waveform to the ring signal amplifier. This low voltage sinusoidal waveform is the right frequency and reference amplitude. The reference amplitude includes dc offset. The microcontroller provides additional information like zero-crossing detect (XOVER) and subcycle cadence information (AF0 and AF1).

Ring-signal amplifier

The ringing signal from the ring-signal generator is fed into a class D amplifier circuit. This circuit modulates the pulse width to a full-bridge switch configuration. This configuration switches the high voltage supply that floats alternately to ground on one side for each half cycle of the output waveform. This process creates a train of variable width pulses. The filtered pulses produce the necessary sinusoidal ringing output voltage and dc offset. The sinusoidal ringing output voltage and dc offset is fed out of the ringing generator. A sample of the filtered output is compared to the input reference signal from the ring-signal generator circuit. This comparison is used to regulate the ringing output.

Output monitors

These circuits monitor the ringing output for ac over- and undervoltage. The circuits also monitor the dc-offset for over- and undervoltage. When an overvoltage condition occurs, the system disables the ringing amplifier. When an undervoltage condition occurs, the current must be less than the current limit point to allow shutdown. These circuits also monitor the output current of the card and send a signal to the system when the load current exceeds approximately ninety percent of its rating. When the load current exceeds the rated load current, the card goes into current limit and the output voltage decreases. The card does not shut down, but continues to try to support the load. If the overload condition is removed, the output voltage is automatically restored to its expected level.

The monitor circuits provide electrically isolated transistor-transistor logic (TTL) level signals to the LCM processor. These signals indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the line concentrating module synchronizes all dc-dc converters and the ringing amplifier on this card. The phase-lock loop synchronizes dc-dc converters and the ringing amplifier at an integer multiple of 8 kHz. The system electrically isolates this synchronization from the clock signal that the LCM provides. The system isolates this synchronization between the various converters on this card.

Signaling

Pin numbers

Pin number information for the NT6X30GB finger connector (P1) appears in the following table.

NT6X30GB (continued)

NT6X30GB pin numbers

Pin	Signal	Pin	Signal
1	AF0	19	-48 V
2	LOGIC GND	20	BR
3	AF1	21	LEDPOWER
4	LOGIC GND	22	FSPMON
5	ACT	23	LOGIC GND
6	LOGIC GND	24	SYNC 64
7	XOVER	25	RRING
8	LOGIC GND	26	RTIP
9	RMS	27	RRING
10	LOGIC GND	28	RTIP
11	CUR	29	NC
12	LOGIC GND	30	ABSBR
13	LOGIC GND	31	NC
14	FSPLINK	32	NC
15	-48 V	33	NC
16	BR	34	NC
17	-48 V	35	NC
18	BR	36	NC

Technical data

Information on NT6X30GB voltages appears in the following table.

Power requirements

The NT6X30GB requires -39.5 V to -75 V, and a nominal current of 2 A to a maximum of 3 A. The NT6X30GB consumes 100 W of power.

NT6X30GB European ring codes

	Voltage		Frequency (Hz)	Subcycle cadence (seconds)	Switch (SW1-4)	Setting 12345678
	ac	dc				
Austria	65	-60	50	2 2 1 1	1 to 4	10000110
Belgium	75	-52	25	0.76 0.76 1 1.48	1 to 4	10000011
Europe (includes Finland, Italy, Luxembourg, Netherlands, Russia)	75	-52	25	1.64 1.64 0.64 1.08	1 to 4	10000000
France/ Slovakia	75	-52	50	1.66 1.66 0.84 0.84	1 to 4	10000010
Germany	65	-60	25	2 2 1 1	1 to 4	01111111
Portugal/ Iceland/ Sweden	75	-52	25	2 2 1 1	1 to 4	10000101
Spain	75	-52	25	1.52 1.52 0.92 0.52	1 to 4	10000100
Switzerland/ Norway/ Czech Republic	70	-52	25	1.64 1.64 0.64 1.08	1 to 4	10000001
UK and Ireland	75	-52	25	1 1 0.4 0.6	1 to 4	01110110

Note: The interpretation of the symbols under the heading settings is 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.

NT6X30HA

Product description

The NT6X30HA ringing generator is a low profile horizontal mount version of the ringing generator. The NT6X30HA is for the North American market. The NT6X30HA contains one card. This card provides all the required functionality.

Location

The NT6X30HA mounts in the cabinetized DMS-100 product above the modular supervisory panel (MSP). The MSP is part of the cabinetized line concentrating equipment (CLCE) frame.

Functional description

The NT6X30HA generates ringing signals and the dc voltages that the automatic number identification (ANI) and coin functions require. Operating company personnel use the four dual inline package (DIP) switches to manually set the ring output frequency and amplitude during installation. This action complies with the North American requirements.

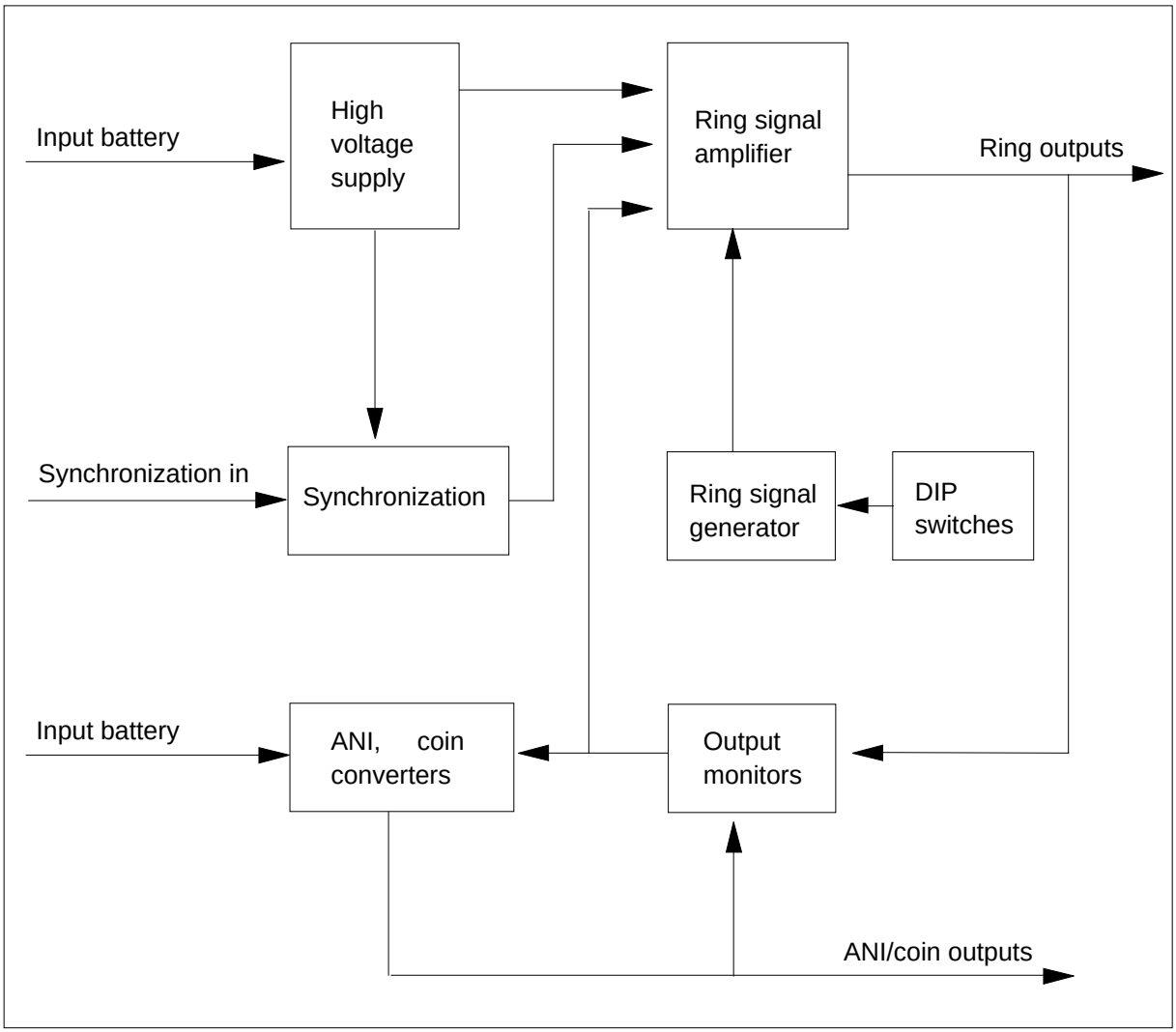
Functional blocks

The NT6X30HA generator has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- ANI, coin converters
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X30HA functional blocks



High voltage supply

The raw battery input voltage (-48V) is filtered and fed to a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of a flyback transformer. The secondary of the flyback transformer is rectified and filtered to produce a regulated floating 300V supply. An isolated output produces the voltages that the ringing control and the monitor circuits require for power.

NT6X30HA (continued)

Ring signal generator

A digital image of the ringing waveform is in the programmable read-only memory (PROM) of the microcontroller of the card. The microcontroller responds to the DIP switch settings. The microcontroller sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. The DAC produces a low voltage sinusoidal waveform of the right frequency and reference amplitude to the ring signal amplifier. This waveform includes dc offset. The microcontroller provides additional information like zero-crossing detect (XOVER) and subcycle cadence information (AF0 and AF1).

Ring signal amplifier

The ringing signal from the ring signal generator feeds to a class D amplifier circuit. This circuit modulates the pulse width to a full-bridge switch configuration. This configuration switches the high voltage floating supply alternately to ground on one side for each half cycle of the output waveform. This process creates a train of variable width pulses. The filtered pulses produce the required sinusoidal ringing output voltage and dc-offset. The sinusoidal ringing output voltage and dc-offset is fed out of the ringing generator. Comparison of a sample of the filtered output to the input reference signal from the ring signal generator circuit regulates this output.

ANI, coin converters

One single-transistor isolated flyback converter provides dc outputs. The ANI feature and the coin feature require the dc outputs. Another converter provides the dc outputs for the coin feature. Linear post-regulators regulate these outputs.

Output monitors

The output monitors check the ringing output and dc-offset for ac overvoltage and undervoltage. Detection of an overvoltage disables the amplifier. If the output monitors detect an undervoltage, the current must be less than the current limit point to allow shutdown.

The output monitors monitor the ANI/Coin outputs for over- and undervoltage conditions. Detection of an overvoltage condition disables the correct converter. If the monitor circuits detect an undervoltage condition, the system raises an alarm. The complete card only shuts down if the ringing output is low.

The monitor circuits provide electrically isolated transistor-transistor logic (TTL) level signals to the LCM processor. The TTL level signals indicate the following:

- low ringing voltage (RMS-bit)
- excess ringing output current (CUR-bit)
- ANI/Coin status (ACT-bit)

Synchronization

A phase-lock loop to the clock frequency of the LCM synchronizes all the dc-dc converters. This loop synchronizes the ringing amplifier on this card. The phase-lock loop uses an integer multiple of 8 kHz to synchronize the converters and ringing amplifier. This synchronization is electrically isolated from the clock signal that the LCM provides. This synchronization is isolated between the different converters on this card.

Technical data

Information about NT6X30HA ringing appears in the following table.

Ringing type applications that use NT6X30HA (Sheet 1 of 3)

Ring type	User	Switches	Table	Line
Coded ringing	Bell Canada U.S. Bell operating companies (BOC)			
• 20 Hz		1-4	"NT6X30HA coded ringing"	1, 4, 5, 6
• 30 Hz		1-4		2, 3, 4
Superimposed ringing	BOC (U.S.)			
• BCS15 or earlier		1 & 2	"NT6X30HA superimposed ringing"	1
		3 & 4		2
• BCS16 and later (non-revertive)		1 & 2	"NT6X30HA superimposed ringing"	3
		3 & 4		4
Note: Do not change DIP switch setting while power is ON. Set the correct circuit breaker on the NT6S35 FSP to OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.				

NT6X30HA (continued)

Ringing type applications that use NT6X30HA (Sheet 2 of 3)

Ring type	User	Switches	Table	Line
• BCS16 and later (revertive)		1 & 2 3 & 4	"NT6X30HA superimposed ringing"	5 6
Superimposed ringing	Rural Electrification Administration (REA)			
• BCS16 and later (non-revertive)		1 & 2 3 & 4	"NT6X30HA superimposed ringing"	9 10
• BCS16 and later (revertive)		1 & 2 3 & 4	"NT6X30HA superimposed ringing"	7 8
Frequency selective ringing				
• Synchromonic	BOC (U.S.)		"NT6X30HA synchromonic ringing (BOC)"	
• Harmonic	BOC (U.S.)		"NT6X30HA harmonic ringing (BOC)"	
• Decimonic	BOC (U.S.)		"NT6X30HA decimonic ringing (BOC)"	
• Synchromonic	REA		"NT6X30HA synchromonic ringing (REA)"	
• Harmonic	REA		"NT6X30HA harmonic ringing (REA)"	

Note: Do not change DIP switch setting while power is ON. Set the correct circuit breaker on the NT6S35 FSP to OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.

Ringing type applications that use NT6X30HA (Sheet 3 of 3)

Ring type	User	Switches	Table	Line
• Decimonic	REA		"NT6X30HA decimonic ringing (REA)"	
	International	1-4	"NT6X30HA international ringing"	
	Japan	1-4	"NT6X30HA international ringing"	
	U.K.	1-4	"NT6X30HA international ringing"	

Note: Do not change DIP switch setting while power is ON. Set the correct circuit breaker on the NT6S35 FSP to OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.

NT6X30HA coded ringing

	Voltage		Freq		Switch	Setting
Line	**ac**	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
1	86	-52	20	2 2 1 1	1 to 4	00000000
2	110	-52	30	2 2 1 1	1 to 4	01010100
3	120	-52	30	2 2 1 1	1 to 4	00110100
4	90	-52	20	2 2 1 1	1 to 4	00011000
5	110	-52	20	2 2 1 1	1 to 4	01011000
6	120	-52	20	2 2 1 1	1 to 4	00111000

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA (continued)

NT6X30HA superimposed ringing

	Voltage		Freq		Switch	Setting
Line	**ac**	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
1	86	-38	20	2 2 1 1	1 & 2	01000000
2	86	+38	20	2 2 1 1	3 & 4	00100000
3	86	-38	20	2 2 1 1	1 & 2	00011110
4	86	+38	20	2 2 1 1	3 & 4	01011110
5	86	-52	20	1.84 1.84 1.84 0.48	1 & 2	10011110
6	86	+52	20	1.84 1.84 1.84 0.48	3 & 4	11011110
7	105	-52	20	1.84 1.84 1.84 0.48	1 & 2	11101100
8	105	+52	20	1.84 1.84 1.84 0.48	3 & 4	11100010
9	105	-52	20	2 2 1 1	1 & 2	01101100
10	105	+52	20	2 2 1 1	3 & 4	01100010

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA synchromonic ringing (BOC) (Sheet 1 of 2)

	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	16	2 2 1 1	1	00010000
	90	-52	20	2 2 1 1	1	00011000
	95	-52	30	2 2 1 1	2	00010100
	100	-52	42	2 2 1 1	3	00000010
	110	-52	54	2 2 1 1	4	00001010
	125	-52	66	2 2 1 1	opt	00000110

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA synchromonic ringing (BOC) (Sheet 2 of 2)

	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Med	105	-52	16	2 2 1 1	1	01010000
	105	-52	20	2 2 1 1	1	01011000
	110	-52	30	2 2 1 1	2	01010100
	115	-52	42	2 2 1 1	3	01000010
	125	-52	54	2 2 1 1	4	01001010
	140	-52	66	2 2 1 1	opt	01000110
High	120	-52	16	2 2 1 1	1	00110000
	120	-52	20	2 2 1 1	1	00111000
	120	-52	30	2 2 1 1	2	00110100
	130	-52	42	2 2 1 1	3	00100010
	140	-52	54	2 2 1 1	4	00101010
	145	-52	66	2 2 1 1	opt	00100110

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA decimonic ringing (BOC) (Sheet 1 of 2)

	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	20	2 2 1 1	1	00011000
	95	-52	30	2 2 1 1	2	00010100
	100	-52	40	2 2 1 1	3	00011100
	110	-52	50	2 2 1 1	4	00010010

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA (continued)

NT6X30HA decimonic ringing (BOC) (Sheet 2 of 2)

	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
	125	-52	60	2 2 1 1	opt	00011010
Med	105	-52	20	2 2 1 1	1	01011000
	110	-52	30	2 2 1 1	2	01010100
	115	-52	40	2 2 1 1	3	01011100
	125	-52	50	2 2 1 1	4	01010010
	140	-52	60	2 2 1 1	opt	01011010
High	120	-52	20	2 2 1 1	1	00111000
	120	-52	30	2 2 1 1	2	00110100
	130	-52	40	2 2 1 1	3	00111100
	140	-52	50	2 2 1 1	4	00110010
	145	-52	60	2 2 1 1	opt	00111010

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA synchromonic ringing (REA) (Sheet 1 of 2)

	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	16	1.95 1.35 1.35 1.35	1	10010000
	90	-52	20	1.95 1.35 1.35 1.35	1	10011000
	95	-52	30	1.95 1.35 1.35 1.35	2	10010100
	100	-52	42	1.95 1.35 1.35 1.35	3	10000010
	110	-52	54	1.95 1.35 1.35 1.35	4	10001010

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA synchromonic ringing (REA) (Sheet 2 of 2)

	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
	125	-52	66	1.95 1.35 1.35 1.35	opt	10000110
Med	105	-52	16	1.95 1.35 1.35 1.35	1	11010000
	105	-52	20	1.95 1.35 1.35 1.35	1	11011000
	110	-52	30	1.95 1.35 1.35 1.35	2	11010100
	115	-52	42	1.95 1.35 1.35 1.35	3	11000010
	125	-52	54	1.95 1.35 1.35 1.35	4	11001010
	140	-52	66	1.95 1.35 1.35 1.35	opt	11000110
High	120	-52	16	1.95 1.35 1.35 1.35	1	10110000
	120	-52	20	1.95 1.35 1.35 1.35	1	10111000
	120	-52	30	1.95 1.35 1.35 1.35	2	10110100
	130	-52	42	1.95 1.35 1.35 1.35	3	10100010
	140	-52	54	1.95 1.35 1.35 1.35	4	10101010
	145	-52	66	1.95 1.35 1.35 1.35	opt	10100110

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA harmonic ringing (REA) (Sheet 1 of 2)

	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	16-2/3	1.95 1.35 1.35 1.35	1	10001000
	95	-52	25	1.95 1.35 1.35 1.35	2	10000100
	100	-52	33-1/3	1.95 1.35 1.35 1.35	3	10001100

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA (continued)

NT6X30HA harmonic ringing (REA) (Sheet 2 of 2)

	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
	110	-52	50	1.95 1.35 1.35 1.35	4	10010010
	125	-52	66-2/3	1.95 1.35 1.35 1.35	opt	10010110
Med	105	-52	16-2/3	1.95 1.35 1.35 1.35	1	11001000
	110	-52	25	1.95 1.35 1.35 1.35	2	11000100
	115	-52	33-1/3	1.95 1.35 1.35 1.35	3	11001100
	125	-52	50	1.95 1.35 1.35 1.35	4	11010010
	140	-52	66-2/3	1.95 1.35 1.35 1.35	opt	11010110
High	120	-52	16-2/3	1.95 1.35 1.35 1.35	1	10101000
	120	-52	25	1.95 1.35 1.35 1.35	2	10100100
	130	-52	33-1/3	1.95 1.35 1.35 1.35	3	10101100
	140	-52	50	1.95 1.35 1.35 1.35	4	10110010
	145	-52	66-2/3	1.95 1.35 1.35 1.35	opt	10110110

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA decimonic ringing (REA) (Sheet 1 of 2)

	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	20	1.95 1.35 1.35 1.35	1	10011000
	95	-52	30	1.95 1.35 1.35 1.35	2	10010100
	100	-52	40	1.95 1.35 1.35 1.35	3	10011100
	110	-52	50	1.95 1.35 1.35 1.35	4	10010010

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA decimonic ringing (REA) (Sheet 2 of 2)

	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
	125	-52	60	1.95 1.35 1.35 1.35	opt	10011010
Med	105	-52	20	1.95 1.35 1.35 1.35	1	11011000
	110	-52	30	1.95 1.35 1.35 1.35	2	11010100
	115	-52	40	1.95 1.35 1.35 1.35	3	11011100
	125	-52	50	1.95 1.35 1.35 1.35	4	11010010
	140	-52	60	1.95 1.35 1.35 1.35	opt	11011010
High	120	-52	20	1.95 1.35 1.35 1.35	1	10111000
	120	-52	30	1.95 1.35 1.35 1.35	2	10110100
	130	-52	40	1.95 1.35 1.35 1.35	3	10111100
	140	-52	50	1.95 1.35 1.35 1.35	4	10110010
	145	-52	60	1.95 1.35 1.35 1.35	opt	10111010

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA international ringing (Sheet 1 of 2)

	Voltage		Freq		Switch	Setting
Line	**ac**	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	67	-52	25	1.95 1.35 1.35 1.35	1 to 4	10001110
Med	75	-52	25	1.95 1.35 1.35 1.35	1 to 4	11001110
High	82	-52	25	1.95 1.35 1.35 1.35	1 to 4	10101110
Low	67	-52	25	2 2 1 1	1 to 4	00001110
Med	75	-52	25	2 2 1 1	1 to 4	01001110

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Use the switch settings for Japan only for Japanese ringing.

NT6X30HA (continued)

NT6X30HA international ringing (Sheet 2 of 2)

	Voltage		Freq		Switch	Setting
Line	**ac**	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
High	82	-52	25	2 2 1 1	1 to 4	00101110
Japan	75	0	16	2 2 1 1	1 to 4	11101110
U.K.	75	-52	25	1 1 0.4 0.6	1 to 4	01101110

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Use the switch settings for Japan only for Japanese ringing.

NT6X30HA harmonic ringing (BOC) (Sheet 1 of 2)

	Voltage		Freq		Switch	Setting
	ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	16-2/3	2 2 1 1	1	00001000
	95	-52	25	2 2 1 1	2	00000100
	100	-52	33-1/3	2 2 1 1	3	00001100
	110	-52	50	2 2 1 1	4	00010010
	125	-52	66-2/3	2 2 1 1	opt	00010110
Med	105	-52	16-2/3	2 2 1 1	1	01001000
	110	-52	25	2 2 1 1	2	01000100
	115	-52	33-1/3	2 2 1 1	3	01001100
	125	-52	50	2 2 1 1	4	01010010
	140	-52	66-2/3	2 2 1 1	opt	01010110
High	120	-52	16-2/3	2 2 1 1	1	00101000
	120	-52	25	2 2 1 1	2	00100100
	130	-52	33-1/3	2 2 1 1	3	00101100

Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.

NT6X30HA harmonic ringing (BOC) (Sheet 2 of 2)

Voltage		Freq		Switch	Setting
ac	**dc**	**(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
140	-52	50	2 2 1 1	4	00110010
145	-52	66-2/3	2 2 1 1	opt	00110110
Note: The symbols under the heading settings are interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON directions. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight secstion set to OFF.					

Information about NT6X30HA tolerances appears in the following tables.

NT6X30HA frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
16 to 33-.33 Hz	±.33 Hz
40 to 66-.66 Hz	±1%
25 Hz international	±.33 Hz
-52V (dc)	-49.75 to -52.5V (dc)
-38V (dc)	±2V (dc)
+38V (dc)	±2V (dc)

NT6X30HA ac voltage tolerances (Sheet 1 of 2)

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8
100	97	103
105	101.9	108.1

NT6X30HA (continued)

NT6X30HA ac voltage tolerances (Sheet 2 of 2)

Nominal	Low	High
110	106.7	113.3
115	111.6	118.4
120	116.4	123.6
125	121.2	128.7
130	126.1	133.9
140	135.8	144.2
145	140.7	149.3

Information about ANI and coin voltages appears in the following table.

NT6X30HA ANI and coin voltages

Output	Limits
+48V	+52, ±2.5V
-48V	-52, ±2.5V
+130V	+130, ±5V
-130V	-130V, ±5V

Signaling

Pin numbers

Pin number information for the NT6X30HA finger connector (P1) appears in the following table.

NT6X30HA pin numbers (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	AF0	19	-48V
2	LOGIC GND	20	BR
3	AF1	21	ABS-48
4	LOGIC GND	22	FSPMON
5	ACT	23	LOGIC GND

NT6X30HA pin numbers (Sheet 2 of 2)

Pin	Signal	Pin	Signal
6	LOGIC GND	24	SYNC 64
7	XOVER	25	RRING
8	LOGIC GND	26	RTIP
9	RMS	27	RRING
10	LOGIC GND	28	RTIP
11	CUR	29	-52V
12	LOGIC GND	30	ABS BR
13	LOGIC GND	31	
14	FSPLINK	32	+52V
15	-48V	33	
16	BR	34	-130V
17	-48V	35	Fuse Alarm
18	BR	36	+130V

Power requirements

The NT6X30HA requires -39.5V to -75V. The nominally requires 2.5A, to a maximum of 4A. The NT6X30HA uses 140W of power.

NT6X30JA

Product description

The NT6X30JA ringing generator is a low profile horizontal mount version of the ringing generator. The NT6X30JA is for the Japanese market. The NT6X30JA contains a single card. This card provides all the required functionality.

Location

The NT6X30JA fits in the cabinetized DMS-100 product above the modular supervisory panel (MSP). The MSP is part of the cabinetized line concentrating equipment (CLCE) frame.

Functional description

The NT6X30JA generates ringing signal voltages. Operating company personnel use the four dual inline package (DIP) switches to set the ring output frequency and amplitude during installation. This setting complies with Japanese requirements.

Functional blocks

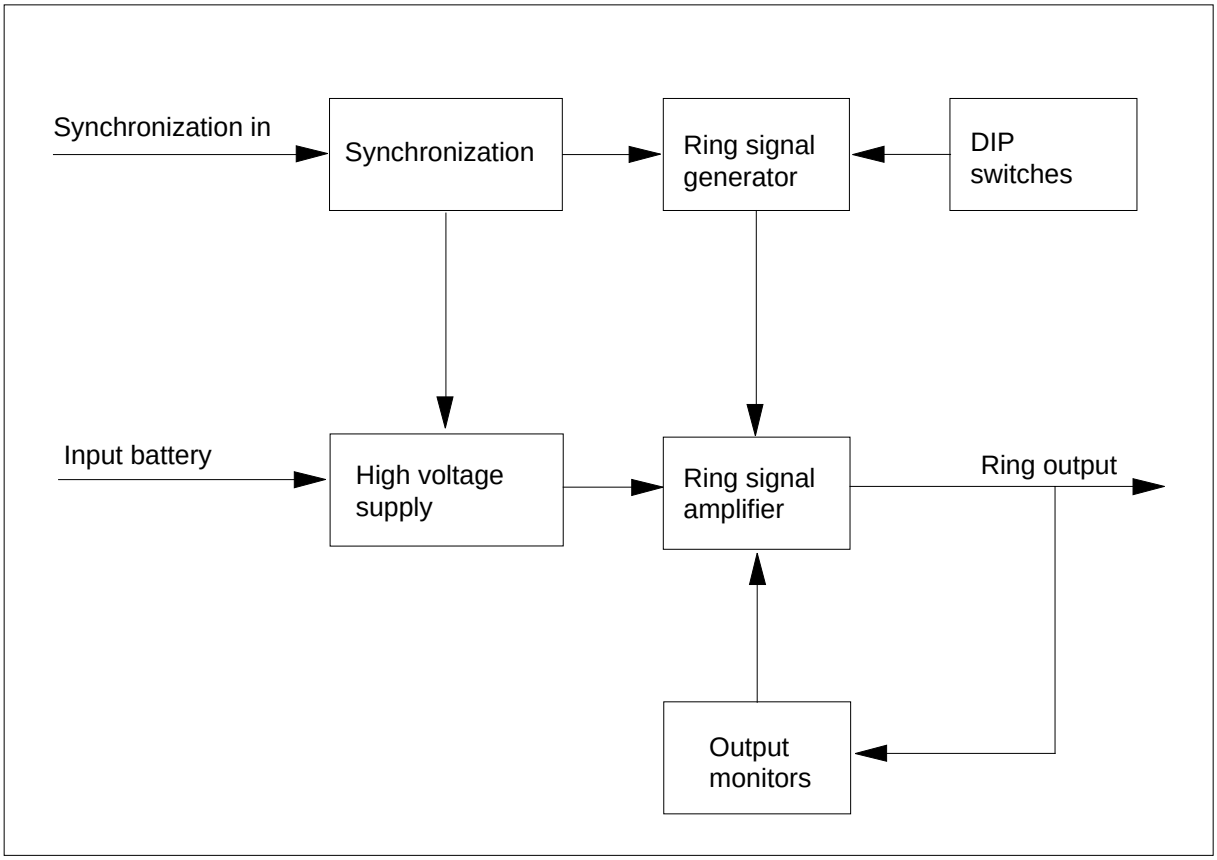
The ringing signal is ground backed or centered about ground. The input battery provides the dc-offset through a fuse for this market. The dc-offset is applied to the tip side of the bus.

The NT6X30JA generator has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X30JA functional blocks



High voltage supply

The raw battery input voltage (-48 V) is filtered and fed to a single-transistor isolated boost converter topology. This action switches the input voltage to a square wave across the primary of a flyback transformer. The secondary is rectified and filtered to produce a regulated floating 300-V supply. An isolated output produces the voltages required to power the ringing control and monitor circuits.

Ring signal generator

A digital image of the ringing waveform is in the programmable read-only memory (PROM) of the microcontroller of the card. The microcontroller responds to the DIP switch settings on the card. The microcontroller sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. This information produces a low voltage sinusoidal waveform of the right frequency and reference amplitude to the ring signal amplifier. The reference amplitude includes dc offset. The microcontroller provides

NT6X30JA (continued)

additional information like zero-crossing detect (XOVER) and subcycle cadence information (AF0 and AF1).

Ring signal amplifier

The ringing signal from the ring signal generator is fed to a class D amplifier circuit. The class D amplifier circuit modulates the pulse width to a full bridge switch configuration. This configuration switches the high voltage floating supply alternately to ground on one side. The configuration performs this procedure for each half cycle of the output waveform. This action creates a train of variable width pulses. The filtered pulses produce the required sinusoidal ringing output voltage and dc-offset. The sinusoidal ringing output voltage and dc-offset is fed out of the ring generator. Comparison of a sample of the filtered output to the input reference signal from the ring signal generator circuit regulates this output.

Output monitors

The output monitors monitor the ringing output for ac overvoltage and undervoltage. The output monitors monitor the dc-offset for overvoltage and undervoltage. When undervoltage occurs, the current must be less than the current limit point to allow shutdown.

The monitor circuits provide electrically isolated transistor-to-transistor logic (TTL) level signals to the (LCM) processor. The TTL level signals indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the LCM synchronizes all the dc-dc converters on this card. This loop synchronizes the ringing amplifier on this card. The phase-lock loop uses an integer multiple of 8 kHz for synchronization. This synchronization is electrically isolated from the clock signal that the LCM provides. This synchronization is isolated between the different converters on this card.

Signaling

Pin numbers

The pin numbers for the NT6X30JA appear in the following table.

Pin numbers for the NT6X30JA (P1 connector) (Sheet 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	AF0	10	LOGICGND	19	-48V	28	RTIP
2	LOGICGND	11	CUR	20	BR	29	(N/C)

Pin numbers for the NT6X30JA (P1 connector) (Sheet 2 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
3	AF1	12	LOGICGND	21	ABS-48	30	ABSBR
4	LOGICGND	13	LOGICGND	22	FSPMON	31	N/C
5	ACT	14	FSPLINK	23	LOGICGND	32	(N/C)
6	LOGICGND	15	-48V	24	SYNC64	33	N/C
7	XOVER	16	BR	25	RRING	34	(N/C)
8	LOGICGND	17	-48V	26	RTIP	35	Fuse Alarm
9	RMS	18	BR	27	RRING	36	(N/C)

Technical data

The card has an output of 16 Hz, with an amplitude of 76 V (rms). The correct setting of the DIP switches is 01110111.

The ringing characteristics and DIP switch setting for the appear in the following table.

NT6X30JA Japan ringing characteristics and switch settings

Voltage AC DC offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
76 0	16	2 2 1 1	1 to 4	11101110
Note: The symbols under the heading settings ar interpreted as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Pull the ringing generator card completely from the shelf to change DIP switch settings.				

Information about voltages appears in the following tables.

NT6X30JA Japan frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
16 Hz	+ or - 1 Hz
0V (dc)	+ or - 2V (dc)
-48V (dc)	+ or - 2V (dc)

NT6X30JA (end)

NT6X30JA Japan ac voltage tolerances

Nominal	Low	High
76	69	83

Power requirements

The NT6X30JA requires -39.5V to -75V. The NT6X30JA requires a nominal current of 1 A, to a maximum of 2 A. The card uses 75W of power.

NT6X31AA

Product description

The NT6X31AA provides signaling terminals (ST) for Common Channel Signaling 7 (CCS7) applications.

The NT6X31AA message signaling 7 frame contains one NT6X32AA message switch and buffer 7 module (MSB7). The NT6X31AA contains one NT6X08AA signaling terminal 7 group shelf (ST7G).

Two NT6X3201 shelves in the NT6X32AA module contain STs. Each shelf contains a maximum of four STs. The NT6X08AA shelf contains a maximum of 16 STs on each shelf. Each NT6X31AA frame can contain a maximum of 24 STs on each shelf. When more than 24 STs are required, the system must use the NT6X09AA signaling terminal 7 extension frame. The system must use the NT6X31AA.

Parts

The NT6X31AA contains the following parts:

- NT0X84AA–Cage filler panel assembly
- NT0X28AP–Frame supervisory panel (FSP)
- NT6X08AA–ST7G
- NT6X32AA–MSB7
- NT6X3201–Signaling terminal 7 array shelf assemblies (ST7A)
- NT3X90AA–Cooling inverter unit (provisionable)
- NT3X90AB–Cooling inverter unit (provisionable)
- NT3X90AC–DC fan cooling unit (provisionable)

Cage filler panel assembly

The NT0X84AA cage filler panel assembly fills in the shelf position 65 that the system does not use.

Frame supervisory panel

The NT0X28AP FSP contains two NT0X91AE converter drive and protection circuits and one NT0X91AA alarm and converter drive circuit. The circuits monitor and control the power supply to the NT6X31AA frame from the power distribution center (PDC) in the DMS-100 system.

The NT0X28AP FSP conveys the required potential from the office battery, -48V nominal. The NT0X28AP FSP uses six circuit breakers to protect the power control and alarm circuits to the shelves in the NT6X31AA. Some

NT6X31AA (continued)

NT0X28 models use fuses to protect the power control. Some NT0X28 models require two or three power feeds.

The NT0X28AP has a feature called a mechanical interlock. This feature consists of a small cover that slides. This cover allows access to only two of the circuit breakers (CB) at a time. The cover allows access to the following pairs of circuit breakers:

- CB1 and CB2
- CB3 and CB4
- CB5 and CB6

If all six circuit breakers are ON, accidental tripping of circuit breakers in other groups cannot occur.

The following pairs of CBs serve an shelf:

- CB1 and CB4 to shelf 51
- CB5 and CB6 to shelf 32
- CB2 and CB3 to shelf 18

Fuses have circuits in the NT0X28AP.

Signaling terminal 7 group shelf

The NT6X08AA signaling terminal 7 group shelf provides a maximum of 16 ST. This shelf is on the NT6X08AA in the NT6X31AA frame at shelf position 51.

The STs in the NT6X08AA are added to the 16 STs in the associated NT6X06AB message switching 6 equipment frame or NT6X31AA frame.

Message switch and buffer 7 module

The NT6X32AA is a dual shelf peripheral module (PM) that consists of two NT6X3201 ST7A.

The NT6X32AA is based on the line trunk controller (LTC) hardware and architecture. The NT6X32AA performs the following tasks:

- provides and maintains a path from the CCS7 digital signaling data link. The card switches the CCS7 digital signaling data link through the network nailed-up connection to the CCS7 ST.
- performs the message switching and distribution function between the digital trunk controllers (DTC) and the correct STs

The STs are on the two NT6X3201 shelves in the NT6X32AA module. Each shelf contains a maximum of four STs. The STs are on the NT6X08AA shelf. Each shelf contains a maximum of 16 STs.

Cooling inverter unit

The NT3X90AA uses fans to provide forced-air cooling for the NT6X09AA frame. The NT3X90AA includes a built-in inverter to provide ac power to the fans. The NT3X90AA uses the -48V dc battery supply.

Cooling inverter unit

The NT3X90AB uses fans to provide forced-air cooling for the NT6X09AA frame. The NT3X90AA includes a built-in inverter to provide ac power to the fans. The NT3X90AB uses the -48V dc battery supply.

DC fan cooling unit

The NT3X90AC dc cooling unit contains five-fan assemblies that maintain a normal five-shelf cabinet. Two feeders in the PDC supply dc power to the fans at 48V. Each feeder is fused at 5 A.

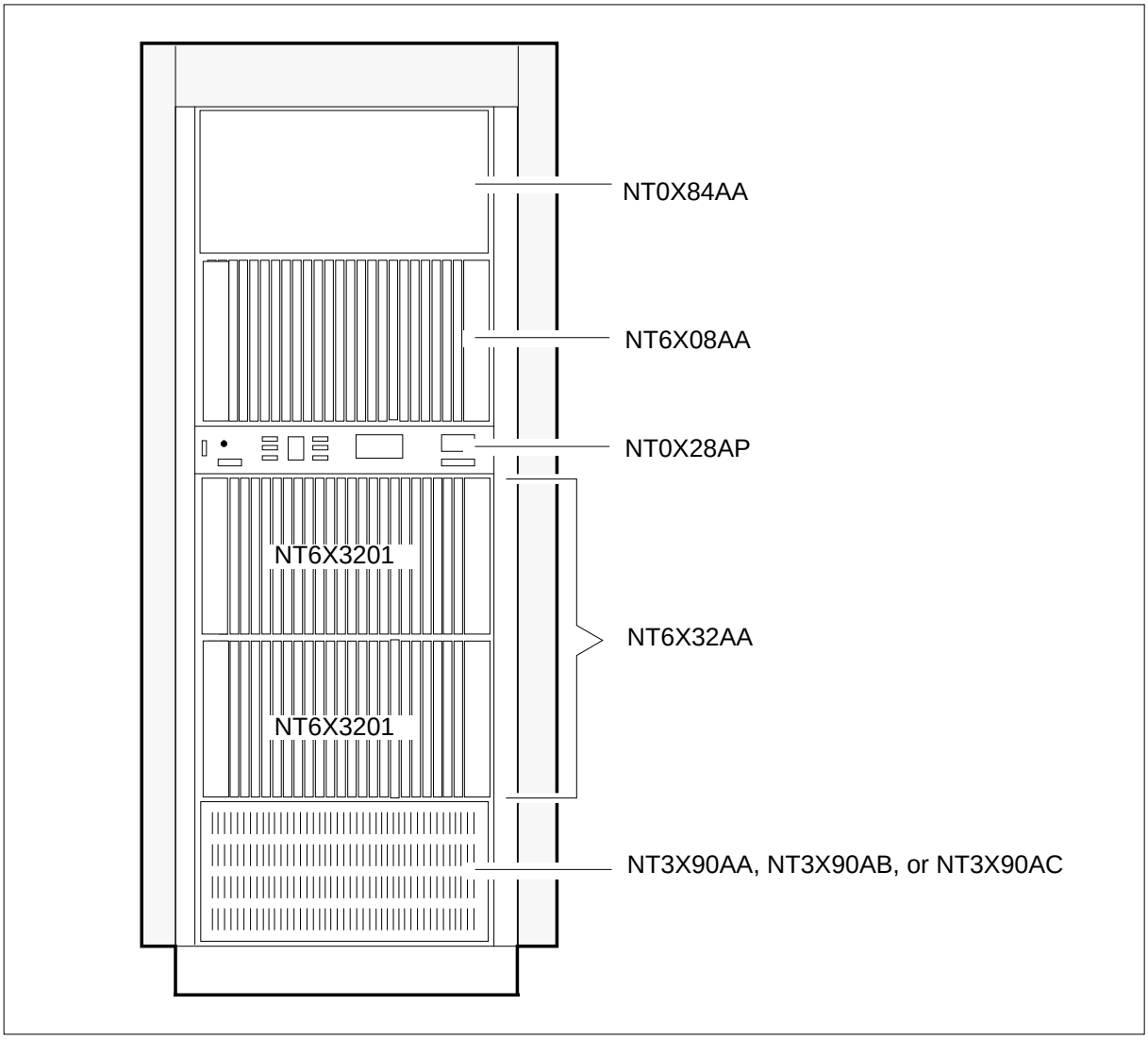
The NT3X90AC cooling unit uses a single-fan failure detection and signaling system. The multiple-fan design contains redundancy. Redundancy allows a single-fan failure to occur without critical loss of cooling air.

Design

The design of the NT6X31AA appears in the following figure.

NT6X31AA (end)

NT6X31AA parts



Note: This figure is not drawn to scale.

NT6X32AA

Product description

The NT6X32AA is a dual shelf peripheral module (PM) that contains two NT6X3201 signaling terminal 7 array shelf assemblies (ST7A). The is in an NT6X31AA message signaling 7 frame at shelf position 18.

The NT6X32AA is based on the line trunk controller (LTC) hardware and architecture. The

performs the following tasks:

- provides and maintains a path from the common channel signaling number 7 (CCS7) digital signaling data link. The PM switches the path through the network nailed-up connection to the CCS7 ST.
- performs the message switching and distribution function between the digital trunk controllers (DTC) and the appropriate STs

The STs are on the two NT6X3201 shelves in the module, a maximum of four for each shelf. The STs are on the NT6X08AA shelf, a maximum of 16 for each shelf.

Parts

The NT6X32AA module contains the following parts:

- NT0X50AA–Filler face plate .875
- NT2X70AE–Power converter, ±5 V/12 V
- NT6X40AB–DS30 network interface circuit pack (CP)
- NT6X41AA–Speech bus formatter CP
- NT6X42AA–Channel supervision message (CSM) CP
- NT6X44AB–Time switch (TS) CP
- NT6X45AF–Line group controller (LGC) DTC processor CP
- NT6X46AB–Signaling processor (SP) memory plus CP
- NT6X47AB–Master processor (MP) memory plus CP
- NT6X48AA–DS30A line concentrating module (LCM) CP
- NT6X66AC–CCS7 ST CP
- NT6X66CA–DPNSS ST CP
- NT6X67AA–ST buffer CP
- NT6X68AC–ST terminal interface CP

NT6X32AA (continued)

- NT6X68AD–ST terminal interface CP
- NT6X69AB–Common peripheral processor (CPP) message protocol and tone CP

Design

The design of the NT6X32AA appears in the following table.

NT6X32AA parts (Sheet 1 of 5)

Card PEC	Slot	Description
NT0X50AA	12, 14, 19, 21 Provisionable: 04-07	*Filler face plate .875* The NT0X50AA filler face plate is used to fill in card slots 12, 14, 19, and 21 and slots 04 to 07. This event occurs when the card slots do not contain the NT6X66AA or NT6X66AC cards.
NT2X70AE	1, 25	*Power converter, ±5V/12V* The NT2X70AE provides a regulated potential of &0xb1;5V or &0xb1;12V to the cards mounted on the NT6X3201 shelf assembly. The NT2X70AE replaces previous NT2X70 power converters.
NT6X40AB	2 4	*DS30 network interface circuit pack* The NT6X40AB provides a central side (C-side) interface for DS30 links to the network. Each port of a DS30 network interface card provides a two-way voice and data interface. Each port contains a looparound circuit for fault isolation.

NT6X32AA (continued)

NT6X32AA parts (Sheet 2 of 5)

Card PEC	Slot	Description
NT6X41AA	2 3	*Speech bus formatter card* The NT6X41AA speech bus formatter contains the clock section and the formatting section. The clock section generates the 10.24-MHz shelf clock. The formatting section of the card provides the following: • parallel-to-serial conversion of the encoded voice signals. The formatting section receives the encoded voice signals from the CSM interface CPs. The signals route to the C-side links. • serial-to-parallel conversion of the encoded voice signals received from the C-side interface cards • network plane selection • parity error generation for test purposes • T1 clock generation.
NT6X42AA	2 2	*Channel supervision message circuit pack* The NT6X42AA CSM CP performs the following functions: • extracts the CSM bit from the C-side channels, assembles the CSM for each channel, and inserts the CSM into the outgoing C-side bytes. • The CSM CP performs parity checks on all incoming bytes and parity generation on all outgoing bytes.

NT6X32AA (continued)

NT6X32AA parts (Sheet 3 of 5)

Card PEC	Slot	Description
NT6X44AB	1 8	*Time switch circuit pack* The NT6X44AB TS CP converts between the serial stream received from, or transmitted to the interface CPs, and the parallel stream. The interface CPs include the DS30, DS30A, or DS-1. The internal speech bus uses the parallel stream. When the SP controls the TS, the TS associates two elements. The TS associates any of the DS30, DS30A, or DS-1 interface CPs with any of the time slots on the parallel speech bus. The TS transfers data between the associated channel and the time slot.
NT6X45AF	11, 16	*LGC/DTC processor* The NT6X45AF processor LGC/DTC runs the programs that control the operation and maintenance of a PM. The NT6X45AF performs digit collection, channel assignment, and interpretation of messages for the central control complex and PM. You must replace the NT6X45AE and NT6X45AF CPs with NT6X45BA and NT6X45BB CPs based on the correct rules in provisioning.
NT6X46AB	1 5	*Signaling processor memory plus circuit pack* The NT6X46AB SP memory plus CP provides RAM to store data and application programming.
NT6X47AB	1 3	*Message processor memory plus circuit pack* The MP memory CP contains RAM and application programs. The RAM contains data, and the application programs apply to both the MP and the NT6X46AB signaling processor SP. The SP uses the SP memory management unit (MMU) to access a part of the MP memory.

NT6X32AA (continued)

NT6X32AA parts (Sheet 4 of 5)

Card PEC	Slot	Description
NT6X48AA	1 7	*DS30A LCM interface circuit pack* The NT6X48AA DS30 LCM interface CP contains two DS-1 ports. Each LGC module can have between one and 10 cards. Each port provides a two-way voice, data, and signaling interface. The NT6X48AA provides the following: • looparound paths for each DS-1 port to allow isolation of faults • transmission of local alarms • detection of remote alarms • detection of error conditions like loss of synchronization, bipolar error and slip
NT6X66AC	Provisionable: 04-07	*CCS7 signaling terminal circuit pack* The CCS7 ST transmits and receives signaling data over the CCS7 transmission links. The CCS7 ST implements the CCS7 level two link protocol and monitors signaling link performance.
NT6X67AA	1 0	*Signaling terminal buffer circuit pack* The NT6X67AA generates and verifies parity on data transmitted between the message switching buffer and the ST controller (STC).
NT6X68AC	09, Provisionable: 08	*Signaling terminal interface circuit pack* The NT6X68AC provides latches for address, data, and control lines to the STC for fault diagnosis and maintenance.

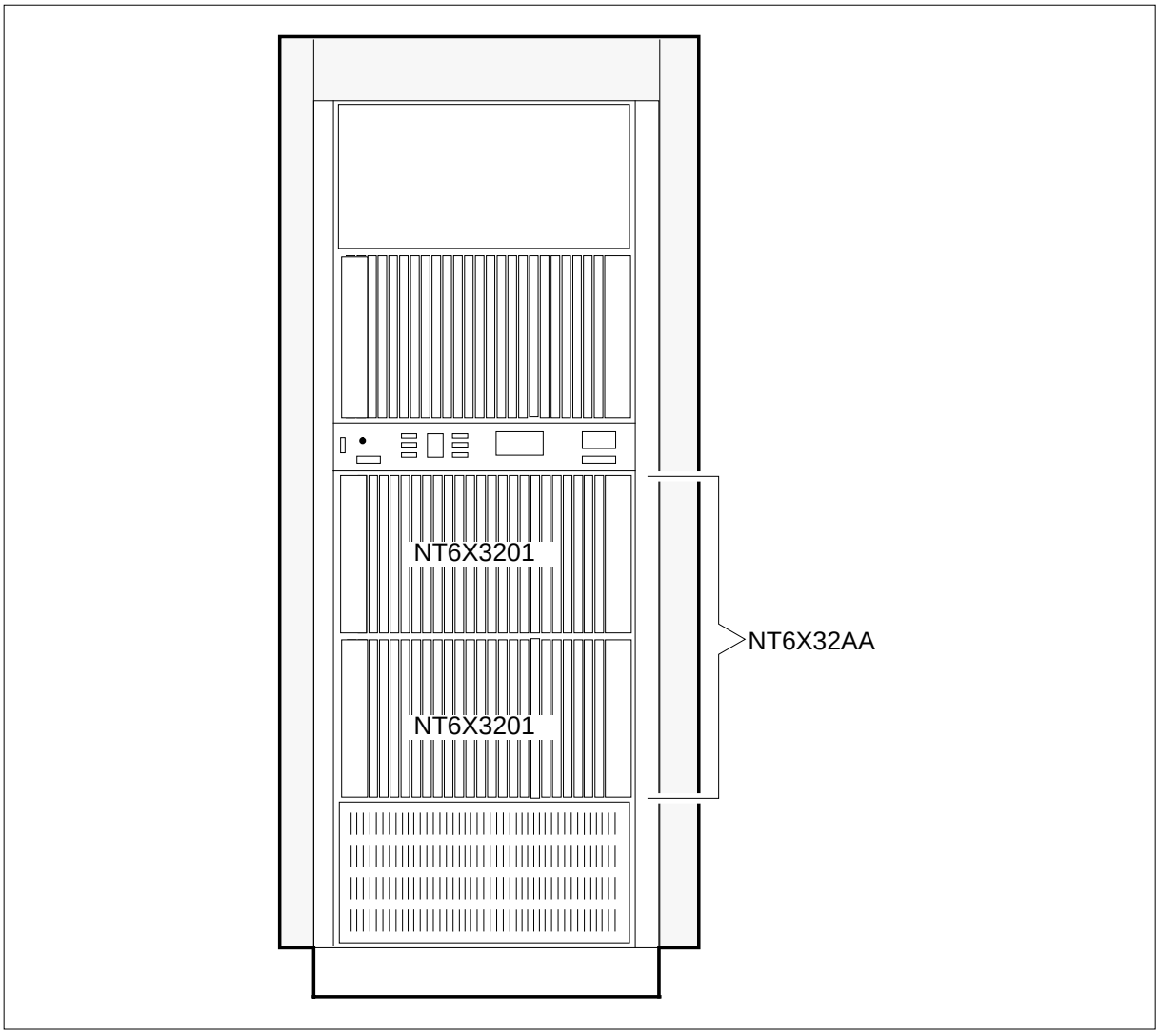
NT6X32AA (continued)

NT6X32AA parts (Sheet 5 of 5)

Card PEC	Slot	Description
NT6X68AD	Provisionable: 08	*Signaling terminal interface with terminator circuit pack* The NT6X68AD provides latches for address, data, and control lines to the STC for fault diagnosis and maintenance. The NT6X68AD contains built-in termination (resistors).
NT6X69AB	2 0	*Common peripheral processor message protocol and tone circuit pack* The NT6X69AB CP interprets and transfers signaling and control messages exchanged between the network and the following PM: • message switch and buffer (MSB) • LGC • line trunk controller • DTC • international DTC • LCM • remote LCM • remote cluster controller (RCC)

The location of the NT6X32AA module in an NT6X31AA frame appears in the following figure.

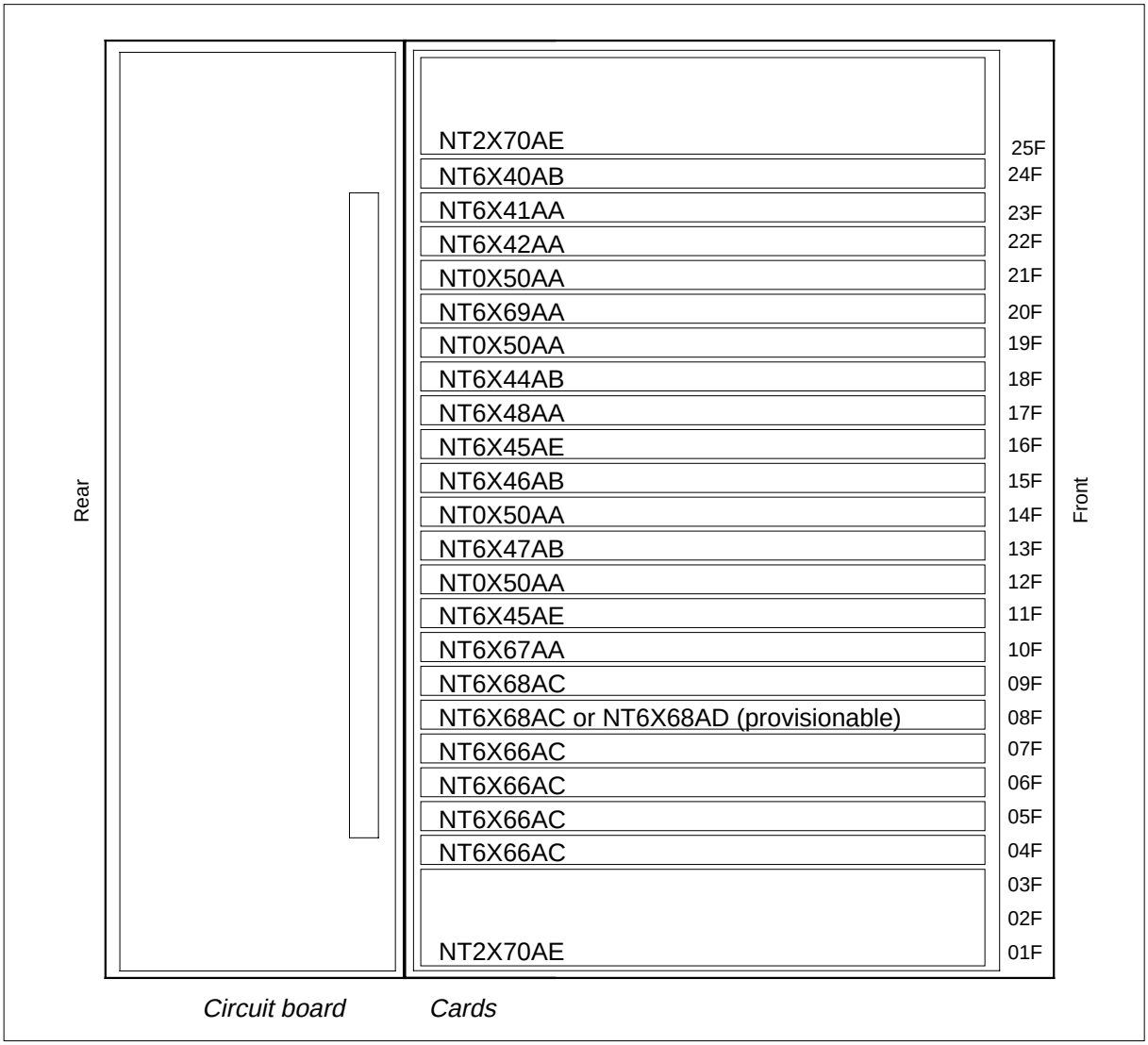
NT6X32AA in the NT6X31AA frame



The design of one of the two shelves that match that make up the NT6X32AA module appears in the following figure.

NT6X32AA (end)

NT6X3201 design



NT6X33AA

Product description

The NT6X33AA DMS10/100 Japan type A general use line (GUL) card is an interface circuit. This interface circuit is for a line concentrating module (LCM) subscriber line. The LCM interface circuit provides a basic plain ordinary telephone service (POTS) interface. The GUL meets the impedance, loss plan, signaling and supervision requirements of DMS10/100 Japan.

The NT6X33AA GUL is compatible with the NT6X05AA LCM drawer and the NT6X54AA bus interface card. This card functions with dial pulse and dual tone multifrequency (DTMF) telephone sets. This card is compatible with A-570001.

The NT6X33AA has the following features:

- synthesized input and balance impedances
- software programmable receive path loss
- loop range of 1700 Ω (loop and set)
- subscriber line interface
- testing features

Location

The NT6X33AA fits in one of the 64 line card slots in an LCM drawer that is in an LCM frame.

Functional description

The NT6X33AA provides a voice and signaling interface. The signaling interface is between a two-wire analog subscriber line and one channel of the switching system. The switching system is a four-wire, 32-channel, 2.56 Mbps bit stream of the DMS family of digital multiplex switching systems.

Functional blocks

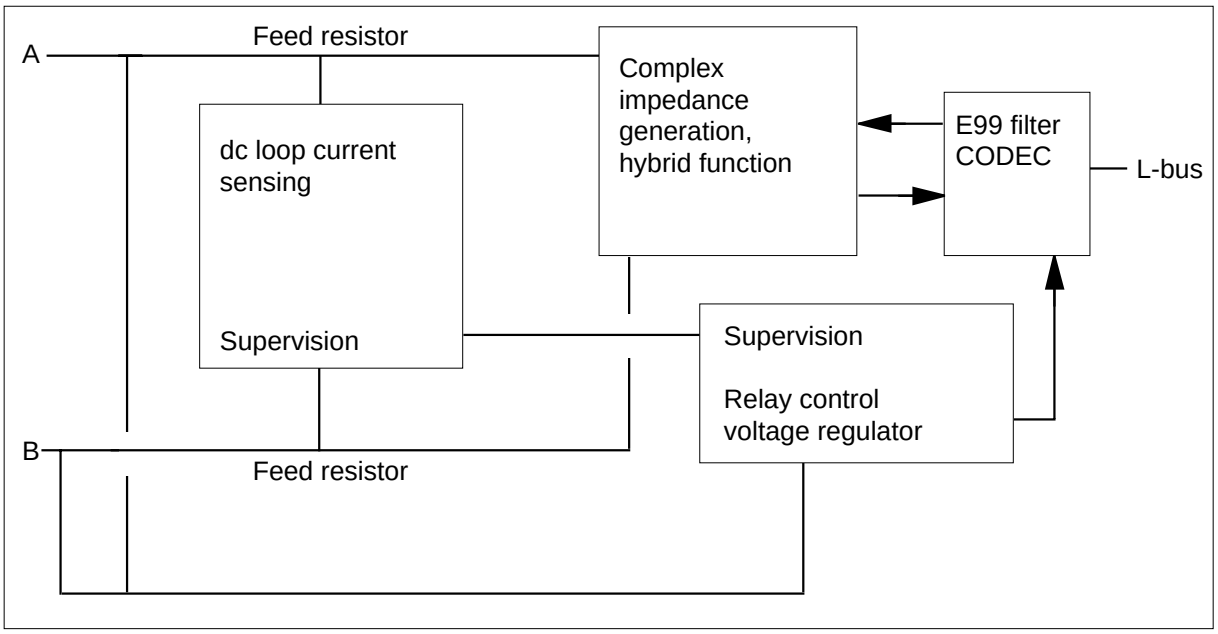
The NT6X33AA has the following functional blocks:

- dc loop current sensing
- complex impedance generation and hybrid function
- coder-decoder (CODEC)
- supervision and relay control and voltage regulator

The relationship between the functional blocks appears in the following figure.

NT6X33AA (continued)

NT6X33AA functional blocks



Signaling

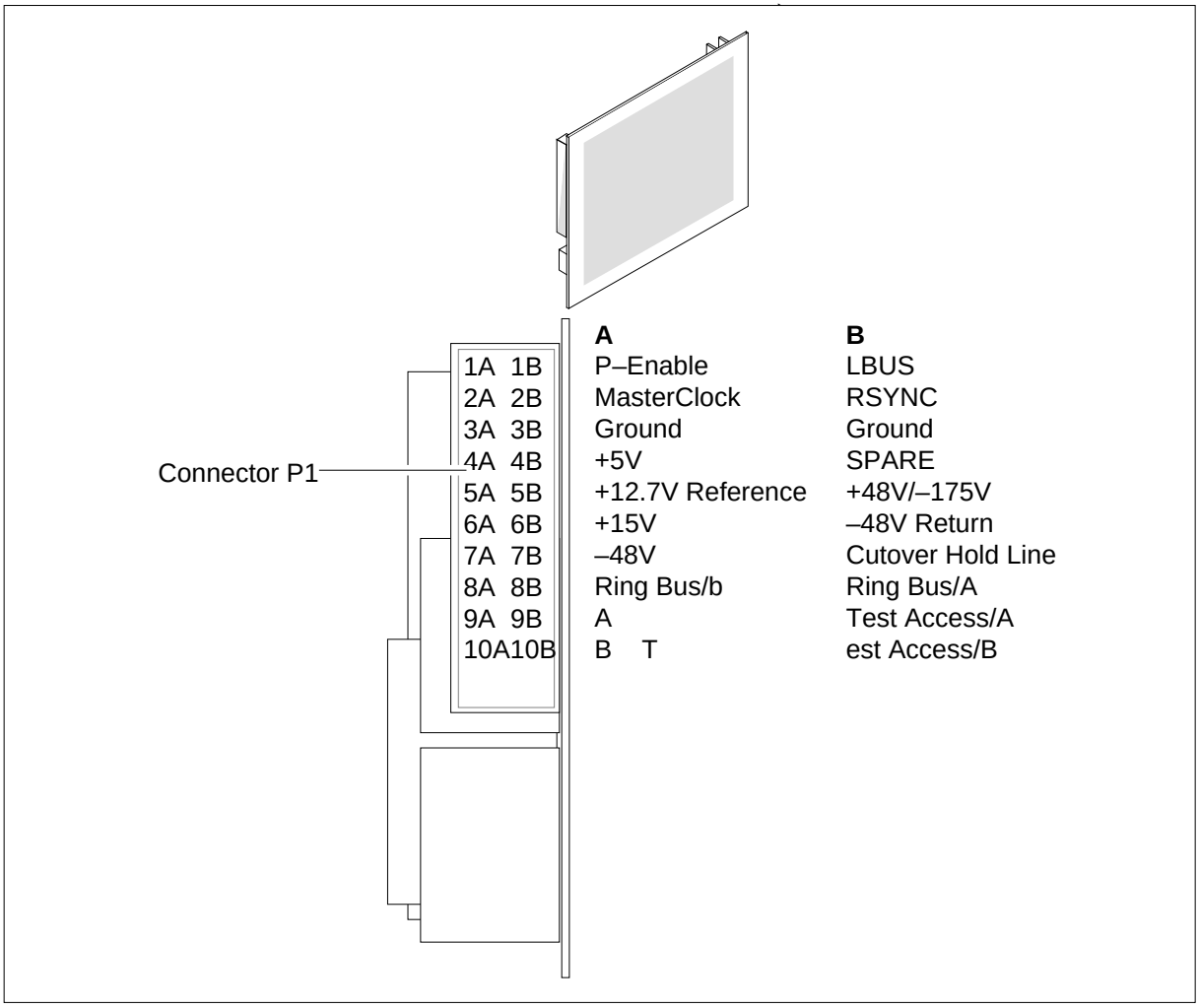
Pin numbers

You can access the following components from the LCM line drawer back panel through the 20-pin line card connector:

- power supply voltages
- the reference voltage
- the subscriber loop
- the ringing signals
- the test interface
- the digital interface

The 20-pin line card connector has the pin numbers that appear in the following figure.

NT6X33AA pin numbers



Technical data

Description

The NT6X33AA line card is constructed on a two-layer printed circuit board. The card weighs approximately 110 g (3.53 oz). The dimensions of the card are 76 mm (2.99 in.) by 89 mm (3.5 in.)

Technology

The NT6X33AA line card contains the following components:

- a thickfilm resistor network
- a 20-pin connector

NT6X33AA (end)

- a E99 line card chip
- a QTK268B1 transformer

Power requirements

The power dissipation for an LCM frame populated with NT6X33AA line cards (1280 GULs) appears in the following table. The figures indicate power levels when the battery voltage is -48V, the external resistance is 200W. The system does not energize relays.

Power dissipation

No active lines	Power dissipation (watts)
0	270
103/1280 (3ccs)	690
284/1280 (8ccs)	1390

NT6X35

Product description

The NT6X35 frame supervisory panel (FSP) contains power control and alarm facilities that provide interfaces. The interfaces are between the NT0X42 power distribution center (PDC) and the NT6X53 power converters in the line concentrating module (LCM) shelves. The LCM is a peripheral module (PM) in the DMS-100 Family of digital switching equipment. The LCM provides operational signals to and from the ringing generators (RGs) . The FSP contains two RGs that operate separately. The FSP circuits supply power to these RGs.

The features of the NT6X35 are as follows:

- provides power control to a maximum of four LCM shelves
- provides power control to two RG circuits in the FSP
- provides two talk battery (filtered -48 V) outputs to the LCM
- monitors the undervoltage (U/V) alarm circuits of a maximum of four NT6X53 power converters and provides circuit breaker trip signals
- monitors the RG power control breaker guard circuits and provides breaker trip signals
- monitors the fuse guard circuits of the +5V and +15V supplies from the NT6X53 power converter and the alarm battery supply (ABS) fuses
- provides frame fail lamp indication on the front panel if breakers trip or fuses fail
- provides a converter fail LED indicator on the front panel below the associated power feed circuit breaker
- provides connections for external aisle alarm circuit and end-aisle alarm lamp
- contains duplicate RGs that generate standard ringing and automatic number identification (ANI)/COIN voltages when the LCM commands these items
- provides ABS test jacks at the front and rear of the FSP
- provides four service jacks that access two telephone (TEL-A, TEL-B) pairs through rear connectors. The NT6X35 provides these features for interframe and interaisle communications.
- provides two data (DATA-A, DATA-B) pairs multiplied to FSP on other frames through rear connectors. The NT6X35 provides these features for interframe and interaisle communications.

NT6X35 (continued)

Location

The LCM FSP is in the PDC in shelf position 72.

Functional description

The following section describes the function of the NT6X35. This section describes the following functions:

- the power control circuits
- the alarm circuits
- the front panel controls and indicators

Power control circuits

The power control circuits consist of six circuit breakers (CB1 to CB6) that work with the FSP alarm card NT6X36AA. When you manually close a circuit breaker, the system connects -48V power to the associated equipment. The guard contact (NC) to the alarm circuit opens. The circuit breaker trip coil (C) does not operate.

A U/V condition can occur in any of the four NT6X53 power converters in the LCM shelves. If a U/V condition occurs, a U/V alarm signal appears. The alarm signal appears at the FSP alarm card input (5, 25, 26 or 30) from the affected converter. This event operates the trip coil (C) and the associated circuit breaker opens. The guard contact (NC) closes. This action causes the alarm circuit to activate the aisle alarms 1 and 2 (19, 20). This action causes the frame fail indicator to light. Aisle alarm 2 can connect to an external end-aisle alarm lamp.

Circuit breakers CB1 and CB4 provide -48V power feeds to the external LCM shelves. Circuit breakers CB5 and CB6 connect internally to RG-0 and RG-1. These circuit breakers provide RG-0 and RG-1 with -48V power feeds. The RG generate standard ringing voltage and ANI/COIN voltages (±48V and ±130V).

Filters A and B provide two talk battery feeds. These filters connect between the -48V supply without a filter from the PDC and the talk battery A and B outputs.

Alarm circuits

The FSP alarm card NT6X36AA is the main component of the FSP alarm circuits. The ABS powers the alarm card. Fuse F02 protects the alarm card. Other fuses protect the following:

- frame fail indicator lamp (F01)
- the end-aisle lamp circuit (F03)
- the ABS jack circuit (F04) on the front and rear of the FSP

Fuses F01, F02, F03 and F04 have a guard contact. The guard contact closes if the associated fuse blows. The four guard contacts connect to an input (37) on the alarm card. When a guard contact closes, the frame fail indicator lights. The system operates aisle alarm circuit 1 and 2.

The alarm card receives inputs from the following:

- the guard contact in CB1 to CB6 and the converter U/V circuits
- the fuse guard contacts in the converter +15V and +5V outputs
- the RG ringing and -48V ANI or COIN outputs

A fuse guard closure in these circuits causes a frame fail indication and aisle alarm operation.

Front panel controls and indicators

You can manually operate circuit breakers CB1 to CB6 from the front panel. Each circuit breaker has a converter fail LED indicator below the associated circuit breaker. Circuit breakers CB1 to CB4 have a label with the base mounting position of the shelf in the LCM frame. The converter that each CB feeds is at this location. Circuit breakers CB5 and CB6 have a label with the correct RG identification. Fuses F01 and F04 have a mechanical indicator that indicates from the front of the panel that a fuse operated.

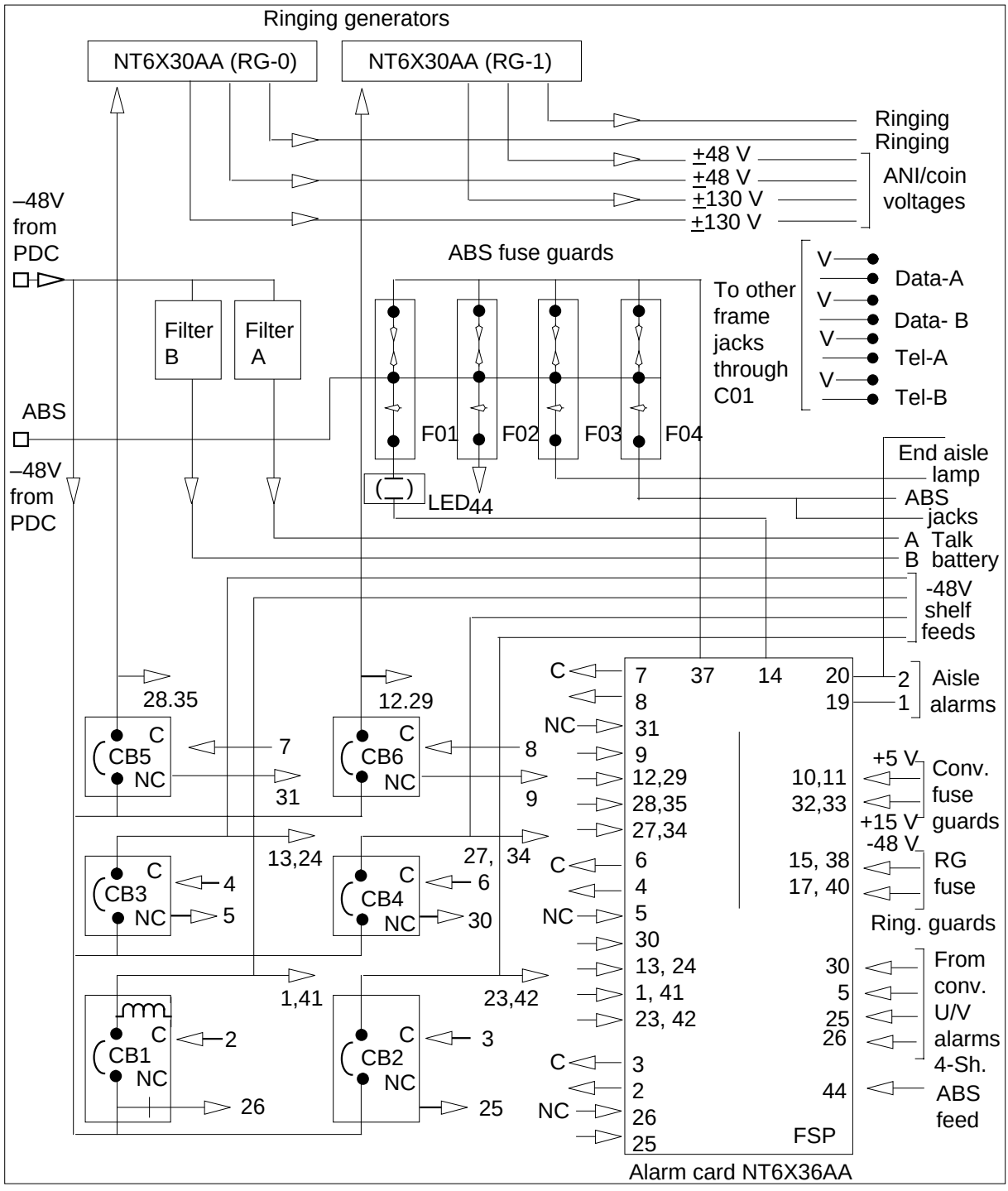
The telephone and data jacks, the ABS jacks and the frame fail indicator are on the front panel.

Functional blocks

The relationship among the NT6X35 functional blocks appears in the following figure.

NT6X35 (continued)

NT6X35 functional blocks

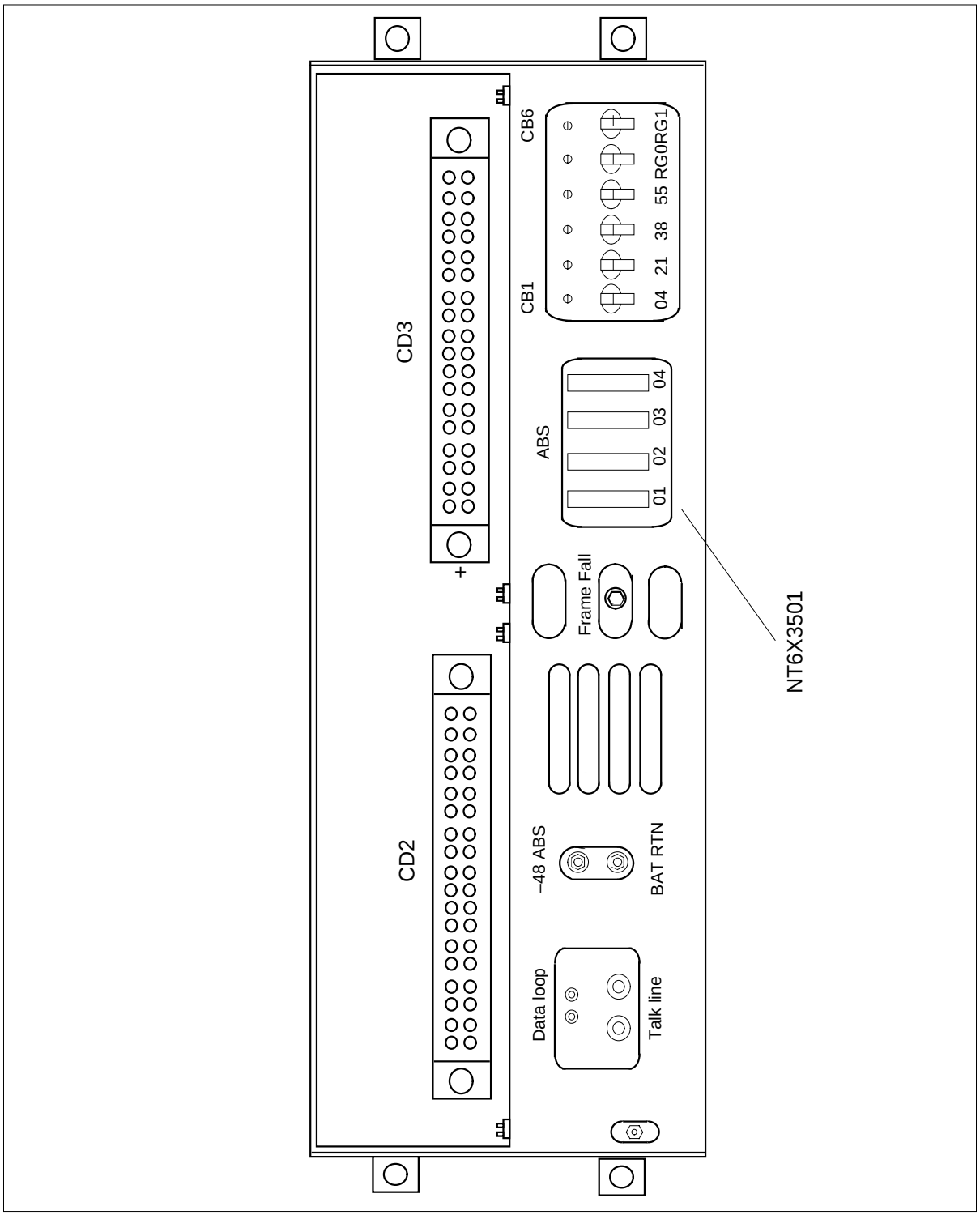


Note: The 48V and ABS battery returns do not appear in this diagram.

The NT6X35 LCM FSP appears in the following figure.

NT6X35 (continued)

NT6X35 LCM FSP front view



Technical data

The technical data section provides the following specifications for the NT6X35:

- power requirements
- power protection
- alarm inputs
- alarm outputs
- equipment dimensions
- environmental conditions

Power requirements

The NT6X35 power requirements appear in the following table.

Power requirements parts

Battery terminal voltage	-42.5V to -55.8V
Normal range (float charge)	-49.0V to -53.5V
Maximum discharge (no charge)	-42.5V
Maximum charge (equalizing)	-55.8V

Power protection and alarm inputs

The NT6X35 power protection and alarm inputs appear in the following table.

Power protection and alarm inputs (Sheet 1 of 2)

Function	CB or fuse	Rating	Alarm input NT6X36
Shelf 04 feed	CB1	10A	26
Shelf 18 feed	CB2	10A	25
Shelf 39 feed	CB3	10A	5
Shelf 53 feed	CB4	10A	30
RG-0 feed (in FSP)	CB5	10A	31
RG-1 feed (in FSP)	CB6	10A	9

Note: The base mounting position number that identifies the shelf is the location of the lowest mounting screw that supports the shelf. Base mounting positions are numbered from 00 at the bottom of the frame to 77 at the top of the frame.

NT6X35 (end)

Power protection and alarm inputs (Sheet 2 of 2)

Function	CB or fuse	Rating	Alarm input NT6X36
Frame fail indicator ABS	F01	1.33A	-37
Alarm card ABS	F02	1.33A	-37
End aisle lamp ABS	F03	1.33A	-37
ABS jacks feed	F04	1.33 A	-37

Note: The base mounting position number that identifies the shelf is the location of the lowest mounting screw that supports the shelf. Base mounting positions are numbered from 00 at the bottom of the frame to 77 at the top of the frame.

Alarm outputs

The alarm output specifications for the NT6X35 are as follows:

- the aisle alarm multiple (NT6X36: 19, 20) normally contains closed (NC) contacts. The aisle alarm multiple opens when an alarm is not present
- the frame fail lamp (NT6X36: 14) has a high resistance ground that uses NC contacts. The frame fail lamp opens when an alarm is not present.

Equipment dimensions

The NT6X35 dimensions are 216 mm (8.5 in.) high, 280 mm (11 in.) deep and 610 mm (24 in.) wide. The approximate weight of the NT6X35 is 10 kg (22 lb).

Environmental conditions

The NT6X35 operates under limited environmental conditions. These conditions appear in the following table.

Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 °C to 30 °C (50 °F to 86 °F)	5 °C to 49 °C (41 °F to 120.2 °F)
Relative humidity	20% to 55%	20% to 80%

Note: Expect a relative humidity of 80% at a maximum ambient temperature of 21°C (69.8°F). At an ambient temperature of 49°C (120.2°F), expect the maximum relative humidity to be 30%.

NT6X35BA

Product description

The NT6X35BA Enhanced Network (ENET) crosspoint card performs the nonblocking switching function for the 128-K ENET. The NT9X35BA accepts 16-K pulse code modulation (PCM) input channels. The NT9X35BA receives these channels from the vertical bus (V-bus). The NT9X35BA switches the channels to any of 16-K PCM output channels on the horizontal bus (H-bus). The V-bus carries data received from the 128-K ENET interface paddle boards. These paddle boards can be NT9X40BA (ENET+ quad fiber paddle board) with four DS512 links, or NT9X41BA (16-port DS30 paddle board). The NT9X41BA is equal to one DS512.

The NT6X35BA uses a double buffer design. The double buffer design allows a constant one-frame delay for all channels. This condition permits switching of services required for wideband services. The switching of services is not limited. Insertion of PCM data on the specified time slot of the H-bus causes switching. The crosspoint card receives and stores the PCM data. Each crosspoint card has a connection memory that controls the output. The correct crosspoint card receives outgoing PCM data from the H-bus. The data is formatted and serialized for transmission on the fiber optic links or DS30.

Functional description

The NT6X35BA card performs the following functions:

- acceptance of maximum 2-K input channels (four DS512) from the associated paddle board of the card
- distribution of the four received DS512 to the appropriate section of the V-bus
- acceptance of maximum 14-K input channels from the V-bus
- alignment of incoming V-bus data to the local shelf frame
- storage of the 16-K input channels into one half of the data memory
- read-out of 16-K output channels from the other half of the memory and transmission to the H-bus
- alternation between the two halves of the memory to provide double buffering
- follow of the V-bus to H-bus mapping in the connection memories
- access and read of the H-bus section that associates with the card slot where the crosspoint card connects
- interface with the shelf controller (NT9X13) through the processor bus (P-bus)

NT6X35BA (continued)

- insertion and removal of test codes at different points on the card
- insertion and removal of pseudo-random data at different points on the card

When the crosspoint card is at the far left and right of the H-bus, the card terminates the H-bus. The card terminates the H-bus with an impedance that matches the backplane. This card is the NT9X35CA and is identical to NT6X35BA.

Functional blocks

The NT6X35BA contains the following functional blocks:

- the V-bus interface
- crosspoint modules
- the H-bus interface
- the P-bus interface
- clock generation

Vertical bus interface

The V-bus interface receives data from the paddle board and feeds the data into the main interface mode. The main interface mode connects the data to a V-bus section. The V-bus distributes the data to crosspoint cards in a vertical column in a cabinet. The crosspoint cards associate in pairs, or mates, that are side by side in each shelf. A mate card receives PCM from the V-bus of the mate. The mate card gives PCM from the mate V-bus to the mate. Each card has 16-K channels of input. A maximum of eight cards in one 128-K ENET cabinet can share the same inputs with this arrangement.

Crosspoint modules

The data streams that the V-bus interface provides transmit to the crosspoint modules for time switching.

Horizontal bus interface

The H-bus distributes switched PCM from the crosspoint cards in each shelf to the fiber optic links. The H-bus distributes switched PCM for transmission out of the 128-K ENET.

Processor bus interface

The P-bus interface block performs the following functions:

- buffer of data and control signals between the P-bus and the card
- decoding of addresses for access to elements on the card
- identification of PROM that contains the card code and version numbers

- decoding of addresses for the paddle board enable signal
- control of lockout feature of the
- generation of the select strobes for the paddle board

Clock generation

This block receives two clocks and one frame pulse. The block generates all the clocks and frame pulses for the card and the paddle board.

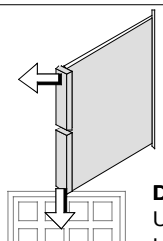
Signaling

Pin numbers

The NT6X35BA pin numbers for appear in the following figure.

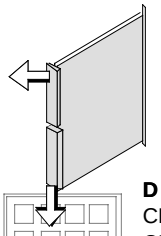
NT6X35BA (continued)

NT6X35BA pin numbers (Part 1 of 2)



	D	C	B	A
1	UAFP	GND	UBFB	GND
2	UA0	UA1	UB0	UB1
3	UA2	UA3	UB2	UB3
4	UA4	UA5	UB4	UB5
5	UA6	UA7	UB6	UB7
6	UA8	UA9	UB8	UB9
7	UCFP	GND	UDFP	GND
8	UC0	UC1	UD0	UD1
9	UC2	UC3	UD2	UD3
10	UC4	UC5	UD4	UD5
11	UC6	UC7	UD6	UD7
12	UC8	UC9	UD8	UD9
13	GND	GND	GND	GND
14	MAFP	GND	MBFB	GND
15	MA0	MA1	MB0	MB1
16	MA2	MA3	MB2	MB3
17	MA4	MA5	MB4	MB5
18	MA6	MA7	MB6	MB7
19	MA8	MA9	MB8	MB9
20	MCFP	GND	MDFP	+5V
21	MC0	MC1	MD0	MD1
22	MC2	MC3	MD2	MD3
23	MC4	MC5	MD4	MD5
24	MC6	MC7	MC6	MD7
25	MC8	MC9	MD8	MD9
26	DA31	RDAT0	RDAT1	GND
27	DA30	RDAT2	RDAT3	+5V
28	DA29	RDAT4	RDAT5	+5V
29	DA28	RDAT6	RDAT7	GND
30	DA27	RDAT8	RDAT9	+5V
31	DA26	WBUS0	WBUS1	+5V
32	DA25	WBUS2	WBUS3	GND
33	DA24	WBUS4	WBUS5	-5V
34	NSEL0	WBUS6	WBUS7	-5V
35	NSEL1	WBUS8	WBUS9	-5V
36	NSEL2	RESET-	RNW	-5V
37	NSEL3	ACK-	DAS32-	GND
38	NSTB0	NMPEN	NSPEN	GND
39	NSTB1			+5V
40	NSTB2	ADDR02	ADDR03	+5V
41	NSTB3	ADDR04	ADDR05	+5V
42		ADDR06	ADDR07	+5V
43		ADDR08	ADDR09	GND
44	NCSEN	ADDR10	ADDR11	+5V
45	CD0	ADDR12	ADDR13	+5V

NT6X35BA pin numbers (Part 2 of 2)



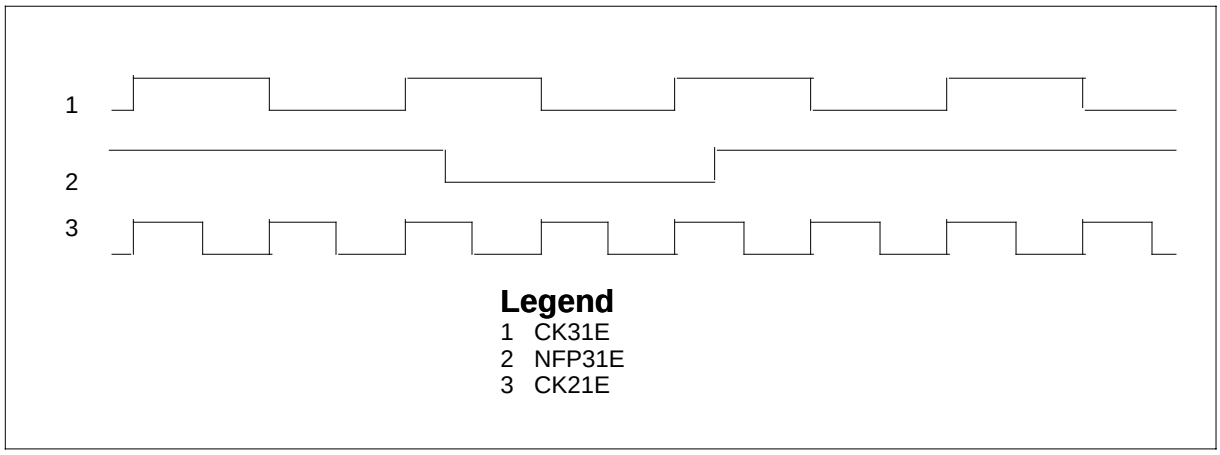
	D	C	B	A
46	CK21P+	ADDR14	CD3	+5V
47	CK21P-	CD1	CD2	+5V
48	NFP21E+			GND
49	NFP21E-			+5V
50	CK61	CK21E-	CK21E+	+5V
51	NFP61	CK31E-	CK31E+	+5V
52	NTFP61	NFP31E-	NFP31E+	+5V
53	GND	GND	CD4	GND
54	H00	H01	H10	H11
55	H02	H03	H12	H13
56	H04	H05	H14	H15
57	H06	H07	H16	H17
58	H08	H09	H18	H19
59	GND	GND	GND	GND
60	H20	H21	H30	H31
61	H22	H23	H32	H33
62	H24	H25	H34	H35
63	H26	H27	H36	H37
64	H28	H29	H38	H39
65	GND	GND	GND	GND
66	H40	H41	H50	H51
67	H42	H43	H52	H53
68	H44	H45	H54	H55
69	H46	H47	H56	H57
70	H48	H49	H58	H59
71	GND	GND	GND	+5V
72	H60	H61	H70	H71
73	H62	H63	H72	H73
74	H64	H65	H74	H75
75	H66	H67	H76	H77
76	H68	H69	H78	H79
77	GND	GND	GND	GND
78	LAFP	GND	LBFB	GND
79	LA0	LA1	LB0	LB1
80	LA2	LA3	LB2	LB3
81	LA4	LA5	LB4	LB5
82	LA6	LA7	LB6	LB7
83	LA8	LA9	LB8	LB9
84	LCFP	GND	LDFP	GND
85	LC0	LC1	LD0	LD1
86	LC2	LC3	LD2	LD3
87	LC4	LC5	LD4	LD5
88	LC6	LC7	LD6	LD7
89	LC8	LC9	LD8	LD9
90	GND	GND	GND	GND

NT6X35BA (end)

Timing

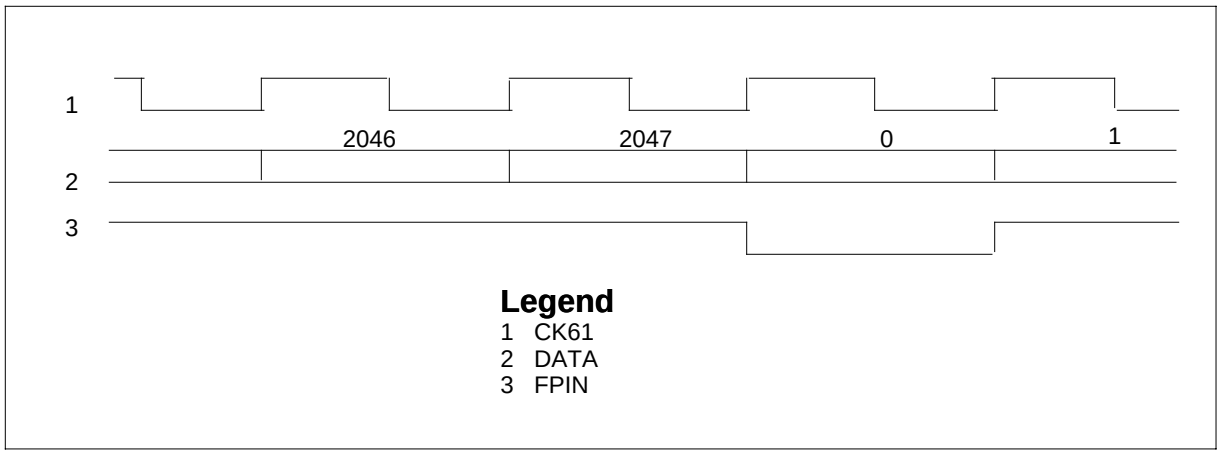
The frame pulse timing of the NT6X35BA appears in the following figure.

NT6X35BA frame pulse timing



The V-bus timing appears in the following figure.

NT6X35BA V-bus timing



Technical data

Power requirements

The NT6X35BA requires a maximum of +5 V and a minimum of -5.2 V, with a variance of ±5%.

NT6X36AA

Product description

The NT6X36AA line concentrating module (LCM) frame supervisory panel (FSP) alarm card activates the FSP circuit breakers. The LCM FSP alarm card activates the breakers in response to an alarm relay release. The alarm relay release occurs in the associated NT6X53 power converters and NT6X30 ringing operators. The initiates frame fail alarms and aisle alarms in response to alarms from fuses in the FSP.

The NT6X36AA LCM FSP card has the following features:

- trip operation a maximum of six circuit breakers
- detection of fuse guards from -48V, 5V, 15V and ringing generator (RG)
- activation of aisle alarms and frame fail lamp
- removal and replacement of a card without a trip of the circuit breakers

Functional description

The NT6X36AA supplies power to the alarm light-emitting diodes (LEDs) on the power converters and ringing generators. When a power converter does not plug in to the back panel, the NT6X36AA trips the associated circuit breaker. When the system does not detect voltage, the NT6X36AA trips the associated circuit breaker. The NT6X36AA system cannot detect voltage when a relay contact shorts on the power converter.

You can remove and replace an NT6X36AA LCM FSP card without a trip of the circuit breakers. Use short fingers on a specified card to initiate to perform this action. The specified card is for terminals 2, 3, 4, 6, 7 and 8 (TRIP1 through TRIP6).

Functional blocks

The NT6X36AA has the following functional blocks:

- alarm circuitry
- trip circuitry

Alarm circuitry

The alarm circuitry responds to changes of state in the fuse guards and the RG. When the system detects voltage failure, the alarm circuitry activates the frame fail lamp and the A and B aisle alarms.

Trip circuitry

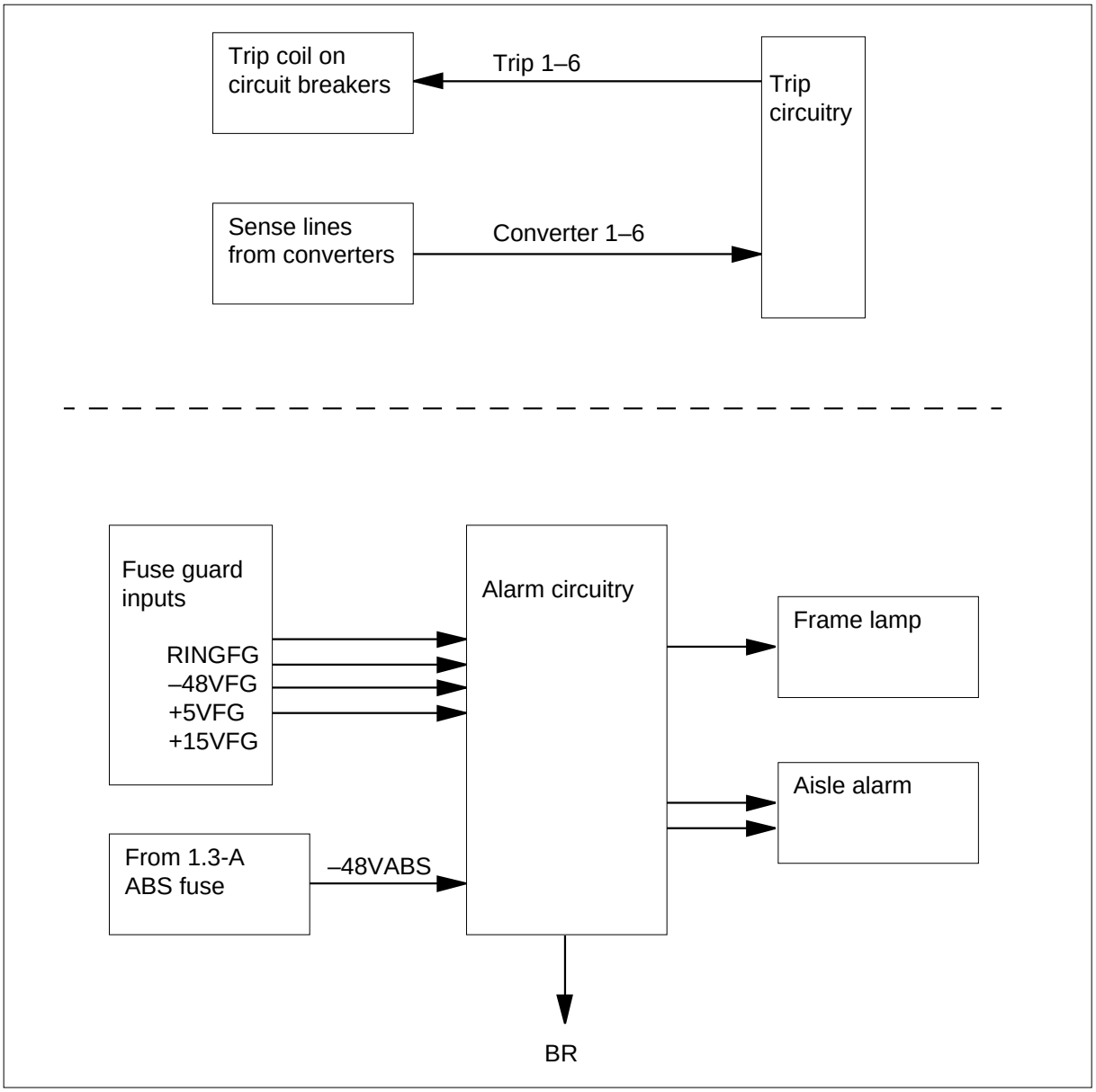
The NT6X36AA trip circuitry responds to power converter failure. Converter failure occurs when the converter does not produce power or is not plugged in

NT6X36AA (continued)

to the backpanel. Converter failure causes the trip circuit to increase the voltage on the sense line. The voltage increases until the trip circuitry activates the trip coil on the circuit breaker, and breaks the circuit.

The relationship among the functional blocks appears in the following figure.

NT6X36AA functional blocks



Signaling

Pin numbers

The pin numbers for the NT6X36AA appear in the following table.

NT6X36AA pin numbers

Pin	Signal	Pin	Signal
1	-48V1	23	-48V2
2	TRIP1	24	-48V3
3	TRIP2	25	CONV2
4	TRIP3	26	CONV1
5	CONV3	27	-48V4
6	TRIP4	28	-48V5
7	TRIP5	29	-48V6
8	TRIP6	30	CONV4
9	CONV6	31	CONV5
10	+5VFG1	32	+15VFG1
11	+5VFG2	33	+15VFG2
12	CB6	34	CB4
13	CB3	35	CB5
14	FRMLMP	36	LEDPW
15	-48VFG1	37	-48VFG3
16		38	-48VFG4
17	RINGFG1	39	
18		40	RINGFG3
19	AILALMB	41	CB1
20	AILALMA	42	CB2
21		43	BR
22	BR	44	-48VABS

NT6X36AA (end)

Technical data

Power requirements

The NT6X36AA operates in the range of 0 to -60V. The standard -48V battery supplies power to the NT6X36AA through a 1.3A QFF1 fuse.

NT6X36AF

Product description

The NT6X36AF frame supervisory panel (FSP) card replaces the NT6X36AA card. The NT6X36AF card can recover from low battery (ARLB). This card monitors the converters connected to the card. When a converter is not plugged in the backpanel, the NT6X36AF trips the associated circuit breaker. When the system does not detect voltage output, the NT6X36AF trips the associated circuit breaker. The system senses the fuse guards of a converter to detect voltage output.

The ARLB function identifies the difference between converter failure and low office battery supply. When a battary has less than 41V of power, a low battary condition is present. Under low battery conditions, the system disables the trip feature. Converters can shut down and not trip the circuit breakers. When the office battery supply gains power again (above 45V), the system enables the trip feature and monitors the converters.

The main features of the NT6X36AF FSP card are as follows:

- trip operation for a maximum of six circuit breakers
- two separate lines to detect low voltage
- deactivation of trip function under low battery conditions
- automatic recovery from low battery
- detection of fuse guards from -48V, 5V, 15V and ringing generator (RG)
- activation of aisle alarms and frame lamp
- removal and replacement of card without a trip of the circuit breakers

Functional description

Functional blocks

The NT6X36AF card contains the following functional blocks:

- alarm circuits
- an NT5L33AC hybrid
- trip circuits

Alarm circuits

The alarm circuits respond to changes of state in the fuse guards or the RG. When the system detects voltage failure, the alarm circuits activate the frame lamp and the A and B aisle alarms.

NT6X36AF (continued)

NT5L33AC hybrid

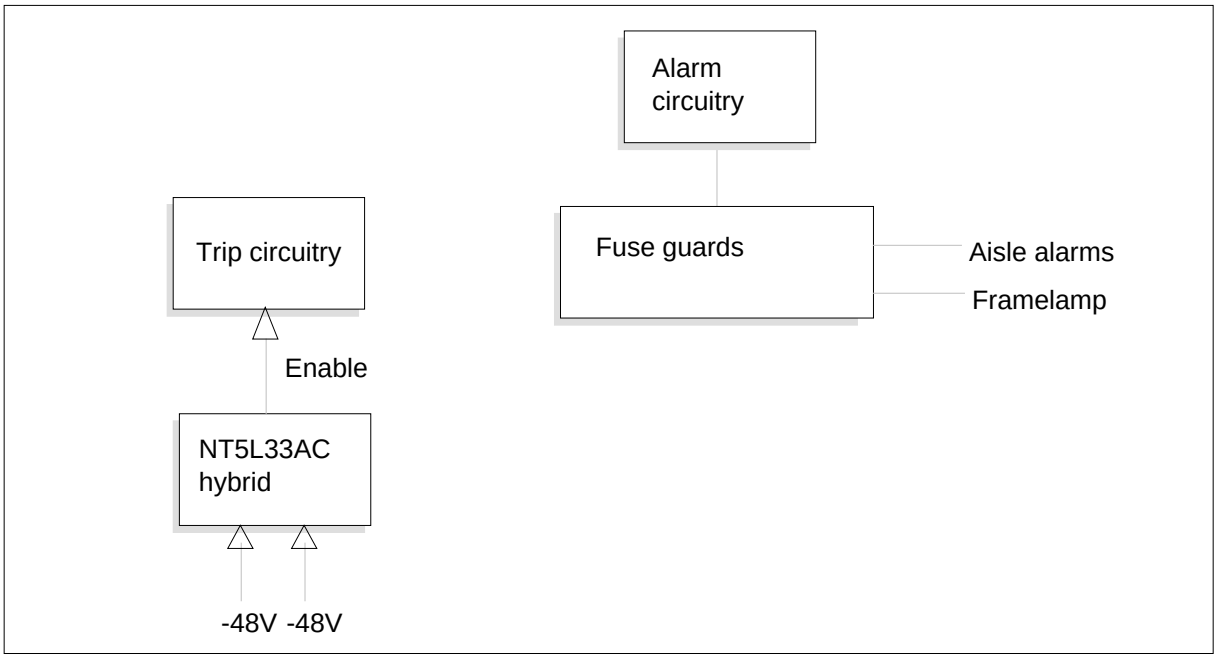
The NT5L33AC hybrid has two -48V inputs and one output. To provide ARLB function, This block detects the office battery supply and enables or disables the trip feature to provide ARLB function. When the input voltage is more than 44.5V +/- 0.5V, this block enables the trip circuits. When the input voltage is less than 41.5 +/- 0.5V, this block disables the trip circuits.

Trip circuits

The trip circuits respond to converter failure. Converter failure occurs when the converter does not produce power or is not plugged in the backpanel. Converter failure causes a rise in the current of the trip circuits. This rise energizes the trip coil on the circuit breaker and breaks the circuit.

The relationship between the functional blocks appears in the following figure.

NT6X36AF functional blocks



Signaling

Pin numbers

The pin numbers for the NT6X36AF appear in the following table.

NT6X36AF pin numbers

Pin	Signal	Pin	Signal
1	-48V1	23	-48V2
2	TRIP1	24	-48V3
3	TRIP2	25	CONV2
4	TRIP3	26	CONV1
5	CONV3	27	-48V4
6	TRIP4	28	-48V5
7	TRIP5	29	-48V6
8	TRIP6	30	CONV4
9	CONV6	31	CONV5
10	+5VFG1	32	+15VFG1
11	+5VFG2	33	+15VFG2
12	CB6	34	CB4
13	CB3	35	CB5
14	FRMLMP	36	LEDPW
15	-48VFG1	37	-48VFG3
16		38	-48VFG4
17	RINGFG1	39	
18		40	RINGFG3
19	AILALMB	41	CB1
20	AILALMA	42	CB2
21		43	BR
22	BR	44	-48VABS

NT6X36AF (end)

Technical data

Power requirements

The NT6X36AF card operates in the range of 0 to -60V. The standard -48V battery supplies power to the NT6X36AF card through a 1.3A QFF1 fuse.

NT6X36KA

Product description

The NT6X36KA line concentrating module (LCM) frame supervisory panel (FSP) alarm card activates the FSP circuit breakers. The alarm card activates the breakers in response to an alarm relay release. The alarm relay release occurs in the associated NT6X53 power converters and NT6X30 ringing operators. The initiates frame fail alarms and aisle alarms in response to alarms from fuses in the FSP.

The NT6X36KA LCM FSP card has the following features:

- trip operation for a maximum of six circuit breakers
- detection of fuse guards from -60V, 5V, 15V and ringing generator (RG)
- activation of aisle alarms and frame fail lamp
- removal and replacement of card without a trip of the circuit breakers

This card is the -60V version of the NT6X36AA.

Functional description

The NT6X36KA supplies power to the alarm light-emitting diodes (LED) on the power converters and ringing generators. When the power converter is plugged in the backpanel, the NT6X36KA trips the associated circuit breaker. The system generates a FRAMEFAIL signal. When the system does not detect a voltage output, the NT6X36KA trips the associated circuit breaker. The system generates a FRAMEFAIL signal. The system cannot detect a voltage when a closed relay contact is present on the power converter.

You can remove and replace an NT6X36KA LCM FSP card without a trip of the circuit breakers. Use short fingers on the card for terminals 2, 3, 4, 6, 7 and 8 (TRIP1 to TRIP6) to perform this action.

Functional blocks

The NT6X36KA has the following functional blocks:

- alarm circuitry
- trip circuitry

Alarm circuitry

The alarm circuitry responds to changes of state in any of the fuse guards. When the system detects fuse failure, the alarm circuitry activates the FRAMEFAIL lamp and the A and B AISLE alarms. The system detects converter failure through current drain on LEDPW.

NT6X36KA (continued)

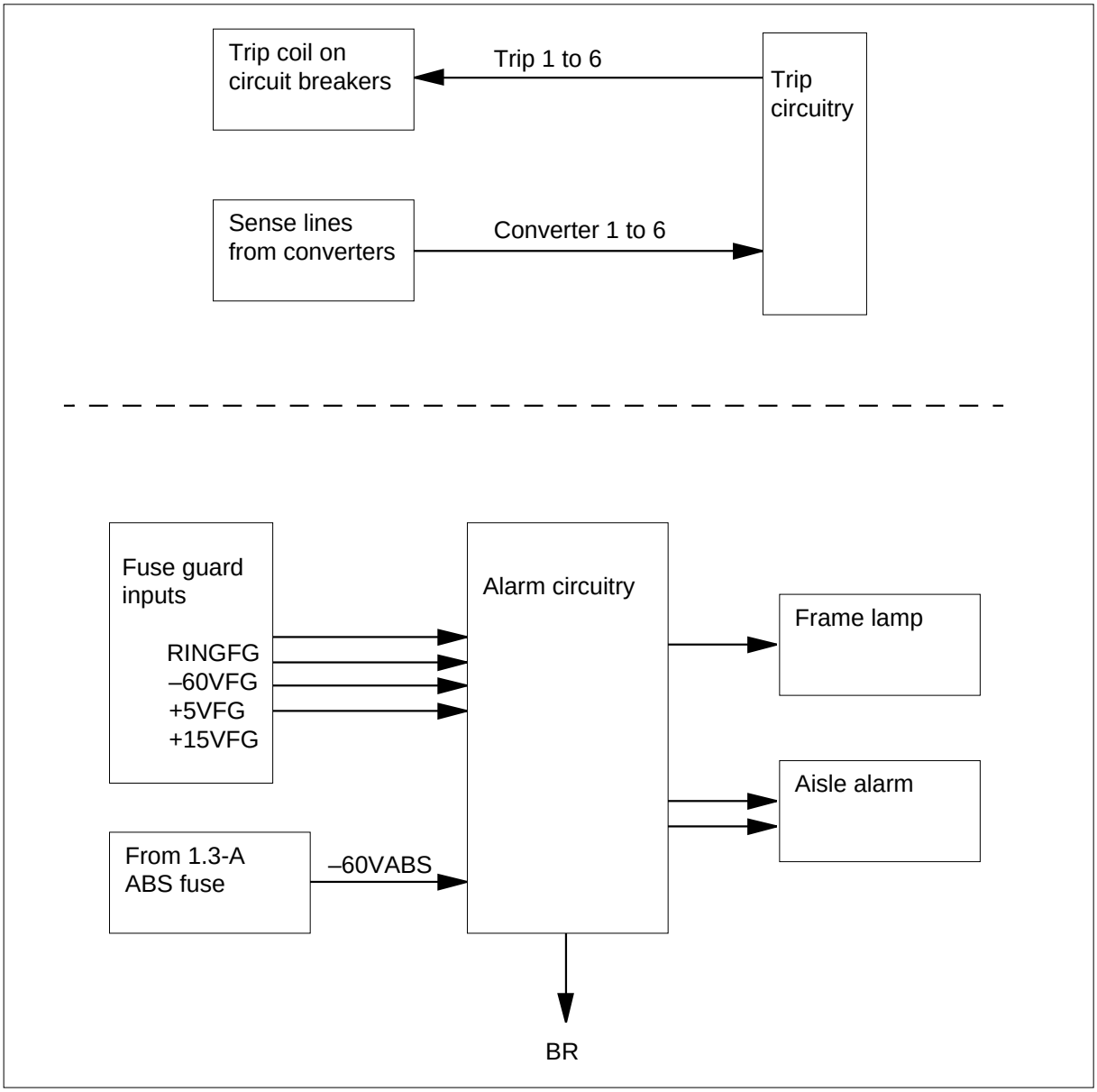
Trip circuitry

The trip circuitry responds to power converter failure. Converter failure occurs when the converter does not produce power or does not plug in the backpanel. Converter failure causes the trip circitry to increase voltage on the sense line. The voltage increases until the trip circuitry activates the trip coil on the circuit breaker and breaks the circuit.

The relationship among the functional blocks appears in the following figure.

NT6X36KA (continued)

NT6X36KA functional blocks



NT6X36KA (continued)

Signaling

Pin numbers

The pin numbers for the NT6X36KA appears in the following table.

NT6X36KA pin numbers

Pin	Signal	Pin	Signal
1	-60V1	23	-60V2
2	TRIP1	24	-60V3
3	TRIP2	25	CONV2
4	TRIP3	26	CONV1
5	CONV3	27	-60V4
6	TRIP4	28	-60V5
7	TRIP5	29	-60V6
8	TRIP6	30	CONV4
9	CONV6	31	CONV5
10	+5VFG1	32	+15VFG1
11	+5VFG2	33	+15VFG2
12	CB6	34	CB4
13	CB3	35	CB5
14	FRMLMP	36	LEDPW
15	-60VFG1	37	-60VFG3
16		38	-60VFG4
17	RINGFG1	39	
18		40	RINGFG3
19	AILALMB	41	CB1
20	AILALMA	42	CB2
21		43	BR
22	BR	44	-60VABS

Technical data

Power requirements

The NT6X36KA operates in the range of -52V to -72V. The standard -60V battery powers the NT6X36KA through a 1.3A QFF1 fuse.

NT6X40AC

Product description

The NT6X40AC card is a DS30-format interface to the network. The NT6X40AC replaces two NT6X40AAs. High-speed data applications use the NT6X40AA card. The W87 chip performs many functions of this card. Refer to the W87 specification for additional information about the NT6X40AC card.

Note: The cable lengths on the network side of the XMS-based peripheral module (XPM) can be a maximum of 228.6 m (750 ft) in length.

Location

The NT6X40AC connects to the central side (C-side) of the common XPM. The TT6X40AC connects to the C-side through a maximum of 16 ports on each plane. The NT6X40AC provides both pulse code modulation (PCM) and messaging.

Functional description

The NT6X40AC communicates with the network side of the XPM in a DS30 format. The card uses the W87 chip to transmit and receive PCM and the frame pulse and clock. The NT6X40AC communicates with the formatter and message card on the other side. The card transmits PCM to the formatter and receives PCM from the formatter at a DS60 rate. The system transmits messaging to and receives messaging from the message card at a DS60 rate.

The three internal data paths are as follows.

- receive PCM (RPCM)
- transmit PCM (XPCM)
- network looparound

In the RPCM direction, the W87 chip receives DS30 data in biphase format. The W87 chip multiplexes the data to a DS60 rate. After the system latches the data, the system transmits the data to the formatter. In the XPCM direction, the system latches the DS60 data from the formatter and sends the data to the W87 chip.

The system demultiplexes the data to the DS30 rate and biphase codes the data for the network. The loop-around path loops data from the network back to the network. The system removes data from the RPCM direction and inserts the loop data in the XPCM path. This event occurs after a delay that corrects differences in the RPCM and XPCM timing. The system sends control from the looparound in series from the formatter card. The NT6X40AC generates the frame pulse from the link data. The NT6X40AC sends the frame pulse to

the formatter for link synchronization. The system inserts, extracts and exchanges messaging data with the messaging card.

Functional blocks

The NT6X40AC performs the following functions:

- provides a DS30 interface on the C-side of the XPM for PCM
- inserts and extracts messaging
- multiplexes link data from a DS30 rate to a DS60 rate
- demultiplexes data that goes to the link from a DS60 rate to a DS30 rate
- supplies frame pulses from link data to the formatter for system synchronization
- provides network looparound path and control circuitry

Technical data

Power requirements

The NT6X40AC requires a connection to a 5V power supply. The NT6X40AC uses less power than the NT6X40AA. The NT6X40AC has fewer parts and uses low-power high-speed CMOS logic.

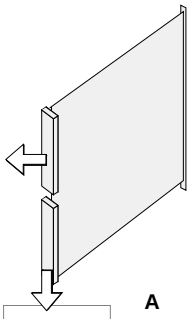
Signaling

Pin numbers

The pin numbers for the NT6X40AC appear in the following figure.

NT6X40AC (end)

NT6X40AC pin numbers



	A	B
1A 1B	GND	GND
2A 2B	+5V	+5V
3A 3B	+5V	+5V
4A 4B	+5V	+5V
5A 5B	GMD	GND
6A 6B	FP–	C97+
7A 7B	GND	GND
8A 8B		
9A 9B	ACT	GND
10A 10B	BPRF0	BPRT0
11A 11B	BPRF2	BPRT2
12A 12B	BPSF0	BPST0
13A 13B	BPSF2	BPST2
14A 14B	BPRF1	BPRT1
15A 15B	BPRF3	BPRT3
16A 16B	BPSF1	BPST1
17A 17B	BPSF3	BPST3
18A 18B	BPRF4	BPRT1
19A 19B	BPRF6	BPRT3
20A 20B	BPSF4	BPST1
21A 21B	BPSF6	BPST3
22A 22B	BPRF5	BPRT1
23A 23B	BPRF7	BPRT3
24A 24B	BPSF5	BPST1
25A 25B	BPSF7	BPST3
26A 26B	GND	GND
27A 27B	SOUT0M	SOUT0
28A 28B	SOUT2M	SOUT2
29A 29B	SOUT4M	SOUT4
30A 30B	SOUT6M	SOUT6
31A 31B	SOUT8M	SOUT8
32A 32B	SOUT10M	SOUT10
33A 33B	SOUT12M	SOUT12
34A 34B	SOUT14M	SOUT14
35A 35B	GND	GND
36A 36B	FPT	C97+5
37A 37B	FP–M	C97+M
38A 38B	FPL–T	SOUT4
39A 39B	FPL–M	SOUT6
40A 40B	CH0TT	SOUT8

	A	B
41A 41B	GND	GND
42A 42B		
43A 43B	LPCNTM	LPCNT
44A 44B		
45A 45B	LPLTM	LPLT
46A 46B	GND	GND
47A 47B	SIN0M	SIN0
48A 48B	SIN2M	SIN2
49A 49B	SIN4M	SIN4
50A 50B	SIN6M	SIN6
51A 51B	SIN8M	SIN8
52A 52B	SIN10M	SIN10
53A 53B	SIN12M	SIN12
54A 54B	SIN14M	SIN14
55A 55B	FPL–	GND
56A 56B	BPRF8	BPRT8
57A 57B	BPRF10	BPRT10
58A 58B	BPSF8	BPST8
59A 59B	BPSF10	BPST10
60A 60B	BPRF9	BPRT9
61A 61B	BPRF11	BPRT11
62A 62B	BPSF9	BPST9
63A 63B	BPSF11	BPST11
64A 64B	BPRF12	BPRT12
65A 65B	BPRF14	BPRT14
66A 66B	BPSF12	BPST12
67A 67B	BPSF14	BPST14
68A 68B	BPRF13	BPRT13
69A 69B	BPRF15	BPRT15
70A 70B	BPSF13	BPST13
71A 71B	BPSF15	BPST15
72A 72B	GND	GND
73A 73B	FPRC2	FPRC0
74A 74B		
75A 75B	CH0S0	CH0R0
76A 76B	CH0S2	CH0R2
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

NT6X40AD

Product description

The NT6X40AD card is a 16-port network interface for the XPM. The primary function of this card is to translate Manchester bi-phase codes to binary code. The card performs message insertions and extractions for diagnostic tests and maintenance purposes. The NT6X40AD uses a programmable logic device. This device adds diagnostic capabilities that are not present on the current XPM.

Note: The cable lengths on the network side of the XMS-based peripheral module (XPM) can be a maximum of 228.6 m (750 ft) in length.

Location

The NT6X40AD connects to the central side (C-side) of the common XPM. The NT6X40AD uses a maximum of 16 ports on each plane to connect to the C-side. The NT6X40AD provides pulse code modulation (PCM) and messaging.

Functional description

The NT6X40AD communicates with the network side of the XPM in a DS30 format. The card uses the N03 chip to transmit and receive PCM and the frame pulse and clock. The NT6X40AD communicates with the formatter and message card. The card transmits PCM to the formatter and receives PCM from the formatter at a DS60 rate. The system transmits messaging to the message card and receives messaging from the message card at a DS60 rate.

The four internal data paths are RPCM, XPCM, XPM C-side Loop path and Network Looparound. The NT6X40AD generates the frame pulse from the C-side link data. The NT6X40AD sends the frame pulses to the formatter for link and channel synchronization. The system inserts messaging data in the data stream and extracts data from the data stream. The system uses this data for transmission to and from the message card. The formatter provides interaction control between the messaging and DS-30 I/F card.

Functional blocks

The NT6X40AD performs the following functions:

- provides a DS30 interface on the C-side of the XPM for PCM
- inserts and extracts messaging
- bit-multiplexes link data from a DS30 rate (2.56 Mbits/sec) to a DS60 rate (5.12 Mbits/sec)
- demultiplexes data that transmits to the link from a DS60 rate to a DS30 rate

NT6X40AD (continued)

- supplies frame pulses from link data to the formatter for system synchronization
- provides control circuitry for the network looparound path and provides C-side looparound. The C-side looparound adds diagnostic capabilities that are not present on the current XPM

An additional feature creates C-side loopback capability for improved XPM diagnostics. You can interchange the NT6X40AD with the NT6X40AC. Software feature AN1121 must be present to allow the XPM C-side loopback capability.

Technical data

Power requirements

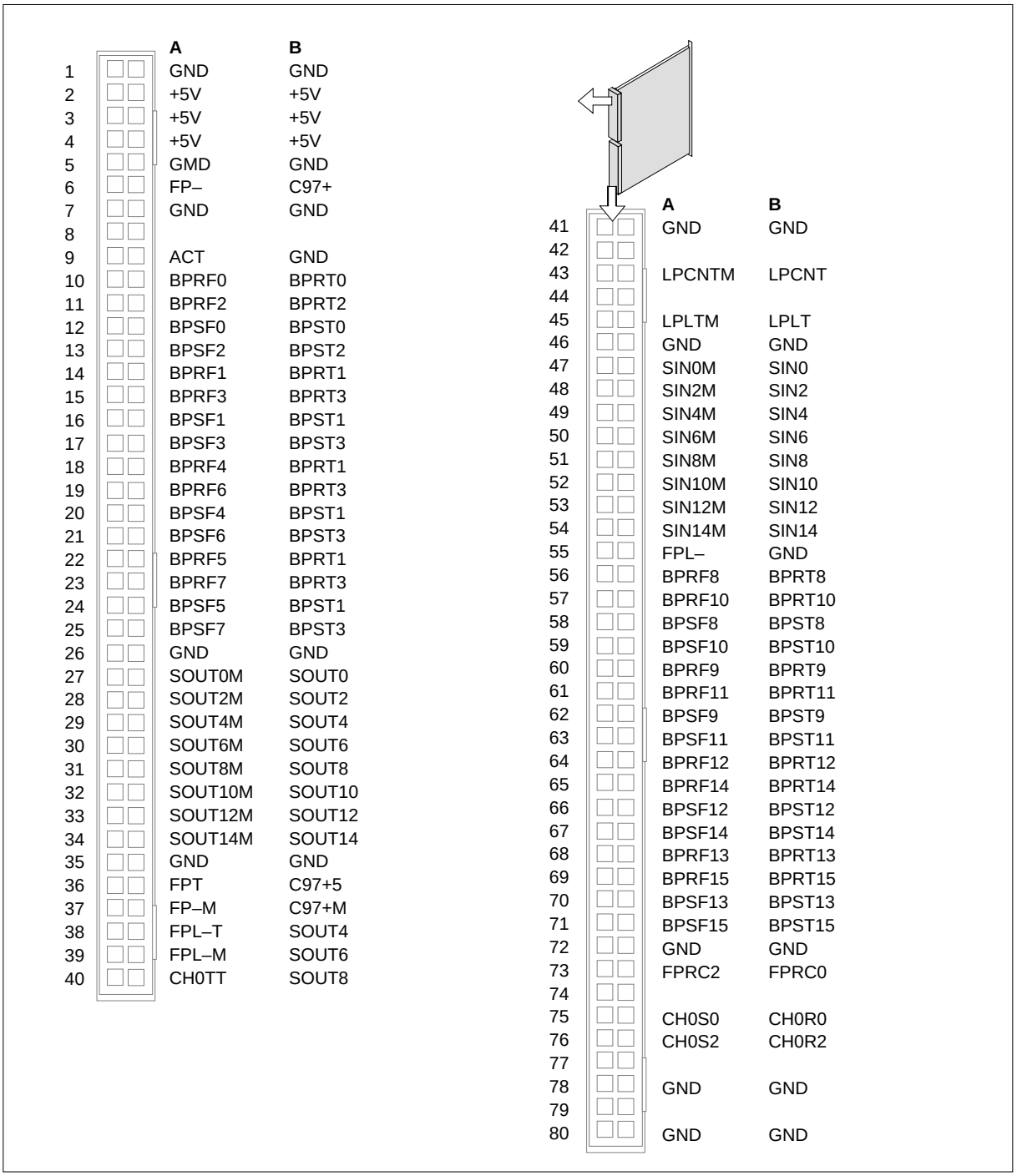
The NT6X40AD requires a connection to a 5V power supply. The NT6X40AD consumes less power than the NT6X40AA. The NT6X40AD has fewer components and uses low-power high-speed CMOS logic.

Signaling

Pin numbers

The pin numbers for the NT6X40AD appear in the following figure.

NT6X40AD pin numbers



NT6X40BA

Product description

The NT6X40BA DS30 central-side (C-side) interface card is a network-side interface for pulse code modulation (PCM) and messaging. The card uses a DS30 data format.

Location

The NT6X40BA resides on the C-side of the subscriber carrier module SLC-96 (SMS). The key slots for this card are 2, 3, 7 and 8. When only four ports are necessary, the NT6X40BA can occupy any NT6X40AB slot.

The NT6X40BA provides four DS30 ports. The NT6X40AB card provides 16 DS30 ports.

Compatibility

The central control (CC) must have a minimum CC load of BCS22.

Functional description

The NT6X40BA card performs the following functions:

- provides a DS30 interface on the network side of the SMS for PCM
- inserts and extracts messaging
- multiplexes data from the link from a DS30 rate (2.56 Mbytes) to a DS60 rate (5.12 Mbytes)
- demultiplexes data that transfers to the link from a DS60 rate to a DS30 rate
- supplies link frame pulse from the link to the formatter for system synchronization
- supplies the network looparound path and control circuitry

The DS30 ports transmit and receive PCM at the rate of 2.56 Mbytes. The system receives the frame pulse and clock from the network side of the SMS.

In the SMS system, the NT6X40BA provides an interface to the formatter card (NT6X41) and the messaging card (NT6X43). The system transmits and receives PCM at a DS60 rate to the formatter and from the formatter. The system transmits messaging to the messaging card and receives messaging from the message card at a DS60 rate. The system uses the biphase format on the C-side of the card. This action allows the system to send the clock, frame pulse and data on a single two-wire interface.

The system inserts and extracts messaging data on the NT6X40BA. The NT6X40BA exchanges data with the formatter card. The system sends the frame pulse from the link to the formatter for synchronization.

The NT6X40BA interface contains three data paths internal to the card. The data loops are the RPCM, XPCM and network looparound. A memory map controls the network looparound. The RAM is on the formatter card.

Network looparound can be controlled for each port or channel. Loop control transfers through a serial link by the same method and by the same format as on the NT6X40AA. The registers that control the loop circuit reside on the formatter card.

Technical data

Requirements

The cables on the network side of the SMS can be a maximum of 228.6 m (750 ft) in length.

Power requirements

The NT6X40 requires a voltage of +5V and a current of 1.3A.

Signaling

Protocol

The hardware on the NT6X40BA card does not look at the protocol that the messaging channels use. The message card and the signaling processor (SP) handles the protocol. The NT6X40BA card can support any 8-bit clear channel protocol.

Timing

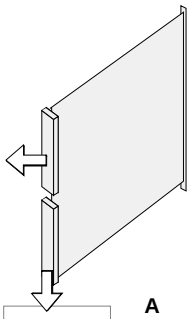
The system transmits and receives PCM at a DS60 rate. The SOUT is the PCM the system transmits to the formatter. The SIN is the PCM the system receives from the formatter.

Pin numbers

The pin numbers for the NT6X40BA appear in the following figure.

NT6X40BA (end)

NT6X40BA pin numbers



	A	B
1A 1B	Gnd	Gnd
2A 2B	+5V	+5V
3A 3B	+5V	+5V
4A 4B	+5V	+5V
5A 5B	Gnd	Gnd
6A 6B	FP–	C97+
7A 7B	Gnd	Gnd
8A 8B		
9A 9B	ACT	Gnd
10A 10B	BPRF0	BPRT0
11A 11B	BPRF2	BPRT2
12A 12B	BPSF0	BPST0
13A 13B	BPSF2	BPST2
14A 14B	BPFR1	BPRT1B
15A 15B	BPFR3	BPRT3
16A 16B	BPSF1	BPST1
17A 17B	BPSF3	BPST3
18A 18B		
19A 19B		
20A 20B		
21A 21B		
22A 22B		
23A 23B		
24A 24B		
25A 25B		
26A 26B	Gnd	Gnd
27A 27B	SOUT0M	SOUT0
28A 28B	SOUT2M	SOUT2
29A 29B		
30A 30B		
31A 31B		
32A 32B		
33A 33B		
34A 34B		
35A 35B	Gnd	Gnd
36A 36B	FPT	C97+T
37A 37B	FP–M	C97+M
38A 38B	FPL–T	Gnd
39A 39B	FPL–M	CH0T
40A 40B	CH0TT	CH0TM

	A	B
41A 41B	Gnd	Gnd
42A 42B		
43A 43B	1PCNTM	1PCNT
44A 44B		
45A 45B	1PLTM	1PLT
46A 46B	Gnd	Gnd
47A 47B	SIN0M	SIN0
48A 48B	SIN2M	SIN2
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B	FPL–	Gnd
56A 56B		
57A 57B		
58A 58B		
59A 59B		
60A 60B		
61A 61B		
62A 62B		
63A 63B		
64A 64B		
65A 65B		
66A 66B		
67A 67B		
68A 68B		
69A 69B		
70A 70B		
71A 71B		
72A 72B	Gnd	Gnd
73A 73B	FPRC2	FPRC0
74A 74B		
75A 75B	CH0S0	CH0R0
76A 76B	CH0S2	CH0R2
77A 77B		
78A 78B	Gnd	Gnd
79A 79B		
80A 80B	Gnd	Gnd

NT6X40CA

Product description

The NT6X40CA DS512 link control card performs the interface function for 512 pulse code modulation (PCM) channels. The PCM channels can connect to a fiber link and to the enhanced network (ENET). The PCM channels connect to the formatter card on one side. The PCM channels connect to the XPM DS512 link paddle board (NT6X40DA) on the other side. The system requires one link control card for each plane of the network.

The NT6X40CA uses the link paddle board to connect to a second paddle board, the NT6X40EA. The NT6X40EA is a DS30 link paddle board. The system uses the NT6X40EA to maintain a temporary interface to the current junctor network during the commissioning interval. The system must equip the XPMs in a specified office with the dual interface. The system must test all the XPMs. When the system completes this action, the system switches operation from the NT6X40EA to the NT6X40CA. You can remove the NT6X40EA and use the cards in other commissioning tasks.

Functional description

A multiplexor selects PCM from the formatter of the active XPM unit and passes the PCM to the network loop multiplexer. The loop multiplexer allows the formatter PCM to go out or allows received PCM from ENET. From this multiplexer, the PCM goes to the bit rate converter (BRC). At the BCR, the serial PCM converts to parallel and changes to a different clock rate. From the BRC the system sends the PCM to the NTCX. In the NTCX, the system adds additional bits for link supervision. The PCM goes to the DS512 link card, the location of the optical components.

The same process occurs in the incoming direction.

This card inserts and extracts a messaging control channel between the CM and the XPM master processor.

Technical data

Power requirements

The NT6X40CA requires a minimum of -5.2V and 0.16A current, and a maximum of +5V and 2.3A to operate correctly.

Signaling

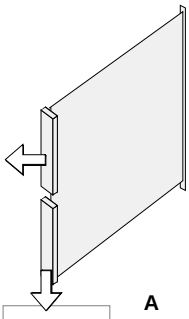
Pin numbers

The pin numbers for the NT6X40CAappear in the following figure.

NT6X40CA (end)

NT6X40CA pin numbers

	A	B
1A 1B	GND	GND
2A 2B	PWR	PWR
3A 3B	PWR	PWR
4A 4B	PWR	PWR
5A 5B	GND	GND
6A 6B	FP	C97
7A 7B	GND	GND
8A 8B		
9A 9B	ACT	GND
10A 10B	TFPT	TFPF
11A 11B	–5.2	–5.2
12A 12B	C122ET	C122EF
13A 13B	GND	GND
14A 14B	TD0	TD1
15A 15B	TD2	TD3
16A 16B	TD4	TD5
17A 17B		
18A 18B		
19A 19B	RLB	
20A 20B	GND	GND
21A 21B	PU1	PU10
22A 22B	PU13	EA
23A 23B	VAR–PULSERSCODE	
24A 24B	PLBSEL	
25A 25B		
26A 26B	GND	GND
27A 27B	SOUT0M	SOUT0
28A 28B	SOUT2M	SOUT2
29A 29B	SOUT4M	SOUT4
30A 30B	SOUT6M	SOUT6
31A 31B	SOUT8M	SOUT8
32A 32B	SOUT10M	SOUT10
33A 33B	SOUT12M	SOUT12
34A 34B	SOUT14M	SOUT14
35A 35B	GND	GND
36A 36B		
37A 37B	FPM	C97M
38A 38B	GND	
39A 39B		
40A 40B		



	A	B
41A 41B	GND	GND
42A 42B		
43A 43B	LPCNTM	LPCNT
44A 44B		
45A 45B	LPLTM	LPLT
46A 46B	GND	GND
47A 47B	SIN0M	SIN0
48A 48B	SIN2M	SIN2
49A 49B	SIN4M	SIN4
50A 50B	SIN6M	SIN6
51A 51B	SIN8M	SIN8
52A 52B	SIN10M	SIN10
53A 53B	SIN12M	SIN12
54A 54B	SIN14M	SIN14
55A 55B		GND
56A 56B	FP97	C195
57A 57B	FR1	FR2
58A 58B	RX0	RX1
59A 59B	RX2	RX3
60A 60B	RX4	RX5
61A 61B	RX6	RX7
62A 62B		
63A 63B	TX0	TX1
64A 64B	TX2	TX3
65A 65B	TX4	TX5
66A 66B	TX6	TX7
67A 67B	GND	GND
68A 68B	RC244	RFP
69A 69B	RXD0	RXD1
70A 70B	RXD2	RXD3
71A 71B	RXD4	RXD5
72A 72B	GND	GND
73A 73B	FPRC2	FPRC0
74A 74B	FPRC0	FPRC2
75A 75B	CH0S0	CH0R0
76A 76B	CH0S2	CH0R2
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

NT6X40DA

Product description

The NT6X40DA XPM DS512 link card is the electro-optical interface between fiber optic cables and the XMS peripheral module (XPM).

The NT6X40DA operates in XPMs like the digital trunk controller, line trunk controller or message switch buffer. The NT6X40DA requires the link control card NT6X40CA to provide a complete interface to the XPM.

Functional description

The NT6X40DA XPM DS512 link card is the electro-optical interface between fiber optic cables and the XMS peripheral module (XPM).

Technical data

Power requirements

The NT6X40DA card requires +5V with a variance of 5%. The NT6X40DA requires 1.3A of power.

Optical specifications

The following module specifications apply to the NT6X40DA:

- wavelength: 1300 nm
- bit error rate: 10E-12
- minimum launch power: -20 dBm
- receiver sensitivity: 28 dBm

A 12.5 cm/125 mm graded-index fiber can be used with an attenuation of 1.75 dB/km and a 3 dB bandwidth of 80 MHz/km. Use of this fiber means that the reach is beyond the specified 1000 m at 49.152 MHz.

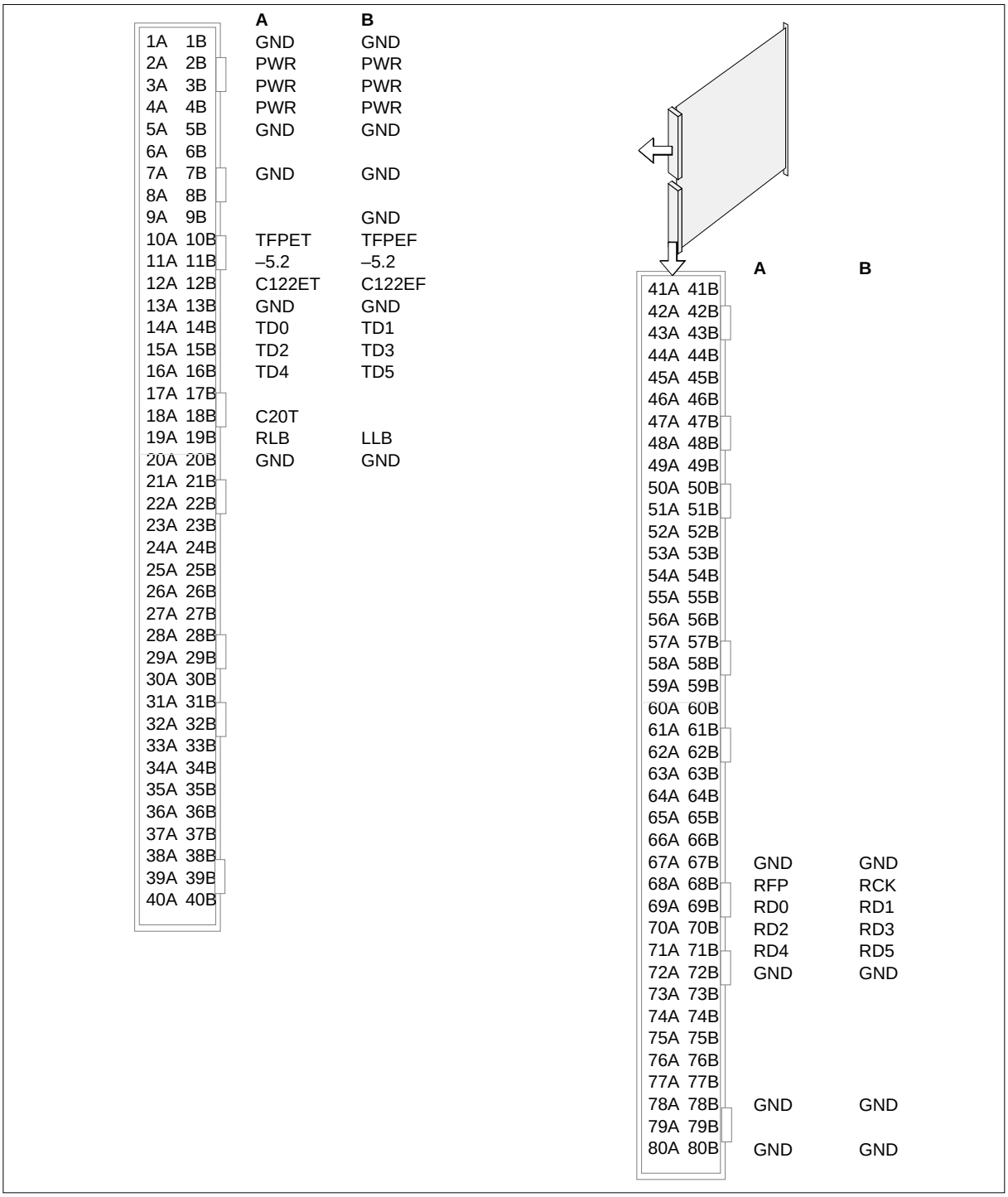
Signaling

Pin numbers

The pin numbers for the NT6X40DA appear in the following figure.

NT6X40DA (end)

NT6X40DA pin outs



NT6X40EA

Product description

The NT6X40EA allows DS512 optical fiber links and DS30 copper links on the extended multiprocessor system (XMS)-based peripheral module (XPM). This dual network appearance aids in the cutover process from the junctor network (JNET) to the enhanced network (ENET). The paddle board can be locally controlled to receive data from the JNET or the ENET. Cutover boards can be chained together and linked to a master control.

Location

The NT6X40EA is in the back of the XPM cabinet in a designed bracket the NT6X40EA shares with the NT6X40DA. The cutover paddle board does not plug into the backplane pins like the NT6X40DA. The cutover paddle board receives power and necessary logic signals through a ribbon cable connected to the NT6X40DA.

Functional description

The NT6X40EA is part of a cutover system. The cutover system involves the NT6X40DA fiber optic link paddle board and the NT6X40CA fiber optic link control card. The cutover system allows XPMs in an office to be equipped with a JNET and an ENET interface. When cutover occurs, you can connect all the NT6X40EA boards to a master control. The master control switches operation from the JNET to the ENET. After the cutover is complete, the NT6X40EA is removed and operation proceeds with the ENET.

Functional blocks

The NT6X40EA contains the following functional blocks:

- DS30 interface circuits
- XPM interface circuits
- remote local control circuits
- clock generation

DS30 interface circuits

The DS30 interface circuits block terminates the DS30 links to the current JNET. The W87D provides the interface circuits for two bidirectional DS30 links. The NT5L67AA provides dual bidirectional DS30 link termination. The two recovered frame pulses that the XPM master clock requires are taken from DS30 link 0 and DS30 link 2.

XPM interface circuits

The XPM interface circuits block latch the RXDATA from the W87s in the DS30 interface circuits. The XPM interface circuits presents the data to the

NT6X40EA (continued)

XPM control card, the NT6X40CA. Data from the XPM is buffered in this block before data goes to the W87s as TXDATA.

Remote local control circuits

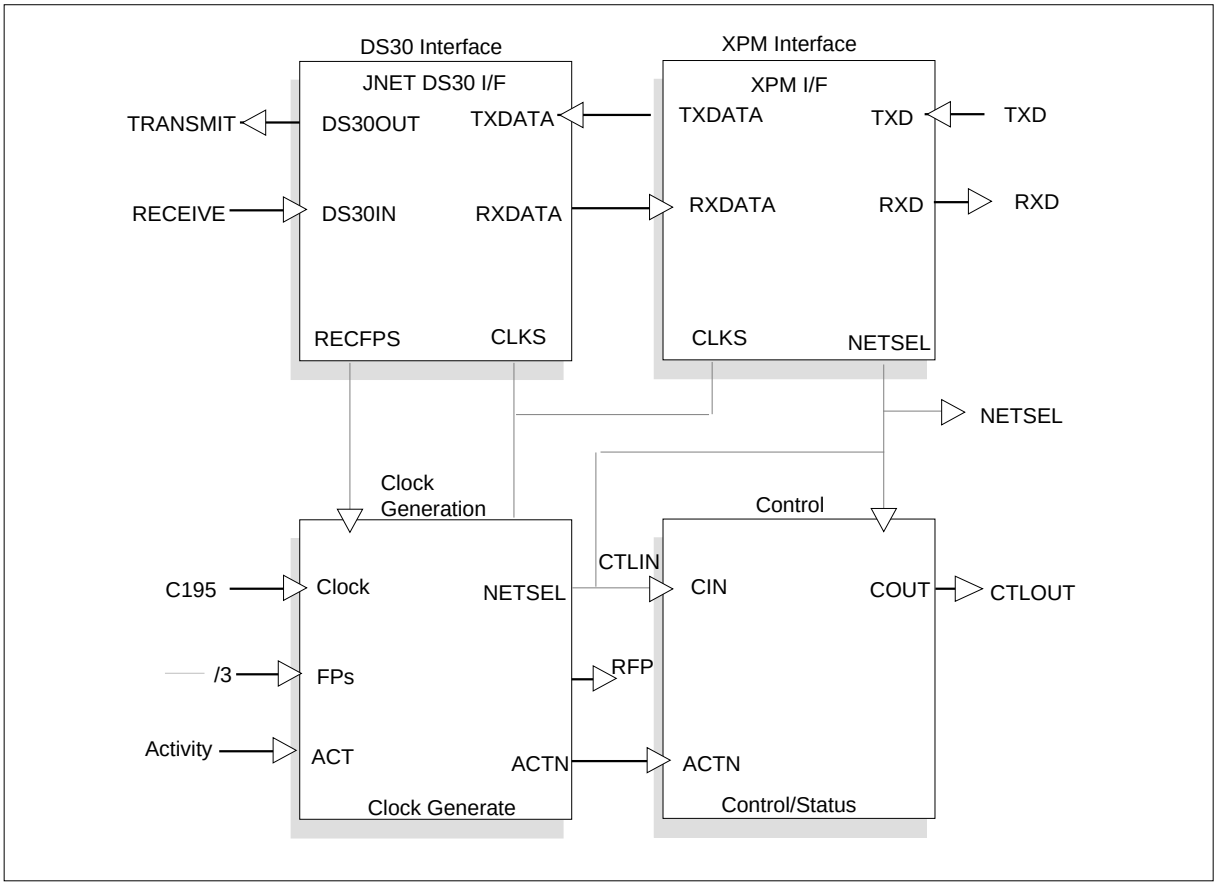
The control block contains circuits that communicate with a master control box through a nine-lead input cable. A nine-lead output cable provides continuity of the control box chain. The lastNT6X40EA in the chain has an output connector equipped with a shorting plug to complete the control loop. Use the master box to control the relays and switches in this block. Operate the relays and switches locally if the master box is not connected.

Clock generation

The clock generation block receives a 5.12 MHz clock and 97 ns frame pulse from the XPM. Two 390 ns frame pulses positioned to provide local and transmit frame pulses to the W87s are also input.

The relationship between the functional blocks appears in the following figure.

NT6X40EA functional blocks



Signaling

Pin numbers

The pin numbers for NT6X40EA appear in the following tables.

Clocking signals-connector J1 (Sheet 1 of 2)

Signal	Pin
C195T	15
FP97	32
FRM2	14
FRM1	31

NT6X40EA (continued)

Clocking signals-connector J1 (Sheet 2 of 2)

Signal	Pin
RECFP0	21
RECFP2	4

Control input signals-connector J2

Signal	Pin
CNTY	1
TIP	2
RING	3
ENIN	4
CNTYRET	5
ENERETIN	6
JNIN	7
SPAREIN	8
JNRET	9

Control output signals-connector J3 (Sheet 1 of 2)

Signal	Pin
CNTY	1
TIP	2
RING	3
ENIN	4
CNTYRET	5
ENRETIN	6
JNIN	7
SPAREIN	8

Control output signals-connector J3 (Sheet 2 of 2)

Signal	Pin
JRET	9

XPM interface signals-connector J1

Signal	Pin
TX0	25
TX1	8
TX2	24
TX3	7
TX4	23
TX5	6
TX6	22
TX7	5
RX0	30
RX1	13
RX2	29
RX3	12
RX4	28
RX5	11
RX6	27
RX7	10

Miscellaneous signals-connector J1 (Sheet 1 of 2)

Signal	Pin
NETSEL	16
ACT	33

NT6X40EA (continued)

Miscellaneous signals-connector J1 (Sheet 2 of 2)

Signal	Pin
+5V	17
+5V	34
GND	1
GND	2
GND	3
GND	9
GND	18
GND	19
GND	20
GND	26

DS30 port signals-connector J4 (Sheet 1 of 2)

Signal	Pin A	Signal	Pin B
TXN0	3	TXP0	3
TXN1	7	TXP1	7
TXN2	4	TXP2	4
TXN3	8	TXP3	8
TXN4	11	TXP4	11
TXN5	15	TXP5	15
TXN6	12	TXP6	12
TXN7	16	TXP7	16
TXN8	19	TXP8	19
TXN9	23	TXP9	23
TXN10	20	TXP10	20
TXN11	24	TXP11	24

DS30 port signals-connector J4 (Sheet 2 of 2)

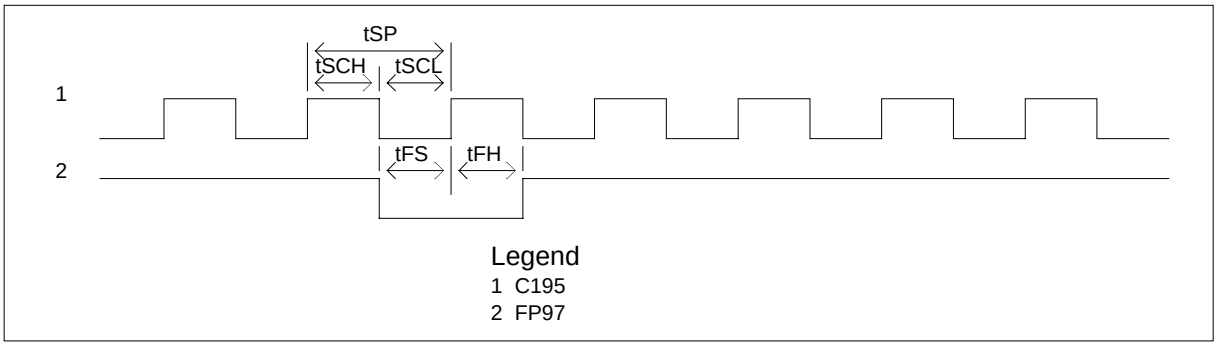
Signal	Pin A	Signal	Pin B
TXN12	27	TXP12	27
TXN13	31	TXP13	31
TXN14	28	TXP14	28
TXN15	32	TXP15	32
RXN0	1	RXP0	1
RXN1	5	RXP1	5
RXN2	2	RXP2	2
RXN3	6	RXP3	6
RXN4	9	RXP4	9
RXN5	13	RXP5	13
RXN6	10	RXP6	10
RXN7	14	RXP7	14
RXN8	17	RXP8	17
RXN9	21	RXP9	21
RXN10	18	RXP10	18
RXN11	22	RXP11	22
RXN12	25	RXP12	25
RXN13	29	RXP13	29
RXN14	26	RXP14	26
RXN15	30	RXP15	30

Timing

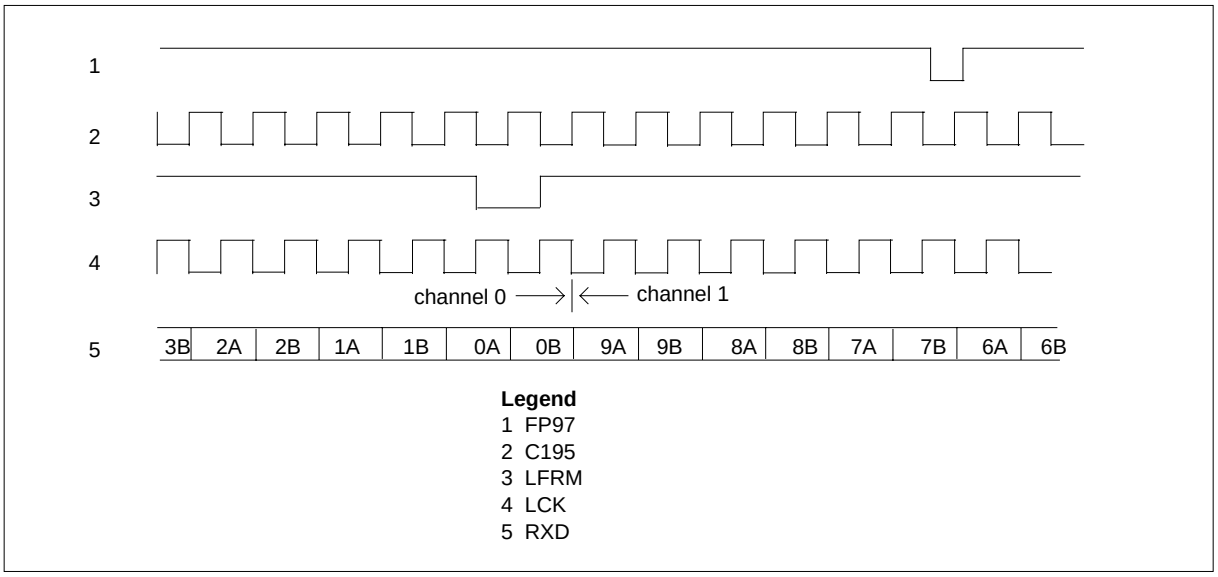
The timing for the NT6X40EA appears in the following figures.

NT6X40EA (continued)

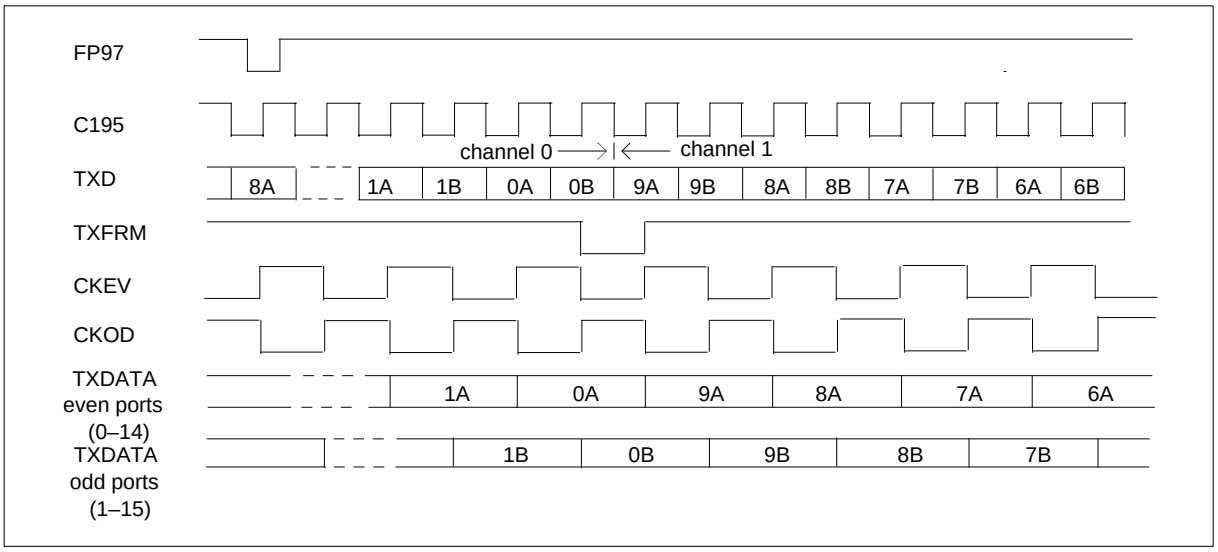
NT6X40EA clock and frame pulse timing



NT6X40EA DS30 port channel timing



NT6X40EA DS30 transmit timing



Technical data

Power requirements

The NT6X40EA requires 5V to operate.

NT6X40FA

Product description

The XMS-based peripheral module (XPM) DS512 link control card provides an interface. The interface is between 512 pulse code modulation (PCM) channels and an optical fiber link to the extended network (ENET). Each plane of the network requires one NT6X40FA.

Functional description

The NT6X40FA performs the following functions:

- DS512 interface to the NT6X40GA
- DS30 bit-interleaved serial data interface to the formatter card, NT6x41AA, and to the NT6X40EA during retrofits
- channel-0 send-and-receive interface to the messaging card
- link maintenance and digital phase-locked loop (DPLL) control that the microprocessor complex provides
- network looparound for each port and for each channel
- global looparound
- clock recovery with a crystal oscillator that voltage controls, and the B12 application-specified integrated circuit (ASIC) for DPLL control

Functional blocks

The NT6X40FA has the following functional blocks:

- formatter interface
- clock and frame pulse interface
- power-up and alarm-1 reset circuits
- network looparound
- channel-0 messaging interface
- 80C31 microprocessor complex
- B12 ASIC and DPLL circuit

Formatter interface

In the outgoing direction, the formatter interface receives DS60 data from the B12 ASIC. The formatter interface clocks the data again. The formatter interface sends the data to the formatter cards and to the network looparound circuit. The formatter cards are on the active and the mate NT6X41AA.

In the incoming direction, the formatter interface receives DS60 data from the formatter cards. The formatter interface applies time delay. The formatter

interface passes the selected data to the looparound circuit. The activity signal controls the selection of the active or the mate DS60 data.

Clock and frame pulse interface

The clock and frame pulse interface contains the different clocking and control signals that the NT6X40FA uses.

Power-up and alarm-1 reset circuits

The power-up circuit asserts the B12 ASIC reset and the 80C31 microprocessor reset momentarily after card insertion.

The alarm-1 reset circuit consists of a 7702 reset chip that generates a reset signal for the 80C31 microprocessor. The power-up circuit or an alarm 1 can reset the microprocessor.

Network looparound

The network looparound can be performed globally or for each channel. The ENET sends an alarm code that initiates the global looparound.

The formatter card, NT6X41AA, controls the looparound for each channel. The formatter card sends a control bit to the looparound multiplexer at the correct port and channel. The data from the receive side of the B12 ASIC loops back through multiplexers to the transmit side. This procedure occurs when a looparound is enabled for each channel. This procedure occurs after a delay RAM.

Channel-0 messaging interface

Channel-0 messages for port 0 and port 2 are extracted from the DS60 data stream during channel-0 time. The signal clocks the data. The clock and frame pulse interface generates the data. The data is passed on to the messaging card, not the formatter card. This block facilitates channel-0 looparound.

80C31 microprocessor complex

The 80C31 microprocessor complex contains of the microprocessor. The microprocessor performs the following functions:

- link maintenance
- control of B12 ASIC operations
- synchronization of the DPLL with the system clock
- control of global looparound

This block contains an EPROM that stores the firmware for the 80C31 microprocessor. The EPROM is 256 kbytes in size. An 8 bit data bus provides

NT6X40FA (continued)

the microprocessor with a communication path to the EPROM and the B12 ASIC.

B12 ASIC and DPLL circuit

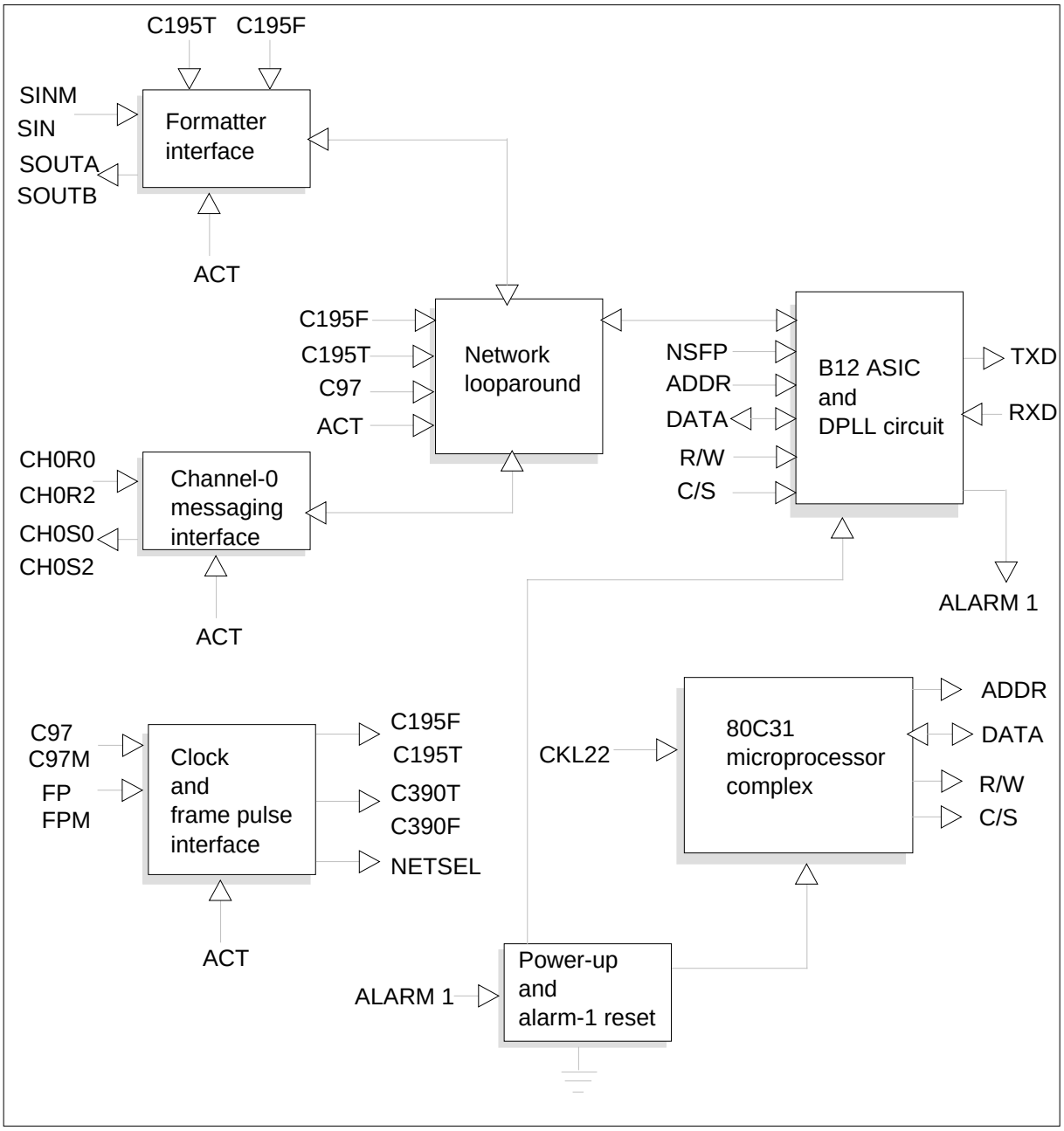
The B12 ASIC performs the following functions:

- digital clock recovery
- 12 bit serial to two 6 bit parallel data conversion
- two 6 bit parallel to 12 bit serial data conversion
- frame word detection
- decodes, encodes, and detects error and alarm codes (10B12B)
- false remote carrier group alarm suppression
- bit rate conversion (4.096 MHz to 5.12 MHz, and the reverse)
- formats parallel-to-serial and serial-to-parallel
- remote loopback
- alarm code 1 reset
- message insertion and removal for each channel during testing
- decodes and encodes ROM during testing
- bypasses formatter during testing

The digital phase-locked loop (DPLL) generates a 49.152 MHz clock for the B12 ASIC. The DPLL provides a crystal oscillator that voltage controls to perform this procedure.

The relationship between the functional blocks appears in the following figure.

NT6X40FA functional blocks



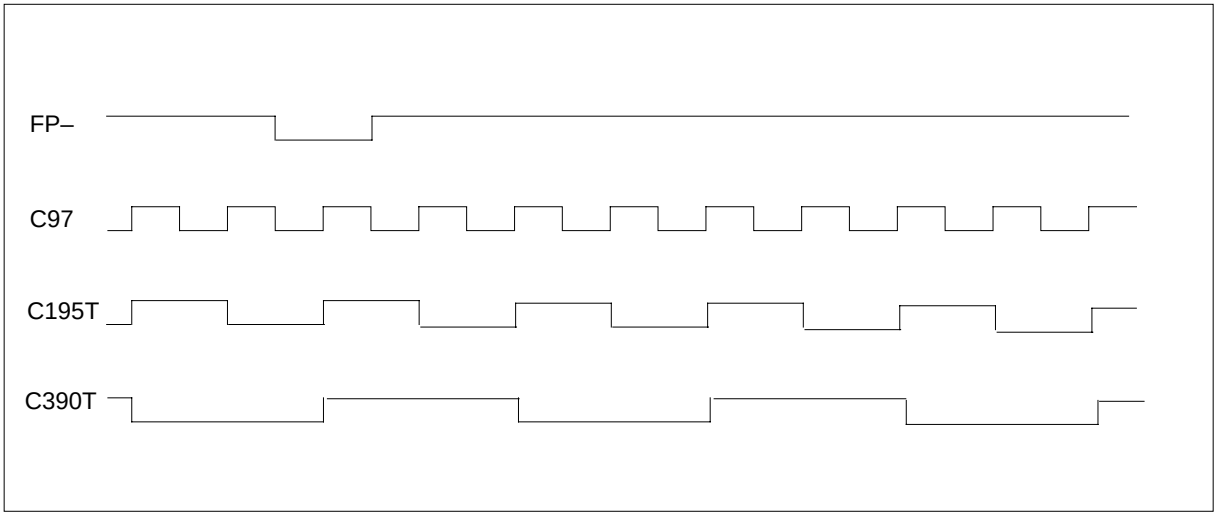
Signaling

Timing

The timing for the NT6X40FA appears in the following figure.

NT6X40FA (continued)

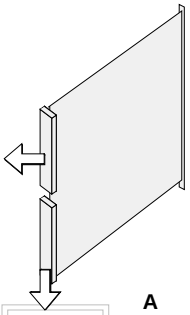
NT6X40FA PCM timing to and from the formatter card



Pin numbers

The pin numbers for the NT6X40FA appear in the following figure.

NT6X40FA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	PWR	PWR
3A 3B	PWR	PWR
4A 4B	PWR	PWR
5A 5B	GND	GND
6A 6B	FP	C97
7A 7B	GND	GND
8A 8B		
9A 9B	ACT	GND
10A10B		
11A11B	–5.2	–5.2
12A12B		
13A13B	GND	GND
14A14B	RXDF	RXDT
15A15B	THR	
16A16B		
17A17B		
18A18B		NETSEL
19A19B		
20A20B	GND	GND
21A21B		
22A22B		
23A23B		
24A24B		
25A25B		
26A26B	GND	GND
27A27B	SOUT01M	SOUT01
28A28B	SOUT23M	SOUT23
29A29B	SOUT45M	SOUT45
30A30B	SOUT67M	SOUT67
31A31B	SOUT89M	SOUT89
32A32B	SOUTABM	SOUTAB
33A33B	SOUTCDM	SOUTCD
34A34B	SOUTEFM	SOUTEF
35A35B	GND	GND
36A36B		
37A37B	FPM	C97M
38A38B		GND
39A39B		
40A40B		

	A	B
41A41B	GND	GND
42A42B		
43A43B	LPCNTM	LPCNT
44A44B		
45A45B	LPLTM	LPLT
46A46B	GND	GND
47A47B	SIN01M	SIN01
48A48B	SIN23M	SIN23
49A49B	SIN45M	SIN45
50A50B	SIN67M	SIN67
51A51B	SIN89M	SIN89
52A52B	SINABM	SINAB
53A53B	SINCDM	SINCD
54A54B	SINEFM	SINEF
55A55B		GND
56A56B	FP97	C195
57A57B	FR1	FR2
58A58B	RX0	RX1
59A59B	RX2	RX3
60A60B	RX4	RX5
61A61B	RX6	RX7
62A62B		
63A63B	TX0	TX1
64A64B	TX2	TX3
65A65B	TX4	TX5
66A66B	TX6	TX7
67A67B	GND	GND
68A68B		
69A69B		
70A70B		
71A71B	TXDT	TXDF
72A72B	GND	GND
73A73B	FPRC0	FPRC2
74A74B	FPRC0	FPRC2
75A75B	CH0S0	CH0R0
76A76B	CH0S2	CH0R2
77A77B		
78A78B	GND	GND
79A79B		
80A80B	GND	GND

NT6X40FA (end)

Technical data

Power requirements

NT6X40FA power requirements

Voltage	Tolerance	Current
-5.2V	±5%	0.16A
+5V	±5%	2.30A

NT6X40FB

Product description

The XMS-based peripheral module (XPM) DS512 link control card provides an interface. The interface is between 512 pulse code modulation (PCM) channels and an optical fiber link to the extended network (ENET). Each plane of the network requires one NT6X40FB.

Functional description

The NT6X40FB performs the following functions:

- DS512 interface to the NT6X40GA
- DS30 bit-interleaved serial data interface to the formatter card, NT6X41AA, and to the NT6X40EA during retrofits
- channel-0 send-and-receive interface to the messaging card
- link maintenance and digital phase-locked loop (DPLL) control that the microprocessor complex provides
- network looparound on a for each port and channel
- global looparound
- clock recovery with a crystal oscillator that voltage controls and the B12 application-specified integrated circuit (ASIC) for DPLL control
- C-side looparound of channel zero on ports on active and inactive planes

Functional blocks

The NT6X40FB contains the following functional blocks:

- formatter interface
- clock and frame pulse interface
- power-up and alarm-1 reset circuits
- network looparound
- C-side looparound
- channel-0 messaging interface
- 80C31 microprocessor complex
- B12 ASIC and DPLL circuit

Formatter interface

In the outgoing direction, the formatter interface receives DS60 data from the B12 ASIC. The formatter interface reclocks the data. The formatter interface sends the data to the formatter cards on the active and the mate NT6X41AA.

NT6X40FB (continued)

The formatter interface sends the data to the formatter cards on the network looparound circuit.

In the incoming direction, the formatter interface receives DS60 data from the formatter cards. The formatter interface applies time delay. The formatter interface passes the selected data to the looparound circuit. The activity signal controls the selection of the active or the mate DS60 data.

Clock and frame pulse interface

The clock and frame pulse interface contains the different clocking and control signals that the NT6X40FB uses.

Power-up and alarm-1 reset circuits

The power-up circuit asserts the B12 ASIC reset and the 80C31 microprocessor reset momentarily after card insertion.

The alarm-1 reset circuit consists of a 7702 reset chip that generates a reset signal for the 80C31 microprocessor. The power-up circuit or an alarm 1 can reset the microprocessor.

Network looparound

The network looparound can be performed globally for each channel. The alarm code that the ENET sends initiates global looparound.

The formatter card, NT6X41AA, controls the looparound for each channel. The formatter card sends a control bit to the looparound multiplexer at the proper port and channel. The data from the receive side of the B12 ASIC loops back through the multiplexers to the transmit side. This procedure occurs when a looparound is enable for each channel. This procedure occurs after a delay RAM.

C-side looparound

These circuits diagnose faults on both the active and inactive units. The circuits provide a loop path back to the XPM through each plane. The loop path back is for both the active and inactive units.

Each unit can perform the looparound separately. The circuits provide a loop path only for channel zero on all ports. The formatter card (NT6X41AA) controls activation. The formatter card sends a control bit to the looparound multiplexer at the correct port and channel time. The formatter interface serial data input (SIN) side loops back through multiplexers to the formatter interface serial port output (SOUT) side. This procedure occurs when the C-side loop is enabled.

Channel-0 messaging interface

Channel-0 messages for port 0 and port 2 are extracted from the DS60 data stream during channel-0 time. The signal clocks data. The clock and frame pulse interface generates data. Data passes on to the messaging card, not the formatter card. This block facilitates channel-0 looparound.

80C31 microprocessor complex

The 80C31 microprocessor complex contains the microprocessor, which performs the following functions:

- link maintenance
- control of B12 ASIC operations
- synchronization of the DPLL with the system clock
- control of global looparound

This block contains an EPROM that stores the firmware for the 80C31 microprocessor. The EPROM is 256 kbytes in size. An 8 bit data bus provides the microprocessor with a communication path to the EPROM and the B12 ASIC.

B12 ASIC and DPLL circuit

The B12 ASIC performs the following functions:

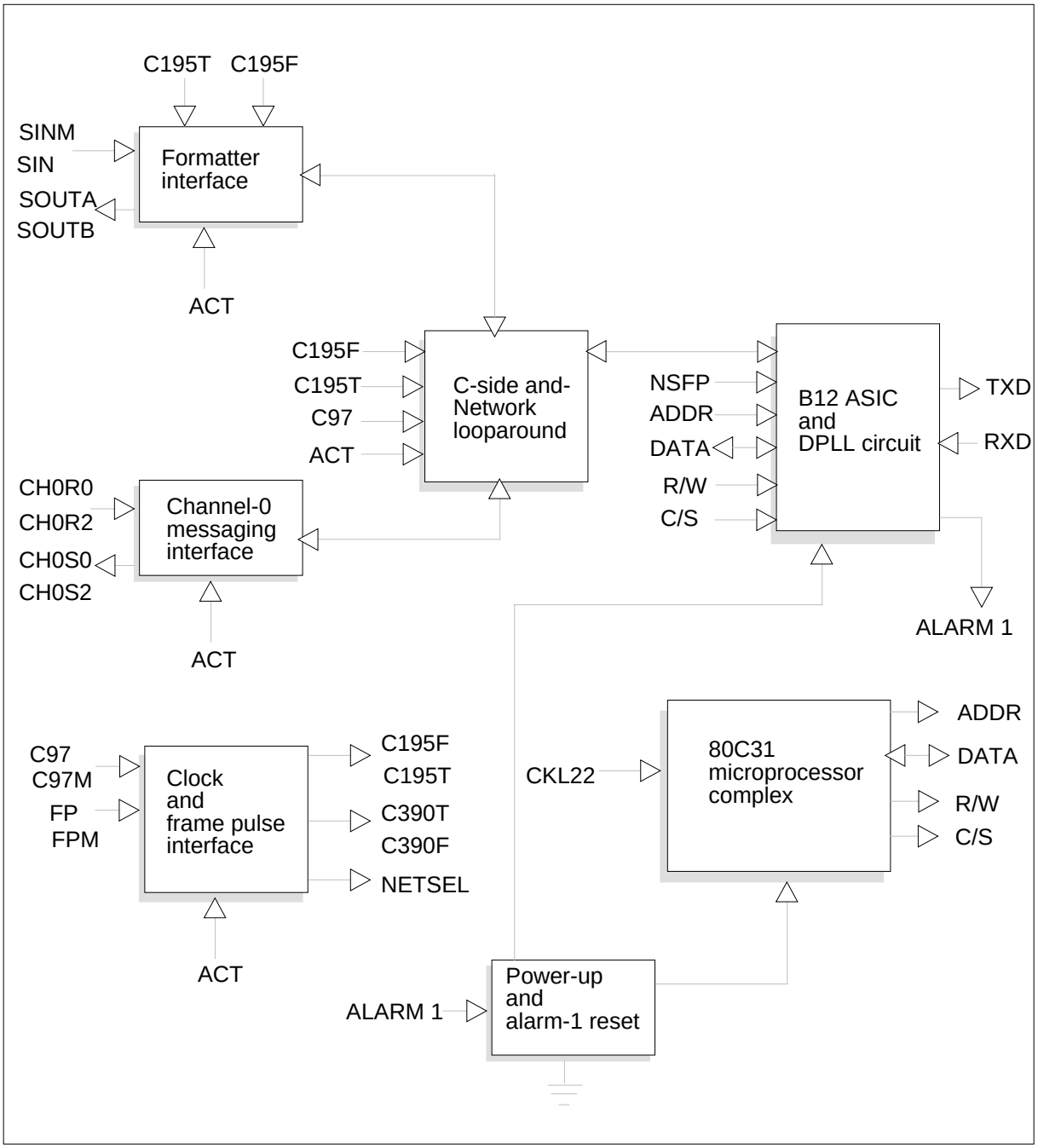
- digital clock recovery
- 12 bit serial to two 6 bit parallel data conversion
- two 6 bit parallel to 12 bit serial data conversion
- frame word detection
- decodes, encodes, and detects error and alarm code (10B12B)
- false remote carrier group alarm suppression
- bit rate conversion (4.096 MHz to 5.12 MHz, and the reverse)
- format parallel-to-serial and serial-to-parallel
- remote loopback
- alarm code 1 reset
- message insertion and extraction for each channel during testing
- decodes and encodes ROM during testing
- bypasses formatter during testing

The digital phase-locked loop (DPLL) provides a crystal oscillator that voltage controls to generate a 49.152 MHz clock for the B12 ASIC.

NT6X40FB (continued)

The relationship between the functional blocks appears in the following figure.

NT6X40FB functional blocks

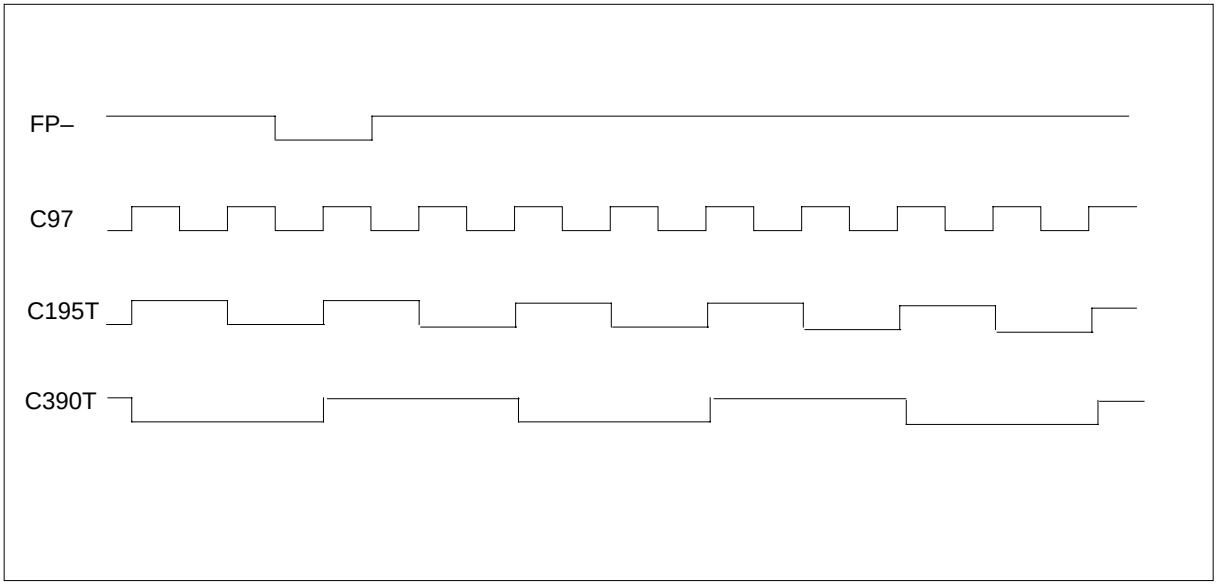


Signaling

Timing

The timing for the NT6X40FB appears in the following figure.

NT6X40FB PCM timing to and from the formatter card

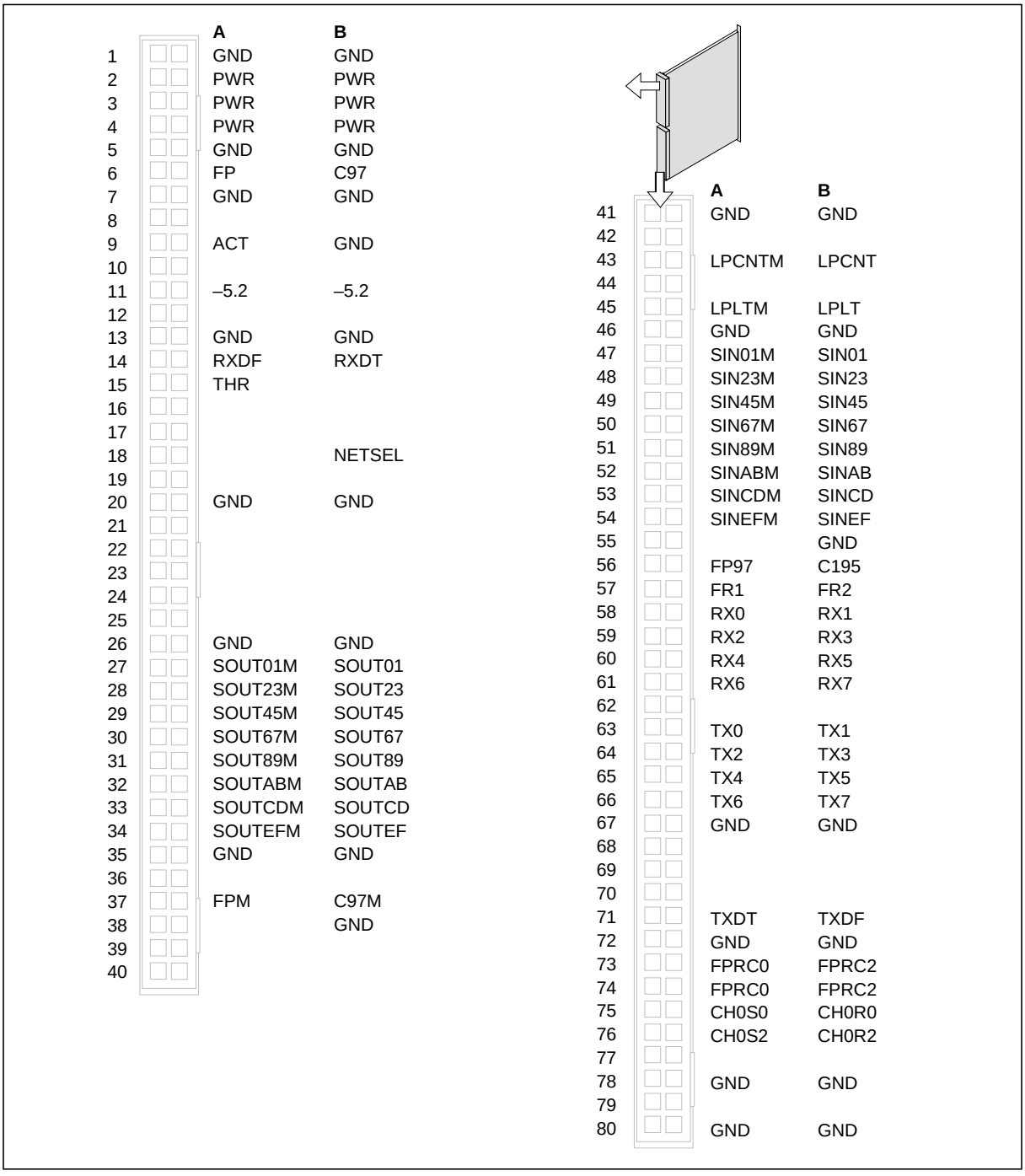


Pin numbers

The pin numbers for the NT6X40FB appear in the following figure.

NT6X40FB (end)

NT6X40FB pin numbers



NT6X40FC

Product description

NT6X40FC, the XMS-based peripheral module (XPM) DS512 link control card, provides an interface. The interface is between 512 pulse code modulation (PCM) channels and an optical fiber link to the extended network (ENET). Each plane of the network requires one NT6X40FC.

Functional description

The NT6X40FC performs the following functions:

- DS512 interface to the NT6X40GA
- DS30 bit-interleaved serial data interface to the formatter card, NT6X41AA, and to the NT6X40EA during retrofits
- channel-0 send-and-receive interface to the messaging card
- link maintenance and digital phase-locked loop (DPLL) control that the microprocessor complex provides
- network looparound on a for each port and channel
- global looparound
- clock recovery with a crystal oscillator that voltage controls and the B12 application-specified integrated circuit (ASIC) for DPLL control
- C-side looparound of channel zero on ports on active and inactive planes

Functional blocks

The NT6X40FC contains the following functional blocks:

- formatter interface
- clock and frame pulse interface
- power-up and alarm-1 reset circuits
- network looparound
- C-side looparound
- channel-0 messaging interface
- 80C31 microprocessor complex
- B12 ASIC and DPLL circuit

Formatter interface

In the outgoing direction, the formatter interface receives DS60 data from the B12 ASIC. The formatter interface reclocks the data. The formatter interface sends the data to the formatter cards on the active and the mate NT6X41AA.

NT6X40FC (continued)

The formatter interface sends the data to the formatter cards on the network looparound circuit.

In the incoming direction, the formatter interface receives DS60 data from the formatter cards. The formatter interface applies time delay. The formatter interface passes the selected data to the looparound circuit. The activity signal controls the selection of the active or the mate DS60 data.

Clock and frame pulse interface

The clock and frame pulse interface contains the different clocking and control signals that the NT6X40FC uses.

Power-up and alarm-1 reset circuits

The power-up circuit asserts the B12 ASIC reset and the 80C31 microprocessor reset momentarily after card insertion.

The alarm-1 reset circuit consists of a 7702 reset chip that generates a reset signal for the 80C31 microprocessor. The power-up circuit or an alarm 1 can reset the microprocessor.

Network looparound

The network looparound can be performed globally for each channel. The alarm code that the ENET sends initiates global looparound.

The formatter card, NT6X41AA, controls the looparound for each channel. The formatter card sends a control bit to the looparound multiplexer at the proper port and channel. The data from the receive side of the B12 ASIC loops back through the multiplexers to the transmit side. This procedure occurs when a looparound is enable for each channel. This procedure occurs after a delay RAM.

C-side looparound

These circuits diagnose faults on both the active and inactive units. The circuits provide a loop path back to the XPM through each plane. The loop path back is for both the active and inactive units.

Each unit can perform the looparound separately. The circuits provide a loop path only for channel zero on all ports. The formatter card (NT6X41AA) controls activation. The formatter card sends a control bit to the looparound multiplexer at the correct port and channel time. The formatter interface serial data input (SIN) side loops back through multiplexers to the formatter interface serial port output (SOUT) side. This procedure occurs when the C-side loop is enabled.

Channel-0 messaging interface

Channel-0 messages for ports 0, 2, and 4-15 are extracted from the DS60 data stream during channel-0 time. Messages are extracted from the DS60 data stream from the formatter card. Then they pass to the messaging card. Messages received from the messaging card are inserted into the DS512 stream out to the network. Data passes on to the messaging card, not the formatter card. This block facilitates channel-0 looparound.

80C31 microprocessor complex

The 80C31 microprocessor complex contains the microprocessor, which performs the following functions:

- link maintenance
- control of B12 ASIC operations
- synchronization of the DPLL with the system clock
- control of global looparound

This block contains an EPROM that stores the firmware for the 80C31 microprocessor. The EPROM is 256 kbytes in size. An 8 bit data bus provides the microprocessor with a communication path to the EPROM and the B12 ASIC.

B12 ASIC and DPLL circuit

The B12 ASIC performs the following functions:

- digital clock recovery
- 12 bit serial to two 6 bit parallel data conversion
- two 6 bit parallel to 12 bit serial data conversion
- frame word detection
- decodes, encodes, and detects error and alarm code (10B12B)
- false remote carrier group alarm suppression
- bit rate conversion (4.096 MHz to 5.12 MHz, and the reverse)
- format parallel-to-serial and serial-to-parallel
- remote loopback
- alarm code 1 reset
- message insertion and extraction for each channel during testing
- decodes and encodes ROM during testing
- bypasses formatter during testing

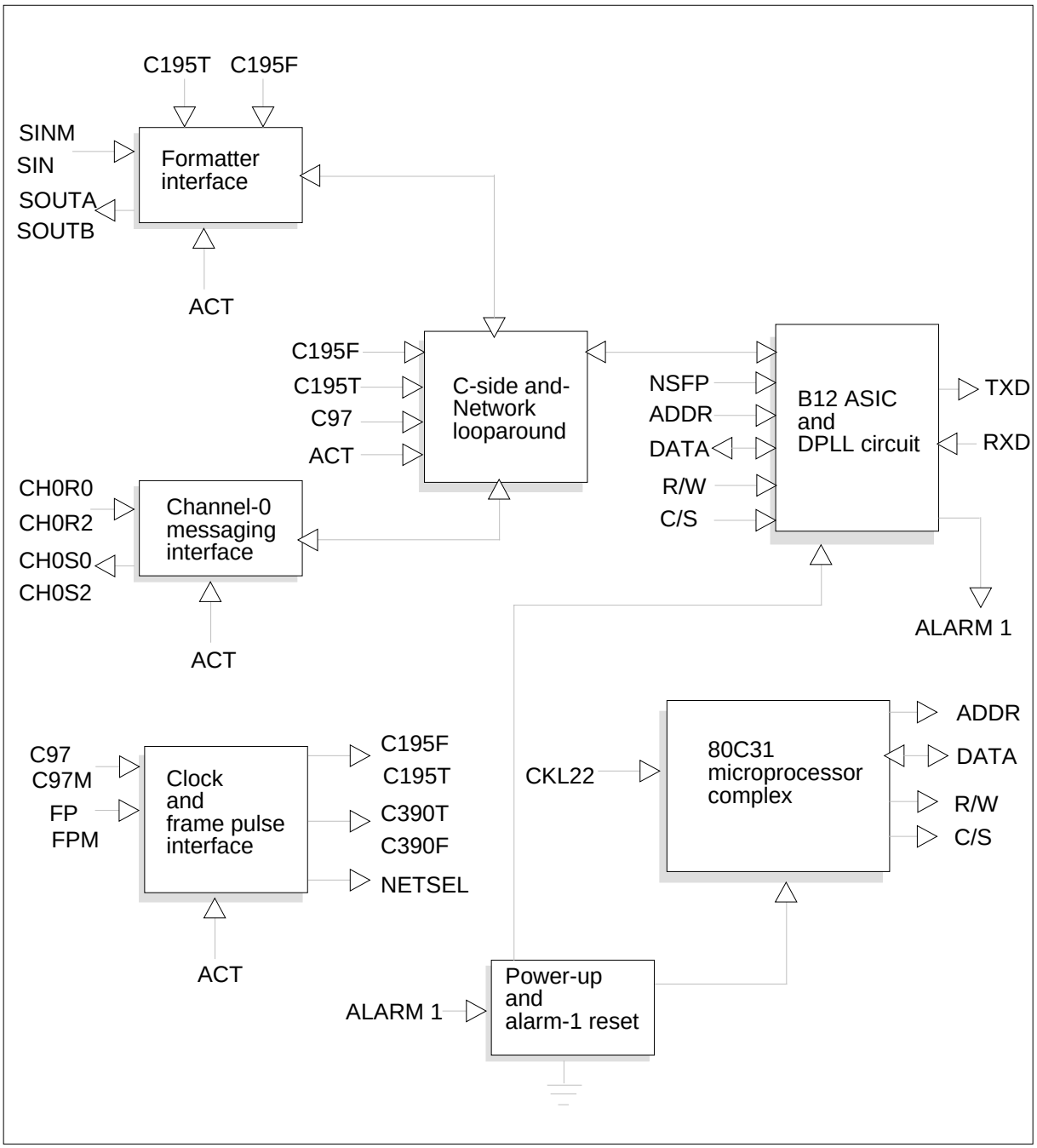
NT6X40FC (continued)

The digital phase-locked loop (DPLL) provides a crystal oscillator that voltage controls to generate a 49.152 MHz clock for the B12 ASIC.

The relationship between the functional blocks appears in the following figure.

NT6X40FC (continued)

NT6X40FC functional blocks



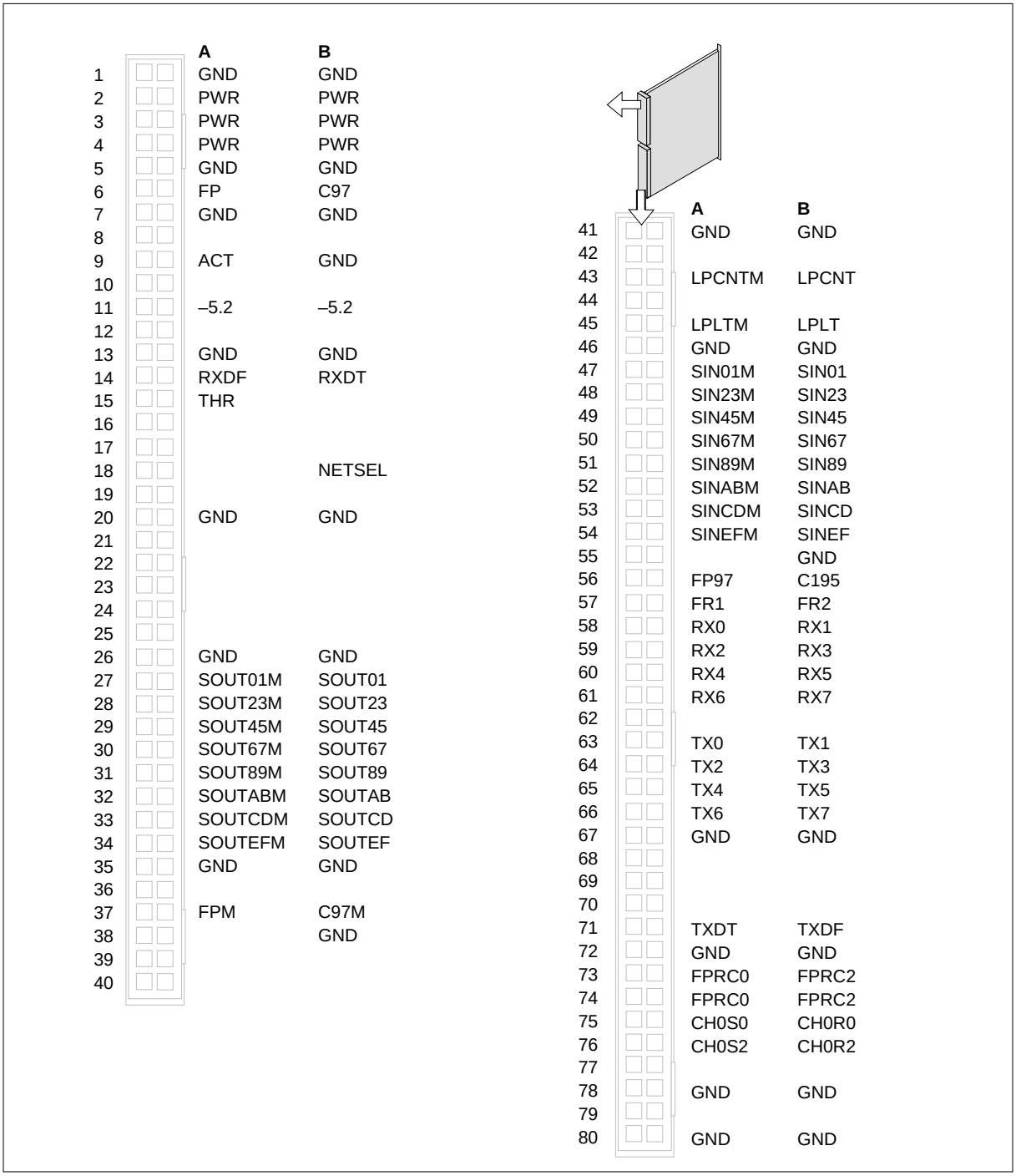
NT6X40FC (continued)

Signaling

Pin numbers

The pin numbers for the NT6X40FC appear in the following figure.

NT6X40FC pin numbers



	A	B
1	GND	GND
2	PWR	PWR
3	PWR	PWR
4	PWR	PWR
5	GND	GND
6	FP	C97
7	GND	GND
8		
9	ACT	GND
10		
11	–5.2	–5.2
12		
13	GND	GND
14	RXDF	RXDT
15	THR	
16		
17		
18		NETSEL
19		
20	GND	GND
21		
22		
23		
24		
25		
26	GND	GND
27	SOUT01M	SOUT01
28	SOUT23M	SOUT23
29	SOUT45M	SOUT45
30	SOUT67M	SOUT67
31	SOUT89M	SOUT89
32	SOUTABM	SOUTAB
33	SOUTCDM	SOUTCD
34	SOUTEFM	SOUTEF
35	GND	GND
36		
37	FPM	C97M
38		GND
39		
40		

	A	B
41	GND	GND
42		
43	LPCNTM	LPCNT
44		
45	LPLTM	LPLT
46	GND	GND
47	SIN01M	SIN01
48	SIN23M	SIN23
49	SIN45M	SIN45
50	SIN67M	SIN67
51	SIN89M	SIN89
52	SINABM	SINAB
53	SINCDM	SINCD
54	SINEFM	SINEF
55		GND
56	FP97	C195
57	FR1	FR2
58	RX0	RX1
59	RX2	RX3
60	RX4	RX5
61	RX6	RX7
62		
63	TX0	TX1
64	TX2	TX3
65	TX4	TX5
66	TX6	TX7
67	GND	GND
68		
69		
70		
71	TXDT	TXDF
72	GND	GND
73	FPRC0	FPRC2
74	FPRC0	FPRC2
75	CH0S0	CH0R0
76	CH0S2	CH0R2
77		
78	GND	GND
79		
80	GND	GND

NT6X40GA

Product description

The NT6X40GA links the enhanced network (ENET) with the XMS-based peripheral module (XPM). The card is on the XPM side and interfaces the ENET with a DS-512 optical fiber link. Use the NT6X40GA with the NT6X40FA link control card.

Location

The NT6X40GA plugs in the back of the shelf at the NT6X40FA card position (slot 22 of the XPM).

Functional description

Use the NT6X40GA with the NT6X40FA in XPMs. The NT6X40GA provides the DS-512 interface to ENET through a fiber optic cable. The NT6X40GA interfaces with the NT6X40EA by a ribbon cable. The NT6X40GA provides a path for the power and signals that the NT6X40EA requires from the backplane.

Functional blocks

The NT6X40GA contains the following operating blocks:

- power converter
- fiber optic modules
- terminations

Power converter

The dc-to-dc power converter generates a -5.2V output from the +5V input received from the backplane. The fiber modules use -5.2V. The -5.2V is supplied to the NT6X40FA through the backplane.

Fiber optic modules

The two fiber optic modules are the transmitter and the receiver. The transmitter is QFT01A. The receiver is QFR01A. Fiber optic cables from the ENET join to ST connectors on each module. The modules are in a 14-pin plastic dual inline package (DIP). The transmitter sends data from the NT6X40FA to the ENET at a rate of 49.152 Mbps. The receiver receives data at 49.152 Mbps from ENET and transfers the data to the NT6X40FA.

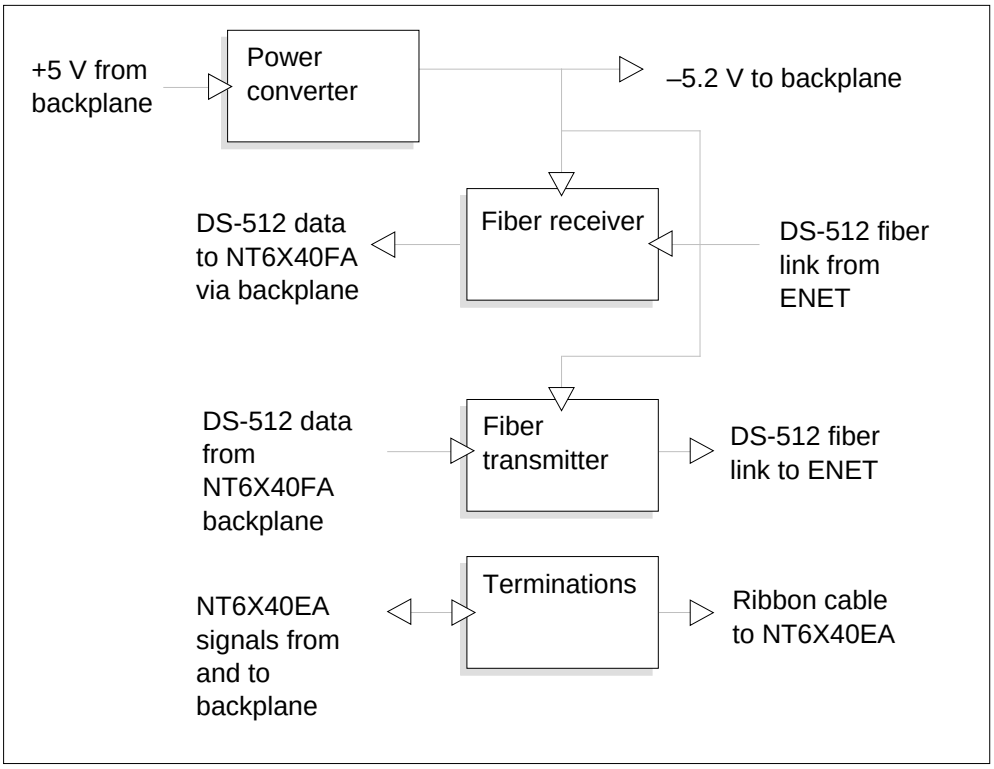
The fiber optic modules require a -5.2V &0xb1;5% voltage supplied from the dc-to-dc converter.

Terminations

The NT6X40GA, through the backplane, provides the NT6X40EA with the power and signals that the NT6X40EA requires. The NT6X40GA is a path for signals between the NT6X40FA and the NT6X40EA. The terminations for these signals are between the backplane connectors and the ribbon cable connector.

The relationship between the operating blocks appears in the following figure.

NT6X40GA functional blocks

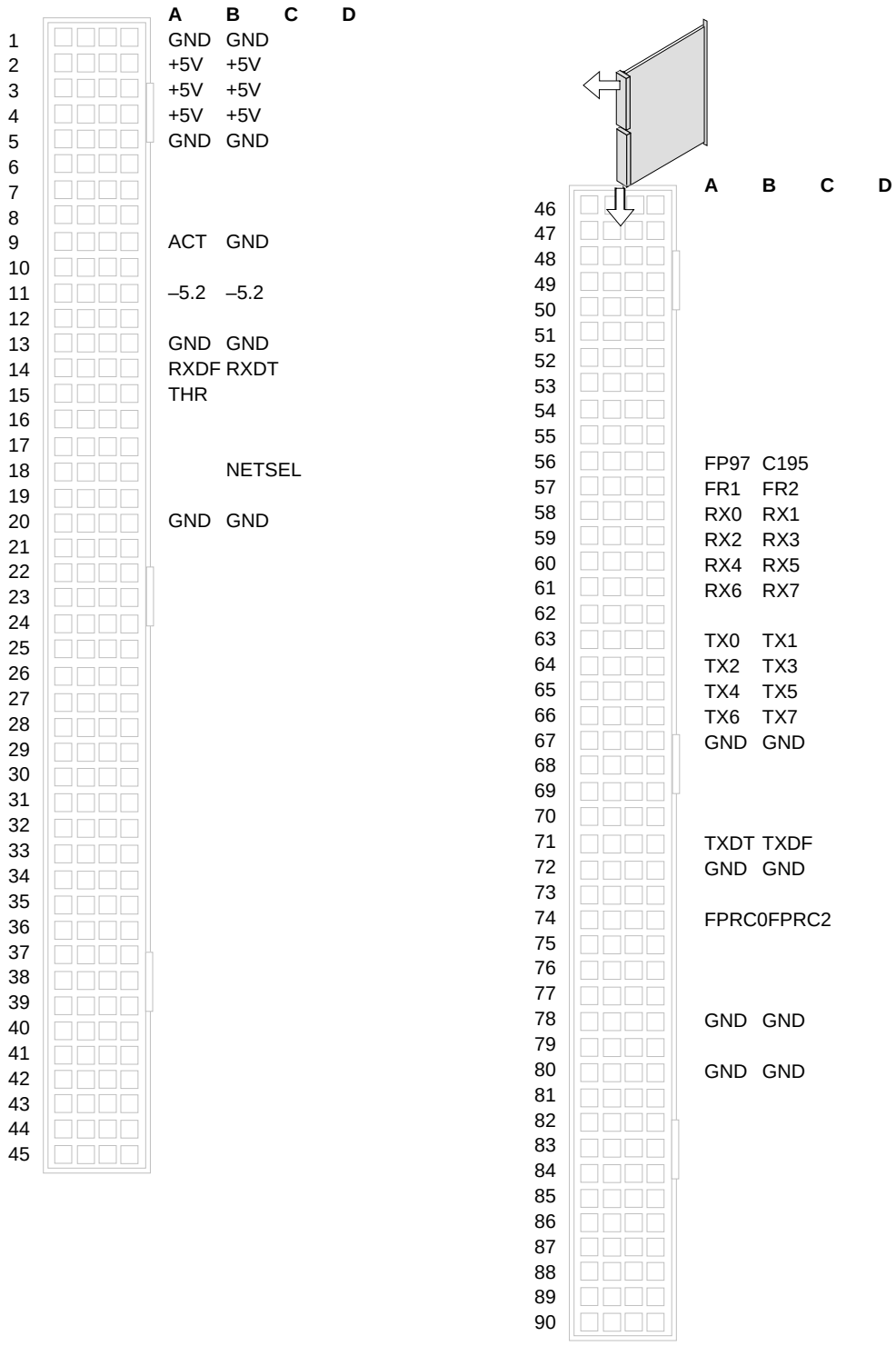


Signaling

Pin numbers

The pin numbers for connector P1 appear in the following figure.

NT6X40GA (continued)



The pin numbers for connector J1 appear in the following table.

J1 pin numbersouts

Pin	Signal	Pin	Signal
3	ACT	15	RX6
4	NETSEL	16	RX7
5	FP97	19	TX0
6	C195	20	TX1
7	FR1	21	TX2
8	FR2	22	TX3
9	RX0	23	TX4
10	RX1	24	TX5
11	RX2	25	TX6
12	RX3	26	TX7
13	RX4	27	FPRC0
14	RX5	28	FPRC2

Technical data

Power requirements

The minimum supply voltage is 4.75V. The nominal supply voltage is 5V. The maximum supply voltage is 5.2V. The maximum output noise is 50mV peak-to-peak. The maximum supply current is 600mA.

NT6X41AA

Product description

The NT6X41AA formatter card is between the 6X40AA DS30 card and the 6X42AA CSM card. The NT6X41AA contains the formatting section and the clock section. The clock section generates the 10.24 MHz shelf clock. The clock section generates signals that other parts of the shelf use, like FP, FP40 and FP48.

The formatting section of the card handles 16 DS30 ports in both directions. The main features of the formatting section are the following:

- parallel-to-serial conversion of the transmit pulse code modulated (XPCM) data
- serial-to-parallel conversion of the receive pulse code modulated (RPCM) data
- network plane selection
- channel supervision message (CSM) looparound
- network looparound
- parity error generation
- raw T1 clock generation

Functional description

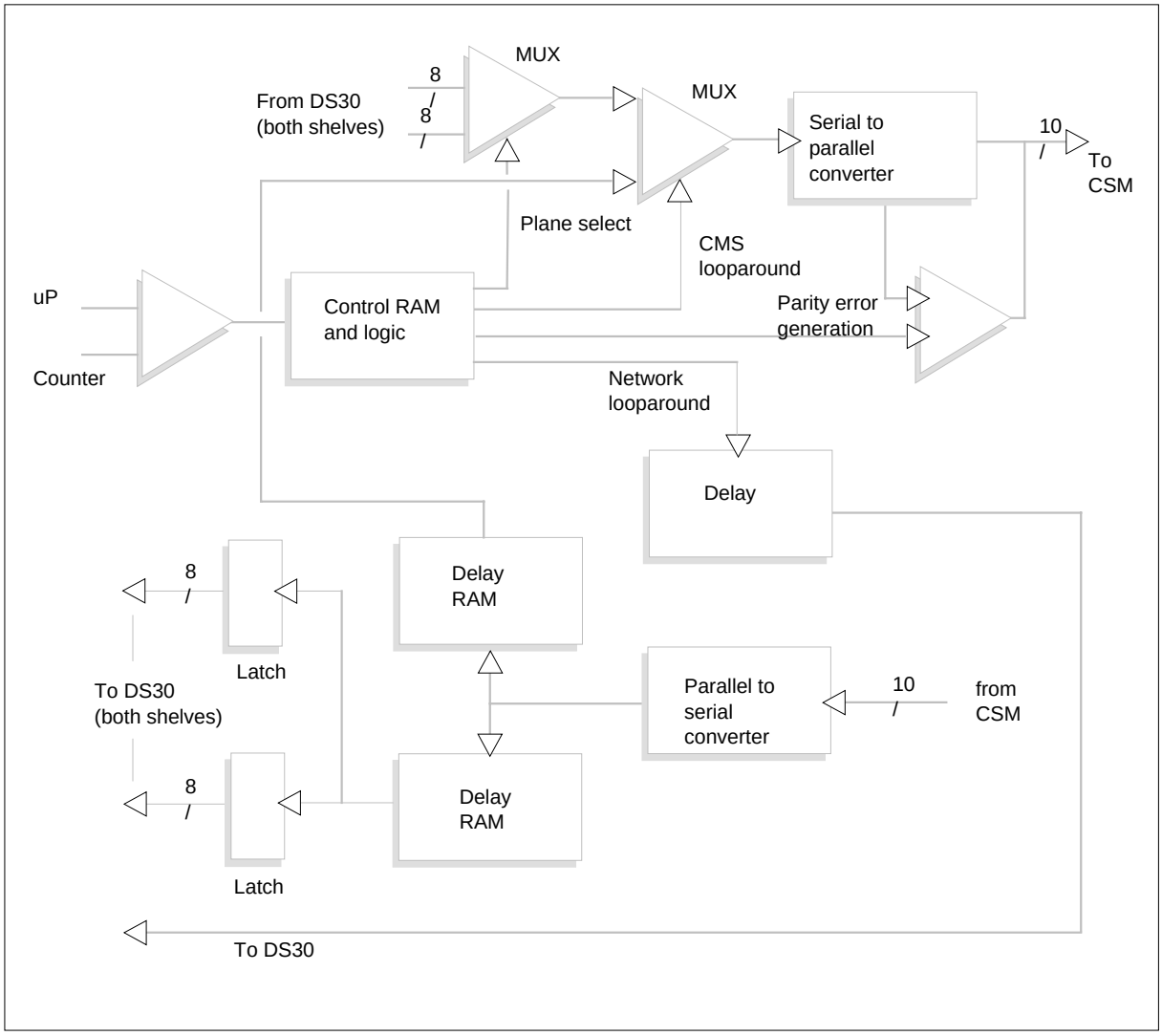
Functional blocks

The NT6X41AA has the following functional blocks:

- RPCM speech path
- XPCM speech path
- control RAM and logic
- signaling processor (SP) interface
- raw T1 clock generation

The relationship between the functional blocks appears in the following figure.

NT6X41AA functional blocks



Raw T1 clock generation

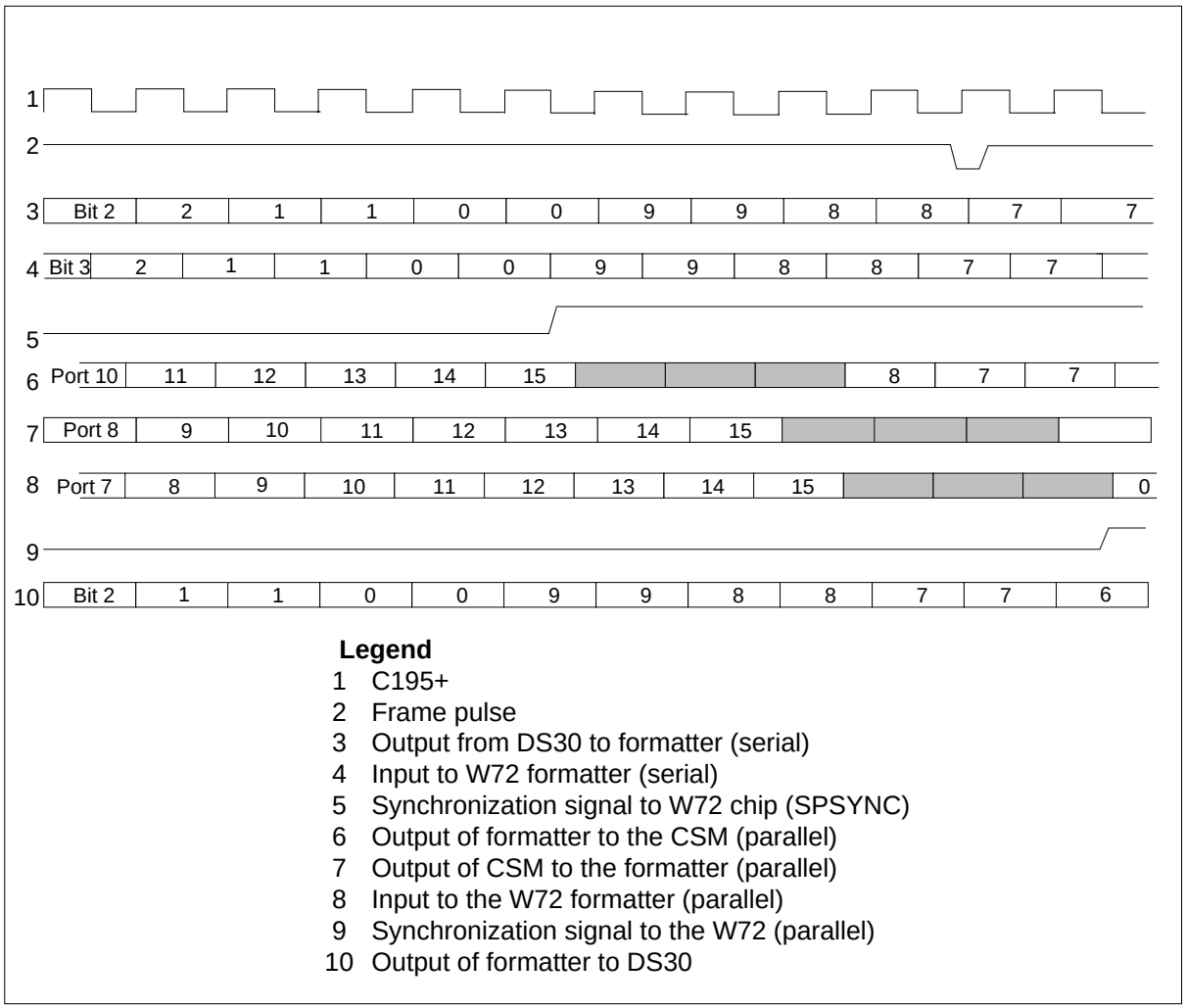
A PROM-based clock circuit generates a clock frequency of 3.088 MHz (two times T1). The NT6X50 cards have this clock.

Signaling

The timing for the NT6X41AA appears in the following figure.

NT6X41AA (end)

NT6X41AA timing



Legend

1 C195+
2 Frame pulse
3 Output from DS30 to formatter (serial)
4 Input to W72 formatter (serial)
5 Synchronization signal to W72 chip (SPSYNC)
6 Output of formatter to the CSM (parallel)
7 Output of CSM to the formatter (parallel)
8 Input to the W72 formatter (parallel)
9 Synchronization signal to the W72 (parallel)
10 Output of formatter to DS30

NT6X41AB

Product description

The NT6X41AB is the international version of the NT6X41AA formatter card. The situates between the NT6X40AA DS30 card and the NT6X42AA channel supervision message (CSM) card. The NT6X40AA consists of a formatting section and a clock section. The clock section generates the 10.24-MHz shelf clock signal. The clock section generates a number of other signals that different other parts of the shelf use, like FP, FP40 and FP48.

The formatting section of the card handles sixteen DS30 ports in both directions. The main features of the formatting section are as follows:

- parallel-to-serial conversion of transmit pulse code modulated (XPCM) data
- serial-to-parallel conversion of receive pulse code modulated (RPCM) data
- network plane selection
- CSM looparound
- network looparound
- parity error generation
- raw T1 clock generation

Functional description

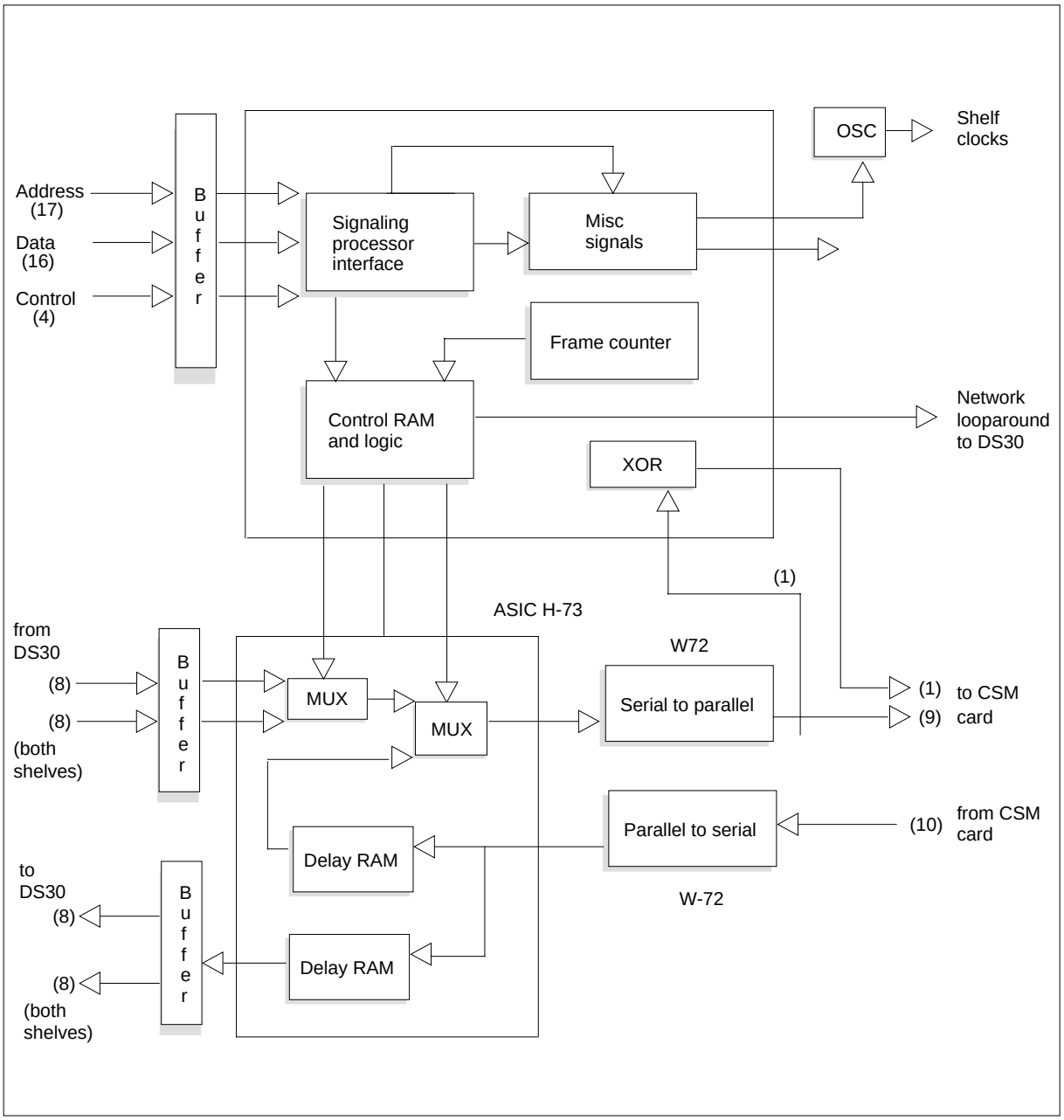
Functional blocks

The NT6X41AB contains the following operating blocks:

- RPCM speech path
- XPCM speech path
- control RAM
- signaling processor (SP) interface
- raw T1 clock generation

The operating relationship between the preceding blocks appears in the following figure.

NT6X41AB (continued)



RPCM and XPCM speech paths

Each serial line from the DS30 cards contains two DS30 ports that are multiplexed together. The plane select multiplexer in the H-73 PCM handler selects the network plane from which to receive data. You can select multiplexing for each port or for each channel. A control RAM controls the

selection and resides in the H-74 clock and processor interface. The RPCM data is passed through a CSM looparound multiplexer (MUX). The MUX switches looped-around XPCM data in to the RPCM data path. The looped-around XPCM data is delayed by almost one frame time to match the same channel time. Serial RPCM data is latched and presented to the formatter chip. The formatter chip converts the data into a 10-bit wide parallel bus. The bus is latched and buffered to the 6X42AA CSM card.

The parity bit of the parallel bus goes through an additional XOR logic gate before the parity bit leaves the card. A bit from the control RAM controls the XOR control gate. This process provides the ability to induce parity error in the parallel bus for each port or each channel for maintenance purposes. The parallel speech bus from the CSM card is latched and presented to the formatter chip. The chip converts the 10-bit parallel bus into eight two-port serial outputs. Serial data is written in to two sets of delay RAM. One set of RAM provides the required delay for the XPCM looparound data, before the data is presented to the CSM looparound MUX. The other set of RAM adjusts the delay of the XPCM path to produce a total delay of 40 bits in the line trunk controller (LTC). Outputs of the RAMs are latched and buffered to the DS30 cards in the two shelves.

Control RAM and signaling processor interface

The control RAM in H-74 is a four-bit wide memory. During the active time, a counter chain sequences the contents of the memory. The SP can access the memory during dead times. Memory controls plane selection, CSM looparound, parity error generation, and network looparound. Network looparound loops 10-bit serial data back to the network in both planes. The accurate looparound occurs on the DS30 cards. Only the control signals are sent to the DS30 cards in both shelves.

The plane selection and CSM looparound outputs of the RAM are written into two sets of shift registers and latches in H-74. The shift registers convert the serial control bits of all ports into parallel form. These signals control serial PCM data that is one channel time long. The latches store the parallel control bits. The latches retain the control bits for one channel time, while the control bits of the next channel shift out.

A 16-bit data interface for the SP is in H-74. The formatting circuit uses the least important four bits of the high byte of each word. The clock circuit uses the least important 12 bits of a word. The most important 4 bits are not used. The SP access to the control RAM is denied during active times until dead times occur. The SP can access the clock circuit at any time.

NT6X41AB (end)

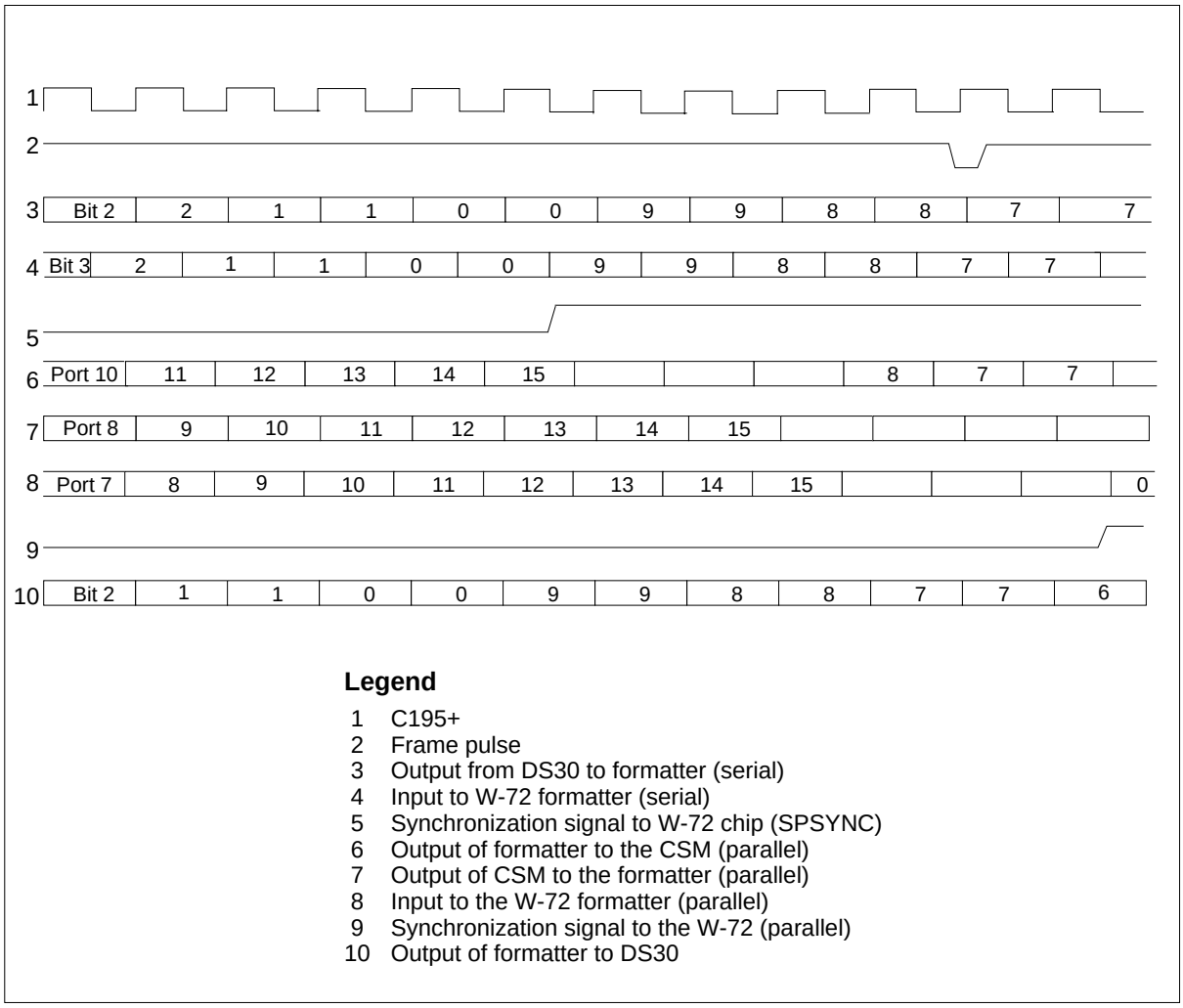
Raw T1 clock generation

A PROM-based clock circuit generates a clock frequency of 3.088 MHz (two times T1). This clock is distributed to NT6X50 cards.

Signaling

The timing for the NT6X41AB appears in the following figure.

NT6X41AB timing



Legend

1 C195+
2 Frame pulse
3 Output from DS30 to formatter (serial)
4 Input to W-72 formatter (serial)
5 Synchronization signal to W-72 chip (SPSYNC)
6 Output of formatter to the CSM (parallel)
7 Output of CSM to the formatter (parallel)
8 Input to the W-72 formatter (parallel)
9 Synchronization signal to the W-72 (parallel)
10 Output of formatter to DS30

NT6X41AC

Product description

The NT6X41AC is the international version of the NT6X41AA formatter card. The NT6X41AC situates between the NT6X40AA DS30 card and the NT6X42AA channel supervision message (CSM) card. The NT6X40AA consists of a formatting section and a clock section. The clock section generates the 10.24-MHz shelf clock signal. The clock section generates a number of other signals that different other parts of the shelf use, like FP, FP40 and FP48.

The formatting section of the card handles sixteen DS30 ports in both directions. The main features of the formatting section are as follows:

- parallel-to-serial conversion of transmit pulse code modulated (XPCM) data
- serial-to-parallel conversion of receive pulse code modulated (RPCM) data
- network plane selection
- CSM looparound
- network looparound
- parity error generation
- raw T1 clock generation

Functional description

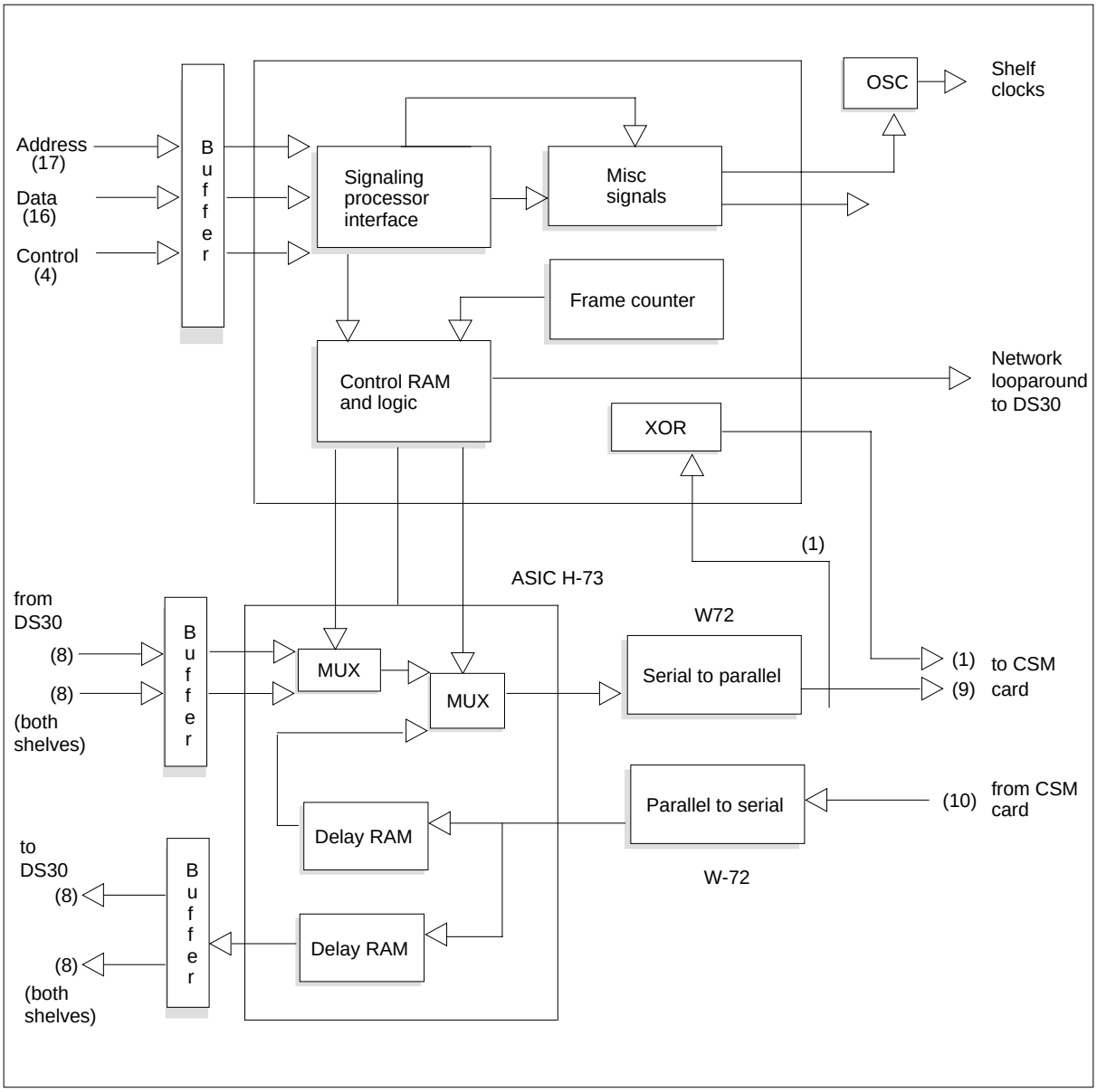
Functional blocks

The NT6X41AC contains the following operating blocks:

- RPCM speech path
- XPCM speech path
- control RAM
- signaling processor (SP) interface
- raw T1 clock generation

The operating relationship between the preceding blocks appears in the following figure.

NT6X41AC (continued)



RPCM and XPCM speech paths

Each serial line from the DS30 cards contains two DS30 ports that are multiplexed together. The plane select multiplexer in the H-73 PCM handler selects the network plane from which to receive data. You can select multiplexing for each port or for each channel. A control RAM controls the selection and resides in the H-74 clock and processor interface. The RPCM data is passed through a CSM looparound multiplexer (MUX). The MUX

switches looped-around XPCM data in to the RPCM data path. The looped-around XPCM data is delayed by almost one frame time to match the same channel time. Serial RPCM data is latched and presented to the formatter chip. The formatter chip converts the data into a 10-bit wide parallel bus. The bus is latched and buffered to the 6X42AA CSM card.

The parity bit of the parallel bus goes through an additional XOR logic gate before the parity bit leaves the card. A bit from the control RAM controls the XOR control gate. This process provides the ability to induce parity error in the parallel bus for each port or each channel for maintenance purposes. The parallel speech bus from the CSM card is latched and presented to the formatter chip. The chip converts the 10-bit parallel bus into eight two-port serial outputs. Serial data is written in to two sets of delay RAM. One set of RAM provides the required delay for the XPCM looparound data, before the data is presented to the CSM looparound MUX. The other set of RAM adjusts the delay of the XPCM path to produce a total delay of 40 bits in the line trunk controller (LTC). Outputs of the RAMs are latched and buffered to the DS30 cards in the two shelves.

Control RAM and signaling processor interface

The control RAM in H-74 is a four-bit wide memory. During the active time, a counter chain sequences the contents of the memory. The SP can access the memory during dead times. Memory controls plane selection, CSM looparound, parity error generation, and network looparound. Network looparound loops 10-bit serial data back to the network in both planes. The accurate looparound occurs on the DS30 cards. Only the control signals are sent to the DS30 cards in both shelves.

The plane selection and CSM looparound outputs of the RAM are written into two sets of shift registers and latches in H-74. The shift registers convert the serial control bits of all ports into parallel form. These signals control serial PCM data that is one channel time long. The latches store the parallel control bits. The latches retain the control bits for one channel time, while the control bits of the next channel shift out.

A 16-bit data interface for the SP is in H-74. The formatting circuit uses the least important four bits of the high byte of each word. The clock circuit uses the least important 12 bits of a word. The most important 4 bits are not used. The SP access to the control RAM is denied during active times until dead times occur. The SP can access the clock circuit at any time.

Raw T1 clock generation

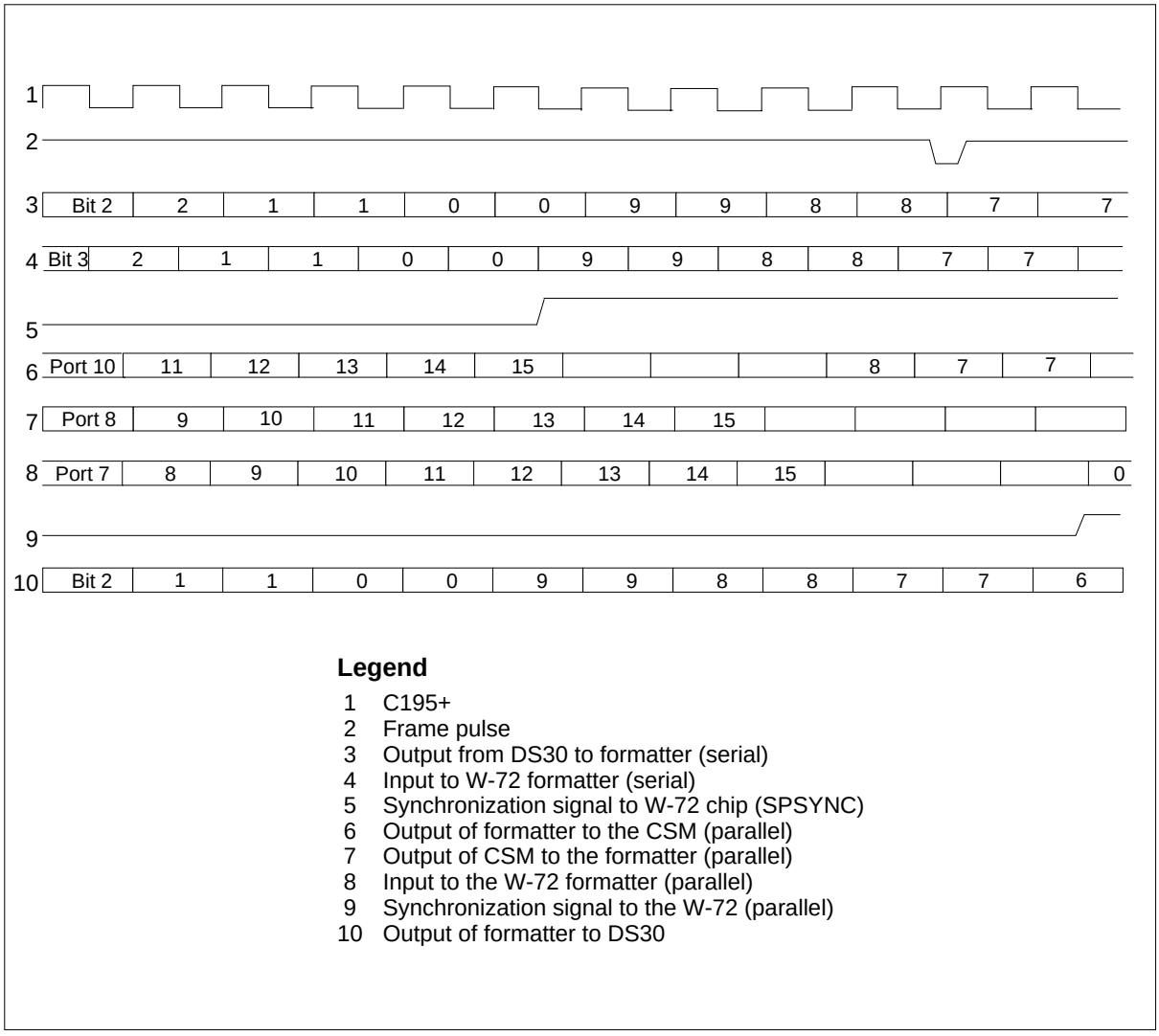
A PROM-based clock circuit generates a clock frequency of 3.088 MHz (two times T1). This clock is distributed to NT6X50 cards.

NT6X41AC (end)

Signaling

The timing for the NT6X41AC appears in the following figure.

NT6X41AC timing



Legend

1 C195+
2 Frame pulse
3 Output from DS30 to formatter (serial)
4 Input to W-72 formatter (serial)
5 Synchronization signal to W-72 chip (SPSYNC)
6 Output of formatter to the CSM (parallel)
7 Output of CSM to the formatter (parallel)
8 Input to the W-72 formatter (parallel)
9 Synchronization signal to the W-72 (parallel)
10 Output of formatter to DS30

NT6X42AA

Product description

The NT6X42AA channel supervision message (CSM) card performs the functions required for channel supervision messaging between peripherals. The CSM card can accommodate 16 network ports or 512 channels. A channel connection between two peripherals establishes a duplex path that transmits a 10-bit byte in each direction every frame time. The parity bit maintains odd parity for all bytes that transmit. The CSM bit provides a 3.2-Kbps message link between the connected peripherals for each path setup. The channel data byte (CDB) transmits the information required to set up, maintain, and terminate a call. The central control for every path setup gives the value of the 8-bit integrity byte. This byte makes sure that a pulse code modulation (PCM) path setup from one peripheral to another is correct. This byte can measure the quality of the speech path in the connection.

Location

The NT6X42AA communicates with the NT6X41AA formatter card on the network side of the card. The NT6X42AA originates the 8-bit parallel receive PCM (RPCM) bus on the peripheral side and terminates the transmit PCM (XPCM) speech bus.

Functional description

The main functions of the NT6X42AA are as follows:

- CSM bit removal from network channels
- parity checking on all bytes, and insertion of a transmit synchronization pattern and a CSM into the PCM path
- frame and logic counting
- CDB and expected accuracy checking
- accuracy match (IM) and parity error reporting
- synchronization pattern transmission
- provision of a signaling processor (SP) interface

CSM bit removal from network channels

The 10-bit parallel bus from the NT6X41AA formatter card passes through the CSM and exits at the 8-bit RPCM speech bus. The circuitry board strips the CMS parity bit off the bus and processes the bit. A set of shifter RAMs collect the CMS bit. The synchronization pattern detector monitors the output from the RAM. Results from the detector are passed to circuits that keeps track of the frame position for each channel. The circuits record parity error and the supervision (SV) bit for each channel. When the outputs from the RAMs detect a synchronization pattern, the frame counter circuit records this and waits for

NT6X42AA (continued)

the CDB and integrity byte. The integrity value is compared with the expected integrity. An IM can be present and a parity error does not always appear for this channel in the last 40 frames. In this event, the received CDB is updated in to a CDB RAM for the SP. An error report RAM for the SP stores the results of the IM and parity check.

Parity checking and the PCM path

The 10-bit parallel bus from the formatter card is latched in the card on the increasing edge of the C195+ clock. The bus is latched out of the card on the following rising edge. Only one 195-ns clock cycle delay through the card occurs. The parity of the most significant 9 bits of the bus is compared with the least significant parity bit. The frame counter circuit reads the result of the comparison and the error report RAM stores the comparison.

A read-modify-write operation is performed on the 16-bit-wide shifter RAMs every 195 ns. A set of counters that are clocked at the same rate address memory locations of the RAMs in sequence. Two registers read and latch the contents of the RAMs in the first half of the C195+ clock cycle. In the latter half of the cycle, the bits are written back to the RAMs. The bits are shifted in position by one and the latest CSM bit received fills the least significant bit. The synchronization pattern detector decodes the outputs of the RAMs; if 16 ones (1) and a zero (0) least significant bit occur, the output of the detector is high.

Frame and logic counting

This section of the circuit keeps track of the frame position and records a parity error flag and an SV bit for all channels. Frame and logic counting contains a set of 8-bit RAMs, adder and randon logics. A read-modify-write operation is performed on the RAMs every 195 ns. The lower 5-bits are counter bits. The adder adds 1 to the last count and increments the count. The next bit is the synchronization bit, which records if a synchronization is found. The parity error bit records if a parity error ever occurred in the current frame, and is cleared at the end of the 40-frame series. The most significant bit is the SV bit, which stores the last SV bit received. This bit is updated at the end of the 40-frame if a parity error does not occur in that frame.

The SV bit in the counter circuit is 0 and the count can be any value. When a synchronization pattern is detected, the SV bit is set to 1 and the counter is forced to 1. The counter begins to increase after every frame until the counter reaches 15 (hexadecimal F). Randon logics decode this together with the SV bit and produce a signal that signifies the end of the frame. This signal clears the counter and sets the SV bit to 0. Other circuits use this signal as a flag to perform an update. The counter increases from 0 until the counter reaches the end of the synchronization pattern. At this point, a check is made for synchronization. If a synchronization occurs, the counter is set to 0 and the SV

bit is set to 1. If a synchronization does not occur, a signal goes high, which signifies a loss of synchronization.

Channel data byte and expected integrity checking

The expected integrity and received CDB are stored in the same set of RAMs, even though the addresses are 4 Kbytes apart. This condition accommodates different SP access requirements. The set of RAMs is divided in two. The lower half is for expected accuracy, and the upper half is for received CDB. A set of multiplexers that normally select the counters as addresses drive the addresses. On the first half of the C195+ clock cycle, the expected integrity value of the incoming time slot is read and compared with the received integrity. The result of the comparison is normally ignored until the signal 39 occurs, and the result is stored. The SP can access the expected integrity RAM only during dead times.

The received CDB uses the second half of the clock cycle. The accurate update of a CDB occurs one clock cycle after the integrity byte is received. This pause allows time for an integrity check. At the end of a 40-frame series, an IM can be present and a parity error does not always occur. In this event, the latched CDB is stored in the RAM. The SP can read the received CDB, unless an update is going occur in the next clock cycle. The SP access delays until an update does not occur or until dead time occurs.

Accuracy match and parity error reporting

The results of parity checking and an IM are stored in a set of RAMs as flags. The RAMs are 16 bits wide and each location represents a network channel, for example 16 ports. The IM bit is updated only at the end of a 40-frame series. The IM bit is set to 0 when there an IM is not present. A loss of synchronization signal is gated with the IM bit. This sets the IM bit to 0 when a loss of synchronization occurs.

In the last two time slots of dead time, the IM and parity results of one channel are read out from the RAMs. Two sets of 16-bit wide shift registers store the results. During active times, these bits are rotated at one bit for each time slot. These bits are gated with the new results of that port or channel. At the end of active times, all bits are updated. The results are written back into the RAMs during the first two cycles of dead times. The SP can access all locations during active times, except when the channel that the SP tries to access is currently under operation. This condition delays access for one channel time to avoid error.

Synchronization pattern transmission

The CSM card receives the 8-bit parallel XPCM bus and inserts the transmit CSM bit and parity bit into the bus. The parallel bus is buffered to the formatter

card. The XPCM bus latches into the card on the falling edge of the C195+ clock. The transmit CSM bit is inserted as B1. An odd parity bit (B0) is generated. The 10-bit word is latched out of the card on the next falling edge of the clock. Only one C195+ clock delay through the card is present.

Two sets of RAMs store the transmit CDB and accuracy. The SP can access the first set to load in new CDB and accuracy values. The SP cannot access second set. The contents of the second set of RAMs are transmitted out as the CSM bit. The hardware copies the contents from the first set of RAMs to the second set. This occurs in the last two frames before the end of the synchronization pattern. A control signal from the PROM determines when the synchronization pattern is enabled as the CSM bit.

SP interface

An 8-bit data bus is provided for the SP. When the SP requests access to RAMs on board, processor-grant circuits compares the access window of the RAMs. These circuits produce a signal when the grant window occurs. This signal also starts the access cycle. Access windows are different for each of the RAMs.

The different access conditions of the RAMs are as follows:

- transmit CDB: all times, except active times of the last two frames before the end of the synchronization pattern
- transmit accuracy: same as transmit CDB
- receive CDB: all times unless the system performs a CDB update in the next clock cycle
- expected accuracy: only during dead times
- IM bits: active times unless the accessed channel is the current PCM channel
- parity error bits: same as IM bits

NT6X42CA

Product description

The NT6X42CA channel supervision message (CSM) card is a development of the NT6X42AA card, with a minor hardware change. The NT6X42CA performs the functions required for channel supervision messaging between peripherals.

The hardware change brings the SPLITN signal to a pin that was not used. This action adds the ability to split the transmit pulse code modulation (XPCM) speech bus in digital CCITT Signaling System 5 (N5) line signaling systems. The N5 tones (2400 Hz and 2600 Hz) are used in international networks for circuit supervisory functions.

In order to provide digital N5 signaling on DMS-300 equipment, the PCM30 digital trunk controller (PDTC) must be equipped with the NT6X62CA. The PCM30 must also include the following three cards:

- the NT6X42DA (specialized tone receiver (STR).
- the NT6X92CA (universal tone receiver (UTR) tone detection),
- the NT6X69LA (common peripheral processor (CPP) message protocol and tones).

The ability to split the channel for each call is also required. The splitting prevents the leakage of tones to additional exchanges in the link-by-link signaling path. The CSM uses a CHSPLIT signal from the STR to perform the splitting function,

Both units of the PDTC must be equipped with CSM cards that can perform the splitting function. The backplane of both units of the PDTC must be fitted with the backplane strap. This strap carries the CHSPLIT signal from the STR to the CSM.

The CSM is for use in the DMS group of extended multiprocessor system (XMS)-based peripheral modules (XPM). The CA version of this card is for PDTC/international digital trunk controller (IDTC) XPMs used in N5 signaling applications. The CA version maintains all the functionality of the AA version and is backward compatible.

Location

The NT6X42CA fits in slot 21 in NT6X02 shelves, in NT6X01 and NTFX33AA frames. On the network side of the card, the connects to the NT6X41 formatter card. On the peripheral side, the connects to the transmit and to the receive pulse code modulation (RPCM) speech buses.

NT6X42CA (continued)

Functional description

The CCITT N5 signaling system uses inband tones that are sent as pulse code modulation (PCM) samples in place of speech data. The link-by-link function of this system requires the ability to detect the incoming signaling tones in a stated time. The next step is to split the speech channel. The splitting occurs so that the tone does not propagate. The tone propagates through the network and out to the next switch on the route.

The STR card detects the N5 tones and produces the split signal. The NT6X42CA card detects the split signal and disables the speech bus, toward the network. The NT6X42CA replaces the N5 tone sample with a known steady value.

The NT6X42CA contains the following functions:

- insertion and removal of the CSM bit in each of the 512 channels of the peripheral
- parity generation and checking on each byte
- transmission of a synchronization pattern
- assembling the received channel data byte (CDB) for each channel
- checking the channel integrity byte
- splitting the transmit PCM (XPCM) bus for each channel, when the card is used in the CCITT N5 link-by-link signaling system
- accommodates 16 network ports or 512 channels

The CSM bit provides a 3.2-Kbps message link between the connected peripherals for each path setup. The CDB transmits the information required to set up, maintain, and stop a call. The central control for every path set up gives the value of the 8-bit integrity byte. This step makes sure that the PCM path set up from one peripheral to another is correct. This step provides a method to measure the quality of the speech path in the connection.

Functional blocks

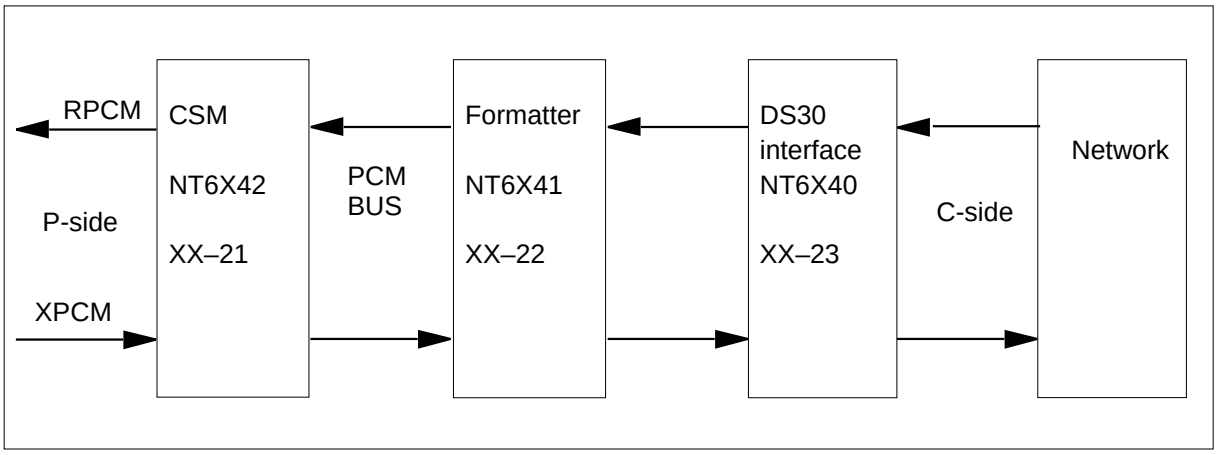
The NT6X42CA contains the following functional blocks:

- parity check
- CSM shifter and synchronization detector
- accuracy match
- channel supervision message frame counter and decoder
- expected accuracy (EI) and CDB RAM

- processor interface (receive)
- clock and frame counters (receive)
- parity generator
- channel data byte accuracy RAM
- parallel-to-serial converter
- accuracy and parity error report RAM
- processor interface (transmit)
- clock and frame counters (transmit)

The location of the NT6X42CA in the XPM shelf appears in the following figure.

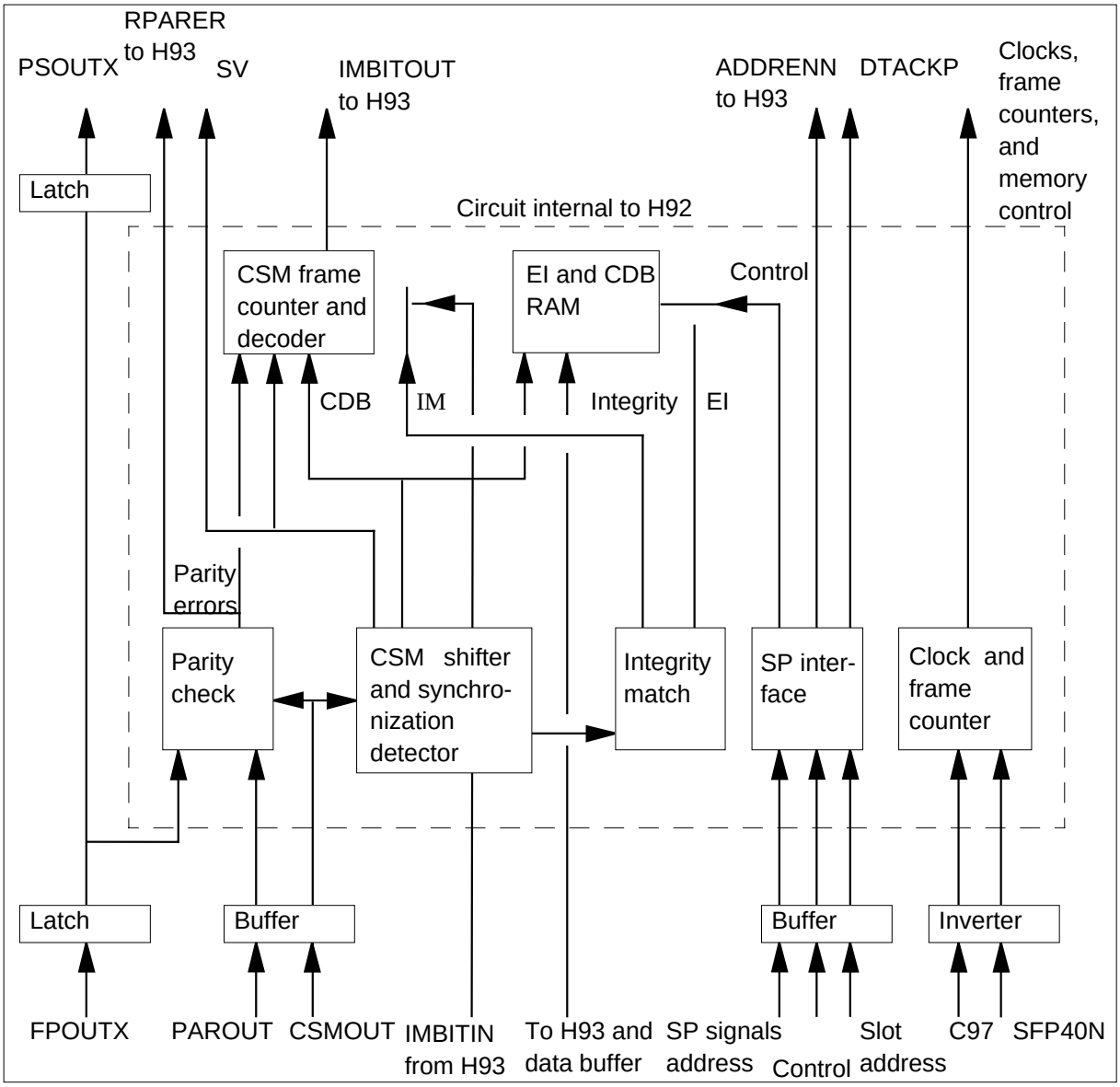
NT6X42CA operating blocks



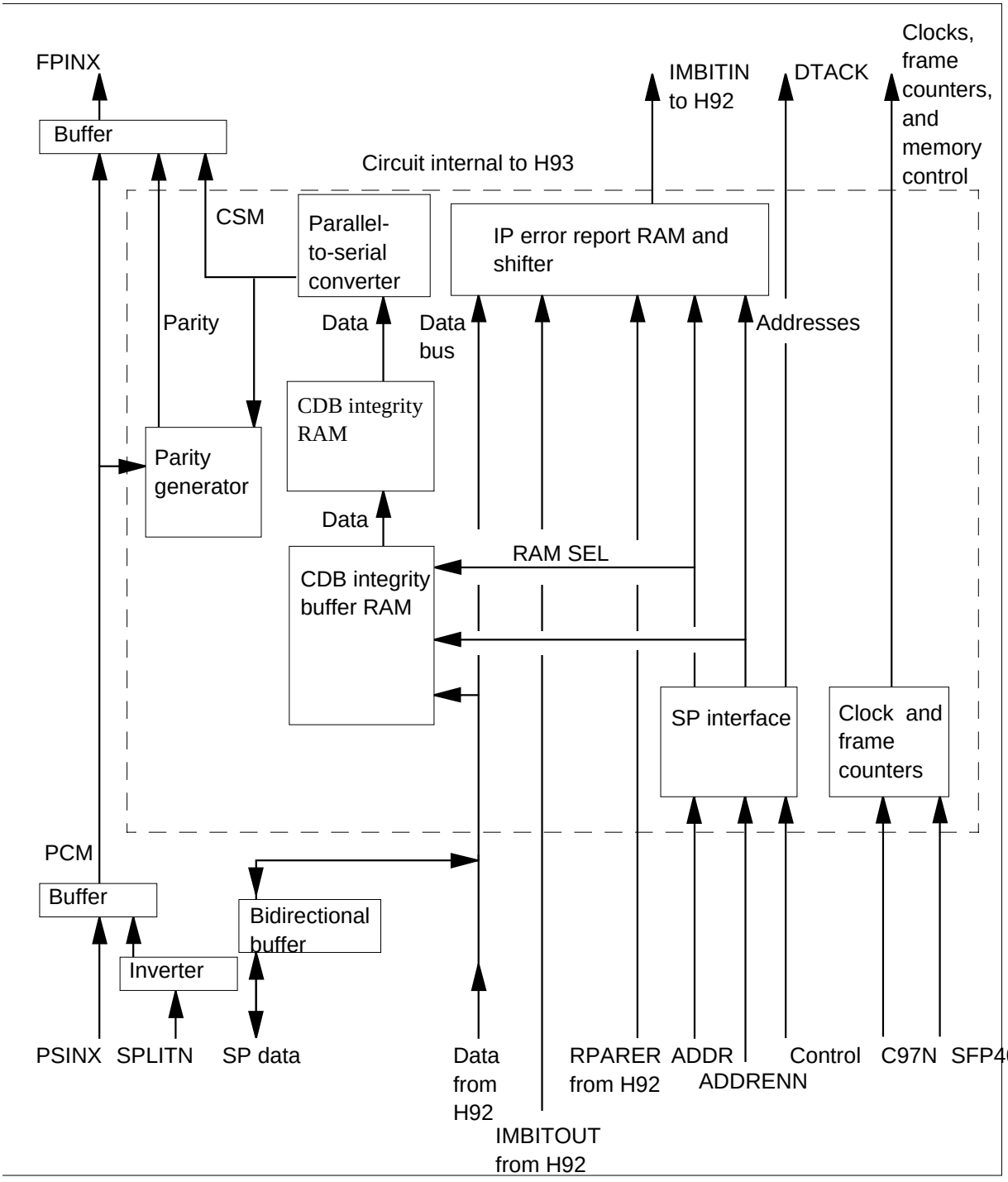
The receive and transmit circuits on the NT6X42CA appear in the following figure.

NT6X42CA (continued)

NT6X42CA receive circuits functional blocks



NT6X42CA transmit circuit functional blocks



NT6X42CA (continued)

Parity check

The parity check block receives PCM, CSM, and parity bits from the formatter. Odd parity is evaluated and compared to the received parity bit. An error sets flags in other chip circuits, and in the parity report RAM in H93. The retimed CSM is distributed to the rest of the chip.

CSM shifter and synchronization detector

Data flow through this block occurs in the following sequence:

1. The RAM stores the received CSM.
2. In the next slot, in the next frame, the old CSM bit reads out of the RAM
3. The old bit shifts to the next higher significant bit position.
4. The shifted old bit is written back back to the RAM, along with the current CSM bit for that channel.

In this method, the CSM message for each channel occupies one byte of the 512-byte RAM. The RAM can store only the last 16 received bits the message of the channel. The bits received earlier are lost.

The SYNC detector decodes the last 16 stored CSM bits and the present value of the CSM bit. The SYNC detector decodes these bits to detect a pattern of 16 ones (1) followed by a zero (0).

Integrity match

The integrity match block compares the integrity byte of a particular channel CSM message with the EI byte. If the bytes match, the integrity match (IM) bit is set, and the system sends the CDB byte to the processor. If the bytes do not match, a flag is set in the integrity match report RAM in the H93. The CDB is not updated.

Channel supervision message frame counter and decoder

The CSM frame counter and decoder RAM contains a byte for each channel. The 8 bits are composed of a 5-bit CSM frame count, a SYNC flag, a parity flag, and an SV bit flag. The 40th CSM frame can be reached and the SYNC and parity flags can be correct. In this event, the CDB stored in the shifter RAM is transferred to the EI RAM. This event occurs if the received accuracy matches the EI (IM = 1).

Expected integrity and channel data byte RAM

The processor card writes EI bytes into the top half of the RAM. The card reads the updated CDB bytes from the lower half of the RAM. The EI bytes are read out of the RAM. The bytes are sent to the shifter block where the bytes are

compared with the received integrity bytes. The comparison occurs 512 times for each frame.

Processor interface (receive)

The processor address and control signals and the card slot identification are decoded to produce access-enable signals. These signals are in the CDB read cycle and EI write cycle. The H93 uses ADDRENN to reduce pin count on the H93. The DTACK is asserted when the processor reads the CDB RAM.

Clock and frame counters (receive)

The receive clock and frame counters process the input 10-MHz clock signal and send the input to the frame counter. The frame counter provides additional processing to the signal. The signal that is worked again forms a pattern. In this pattern, the first 16 bits coincide with the valid channel data received from the formatter card. The first 16-bits are known as *active* time, and the last four-bits are called *dead* time.

Parity generator

As 8-bit XPCM data passes, the system inserts transmit CSM bit (bit 1) into the data. The parity generator inserts a parity bit (bit 0). The parity bit maintains odd parity on the ten bits.

Channel data byte integrity RAM

Two sets of RAMs store the transmit CDB and integrity bytes. The first set is the transmit CDB and integrity buffer RAM, and is accessible by the signaling processor (SP). The second set is called the *clone* of the buffer RAM. This set is named the clone because the contents of the first set are copied over to the second set during frames 22 and 23. During frames 24 to 39, the contents of the clone are shipped out as CSM bits. The SP is not permitted to access the clone. This limit eliminates the possibility of corrupting the outgoing CDB and accuracy bit streams.

Parallel-to-serial converter

The parallel-to-serial converter changes the 8-bit CDB and the SYNC pattern in to serial format. The parallel-to-serial converter makes these changes so that the data can be inserted 1 bit at a time as the CSM bit.

Integrity and parity error report RAM

The integrity and parity error report RAM stores the IMBITOUT and RPARER signals. These signals are the results of the integrity match and parity checking that is carried out in H92 and transmitted to H93. The SP can access all locations during active times except when the channel being accessed is currently being operated on. The system delays access for one channel time to avoid error.

NT6X42CA (continued)

Processor interface (transmit)

The signaling processor accesses the two RAMs of the H93 over the transmit processor interface. The SP accesses the H93 to update or read the transmit CDB and integrity bytes. The SP accesses the H93 to update or read the integrity match and parity error bits.

Clock and frame counters (transmit)

The transmit clock and frame counters generate several internal clocks from the input 10-MHz clock signal. These clocks are synchronized to the frame signal. Some of the clocks generate channel and frame counters. Some of the counter bits drive a combined circuit to produce control signals.

Technical data

Power requirements

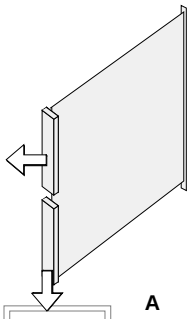
The NT6X42CA uses a voltage supply of 5 V (±0.25 V), and a current of 0.35 A.

Signaling

Pin numbers

The pin numbers for the NT6X42CA appear in the following figure.

NT6X42CA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	PWRP5	PWRP5
3A 3B	PWRP5	PWRP5
4A 4B	PWRP5	PWRP5
5A 5B	GND	GND
6A 6B		C97
7A 7B	GND	GND
8A 8B		
9A 9B	SFP40N	FPIN0
10A10B		FPIN1
11A11B		FPIN2
12A12B	DASN	FPIN3
13A13B		FPIN4
14A14B	DTACKN	FPIN5
15A15B	USDN	FPIN6
16A16B	WRTN	FPIN7
17A17B		CSMIN
18A18B		PARIN
19A19B		
20A20B		
21A21B	PSIN0	PSOUT0
22A22B	PSIN1	PSOUT1
23A23B	PSIN2	PSOUT2
24A24B	PSIN3	PSOUT3
25A25B	PSIN4	PSOUT4
26A26B	PSIN5	PSOUT5
27A27B	PSIN6	PSOUT6
28A28B	PSIN7	PSOUT7
29A29B	ADDR01	FPOUT0
30A30B	ADDR02	FPOUT1
31A31B	ADDR03	FPOUT2
32A32B	ADDR04	FPOUT3
33A33B	ADDR05	FPOUT4
34A34B	GND	FPOUT5
35A35B	ADDR06	FPOUT6
36A36B	ADDR07	FPOUT7
37A37B	ADDR08	CSMOUT
38A38B	ADDR09	PAROUT
39A39B		SV
40A40B	ADDR11	

	A	B
41A41B	GND	GND
42A42B	ADDR12	
43A43B	ADDR13	
44A44B	ADDR14	
45A45B		POSDC0
46A46B		POSDC1
47A47B	ADDR17	POSDC2
48A48B	ADDR18	
49A49B	ADDR19	
50A50B	ADDR20	
51A51B	ADDR21	
52A52B		
53A53B		
54A54B		FOUTEP
55A55B		GND
56A56B	POUTEP	GND
57A57B	GND	GND
58A58B		GND
59A59B		GND
60A60B		GND
61A61B		GND
62A62B		GND
63A63B		GND
64A64B	GND	GND
65A65B		GND
66A66B		
67A67B	DATA08	
68A68B	DATA09	
69A69B	DATA10	
70A70B	DATA11	SPLITN
71A71B	DATA12	
72A72B	DATA13	
73A73B	DATA14	
74A74B	DATA15	
75A75B		
76A76B	GND	GND
77A77B	GND	GND
78A78B		
79A79B		
80A80B	GND	GND

NT6X44AA

Product description

The NT6X44AA is a process that has more than one function control block (PCB). The NT6X44AA is part of the permanent set of cards in the line trunk controller (LTC) shelf.

Functional description

The NT6X44AA performs the following functions:

- time switching of incoming and outgoing pulse code modulation (PCM)
- hiway-select multiplexers (MUX) to allow the selection of PCM from a T1 or a DS30A interface for each port
- parallel-to-serial and serial-to-parallel formatting of PCM
- A/B bit transmit and receive interfaces for digital trunk applications with an optional extended format capability
- 3-ms interrupt to the signaling processor (SP)
- phase comparators for the office synchronization feature, formally provided by the digital carrier module type S (DCM-S)
- global peripheral side (P-side) looparound for diagnostic purposes

Time switching

The time switch allows the concentration of 20 P-side ports to 16 network ports in line concentrating modules (LCM). The time switch also spreads T1 channels over network ports in LTCs. A limited number of service circuits are shared among all ports and channels that use the time switching capability.

The circuit contains separate switching and connection memories for incoming and outgoing directions. The switching memories are written with PCM during the first half of each timeslot. During the second half, the PCM from a location indicated by the connection memory reads out, providing time switching that is not restricted. The connection memories are also time sliced, which allows the SP access during the first half of each timeslot. The processor is not held up during these accesses. The delay through each time switch is a variable of the switching RAM read access. This delay ranges from one-and-a-half timeslots to over a frame time.

Hiway-select multiplexers

The hiway-select MUXs appear as 16-bit lower and upper hiway-select registers to the SP. Each of these write-only registers has 10 bits. Each bit corresponds to a port. Ports 0 through 9 in the lower register, and ports 10 through 19 in the upper register. Writing a one (1) into a bit allows the

corresponding port to the T1 interfaces. A zero (0) selects the PCM from the DS30A port.

Parallel-to-serial and serial-to-parallel formatting

On the parallel side, 640 timeslots appear of 195-ns duration each. On the serial side, ten-outputs are provided. Each output consists of two serial ports that are bit multiplexed together. Serial data is presented to the DS30A and T1 interface cards. Data with the same multiplexing format is returned from those cards in the incoming direction.

A/B bit signaling interfaces

The outgoing A/B bit interface contains a 12-bit memory location for each of the 640 timeslots. Signaling is enabled and extended, or normal T1 formats are selected for each channel and for each port. Direct hardware mapping of the supervision bit on A and B bits in the outgoing direction can be selected.

The incoming A/B circuit formats the received signaling bits into a 256-byte memory. A 64-byte buffer for the A, B, C, and D signaling bits is present. When extended format is not used, the C and D buffers are updated. These buffers are updated with received A and B bits each second superframe (12 frame) cycle.

For diagnostic purposes, the A/B bit update is disabled and the system performs a memory test on the A/B receive memory. You can disable the update by writing a 1 to bit 14 of the low hiway MUX. The A/B bit update is resumed by rewriting bit 14 to 0.

3-ms interrupt

The NT6X44AA system provides A 3-ms interrupt to the SP for A-to-B scanning synchronization. The interrupt occurs after the A and B tables are updated in the receive memory, before the C and D maps are updated. The interrupt is latched and can be disabled in the hardware. The interrupt is disabled by writing a 1 to bit 13 of the low hiway MUX, and re-enabled by writing a 0 to the same bit.

Phase comparators for office synchronization

The phase comparators in the NT6X42CA operate like the phase comparator in the DCM-S. The selection MUX for the source T1 is eliminated. TheNT6X42CA provides a single 16-bit word withs phase comparator readings from two T1s. The shelf wiring selects the two T1s.

Global P-side looparound

The global looparound loops all 640 outgoing timeslots back to the incoming direction. You can activate the global looparound by setting the most

NT6X44AA (end)

significant bit (bit 15) of the lower hiway MUX register to 1. The system disables the global looparound by the activity signal. The A and B bits are in the global looparound. These bits arrive at the incoming time switch one timeslot later than the PCM for a given outgoing timeslot because of timing restrictions.

NT6X44AB

Product description

The NT6X44AB is based on the NT6X44AA. The NT6X44AB is a multifunction printed circuit card. The NT6X44AB is part of the permanent set of cards in the line trunk controller (LTC) shelf.

Functional description

The NT6X44AB performs the following functions:

- time switching of incoming and outgoing pulse code modulation (PCM)
- selection of PCM from a T1 or a DS30A interface for each port, with hiway-select multiplexers (MUX)
- parallel-to-serial and serial-to-parallel formatting of PCM
- A/B bit transmit and receive interfaces for digital trunk applications with an optional extended format capability
- 3-ms interrupt to the signaling processor (SP)
- phase comparators for the office synchronization feature that the digital carrier module type S (DCM-S) provided
- global peripheral side (P-side) looparound for diagnostic purposes

Time switching

The time switch allows the concentration of 20 peripheral side (P-side) ports to 16 network ports in line concentrating modules (LCM). The time switch spreads T1 channels over network ports in LTCs. The time switching capability allows all ports and channels to share a limited number of service circuits.

The circuit contains separate switching and connection memories for incoming and outgoing directions. The switching memories are written with PCM during the first half of each time slot. During the second half, the PCM is read out. The PCM is read out from a specified location. The connection memory specifies this location. This event provides time switching that is not restricted. The connection memories are time sliced. The time slice allows the SP access during the first half of each time slot. The processor is not held up during these accesses. The delay, through each time switch, is a variable of the switching RAM read access. The read access is connection memory data. The variable ranges from one-and-a-half time slots to just over a frame time.

Hiway-select multiplexers

The hiway-select MUXs appear as 16-bit lower and upper hiway-select registers to the SP. Each of these write-only registers has 10 bits that correspond to a port. The registers correspond to ports 0 through 9 in the lower

register, and ports 10 through 19 in the upper register. A one (1) written to a bit enables the associated port to the T1 interfaces. A zero (0) selects the PCM from the DS30A port.

Parallel-to-serial and serial-to-parallel formatting

On the parallel side, each of the 640 time slots appears for a 195-ns duration. The serial side has ten outputs. Each output contains two serial ports that are bit multiplexed together. The DS30A and T1 interface cards receive serial data. The cards return the same multiplexing format in the incoming direction.

A/B bit signaling interfaces

The outgoing A/B bit interface contains a 12-bit memory location for each of the 640 time slots. Signaling is enabled and extended, or normal T1 formats are selected for each channel and port. Direct hardware mapping of the supervision bit on A and B bits in the outgoing direction can be selected.

The incoming A/B circuit formats the received signaling bits to a 256-byte memory. A 64-byte buffer is present for the A, B, C, and D signaling bits. When the extended format is not in use, the C and D buffers are updated. The C and D buffers receive A and B bits every second superframe cycle. A superframe cycle contains 12 frames.

For diagnostic purposes, the system disables A/B bit update. The system performs a memory test on the A/B receive memory. The system writes a 1 to bit 14 of the low hiway MUX to disable the update. The system rewrites bit 14 to 0 to resume the A/B bit update.

3-ms interrupt

The NT6X44AB provides a 3-ms interrupt to the SP for A-to-B scanning synchronization. The interrupt occurs after the system updates the A and B tables in the receive memory. The interrupt occurs before the system updates the C and D maps. The interrupt is latched. The system can disable the interrupt in the hardware. The system writes a 1 to bit 13 of the low hiway MUX to disable the interrupt. The system writes a 0 to the same bit to enable the interrupt.

Phase comparators for office synchronization

The phase comparators in the NT6X44AB operate like the phase comparator in the DCM-S. The selection MUX for the source T1 in the phase comparators of the NT6X44AB is not available. The NT6X44AB provides a single 16-bit word with phase comparator readings from the two T1s. The shelf wiring selects the two T1s.

NT6X44BA

Product description

The NT6X44BA provides pulse code modulation (PCM) conversions for each channel. The PCM conversions provide compatibility between the North American and international DMS-100 switches. This version of the card allows A-law-to-μ-law, and μ-law-to-A-law conversions.

Location

The time switch card is a printed circuit card with more than one function. This card is part of the permanent set of cards in the line trunk controller (LTC) shelf.

Functional description

Functional blocks

The NT6X44BA contains the following operating blocks:

- time switch
- hiway select multiplexer (MUX)
- parallel-to-serial (P/S) and serial-to-parallel (S/P) formatting
- A/B bit signaling interface
- A-law/μ λαω χονϖερσιον
- phase comparators
- 3-ms interrupt
- global looparound

Time switch

The NT6X44BA allows the concentration of 20 peripheral-side (P-side) ports to 16 network ports. In the trunks, the time switch spreads the T1 channels over network ports. The time switch capability allows all ports and channels to share a limited number of service circuits. These service circuits include the tone generator and common channel interoffice signaling (CCIS) continuity checker.

The circuit contains separate switching and connection memories for the outgoing and incoming directions. The switching memories are written with the PCM during the first half of each of the 640 timeslots. During the second half, the system reads the PCM out. The connection memory indicates the location from which the system reads the PCM out. This event provides time switches that are not restricted. The connection memories are time sliced. This event allows the signaling processor (SP) access during the first half of each timeslot. The processor is not held up during these accesses.

NT6X44BA (continued)

The delay through each time switch is a variable of the switching RAM read address. The switching RAM read address is the connection memory data. The value of the variable ranges from one-and-a-half timeslots (292 ns) to just over one frame time (125µs + 97 ns).

Hiway-select multiplexer

The hiway-select MUX contains two 16-bit write-only registers. These registers are the upper and lower hiway MUX registers. Writing a one (1) to a bit enables the associated port to the T1 interfaces. A zero (0) selects the PCM from the DS30A port. Ten bits in these registers also correspond to a port–ports 0 to 9 in the lower register. Ten bits in these registers correspond to a specified port. These bits correspond to ports 10 to 19 in the upper register. The least important 10 bits of each register form a bit map of the P-side ports. A 1 bit corresponds to a PCM30 or DS1 port. A 0 bit corresponds to a DS30A port.

Parallel-to-serial and serial-to-parallel formatting

Two W72 PCM formatter integrated circuits implement the P/S and S/P formatting function. On the parallel side, 640 timeslots of 195-ns duration appear in the format described under the definition of timeslot. Ten outputs are on the serial side. Each output contains two serial ports that are bit-multiplexed together. The function presents the serial data in this form to the DS30A and T1 interface cards. The interface cards return the data with the same multiplexing format in the incoming direction.

A/B bit signaling interface

The outgoing A/B bit signaling interface inserts signaling information in the P-side timeslots. The interface contains a 12-bit memory location for each of the 640 timeslots. Signaling can be enabled for each timeslot. The system can choose normal or extended PCM30 or DS1 formats. The system can select mapping of the SV bit to A and B bits.

The incoming A/B circuit formats the received signaling bits to a 256-byte memory. A 64-byte buffer is present for the A, B, C, and D signaling bits. When extended format is not in use, the A and B bits update the C and D buffers. The C and D buffers receive A and B bits every second superframe cycle. Each superframe cycle contains 12 frames.

A-law/µ-law conversion

The system compands voice data to aµ-law or an A-law standard to improve the voice data signal-to-noise ratio. The NT6X44BA must convert data before a transfer from a µ -law switch to an A-law switch can occur. All ports that enter the switch do not have data companded in the same way. A-law-to µ-law conversion and µ-law-to-A-law conversion is programmable for each port. When the line group controller (LGC) is initialized, the incoming and outgoing

connection memories are loaded with control bits. These control bits are for A-law-to-µ-law data conversion for each timeslot. If the switch uses A-law companion, TOA = 1. If the switch uses µ-law companion, TOA = 0. If the P-side port uses A-law, ISA = 1. If the P-side port uses µ-law, ISA = 0. The P-side TSA represents the P-side port.

Note: The memory fills only once. All following writes to the incoming connection memory must not overwrite the memory.

Phase comparators

The phase comparators in the NT6X44BA operate like the comparators in the DCM/S. The phase comparators of the NT6X44BA do not have the selection MUX for the source T1. A single 16-bit word contains the comparator readings from two T1s. The shelf wiring selects the monitored T1s.

3-ms interrupt

The SP has a 3-ms interrupt for signaling bit scanning synchronization. The interrupt occurs after the system updates the A and B tables. The interrupt occurs before the system updates the C and D tables. The interrupt is latched. The SP must clear the interrupt. To clear the interrupt, the SP accesses location $107000. To disable the interrupt, the system writes a 1 to bit 13 of the lower hiway MUX. To enable the interrupt, the system writes a 0.

Global looparound

The global looparound circuit loops all 640 timeslots from the outgoing direction back to the incoming direction. The most significant bit (bit 15) of the lower hiway MUX register is set to 1 to enable the looparound. The system writes a 1 to disable the looparound. Activity qualifies the enable bit. Only the active unit can use global looparound when this event occurs.

Note 1: Compensation must occur for the misalignment of outgoing and incoming channels when the looparound is in use.

Note 2: The A/B bits are in the global looparound. Timing limits cause bits to arrive in the receive memory one timeslot later than expected for a specified outgoing timeslot. The bits appear correctly in the data.

Note 3: The system must enter the A-law/µ-law bits again in the incoming connection memory. The data changes according to CCITT recommendations, volume III, G711 if TOA is not set to ISA.

Technical data

Power requirements

The NT6X44BA requires a voltage of +5V. The NT6X44BA requires a current of 3A.

NT6X44BA (end)

Global P-side looparound

The global looparound circuit loops all 640 outgoing time slots back to the incoming direction. Bit 15 of the lower hiway register must be set to 1 to enable the looparound. The activity signal disables the looparound. The A and B bits are in the global looparound. The timing limits cause these bits to arrive in the incoming time switch one time slot later than the PCM. These bits arrive in the incoming time switch for a specified outgoing time slot.

NT6X44DA

Product description

The NT6X44DA is a multifunction printed circuit card for the United Kingdom SL-100 application. The card is based on the NT6X44BA. The NT6X44DA has a change from A-law and &0xb5;-law conversion firmware to even-bit inversion (EBI) compensation firmware. This version of the time switch compensates for EBI. The NT6X27AA PCM30 interface applies EBI to the data packet network switching system (DPNSS) signaling channel. The NT6X27AA PCM30 inteface is in the international digital trunk controllers (IDTC) of A-law DMS switches.

This card is for the message switch and buffer 7 (MSB7) DPNSS extended multiprocessor system (XMS)-based peripheral module (XPM). This card compensates for EBI data. The compensation for EBI data creates a clear digital channel for the internal digital sources, the DPNSS signaling terminals. The time switch DPNSS card can be applied to other XPMs, like the IDTC. This event allows the EBI to be disabled for internally generated data that normally switches through the IDTC to the digital trunks.

This document describes all of the features available from the NT6X44DA . Application of the card in the MSB7 DPNSS shelf uses all available features. Available features include the A/B bit signaling interface.

Location

The time switch DPNSS card was developed for the permanent set of cards in the MSB7 common circuit pack DPNSS shelf. The time switch card is part of the permanent set of cards in the line trunk controller (LTC) shelf.

Functional description

The NT6X44DA performs the following functions:

- time switching of incoming and outgoing pulse code modulation (PCM)
- selection of PCM from a PCM30 or a DS30A interface for each port with hiway select multiplexers (MUX)
- parallel-to-serial and serial-to-parallel formatting of PCM
- A/B bit transmit and receive interfaces for digital trunk applications with an optional extended format capability
- compensation and no compensation for EBI, programmable for each port
- 3-ms interrupt to the signaling processor (SP) for A and B bit scan
- phase comparators for the office synchronization feature. The digital carrier module type S (DCM-S) previously provided this feature.
- global peripheral side (P-side) looparound for diagnostic purposes

NT6X44DA (continued)

Time switching

The time switch allows the concentration of 20 P-side ports to 16 network ports. The time switching capability allows all ports and channels to share a limited number of service circuits. The tone generator and common office interoffice signaling are examples of a service circuit. For application of the in international digital trunks, the time switch spreads the PCM30 channels over network ports.

The circuit contains separate switching and connection memories for incoming and outgoing directions. The switching memories are written with PCM during the first half of each timeslot. During the second half, the PCM is read out from a specified location. The connection memory specifies this location. This event provides time switches that are not restricted. The connection memories are time sliced. This event allows the SP access during the first half of each timeslot. The processor is not held up during these accesses. The delay through each time switch is a variable of the switching RAM read access, connection memory data. The value of the variable ranges from one and a half timeslots to just over a frame time.

Hiway-select multiplexers

The hiway-select MUXs appear to the SP as 16-bit lower and upper hiway-select registers. Each write-only register has 10 bits. Each bit corresponds to a port. Ports 0 through 9 are in the lower register. Ports 10 through 19 are in the upper register. To enable the associated port to the T1 interfaces, the system writes a one (1) to a bit. To select the PCM from the DS30A port, the system writes a zero (0). All ports correspond to the DS30A interface for the MSB7 DPNSS application.

Parallel-to-serial and serial-to-parallel formatting

On the parallel side, each of the 640 timeslots appear of 195-ns duration. On the serial side, ten outputs are available. Each output contains two serial ports that are bit multiplexed together. The DS30A and PCM30 interface cards receive serial data for IDTC applications. The interface cards return the serial data with the same multiplexing format from the cards in the incoming direction. The DS30A interface cards receive serial data for the MSB7 DPNSS application.

A/B bit signaling interfaces

The outgoing A/B bit interface contains a 12-bit memory location for each of the 640 timeslots. The system enables and extends signaling. The system choses normal PCM30 formats for each channel and port. The system can select direct hardware mapping of the supervision bit on A and B bits in the outgoing direction.

The incoming A/B circuit formats the received signaling bits to a 256-byte memory. A 64-byte buffer is present for the A, B, C, and D signaling bits. When extended format is not in use, the received A and B bits update the C and D buffers every second superframe (12 frame) cycle.

The card disables the A/B bit update and performs a memory test on the A/B receive memory for diagnostic purposes. To disable the update, the system writes a 1 to bit 14 of the low hiway. To resume the A/B bit update, the system writes bit 14 to 0.

Compensation for even-bit inversion

The MSB7 DPNSS XPM must compensate for the EBI that the IDTC applies to the data stream. The DPNSS application, or any application that involves generated data in DMS, uses this compensation. The time switch DPNSS card applies EBI to the even-bit inverted data stream. This action creates a clear digital stream. Some ports that come to the switch do not require compensation of data for EBI. EBI <-> CLEAR STREAM CONVERSION is programmable for each port. The application determines the type of data the switch uses. Examples of data is even-bit inverted data in A-law switches and data of the P-side ports for any compensation.

At initialization of the MSB7 DPNSS shelf, incoming and out-connection memories are loaded with the control bits for EBI to CLEAR DATA STREAM CONVERSION for each timeslot. The MSB7 DPNSS XPM, or any other XPM in the international application, is in an A-law switch and TOA = 1. The P-side timeslot (TSA) port represents the P-side port. If the P-side port does not require conversion to a clear data stream, ISA = 1. If conversion is required, ISA = 0. The connection memory is filled once. All write operations to incoming connection memory must not overwrite the connection memory.

3-ms interrupt

The NT6X44DA provides a 3-ms interrupt to the SP for A-to-B scanning synchronization. The interrupt occurs after the update of the A and B tables in the receive memory. The interrupt occurs before the update of the C and D maps. The interrupt is latched. The card can disable the interrupt in the hardware. To disable the interrupt, the card writes a 1 to bit 13 on the low hiway MUX. To enable the interrupt, the card writes a 0 to the same bit.

Phase comparators for office synchronization

The phase comparators operate like the phase comparators in the DCM-S. The selection MUX for the source PCM30 is not present for phase comparators of the NT6X44DA. A single 16-bit word that contains phase comparator readings from two PCMs is available. Shelf wiring selects the two PCMs.

NT6X44DA (end)

Global P-side looparound

The global looparound circuit loops all 640 outgoing timeslots back to the incoming direction. A setting of 1 for bit 15 of the lower hiway MUX register enables the looparound. The activity signal disables the looparound. Only the inactive module can use the looparound.

Note 1: When the looparound is in use, a bad alignment of incoming and outgoing channels occurs. Compensation must occur in the incoming connection memory data.

Note 2: The A and B bits are in the global looparound. Timing limits cause the bits to arrive to the receive memory one timeslot later than the bits that arrive for a specified outgoing timeslot. The A and B bits appear correctly in the data. The receive memory can require the A and B bits. When this event occurs, the incoming connection memory must be changed, or the A/B bits in the A/B connection memory must be set up.

Note 3: The EBI bits must be entered in the incoming connection memory only.

NT6X44EA

Product description

The NT6X44EA provides pulse code modulation (PCM) conversions on each channel. The PCM conversions allow compatibility between the North American and international DMS-100 switches. The universal time switch can perform nine different types of PCM conversions. The switch performs the conversions from central side (C-side) to peripheral side (P-side). The switch also performs the conversions from the P-side to the C-side.

The NT6X44EA can directly replace current versions of the NT6X44 time switch with the following exceptions:

- NT6X44AC
- NT6X44CA

Functional description

Functional blocks

The NT6X44EA contains the following functional blocks:

- time switch
- hiway-select multiplexer (MUX)
- A/B bit signaling interface
- phase comparators
- 3-ms interrupt
- global looparound
- PCM conversions

Time switch

The NT6X44EA contains two separate time switches. One switch is for incoming data, the other switch is for outgoing data. The two time switches operate by the same method.

The outgoing time switch maps PCM samples from the C-side time-slot addresses (TSA) to the P-side TSAs. To create a connection, 10 bits must be written in the time switch connection memory. The outgoing connection memory contains one memory location for every P-side TSA. The data in each location corresponds to the C-side TSA . The C-side TSA connects to that channel. More than one P-side channel can map to the same C-side channel, which allows for broadcasting to the peripherals. This ability can send tones (dial tone, ringing tone, and others tones) to the peripheral.

NT6X44EA (continued)

The incoming time switch operates through a similar method except that the address corresponds to the C-side TSA. The data is also the P-side TSA.

Hiway-select multiplexer

The hiway-select MUX selects if the system routes data to the PCM30 or DS1 interface card or DS30A cards for each port. The MUX consists of two 16-bit write-only registers: the upper and lower hiway MUX registers. The least important 10 bits of each register form a bit map of the P-side ports. A one (1) bit corresponds to a PCM30 or DS1 port and a zero (0) bit corresponds to a DS30A port.

A/B bit signaling interface

The outgoing A/B bit signaling interface inserts signaling information in a P-side time slots. Signaling can be enabled for each time slot. Choose normal or extended PCM30 or DS1 formats. Select the mapping of the SV bit to A and B bits.

Phase comparators

The phase comparators operate through the same method as the comparators in the DCM/S, but the selection MUX is eliminated. A single word contains the comparator readings from two PCM30s or DS1s. The wiring string selects the monitored PCM30s or DS1s.

3-ms interrupt

The signaling processor (SP) has a 3-ms interrupt for signaling bit scanning synchronization. The interrupt occurs after updates of the A and B tables occur, and just before updates of the C and D tables. The interrupt is latched. The SP must clear the interrupt. The SP accesses location 107000 to clear the interrupt. Write a 1 to bit 13 to disable the interrupt. Enable the lower hiway MUX and write a 0.

Global looparound

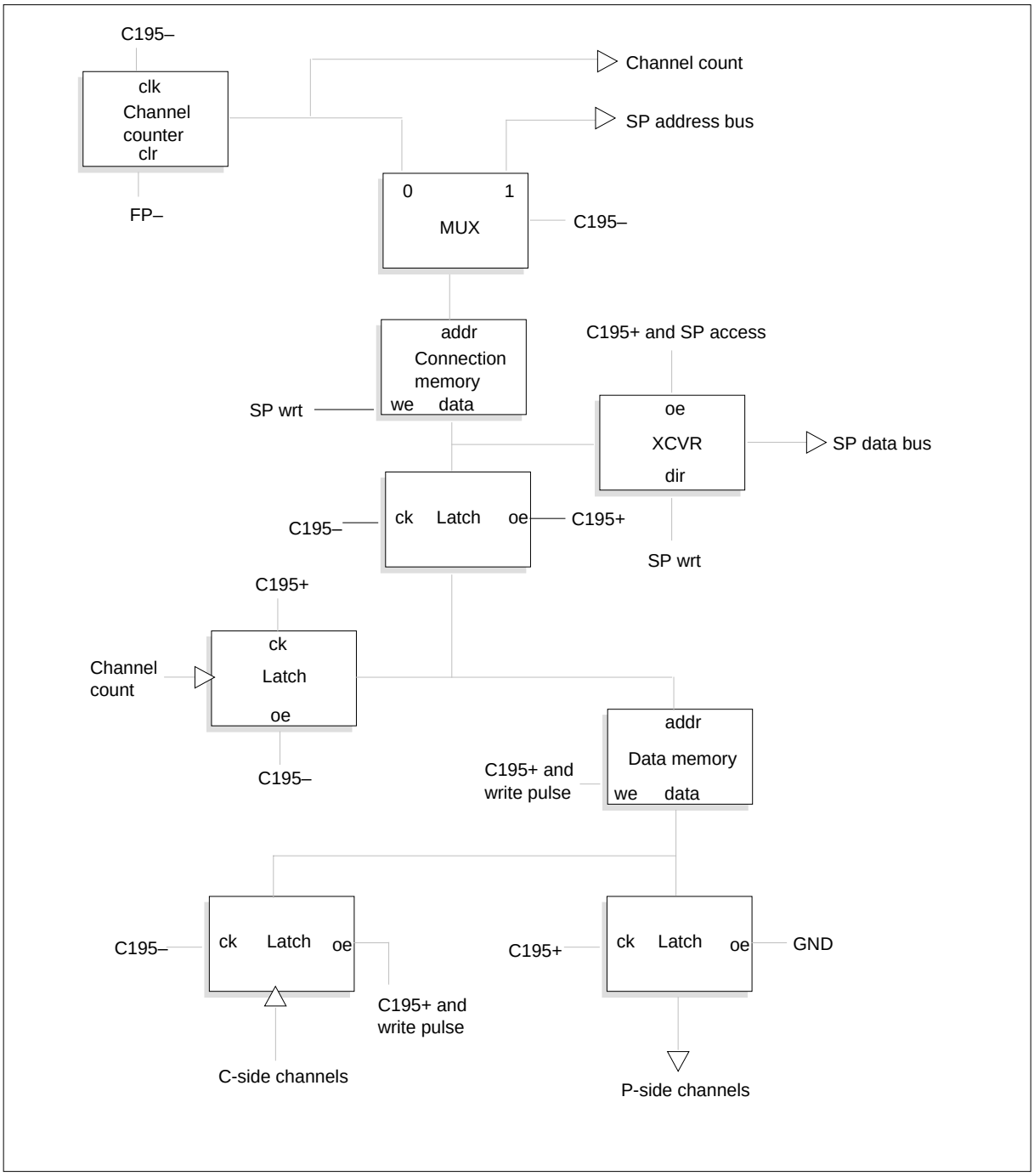
The global looparound circuit loops the 640 time slots from the outgoing direction back to the incoming. Set bit 15 of the lower-hiway MUX to 1 to enable the looparound. Write a 0 to disable the looparound. The enable bit is qualified with activity so that global looparound can be used in the inactive unit.

PCM conversions

Some ports that come to the switch require a type of PCM conversion for data or voice. The PCM conversions are progammable for each channel.

The relationship between the functional blocks appears in the following figure.

NT6X44EA functional blocks



NT6X44EA (continued)

Technical data

Power requirements

The voltage required is +5V. The current required is 3A.

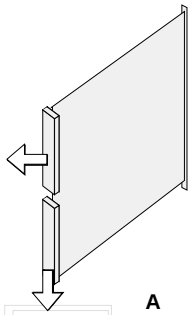
Signaling

Pin numbers

The pin numbers for the NT6X44EA appear in the following figure.

NT6X44EA pin numbers

	A	B
1A 1B	GND	GND
2A 2B	+5V	+5V
3A 3B	+5V	+5V
4A 4B	+5V	+5V
5A 5B	GND	GND
6A 6B	FP–	C97+
7A 7B	GND	GND
8A 8B	ACT–	
9A 9B		
10A 10B	FP48–	SBIT
11A 11B	GND	GND
12A 12B	DAS–	TWR
13A 13B	LDS–	TST1
14A 14B	DTACK–	TST0–
15A 15B	UDS–	ABOUT
16A 16B	WRT–	ABIN
17A 17B		3MSIRQ–
18A 18B		GND
19A 19B		
20A 20B		MB
21A 21B	PIN0	POUT0
22A 22B	PIN1	POUT1
23A 23B	PIN2	POUT2
24A 24B	PIN3	POUT3
25A 25B	PIN4	POUT4
26A 26B	PIN5	POUT5
27A 27B	PIN6	POUT6
28A 28B	PIN7	POUT7
29A 29B	ADDR01	C0
30A 30B	ADDR02	C2
31A 31B	ADDR03	C4
32A 32B	ADDR04	C6
33A 33B	ADDR05	C8
34A 34B	GND	GND
35A 35B	ADDR06	C10
36A 36B	ADDR07	C12
37A 37B	ADDR08	C14
38A 38B	ADDR09	C16
39A 39B	ADDR10	SV
40A 40B		C18



	A	B
41A 41B	GND	DSOUT0
42A 42B	ADDR12	DSOUT2
43A 43B	ADDR13	DSOUT4
44A 44B	ADDR14	DSOUT6
45A 45B	ADDR15	DSOUT8
46A 46B		DSOUT10
47A 47B	ADDR17	DSOUT12
48A 48B	ADDR18	DSOUT14
49A 49B	ADDR19	DSOUT16
50A 50B	ADDR20	DSOUT18
51A 51B	ADDR21	GND
52A 52B		T1IN0
53A 53B		T1IN2
54A 54B		T1IN4
55A 55B	PSPEN	T1IN6
56A 56B		T1IN8
57A 57B	GND	T1IN10
58A 58B	DATA00	T1IN12
59A 59B	DATA01	T1IN14
60A 60B	DATA02	T1IN16
61A 61B	DATA03	T1IN18
62A 62B	DATA04	GND
63A 63B	DATA05	DSIN0
64A 64B	GND	DSIN2
65A 65B	DATA06	DSIN4
66A 66B	DATA07	DSIN6
67A 67B	DATA08	DSIN8
68A 68B	DATA09	DSIN10
69A 69B	DATA10	DSIN12
70A 70B	DATA11	DSIN14
71A 71B	DATA12	DSIN16
72A 72B	DATA13	DSIN18
73A 73B	DATA14	GND
74A 74B	DATA15	RECFP0
75A 75B		RECFP1
76A 76B	GND	GND
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

NT6X45BA

Product description

The NT6X45BA card is a 68000-based processor for use in every extended multiprocessor system (XMS)-based peripheral module (XPM) of the DMS-100. The applications that require the NT6X45CA are exceptions. The external bus structure conforms to the XMS address bus (A-bus) interface specification.

Compatibility

The NT6X45BA processor is functionally equivalent to the other NT6X45 processors. The NT6X45BA processor is specified for each application. The difference between the AB, AC, AD, AE, and AF versions is the onboard firmware. The firmware in the provides for fault isolation and office recovery. These processes must use the inter-module communication (IMC) link between shelves. The NT6X45BA can be used in an XPM (BCS19 and greater) that uses new messaging. The NT6X45BA is not compatible with the other versions of the NT6X45 family. Use of a NT6X45BA and other versions of NT6X45 processor at the same time, in the same XPM, can cause problems. Use of a NT6X45BA in this way can result in the wrong operation of one or two of the shelves.

The NT6X45 is available in the following versions:

- XPM processor circuit card–standard
- XPM processor circuit card–standard NT6X45AC
- XPM processor circuit card–international NT6X45AD
- XPM processor circuit card–RCC NT6X45AE
- XPM processor circuit card–FSA NT6X45AF
- XPM processor circuit card–FJOR

Functional description

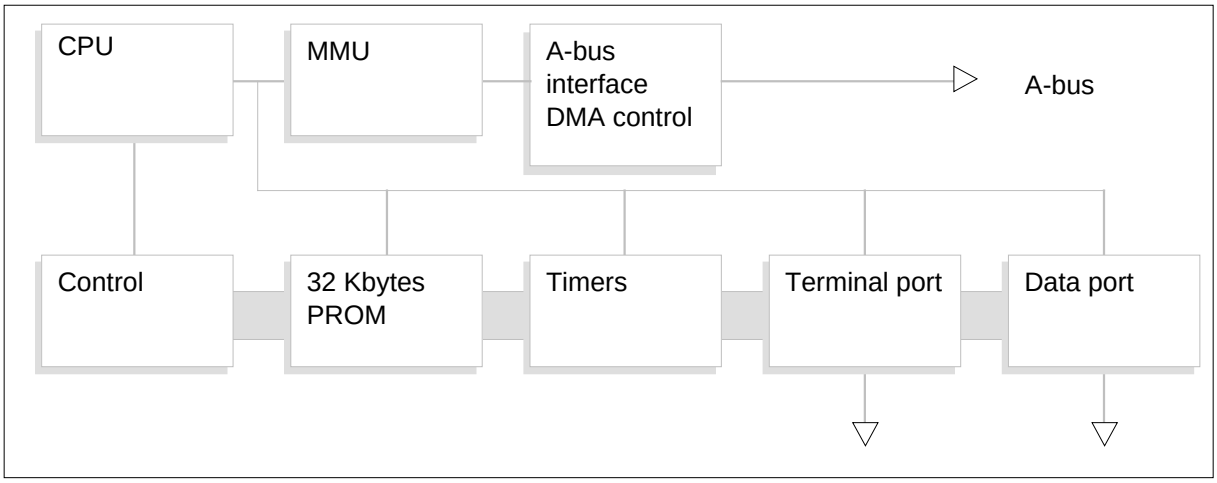
Functional blocks

The NT6X45BA contains the following operating blocks:

- CPU
- memory management unit
- sanity and clock control
- A-bus interface
- onboard I/O facilities

The relationship between these blocks appears in the following figure.

NT6X45BA functional blocks



Central processing unit

The CPU supports 16 linear 16-Mbyte virtual address spaces. A Motorola 68000 microprocessor that runs at 8 MHz is used for the CPU.

Data bus

The data bus uses data paths to memory that are 16 bits wide.

Memory management unit

The memory management unit converts the virtual addresses, that an executing program generates, to addresses used to access real memory.

Sanity and clock control

The sanity timer protects the computing node against software failure. The total software failure can mask each interrupt level and prevent external communication.

Address-bus interface

Memory and I/O controllers communicate with the processor board over the A-bus. Enough drive capability allows a maximum of 16 LS Schottky connections to the A-bus.

On-board I/O facilities

The CPU has access to the following I/O facilities:

- PROM
- programmable timers
- terminal controller

NT6X45BA (continued)

- dataport controller
- baud rate selection

Two EPROM chips are the resident bootstrap loader and low-level monitor.

An Intel 8253 provides three timers, each under software control. Timer 1 provides the clock tick to schedule tasks. Timers 2 and 3 that connect to form the 32-bit sanity timer (STR) register.

An Intel 8251A universal synchronous/asynchronous receiver/transmitter (USART) accesses the terminal.

An Intel 8251A USART communicates with the dataport port.

A Motorola K1135B baud rate generator provides terminal and dataport clocks.

Signaling

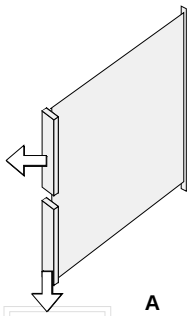
Pin numbers

The pin numbers for NT6X45BA appear in the following figure.

NT6X45BA (continued)

NT6X45BA pin numbers

		A	B
1A	1B	Gnd	Gnd
2A	2B	PWR+5	PWR+5
3A	3B	PWR+5	PWR+%
4A	4B	PWR+5	PWR+5
5A	5B	Gnd	Gnd
6A	6B	BUSReq–	
7A	7B	BUSGRI–	
8A	8B	BUSGRO–	
9A	9B	BUSBSY–	
10A	10B	4XCLK–	OSCOUT–
11A	11B	Gnd	MMUTSTO–
12A	12B	DAS–	AS+
13A	13B	LDS–	2XCLK+
14A	14B	DTACK–	2XCLKSYN+
15A	15B	UDS–	1XCLKSYN+
16A	16B	WRT–	SANDIS–
17A	17B	1XCLK+	1XCLK–
18A	18B	RSTOUT–	RSTIN–
19A	19B	PERINTO–	HWRST–
20A	20B	PERINT1–	IRQ4
21A	21B	PERINT2–	
22A	22B	Gnd	
23A	23B	PERINT3–	
24A	24B	PERINT4–	
25A	25B	PERINT5–	
26A	26B	PERINT6–	
27A	27B	PERINT7–	Gnd
28A	28B	MEMIRQ–	LOOPI–
29A	29B	ADDRO1+	LOOPO–
30A	30B	ADDRO2+	HPU12+
31A	31B	ADDRO3+	HDICLK+
32A	32B	ADDRO4+	HDOCLK+
33A	33B	ADDRO5+	HACKOUT+
34A	34B	Gnd	HDOUT+
35A	35B	ADDRO6+	HDIN+
36A	36B	ADDRO7+	TPU12+
37A	37B	ADDRO8+	TACKIN+
38A	38B	ADDRO9+	TDOUT+
39A	39B	ADDR10+	TDIN+
40A	40B	ADDR11+	Gnd



		A	B
41A	41B	Gnd	BUSTIMO–
42A	42B	ADDR12+	F0BXXX–
43A	43B	ADDR13+	F0CXXX–
44A	44B	ADDR14+	
45A	45B	ADDR15+	
46A	46B	ADDR16+	
47A	47B	ADDR17+	Gnd
48A	48B	ADDR18+	
49A	49B	ADDR19+	
50A	50B	ADDR20+	
51A	51B	ADDR21+	
52A	52B	(ADDR22+)	
53A	53B	Gnd	
54A	54B	(ADDR23+)	
55A	55B	FC0–	
56A	56B	FC1–	
57A	57B	FC2–	
58A	58B	DATA00+	
59A	59B	DATA01+	Gnd
60A	60B	DATA02+	
61A	61B	DATA03+	
62A	62B	DATA04+	
63A	63B	DATA05+	
64A	64B	Gnd	
65A	65B	DATA06+	
66A	66B	DATA07+	
67A	67B	DATA08+	
68A	68B	DATA09+	
69A	69B	DATA10+	
70A	70B	DATA11+	Gnd
71A	71B	DATA12+	
72A	72B	DATA13+	BP1+
73A	73B	DATA14+	BP2+
74A	74B	DATA15+	BP3+
75A	75B		BP4+
76A	76B	Gnd	Gnd
77A	77B	PWR+12	PWR–12
78A	78B	Gnd	Gnd
79A	79B	PWR+12	PWR–12
80A	80B	Gnd	Gnd

NT6X45BA (end)

Technical data

Physical characteristics

The dimensions for the NT6X45 circuit card are:

- height: 19.05 mm (00.75 in)
- depth: 317.50 mm (12.50 in)
- width: 254.00 mm (10.00 in)

Power requirements

The power requirements for the NT6X45 circuit card are:

- voltage: +5V, +12V, -12Vdc
- current: 1.5A
- 48-V power use: 7.5W

NT6X45BC

Product description

The NT6X45BC is a Motorola 68000-based processor card used in every extended multiprocessor system (XMS)-based peripheral module (XPM) of the DMS-100. Applications that require the NT6X45BC are exceptions. The external bus structure conforms with the XMS address bus (A-bus) interface specification.

Compatibility

The NT6X45BC is functionally equivalent to the other NT6X45 processors. The difference between the AB, AC, AD, AE, AF, BA, and BB versions is in the onboard firmware. The firmware in the added functionality that supports initialization of the NT6X50AB on the central side (C-side) in a remote application. This added functionality is backward-compatible with the NT6X45BA and NT6X45BB. This functionality is in the remote cluster controller (RCC) and ISDN RCC (RCCI) XPMs.

Functional description

Functional blocks

The NT6X45BC contains the following functional blocks:

- CPU
- data bus
- memory management unit
- sanity and clock control
- A-bus interface
- onboard input/output (I/O) facilities

Central processing unit

The CPU supports 16 linear 16-Mbyte virtual address spaces. A Motorola 68000 microprocessor that runs at 8 MHz is used for the CPU.

Data bus

The data bus uses data paths to memory that are 16-bits wide.

Memory management unit

The memory management unit converts virtual addresses, that an executing program generates, to addresses used to access real memory.

NT6X45BC (continued)

Sanity and clock control

The sanity timer protects the computing node against a software failure. The software failure can mask each interrupt level and prevent external communication.

Address-bus interface

Memory and I/O controllers communicate with the processor board over the A-bus. Enough drive capability is available to allow a maximum of 16 LS Schottky connections to the A-bus.

Onboard input/output facilities

The CPU has access to the following input/output facilities:

- PROM
- programmable timers
- terminal controller
- dataport controller
- baud rate selection

Two EPROM chips are the resident bootstrap loader and low-level monitor.

An Intel 8253 provides three timers, each under software control. Timer 1 provides the clock tick for task scheduling. Timers 2 and 3 connect to form the 32-bit sanity timer register (STR).

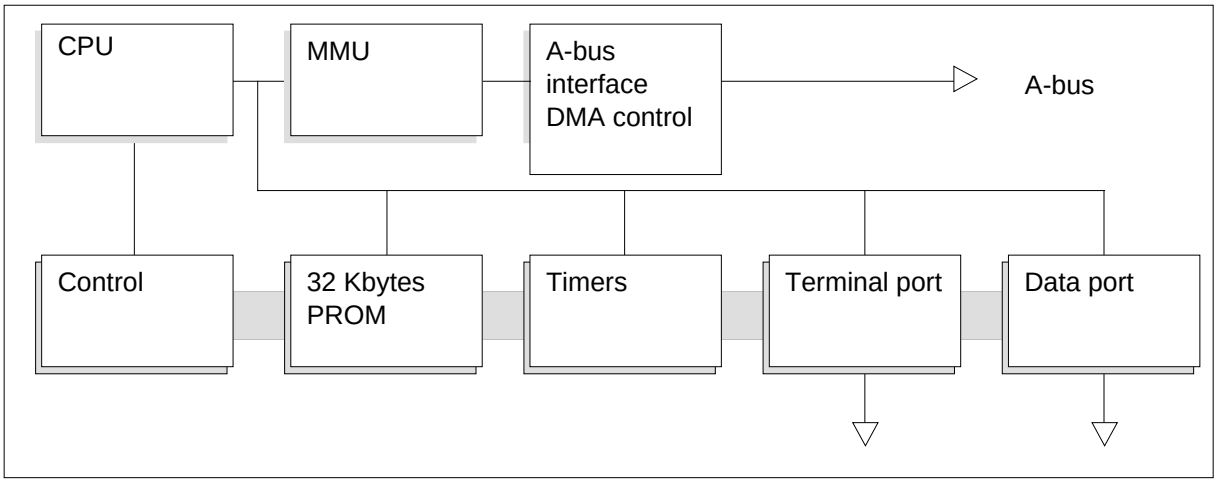
An Intel 8251A universal synchronous/asynchronous receiver/transmitter (USART) accesses the terminal.

An Intel 8251A USART communicates with the dataport port.

A Motorola K1135B baud-rate generator provides terminal and dataport clocks.

The relationship between the functional blocks appears in the following figure.

NT6X45BC functional blocks



Technical data

Power requirements

The power requirements for the NT6X45 circuit card are:

- voltage: +5V, +12V, -12Vdc
- current: 1.5A
- 48V power use: 7.5W

Signaling

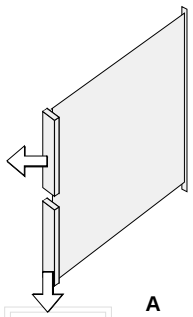
Pin numbers

The pin numbers for the NT6X45BC appear in the following figure.

NT6X45BC (end)

NT6X45BC pin numbers

		A	B
1A	1B	GND	GND
2A	2B	PWR+5	PWR+5
3A	3B	PWR+5	PWR+%
4A	4B	PWR+5	PWR+5
5A	5B	GND	GND
6A	6B	BUS	Req–
7A	7B	BUSGRI–	
8A	8B	BUSGRO–	
9A	9B	BUSBSY–	
10A	10B	4XCLK–	OSCOUT–
11A	11B	GND	MMUTSTO–
12A	12B	DAS–	AS+
13A	13B	LDS–	2XCLK+
14A	14B	DTACK–	2XCLKSYN+
15A	15B	UDS–	1XCLKSYN+
16A	16B	WRT–	SANDIS–
17A	17B	1XCLK+	1XCLK–
18A	18B	RSTOUT–	RSTIN–
19A	19B	PERINTO–	HWRST–
20A	20B	PERINT1–	IRQ4
21A	21B	PERINT2–	
22A	22B	GND	
23A	23B	PERINT3–	
24A	24B	PERINT4–	
25A	25B	PERINT5–	
26A	26B	PERINT6–	
27A	27B	PERINT7–	GND
28A	28B	MEMIRQ–	LOOPI–
29A	29B	ADDRO1+	LOOPO–
30A	30B	ADDRO2+	HPU12+
31A	31B	ADDRO3+	HDICLK+
32A	32B	ADDRO4+	HDOCLK+
33A	33B	ADDRO5+	HACKOUT+
34A	34B	GND	HDOUT+
35A	35B	ADDRO6+	HDIN+
36A	36B	ADDRO7+	TPU12+
37A	37B	ADDRO8+	TACKIN+
38A	38B	ADDRO9+	TDOUT+
39A	39B	ADDR10+	TDIN+
40A	40B	ADDR11+	GND



		A	B
41A	41B	GND	BUSTIMO–
42A	42B	ADDR12+	F0BXXX–
43A	43B	ADDR13+	F0CXXX–
44A	44B	ADDR14+	
45A	45B	ADDR15+	
46A	46B	ADDR16+	
47A	47B	ADDR17+	GND
48A	48B	ADDR18+	
49A	49B	ADDR19+	
50A	50B	ADDR20+	
51A	51B	ADDR21+	
52A	52B	(ADDR22+)	
53A	53B	GND	
54A	54B	(ADDR23+)	
55A	55B	FC0–	
56A	56B	FC1–	
57A	57B	FC2–	
58A	58B	DATA00+	
59A	59B	DATA01+	GND
60A	60B	DATA02+	
61A	61B	DATA03+	
62A	62B	DATA04+	
63A	63B	DATA05+	
64A	64B	GND	
65A	65B	DATA06+	
66A	66B	DATA07+	
67A	67B	DATA08+	
68A	68B	DATA09+	
69A	69B	DATA10+	
70A	70B	DATA11+	GND
71A	71B	DATA12+	
72A	72B	DATA13+	BP1+
73A	73B	DATA14+	BP2+
74A	74B	DATA15+	BP3+
75A	75B		BP4+
76A	76B	GND	GND
77A	77B	PWR+12	PWR–12
78A	78B	GND	GND
79A	79B	PWR+12	PWR–12
80A	80B	GND	GND

NT6X46BA

Product description

The NT6X46BA CPCE signaling processor (SP) memory card supplies the memory for the SP. The memory is used in new peripherals like line trunk controllers (LTC) or digital trunk controllers (DTC).

The SP can have with one NT6X46BA card.

Functional description

The NT6X46BA performs the following functions:

- provides 1 Mbyte of dynamic RAM for the SP
- provides memory for the floating point (FP), in the event of the international line trunk controller (ILTC)
- provides direct memory access (DMA) to the modem pool (MP) memory
- controls shelf activity in dual-shelf configurations of new peripherals.

Signaling

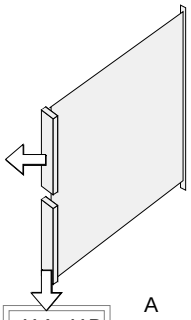
During DMA operation, the SP controls the MP memory and supplies the signals necessary for data transfers. The DMA sequencing logic makes sure that the timing of these signals maintains 68000 microprocessor protocol.

Interface pin numbers

The backplane pin numbers for the NT6X46BA appear in the following figure.

NT6X46BA (end)

NT6X46BA pin numbers



	A	B
1A 1B	Gnd	Gnd
2A 2B	PWR+5	PWR+5
3A 3B	PWR+5	PWR+5
4A 4B	PWR+5	PWR+5
5A 5B	Gnd	Gnd
6A 6B	BUSREQ–	MBUSREQ–
7A 7B	BUSGRI–	MBUSGRI–
8A 8B	BUSGRO–	MBUSGRO–
9A 9B	BUSBSY–	MBUSBSY–
10A 10B	4XCLK–	MDAS–
11A 11B	Gnd	MLDS
12A 12B	DAS–	AS+
13A 13B	LDS–	2XCLK+
14A 14B	DTACK–	MDTACK–
15A 15B	UDS–	MUDS–
16A 16B	WRT–	MWRT–
17A 17B	1XCLK+	1XCLK–
18A 18B	SPRST–	MSGRST–
19A 19B	MPRST–	
20A 20B	FPRST–	
21A 21B	ADM20+	
22A 22B	Gnd	REFDIS–
23A 23B	SP–	EXTREF–
24A 24B	MP–	ACTIRQ–
25A 25B	ACTIVE–	MLPBAD–
26A 26B	OWNACT–	MUPBAD–
27A 27B	MATEACT–	Gnd
28A 28B	MEMIRQ–	MDMADEV–
29A 29B	ADDR01+	MADDR01+
30A 30B	ADDR02+	MADDR02+
31A 31B	ADDR03+	MADDR03+
32A 32B	ADDR04+	MADDR04+
33A 33B	ADDR05+	MADDR05+
34A 34B	Gnd	MADDR06+
35A 35B	ADDR06+	MADDR07+
36A 36B	ADDR07+	MADDR08+
37A 37B	ADDR08+	MADDR09+
38A 38B	ADDR09+	MADDR10+
39A 39B	ADDR10+	MADDR11+
40A 40B	ADDR11+	Gnd

	A	B
41A 41B	Gnd	MADDR12+
42A 42B	ADDR12+	MADDR13+
43A 43B	ADDR13+	MADDR14+
44A 44B	ADDR14+	MADDR15+
45A 45B	ADDR15+	MADDR16+
46A 46B	ADDR16+	MADDR17+
47A 47B	ADDR17+	Gnd
48A 48B	ADDR18+	MADDR18+
49A 49B	ADDR19+	MADDR19+
50A 50B	ADDR20+	MADDR20+
51A 51B	ADDR21+	MADDR21+
52A 52B	(ADDR22+)	MADDR22+
53A 53B	Gnd	MODRST+
54A 54B	(ADDR23+)	MADDR23+
55A 55B	TSTO–	TLPO–
56A 56B	FC1–	TUPO–
57A 57B	FC2–	MFC2–
58A 58B	DATA00+	MDATA00+
59A 59B	DATA01+	Gnd
60A 60B	DATA02+	MDATA01+
61A 61B	DATA03+	MDATA02+
62A 62B	DATA04+	MDATA03+
63A 63B	DATA05+	MDATA04+
64A 64B	Gnd	MDATA05+
65A 65B	DATA06+	MDATA06+
66A 66B	DATA07+	MDATA07+
67A 67B	DATA08+	MDATA08+
68A 68B	DATA09+	MDATA09+
69A 69B	DATA10+	MDATA10+
70A 70B	DATA11+	Gnd
71A 71B	DATA12+	MDATA11+
72A 72B	DATA13+	MDATA12+
73A 73B	DATA14+	MDATA13+
74A 74B	DATA15+	MDATA14+
75A 75B	SWACLK+	MDATA15+
76A 76B	Gnd	Gnd
77A 77B	PWR+12	PWR+12
78A 78B	Gnd	Gnd
79A 79B	PWR–12	PWR–12
80A 80B	Gnd	Gnd

NT6X46BB

Product description

The NT6X46BB extended multiprocessor system (XMS)-based peripheral module (XPM) signaling processor (SP) memory card provides a maximum of 1 Mbyte of SP XPM dynamic RAM (DRAM). The DRAM contains one half-bank of 1-Mbyte words, or 16 bits. The system uses 1-Mbyte times 1-bit DRAM devices for this arrangement. Any domestic XPM can have a maximum of one circuit pack. International XPMs use two packs.

The NT6X46BB fills the complete physical address range of the current architecture. The RAM on this card occupies the SP real address range of 00 0000 to 0F FFFF Hex. The current XPM backplanes have 21 SP address lines. These lines provide a maximum physical address space of 4 Mbyte:

- SP memory uses 1 Mbyte
- memory-mapped Input/Output (I/O) uses 1 Mbyte. Memory-mapped I/O includes:
  - — universal tone receiver (UTR) cards
  - — custom local area signaling service (CLASS) modem resource (CMR) cards
  - — message cards
- master processor (MP) memory uses 2 Mbytes

The control/status words conform to the NT6X46BA card. The control/status registers are backward compatible with the NT6X46AB/BA. The control/status registers respond to reads and writes from the control/status location of the NT6X46AB/BA. The contents of the one on-board status register on the 6X46BBA appear at a read to location 3F 8XXX. A read or write to address 3F AXXX or 3F DXXX does not cause a response. This condition is a bus error and conforms with the NT6X46BA.

Location

New peripherals like the line trunk controllers (LTC) and the ISDN line trunk controllers (LTCI) use the NT6X46BB.

Functional description

The functions of the NT6X46BB are the same as the functions of the NT6X46BA. The logic of the NT6X46BB is power reduced with current technologies. The 1 Mbyte of DRAM appears as one bank of 1 Mbyte (8 bits). The byte has one parity bit added. The system accesses this 1-Mbyte bank twice during memory access. The system access the bank to obtain 16 bits of

NT6X46BB (continued)

data. The SP memory space is 0.5 Mwords. Sixteen 1-Mbyte times 1-bit DRAM integrated circuits (IC) leaves half the available memory in each chip.

The NT6X46BB uses the upper and lower data strobe signals to determine when to generate the write enable (WE) signal. The upper and lower data strobe signals are IUDS- and ULDS-. For a word access, the card asserts WE for the complete cycle. For a byte access, the card only asserts the WE signal during a specified part of the cycle. The card asserts this signal in a specified part of the cycle to obtain the correct byte.

After the card starts a valid memory access, the system activates a data transfer acknowledge (DTACK-) signal. This signal indicates a completed memory transaction to the processor. The system generates DTACK- for a processor that runs at 8 MHz. This action makes sure the processor does not insert wait states in a memory cycle.

You can apply the NT6X46BB to any XPM that uses the NT6X46BA/AC memory.

You must remove the NT6X1205 backplane terminator from any XPM before you introduce this circuit card in the XPM.

Refresh

Refresh on the NT6X46BB is column address strobe (CAS) before row address strobe (RAS). The system generates a refresh request, internal to the logic cell array (LCA) at intervals of 15.8 &0xb5;s. The LCA performs a memory refresh cycle at the end of the current memory cycle. The cycle is AS and DTACK unasserted.

Parity

The LCA checks parity on the NT6X46BB. During a read, the LCA examines QP and DP twice. The LCA checks QP and DP once for each byte of data. The LCA latches the results at the correct time. If an error occurs, the system generates an interrupt (MEMIRQ-).

Control and status

A read or a write to hex address 3F80XX where XX indicates don’t care, allows access to the control area. The control register controls parity checking. A write to the least significant data byte of location 3F80XX sets the control bits.

Interprocessor interrupts

The NT6X46BB does not use pins 19B, 20B, and 21B. These pins previously served as interprocessor interrupts on NT6X46AA. The redefines pin 18B as

an additional reset input. The NT6X46BB does not use control address 3F84XX.

Direct memory access

The SP memory card provides memory for the SP. The SP memory card provides direct memory access (DMA) to the memory of the MP. An address decode in the SP of a hex address in the range of 200000 to 3EFFFF initiates DMA access. The addresses on the SP correspond to real addresses on the MP memory in the range of 000000 to 1EFFFF. The SP uses the upper 2 Mbyte of the SP 4-Mbyte memory space. The SP uses this space to view the bottom 2 Mbyte of the MP memory. The upper 64-Kbyte block of this range is not available. This state prevents potential conflicts with control or status addresses located above 3EFFFF.

When an attempt to access memory in this range occurs, the backplane signal MBUSREQ- issues a bus request to the MP. If the MP is busy, the bus busy signal (MBUSBSY-) delays DMA action. When the request occurs, the MP issues a bus grant out (MBUSGRO-) signal. When the current bus cycle of the MP completes, the MP releases the MBUSBSY- signal to return the bus. The SP receives the bus grant from the MP on the backpanel pin of the MP bus. The SP memory asserts the MBUSBSY- signal to indicate that the SP received the bus grant.

During DMA operation, the SP controls the memory of the MP. The SP must supply all signals for data transfers. DMA action (DMA-) enables the following processes on the backplane as signals:

- delayed address strobe (MDAS-)
- write (MWRT-)
- upper data strobe (MUDS-)
- lower data strobe (MLDS-)

These signals perform the same function as the DAS-, WRT-, UDS-, and LDS- signals. The MP disabled off the bus supplied this group of signals. DMA sequencing logic makes sure the timing of these signals complies with 68000 microprocessor protocol. In response to a DMA action, the DTACK- signal is delayed through a flip-flop and gated with the data strobe (DS+). This action provides the SP with a DMA data transfer acknowledge. An MP memory provides the DTACK- signal.

When the DMA cycle completes, the SP memory card releases the MBUSBSY- signal. This action returns the bus to the MP. The MP resumes control of the bus for a minimum of one instruction cycle. When this cycle completes, another DMA request can cause the SP to control the bus again.

NT6X46BB (continued)

Shelf activity

The SP memory card contains logic to control shelf activity in dual shelf configurations of the current peripherals. A supervisor state read of address area 3F830X accesses the control area for the activity logic. Shelf activity logic appears in the following table:

Shelf activity

Address area	Supervisor state read
3F8301	PREPARE-
3F8303	ACTACK-
3F8305	DROPACT-
3F8307	ACTIAK-
3F8309	CLR_AM-

A supervisor read of any of the above addresses causes the system to generate the specified control pulse. A description of the operation of the activity logic follows. The module reset generator is part of the activity logic. A counter clocked by 1XCLK+ divided by 2 (CLKDIV2+) generates the module reset pulse (MODRST-). The counter makes sure the minimum pulse width on the reset line complies with the 68000 protocol. The activity circuits can start a module reset.

The backplane inputs to the circuit pack supply the following external sources of the reset:

- the SP reset (1SPRST-)
- the MP reset (MPRST-)
- the facilities processor reset (FPRST-)
- the message card reset (MSGRST-)

A reset from any of these sources causes a module reset.

The loss of activity signal (LOSTACT-) can cause a module reset. The system cannot prevent module resets that external reset sources cause. The system can prevent a module reset that a LOSTACT- signal causes. The system must use the PREPARE- pulse to inhibit the LOSTACT- signal. The system must inhibit this signal to prevent a module reset during a controlled switch of activity.

To synchronize the drop of activity, the system clocks the drop activity control pulse (DROPACT-) with the switch activity clock (SWACLK+). The drop

signal (DROP-) sets a flip-flop with two NAND gates. Each of the two SP memory cards in shelf 0 and shelf 1 of a dual shelf system contains one gate. The flip-flop allows the DROP- to signal the mate shelf. The signal indicates that the mate shelf must take over activity. The loss of activity clocks a flip-flop that can trigger the module reset generator. The time that the system used the PREPARE- signal determines if the flip-flop triggers the generator. Activity gain issues an activity interrupt request (ACTIRQ-) to the SP. The SP must acknowledge the request. The SP sends the acknowledge signal ACTIAK- to clear the request. A read of this register can determine activity.

A monostable multivibrator serves as an activity timer. This timer is set to time out at 1.5 s. An activity acknowledge control pulse (ACTACK-) resets the activity timer. This action prevents a time out if the system issues an acknowledge at intervals shorter than 1.5 s. A time out of the activity timer forces a drop of activity. This event causes the system to request the inactive mate shelf to take over activity.

The activity monitor flip-flop can test activity drop on an inactive shelf. A clear activity monitor (CLRAM-) control pulse clears this flip-flop. A software-initiated drop of activity or an activity time out sets the flip-flop. The read of the status register can occur after the CLRAM- signal and before the DROP- signal. If this condition occurs, bit D10 of the status register must be 0. After the DROP-, bit D10 must be 1. This setting indicates that a request occurred for a drop of activity.

Reset operation

The reset circuits on the NT6X46 generate the shelf or unit reset signal (MODRST-). This action occurs in response to external reset input, loss of activity, or insane software.

External resets

Any of the following four input signals can cause the 6X46 to reset the shelf:

- MPRST-MP reset (6X45)
- SPRST-SP reset (6X45)
- FPRST-FP reset (6X45)
- MSGRST-Message card reset (6X69)

NT6X46BB (continued)

The processor card generates the first three reset inputs. One of the following conditions causes the first three reset inputs:

- Power-up
- Sanity problem
- 68000 reset instruction

The 6X69 can decode a reset message from the C-side DS30s to generate a reset to the 6X69.

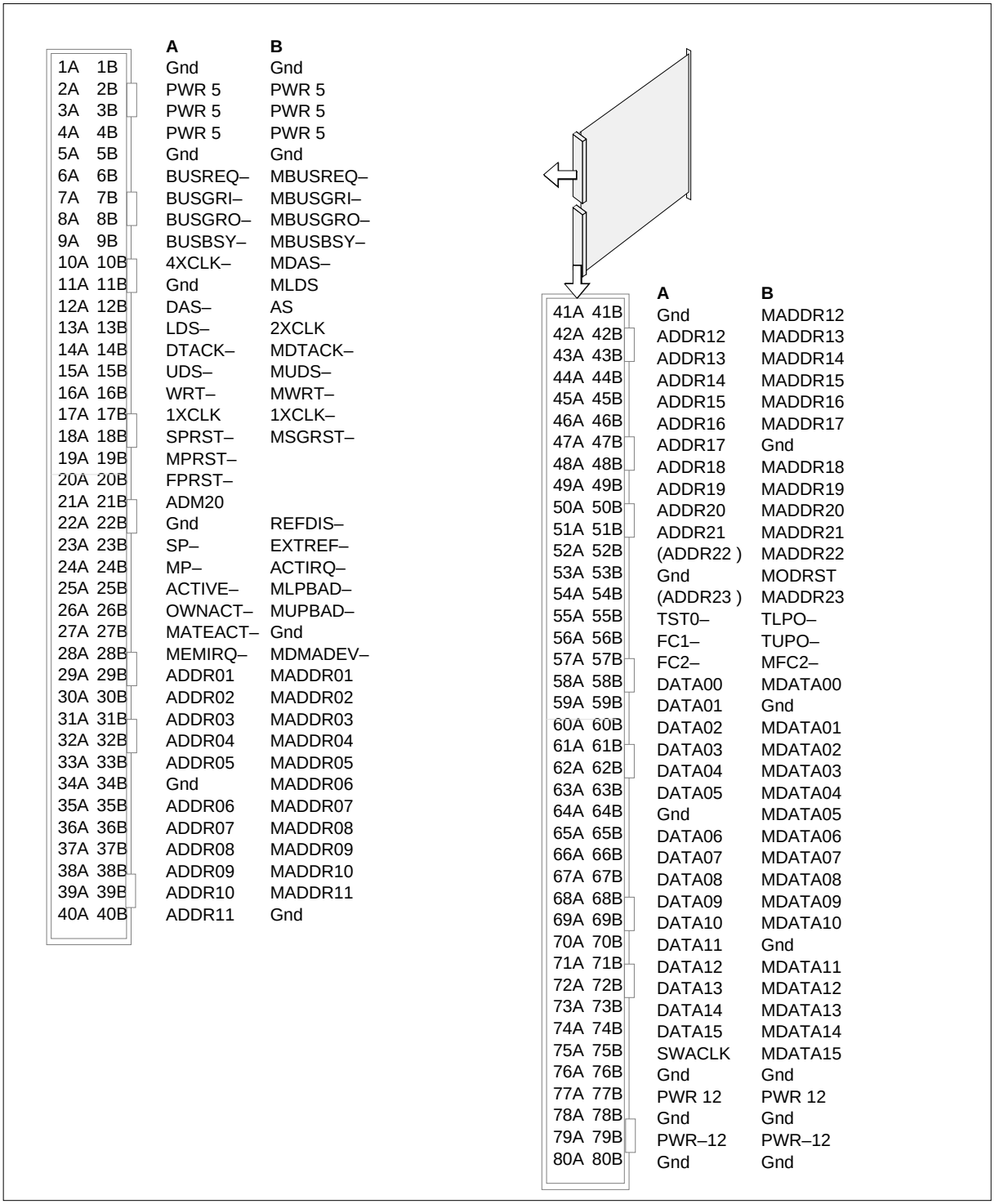
Signaling

Pin numbers

The pin numbers for NT6X46BB appear in the following figure.

NT6X46BB (continued)

NT6X46BB pin numbers



	A	B
1A 1B	Gnd	Gnd
2A 2B	PWR 5	PWR 5
3A 3B	PWR 5	PWR 5
4A 4B	PWR 5	PWR 5
5A 5B	Gnd	Gnd
6A 6B	BUSREQ–	MBUSREQ–
7A 7B	BUSGRI–	MBUSGRI–
8A 8B	BUSGRO–	MBUSGRO–
9A 9B	BUSBSY–	MBUSBSY–
10A 10B	4XCLK–	MDAS–
11A 11B	Gnd	MLDS
12A 12B	DAS–	AS
13A 13B	LDS–	2XCLK
14A 14B	DTACK–	MDTACK–
15A 15B	UDS–	MUDS–
16A 16B	WRT–	MWRT–
17A 17B	1XCLK	1XCLK–
18A 18B	SPRST–	MSGRST–
19A 19B	MPRST–	
20A 20B	FPRST–	
21A 21B	ADM20	
22A 22B	Gnd	REFDIS–
23A 23B	SP–	EXTREF–
24A 24B	MP–	ACTIRQ–
25A 25B	ACTIVE–	MLPBAD–
26A 26B	OWNACT–	MUPBAD–
27A 27B	MATEACT–	Gnd
28A 28B	MEMIRQ–	MDMADEV–
29A 29B	ADDR01	MADDR01
30A 30B	ADDR02	MADDR02
31A 31B	ADDR03	MADDR03
32A 32B	ADDR04	MADDR04
33A 33B	ADDR05	MADDR05
34A 34B	Gnd	MADDR06
35A 35B	ADDR06	MADDR07
36A 36B	ADDR07	MADDR08
37A 37B	ADDR08	MADDR09
38A 38B	ADDR09	MADDR10
39A 39B	ADDR10	MADDR11
40A 40B	ADDR11	Gnd

	A	B
41A 41B	Gnd	MADDR12
42A 42B	ADDR12	MADDR13
43A 43B	ADDR13	MADDR14
44A 44B	ADDR14	MADDR15
45A 45B	ADDR15	MADDR16
46A 46B	ADDR16	MADDR17
47A 47B	ADDR17	Gnd
48A 48B	ADDR18	MADDR18
49A 49B	ADDR19	MADDR19
50A 50B	ADDR20	MADDR20
51A 51B	ADDR21	MADDR21
52A 52B	(ADDR22)	MADDR22
53A 53B	Gnd	MODRST
54A 54B	(ADDR23)	MADDR23
55A 55B	TST0–	TLPO–
56A 56B	FC1–	TUPO–
57A 57B	FC2–	MFC2–
58A 58B	DATA00	MDATA00
59A 59B	DATA01	Gnd
60A 60B	DATA02	MDATA01
61A 61B	DATA03	MDATA02
62A 62B	DATA04	MDATA03
63A 63B	DATA05	MDATA04
64A 64B	Gnd	MDATA05
65A 65B	DATA06	MDATA06
66A 66B	DATA07	MDATA07
67A 67B	DATA08	MDATA08
68A 68B	DATA09	MDATA09
69A 69B	DATA10	MDATA10
70A 70B	DATA11	Gnd
71A 71B	DATA12	MDATA11
72A 72B	DATA13	MDATA12
73A 73B	DATA14	MDATA13
74A 74B	DATA15	MDATA14
75A 75B	SWACLK	MDATA15
76A 76B	Gnd	Gnd
77A 77B	PWR 12	PWR 12
78A 78B	Gnd	Gnd
79A 79B	PWR–12	PWR–12
80A 80B	Gnd	Gnd

NT6X46BB (end)

Technical data

Power requirements

The NT6X46BB card has the following power requirements:

- voltage:+5 V, +12 V, -12 V
- current:1.85 A mean (+ or - 0.1 A)
- power:9.25 W typical

NT6X47AC

Product description

This document describes the NT6X47AC master processor (MP) memory circuit card. The NT6X47AC provides dynamic RAM (DRAM) to extended multiprocessor system (XMS)-based peripheral modules (XPM).

The NT6X47AC card eliminates the need for two NT6X47AB circuit cards. The card reduces power use. The card permits more than two Mbytes of MP memory in emergency stand-alone (ESA) and message switch buffer (MSB7) XPMs. The NT6X47AC has the following features:

- four Mbyte of DRAM on a single card
- onboard refresh clock. This clock allows the card to retain the contents of the memory when you remove the NT6X45AC processor cards
- backward compatibility with NT6X47AB. There is no change in functionality.
- parity selection
- memory bank selection
- faster read and write cycle times

Functional description

The NT6X47AC provides 4 Mbyte of DRAM on a single circuit card. The NT6X47AC replaces the NT6X47AB. The memory in the NT6X47AC is twice the memory of the NT6X47AB.

The 4-Mbyte memory divides in two independent 2-Mbyte modules. Each module consists of two banks of 1-Mbyte words (16 bits). Each byte of each word has two parity bits for a total of 18 bits on each bank. The 1-Mbyte times one-bit DRAM devices implement the bits on each bank. The DRAM consists of 36 one-Mbyte times one-bit memory devices.

NT6X47AB memory can equip the NT6X47AC card in all XPMs. The use of the NT6X47AC in MSB6/7 applications has limits. You must make software modifications to the MSB to eliminate the limits.

The operation of the NT6X47AC is transparent to the user. The NT6X47AC uses a single parity bit for the least and most important bytes of data to provide data integrity checking.

The refresh clock source generated on the NT6X45AC does not maintain the data integrity of the DRAM array. The on-board 20-MHz clock source continues to run when you remove the NT6X45AC processor.

NT6X47AC (continued)

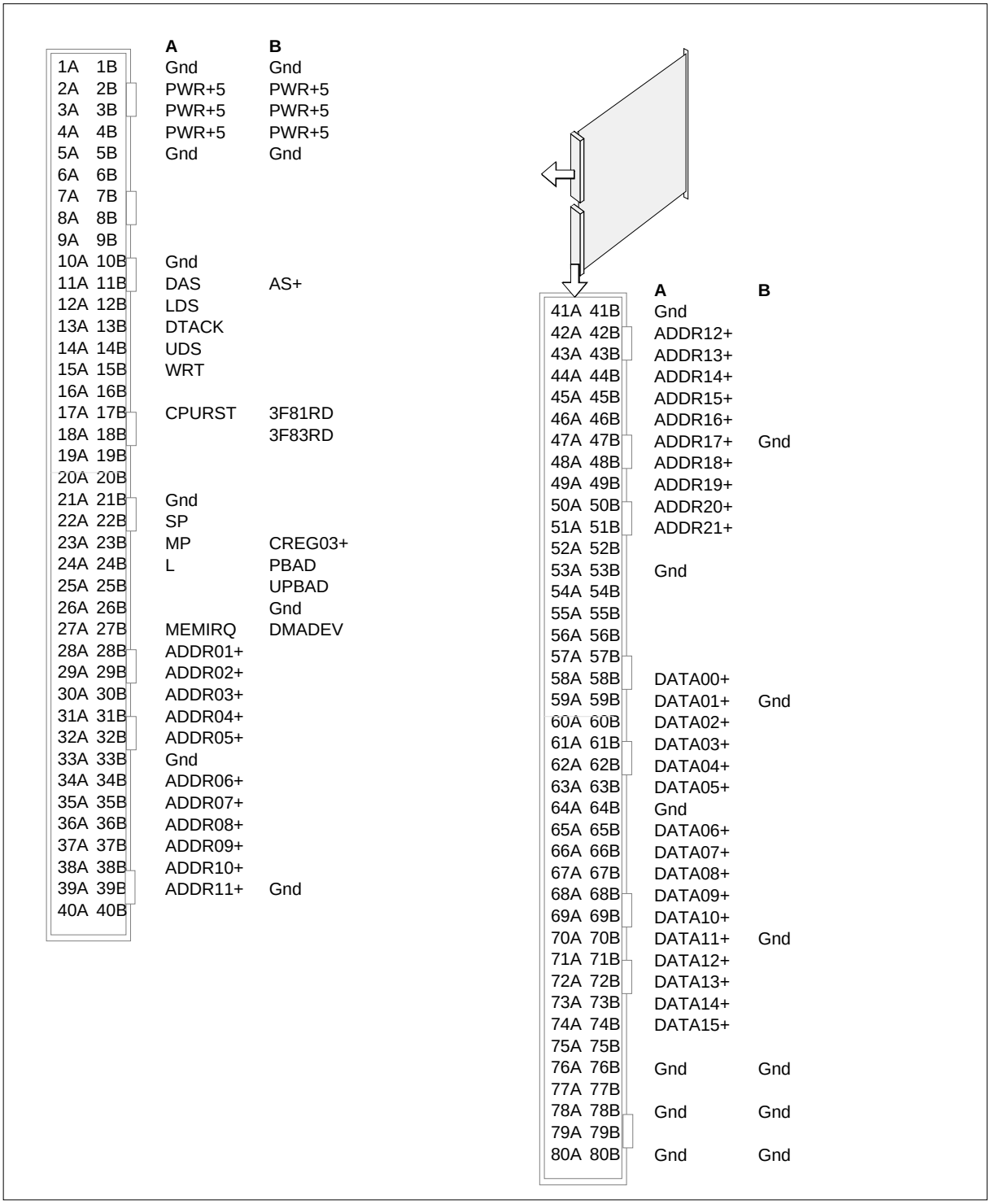
Signaling

Pin numbers

The pin numbers for the NT6X47ACappear in the following table.

NT6X47AC (continued)

NT6X47AC pin numbers



	A	B
1A 1B	Gnd	Gnd
2A 2B	PWR+5	PWR+5
3A 3B	PWR+5	PWR+5
4A 4B	PWR+5	PWR+5
5A 5B	Gnd	Gnd
6A 6B		
7A 7B		
8A 8B		
9A 9B		
10A 10B	Gnd	
11A 11B	DAS	AS+
12A 12B	LDS	
13A 13B	DTACK	
14A 14B	UDS	
15A 15B	WRT	
16A 16B		
17A 17B	CPURST	3F81RD
18A 18B		3F83RD
19A 19B		
20A 20B		
21A 21B	Gnd	
22A 22B	SP	
23A 23B	MP	CREG03+
24A 24B	L	PBAD
25A 25B		UPBAD
26A 26B		Gnd
27A 27B	MEMIRQ	DMADEV
28A 28B	ADDR01+	
29A 29B	ADDR02+	
30A 30B	ADDR03+	
31A 31B	ADDR04+	
32A 32B	ADDR05+	
33A 33B	Gnd	
34A 34B	ADDR06+	
35A 35B	ADDR07+	
36A 36B	ADDR08+	
37A 37B	ADDR09+	
38A 38B	ADDR10+	
39A 39B	ADDR11+	Gnd
40A 40B		

	A	B
41A 41B	Gnd	
42A 42B	ADDR12+	
43A 43B	ADDR13+	
44A 44B	ADDR14+	
45A 45B	ADDR15+	
46A 46B	ADDR16+	
47A 47B	ADDR17+	Gnd
48A 48B	ADDR18+	
49A 49B	ADDR19+	
50A 50B	ADDR20+	
51A 51B	ADDR21+	
52A 52B		
53A 53B	Gnd	
54A 54B		
55A 55B		
56A 56B		
57A 57B		
58A 58B	DATA00+	
59A 59B	DATA01+	Gnd
60A 60B	DATA02+	
61A 61B	DATA03+	
62A 62B	DATA04+	
63A 63B	DATA05+	
64A 64B	Gnd	
65A 65B	DATA06+	
66A 66B	DATA07+	
67A 67B	DATA08+	
68A 68B	DATA09+	
69A 69B	DATA10+	
70A 70B	DATA11+	Gnd
71A 71B	DATA12+	
72A 72B	DATA13+	
73A 73B	DATA14+	
74A 74B	DATA15+	
75A 75B		
76A 76B	Gnd	Gnd
77A 77B		
78A 78B	Gnd	Gnd
79A 79B		
80A 80B	Gnd	Gnd

NT6X47AC (end)

Technical data

Characteristics

The characteristics of the NT6X47AC are as follows:

- height: 12.5 inches (317.5 mm)
- width: 10.0 inches (254.0 mm)

Power requirements

NT6X47AC uses a maximum current of 1.01 A and requires a continuous dc voltage of +5 V. This method cuts power use by a minimum of half the amount of power that one NT6X47AB circuit card uses. One NT6X47AB circuit card uses 2.31 A. The NT6X47AC card reduces power use by a minimum of one fourth the amount of power that the two NT6X47AB circuit cards used. The NT6X47AC replaces the two NT6X47AB circuit cards. The system does not use ac voltage on the card.

The NT6X47AC has the following power requirements.

- voltage: +5V (+4.75 to +5.25 V)
- current: 1.01 A maximum
- power: 5.05 W maximum

NT6X48AA

Product description

The NT6X48AA provides the interface between the line group controller (LGC) and the line concentrating module (LCM).

Functional description

Functional blocks

The NT6X48AA contains the following functional blocks:

- port multiplexers (MUX)
- port demultiplexers (DEMUX)
- clock and floating point (FP) generator
- differential drivers
- differential receivers
- DS30A link enable circuit
- channel 16 (CH16) looparound circuit

Port multiplexers

The port multiplexers clock pulse code modulation (PCM) incoming (PCMIN) data at the positive edge of the clock at the LCM. The port multiplexers clock the data in on the next positive edge of the C390+ clock at the LGC. This action makes sure the required setup time is available to accommodate different delays. Different cable lengths and delays cause delays. The cable between the LGC and the LCM must be a maximum length of 50 ft. The multiplexers multiplex and clock latched data. Multiplexing is necessary because pin number limits are present on the backplane. The multiplexers multiplex adjacent ports together.

Port demultiplexers

The port demultiplexers demultiplex PCM outgoing (PCMOUT) data from the formatter. The demultiplexers clock out demultiplexed remote pulse code modulation (RPCM) ports to the LCM on the positive edge of the C390+ clock.

Clock and floating point generator

The C97+ shelf clock divides in the C195 and C390+ clocks. The clock and floating generator synchronizes these clocks to have a positive transition in the middle of the shelf FP. The generator distributes the C195+ clock to the balance drivers. The balance drivers send the C195+ clock to the LCM. The balance drivers transmit a clock that is twice the data rate because the transmission path contains a skew. The required clock rate is recovered at the LCM with a 50% duty cycle.

NT6X48AA (continued)

The DS30A delays the PCMOUT data from the formatter. The DS30A card delays the FP to align the FP to the LCM. The card uses two cascaded binary counters to delay the FP. These cascaded binary counters use the C195+ clock. When the shelf FP occurs, the counter is initialized to a value that produces an overflow pulse with the required delay. The balance drivers send the delayed FP to the LCM. The balance drivers feed the FP back to stop the counters. This action allows the counters to restart at the next FP.

Differential drivers

Differential drivers are balanced drivers. Each incoming pack contains three drivers needed for one DS30A link. A fourth driver is available, which the link does not use. This fourth driver increases reliability. The differential outputs of the drivers are series terminated by 27[_Inline:Symbols:A ~Symbol {-w}] resistors to keep reflection to a minimum. The activity line determines the activation or deactivation of these drivers. The drivers send the clock, FP, and RPCM to the LCM.

Differential receivers

Differential receivers are balanced receivers that accept PCMIN differential input. These receivers produce a transistor-transistor logic (TTL) output. 200 Ω resistors terminate the inputs. The two receiver inputs that correspond to the two DS30A cards are tied together. The termination that results is 100 Ω. This impedance matching keeps reflection to a minimum.

DS30A link enable circuit

An LCM pair uses between 2 and 6 of the 20 DS30A links that extend from an LGC pair. The DS30A link enable circuit allows the system to disable drivers for the links that the system does not use. The time switch card uses five control lines to control the activation and deactivation of the ports. Each control line contains multiplexed information for two ports. The ports are demultiplexed and used with the activity line to enable and disable the drivers.

CH16 looparound circuit

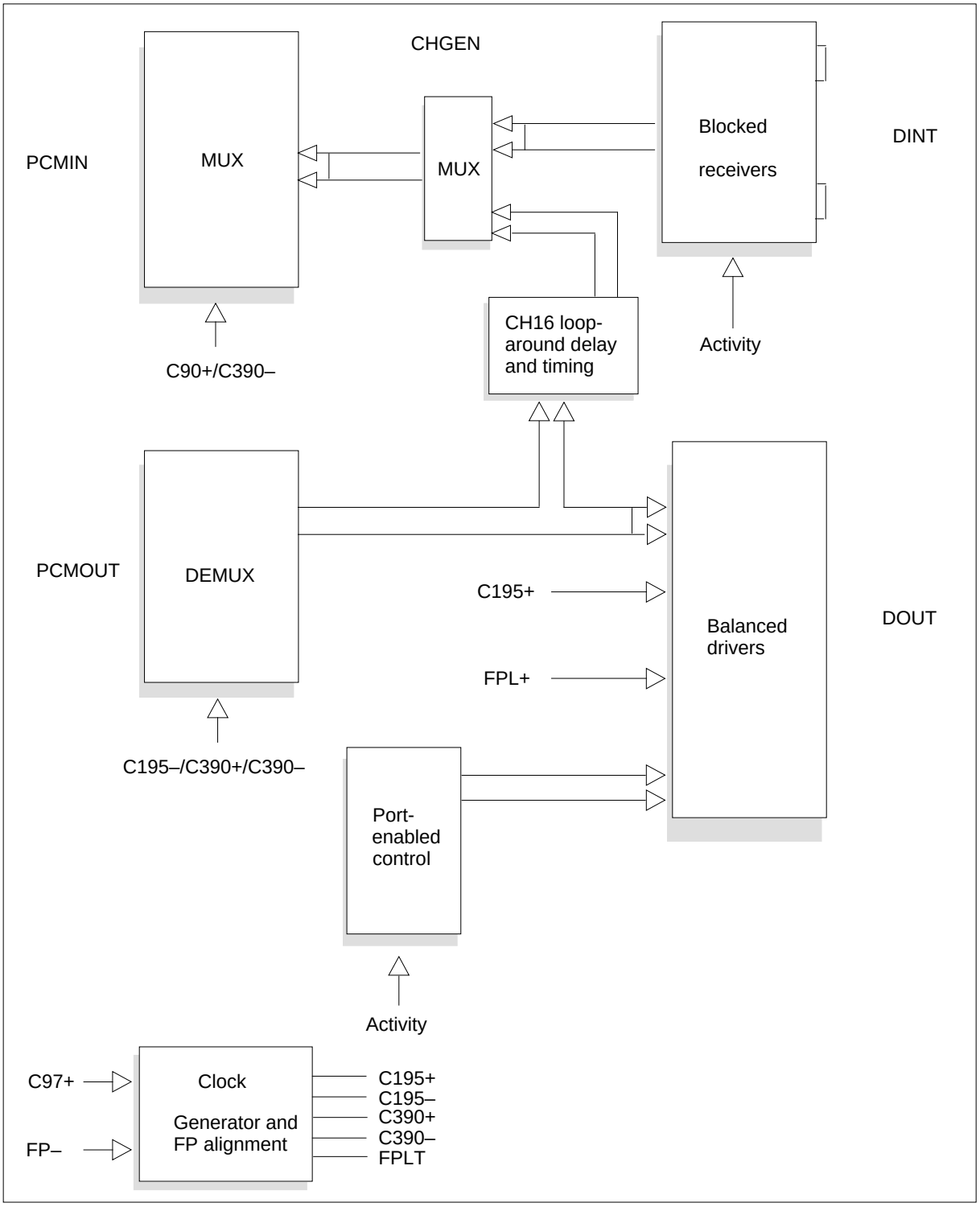
The system permanently loops the CH16 PCMOUT data around the looparound circuit. Approximately four channels separate PCMIN and PCMOUT data. Three RAMs help delay the PCMOUT by the correct bit times. The system reads from and writes in the RAMs during a cycle for each address. A counter chain that resets to a preset value at overflow generates addresses. Another counter chain generates the CH16EN signal. This signal is an 8-bit-long pulse that coincides with CH16 of PCMIN, or CH12 of PCMOUT. This signal inserts the delayed looped-around PCMOUT for CH16 to the PCMIN stream during the correct channel slot. Two ports are multiplexed together. The ports transfer to the time switch.

NT6X48AA (continued)

The relationships between the functional blocks appear in the following figure.

NT6X48AA (end)

NT6X48AA functional blocks



NT6X50AA

Product description

The NT6X50AA DS-1 interface card provides a two-way voice, data, and signaling interface. This interface occurs between the common peripheral controller (CPC) in the DMS-100 and one two-way port in standard DS-1 systems. The card contains two circuits that perform the same functions separately.

Location

The DS-1 interface card plugs in one of five assigned slots in the NT6X02 CPC shelf. This interface card can plug in additional shelves that use NT6X50 cards.

Functional description

The NT6X50AA receives and transmits data between the CPC shelf and the DS-1 ports. Clock signals control the card. The card converts unipolar data to bipolar data for transmission to the DS-1 ports. The card converts bipolar data to unipolar data for transmission to the CPC shelf.

Functional blocks

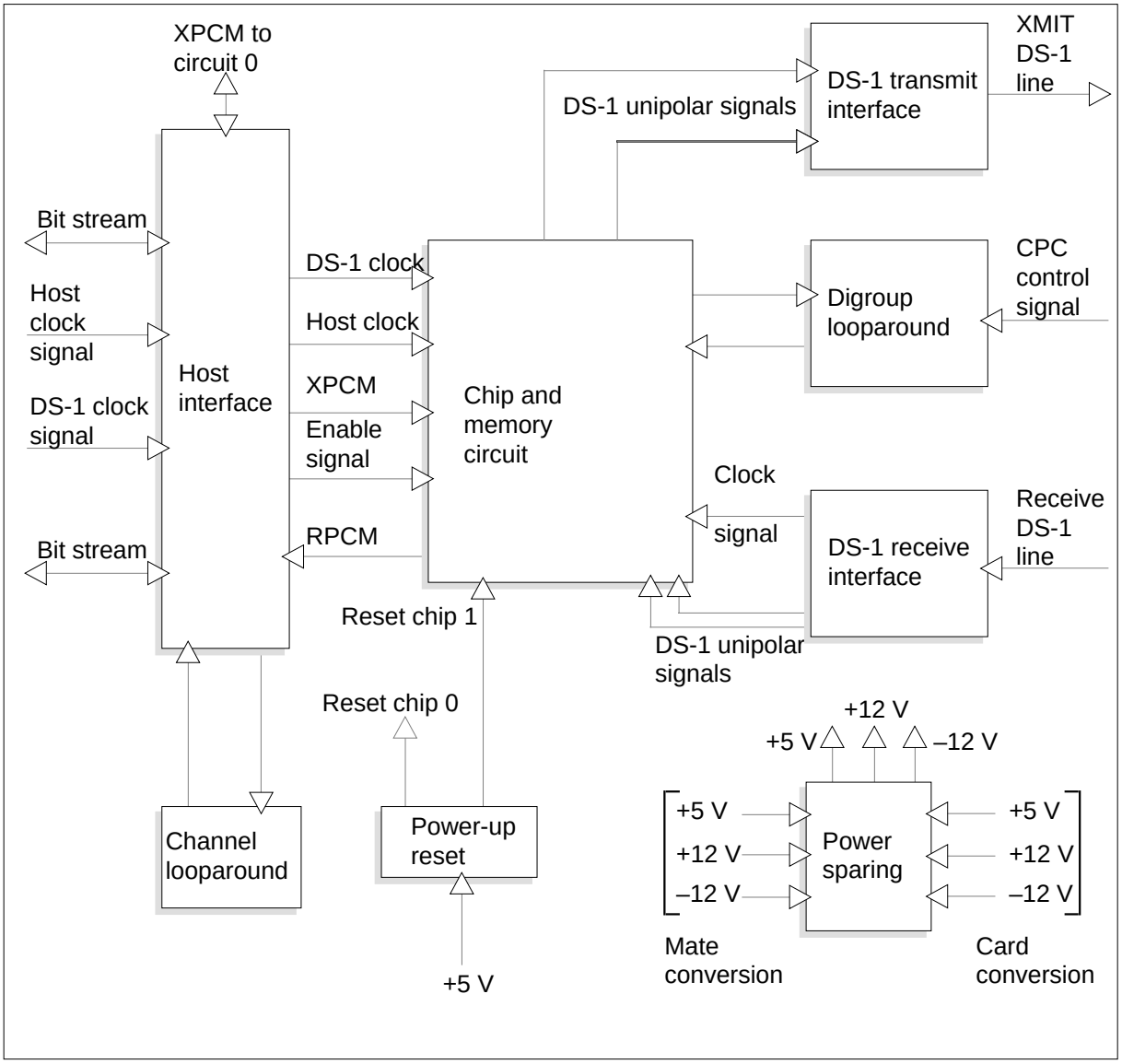
The NT6X50AA card has the following functional blocks:

- host interface
- chip and memory circuit
- DS-1 transmit interface
- DS-1 receive interface
- digroup looparound
- channel looparound
- power sparing
- power-up reset

The relationship between functional blocks in circuit 1 appears in the following figure. Circuit 0 operates by the same method.

NT6X50AA (continued)

NT6X50AA functional blocks



Host interface

The host interface receives two sets of 64-channel, 5.12-Mbps bit streams from the CPC shelf. One bit stream is active and one bit stream is inactive. The host interface demultiplexes each stream to two separate transmit-PCM (XPCM) bit streams. A host clock signal controls the XPCM bit streams. The host clock signal sends one XPCM bit stream to the chip and memory circuit. The host clock signal sends another bit stream to the chip and memory circuit in the mate circuit.

The host interface receives a DS-1 clock signal from the CPC shelf. The interface sends this signal to the chip and memory circuit. This transmission provides the timing required to send XPCM data to the DS-1 transmit interface.

The interface multiplexes receive-PCM (RPCM) data from the chip and memory circuit with the RPCM data from the mate circuit. The interface sends all this data to the CPC shelf. The host interface sends an enable signal to activate the associated DS-1 port. If the enable signal is inactive, the host interface disables the circuit and the port. The host interface places the circuit and the port in digroup looparound on all channels.

Chip and memory circuit

The chip and memory circuit stores signaling data present in the A and B bits of the DS-1 12-frame cycle. This circuit transmits the data in the RPCM stream at the required time. The circuit maps the 32 channels of the XPCM bit stream to the 24 channels of the DS-1 bit stream. The circuit uses non-PCM channels for control and signaling purposes.

The circuit retimes the 2.56-Mbps XPCM data to a 1.544-Mbps DS-1 transmit bit stream and the 1.544-Mbps DS-1 receive bit stream to 2.54-Mbps RPCM data.

DS-1 transmit interface

The DS-1 transmit interface receives two unipolar signals from the chip and memory circuit. This interface converts the signals to a bipolar DS-1 bit stream for transmission to the DS-1 port.

DS-1 receive interface

The DS-1 receive interface receives a bipolar signal from the DS-1 receive line. This interface converts the signal to two unipolar transistor-transistor logic (TTL) compatible signals. The circuit recovers a 1.544-MHz clock signal from the incoming bipolar signal. The circuit sends this clock signal to the chip and memory circuit to synchronize DS-1 functions.

Digroup looparound

The digroup looparound performs tests on all parts of the card except the DS-1 receive and transmit interfaces. The CPC control signal activates the CPC control signal. The circuit loops all 24 channels of the DS-1 bit stream from the transmit side to the receive side of the chip. The circuit loops the channels to the CPC.

NT6X50AA (continued)

Channel looparound

The channel looparound provides a path for diagnostic tests of the host interface. The circuit receives PCM data on channel 16 and sends data back to the host on channel 12.

Power sparing

The power sparing circuit connects to the two NT6X70 power converters in the CPC shelf. This connection makes sure card operation is reliable. A power failure can occur in the card. If this condition occurs, the power sparing circuit switches the card to the converter in the mate CPC shelf.

Power-up reset

The power-up reset circuit makes sure correct initialization of the chip occurs. This action occurs when you insert a chip. This action occurs when the CPC shelf is powered up. This circuit holds the reset line to the chip until a +5V power supply is stable.

Technical data

The card requires a 10.24-MHz system clock. The card has a multiframe pulse that occurs at intervals of 48 frames.

The card uses equalizer switch settings to balance the line impedance on cables of different lengths. The eight switches and the settings of the switches appears in the following table.

Equalizer switch settings

	Switch settings							
Cable length	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0 to 91 m (0 to 300 ft)	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
92 to 137 m (301 to 450 ft)	OFF	OFF	ON	OFF	OFF	ON	OFF	ON
138 to 228 m (451 to 750 ft)	ON	OFF	OFF	OFF	ON	OFF	ON	OFF

The DS-1 carrier interface characteristics appear in the following table.

DS-1 carrier interface characteristics (Sheet 1 of 2)

Characteristic	Value
Input rate	1.544 Mbps ±200 bps
Output rate	1.544 Mbps–phase locked to office clock
Structure	24 channels for each frame, 8 bits for each channel
Data format	Bits numbered 1 through 8, bit 1 sent first
Idle code setting	OFF ON ON ON ON ON ON ON
Channels	Numbered 1 through 24, channel 1 sent first
Ports	2 ports for each card, 1 and 0
Frame	193 bits for each frame
Superframe	193 bits plus 4 bits. The superframe is inserted before frame 1, frame 6, frame 12, and frame 18, and consists of 12 frames
Extended superframe	193 bits plus 4 bits. The extended superframe is inserted before frame 1, frame 6, frame 12, and frame 18, and consists of 24 frames
Signaling	A and B bits
Code	Bipolar
DS-1 receive input signal	±1.5 V to ±3 V
DS-1 transmitter	±6 output pulse height ±0.3-V positive-negative unbalance 324-ns half-amplitude width ±15-ns unbalance in width of positive-negative pulse 80-ns rise and fall time 20 to 40% overshoot at trailing edge Average minimum density, a minimum of 1 pulse in 8, a maximum of 15 consecutive zeros

NT6X50AA (continued)

DS-1 carrier interface characteristics (Sheet 2 of 2)

Characteristic	Value
Line impedance	100 Ω balanced
Transformer interwinding isolation	500 Vdc minimum

The host interface characteristics appear in the following table.

Host interface characteristics

Characteristic	Value
Rate	5.12 Mbps
Format	64 10-bit time slots numbered 9 through 0, bit 9 sent first
Polarity	Inverted DS-1 data, 0 on serial PCM equals 1 (3-V pulse) on DS-1
Multiplexing	The first half of the system clock cycle contains circuit 0 data. The second half contains the circuit 1 data.
Time slots	Numbered 0 through 31, time slot 0 transmitted first
Channel skew	T1IN data is advanced 37.5 bits at intervals of 390 ns for DSOUT data.

Dimensions

The dimensions of the NT6X50AA card are as follows:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 20 mm (0.78 in.)

Power requirements

The NT2X70 power converter provides the power requirements for the card. The power requirements appear in the following table.

Power requirements (Sheet 1 of 2)

Voltage	Current
+5 V	1 A

Power requirements (Sheet 2 of 2)

Voltage	Current
+12 V	100 mA
-12 V	5 mA

NT6X50AB

Product description

The NT6X50AB DS-1 extended frame format (EFF) card provides a two-way voice, data, and signaling interface. This interface is between the common peripheral controller (CPC) in the DMS-100 and one two-way port in standard DS-1 systems. The card contains two circuits that perform separately. These two circuits function the same method.

Location

The card plugs in one of five assigned slots in the NT6X02 CPC shelf or other shelves that use NT6X50 cards.

Functional description

The NT6X50AB receives and transmits data between the CPC shelf and the DS-1 ports. Clock signals control the card. The card converts unipolar data to bipolar data for transmission to the DS-1 ports. The card converts bipolar data to unipolar data for transmission to the CPC shelf.

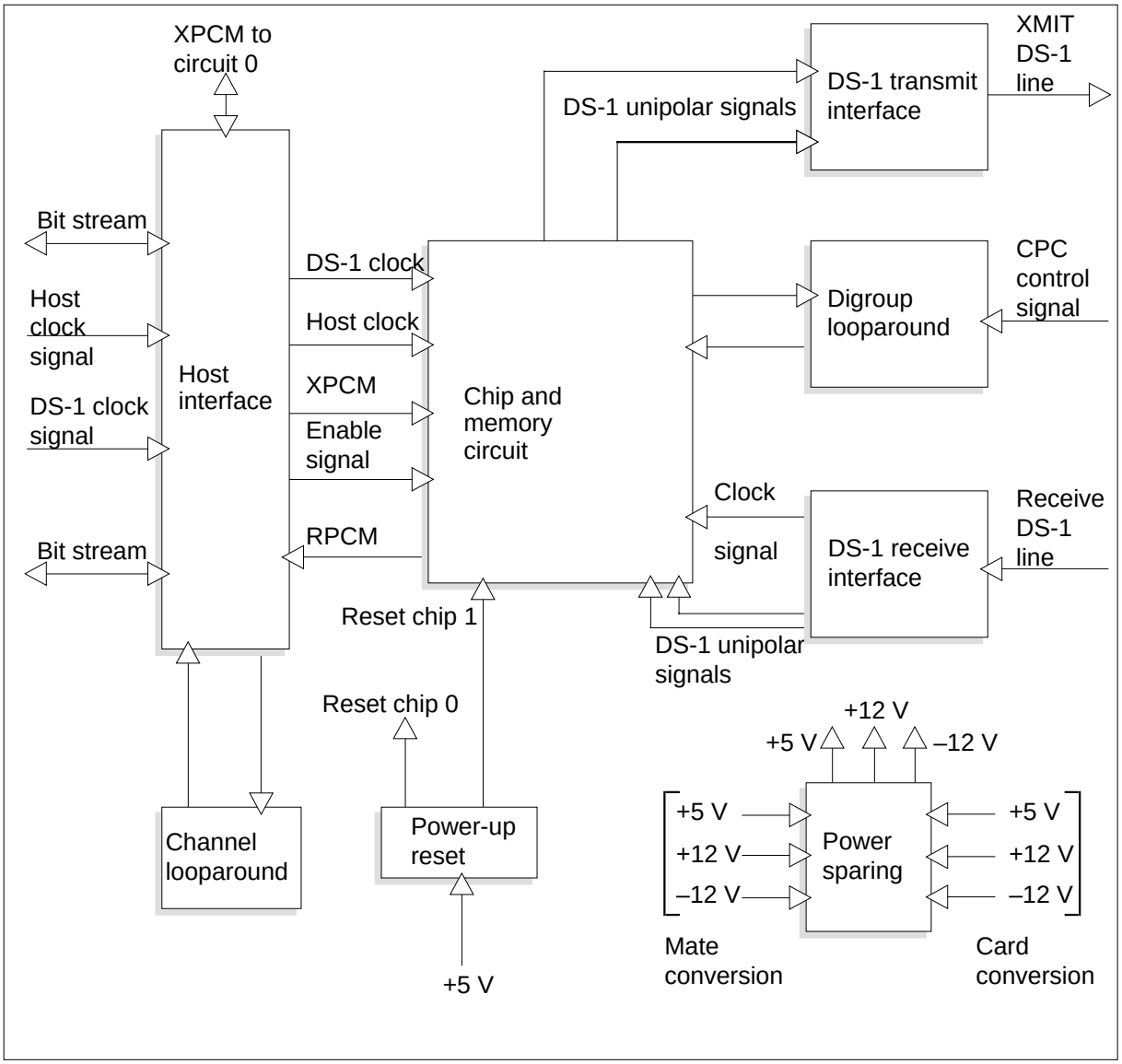
Functional blocks

The NT6X50AB has the following functional blocks:

- host interface
- chip and memory circuit
- DS-1 transmit interface
- DS-1 receive interface
- digroup looparound
- channel looparound
- power sparing
- power-up reset

The relationship between functional blocks in circuit 1 appears in the following figure. Circuit 0 operation is the same.

NT6X50AB functional blocks



Host interface

The host interface receives two sets of 64-channel, 5.12-Mbps bit streams from the CPC shelf. One bit stream is active and one bit stream is inactive. The host interface demultiplexes each stream in two separate transmit-PCM (XPCM) bit streams. One XPCM bit stream transfers to the chip and memory circuit. The other bit stream transfers to the chip and memory circuit in the mate circuit. A host clock signal controls this bit stream transfer.

NT6X50AB (continued)

The interface receives a DS-1 clock signal from the CPC shelf and sends this signal to the chip and memory circuit. This action provides timing to send XPCM data to the DS-1 transmit interface.

The interface multiplexes receive-PCM (RPCM) data from the chip and memory circuit with the RPCM data from the mate circuit. The interface sends this data to the CPC shelf. The host interface sends an enable signal to activate the associated DS-1 port. If the enable signal is inactive, the system disables the circuit and the port. The system places the circuit and port in digroup looparound on all channels.

Chip and memory circuit

The chip and memory circuit stores signaling data present in the A and B bits of the DS-1 12-frame cycle. The chip and memory circuit transmits the data to the RPCM stream at the appropriate time. The circuit maps the 32 channels of the XPCM bit stream to the 24 channels of the DS-1 bit stream. Channel 2 carries facility data link (FDL) information. The circuit uses non-PCM channels for control, signaling, and other purposes.

The circuit accesses A/B/C/D-bit signaling and supports zero code suppression (ZCS) and bipolar 8-bits zero suppression (B8ZS) coding. The circuit retimes the 2.56-Mbps XPCM data to a 1.544-Mbps DS-1 transmit bit stream. The circuit retimes the 1.544-Mbps DS-1 receive bit stream to 2.54-Mbps RPCM data.

DS-1 transmit interface

The DS-1 transmit interface receives two unipolar signals from the chip and memory circuit. The DS-1 transmit interface converts the signals to a bipolar DS-1 bit stream for transmission to the DS-1 port.

DS-1 receive interface

The DS-1 receive interface receives a bipolar signal from the DS-1 receive line. The DS-1 converts the signal to two unipolar transistor-transistor logic (TTL) compatible signals. The circuit recovers a 1.544-MHz clock signal from the incoming bipolar signal. The circuit sends this clock signal to the chip and memory circuit to synchronize DS-1 functions.

Digroup looparound

The digroup looparound performs tests on all card components except the DS-1 receive and transmit interfaces. The CPC control signal activates this circuit. The circuit loops all 24 channels of the DS-1 bit stream from the transmit side to the receive side of the chip. The circuit loops the channels to the CPC.

Channel looparound

The channel looparound provides a path for diagnostic tests of the host interface. The circuit receives PCM data on channel 16. The circuit sends data back to the host on channel 12.

Power sparing

The power sparing circuit in this card connects to the two NT2X70 power converters in the CPC. This connection makes sure that power for this card is available. A power failure can occur in the power converter supplying this card. If this condition occurs, the power sparing circuit switches this card to receive power from the other power converter which is located in the mate CPC unit.

Power-up reset

When you insert a chip or power up the CPC shelf, the power-up reset circuit holds the reset line to the chip until a +5 V power supply is stable. Action makes sure initialization of the chip is correct.

Technical data

The NT6X50AB requires a 10.24-MHz system clock. The card has a multiframe pulse that occurs at intervals of 48 frames. The card uses equalizer switch settings to balance the line impedance on cables that are different lengths.

The switch settings for 22 AWG DS-1 cable appear in the following table.

Switch settings for NT6X50AB for 24 AWG DS-1 (Sheet 1 of 2)

Card release and length of cables	Leave the switch contacts ON and leave all others OFF
NT6X50AB, release number 39 or lower	
0 m to 91 m (0 ft to 299 ft)	SW1
91 m to 137 m (299 ft to 449 ft)	SW2 SW5 SW7
137 m to 200 m (449 ft to 655 ft)	SW3 SW6 SW8
NT6X50AB, release numbers 40 to 59	
0 m to 91 m (0 ft to 299 ft)	SW4
91 m to 137 m (299 ft to 449 ft)	SW3 SW6 SW8
137 m to 200 m (449 ft to 655 ft)	SW1 SW5 SW7

NT6X50AB (continued)

Switch settings for NT6X50AB for 24 AWG DS-1 (Sheet 2 of 2)

Card release and length of cables	Leave the switch contacts ON and leave all others OFF
NT6X50AB, release numbers 60 or higher	
0 m to 41 m (0 ft to 133 ft)	SW1
41 m to 81 m (133 ft to 266 ft)	SW2 SW3
81 m to 122 m (266 ft to 399 ft)	SW2
122 m to 163 m (339 ft to 533 ft)	SW3
163 m to 200 m (533 ft to 655 ft)	None, all contacts are OFF

The following table lists the switch settings for 22 AWG DS-1 cable.

Switch settings for NT6X50AB for 22 AWG DS-1 cable

Card release and length of cables	Leave the switch contacts ON and leave all others OFF
NT6X50AB, release number 39 or lower	
0 m to 91 m (0 ft to 299 ft)	SW1
91 m to 137 m (299 ft to 449 ft)	SW2 SW5 SW7
137 m to 200 m (449 ft to 655 ft)	SW3 SW6 SW8
NT6X50AB, release numbers 40 to 59	
0 m to 91 m (0 ft to 299 ft)	SW4
91 m to 137 m (299 ft to 449 ft)	SW3 SW6 SW8
137 m to 200 m (449 ft to 655 ft)	SW1 SW5 SW7
NT6X50AB, release numbers 60 or higher	
0 m to 27 m (0 to 88.6 ft)	SW1
27 to 55 m (88.6 to 180.5 ft)	SW2 SW3
55 to 82 m (180.5 to 269 ft)	SW2
82 to 110 m (269 to 361 ft)	SW3
110 to 137 m (361 to 449.5 ft)	None, all contacts are OFF

The following table lists the DS-1 carrier interface characteristics.

DS-1 carrier interface characteristics

Characteristic	Value
Input rate	1.544-Mbps ±200 bps
Output rate	1.544-Mbps–phase locked to office clock
Structure	24 channels per frame, 8 bits per channel
Data format	Bits numbered 1 through 8, bit 1 sent first
Idle code setting	OFF ON ON ON ON ON ON ON
Channels	Numbered 1 through 24, channel 1 sent first
Ports	2 ports per card, 1 and 0
Frame	193 bits per frame
Superframe	193 bits plus 4 bits that are inserted before frame 1, frame 6, frame 12, and frame 18, consists of 12 frames
Extended superframe	193 bits plus 4 bits that are inserted before frame 1, frame 6, frame 12, and frame 18, consists of 24 frames
Signaling	A- and B-bits or A/B/C/D-bits (EFF)
Code	Bipolar
DS-1 receive input signal	±1.5 V to ±3 V
DS-1 transmitter	3 ± .6 V output pulse height ±0.3-V positive-negative unbalance 324-ns half-amplitude width ±15-ns unbalance in width of positive-negative pulse 80-ns rise and fall time 20 to 40% overshoot at trailing edge Average minimum density, not less than 1 pulse in 8, no more than 15 consecutive zeros
Line impedance	100 ohms balanced
Transformer interwinding isolation	500 Vdc minimum

NT6X50AB (end)

The following table lists host interface characteristics.

Host interface characteristics

Characteristic	Value
Rate	5.12 Mbps
Format	64 10-bit time slots numbered 9 through 0, bit 9 sent first
Polarity	Inverted DS-1 data, 0 on serial PCM equals 1 (3-V pulse) on DS-1
Multiplexing	Circuit 0 data is contained in the first half of the system clock cycle, circuit 1 data is contained in the second half
Time slots	Numbered 0 through 31, time slot 0 transmitted first
Channel skew	T1IN data is advanced 37.5 bits each 390 ns with respect to DSOUT data

Physical dimensions

The physical dimensions of the NT6X50AB card are as follows:

- overall height: 353 mm (13.9 in.)
- overall depth: 277 mm (10.9 in.)
- overall width: 20 mm (0.78 in.)

Power requirements

Power requirements for the card are received from the NT2X70 power converter and are shown in the following table.

Power requirements

Voltage	Current
+5 V	1 A
+12 V	100 mA
-12 V	5 mA

NT6X50EC

Product description

The integrated echo canceller card (NT6X50EC) incorporates echo cancellation capabilities on any number of DS1 links. This card provides the interface between two DS1 ports and one DS60 link in the digital trunk controller (DTC).

The NT6X50EC card supports extended super frame (ESF), binary 8 zero substitution (B8ZS), and all other features that the NT6X50AB card provides. The following conditions apply to the NT6X50EC:

- The NT6X50EC does not support inactive loopback function.
- The NT6X50EC performs remote loopback with a different method that requires software upgrade.

Location

The NT6X50EC card is in a DTE/DTEI frame. This frame requires near-end echo cancellation on a minimum of one DS1 trunks. Each of the four shelves in the DTE/DTEI frame can hold a maximum of five NT6X50EC cards.

Note: Nortel Networks does not support any 6X50EC cards in an AA frame.

A DTCI shelf in a DTEI frame normally has the NT6X50EC card. This DTEI frame has 48-V power provided for AB/AD frames.

Functional description

Functional blocks

The NT6X50EC card consists of the following functional blocks:

- DS1 interface
- DS60 interface
- control block
- digital signal processor (DSP)
- power circuitry block

DS1 interface

The DS1 interface block is the interface between a 1.544-Mbps serial DS1 link and a 2.56-Mbps DS30 serial speech bus. This speech bus is on the card. Each DS1 interface block handles the data in the transmit and receive directions of one bidirectional DS1 port.

NT6X50EC (continued)

DS60 interface

The DS60 interface block handles data transfers between the DS60 port and the two DS30 serial pulse code modulation (PCM) channels. The PCM channels are on the NT6X50EC card.

The DS60 interface performs the following functions:

- clock generation
- synchronization of incoming DS60 data
- multiplexing/demultiplexing of incoming and outgoing DS60 data
- inactive channel loopback
- activity steering

Control block

The control block controls the timing and flow of information between the DS60 interface, the DS1 interfaces, and the DSPs. This block supports the following:

- six DSPs
- two sets of DS1 interface control and status registers
- the DS60 active channel 12 to 16 loopback

DSP

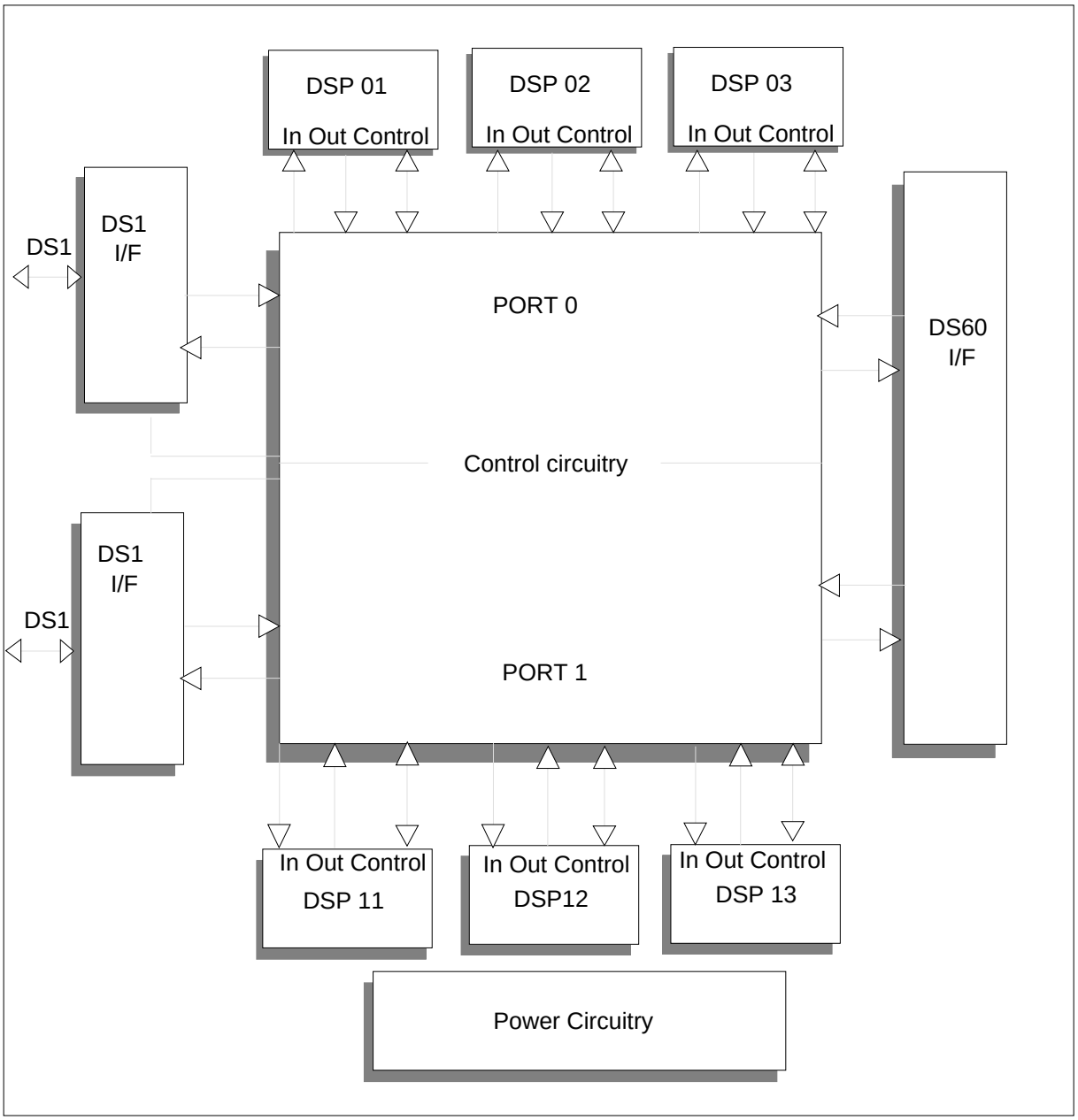
Each DSP block contains a high-speed Texas Instruments 320C25 processor. Three DSPs are present for each of the two DS30 ports. The DSPs perform echo cancellation processing of the 24 DS0 channels that each DS30 serial PCM channel carries.

Power circuit block

The power circuit block contains a DC-to-DC converter, the reset circuits, and two power supply monitors. The DC-to-DC converter converts 48 V to 5 V. This converter powers all six DSPs and the associated circuits. Without the 48 V power, the DSPs are isolated from the rest of the circuits and the card functions as an NT6X50AB card. The two exceptions, described in the product description of this document, apply when the 48V power is not present.

The relationship between the functional blocks appears in the following figure.

NT6X50EC functional blocks



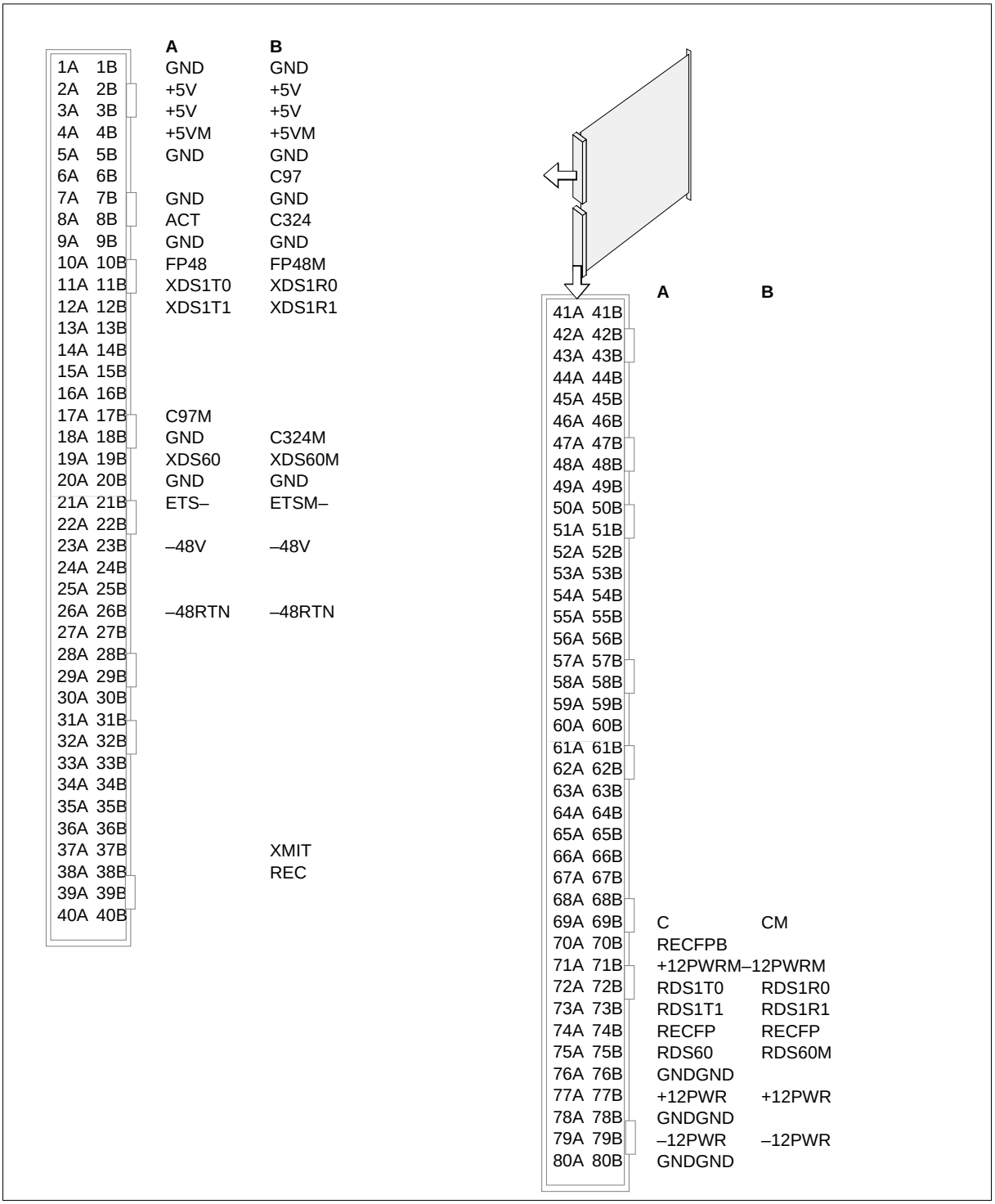
Signaling

Pin numbers

The pin numbers for the NT6X50EC appear in the following figure.

NT6X50EC (continued)

NT6X50EC pin numbers



Technical data

The NT6X50EC power requirements appear in the following table.

Power requirements

Voltage	Voltage and current combinations			
parameter	**Minimum**	**Nominal**	**Maximum**	**Condition**
+5V frame	4.75 V	5.00 V	5.25 V	V_{cc} = +5 V
		650 mA	950 mA	
+12V supply	11.00 V	12.00 V	13.00 V	V_{cc} = +5 V
		10 mA	25 mA	
-12V supply	-11.50 V	-12.00 V	-12.50 V	V_{cc} = +5 V
		5 mA	20 mA	
-48V supply	-42.50 V	-48.00 V	-55.60 V	V_{bb} = -48 V
		175 mA	400 mA	

Equalization switch settings

The NT6X50EC card has two equalization switches. The system sets the switches to default values when the installation of the card occurs. The equalization switches have labels S2 and S3 on the card. These two switches are 3-position dip switches. Datafill overwrites the default values with the values that appear in the following table.

Equalization switch settings for S2 and S3 (Sheet 1 of 2)

Cable length (feet)	Position setting 3	Position setting 2	Position setting 1
0-110	OFF	OFF	OFF
110-220	OFF	OFF	ON
220-330	OFF	ON	OFF
330-440	OFF	ON	ON
440-550	ON	OFF	OFF
550-650	ON	OFF	ON

NT6X50EC (end)

Equalization switch settings for S2 and S3 (Sheet 2 of 2)

Cable length (feet)	Position setting 3	Position setting 2	Position setting 1
Do not use*	ON	ON	OFF
Do not use*	ON	ON	ON

*The use of these settings can cause card failure.

Tone disable switch settings

A third dip switch is a 2-position dip switch. This switch has label S1 on the card. This switch sets the Tone Disable for Ports 0 and 1 for G.164 or G.165.

Tone disable switch settings for S1

Ports	Position setting	Description
0 & 1	ON	G.165
0 & 1	OFF	G.164

Note: Switch S1 must be set when use of the NT6X50EC card occurs in the EC or AB datafill modes in the switch data tables. The default setting for S1 position settings 1 and 2 is OFF.

NT6X51AB

Product description

The line concentrating module (LCM) processor functions as an interface between the line group controller (LGC) and the line drawers. The LCM is responsible for the following:

- processing associated with scanning bus interface cards (BIC), ringing control, and DMS-X messages
- background tasks for diagnostic purposes to protect the integrity of the LCM
- call processing and maintenance tasks to support 640 line cards

The extended LCM processor, NT6X51AB, increases processor memory from 64 Kbytes to 256 Kbytes and increases on-board diagnostics. Software features like custom local area signaling service (CLASS) Calling Number Display (CND), integrated services digital network (ISDN), and clear channel DS-1 capability require the NT6X51AB.

The NT6X51AB replaces the NT6X51AA, and can serve as a replacement card for in-service offices. The NT6X51AB is part of the NT6X04 LCM common circuit card fill. The NT6X51AA is in the following:

- the NT6X03 line concentrating equipment (LCE) frame
- the NT6X14 remote LCM (RLCM)
- the NT8X01 outside plant module (OPM) for BCS27 and greater.

The NT6X51AB is fully compatible to the NT6X51AA and previous releases. This compatibility includes backplane and interface. The NT6X51AB can connect to a NT6X51AA slot and execute software that runs in the NT6X51AA. The NT6X51AA does not execute software for the NT6X51AB correctly. The LCM firmware in the is not compatible with the NT6X51AA.

Functional description

The NT6X51AB is an 8085-based processor card for the LCM, RLCM, and OPM line peripherals. The NT6X51AB functions as an interface between the LGC and the line drawers. The NT6X51AA is responsible for processing with scanning BICs, ringing control, and DMS-X messages. The LCM processor performs call processing and maintenance tasks to support 640 line cards. The NT6X51AB is a modified version of the NT6X51AA that provides expanded random access memory (RAM). The memory is separated into program store and data store. Data store has one reserved bank of 64 Kbytes. The three banks of 64 Kbytes that remain are bank-switched program store. Common code has a section of reserved program store. The complete memory structure can be write-protected.

NT6X51AB (continued)

The increased memory that the NT6X51AB provides, supports the following features:

- bit error rate (BER) tests
- ringing generator maintenance
- emergency stand-alone (ESA) warm entry/exit
- clear channel DS-1 (NT6X50AB)
- the CLASS
- teen service (ringing)
- the ISDN

The NT6X03 LCE frame, the NT6X14 RLCM, and the NT8X01 OPM have the NT6X51AB installed. The circuit card needs keyslots in positions 3, 6, 10, and 11 of the frames. These positions are the same as the positions for the NT6X51AA.

Functional blocks

The NT6X51AB has the following functional blocks:

- central processing unit (CPU) interface that includes an 8085A microprocessor, EPROM, RAM, and associated circuits
- timing and control that include the following:
  - — the CPU control signals read (RD), write (WR), and ready (RDY)
  - — interrupts
  - — timers: sanity, 5 ms, and bus timeout (BTO)
  - — enables
  - — the 390-ns clock generation
- a 19 200-baud asynchronous link to the mate processor
- message interface that has a serial data link to each line drawer BIC

The NT6X51AB provides the following external interfaces:

- the NT6X52 digroup control card
- line drawer interface
- ring generator interface
- power converter interface
- the DMS-X messaging

The following paragraphs describe these external interfaces.

The NT6X52 digroup control card

The NT6X52 represents four blocks of memory to the NT6X51AB. As a result the following must interface with the NT6X52:

- the address and data bus
- the read, write, and ready signals
- the five address decode signals

Own and mate activity feeds to the NT6X52 for correct link control.

Line drawer interface

There are ten line drawers in the LCM. The NT6X51AB can communicate control information with each drawer. The receive control (RCON) signals are 20-bit serial data streams that transmit from the to the NT6X54 BIC card. The transmit control (TCON) signals are 20-bit serial data streams from the BIC cards to the .

The CPU writes the data field, the address field, and the status bits with the digroup number. The CPU writes this information to registers on the NT6X51AB. The CPU writes 22 bits. On the last write, a hardware sequencer begins to shift 20 bits to the drawer. The 4-bit digroup number selects the bits. The sequencer shifts 20 bits from the drawer, ready for the CPU to read. The system disables CPU access to the drawer interface circuits during shift operations. The CPU can communicate with only one drawer at a time.

There are ten status bits available for the CPU. The status bits indicate if a drawer has new data to read.

The NT6X51AB sends an activity signal to the BIC cards that indicates if the processor is currently processing calls.

Ring generator interface

There are six available status lines from each of the two ring generators in the LCM. The NT6X51AB does not send any signals to the ring generators. The LCM software does not have control over the operation of the ring generators.

Power converter interface

The NT6X53 power converter contains relays to switch around ringing and ANI/COIN voltages. The NT6X53 provides a current sense output to the .

NT6X51AB (continued)

The DMS-X messaging

The DMS-X message protocol accomplishes messaging to and from the central control (CC) and LGC.

There are two units in an LCM. Each unit operates separately to perform call processing and maintenance functions for the half of the line drawers the unit works. If one unit fails, the mate unit must take over call processing for the complete LCM. To handle this task, the two units must be able to communicate. A 19 200-baud serial link between the s on the two units facilitates communication. Activity status must transfer between the units.

Hardware description

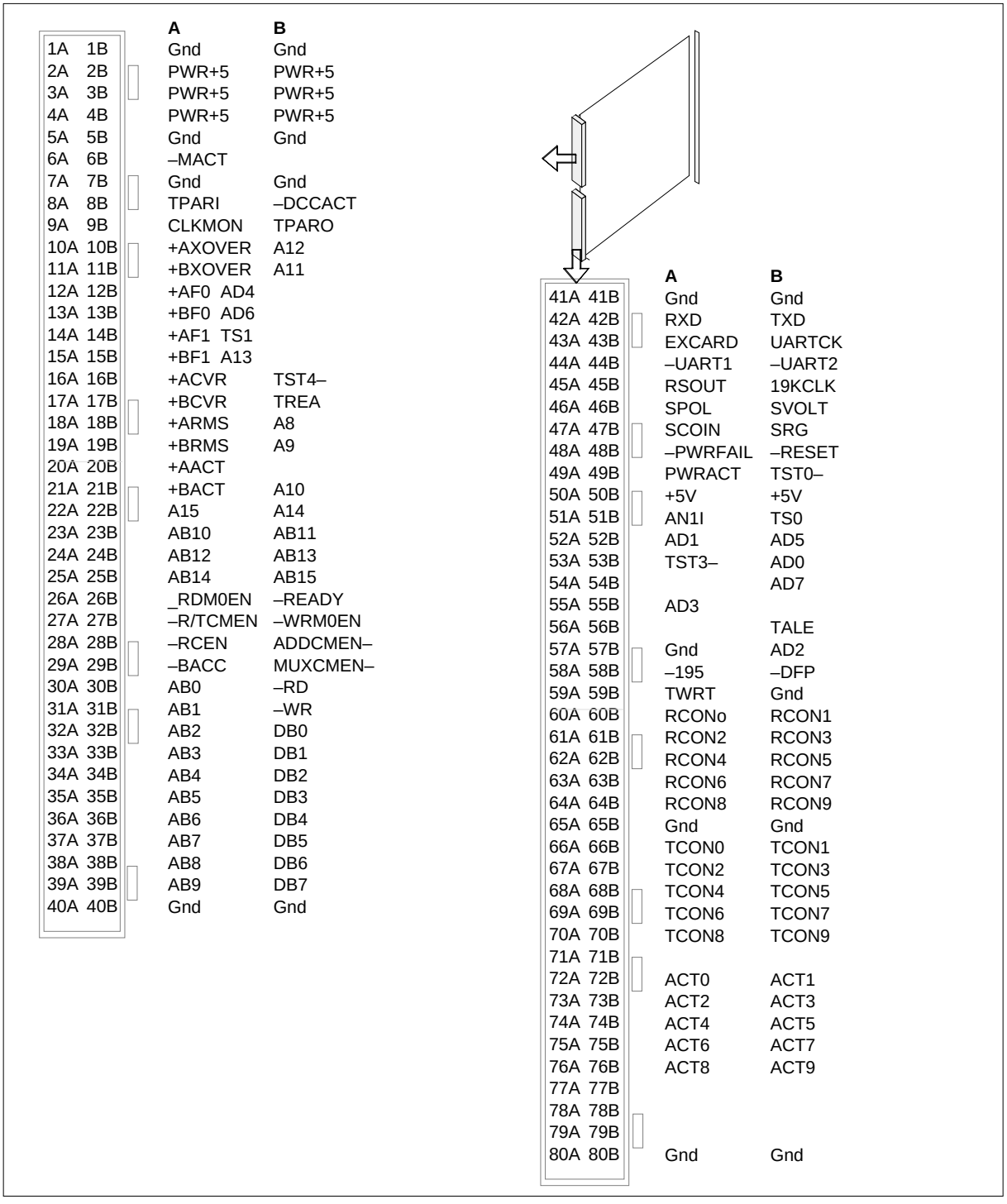
The NT6X51AB contains a microprocessor, RAM, ROM, and interface circuits that allow the NT6X51AB to control the activity of the LCM. The NT6X51AB operates based on instructions from the DMS-100 central control (CC) or the LGC. The NT6X51AB also operates on autonomous functions the NT6X51AB performs for maintenance or call processing tasks. The CPU is an 8085 microprocessor that runs at 6 MHz (12 MHz crystal). The NT6X51AB contains 32 Kbytes of erasable programmable read-only memory (EPROM) and 256 Kbytes of RAM.

Signaling

Pin numbers

The following figure describes the pin numbers for the NT6X51AB.

The NT6X51AB pin numbers



	A	B
1A 1B	Gnd	Gnd
2A 2B	PWR+5	PWR+5
3A 3B	PWR+5	PWR+5
4A 4B	PWR+5	PWR+5
5A 5B	Gnd	Gnd
6A 6B	–MACT	
7A 7B	Gnd	Gnd
8A 8B	TPARI	–DCCACT
9A 9B	CLKMON	TPARO
10A 10B	+AXOVER	A12
11A 11B	+BXOVER	A11
12A 12B	+AF0 AD4	
13A 13B	+BF0 AD6	
14A 14B	+AF1 TS1	
15A 15B	+BF1 A13	
16A 16B	+ACVR	TST4–
17A 17B	+BCVR	TREA
18A 18B	+ARMS	A8
19A 19B	+BRMS	A9
20A 20B	+AACT	
21A 21B	+BACT	A10
22A 22B	A15	A14
23A 23B	AB10	AB11
24A 24B	AB12	AB13
25A 25B	AB14	AB15
26A 26B	_RDM0EN	–READY
27A 27B	–R/TCMEN	–WRM0EN
28A 28B	–RCEN	ADDCMEN–
29A 29B	–BACC	MUXCMEN–
30A 30B	AB0	–RD
31A 31B	AB1	–WR
32A 32B	AB2	DB0
33A 33B	AB3	DB1
34A 34B	AB4	DB2
35A 35B	AB5	DB3
36A 36B	AB6	DB4
37A 37B	AB7	DB5
38A 38B	AB8	DB6
39A 39B	AB9	DB7
40A 40B	Gnd	Gnd

	A	B
41A 41B	Gnd	Gnd
42A 42B	RXD	TXD
43A 43B	EXCARD	UARTCK
44A 44B	–UART1	–UART2
45A 45B	RSOUT	19KCLK
46A 46B	SPOL	SVOLT
47A 47B	SCOIN	SRG
48A 48B	–PWRFAIL	–RESET
49A 49B	PWRACT	TST0–
50A 50B	+5V	+5V
51A 51B	AN1I	TS0
52A 52B	AD1	AD5
53A 53B	TST3–	AD0
54A 54B		AD7
55A 55B	AD3	
56A 56B		TALE
57A 57B	Gnd	AD2
58A 58B	–195	–DFP
59A 59B	TWRT	Gnd
60A 60B	RCONo	RCON1
61A 61B	RCON2	RCON3
62A 62B	RCON4	RCON5
63A 63B	RCON6	RCON7
64A 64B	RCON8	RCON9
65A 65B	Gnd	Gnd
66A 66B	TCON0	TCON1
67A 67B	TCON2	TCON3
68A 68B	TCON4	TCON5
69A 69B	TCON6	TCON7
70A 70B	TCON8	TCON9
71A 71B		
72A 72B	ACT0	ACT1
73A 73B	ACT2	ACT3
74A 74B	ACT4	ACT5
75A 75B	ACT6	ACT7
76A 76B	ACT8	ACT9
77A 77B		
78A 78B		
79A 79B		
80A 80B	Gnd	Gnd

NT6X51AB (end)

Technical data

Dimensions

The following are the dimensions for the NT6X51AB circuit card:

- height: 317.5 mm (12.5 in)
- depth: 254.0 mm (10.0 in)

Power requirements

The following are the power requirements for the NT6X51AB circuit card:

- voltage required: +5 V (±.25)
- current required: (normal) 3.0 A
- current required: (maximum) 4.6 A

NT6X51AC

Product description

The line concentrating module (LCM) processor functions as an interface between the line group controller (LGC) and the line drawers. The LCM is responsible for the following:

- processing associated with scanning bus interface cards (BIC), ringing control, and DMS-X messages
- background tasks for diagnostic purposes to protect the integrity of the LCM
- call processing and maintenance tasks to support 640 line cards

The NT6X51AC is the processor circuit pack of the LCM and is a new design of the extended LCM processor NT6X51AB. The NT6X51AC features faceplate LEDs to clearly indicate unit activity. The design incorporates most of the circuitry into surface mount technology to improve manufacturability. The NT6X51AC is software compatible back to the NT6X51AB, but not the NT6X51AA.

The NT6X51AB replaced the NT6X51AA, and can serve as a replacement card for in-service offices. The NT6X51AB is part of the NT6X04 LCM common circuit card fill. The NT6X51AA is in the following:

- the NT6X03 line concentrating equipment (LCE) frame
- the NT6X14 remote LCM (RLCM)
- the NT8X01 outside plant module (OPM) for BCS27 and greater.

The NT6X51AB is fully compatible to the NT6X51AA and previous releases. This compatibility includes backplane and interface. The NT6X51AB can connect to a NT6X51AA slot and execute software that runs in the NT6X51AA. The NT6X51AA does not execute software for the NT6X51AB correctly. The LCM firmware in the NT6X51AB is not compatible with the NT6X51AA.

Functional description

The NT6X51AC is an 8085A-based processor card for the LCM, RLCM, and OPM line peripherals. The NT6X51AC functions as an interface between the LGC and the line drawers. The NT6X51AC is responsible for processing with scanning BICs, ringing control, and DMS-X messages. The LCM processor performs call processing and maintenance tasks to support 640 line cards. The NT6X51AC provides expanded random access memory (RAM). The memory is separated into program store and data store. Data store has one reserved bank of 64 Kbytes. The three banks of 64 Kbytes that remain are bank-switched

NT6X51AC (continued)

program store. Common code has a section of reserved program store. The complete memory structure can be write-protected.

The NT6X51AC provides and supports the following features:

- bit error rate (BER) tests
- ringing generator maintenance
- emergency stand-alone (ESA) warm entry/exit
- clear channel DS-1 (NT6X50AB)
- the CLASS
- teen service (ringing)
- the ISDN

The NT6X03 LCE frame, the NT6X14 RLCM, and the NT8X01 OPM have the NT6X51AB installed. The circuit card needs keyslots in positions 3, 6, 10, and 11 of the frames. These positions are the same as the positions for the NT6X51AA.

Functional blocks

The NT6X51AC has the following functional blocks:

- central processing unit (CPU) interface that includes an 8085A microprocessor, EPROM, RAM, and associated circuits
- timing and control that include the following:
  - — the CPU control signals read (RD), write (WR), and ready (RDY)
  - — interrupts
  - — timers: sanity, 5 ms, and bus timeout (BTO)
  - — enables DMS-X message handling
  - — the 390-ns clock generation
- a 19,200-baud asynchronous link to the mate processor (IUC link)
- message interface that has a serial data link to each line drawer bus interface card (BIC)
- most circuitry implemented in surface mount packaging
- Hardware Watchdog Timer (not enabled)

  Note: Additional firmware changes are necessary to enable the H/W Watchdog.

- Inrush current conditioning
- additional filtering on the Activity and IUC Receive signals
- LED activity indicators

The NT6X51AC provides the following external interfaces:

- the NT6X52 digroup control card
- line drawer interface (NT6X54)
- ring generator interface
- power converter interface (NT6X53)
- the DMS-X messaging
- Inter-Unit communication (IUC, NT6X51)
- monitor card (Debug)

The following paragraphs describe these external interfaces.

The NT6X52 digroup control card

The NT6X52 represents four blocks of memory to the NT6X51AC. As a result the following must interface with the NT6X52:

- the address and data bus
- the read, write, and ready signals
- the five address decode signals
- Bus access enable
- Transmit timeswitch data enable
- 6X52 Clock monitor output

Own and mate activity feeds to the NT6X52 for correct link control.

Line drawer interface

There are ten line drawers in the LCM. The NT6X51AC can communicate control information with each drawer. The receive control (RCON) signals are 20-bit serial data streams that transmit from theNT6X51 to the NT6X54 BIC card. The transmit control (TCON) signals are 20-bit serial data streams from the BIC cards to the NT6X51.

The CPU writes the data field, the address field, and the status bits with the digroup number. The CPU writes this information to registers on the NT6X51AC. The CPU writes 22 bits. On the last write, a hardware sequencer begins to shift 20 bits to the drawer. The 4-bit digroup number selects the bits.

NT6X51AC (continued)

The sequencer shifts 20 bits from the drawer, ready for the CPU to read. The system disables CPU access to the drawer interface circuits during shift operations. The CPU can communicate with only one drawer at a time.

There are ten status bits available for the CPU. The status bits indicate if a drawer has new data to read.

The NT6X51AC sends an activity signal to the BIC cards that indicates if the processor is currently processing calls.

Ring generator interface

There are six available status lines from each of the two ring generators in the LCM. The NT6X51AC does not send any signals to the ring generators. The LCM software does not have control over the operation of the ring generators.

Power converter interface

The NT6X53 power converter contains relays to switch around ringing and ANI/COIN voltages. The NT6X53 provides a current sense output to the NT6X51.

The DMS-X messaging

The DMS-X message protocol accomplishes messaging to and from the central control (CC) and LGC.

Inter-Unit Communication

There are two units in an LCM. Each unit operates separately to perform call processing and maintenance functions for the half of the line drawers the unit works. If one unit fails, the mate unit must take over call processing for the complete LCM. To handle this task, the two units must be able to communicate. A 19,200-baud serial link between the NT6X51s on the two units facilitates communication. Activity status must transfer between the units.

Hardware description

The NT6X51AC contains a microprocessor, RAM, ROM, and interface circuits that allow the NT6X51AC to control the activity of the LCM. The NT6X51AC operates based on instructions from the DMS-100 central control (CC) or the LGC. The NT6X51AC also operates on autonomous functions the NT6X51AC performs for maintenance or call processing tasks. The CPU is an 8085A microprocessor that runs at 6 MHz (12 MHz crystal). The NT6X51AC contains 32 Kbytes of erasable programmable read-only memory (EPROM) and 256 Kbytes of RAM.

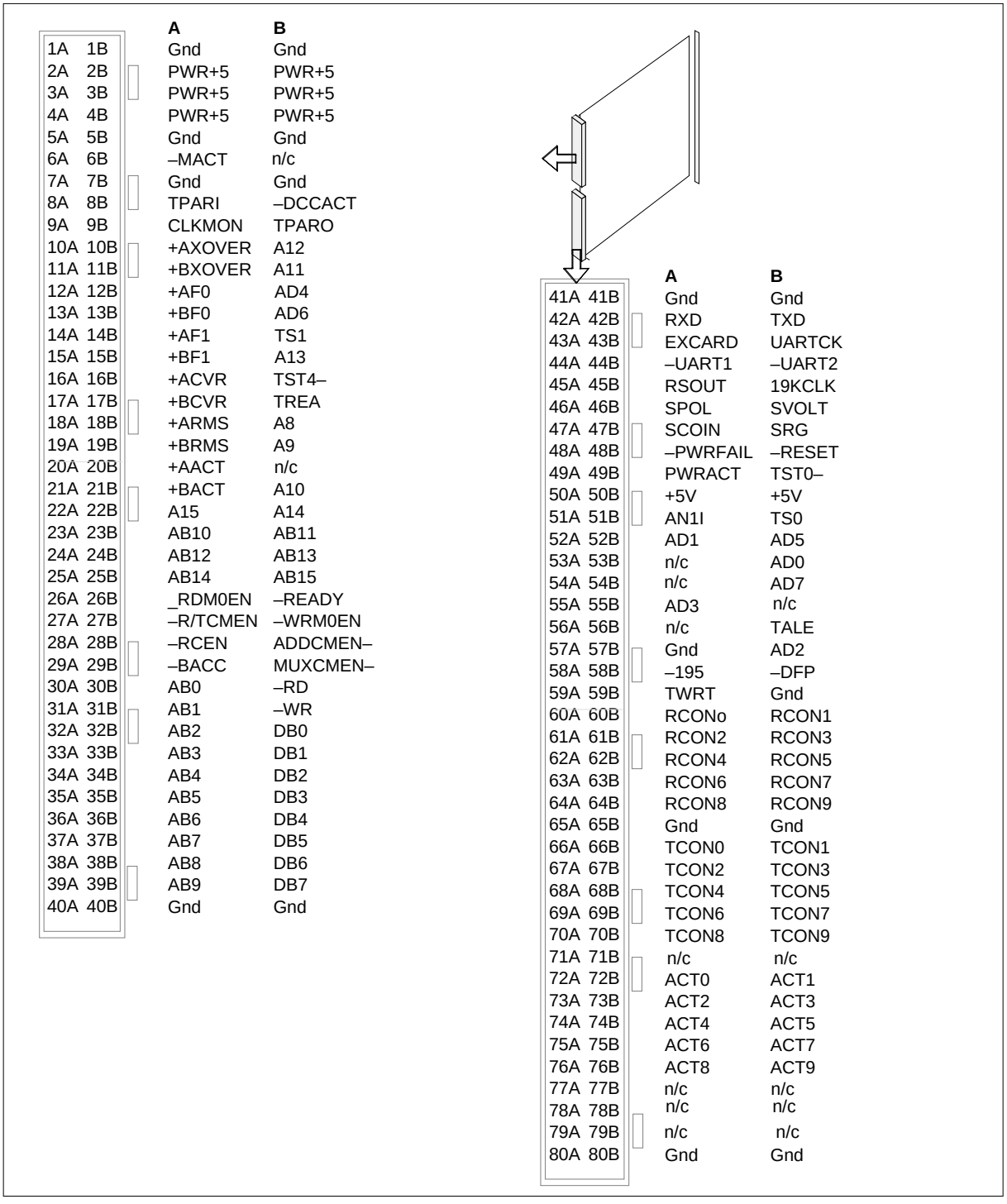
Signaling

Pin numbers

The following figure describes the pin numbers for the NT6X51AC.

NT6X51AC (continued)

The NT6X51AC pin numbers



	A	B
1A 1B	Gnd	Gnd
2A 2B	PWR+5	PWR+5
3A 3B	PWR+5	PWR+5
4A 4B	PWR+5	PWR+5
5A 5B	Gnd	Gnd
6A 6B	–MACT	n/c
7A 7B	Gnd	Gnd
8A 8B	TPARI	–DCCACT
9A 9B	CLKMON	TPARO
10A 10B	+AXOVER	A12
11A 11B	+BXOVER	A11
12A 12B	+AF0	AD4
13A 13B	+BF0	AD6
14A 14B	+AF1	TS1
15A 15B	+BF1	A13
16A 16B	+ACVR	TST4–
17A 17B	+BCVR	TREA
18A 18B	+ARMS	A8
19A 19B	+BRMS	A9
20A 20B	+AACT	n/c
21A 21B	+BACT	A10
22A 22B	A15	A14
23A 23B	AB10	AB11
24A 24B	AB12	AB13
25A 25B	AB14	AB15
26A 26B	_RDM0EN	–READY
27A 27B	–R/TCMEN	–WRM0EN
28A 28B	–RCEN	ADDCMEN–
29A 29B	–BACC	MUXCMEN–
30A 30B	AB0	–RD
31A 31B	AB1	–WR
32A 32B	AB2	DB0
33A 33B	AB3	DB1
34A 34B	AB4	DB2
35A 35B	AB5	DB3
36A 36B	AB6	DB4
37A 37B	AB7	DB5
38A 38B	AB8	DB6
39A 39B	AB9	DB7
40A 40B	Gnd	Gnd

	A	B
41A 41B	Gnd	Gnd
42A 42B	RXD	TXD
43A 43B	EXCARD	UARTCK
44A 44B	–UART1	–UART2
45A 45B	RSOUT	19KCLK
46A 46B	SPOL	SVOLT
47A 47B	SCOIN	SRG
48A 48B	–PWRFAIL	–RESET
49A 49B	PWRACT	TST0–
50A 50B	+5V	+5V
51A 51B	AN1I	TS0
52A 52B	AD1	AD5
53A 53B	n/c	AD0
54A 54B	n/c	AD7
55A 55B	AD3	n/c
56A 56B	n/c	TALE
57A 57B	Gnd	AD2
58A 58B	–195	–DFP
59A 59B	TWRT	Gnd
60A 60B	RCONo	RCON1
61A 61B	RCON2	RCON3
62A 62B	RCON4	RCON5
63A 63B	RCON6	RCON7
64A 64B	RCON8	RCON9
65A 65B	Gnd	Gnd
66A 66B	TCON0	TCON1
67A 67B	TCON2	TCON3
68A 68B	TCON4	TCON5
69A 69B	TCON6	TCON7
70A 70B	TCON8	TCON9
71A 71B	n/c	n/c
72A 72B	ACT0	ACT1
73A 73B	ACT2	ACT3
74A 74B	ACT4	ACT5
75A 75B	ACT6	ACT7
76A 76B	ACT8	ACT9
77A 77B	n/c	n/c
78A 78B	n/c	n/c
79A 79B	n/c	n/c
80A 80B	Gnd	Gnd

Technical data

Dimensions

The following are the dimensions for the NT6X51AC circuit card:

- height: 317.5 mm (12.5 in)
- depth: 254.0 mm (10.0 in)

Power requirements

The following are the power requirements for the NT6X51AC circuit card:

- voltage required: +5 V (±.25)
- current required: (normal) 3.0 A
- current required: (maximum) 4.6 A

NT6X51BA

Product description

The line concentrating module (LCM) processor contains three Motorola 68302 processors. These processors are the 68302 or the 68302 processor. The processors are in a tight coupled distributed process architecture. The Main Processor (MP) is responsible for operation of the LCM processor and the LCM. The second 68302 processor, C-side Processor (CP), is a front-end processor that terminates C-side messaging data. The data is in DMS-X or HDLC packet format. A second front-end processor or third 68302 processor, P-side processor (PP), operates the serial communication links. These links are between the NT6X51 pack and the bus interface card (BIC) packs in each line drawer of the LCM.

Under normal LCM operation, the LCM processors are active and load share to operate the LCM resources. Each LCM Processor has control of 50% of the line cards (320 of 640). The line cards are in units of 32 line cards called Line SubGroups (LSG). Each LSG is half of an NT6X05 line drawer. When one LCM processor or one digroup control card (DCC) pack fails, the mate LCM processor/DCC pair assumes control of all 640 lines in the LCM. The LCM continues operation in this failure state at a lower call traffic rate because of pulse code modulation (PCM) channel limitations at the line drawers. Each LCM processor performs background tasks for diagnostic purposes to make sure the LCM operates accurately.

The NT6X51BA is provisionable in LCMs packaged in line concentrating equipment (LCE) frames for host switch applications or remote LCM (RLCM) modules. The LCM processor functions are the same for both applications. The details of the frame equipment for the applications differ.

The NT6X51BA hardware is not compatible with the earlier generations of the NT6X51AA. Backward compatibility is not possible because of differences between the current generation of 68302 processors and the earlier Intel 8085. The software functionality does not allow operation of a hybrid configuration.

Functional description

The NT6X51BA is a 68302-based processor card for the LCM, RLCM, and outside plant module (OPM) line peripherals. The NT6X51BA is an interface between the LTC+ and the line drawers. The NT6X51BA is responsible for processing associated with scanning BICs, ringing control, and DMS-X messages. The LCM processor performs call processing and maintenance tasks to support 640 line cards.

The LCM processor has the following interfaces to other packs in the LCM:

- a parallel processor bus interface to the NT6X52 DCC pack
- a separate serial communications link (RCON/TCON) with the bus interface card (BIC) pack in each NT6X05 line drawer in the LCM
- separate control and status signals to the NT6X53 power supply pack. This interface defines the configuration of the ringing buses in the LCM
- ringing supply status signals from the two ring generators in the LCE frame
- a serial communication link, the Inter-Unit Communication (IUC) link, to the mate processor pack in the LCM
- pack activity status output signals to all other circuit packs in the LCM.

The LCM processor offers an integrated RS-232 serial port and faceplate light-emitting diodes (LED) to convey pack status. The RS-232 interface connector is on the pack faceplate and is for use as a VT-100 type monitor. The RS-232 interface connector allows Nortel Networks personnel to access the computer environment. The faceplate LEDs duplicate the LED functions on the NT6X51AC processor pack. The LEDs indicate if the LCM processor pack is active. The LEDs indicate if power is present in the pack.

The MP functions

The Main Processor (MP) is responsible for the operation of the NT6X51BA LCM processor. During normal operation, the MP controls all LCM resources except the C-side and P-side message termination logic. During failure or hardware diagnostics test conditions, the system permits the MP limited C-side and P-side message termination functionality.

The MP controls the following LCM resources:

- configuration of the ringing buses in the line drawers through a relay multiplexer on the NT6X53 power supply pack
- the BICs in line drawers, the ringing resource bus multiplex logic on the NT6X53 power supply, and the mate LCM processor
- all DCC connection memory, time-switch, and PCM channel test resources
- the IUC link to the mate processor pack and the access debug port

NT6X51BA (continued)

The following functional elements are in the MP circuit:

- a 68302 processor. The 68302 processor incorporates three serial port controllers, three timers, a DMS controller, and different processor resources
- a 4-Mbyte dynamic RAM (DRAM) bank
- two banks of flash read-only memory (ROM), 4 Mbytes each, with hardware control logic to determine the active and spare banks
- logic to monitor bus accesses for not permitted operations and generate a bus error interrupt to the 68302 processor
- logic to monitor bus accesses in specified 256 byte sectors of memory and generate a nonmaskable interrupt to the 68302 processor
- interface control register and buffers to implement the ringing resource and activity signal functions in the LCM
- a bus interface to the DCC circuit pack
- bus interfaces into the CP and PP circuits

The MP can force the CP or PP to hardware reset to take over the processor resources of the CP or PP. When the front end processor is in reset, the MP can configure the operating environment of the front end processor completely.

The CP functions

The C-side Processor (CP) terminates or sources message packets from the DMS core that C-side message links carry. One processor bus interface on the DCC pack requires the MP to share access with the CP. The CP uses the hardware state machine of the CP to take bus cycles from the MP every frame. The CP takes bus cycles from the MP in order to retrieve C-side message bytes from the DCC.

The CP communicates messages with the MP and the PP. The CP communicates messages with the MP. To communicate with the MP the CP allows the MP to use DMS accesses to retrieve message packets. The packets that the MP retrieves are from the CP memory area. The system sends messages between the CP and PP through a serial link. The serial link interfaces at the CP processor.

The CP provides the following memory resources:

- a 256 Kbyte static RAM (S-RAM) area split between read-only and read-write sectors. The MP control logic controls the split when the CP is in hardware reset.
- logic to monitor bus accesses for not permitted operations and generate a bus error interrupt to the 68302
- logic to monitor bus accesses in specified 256 Kbyte sectors of memory and generate a nonmaskable interrupt to the 68302

The MP configures the code and global data sections of the CP memory before the system releases CP from reset to operate. This action cannot occur while the CP operates.

The PP functions

The P-side Processor (PP) terminates or sources message packets from the line drawer BIC circuits. The RCON/TCON carries these serial message links.

The PP communicates messages with the MP and the CP. To communicate messages with the MP, the PP allows the MP to use DMS accesses to retrieve message packets. The MP retrieves message packets from the PP memory area. Communication of messages between the CP and PP occurs through a serial link. The serial link interfaces at the PP processor.

The PP provides the following memory resources:

- a 256 Kbyte S-RAM area split between read-only and read-write sectors. The MP control logic controls the split when the CP is in hardware reset.
- logic to monitor bus accesses for not permitted operations and generate a bus error interrupt to the 68302
- logic to monitor bus accesses in specified 256 Kbyte sectors of memory and generate a nonmaskable interrupt to the 68302

The MP configures the code and global data sections of the PP memory before the system releases PP from reset to operate. This action cannot occur while the PP operates.

Other functions

Two hardware control functions on the LCM processor do not map to one of the three processor circuits. These functions are the 5V power input circuit and the C-side clock interface to the NT6X52 DCC pack. These two circuits provide hardware control logic for the complete NT6X51BA.

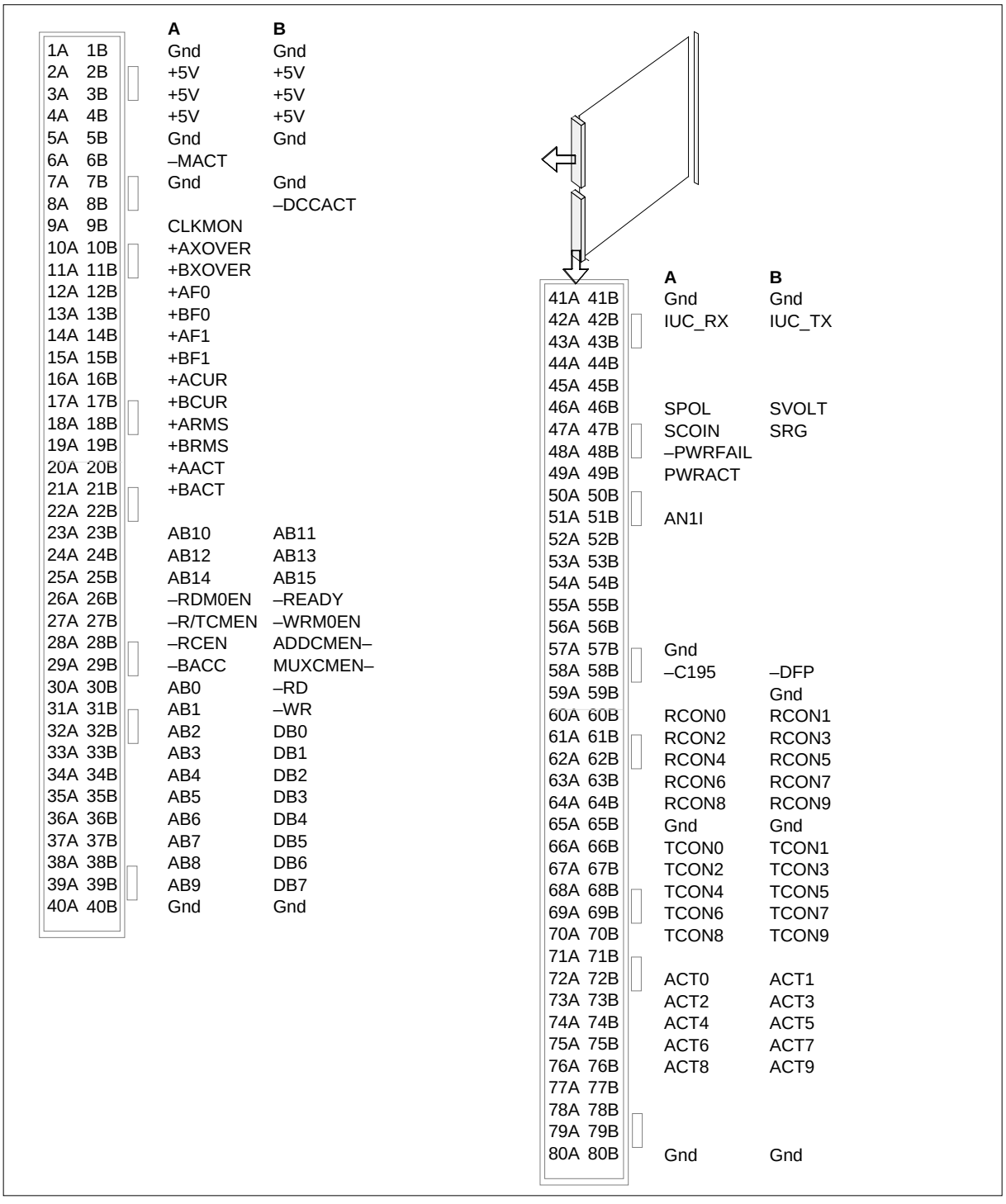
NT6X51BA (continued)

Signaling

Pin numbers

The pin numbers for the NT6X51BA appear in the following figure.

The NT6X51BA pin numbers



	A	B
1A 1B	Gnd	Gnd
2A 2B	+5V	+5V
3A 3B	+5V	+5V
4A 4B	+5V	+5V
5A 5B	Gnd	Gnd
6A 6B	–MACT	
7A 7B	Gnd	Gnd
8A 8B		–DCCACT
9A 9B	CLKMON	
10A 10B	+AXOVER	
11A 11B	+BXOVER	
12A 12B	+AF0	
13A 13B	+BF0	
14A 14B	+AF1	
15A 15B	+BF1	
16A 16B	+ACUR	
17A 17B	+BCUR	
18A 18B	+ARMS	
19A 19B	+BRMS	
20A 20B	+AACT	
21A 21B	+BACT	
22A 22B		
23A 23B	AB10	AB11
24A 24B	AB12	AB13
25A 25B	AB14	AB15
26A 26B	–RDM0EN	–READY
27A 27B	–R/TCMEN	–WRM0EN
28A 28B	–RCEN	ADDCMEN–
29A 29B	–BACC	MUXCMEN–
30A 30B	AB0	–RD
31A 31B	AB1	–WR
32A 32B	AB2	DB0
33A 33B	AB3	DB1
34A 34B	AB4	DB2
35A 35B	AB5	DB3
36A 36B	AB6	DB4
37A 37B	AB7	DB5
38A 38B	AB8	DB6
39A 39B	AB9	DB7
40A 40B	Gnd	Gnd

	A	B
41A 41B	Gnd	Gnd
42A 42B	IUC_RX	IUC_TX
43A 43B		
44A 44B		
45A 45B		
46A 46B	SPOL	SVOLT
47A 47B	SCOIN	SRG
48A 48B	–PWRFAIL	
49A 49B	PWRACT	
50A 50B		
51A 51B	AN1I	
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B	Gnd	
58A 58B	–C195	–DFP
59A 59B		Gnd
60A 60B	RCON0	RCON1
61A 61B	RCON2	RCON3
62A 62B	RCON4	RCON5
63A 63B	RCON6	RCON7
64A 64B	RCON8	RCON9
65A 65B	Gnd	Gnd
66A 66B	TCON0	TCON1
67A 67B	TCON2	TCON3
68A 68B	TCON4	TCON5
69A 69B	TCON6	TCON7
70A 70B	TCON8	TCON9
71A 71B		
72A 72B	ACT0	ACT1
73A 73B	ACT2	ACT3
74A 74B	ACT4	ACT5
75A 75B	ACT6	ACT7
76A 76B	ACT8	ACT9
77A 77B		
78A 78B		
79A 79B		
80A 80B	Gnd	Gnd

NT6X51BA (end)

Technical data

Dimensions

The following are the dimensions for the NT6X51BA circuit card:

- height: 317.5 mm (12.5 in)
- depth: 254.0 mm (10.0 in)

Power requirements

The following are the power requirements for the NT6X51BA circuit card:

- voltage required: +5 V (±.25)
- current required: (normal) 3.0 A
- current required: (maximum) 4.6 A

NT6X52AA

Product description

The lNT6X52AA ine concentrating module (LCM) digroup control card (DCC) performs pulse code modulation (PCM) time switching functions. The NT6X52AA card performs this function for 320 or 640 subscriber lines. The number of line depends on the state of the mate LCM unit.

The NT6X52AA allows PCM data to loop back for diagnostic purposes. The NT6X52AA allows the insertion of special codes, like ring enable, in the PCM path.

The NT6X52AA card is the North American version of the 6X52.

Functional description

The LCM processor card and separate control logic control the NT6X52AAcard. The NT6X52AA card contains an application-specific integrated circuit (ASIC) with a plain old telephone service (POTS) digroup controller chip (N11). The ASIC is responsible for most of the functionality of the card. The ASIC allows the card to perform the time switching functions of the LCM. The card performs switching functions for PCM speech data, between the line drawers and the peripheral modules (PM).

The NT6X52AA has control logic, and interface circuits. The link arbitration circuit is external to the ASIC. This circuit allows the output of the PCM links to flow back to the PMs. This circuit makes sure that the LCM unit and the mate LCM unit use the correct links.

Functional blocks

The NT6X52AA has the following functional blocks:

- receive time switch (RTS)
- transmit time switch (TTS)
- connection memories
- timing and control
- test register
- looparound circuit
- message buffers
- the LCM processor interface
- formatter

NT6X52AA (continued)

The RTS

The RTS is a memory array inside the N11 ASIC. The RTS receives incoming PCM data from the central processor-side (C-side) ports. Each memory location is for a channel on one of the eight incoming C-side ports. The system automatically loads data to the receive time switch memory location. The timing and control block controls the data load. The data load occurs during the second half of the 390-ns clock cycle.

The connection memory reads the PCM data from the receive time switch. The connection memory reads the PCM data during the first half of the 390 ns clock cycle. The system routes the PCM data to a peripheral module-side (P-side) port and channel. The address in the connection memory block controls this action.

The TTS

The TTS is a memory array inside the N11 ASIC that receives incoming P-side PCM data. Each memory location is for a specified channel on one of the eight outgoing C-side ports. The timing and control block automatically reads data from the transmit time switch. The system routes the data to a channel on a C-side port.

Connection memories

There are two different connection memories in the N11 ASIC. The connection memories are: receive/transmit time switch connection memory and the receive/transmit multiplex connection memory.

The receive/transmit time switch connection memory (RTTSCM) is an 8-bit memory array. In the RTTSCM each location represents a channel on one of the P-side ports in the receive or transmit direction. The RTTSCM stores the address of the location in the receive/transmit time switch. This address represents a channel and a port on the C-side. The RTTSCM facilitates a PCM path between any P-side port and channel, and a C-side port and channel.

The receive/transmit multiplex connection memory (RTMCM) is a four-bit memory array that stores data to control the two multiplexers. The two multiplexers are between the two time switches (transmit and receive) and the P-side ports.

Timing and control

The N11 ASIC has two counters that control the flow of PCM data through the chip. One counter is a count-to-320 timer that addresses the connection memories and a timing control read-only memory (ROM).

The other counter is a count-to-256 timer that produces the automatically controlled address for the two time switches.

Test register

The LCM processor writes to the test register when the system routes data by one of the following:

- through the looparound circuit for diagnostics
- to a specified outgoing channel for external communications.

Looparound circuit

A set of RAM cells functions as the looparound buffer in the N11 ASIC. The system routes the PCM data of every channel to this buffer from every outgoing P-side port. The system realigns this data between the transmit and receive paths on the P-side ports and channels by the offset. The offset is between the timing and control count-to-320 counter and another separate count-to-320 counter.

Message buffers

There are two message buffers in the N11 ASIC. The two mesage buffers are one write-only buffer, and one read-only buffer. The timing and control block can read from the write-only buffer. The timing and control block can write to the read-only buffer. The LCM processor uses these buffers for communication to the controlling node in the DMS system.

The LCM processor interface

The LCM processor interface, inside the N11 ASIC, controls the bus timing to the 6X51 LCM processor card. This interface allows the processor access to the connection memories. This interface allows the processor to read from the transmit time switch.

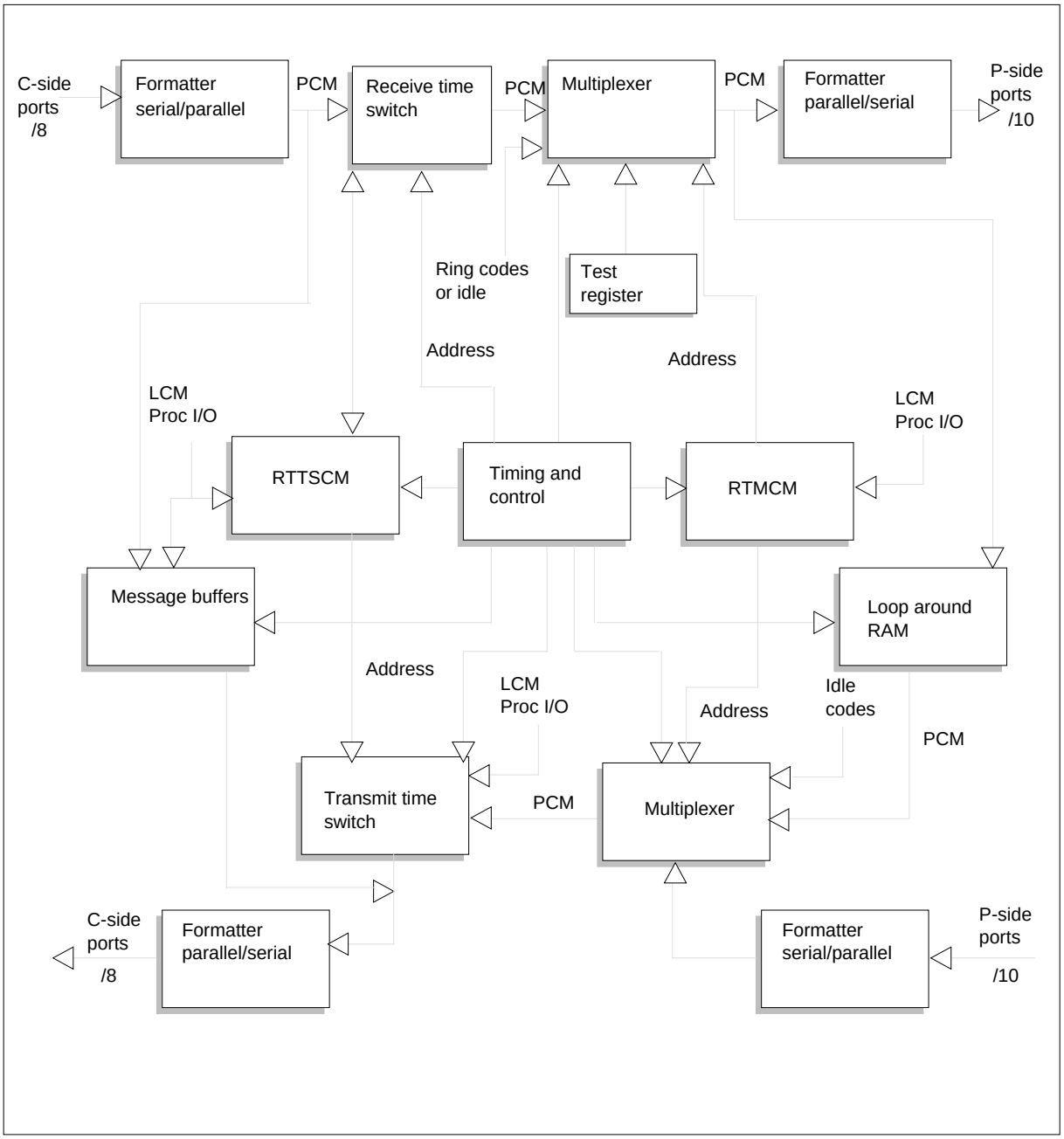
Formatter

The formatter, inside the N11 ASIC, converts all incoming serial transmission data to a parallel format. The formatter converts and all outgoing data back to a serial format before transmission to the ports.

The following figure describes the relationship between these functional blocks.

NT6X52AA (continued)

The NT6X52AA (N11 ASIC) functional blocks



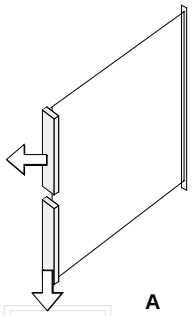
Signaling

Pin numbers

The pin numbers for the NT6X52AA appear in the following figure.

The NT6X52AA pin numbers

	A	B
1A 1B	GND	GND
2A 2B	+5V	+5V
3A 3B	+5V	+5V
4A 4B	+5V	+5V
5A 5B	GND	GND
6A 6B		
7A 7B	GND	CH0–
8A 8B	CLKMON	ACT–
9A 9B	MCH0–	MACT–
10A 10B	PCLK0+	PCLK0+
11A 11B	PFP0+	PFP0–
12A 12B	PRPCM0+	PRPCM0–
13A 13B	PRPCM1+	PRPCM1–
14A 14B	RPCM2+	RPCM2–
15A 15B	RPCM3+	RPCM3–
16A 16B	RPCM4+	RPCM4–
17A 17B	RPCM5+	RPCM5–
18A 18B	RPCM6+	RPCM6–
19A 19B	XPCM0+	XPCM0–
20A 20B	XPCM1+	XPCM1–
21A 21B	XPCM2+	XPCM2–
22A 22B	XPCM3+	XPCM3–
23A 23B	XPCM4+	XPCM4–
24A 24B	XPCM5+	XPCM5–
25A 25B	XPCM6+	XPCM6–
26A 26B	RMSGOEN	RDY–
27A 27B	EN3–	WMSGOEN
28A 28B	RCEN–	EN1–
29A 29B	–BACC	EN2–
30A 30B	A0	RD–
31A 31B	A1	WR–
32A 32B	A2	D0
33A 33B	A3	D1
34A 34B	A4	D2
35A 35B	A5	D3
36A 36B	A6	D4
37A 37B	A7	D5
38A 38B	A8	D6
39A 39B	A9	D7
40A 40B	GND	GND



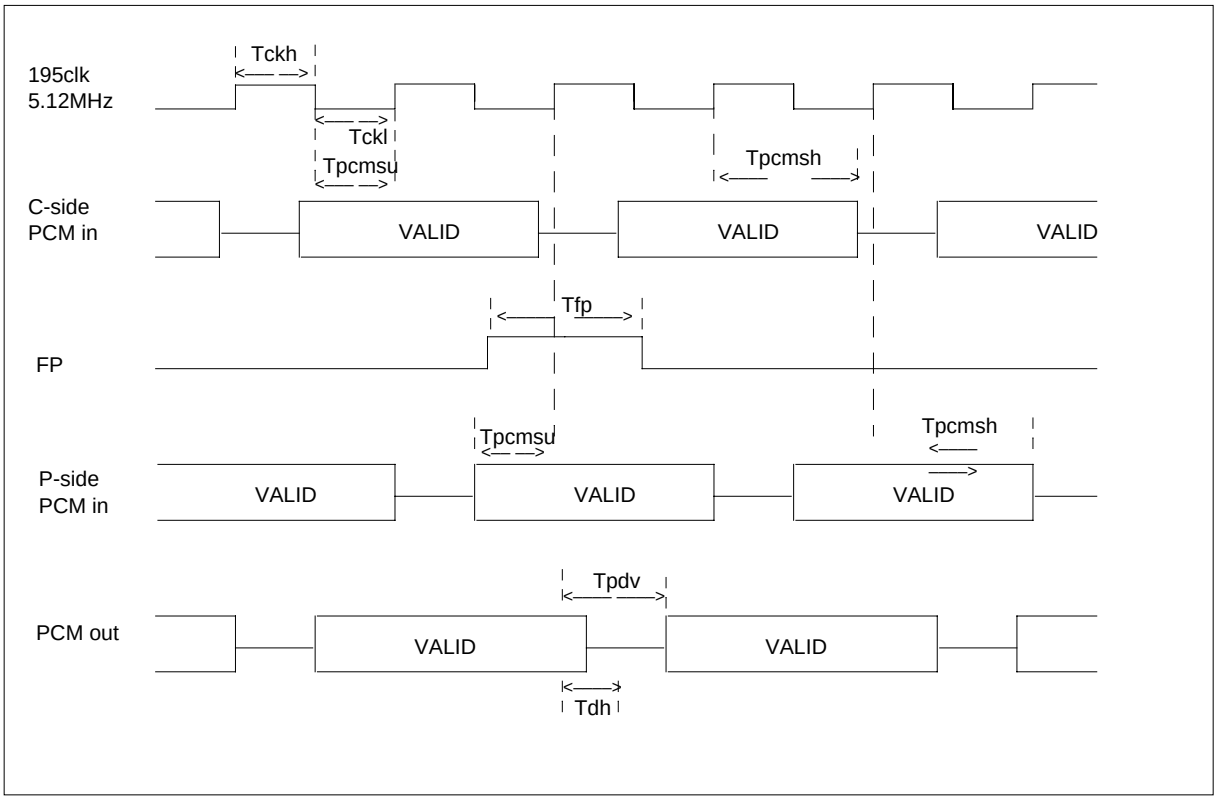
	A	B
41A 41B	GND	GND
42A 42B	RPCM7+	RPCM7–
43A 43B	XPCM7+	XPCM7–
44A 44B		
45A 45B		
46A 46B		
47A 47B	RD0	RD1
48A 48B	RD2	RD3
49A 49B	RD4	RD5
50A 50B	RD6	RD7
51A 51B	RD8	RD9
52A 52B	TD0	TD1
53A 53B	TD2	TD3
54A 54B	TD4	TD5
55A 55B	TD6	TD7
56A 56B	TD8	TD9
57A 57B		SYNC
58A 58B	–195	DFP–
59A 59B		GND
60A 60B	DCLK0+	DCLK0–
61A 61B	DCLK1+	DCLK1–
62A 62B	DCLK2+	DCLK2–
63A 63B	DCLK3+	DCLK3–
64A 64B	DCLK4+	DCLK4–
65A 65B	DCLK5+	DCLK5–
66A 66B	DCLK6+	DCLK6–
67A 67B	DCLK7+	DCLK7–
68A 68B	DCLK8+	DCLK8–
69A 69B	DCLK9+	DCLK9–
70A 70B	DFP0+	DFP0–
71A 71B	DFP1+	DFP1–
72A 72B	DFP2+	DFP2–
73A 73B	DFP3+	DFP3–
74A 74B	DFP4+	DFP4–
75A 75B	DFP5+	DFP5–
76A 76B	DFP6+	DFP6–
77A 77B	DFP7+	DFP7–
78A 78B	DFP8+	DFP8–
79A 79B	DFP9+	DFP9–
80A 80B	GND	GND

NT6X52AA (continued)

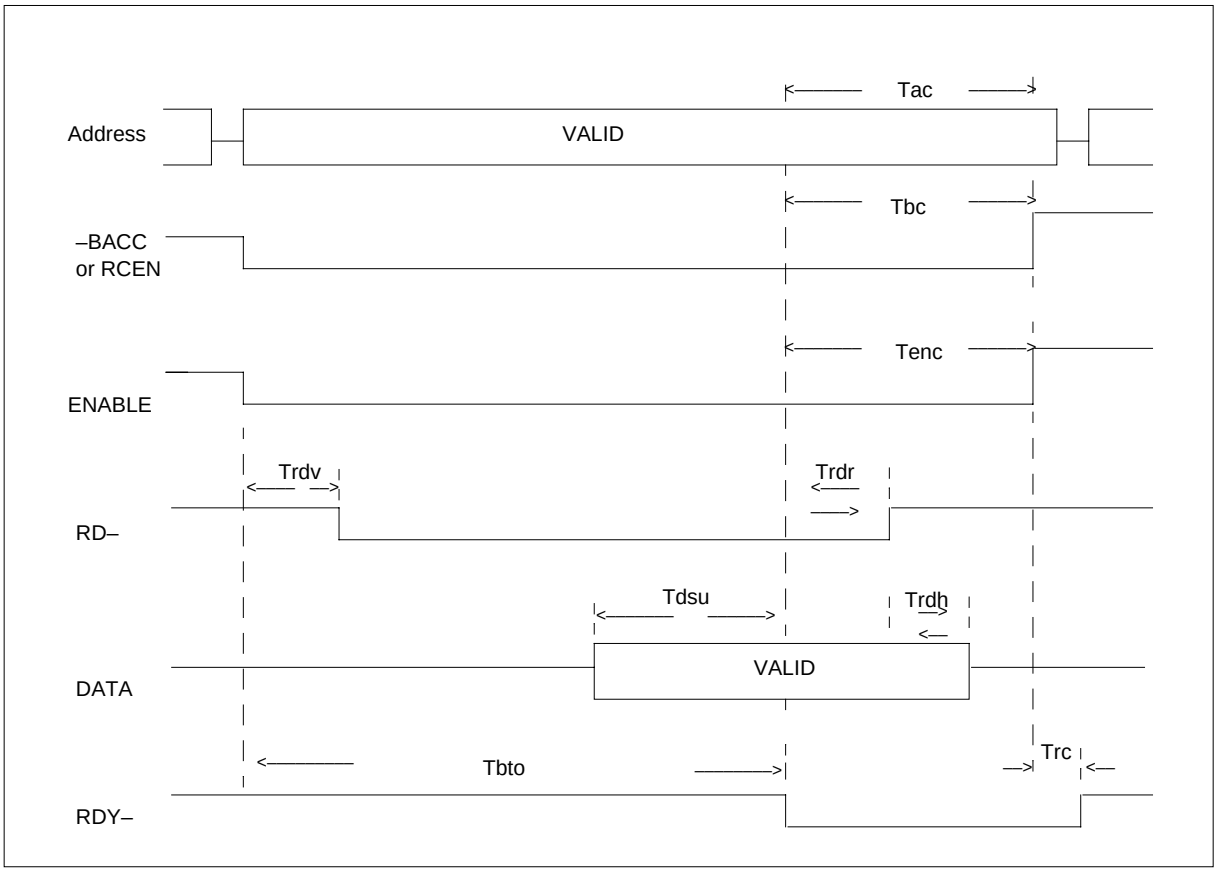
Timing

The following figures describe the timing for the NT6X52AA.

The NT6X52AA PCM timing

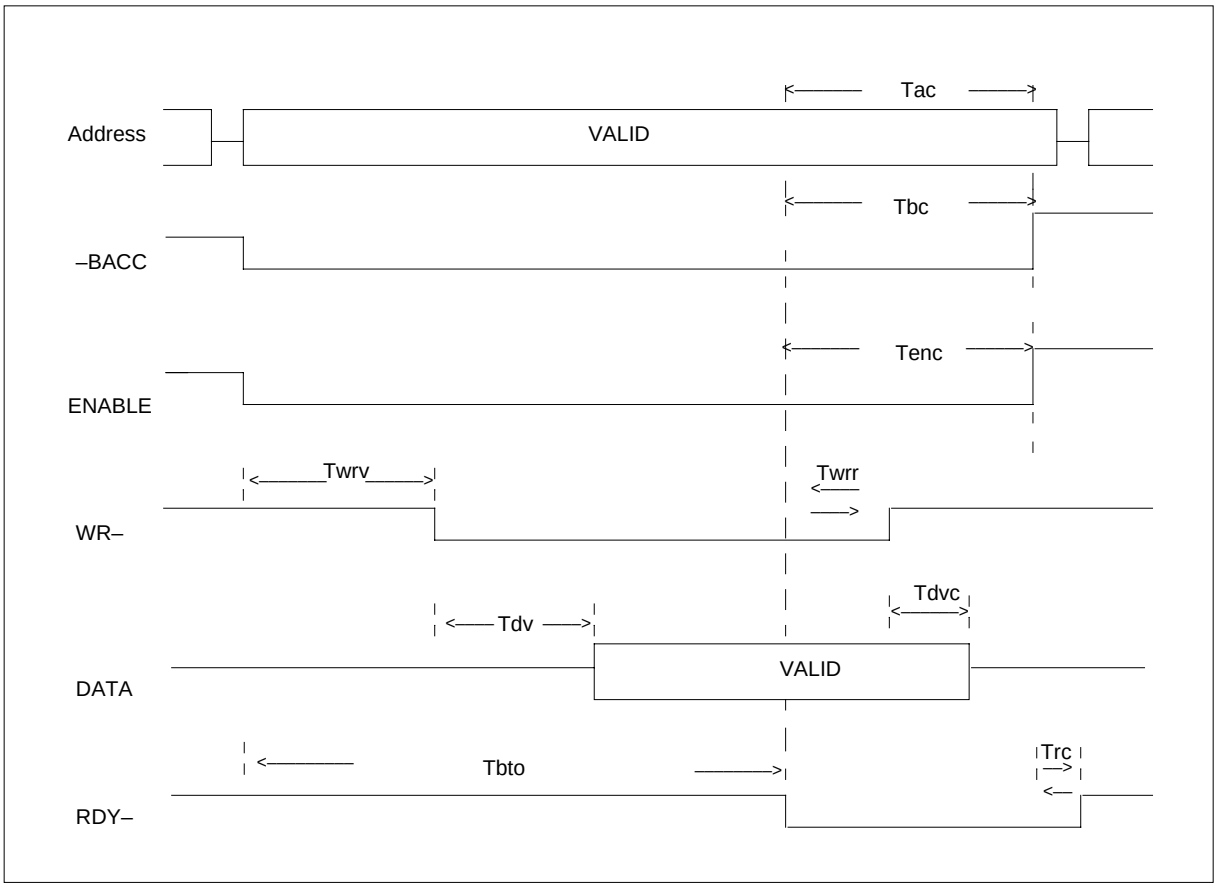


The NT6X52AA bus access read timing

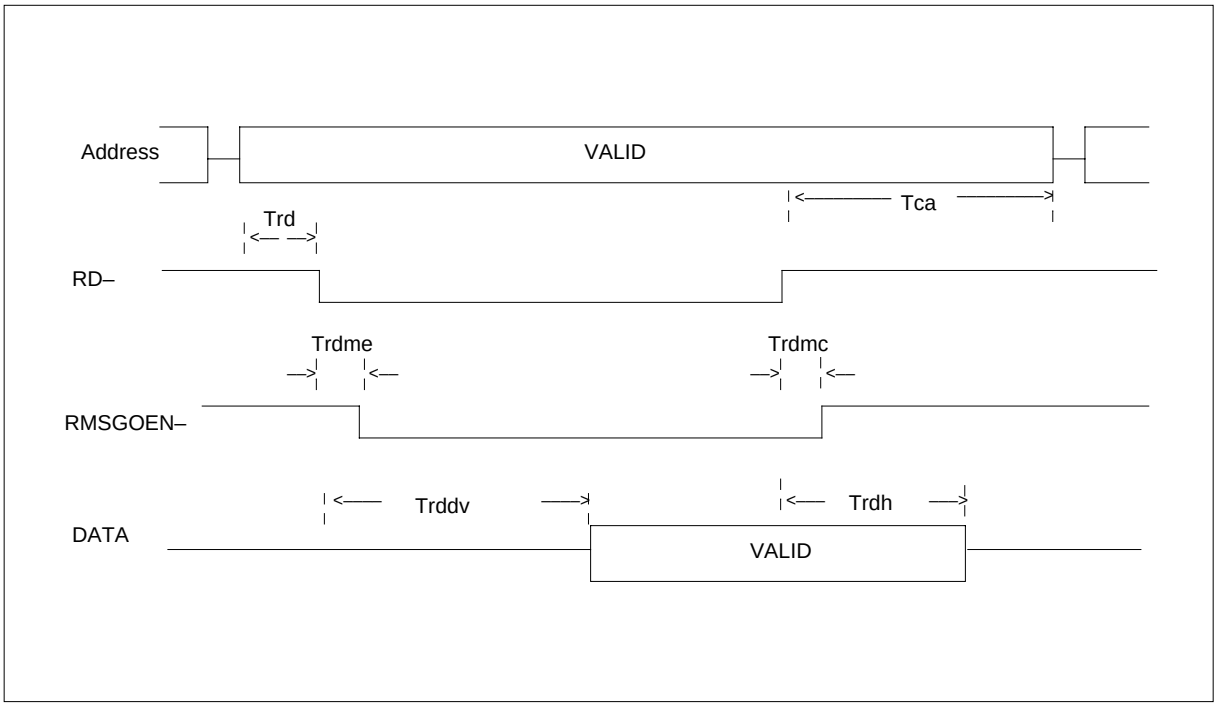


NT6X52AA (continued)

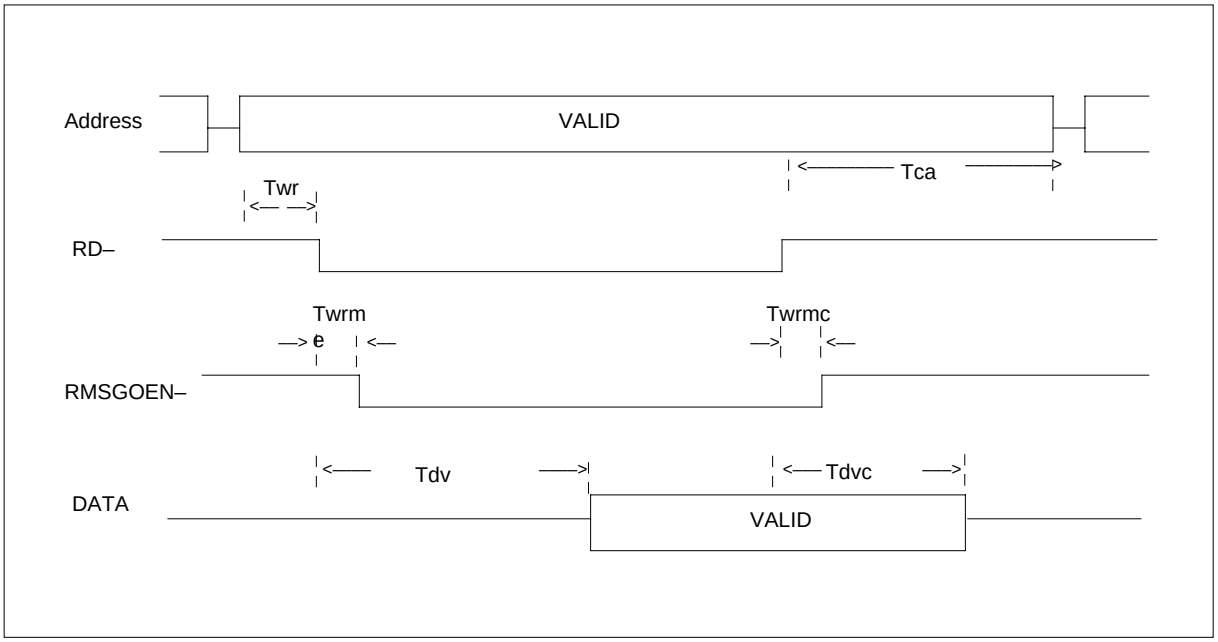
The NT6X52AA bus access write timing



The NT6X52AA message read timing



The NT6X52AA message write timing



NT6X52AA (end)

Technical data

Power requirements

The supply voltage for the NT6X52AA is as follows:

- minimum 4.5 V
- nominal 5.0 V
- maximum 5.5 V

The supply ripple is a maximum 50 mV. The supply current is 1.4mA nominal, and 3.0mA maximum.

NT6X52AB

Product description

The NT6X52AB is the international version of the line concentrating module (LCM) NT6X52AA digroup control card (DCC). This card performs the same pulse code modulation (PCM) time switching functions for 320, or 640 subscriber lines as the NT6X52AA performs. Line selection depends on the state of the mate LCM unit. The NT6X52AB allows the metering functions that international markets require.

Functional description

The LCM processor card and independent control logic control the NT6X52AB card. The NT6X52AB card contains a application-specific integrated circuit (ASIC) with a plain old telephone service (POTS) digroup controller chip (N11). The ASIC is responsible for most of the functionality of the card. The ASIC allows the card to perform the time switching functions of the LCM. The card performs switching functions for PCM speech data transferred between the line drawers and the controlling peripheral modules (PM).

The NT6X52AB has control logic and interface circuits. The link arbitration circuit is external to the ASIC. This circuit allows the output of the PCM links to flow back to the peripheral modules. This circuit makes sure that the LCM unit and the mate LCM use the correct links.

Functional blocks

The NT6X52AB has the following functional blocks:

- receive time switch (RTS)
- transmit time switch (TTS)
- connection memories
- timing and control
- test register
- looparound circuit
- message buffers
- thr LCM processor interface
- formatter

RTS

The RTS is a memory array inside the N11 ASIC. The RTS receives incoming PCM data from the central processor-side (C-side) ports. Each memory location has an associated channel on one of the eight incoming C-side ports.

NT6X52AB (continued)

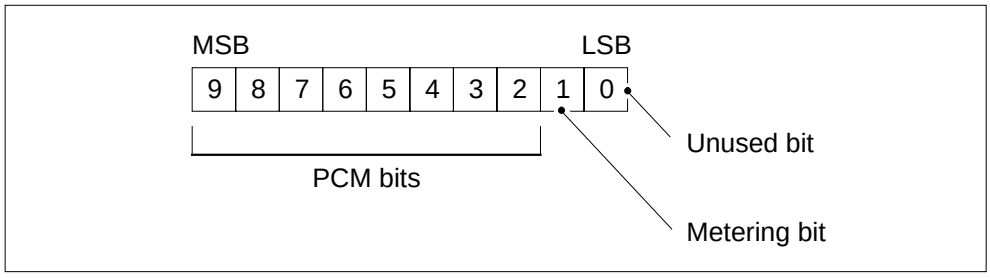
The system automatically loads data to the receive time switch memory location. The timing and control block controls the data load. The data load occurs during the second half of the 390-ns clock cycle.

The connection memory reads the PCM data from the receive time switch. The connection memory reads the PCM data during the first half of the 390-ns clock cycle. The system routes the PCM data to a peripheral module-side (P-side) port and channel. The address in the connection memory block controls this action.

TTS

The TTS is a memory array inside the N11 ASIC that receives incoming P-side PCM data. Each memory location is for a specified channel on one of the eight outgoing C-side ports. The timing and control block automatically reads data from the transmit time switch. The system routes the data to a channel on a C-side port. The following figure describes the 10 bits of data switched through the NT6X52AB.

NT6X52AB P-side PCM data bits



Connection memories

There are two different connection memories in the N11 ASIC. The connection memories are receive/transmit time switch connection memory and the receive/transmit multiplex connection memory.

The receive/transmit time switch connection memory (RTTSCM) is an 8-bit memory array. In the RTTSCM each location represents a specified channel on one of the P-side ports. This condition applies in the receive or transmit direction. The RTTSCM stores the address of the location in the receive/transmit time switch. This address represents a channel and a port on the C-side. The RTTSCM facilitates a PCM path between any P-side port and channel, and a C-side port and channel.

The receive/transmit multiplex connection memory (RTMCM) is a four-bit memory array that stores data that controls the two multiplexers. The two

multiplexers are between the two time switches (transmit and receive) and the P-side ports.

Timing and control

The N11 ASIC has two counters that control the flow of PCM data through the chip. One counter is a count-to-320 timer that addresses the connection memories and addresses a timing control read-only memory(ROM).

The other counter is a count-to-256 timer that produces the automatically controlled address for the two time switches.

Test register

The LCM processor writes to the test register when the system routes data by the following:

- through the looparound circuit for diagnostics
- to a specified outgoing channel for external communications.

Looparound circuit

A set of random access memory (RAM) cells functions as the looparound buffer in the N11 ASIC. The system routes the PCM data of every channel to this buffer from every outgoing P-side port. The system realigns this data between the transmit and receive paths on the P-side ports and channels by the offset. The offset is between the timing and control count-to-320 counter and another separate count-to-320 counter.

Message buffers

There are two message buffers in the N11 ASIC. The two message buffers are one write-only buffer, and one read-only buffer. The timing and control block can read from the write-only buffer. The timing and control block can write to the read-only buffer. The LCM processor uses these buffers for communication to the controlling node in the DMS system.

LCM processor interface

The LCM processor interface, inside the N11 ASIC, controls the bus timing to the 6X51 LCM processor card. This interface allows the processor access to the connection memories. This interface allows the processor to read from the transmit time switch.

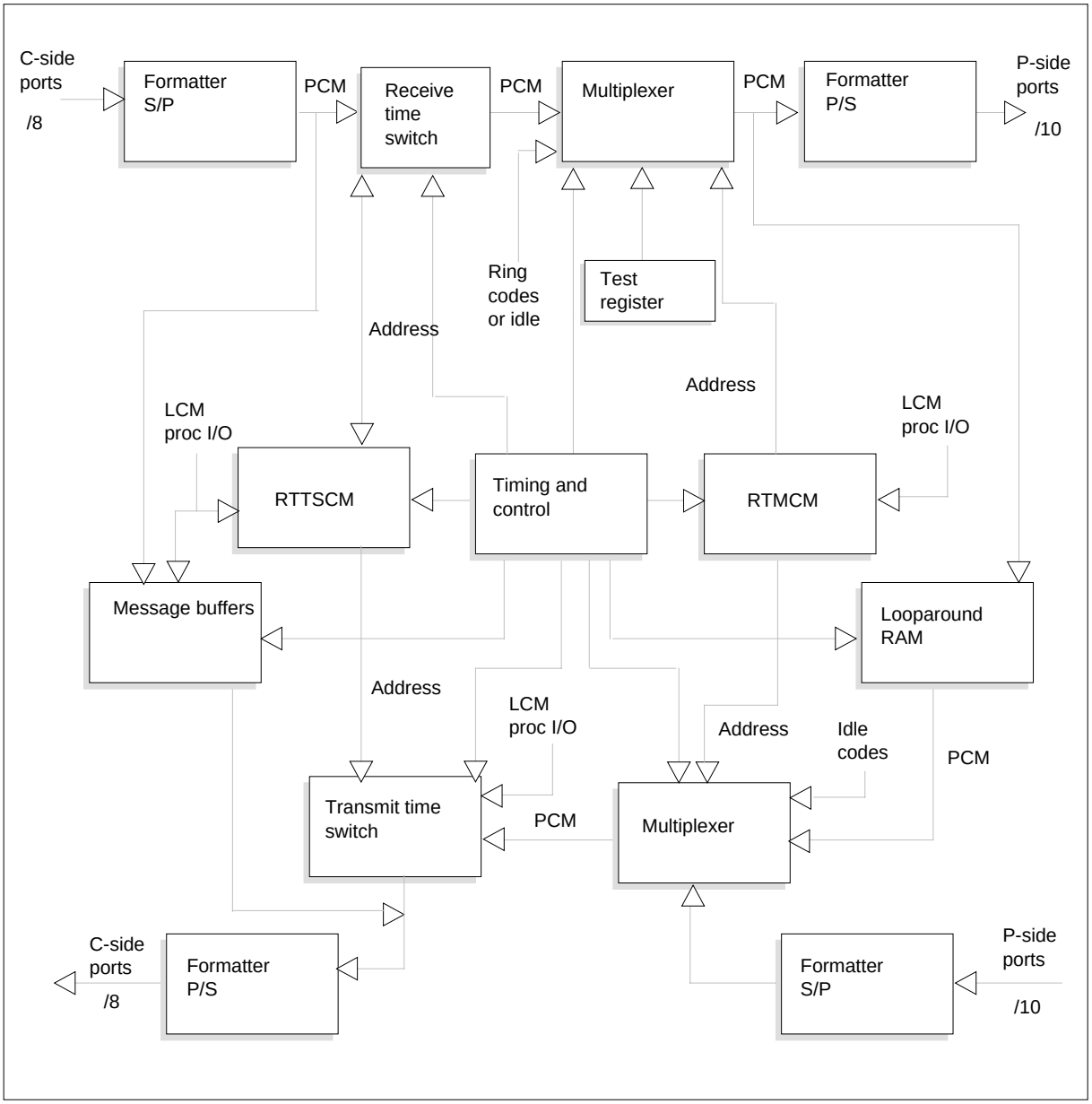
Formatter

The formatter, inside the N11 ASIC, converts all incoming serial transmission data to a parallel format. The formatter converts and all outgoing data back to a serial format before transmission to the ports.

NT6X52AB (continued)

The relationship between the functional blocks appears in the following figure.

NT6X52AB (N11 ASIC) functional blocks



Signaling

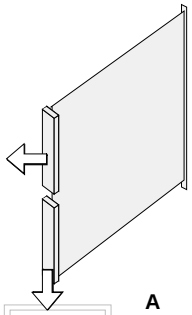
Pin numbers

The pin numbers for the NT6X52AB appear in the following figure.

NT6X52AB (continued)

NT6X52AB pin numbers

	A	B
1A 1B	GND	GND
2A 2B	+5V	+5V
3A 3B	+5V	+5V
4A 4B	+5V	+5V
5A 5B	GND	GND
6A 6B		
7A 7B	GND	CH0–
8A 8B	CLKMON	ACT–
9A 9B	MCH0–	MACT–
10A 10B	PCLK0+	PCLK0+
11A 11B	PFP0+	PFP0–
12A 12B	PRPCM0+	PRPCM0–
13A 13B	PRPCM1+	PRPCM1–
14A 14B	RPCM2+	RPCM2–
15A 15B	RPCM3+	RPCM3–
16A 16B	RPCM4+	RPCM4–
17A 17B	RPCM5+	RPCM5–
18A 18B	RPCM6+	RPCM6–
19A 19B	XPCM0+	XPCM0–
20A 20B	XPCM1+	XPCM1–
21A 21B	XPCM2+	XPCM2–
22A 22B	XPCM3+	XPCM3–
23A 23B	XPCM4+	XPCM4–
24A 24B	XPCM5+	XPCM5–
25A 25B	XPCM6+	XPCM6–
26A 26B	RMSGOEN	RDY–
27A 27B	EN3–	WMSGOEN
28A 28B	RCEN–	EN1–
29A 29B	–BACC	EN2–
30A 30B	A0	RD–
31A 31B	A1	WR–
32A 32B	A2	D0
33A 33B	A3	D1
34A 34B	A4	D2
35A 35B	A5	D3
36A 36B	A6	D4
37A 37B	A7	D5
38A 38B	A8	D6
39A 39B	A9	D7
40A 40B	GND	GND



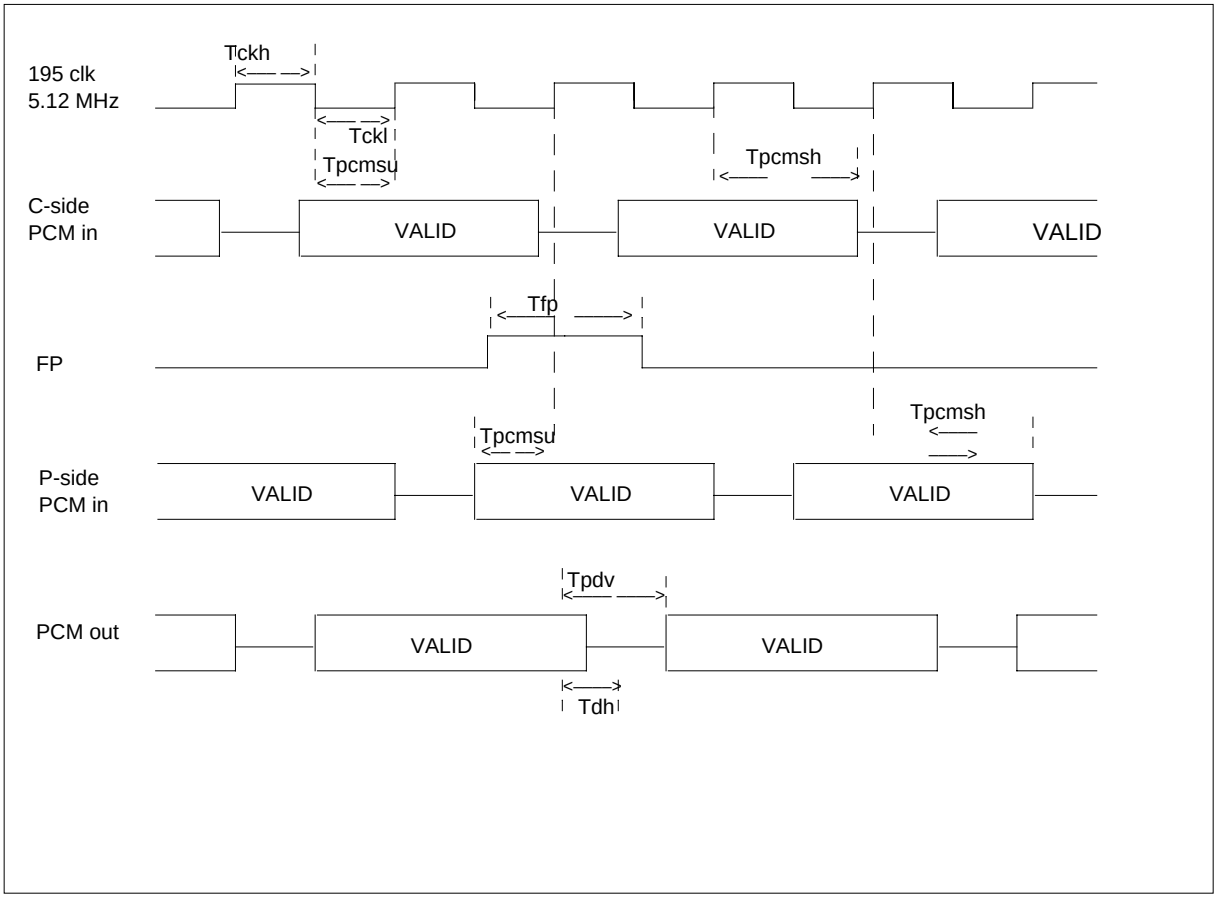
	A	B
41A 41B	GND	GND
42A 42B	RPCM7+	RPCM7–
43A 43B	XPCM7+	XPCM7–
44A 44B		
45A 45B		
46A 46B		
47A 47B	RD0	RD1
48A 48B	RD2	RD3
49A 49B	RD4	RD5
50A 50B	RD6	RD7
51A 51B	RD8	RD9
52A 52B	TD0	TD1
53A 53B	TD2	TD3
54A 54B	TD4	TD5
55A 55B	TD6	TD7
56A 56B	TD8	TD9
57A 57B		SYNC
58A 58B	–195	DFP–
59A 59B		GND
60A 60B	DCLK0+	DCLK0–
61A 61B	DCLK1+	DCLK1–
62A 62B	DCLK2+	DCLK2–
63A 63B	DCLK3+	DCLK3–
64A 64B	DCLK4+	DCLK4–
65A 65B	DCLK5+	DCLK5–
66A 66B	DCLK6+	DCLK6–
67A 67B	DCLK7+	DCLK7–
68A 68B	DCLK8+	DCLK8–
69A 69B	DCLK9+	DCLK9–
70A 70B	DFP0+	DFP0–
71A 71B	DFP1+	DFP1–
72A 72B	DFP2+	DFP2–
73A 73B	DFP3+	DFP3–
74A 74B	DFP4+	DFP4–
75A 75B	DFP5+	DFP5–
76A 76B	DFP6+	DFP6–
77A 77B	DFP7+	DFP7–
78A 78B	DFP8+	DFP8–
79A 79B	DFP9+	DFP9–
80A 80B	GND	GND

NT6X52AB (continued)

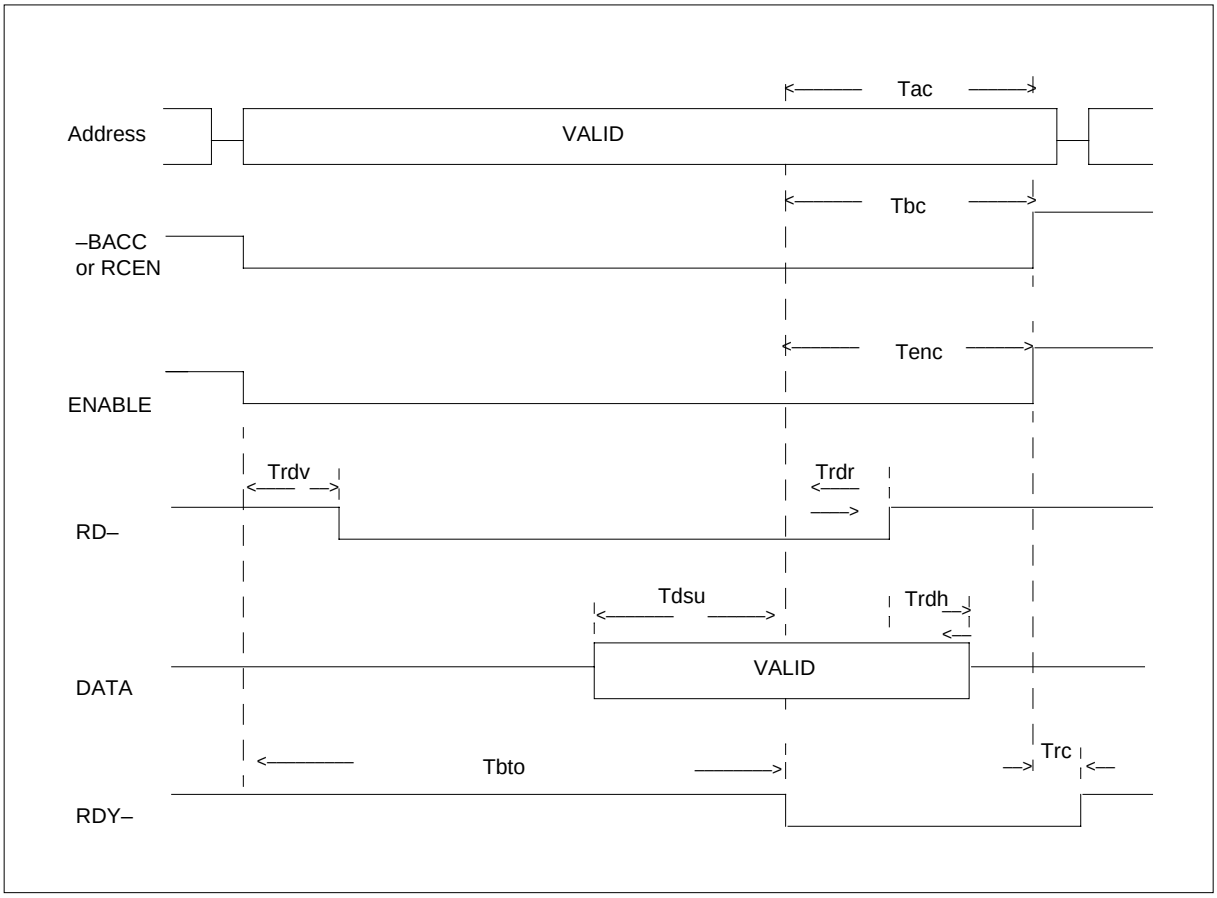
Timing

The timing for the NT6X52AB appears in the following figures.

NT6X52AB PCM timing

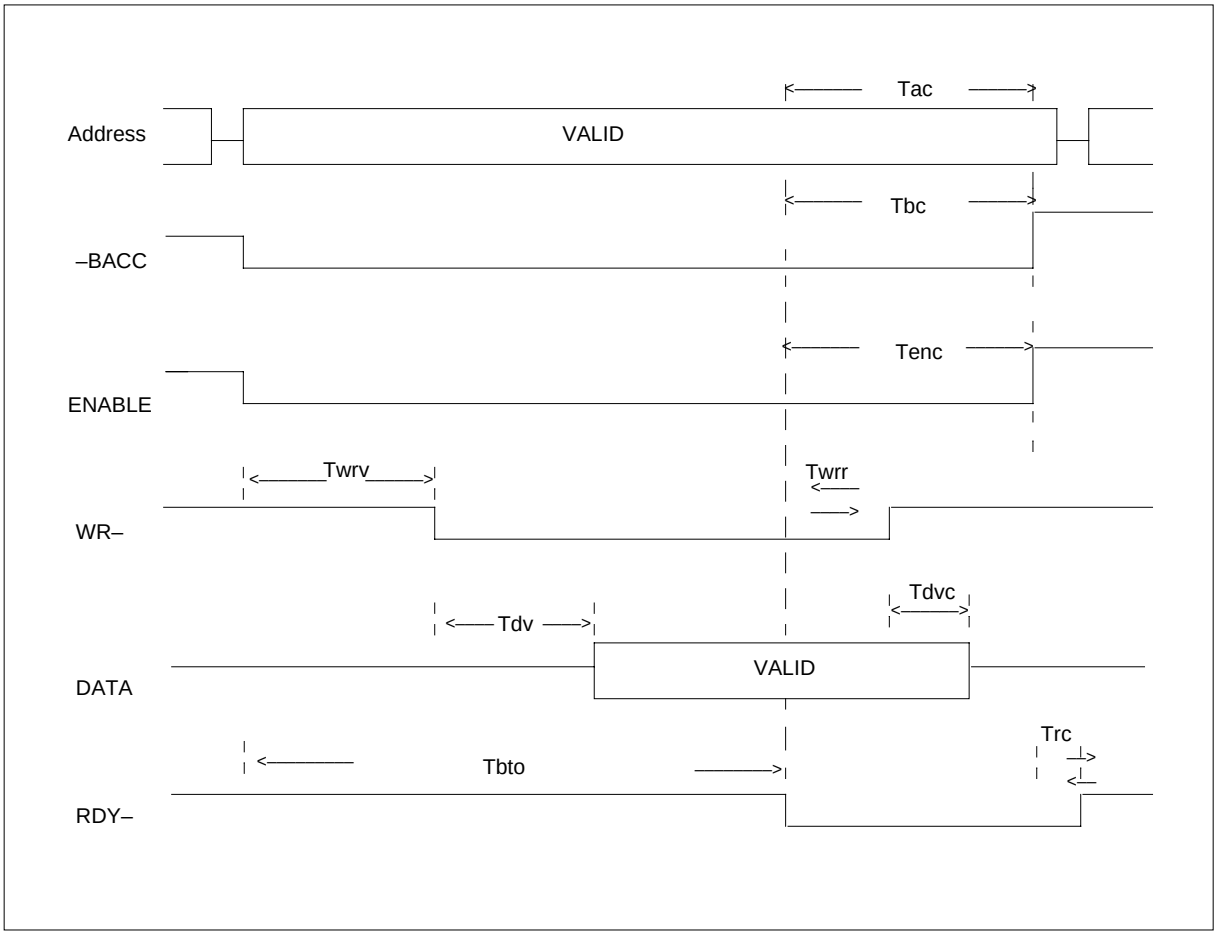


NT6X52AB bus access read timing

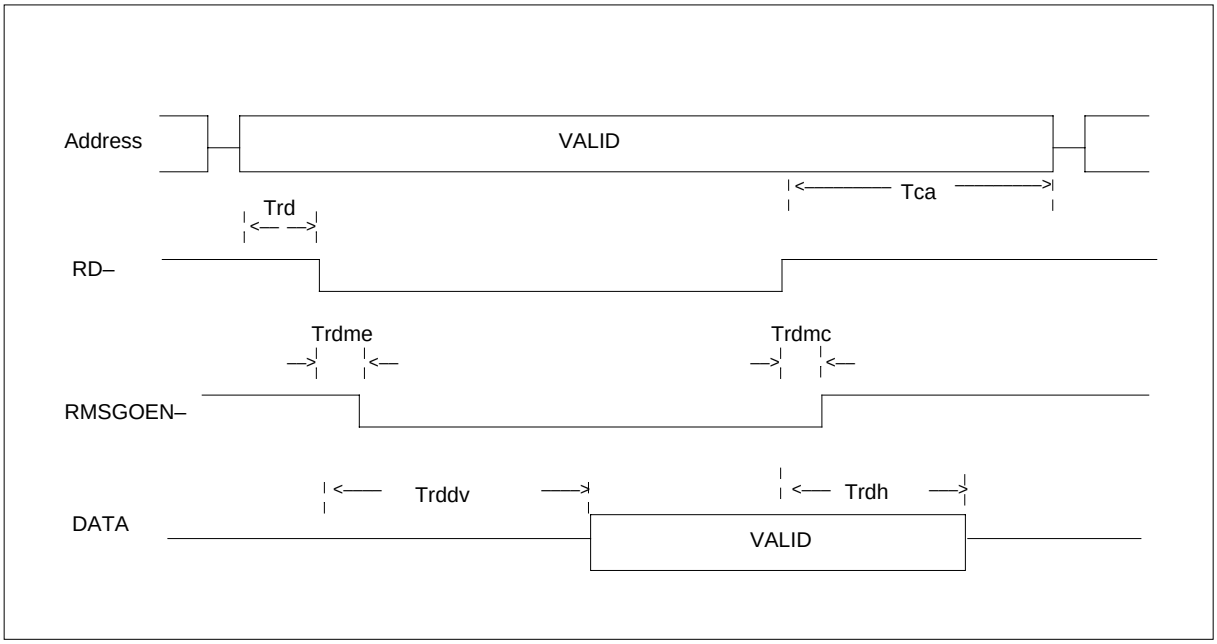


NT6X52AB (continued)

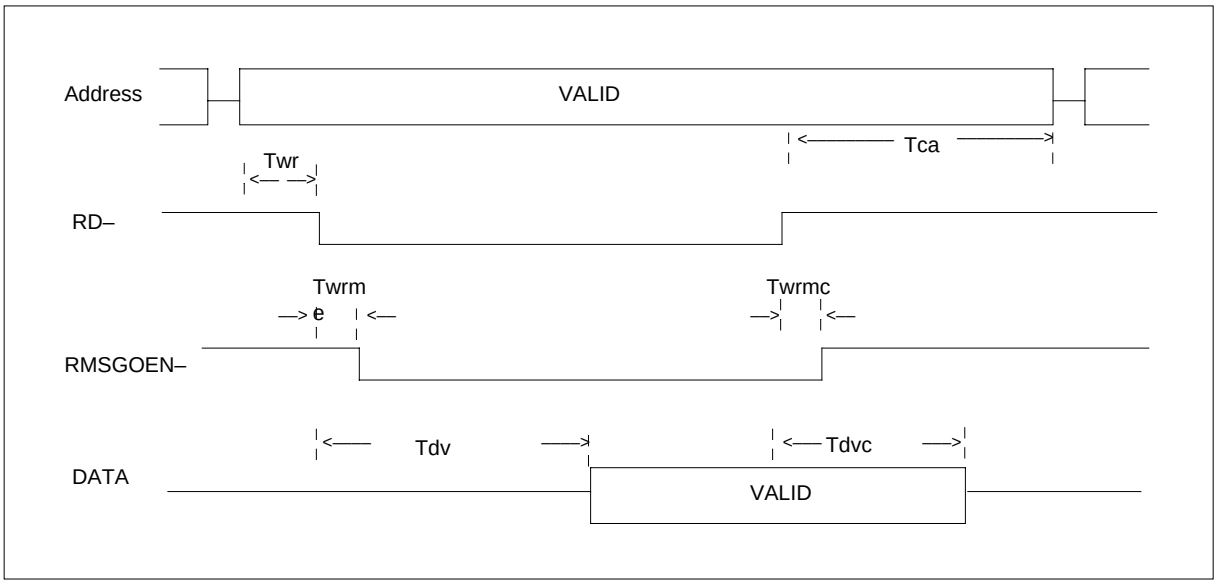
NT6X52AB bus access write timing



NT6X52AB message read timing



NT6X52AB message write timing



NT6X52AB (end)

Technical data

Power requirements

The supply voltage for the NT6X52AB is as follows:

- minimum 4.5 V
- nominal 5.0 V
- maximum 5.5 V

The supply ripple is a maximum 50 mV. The supply current is 1.4 mA nominal, and 3.0 mA maximum.

NT6X53AA

Product description

The NT6X53AA power converter 5V/15V card provides regulated +5.1V and +15V power supplies to circuit cards in a line concentrating module (LCM) shelf.

The card must be paired with another NT6X53AA on another shelf in the same LCM. The card is normally used in redundant pairs so that each converter operates at half of the rated output.

Location

The card is in the LCM shelf.

Functional description

The NT6X53AA receives a nominal -48V power supply from the office battery. The NT6X53AA provides output voltages of +5.1V and +15V. The circuits of the card monitor the output voltages. If overvoltage or undervoltage conditions are present, these circuits generate an alarm signal and shut down the converter.

Functional blocks

The NT6X53AA has the following functional blocks:

- input filter
- auxiliary power supply
- +15V power switch
- two pulse width modulation (PWM) circuits
- two transformers
- +15V rectifier/filter circuit
- two isolated diodes
- +5.1V power switch
- +5.1V rectifier/filter circuit
- ring current detector and ANI/coin multiplexer (MUX)
- overvoltage/undervoltage (OV/UV) monitor
- relay

Input filter

The power card produces the input filter that prevents the appearance of noise on the -48V office battery supply line.

NT6X53AA (continued)

Auxiliary power supply

The auxiliary power supply uses the -48V office battery input to produce a nominal +15V, 80mA output.

+15V power switch

The -48V office battery input activates +15V power switch. The power switch sends the power current through the +15V circuits on the card. The power switch contains an oscillator to synchronize the card if the 64 kHz synchronization signal from the LCM fails.

PWM

The auxiliary power supply powers PWM circuits. The power supply uses a 64 kHz synchronization signal from the LCM shelf. This signal operates the power switches in a 32 kHz synchronized mode.

Transformers

The transformers couple the ac output from the power switches for transmission to the +15V rectifier/filter circuit and the +5.1V rectifier/filter circuit.

+15V rectifier/filter circuit

The +15V rectifier/filter circuit converts the +15V ac output to a dc output.

Isolated diodes

Removal or insertion of a card when the power is on can damage the card and the LCM shelf. The isolated diode circuits protect the card and the LCM shelf in this event. The circuits allow one of a group of two or more converters to fail. This action does not affect the other units.

+5.1V power switch

The -48V office battery input activates the +5.1V power switch. The power switch sends the power current through the +5.1V circuits on the card. The power switch contains an oscillator to synchronize the card if the 64 kHz synchronization signal from the LCM fails.

+5.1V rectifier/filter circuit

The +5.1V rectifier/filter circuit converts the +5.1V ac output to a dc output.

Ring current detector and ANI/coin MUX

The ring current detector and ANI/coin MUX monitors the current that flows in the path the MUX selects. If the current reaches or exceeds 10mA, the output logic state of the circuit changes. This change of state provides an indication of the ringing current level to the external equipment.

OV/UV monitor

The OV/UV monitor circuit detects overvoltage and undervoltage conditions and generates an external alarm with an alarm relay. The monitor sends a shutdown signal to the PWM circuits when overvoltage and undervoltage conditions are present.

Relay

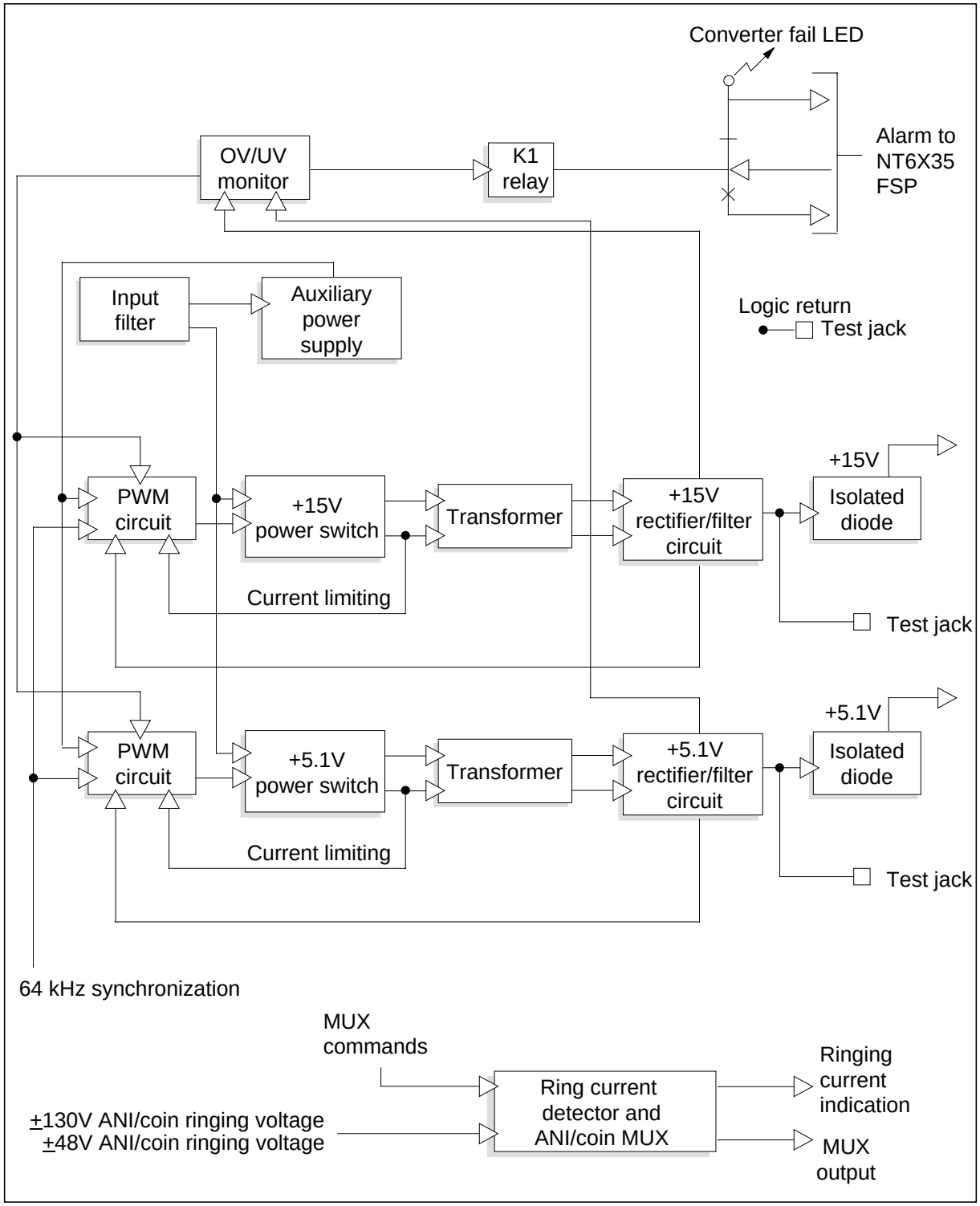
One relay is in the card to send alarm information to the NT6X35 frame supervisory panel (FSP). The following table is the alarm and the operated and released functions.

Relay operation

Relay	Operated	Released
K1	Normal operation	The relay sends an alarm to the NT6X35. The converter fail LED is on.

The relationship between the functional blocks appears in the following figure.

NT6X53AA (continued)



Technical data

The MUX of the card has an ANI/coin input voltage of ±130V and ±48V; the MUX must have a ringing current input that meets Bell and Rural Electrification Administration (REA) requirements. The MUX relay commands must have logic return on appropriate inputs.

The MUX outputs a 5V ±1V transistor-transistor logic (TTL) high current detector. The multiplexer relay functions have open circuit, resistive path, low resistance at the appropriate outputs.

The card has an 50% efficiency input rating and uses a 64 kHz synchronization pulse. The output specifications for the +5.1V output of the card appear in the following table.

Output specifications +5.1V

Characteristic	Value
Nominal voltage	+5.1V
Regulation	±4%
High voltage shutdown	+6.5V ±1.5V
Low voltage shutdown	+4.0V ±0.5V
Ripple	50.0mV rms
Current	15.5A maximum 0.0A minimum
Current limit	20.0A ±4.5A

The output specifications for the +15V output appear in the following table.

Output specifications +15V (Sheet 1 of 2)

Characteristic	Value
Nominal voltage	+15.0V
Regulation	±5%
High voltage shutdown	+17.5V ±1.5V
Low voltage shutdown	+13.0V ±1.0V
Ripple	100.0mV rms

NT6X53AA (end)

Output specifications +15V (Sheet 2 of 2)

Characteristic	Value
Current	15.0A maximum 0.0A minimum
Current limit	19.0A ±4.0A

Dimensions

The dimensions for the NT6X53AA are as follows:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11 in.)
- width: 66 mm (2.6 in.)

Power requirements

The power requirements for the NT6X53AA appear in the following table.

Power requirements

Voltage	Current
-42V minimal	
-48V nominal	
-56V maximum	10A

The maximum heat distribution is 95W at full load.

NT6X53BA

Product description

The NT6X53BA power converter 5.25V/15V card provides regulated +5.25V and +15V power supplies to circuit cards in an integrated services digital network (ISDN) line concentrating module (LCMI) shelf.

The card operates with an NT6X53EA converter on the same shelf in the LCMI. Another NT6X53BA and NT6X53EA on another shelf in the same LCMI must use this card. Each converter normally operates at half of the rated output.

Location

The card is in the LCMI shelf.

Functional description

The NT6X53BA receives a nominal -48V power supply from the office battery and provides output voltages of +5.25V and +15V. The circuits of the card monitor the output voltages. If overvoltage or undervoltage conditions are present, the circuits generate an alarm signal and shut down the converter.

Functional blocks

The NT6X53BA contains the following functional blocks:

- input filter
- auxiliary power supply
- +15V power switch
- two pulse width modulation (PWM) circuits
- two transformers
- +15V rectifier/filter circuit
- two isolated diodes
- +5.25V power switch
- +5.25V rectifier/filter circuit
- ring current detector and ANI/coin multiplexer (MUX)
- overvoltage/undervoltage (OV/UV) monitor
- relay

Input filter

The power card produces the input filter that prevents noise on the -48V office battery supply line.

NT6X53BA (continued)

Auxiliary power supply

The auxiliary power supply uses the -48V office battery input to produce a nominal +15V, 80mA output.

+15V power switch

The -48V office battery input activates the +15V power switch. The power switch sends the power current through the +15V circuits on the card. The power switch contains an oscillator to synchronize the card if the 64 kHz synchronization signal from the LCMI fails.

PWM circuits

The auxiliary power supply powers the PWM circuits. The power supply uses a 64 kHz synchronization signal from the LCMI shelf to operate the power switches in a 32 kHz synchronized mode.

Transformers

The transformers couple the ac output from the power switches for transmission to the +15V rectifier/filter circuit and the +5.25V rectifier/filter circuit.

+15V rectifier/filter circuit

The +15V rectifier/filter circuit converts the +15V ac output to a dc output.

Isolated diodes

Removal or insertion of a card when the power is on can damage the card and the LCMI shelf. The isolated diode circuits protect the card and the LCMI shelf in this event. The circuits allow one group of two or more converters to fail. This action does not affect other units.

+5.25V power switch

The -48V office battery activates the +5.25V power switch. The power switch sends the power current through the +5.25V circuits on the card. The power switch contains an oscillator to synchronize the card if the 64 kHz synchronization signal from the LCMI fails.

+5.25V rectifier/filter circuit

The +5.25V rectifier/filter circuit converts the +5.25V ac output to a dc output.

Ring current detector and ANI/coin MUX

The ring current detector and ANI/coin MUX monitors the current that flows in the path the MUX selects. If the current reaches or exceeds 10mA, the output logic state of the circuit changes. This change of state provides an indication of the ringing current level to the external equipment.

OV/UV monitor

The OV/UV monitor circuit detects overvoltage and undervoltage conditions. The monitor circuit generates an external alarm that uses an alarm relay. The monitor sends a shutdown signal to the PWM circuits when overvoltage and undervoltage conditions are present.

Relay

One relay is in the card to send alarm information to the NT6X35 frame supervisory panel (FSP). The alarm and the operated and released functions appear in the following table.

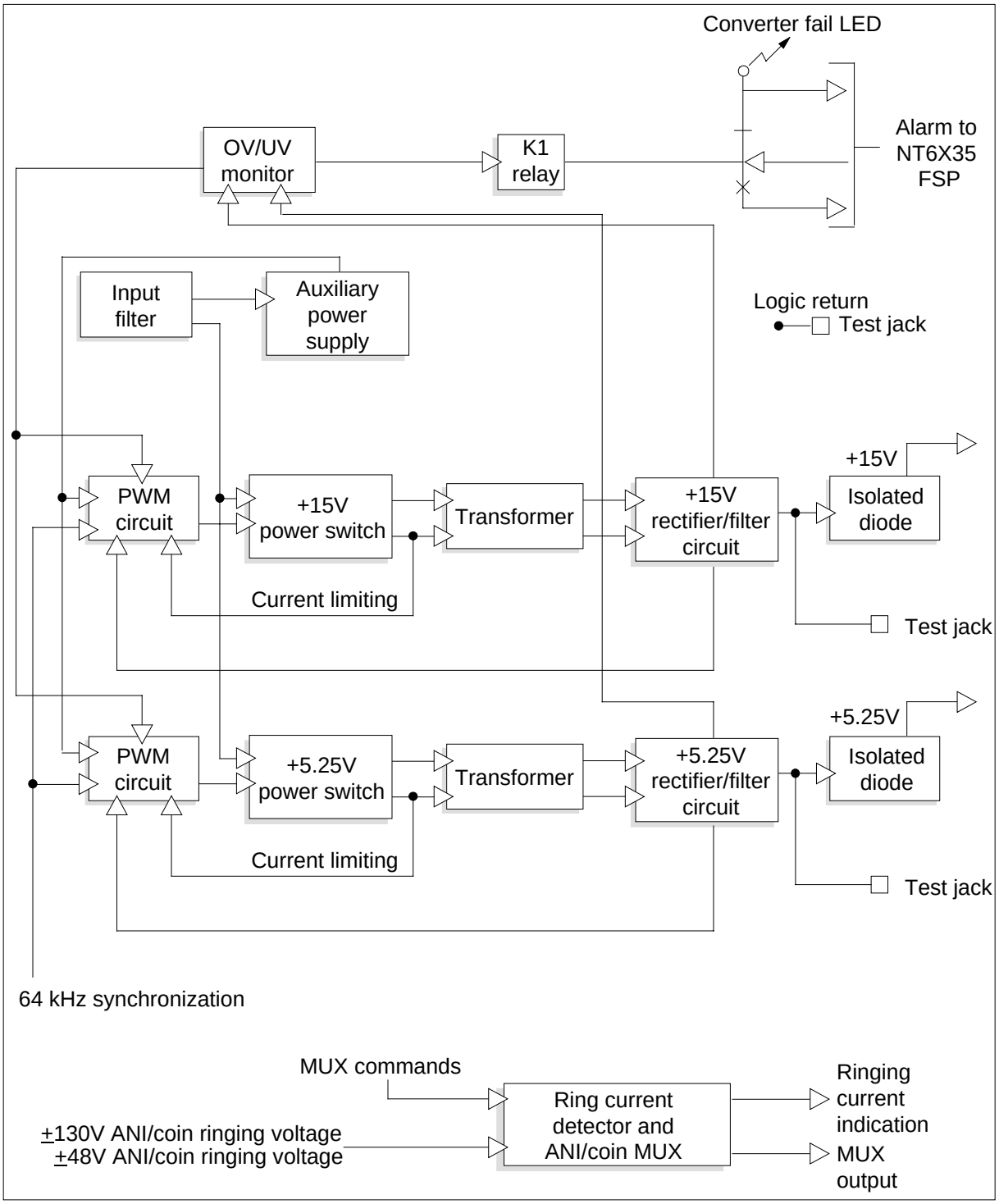
Relay operation

Relay	Operated	Released
K1	Normal operation	The relay sends an alarm to the NT6X35. The converter fail LED is on.

The relationship between the functional blocks appears in the following figure.

NT6X53BA (continued)

NT6X53BA functional blocks



Technical data

The MUX of the card has an ANI/coin input voltage of ±130V and ±48V. The MUX must have a ringing current input that meets Bell and Rural Electrification Administration (REA) requirements. The MUX relay commands must have logic return on appropriate inputs.

The multiplexer outputs a 5V ±1V transistor-transistor logic (TTL) high current detector. The MUX relay functions have open circuit, resistive path, or low resistance at the appropriate outputs.

The card has an 80% efficiency input rating and uses a 64 kHz synchronization pulse. The following table lists the output specifications for the card's +5.25V output.

Output specifications +5.25V

Characteristic	Value
Nominal voltage	+5.25V
Regulation	±4%
High voltage shutdown	+6.50V ±1.50V
Low voltage shutdown	+4.00V ±0.50V
Ripple	50.00mV rms
Current	15.50A maximum 0.00A minimum
Current limit	20.00A ±4.50A

The output specifications for the +15V output appear in the following table.

Output specifications +15V (Sheet 1 of 2)

Characteristic	Value
Nominal voltage	+15.0V
Regulation	±5%
High voltage shutdown	+17.5V ±1.5V
Low voltage shutdown	+13.0V ±1.0V
Ripple	100.0mV rms

NT6X53BA (end)

Output specifications +15V (Sheet 2 of 2)

Characteristic	Value
Current	15.0A maximum 0.0A minimum
Current limit	19.0A ±4.0A

Dimensions

The dimensions for the NT6X53BA are as follows:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11 in.)
- width: 66 mm (2.6 in.)

Power requirements

The power requirements for the NT6X53BA appear in the following table.

Power requirements

Voltage	Current
-42V minimal	
-48V nominal	
-56V maximum	10A

The maximum heat distribution is 95W at full load.

NT6X53CA

Product description

The integrated services digital network (ISDN) enhanced line concentrating module (LCME) power converter card provides +5V and +15V power supplies to the DMS-100 switching center.

Functional description

The NT6X53CA card is a dc-to-dc regulated converter that converts a nominal -48V input to a +5V and a +15V output. The converter has protection against overvoltage, undervoltage and overcurrent.

Functional blocks

The NT6X53CA contains the following functional blocks:

- input filter
- auxiliary power supply
- pulse width modulator (PWM) modules
- power stages
- output stages
- monitor module
- alarm relay circuit

Input filter

The input filter contains a set of inductors and capacitors. This set prevents the return to the input line of an excess of ripple and electromagnetic interference (EMI).

Auxiliary power supply

The auxiliary power supply provides housekeeping power for the NT6X53CA card. The output of this block is separate from the input line.

PWM modules

Two PWM modules control the power stages of the converter to regulate the outputs and provide synchronization to an external 32 kHz clock.

Power stages

The power stages switch the -48V dc input across the power transformers, where the voltage is stepped down. The power stages are a single-stage forward converter that generate +6V ac output. The power stages are a push-pull converter that generate a +16V ac output.

NT6X53CA (continued)

Output stages

The output stages rectify and filter the +6V from the forward converter power stage and the +16V from the push-pull power stage. This action produces the +5.1V and +15V outputs respectively.

Monitor module

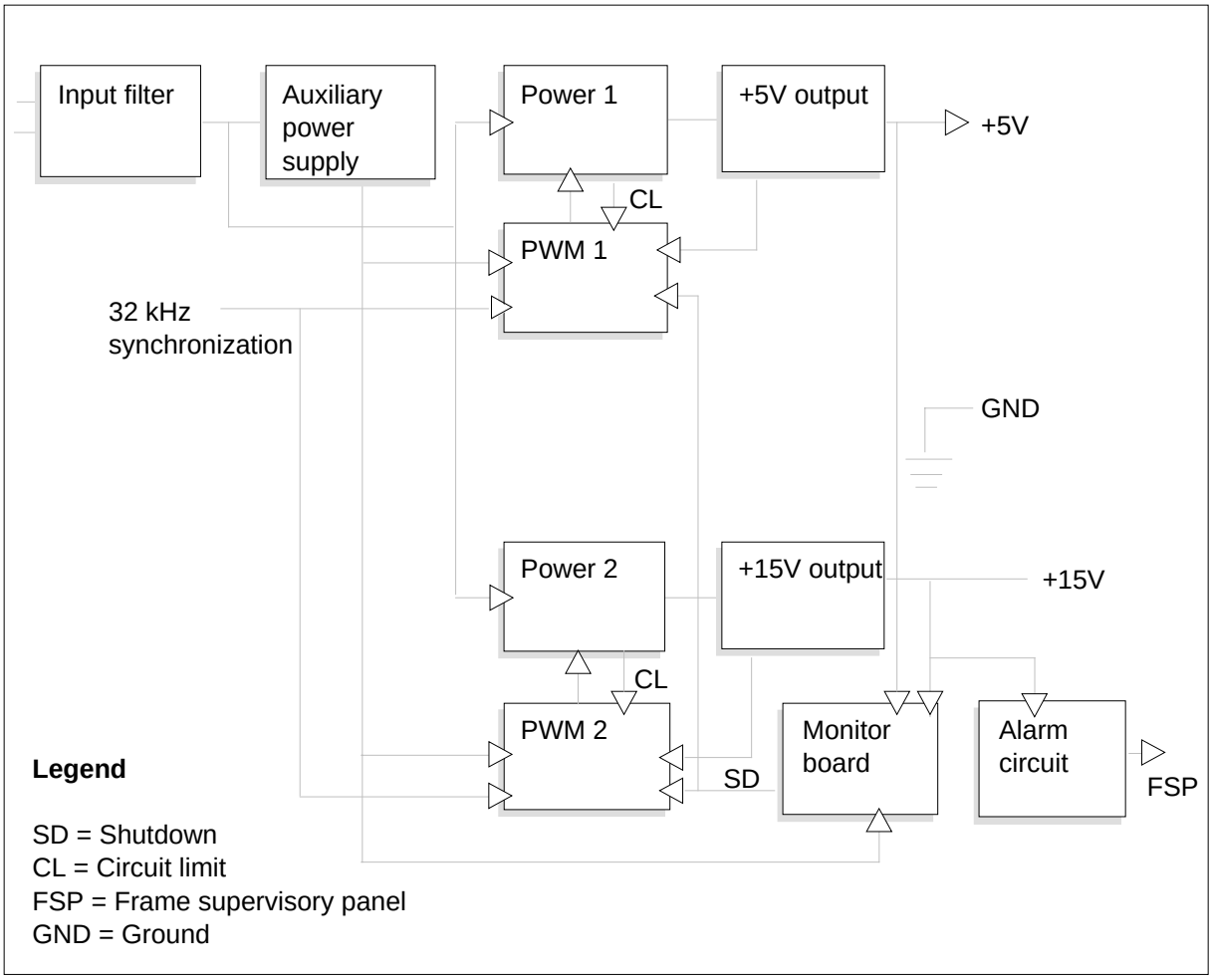
The monitor module shuts down the NT6X53CA in the event of converter failure to protect against overvoltage and undervoltage conditions.

Alarm relay circuit

The alarm relay circuit turns on the faceplate LED failure indicator and sends an alarm signal to the frame supervisory panel. This action occurs when failure in any part of the NT6X53CA is present.

The relationship between the functional blocks appears in the following figure.

NT6X53CA functional blocks



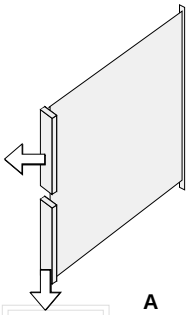
Signaling

Pin numbers

The pin numbers for the NT6X53CA appear in the following figure.

NT6X53CA (continued)

NT6X53CA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	GND	GND
3A 3B	GND	GND
4A 4B	GND	GND
5A 5B	GND	GND
6A 6B	GND	GND
7A 7B	GND	GND
8A 8B	GND	GND
9A 9B	GND	GND
10A 10B	GND	GND
11A 11B	+5V	+5V
12A 12B	+5V	+5V
13A 13B	+5V	+5V
14A 14B	+5V	+5V
15A 15B	+5V	+5V
16A 16B	+5V	+5V
17A 17B	+5V	+5V
18A 18B	+5V	+5V
19A 19B	+5V	+5V
20A 20B	+5V	+5V
21A 21B	+15V	+15V
22A 22B	+15V	+15V
23A 23B	+15V	+15V
24A 24B	+15V	+15V
25A 25B	+15V	+15V
26A 26B	+15V	+15V
27A 27B	+15V	+15V
28A 28B	+15V	+15V
29A 29B	+15V	+15V
30A 30B	+15V	+15V
31A 31B	GND	GND
32A 32B	GND	GND
33A 33B	GND	GND
34A 34B	GND	GND
35A 35B	GND	GND
36A 36B	GND	GND
37A 37B	GND	GND
38A 38B	GND	GND
39A 39B	GND	GND
40A 40B	GND	GND

	A	B
41A 41B	GND	GND
42A 42B		
43A 43B		
44A 44B		
45A 45B		
46A 46B	GND	GND
47A 47B		
48A 48B		
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B		
58A 58B		
59A 59B		
60A 60B	PWRFAIL0	
61A 61B		
62A 62B		
63A 63B		
64A 64B		
65A 65B		
66A 66B		GND
67A 67B	ABS	MONITOR
68A 68B	SYNC	ABS–RET
69A 69B		
70A 70B	–48VBAT	–48VBAT
71A 71B	–48VBAT	–48VBAT
72A 72B	–48VBAT	–48VBAT
73A 73B	–48VBAT	–48VBAT
74A 74B		
75A 75B		
76A 76B		
77A 77B	BAT–RET	BAT–RET
78A 78B	BAT–RET	BAT–RET
79A 79B	BAT–RET	BAT–RET
80A 80B	BAT–RET	BAT–RET

Technical data

Power requirements

The input and output specifications for the NT6X53CA appear in the following tables.

NT6X53CA input specifications

Parameter	Nominal	Minimum	Maximum
Voltage	-48Vdc	-42Vdc	-56Vdc
Current			10A
Efficiency	80%		
Synchronizing TTL	32 kHz		

NT6X53CA output specifications

Parameter	+5.1V output	+15V output
Regulation	±4%	±5%
High voltage shutdown	±6.5V	+17.5V
Tolerance (HVS)	±0.5V	±1.5V
Low voltage shutdown	+4V	+13V
Tolerance (LVS)	±0.5V	±1V
Voltage (nominal)	+5.1V	+15V
Ripple	50mv RMS	100mv RMS
Maximum current	15.5A	15A
Minimum current	0	0
Current limit	20A	19A
Tolerance (CL)	±4.5A	±4A

NT6X53EA

Product description

The integrated services digital network (ISDN) line concentrating module (LCMI) power converter card provides +5V and -15V power supplies to the DMS-100 switching center.

Functional description

The NT6X53EA card is a dc-to-dc regulated converter that converts a nominal -48V input to a +5V and a -15V output. The converter protects against overvoltage, undervoltage, and overcurrent.

Functional blocks

The NT6X53EA contains the following functional blocks:

- input filter
- auxiliary power supply
- pulse width modulator (PWM) modules
- power stages
- output stages
- monitor module
- alarm relay circuit

Input filter

The input filter contains a set of inductors and capacitors. The inductors and capacitors make sure an excess of ripple and electromagnetic interference (EMI) does not return to the input line.

Auxiliary power supply

The auxiliary power supply provides housekeeping power for the NT6X53EA card. The output of this block is separate from the input line.

PWM modules

Two PWM modules control the power stages of the converter. The PWM modules regulate the outputs and provide synchronization to an external 32 kHz clock.

Power stages

The power stages switch the -48V dc input across the power transformers. The voltage is stepped down in the transformers. The power stages are a single-stage forward converter that generates +6V ac output, and a push-pull converter that generates a -16V ac output.

Output stages

The output stages rectify and filter the +6V from the forward converter power stage and the -16V from the push-pull power stage. The stages produce the +5.1V and -15V outputs.

Monitor module

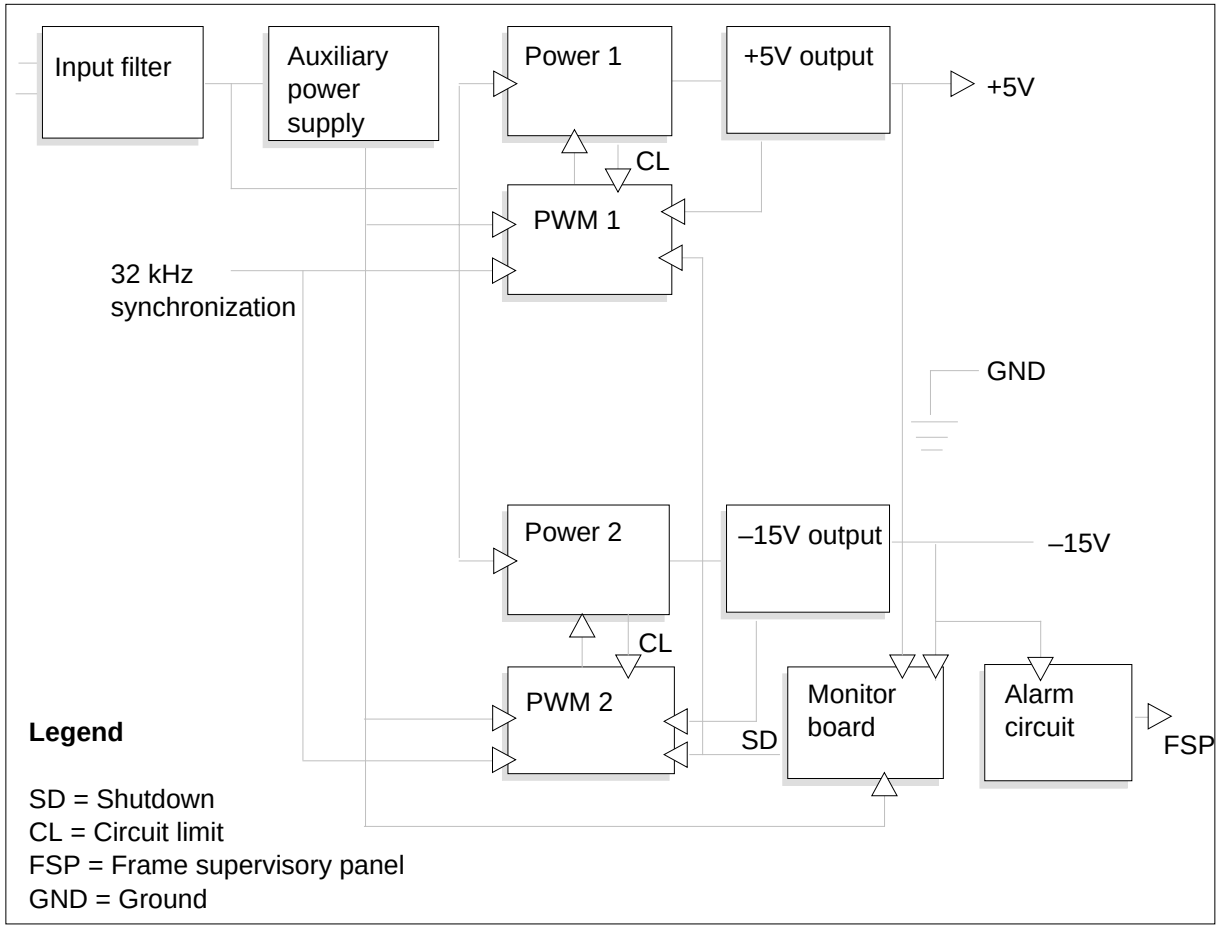
The monitor module shuts down the if converter failure occurs. This action protects the card against overvoltage and undervoltage conditions.

Alarm relay circuit

The alarm relay circuit turns on the faceplate LED failure indicator. The circuit sends an alarm signal to the frame supervisory panel. The circuit sends this alarm signal when failure occurs in any part of the NT6X53EA.

The relationship between the functional blocks appears in the following figure.

NT6X53EA functional blocks



NT6X53EA (continued)

Signaling

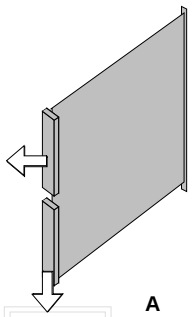
Pin numbers

The pin numbers for the NT6X53EA appear in the following figure.

NT6X53EA (continued)

NT6X53EA pin numbers

	A	B
1A 1B	GND	GND
2A 2B	GND	GND
3A 3B	GND	GND
4A 4B	GND	GND
5A 5B	GND	GND
6A 6B	GND	GND
7A 7B	GND	GND
8A 8B	GND	GND
9A 9B	GND	GND
10A 10B	GND	GND
11A 11B	+5V	+5V
12A 12B	+5V	+5V
13A 13B	+5V	+5V
14A 14B	+5V	+5V
15A 15B	+5V	+5V
16A 16B	+5V	+5V
17A 17B	+5V	+5V
18A 18B	+5V	+5V
19A 19B	+5V	+5V
20A 20B	+5V	+5V
21A 21B	–15V	–15V
22A 22B	–15V	–15V
23A 23B	–15V	–15V
24A 24B	–15V	–15V
25A 25B	–15V	–15V
26A 26B	–15V	–15V
27A 27B	–15V	–15V
28A 28B	–15V	–15V
29A 29B	–15V	–15V
30A 30B	–15V	–15V
31A 31B	GND	GND
32A 32B	GND	GND
33A 33B	GND	GND
34A 34B	GND	GND
35A 35B	GND	GND
36A 36B	GND	GND
37A 37B	GND	GND
38A 38B	GND	GND
39A 39B	GND	GND
40A 40B	GND	GND



	A	B
41A 41B	GND	GND
42A 42B		
43A 43B		
44A 44B		
45A 45B		
46A 46B	GND	GND
47A 47B		
48A 48B		
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B		
58A 58B		
59A 59B		
60A 60B	PWRFAIL0	
61A 61B		
62A 62B		
63A 63B		
64A 64B		
65A 65B		
66A 66B		GND
67A 67B	ABS	MONITOR
68A 68B	SYNC	ABS–RET
69A 69B		
70A 70B	–48VBAT	–48VBAT
71A 71B	–48VBAT	–48VBAT
72A 72B	–48VBAT	–48VBAT
73A 73B	–48VBAT	–48VBAT
74A 74B		
75A 75B		
76A 76B		
77A 77B	BAT–RET	BAT–RET
78A 78B	BAT–RET	BAT–RET
79A 79B	BAT–RET	BAT–RET
80A 80B	BAT–RET	BAT–RET

NT6X53EA (end)

Technical data

Power requirements

The input and output specifications for the NT6X53EA appear in the following tables.

NT6X53EA input specifications

Parameter	Heading	Heading	Heading
Voltage	-48Vdc	-42Vdc	-56Vdc
Current			10A
Efficiency	80%		
Synchronizing TTL	32 kHz		

NT6X53EA output specifications

Parameter	+5.0V output	+15V output
Regulation	±3%	±5%
High voltage shutdown	±6.5V	+17.5V
Tolerance (HVS)	±0.5V	±1.5V
Low voltage shutdown	+4V	+13V
Tolerance (LVS)	±0.5V	±1V
Voltage (nominal)	+5.1V	+15V
Ripple	50mv RMS	100mv RMS
Maximum current	15.5A	15A
Minimum current	0	0
Current limit	20A	19A
Tolerance (CL)	±4.5A	±4A

NT6X54AA

Product description

The NT6X54AA bus interface card (BIC) provides interfaces. These interfaces are between 64 line cards in the line drawer and one 32-channel digroup to each line concentrating array (shelf).

Location

The NT6X54AA is in the drawer of a line concentrating module (LCM). Each line drawer has one bus interface card (BIC) and a maximum of 64 line cards of different types. Each scan chip links one digroup with 32 line cards. If one digroup (scan chip) fails, the digroup that remains takes over all 64 lines.

Functional description

The NT6X54AA performs the following functions:

- multiplexes and demultiplexes a 32-channel link on 32 line card buses
- receives control messages to line cards asynchronously. Stores these messages until the messages are output to line cards during channels 0 or 16
- stores responses to control messages
- scans 32 line cards for changes in supervision bits. The NT6X54AA stores a message when the card detects a change in state.
- writes new information to the ring multiplexer

The scan chip demultiplexes each 32-channel serial (RD) link on 32 line card buses. The scan chip multiplexes the line card responses on the outgoing (TD) serial links. The multiplex uses a 32-byte connection memory in each scan chip. Each scan chip is accessed in sequence each channel time. One location of the connection memory corresponds to a specified channel time. The address of the line card accessed at that time is in this location. To assign line card numbers to channel times, the system writes to the connection memory with a message written to the chip on RCON. The message has the channel number and the line card address.

Control messages to line cards are written asynchronously following the channel times on the RCON. First, an input first-in-first-out (FIFO) base stores these messages on the scan chip. The messages remain on the scan chip until channel time 0 to 16. Second, the control message is output to the line card. If requested, an output FIFO stores the line card response on the chip. If the input FIFO does not contain control messages, channels 0 and 16 scan line cards. To scan line cards, send an output and idle code to the E99 integrated circuit (IC) on the addressed line card. Compare the state of the supervision bits (SV1, SV0) with the earlier two states of those bits from earlier scans. If two

NT6X54AA (continued)

consecutive scans detect a change, the system loads the address and response of the line card into the output FIFO. The system scans all 32 cards every 4 ms if the system does not send control messages during that time. When the system sends a control message, the scan is on hold for one frame. When the LCM controller outputs the appropriate code on the RCON, the controller can read these scan messages. The controller responses to control messages. This action results in a response on the TCON that consists of one word from the output FIFO. All transactions on RCON and TCON are 20 bits long. The bits contain address (or op-code) and data.

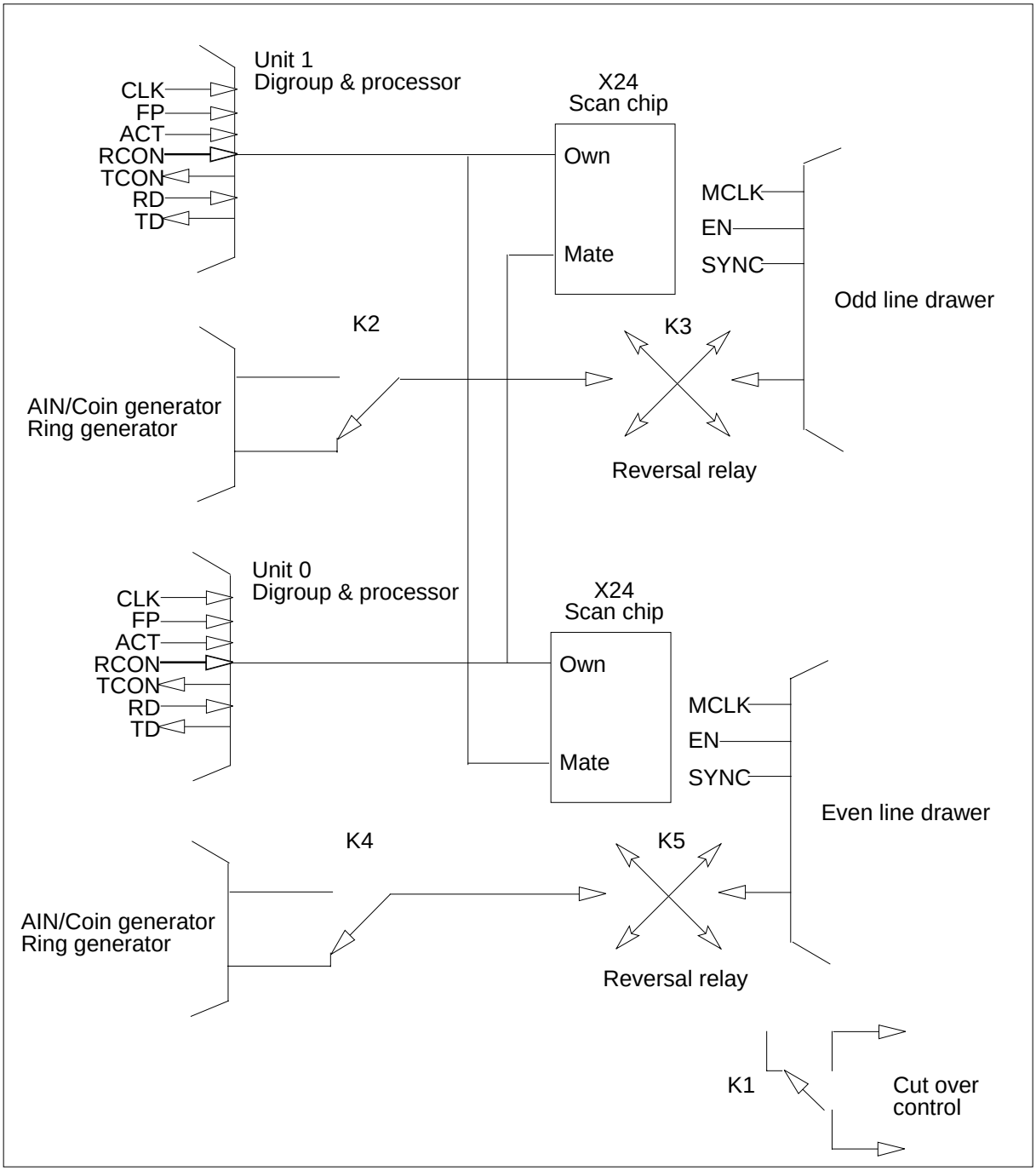
The BIC holds the TCON low to alert the controller that the output FIFO contains a minimum of one word. When the FIFO is empty, the TCON remains high.

The NT6X54AA provides a +12.7V reference to all 64 line positions.

Functional blocks

The relationship between the functional blocks appears in the following figure.

NT6X54AA functional blocks

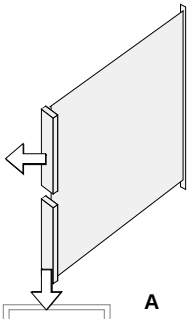


Pin numbers

The pin numbers for the NT6X54AA appear in the following figure.

NT6X54AA (end)

NT6X54AA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	+5 V	+5 V
3A 3B	GND	GND
4A 4B	BUS62	BUS63
5A 5B	BUS60	BUS61
6A 6B	BUS58	BUS59
7A 7B	BUS56	BUS57
8A 8B	BUS54	BUS55
9A 9B	BUS52	BUS53
10A 10B	BUS50	BUS51
11A 11B	BUS48	BUS49
12A 12B	SYNCD	END
13A 13B	VREFD	MCLKD
14A 14B	CUTOB	GND
15A 15B	RGBUS1T	RGBUS1R
16A 16B	GND	GND
17A 17B	+15 V	+15 V
18A 18B	BUS46	BUS47
19A 19B	BUS44	BUS45
20A 20B	BUS42	BUS43
21A 21B	BUS40	BUS41
22A 22B	BUS38	BUS39
23A 23B	BUS36	BUS37
24A 24B	BUS34	BUS35
25A 25B	BUS32	BUS33
26A 26B	GND	GND
27A 27B	SYNCC	ENC
28A 28B	VREFC	MCLKC
29A 29B	CUTOC	GND
30A 30B	CLK1+	CLK1–
31A 31B	FP1+	FP1–
32A 32B	RD1+	RD1–
33A 33B	TD1+	TD1–
34A 34B	RCON1+	RCON1–
35A 35B	TCON1+	TCON1–
36A 36B	ACT1+	ACT1–
37A 37B	ACT0+	ACT0–
38A 38B	RCON0+	RCON0–
39A 39B	TCON0+	TCON0–
40A 40B	TD0+	TD0–

	A	B
41A 41B	RD0+	RD0–
42A 42B	CLK0+	CLK0–
43A 43B	FP0+	FP0–
44A 44B	GND	GND
45A 45B	GND	GND
46A 46B	GND	GND
47A 47B	BUS30	BUS31
48A 48B	BUS28	BUS29
49A 49B	BUS26	BUS27
50A 50B	BUS24	BUS25
51A 51B	BUS22	BUS23
52A 52B	BUS20	BUS21
53A 53B	BUS18	BUS19
54A 54B	BUS16	BUS17
55A 55B	GND	GND
56A 56B	SYNCB	ENB
57A 57B	VREFC	VREFC
58A 58B	CUTOB	GND
59A 59B	GND	GND
60A 60B	BUS14	BUS15
61A 61B	BUS12	BUS13
62A 62B	BUS10	BUS11
63A 63B	BUS8	BUS9
64A 64B	BUS6	BUS7
65A 65B	BUS4	BUS5
66A 66B	BUS2	BUS3
67A 67B	BUS0	BUS1
68A 68B	GND	GND
69A 69B	SYNCA	ENA
70A 70B	VREFA	MCLKA
71A 71B	CUTOA	GND
72A 72B	RGBUS0T	RGBUS0R
73A 73B	GND	GND
74A 74B	RING1T	RING1R
75A 75B	A/C1T	A/C1R
76A 76B	RING0T	RING0R
77A 77B	A/C0T	A/C0R
78A 78B	GND	GND
79A 79B	+5 V	+5 V
80A 80B	GND	GND

NT6X55AB

Product description

The NT6X55AB interface card provides level access for one 64 kbps DS-0 link in the digital trunk controller (DTC).

A DTC with NT6X55AB cards in a signal switching point (SSP) office has CCS7 link access to a signal transfer point (STP) node. This access is through the DS-0. The link access is direct or indirect through the channel bank dataport. The DS-0 interface on the SSP node can respond to loopback requests the network initiates.

Location

The NT6X55AB occupies the same common peripheral controller (CPC) shelf slot as the NT6X50 (AA or BA). The DTC can contain from one to ten cards.

Functional description

The NT6X55AB card performs the following five functions:

- provides the termination for a DS-0 56 kbps or 64 kbps CCS7 link
- terminates the composite clock (CC) input to provide the clock timing for the DS-0 link
- generates the CC applications that involve back-to-back DS-0 data links
- responds to latching loopback requests from the DS-0 link
- provides the interface between the terminated DS-0 data link and the DS60 interface to the CPC in the DTC

Functional blocks

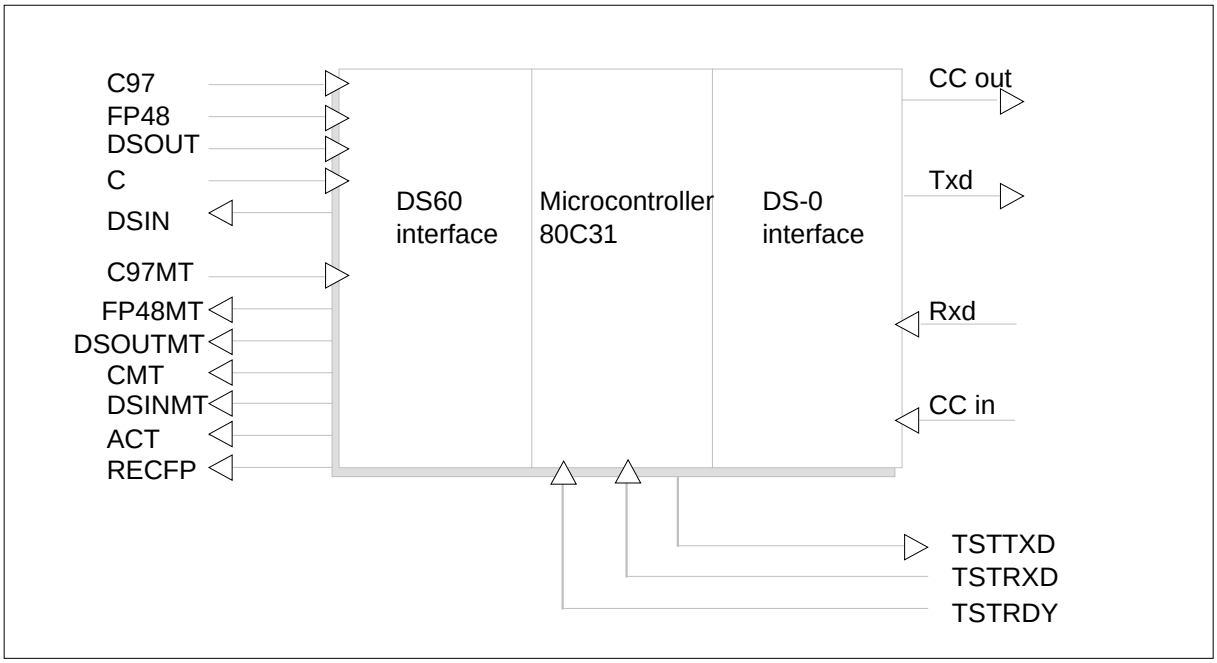
The NT6X55AB contains the following three functional blocks:

- the DS60 interface
- microcontroller
- DS-0 interface

The relationship between functional blocks appears in the following figure.

NT6X55AB (continued)

NT6X55AB functional blocks



DS60 interface

The DS60 is the interface between the DS-0 interface and the time switch card, NT6X44. The DS-0 interface has the following eight functions:

- receives DS60 data from the active CPC plane on port 0
- transmits DS60 data on the active CPC plane on port 0
- provides continuous loopback to the DS60 bus of incoming channel 12 (DSOUT) to outgoing channel 16 (DSIN). This action is for the active and the inactive bus
- multiplexes the data from the DS-0 interface block to port 0 of the DS60 bus
- separates the data from port 0 of the DS60 bus to the DS-0 interface block
- generates a local clock for the DS-0 interface block when the block operates in DCE mode
- monitors the backplane for power and switches to the backup supply if a power failure occurs
- provides a loopback to the DS-0 interface block of the data and status channels the DS-0 controls

Microcontroller

The microcontroller is the interface between the DS60 and the DS-0 interface blocks. The microcontroller has the following five functions:

- supports the control and status register interface
- controls data transfers between the DS60 and DS-0 interface
- provides a remote loopback from the DS-0 data stream to the transmit DS-0 data stream
- connect a terminal interface to the microcontroller through the backplane provides for a self-test
- use the same interface to provide for bit error rate testing (BERT)

DS-0 interface

The DS-0 interface is the interface between the microcontroller and the DS-0 link. The DS-0 has the following five functions:

- provides bipolar-to-unipolar conversion for receive data
- provides unipolar-to-bipolar conversion for transmit data
- provides a local loopback from the transmit DS-0 data stream to the receive DSO data stream on the bipolar line
- detects clock loss
- detects bipolar violation on the receive DS-0 data stream

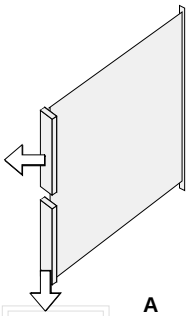
Signaling

Pin numbers

The pin numbers for the NT6X55AB appear in the following figure.

NT6X55AB (continued)

NT6X55AB pin numbers

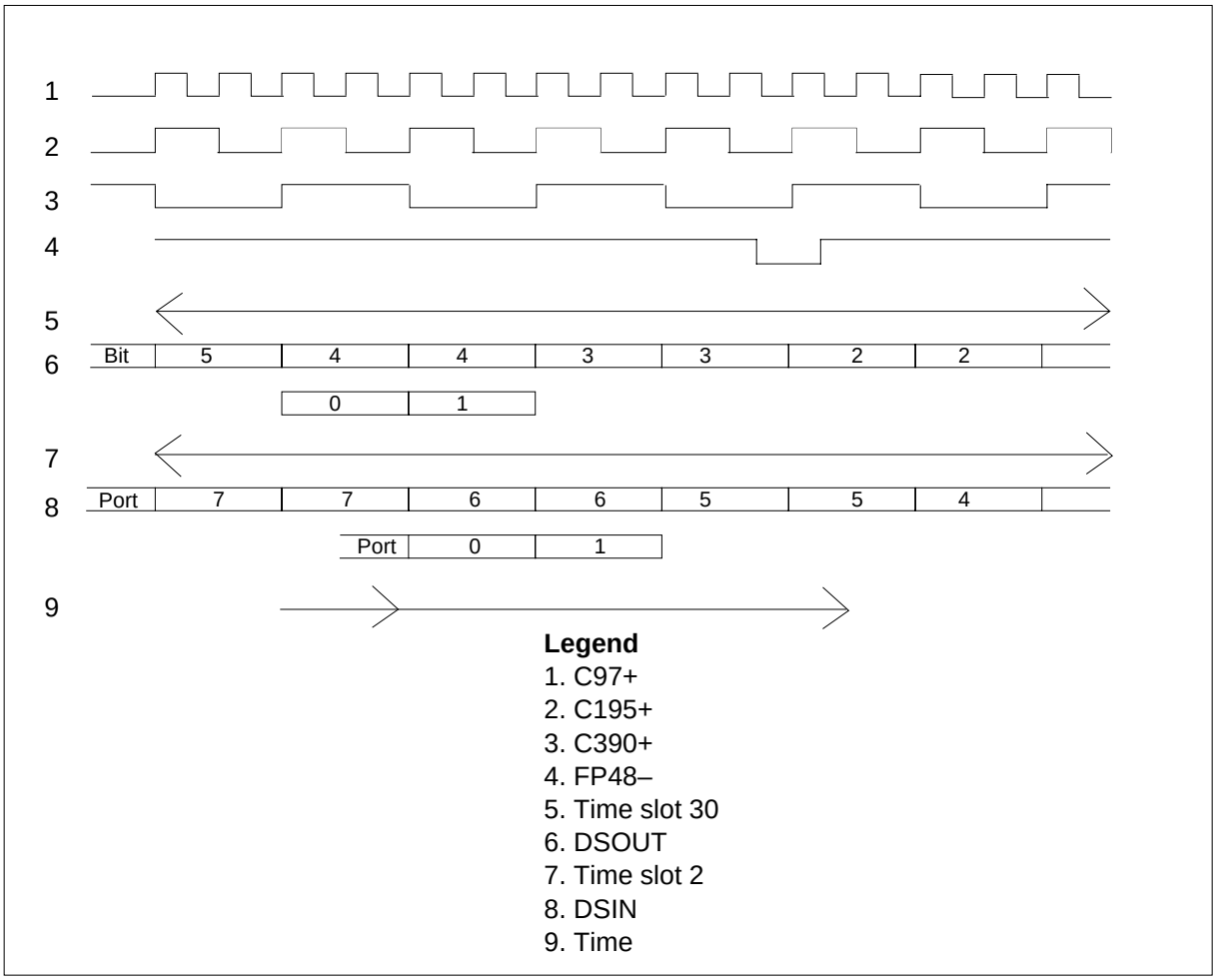


	A	B
1A 1B	Gnd	Gnd
2A 2B	+5V	+5V
3A 3B	+5V	+5V
4A 4B	+5VMT	+5VMT
5A 5B	Gnd	Gnd
6A 6B		C97
7A 7B		
8A 8B	ACT	
9A 9B	FP48	FP48MT
10A 10B		
11A 11B	TXT	TXR
12A 12B	CCOUTT	CCOUTR
13A 13B		
14A 14B		
15A 15B		
16A 16B		
17A 17B	C97MT	
18A 18B		
19A 19B	DSOUT	DSOUTMT
20A 20B		
21A 21B		
22A 22B		
23A 23B		
24A 24B		
25A 25B		
26A 26B		
27A 27B		
28A 28B		
29A 29B		
30A 30B		
31A 31B		
32A 32B		
33A 33B		
34A 34B		
35A 35B	TSTTXD	TSTRXD
36A 36B	TERMEN	
37A 37B		
38A 38B		
39A 39B		
40A 40B		

	A	B
41A 41B		
42A 42B		
43A 43B		
44A 44B		
45A 45B		
46A 46B		
47A 47B		
48A 48B		
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B		
58A 58B		
59A 59B		
60A 60B		
61A 61B		
62A 62B		
63A 63B		
64A 64B		
65A 65B		
66A 66B		
67A 67B		
68A 68B		
69A 69B	C	CMT
70A 70B	RECFPR	
71A 71B	+12PWRMT	–12PWRMT
72A 72B	RXT	RXR
73A 73B	CCINT	CCINR
74A 74B	RECFP	RECFPMT
75A 75B	DSIN	DSINMT
76A 76B		
77A 77B	+12PWR	+12PWR
78A 78B		
79A 79B	–12PWR	–12PWR
80A 80B	Gnd	Gnd

The timing of NT6X55AB appears in the following table.

NT6X55AB timing



Electrical requirements

The interface dc and ac specifications for the NT6X55AB appear in the following tables.

DS60 interface dc specifications (Sheet 1 of 2)

Dc specification	Minimum	Maximum	Units
Input voltage low	-0.5	0.8	V
Input voltage high	2.0	7.0	V

NT6X55AB (continued)

DS60 interface dc specifications (Sheet 2 of 2)

Dc specification	Minimum	Maximum	Units
Input current low (except DSOUT, DSOUTM)		200.0	µA
Input current low		20.6	mA
Input capacitance		100.0	pF
Input current high		40.0	µA
Output voltage low	-0.5	0.4	V
Output voltage high	3.0	7.0	V
Output current log		30.0	mA
Output current high		400.0	µA
Output capacitive		100.0	pF
Output capacitance drive	400.0		pF

DS60 interface ac specifications

Ac specification	Minimum	Maximum	Units
C97 period	93	101	ns
C97 period low	39	59	ns
C97 period high	39	59	ns
C97 low to FP48 low	-6	34	ns
C97 low to FP48 high	-6	34	ns
C97 high to DSOUT stable	17.1	81.4	ns
C97 high to DSIN stable	5.9	61.4	ns

The power requirements for the appear in the following table.

NT6X55AB power requirements

Voltage	Current	Power
+5	900mA MAX 600mA TYP	4.5W MAX 3.0W TYP
+12	50mA MAX 35mA TYP	0.6W MAX 0.42W TYP
-12	40mA MAX 25mA TYP	0.48W MAX 0.3W TYP
Total		5.58W MAX 3.22W TYP

NT6X55BA

Description

The NT6X55BA 64 kbit access circuit pack provides level access. The NT6X55BA provides access for one (CCITT) G.703 64 kbps contradirectional interface in the PCM30 digital trunk controller (PDTC).

A PDTC that contains NT6X55BA circuit packs provides access to timeslot 1 of the port 0 DS60 data. The composite clock input is present only because the circuit pack is based on the NT6X55AB.

Location

The NT6X55BA circuit pack occupies the same shelf slot in a common peripheral controller (CPC) as the NT6X27 (AA, AC, or BA). The PDTC can contain one to eight circuit packs.

Functional description

The NT6X55BA provides the following functions:

- provides the termination for a G.703 64 kbps data link.
- terminates a composite clock (CClk) input and provides the clock timing for the 64 kbps link. This function is for tests.
- provides the CClk outputs for a 64 kbps contradirectional interface as timing for the transmit and receive data.
- responds to latching loopback requests from the 64 kbps link.
- provides the interface between the terminated 64 kbps link and the DS60 interface to the CPC of the PDTC.

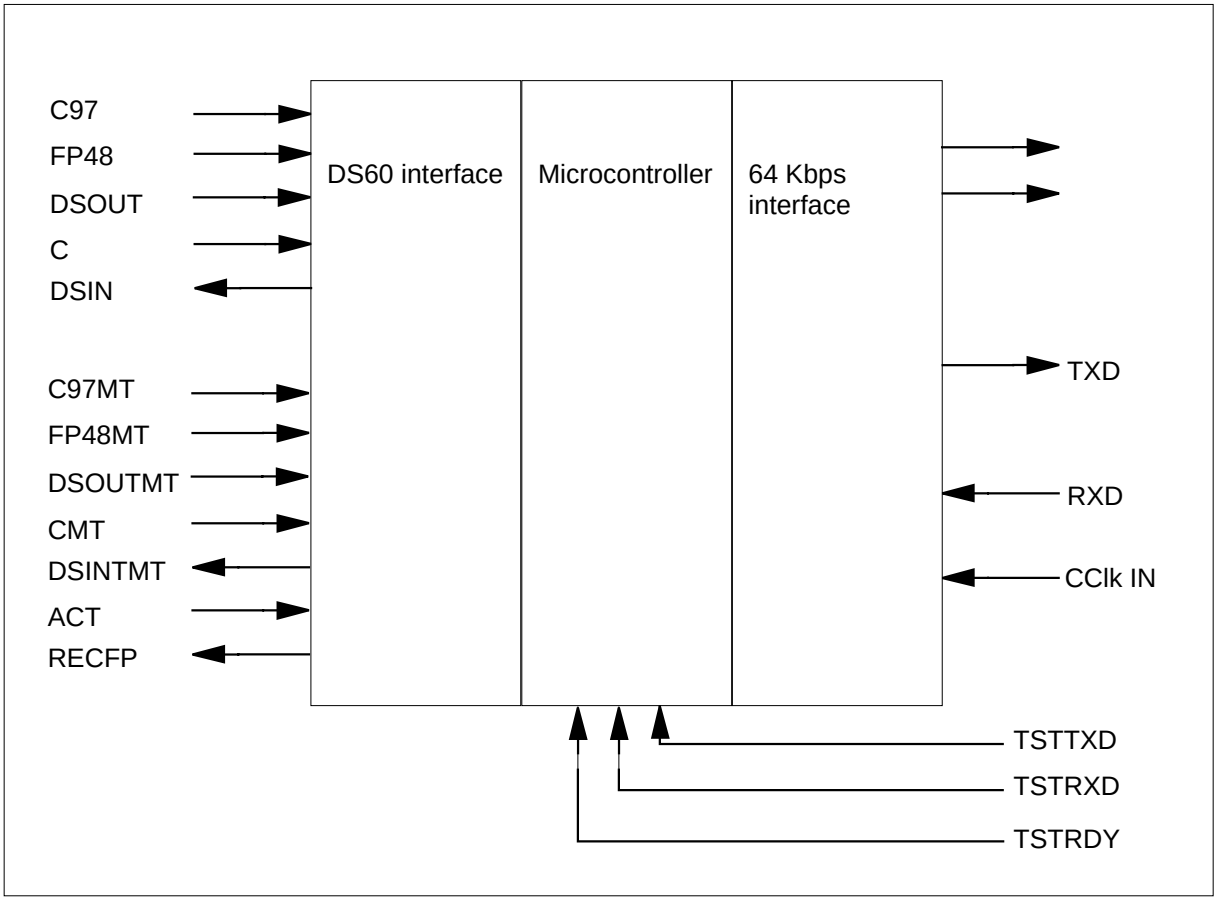
Functional blocks

The NT6X55BA contains the following functional blocks:

- DS60 interface
- microcontroller
- 64 Kbps interface

The functional blocks appear in the following figure.

NT6X55BA functional blocks



DS60 interface

The DS60 interface block provides an interface between the 64 kbps interface and the NT6X44 time switch card. The DS60 interface has the following functions:

- receives DS60 data on port 0 from the active CPC plane
- transmits DS60 data on port 0 of the active CPC plane
- provides continuous loopback to the DS60 bus of incoming channel 12 (DSOUT) to outgoing channel 16 (DSIN). This loopback is for the active bus and the inactive bus.
- multiplexes the data from the 64 kbps interface block to port 0 of the DS60 bus
- separates the data from port 0 of the DS60 bus to the 64 kbps interface block

NT6X55BA (continued)

- generates a local clock for the 64 kbps interface block. The DS60 generates this clock when the block operates in the normal mode of operation digital carrier equipment (DCE mode).
- monitors the backplane for power, and switches over to the emergency supply if a power failure occurs
- provides a loopback to the 64 kbps interface block of the data and status channels that the 64 kbps interface controls. This loopback allows stand-alone tests of the 64 kbps block and the main part of the DS60 interface block.

Microcontroller

The microcontroller provides the interface between the DS60 and the 64 kbps interface blocks. The microcontroller has the following functions:

- supports the control and status register interface.
- controls data transfers between the DS60 and 64 kbps interface
- provides a remote loopback. This loopback loops the 64 kbps data stream that the system receives to the 64 kbps data stream the system transmits. The loopback occurs in the microcontroller.
- allows a connecting terminal interface test that tests the interface to initiate to the microcontroller through the backplane

64 kbps interface

The 64 kbps interface provides communication between the microcontroller and the 64 kbps link. The 64 kbps interface has the following functions:

- provides bipolar-unipolar conversion for receive data
- provides unipolar-bipolar conversion for transmit data
- provides a local loopback. This loopback is from the 64 kbps data stream that the system receives to the 64 kbps data stream the system transmits. The data stream is on the bipolar line.
- detects clock loss
- detects bipolar violation on the 64 kbps data stream that the system receives
- provides two identical transmit clocks for the G.703 contradirectional interface (TCCLK and RCCLK)

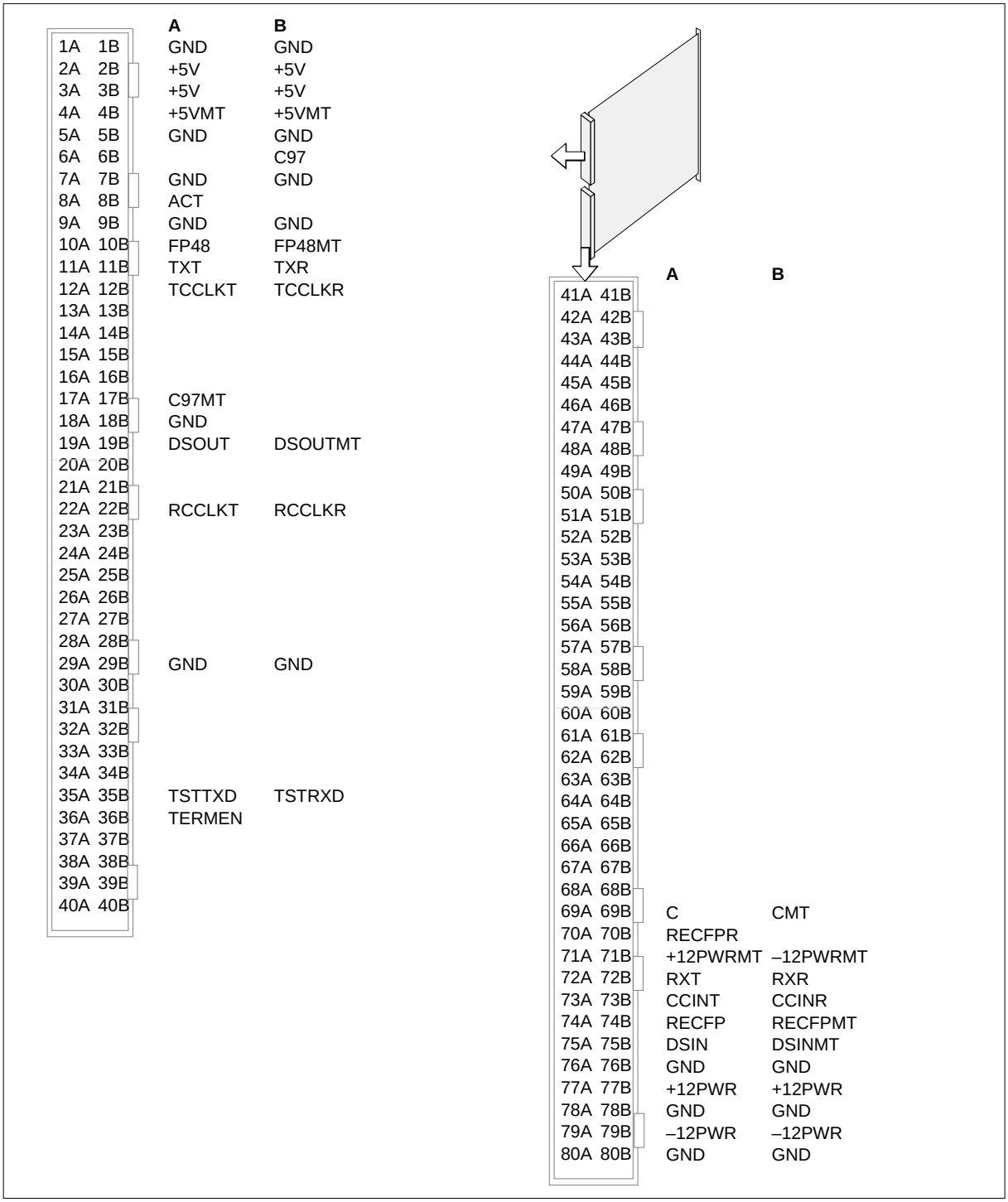
Signaling

Pin numbers

The pin numbers for NT6X55BA appear in the following figure.

NT6X55BA (continued)

NT6X55BA pin numbers



NT6X55BA (continued)

Electrical requirements

The interface dc and ac specifications for the NT6X55BA appear in the following tables

DS60 interface dc specifications

dc specifications	Minimum	Maximum	Units
Input voltage low	-0.5	0.8	V
Input voltage high	2.0	7.0	V
Input current low (except DSOUT, DSOUTM)		200.0	µA
Input current low		20.6	mA
Input capacitance		100.0	pF
Input current high		40.0	µA
Output voltage low	-0.5	0.4	V
Output voltage high	3.0	7.0	V
Output current low		30.0	mA
Output current high		400.0	µA
Output capacitance		100.0	pF
Output capacitance drive	400.0		pF

DS60 interface ac specifications

ac specification	Minimum	Maximum	Units
C97 period	93	101	ns
C97 period low	39	59	ns
C97 period high	39	59	ns
C97 low to FP48 low	-6	34	ns
C97 low to FP48 high	-6	34	ns
C97 high to DSOUT stable	17.1	81.4	ns
C97 high to DSIN stable	5.9	61.4	ns

The power requirements for the NT6X55BA appear in the following table.

NT6X55BA Power requirements

Voltage	Current	Power
+ 5	900 mA MAX 600 mA TYP	4.5W MAX 3.0W TYP
+ 12	50 mA MAX 35 mA TYP	0.6W MAX 0.42W TYP
-12	40 mA MAX 25 mA TYP	0.48W MAX 0.3W TYP
Total		5.58W MAX 3.72W TYP

NT6X55CA

Description

The NT6X55CA 8-port 64 Kbit interface card provides eight 64 kbps links. These links are in a single card slot in a PCM30 digital trunk controller (PDTC). The links can be Bellcore DS0 or CCITT levels.

Current use and cable limits allow the PDTC to have one interface card. This limit applies when the cabinetized international line group controller/international digital trunk controller (ILGC/IDTC) frame uses the card.

The NT6X55CA has the following features:

- eight links that are set separately with manual switches
- each link has two transmit (TX) clock circuits and two receive (RX) clock circuits that allow the use of six interface types
- separate control and status registers control each link
- the clock sources that TX and RX use are monitored separately
- a switch (S1) on the board controls the received clock the system uses for each of the eight links. This system uses this switch in link peripheral processor (LPP) applications. When the four even-numbered links or all eight links can be configured to run from a common clock
- a clock detect circuit controls the common clock source. This feature allows the establishment of synchronous islands of NT6X55CA cards and LPPs without the use of a timing signal generator (TSG)

The NT6X55CA is not backward compatible with the NT6X55AB card or the NT6X55BA card.

Location

The original release of NT6X55CA was for use in the cabinetized NTFX33AA ILGC/IDTC frame. The ISFX33AA interconnect schematic allows provisioning of one card for each module: position 19, slot 1 in module 0, and position 47, slot 1 in module 1. The backplane signals move from the NT6X55CA to four 37-pin, D-type connectors on the bulkhead.

Functional description

The NT6X55CA provides level access for eight 64 kbps links in the PCM30 PDTC. You can use manual switches on the card to set the 64 kbps interfaces to Bellcore DS0 or CCITT levels.

Timeslot 0 carries control and status data to and from the NT6X69 messaging card. The software feature for the NT6X55CA, AE0934, is for a PDTC. When the correct software is available, the NT6X55CA can operate in a digital trunk controller (DTC). The NT6X55CA can operate in a DTC because the feature does not require access to timeslot 16.

Functional blocks

The NT6X55CA contains the following functional blocks:

- DS60 interface
- S46 application-specific integrated circuit (ASIC)
- analog interface
- switch setting
- clock control

The relationship between the functional blocks appears in the following figure.

DS60 interface

The DS60 interface selects the correct activity signal (C97, FP48, DSOUT or an MT signal). The DS60 sends the signal to the S46 ASICs. The DS60 interface sends the active DS60 signal to both ASICs for demultiplexing for additional transmission to DS30 data streams. A select input on each ASIC determines which DS30 signal to use.

The DS30 signals from the ASICs are multiplexed to the DSIN/DSINMT data streams. The DS60 interface sends the DS30 signals to the backplane.

S46 application-specific integrated circuit

The S46 ASICs handle a maximum of four 64 Kbps channels. The operation of the S46 ASICs complies with Bellcore or CCITT standards. The NT6X55CA has two ASICs. One ASIC is for even-numbered links and one ASIC is for odd links. An input on each ASIC decides if the ASIC acts on the even or the odd part of the DSOUT signal.

Analog interface

The analog interface for each port has three identical drivers and three identical receivers. The driver circuit takes the POS and NEG signals from an S46. The driver circuit converts the signals to balanced line signals, on the line side of the transformer. The receiver uses a dual comparator circuit to determine if line signals from the transformer are POS signals or NEG signals.

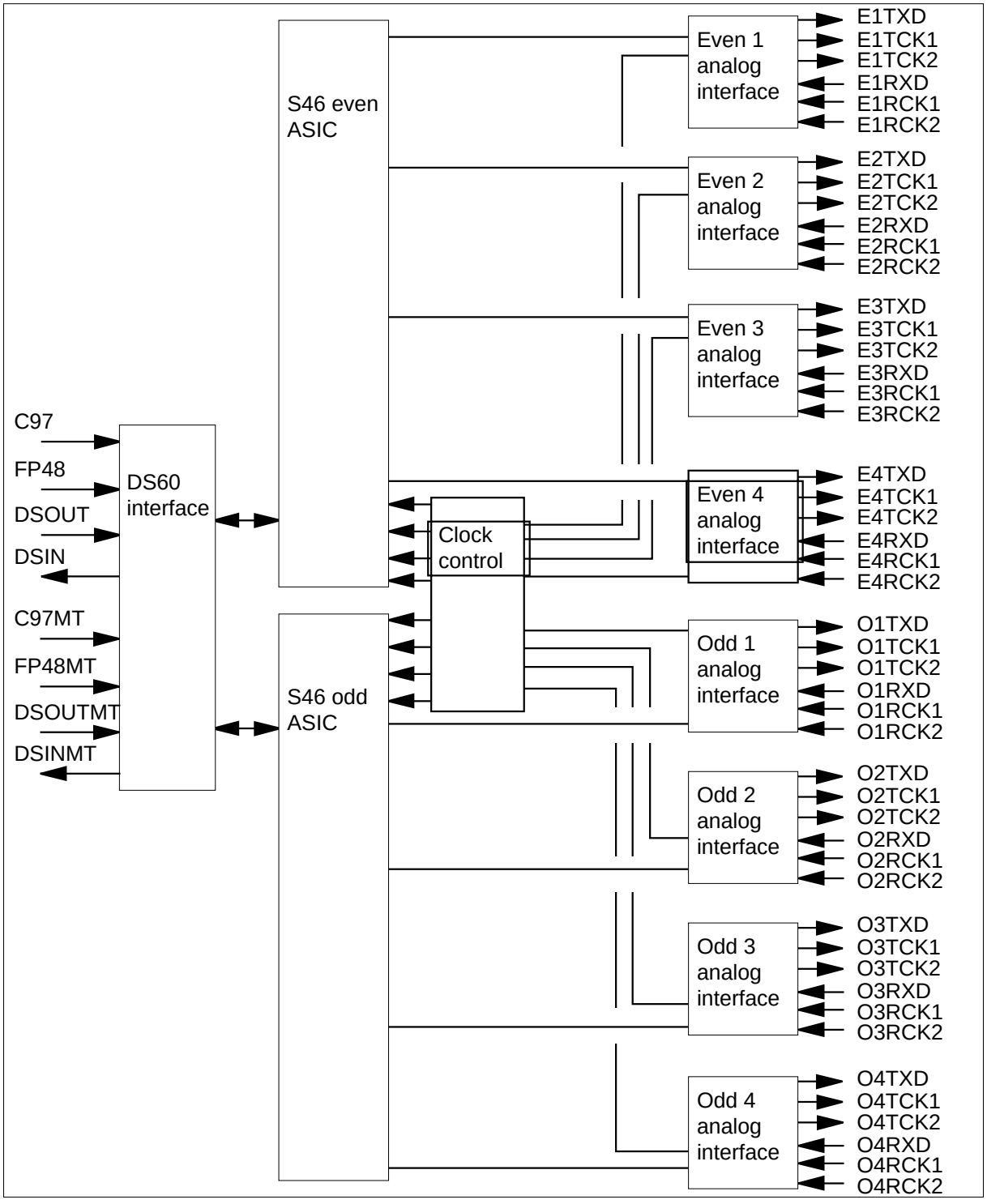
NT6X55CA (continued)

The driver block is a bipolar circuit with two high-current transistor switches that are transformer-coupled to the line. Surge protectors protect the output stage of the driver block from transient input signals.

The receiver block terminates the clock or data balanced signals from the line signal. This bipolar circuit is transformer-coupled and has a high-speed comparator with a low-pass filter to reduce noise. The input to the receiver block is diode-clamped to prevent overload. The output is POS and NEG signals.

NT6X55CA (continued)

NT6X55CA functional blocks



NT6X55CA (continued)

Switch setting

The NT6X55CA has 17 switches. The switches must be set before you power up the card.

Switches S2 to S17 control the electrical level of the data and clock interfaces. The switches are arranged in eight pairs on the circuit board. The circuit board has one pair of switches for each interface. Text appears on the board next to the backplane connector. This text indicates which pair of switches relates to interfaces Even 1, Even 2, Even 3, Even 4, and Odd 1. The rest of the switches follow in sequence.

An arrow and text next to each pair of switches indicates the ON position for the switches. Text appears next to the backplane connector. This text indicates that the ON position is for Bellcore level interfaces, and the OFF position is for CCITT level interfaces. If you move the switches, the resistors connect and disconnect. These resistors adjust the voltage levels of the transmit signals. These resistors adjust the threshold levels of the receive circuits in the analog interface blocks.

Switch S1 controls the clock select circuit, and separate actuators on S1 control the Even and Odd interfaces. The arrow on the board is the OFF position of each actuator. When the actuator is in the OFF position, the interfaces that the actuator control use the same clock. The text on the board identifies LPP for this configuration.

The NT6X55CA text identifies LPP because of the first use of the card. The first use of the card was in an application in which the data links connected to an LPP in an island configuration. In the island configuration, all links on each card have the S1 switch set to LPP. This configuration allows all data links to use the same clock.

Clock control

The clock control block determines the source of the common clock. The clock control circuits is active if one or both actuators on switch S1 are set to LPP. This condition causes some or all of the data links to use a common clock.

This block has clock-detect circuits. When switch S1 is set, the two clock inputs to the board are E1RCK1 and E1RCK2. Each clock input has a shift register that can detect negative pulses. The register identifies the loss of five consecutive negative pulses as an indication of clock failure. The programmable array logic (PAL) uses E1RCK1 if E1RCK1 is available, and E1RCK2 if E1RCK2 is available. If E1RCK2 fails the PAL uses the clock that PAL generates.

The connects to LIUs in an LPP with DS0 interfaces, and connects to test equipment with CCITT contradirectional interfaces. For robust DS0 links, a timing signal generator must clock the LPP and the NT6X55CA.

Technical data

Description

The NT6X55CA is a six-layer, standard size DMS-100 printed circuit board.

Technology

The NT6X55CA has one PAL device. All components are preference level three or higher. The NT6X55CA uses auto-insertable components when possible. The has two S46 ASICs packaged in 120-pin pin grid array (PGA) style.

Power requirements

The power requirements for the appear in the following table. The supply on the backplane can be as low as 4.75V.

Power requirements of the NT6X55CA

Parameter	Minimum	Nominal	Maximum	Units
+5V SUPPLY				
Supply voltage	4.75	5.00	5.25	volts
Supply ripple	not known	0.05	not known	volts
Supply current	0.50	0.70	1.00	amperes
+12V SUPPLY				
Supply voltage	11.75	+12.0	+12.20	volts
Supply ripple	not known	0.10	not known	volts
Supply current	0.50	1.10	1.20	amperes
-12V SUPPLY				
Supply voltage	12.25	-12.00	-11.70	volts
Supply ripple	not known	0.10	not known	volts
Supply current	0.06	0.08	0.10	amperes

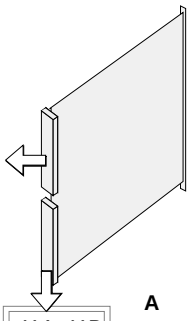
NT6X55CA (continued)

Signaling

Pin numbers

The pin numbers for the NT6X55CA appear in the following figure.

NT6X55CA pin numbers



	A	B
1A 1B	GN D	GND
2A 2B	+5V	+5V
3A 3B	+5V	+5V
4A 4B	+5VMT	+5VMT
5A 5B	GND	GND
6A 6B		C97
7A 7B	GND	GND
8A 8B	ACT	
9A 9B	GND	GND
10A 10B	FP48	FP48MT
11A 11B		
12A 12B		
13A 13B		
14A 14B		
15A 15B		GND
16A 16B	E1TXDP	
17A 17B	C97MT	E1TXDN
18A 18B	GND	E1TCK1P
19A 19B	DSOUT	DSOUTMT
20A 20B	GND	E1TCK1N
21A 21B		
22A 22B	E1TCK2P	E1TCK2N
23A 23B	E1RXDP	E1RXDN
24A 24B	E1RCK1P	E1RCK1N
25A 25B	E1RCK2P	E1RCK2N
26A 26B	E2TXDP	E2TXDN
27A 27B	E2TCK1P	E2TCK1N
28A 28B	E2TCK2P	E2TCK2N
29A 29B	E2RXDP	E2RXDN
30A 30B	E2RCK1P	E2RCK1N
31A 31B	E2RCK2P	E2RCK2N
32A 32B	E3TXDP	E3TXDN
33A 33B	E3TCK1P	E3TCK1N
34A 34B	E3TCK2P	E3TCK2N
35A 35B	E3RXDP	E3RXDN
36A 36B	E3RCK1P	E3RCK1N
37A 37B	E3RCK2P	E3RCK2N
38A 38B	E4TXDP	E4TXDN
39A 39B	E4TCK1P	E4TCK1N
40A 40B	E4TCK2P	E4TCK2N

	A	B
41A 41B	E4RXDP	E4RXDN
42A 42B	E4RCK1P	E4RCK1N
43A 43B	E4RCK2P	E4RCK2N
44A 44B	O1TXDP	O1TXDN
45A 45B	O1TCK1P	O1TCK1N
46A 46B	O1TCK2P	O1TCK2N
47A 47B	O1RXDP	O1RXDN
48A 48B	O1RCK1P	O1RCK1N
49A 49B	O1RCK2P	O1RCK2N
50A 50B	O2TXDP	O2TXDN
51A 51B	O2TCK1P	O2TCK1N
52A 52B	O2TCK2P	O2TCK2N
53A 53B	O2RXDP	O2RXDN
54A 54B	O2RCK1P	O2RCK1N
55A 55B	O2RCK2P	O2RCK2N
56A 56B	O3TXDP	O3TXDN
57A 57B	O3TCK1P	O3TCK1N
58A 58B	O3TCK2P	O3TCK2N
59A 59B	O3RXDP	O3RXDN
60A 60B	O3RCK1P	O3RCK1N
61A 61B		
62A 62B	O3RCK2P	O3RCK2N
63A 63B	O4TXDP	O4TXDN
64A 64B	O4TCK1P	O4TCK1N
65A 65B	O4TCK2P	O4TCK2N
66A 66B	O4RXDP	O4RXDN
67A 67B	O4RCK1P	O4RCK1N
68A 68B	O4RCK2P	O4RCK2N
69A 69B		
70A 70B		
71A 71B	+12PWRMT	–12PWRMT
72A 72B		
73A 73B		
74A 74B		
75A 75B	DSIN	DSINMT
76A 76B	GND	GND
77A 77B	+12PWR	+12PWR
78A 78B	GND	GND
79A 79B	–12PWR	–12PWR
80A 80B	GND	GND

NT6X55JA

Description

The NT6X55JA is a digital trunk controller (DTC) common interoffice interface (CII) and common metallic interface (CMI) card. The JPN7 network uses the NT6X55JA with the DMS switch with Common Channel Signaling 7 (CCS7).

The NT6X55JA resides in a domestic type DTC. The CII conveys call supervision and signaling information between the DMS and the JPN7 network. The CMI provides connection to test systems and to protocol analyzers.

The NT6X55JA is not backward compatible with earlier suffixes of the NT6X55.

Location

The NT6X55JA occupies one slot in a DTC. The location of the NT6X55JA are positions 1, 2, 3, 4, or 5, on shelf 0 or shelf 1.

You can add this card to the shelf configuration. Consider this addition in relation to the power current rating of the shelf power converter.

Functional description

The primary function of the NT6X55JA is the conversion of data from DS60 format to CII format or CMI format. Additional functions include looparounds, self-tests, error counts, and control functions. These functions support and maintain the primary function.

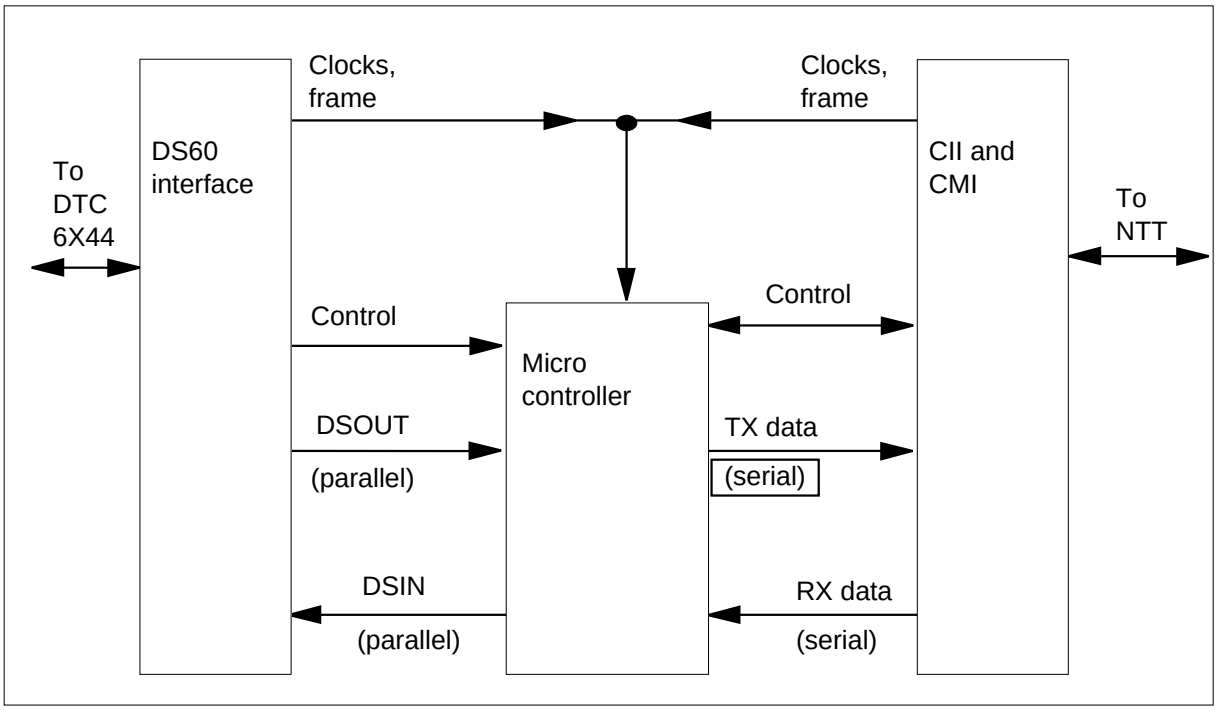
Functional blocks

The NT6X55JA contains the following functional blocks:

- DS60 interface
- microcontroller
- CII/CMI

The relationship between the functional blocks appears in the following figure.

NT6X55JA functional blocks



DS60 interface

The DS60 interface contains two blocks:

- DS60 OUT interface, from the DTC to the CII/CMI
- DS60 IN interface, from the CII/CMI to the DTC

The DS60 OUT interface provides control, clock, and DSOUT data to the microcontroller and the CII/CMI. The DS60 OUT interface provides this data in parallel format. This data is for internal use and transmission to the CII or CMI ports.

The DS60 IN interface takes data and state information from the microcontroller and the CII/CMI. The DS60 IN interface takes this data in parallel format. The DS60 IN takes clock data from DS60 OUT interface. The DS60 IN interface sends the information and data through the DS60 channels and the 6X44 time switch. The DS60 IN takes the data from the DTC to a link interface unit (LIU) through a DS30 link. The DS60 IN also takes data from a message switch and buffer (MSB) through a DS30 link.

NT6X55JA (continued)

Microcontroller

The microcontroller moves control and state information, and data between the DS60 interface and the CII/CMI. The microcontroller performs microcontroller test diagnostics on that microcontroller and on the equipment that attaches to the microcontroller.

Common interoffice interface and common metallic interface

The CII/CMI converts data from parallel to serial formats, and from NRZ format to CII or CMI format.

The CII/CMI:

- generates or receives CII and CMI clocks
- monitors clock and data streams
- provides clock and data loopback functions

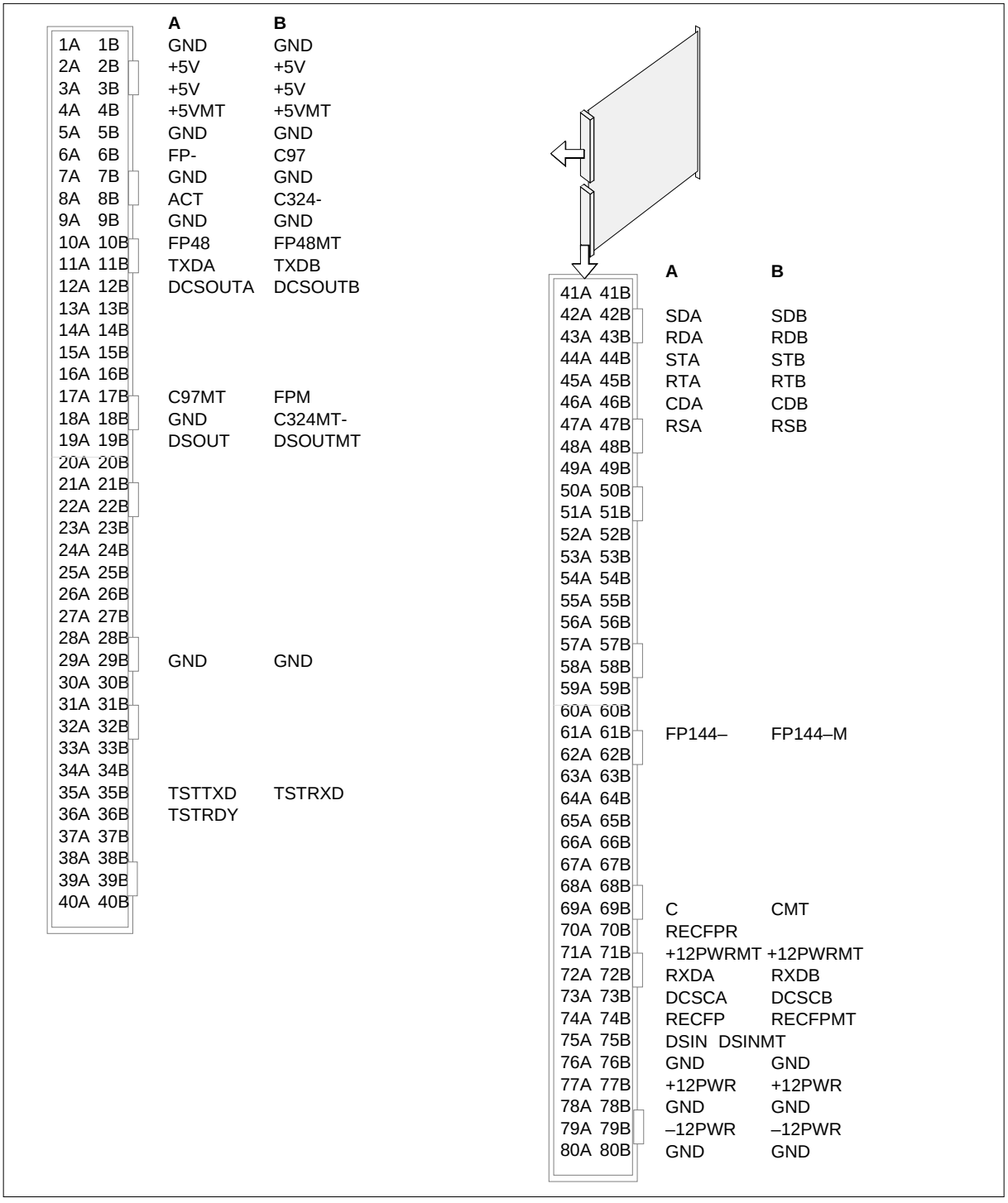
Signaling

Pin numbers

The pin numbers for the NT6X55JA appear in the following figure.

NT6X55JA (continued)

NT6X55JA pin numbers



NT6X55JA (continued)

Technical data

The CII and CMI specifications for direct current (dc) and alternating current (ac) appear in the following tables.

CII interface specifications

dc specification	Minimum	Maximum	Units
Input voltage 1+	0.63	1.1	V
Input voltage 1-	-1.1	-0.63	V
Input voltage 0	-0.1	0.1	V
Output voltage 1+	0.9	1.1	V
Output voltage 1-	-1.1	-0.9	V
Output voltage 0	-0.1	0.1	V
Input impedance	90	130	ω

CII interface specifications

ac specifications	Minimum	Maximum	Units
Output impedance	90	130	ω
CII pulse width	14.0	18.8	µs
DCS pulse width	7.0	9.4	µs
DCS frequency (must match frame rate of switch)	63.9999	64.0001	kHz
DCS frame frequency (must match frame rate of switch)	7.9999	8.0001	kHz
CII rise and fall time, 0% to 50%	0.0	2.4	µs
DCS rise and fall time, 0% to 50%	0.0	1.2	µs
DCS+ to CII RXD+	1.9	5.9	µs
DCS+ to CII TXD+	0.5	1.9	µs

CMI interface specifications

ac specifications	Minimum	Maximum	Units
Input voltage differential logic high	0.2	7	V
Input voltage differential logic low	–7	–0.2	V
Input voltage common mode	–7	7	V
Input impedance	95	105	ω
Output voltage differential logic high	2.0	5.0	V
Output voltage differential logic low	–5	–2.0	V
Output voltage common mode	–7	7	V
Output impedance	21	145	ω

CMI interface specifications

ac specifications	Minimum	Maximum	Units
ST or RT frequency (must equal 0.75 bit rate of switch)	47.9999	48.0001	kHz
ST or RT period high	6.0	10.0	µs
ST or RT period low	6.0	45.0	µs
SD or RD period high	15.0	--	µ s
SD or RD period low	15.0	--	µs
ST to SD	–0.100	0.100	µ s
RT to RD	–0.100	1.0	µ s

NT6X55JA (end)

Power requirements

The power requirements for the appear in the following table.

+ 5Vsupply

Parameter	Minimum	Nominal	Maximum	Units
Supply voltage	4.75	5.00	5.25	V
Supply current	1.10	1.20	1.30	A

-12V supply

Parameter	Minimum	Nominal	Maximum	Units
Supply voltage	–12.25	–12.00	–11.75	V
Supply current	8.00	10.00	12.00	mA

+12V supply

Parameter	Minimum	Nominal	Maximum	Units
Supply voltage	+11.75	+12.00	+12.25	V
Supply current	12.00	18.00	24.50	mA

Total of tables above

Parameter	Minimum	Nominal	Maximum	Units
Total power	5.50	6.34	7.27	W

NT6X60AA

Description

The NT6X60AA contains two cards. The NT6X38 is for ringing control. The NT6X37 is for ringing amplification. Ringing signals start in the NT6X38. The NT6X37 amplifies the ringing signals to the necessary output level.

Location

The NT6X60 operates with the NT6X25 remote line concentrating equipment (RLCE) frame supervisory panel (FSP). The NT6X60 mounts in the host interface equipment (HIE) shelf in the RLCE.

Functional description

The NT6X60AA generates ringing signals and dc voltages for automatic number identification (ANI) and coin functions. Operating company personnel set the frequency and amplitude of ringing waveforms manually. Operating company personnel use dual inline package (DIP) switches or straps to set the frequency and amplitude to meet telephone company requirements.

Ringing control NT6X38

The NT6X38 performs the following functions:

- generates ringing signal
- provides ANI and coin outputs
- monitors ring bus output
- synchronizes dc-to-dc converters
- provides auxiliary supply

Generating ringing signal

The waveform store PROM holds a digital representation of a single cycle of each ringing waveform. The control logic selects the correct timing, frequency, and amplitude to correspond to the manual settings. Output from the waveform store passes through the digital-to-analog converter and the low-pass filter. This process provides the analog input signal for the ringing amplifier card.

Providing ANI and coin outputs

A single dc-to-dc converter provides ±48V output for ANI functions and ±130V output for coin functions.

Monitoring ring bus output

The NT6X38 monitors ring bus output from the NT6X37 for output voltage and current. If the NT6X38 detects a ringing overvoltage, the NT6X38 signals the NT6X37 to shut down the amplifier. If the NT6X38 detects an ANI or coin

NT6X60AA (continued)

overvoltage, the NT6X38 signals the NT6X37 to shut down the appropriate converter. If both types of overvoltage occur, the FSP disconnects primary power.

The monitor circuit provides transistor-transistor logic (TTL)-level status signals to the LCM processor. These signals indicate ringing voltage (RMS), ringing current (CUR), and low ANI or coin voltage (ACT). These signals are combined with three state bits from the control logic, AFO, AF1, and XOVER. The monitor circuit sends the signals through a serial data link to provide isolation of the ground reference.

Synchronization of dc-to-dc converters

The dc-to-dc converters in the NT6X37 must be synchronized to the LCM system clock. The converter requires 48 kHz synchronization, and the LCM provides 64 kHz synchronization. A phase-locked loop converts the frequency. The card provides dc isolation of the grounds between the RLCM synchronization feed and the NT6X37 synchronization input.

Auxiliary supply

A small dc-to-dc converter supplies ±15 Vand +5V for the internal circuits of the NT6X38. The control circuits on the NT6X37 use the supply of ±15V.

Ringing amplifier NT6X37

The NT6X37 amplifier is a dc-coupled class B type, which uses power field-effect transistors as the output devices. Two dc-to-dc converters power the amplifier. This function allows a feedback signal from the ring bus output to independantly control the positive and negative supply voltages.

If ringing output is not available, the supply voltages are a minimum of approximately ±20V. Under normal operation, the feedback from the ringing output causes the positive and negative supply voltages to increase alternately. This process allows enough available voltage to produce the necessary output.

Technical data

Data on NT6X60AA ringing appears in the following tables.

Signaling

Pin numbers

The pin numbers for the NT6X60AA card edge connector (P1) and finger connector (P3) appear in the following table.

NT6X60AA pin numbers (Sheet 1 of 2)

P3 pin	P1 pin	Signal
1	55B	AF0
2	60A	LOGIC GND
3	49B	AF1
4	60B	LOGIC GND
5	48A	ACT
6	61A	LOGIC GND
7	54B	XOVER
8	61B	LOGIC GND
9	54A	RMS
10	62A	LOGIC GND
11	50B	CUR
12	62B	LOGIC GND
13	63A	LOGIC GND
14	47A	FSPLINK
15	76B, 76A	-48V
16	79A	BR
17	77A	-48V
18	79B	BR
19	77B	-48V
20	80A, 80B	BR
21	58A	ABS-48

NT6X60AA (continued)

NT6X60AA pin numbers (Sheet 2 of 2)

P3 pin	P1 pin	Signal
22	59B	FSPMON
23	63B	LOGIC GND
24	49A	SYNC 64
25	75B	RRING
26	73A	RTIP
27	75A	RRING
28	73B, 56A, 57A, 57B	RTIP
29	53A	-52V
30	70A	ABS BR
31		
32	55A	+52V
33		
34	56B	-130V
35		
36	58B	+130V

NT6X60AA ringing type applications (Sheet 1 of 2)

Ring type	User	Revertive	Switch (SW1-4)	Dip switch setting (refer to the following table)
Coded	Bell Canada	N/A	1 to 4	Line 1
Superimposed	BOC (U.S.)	Non-revertive	1 and 2	Line 4
			3 and 4	Line 5
		Revertive	1 and 2 *	Line 6
Note: * Release numbers 06, 07, 08, 09, 0A, OB or OC. If a release number is not available, the card is release 06 or earlier. ** Release numbers OD through OJ or later. *** Release numbers BP or later.				

NT6X60AA ringing type applications (Sheet 2 of 2)

Ring type	User	Revertive	Switch (SW1-4)	Dip switch setting (refer to the following table)
			3 and 4 *	Line 7
			1 and 2 **	Line 8
			3 and 4**	Line 9
	REA ***	Non-revertive	1 and 2	Line 12
			3 and 4	Line 13
		Revertive	1 and 2	Line 10
			3 and 4	Line 11

Note: * Release numbers 06, 07, 08, 09, 0A, OB or OC. If a release number is not available, the card is release 06 or earlier. ** Release numbers OD through OJ or later. *** Release numbers BP or later.

NT6X60AA coded and superimposed ringing (Sheet 1 of 2)

Line	Voltage ac dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
1	86 -52	20	2.00 2.00 1.00 1.00	1 to 4	00000000
2	86 -38	20	2.00 2.00 1.00 1.00	1 and 2	01000000
3	86 +38	20	2.00 2.00 1.00 1.00	3 and 4	00100000
4	86 -38	20	2.00 2.00 1.00 1.00	1 and 2	01011110
5	86 +38	20	2.00 2.00 1.00 1.00	3 and 4	01011110
6	86 -38	20	2.00 2.00 2.00 0.50	1 and 2	10011110
7	86 +38	20	2.00 2.00 2.00 0.50	3 and 4	11011110
8	86 -52	20	1.84 1.84 1.84 0.48	1 and 2	10011110
9	86 +52	20	1.84 1.84 1.84 0.48	3 and 4	11011110
10	105 -52	20	1.84 1.84 1.84 0.48	1 and 2	11101110
11	105 +52	20	1.84 1.84 1.84 0.48	3 and 4	11100010

NT6X60AA (continued)

NT6X60AA coded and superimposed ringing (Sheet 2 of 2)

Line	Voltage ac dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
12	105 -52	20	2.00 2.00 1.00 1.00	1 and 2	01101100
13	105 +52	20	2.00 2.00 1.00 1.00	3 and 4	01100010
14	90 +52	20	2.00 2.00 1.00 1.00	1 to 4	00011000
15	105 +52	20	2.00 2.00 1.00 1.00	1 to 4	01011000
16	120 +52	20	2.00 2.00 1.00 1.00	1 to 4	00111000

NT6X60AA synchromonic ringing(BOC) (Sheet 1 of 2)

	Voltage as dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
Low	90 -52	16	2.00 2.00 1.00 1.00	1	00010000
	90 -52	20	2.00 2.00 1.00 1.00	1	00011000
	90 -52	30	2.00 2.00 1.00 1.00	2	00010100
	100 -52	42	2.00 2.00 1.00 1.00	3	00000010
	110 -52	54	2.00 2.00 1.00 1.00	4	00001010
	125 -52	66	2.00 2.00 1.00 1.00	opt	00000110
Med	105 -52	16	2.00 2.00 1.00 1.00	1	01010000
	105 -52	20	2.00 2.00 1.00 1.00	1	01011000
	110 -52	30	2.00 2.00 1.00 1.00	2	01010100
	115 -52	42	2.00 2.00 1.00 1.00	3	01000010
	125 -52	54	2.00 2.00 1.00 1.00	4	01001010
	140 -52	66	2.00 2.00 1.00 1.00	opt	01000110
High	120 -52	16	2.00 2.00 1.00 1.00	1	00110000
	120 -52	20	2.00 2.00 1.00 1.00	1	00111000
	120 -52	30	2.00 2.00 1.00 1.00	2	00110100
	130 -52	42	2.00 2.00 1.00 1.00	3	00100010

NT6X60AA synchromonic ringing(BOC) (Sheet 2 of 2)

	Voltage as dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
	140 -52	54	2.00 2.00 1.00 1.00	4	00101010
	150 >-52	66	2.00 2.00 1.00 1.00	opt	00100110

NT6X60AA barmonic ringing (BOC)

	Voltage ac dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
Low	90 -52	16.66	2.00 2.00 1.00 1.00	1	00001000
	95 -52	25	2.00 2.00 1.00 1.00	2	00000100
	100 -52	33.33	2.00 2.00 1.00 1.00	3	00001100
	110 -52	50	2.00 2.00 1.00 1.00	4	00010010
	125 -52	66.66	2.00 2.00 1.00 1.00	opt	00010110
Med	105 -52	16.66	2.00 2.00 1.00 1.00	1	01010000
	110 -52	25	2.00 2.00 1.00 1.00	2	01010100
	115 -52	33.33	2.00 2.00 1.00 1.00	3	01000010
	125 -52	50	2.00 2.00 1.00 1.00	4	01001010
	140 -52	66.66	2.00 2.00 1.00 1.00	opt	01000110
High	120 -52	16.66	2.00 2.00 1.00 1.00	1	00110000
	120 -52	25	2.00 2.00 1.00 1.00	2	00110100
	130 -52	33.33	2.00 2.00 1.00 1.00	3	00100010
	140 -52	50	2.00 2.00 1.00 1.00	4	00101010
	150 -52	66.66	2.00 2.00 1.00 1.00	opt	00100110

NT6X60AA (continued)

NT6X60AA decimonic ringing (BOC)

	Voltage ac dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
Low	90 -52	20	2.00 2.00 1.00 1.00	1	00011000
	95 -52	30	2.00 2.00 1.00 1.00	2	00010100
	100 -52	40	2.00 2.00 1.00 1.00	3	00011100
	110 -52	50	2.00 2.00 1.00 1.00	4	00010010
	125 -52	60	2.00 2.00 1.00 1.00	opt	00011010
Med	105 -52	20	2.00 2.00 1.00 1.00	1	01011000
	110 -52	30	2.00 2.00 1.00 1.00	2	01010100
	115 -52	40	2.00 2.00 1.00 1.00	3	01011100
	125 -52	50	2.00 2.00 1.00 1.00	4	01010010
	140 -52	60	2.00 2.00 1.00 1.00	opt	01011010
High	120 -52	20	2.00 2.00 1.00 1.00	1	00111000
	120 -52	30	2.00 2.00 1.00 1.00	2	00110100
	130 -52	40	2.00 2.00 1.00 1.00	3	00111100
	140 -52	50	2.00 2.00 1.00 1.00	4	00110010
	155 -52	60	2.00 2.00 1.00 1.00	opt	00111010

NT6X60AA synchromonic ringing (REA) (Sheet 1 of 2)

	Voltage ac dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
Low	90 -52	16	1.95 1.35 1.35 1.35	1	10010000
	90 -52	20	1.95 1.35 1.35 1.35	1	10011000
	95 -52	30	1.95 1.35 1.35 1.35	2	10010100
	100 -52	42	1.95 1.35 1.35 1.35	3	10000010
	110 -52	54	1.95 1.35 1.35 1.35	4	10001010
	125 -52	66	1.95 1.35 1.35 1.35	opt	10000110

NT6X60AA synchromonic ringing (REA) (Sheet 2 of 2)

	Voltage ac dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
Med	105 -52	16	1.95 1.35 1.35 1.35	1	11010000
	105 -52	20	1.95 1.35 1.35 1.35	1	11011000
	110 -52	30	1.95 1.35 1.35 1.35	2	11010100
	115 -52	42	1.95 1.35 1.35 1.35	3	11000010
	125 -52	54	1.95 1.35 1.35 1.35	4	11001010
	140 -52	66	1.95 1.35 1.35 1.35	opt	11000110
High	120 -52	16	1.95 1.35 1.35 1.35	1	10110000
	120 -52	20	1.95 1.35 1.35 1.35	1	10111000
	120 -52	30	1.95 1.35 1.35 1.35	2	10110100
	130 -52	42	1.95 1.35 1.35 1.35	3	10100010
	140 -52	54	1.95 1.35 1.35 1.35	4	10101010
	150 -52	66	1.95 1.35 1.35 1.35	opt	10100110

NT6X60AA harmonic ringing (REA) (Sheet 1 of 2)

	Voltage ac dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
Low	90 -52	16.66	1.95 1.35 1.35 1.35	1	10001000
	95 -52	25	1.95 1.35 1.35 1.35	2	10000100
	100 -52	33.33	1.95 1.35 1.35 1.35	3	10001100
	110 -52	50	1.95 1.35 1.35 1.35	4	10010010
	125 -52	66.66	1.95 1.35 1.35 1.35	opt	10010110
Med	105 -52	16.66	1.95 1.35 1.35 1.35	1	11001000
	110 -52	25	1.95 1.35 1.35 1.35	2	11000100
	115 -52	33.33	1.95 1.35 1.35 1.35	3	11001100
	125 -52	50	1.95 1.35 1.35 1.35	4	11010010

NT6X60AA (continued)

NT6X60AA harmonic ringing (REA) (Sheet 2 of 2)

	Voltage ac dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
	140 -52	66.66	1.95 1.35 1.35 1.35	opt	11010110
High	120 -52	16.66	1.95 1.35 1.35 1.35	1	10101000
	120 -52	25	1.95 1.35 1.35 1.35	2	10100100
	120 -52	33.33	1.95 1.35 1.35 1.35	3	10101100
	140 -52	50	1.95 1.35 1.35 1.35	4	10110010
	150 -52	66.66	1.95 1.35 1.35 1.35	opt	10110110

NT6X60AA decimonic ringing (REA) (Sheet 1 of 2)

	Voltage ac dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
Low	90 -52	20	1.95 1.35 1.35 1.35	1	10011000
	95 -52	30	1.95 1.35 1.35 1.35	2	10010100
	100 -52	40	1.95 1.35 1.35 1.35	3	10011100
	110 -52	50	1.95 1.35 1.35 1.35	4	10010010
	125 -52	60	1.95 1.35 1.35 1.35	opt	10011010
Med	105 -52	20	1.95 1.35 1.35 1.35	1	11011000
	110 -52	30	1.95 1.35 1.35 1.35	2	11010100
	115 -52	40	1.95 1.35 1.35 1.35	3	11011100
	125 -52	50	1.95 1.35 1.35 1.35	4	11010010
	140 -52	60	1.95 1.35 1.35 1.35	opt	11011010
High	120 -52	20	1.95 1.35 1.35 1.35	1	10111000
	120 -52	30	1.95 1.35 1.35 1.35	2	10110100

Note: Symbols for switch settings: 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any SW1 to SW4 not in use must have all eight sections set to OFF. All four sections of switch SW5 must be in the ON position.

NT6X60AA decimonic ringing (REA) (Sheet 2 of 2)

Voltage ac dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
130 -52	40	1.95 1.35 1.35 1.35	3	10111100
140 -52	50	1.95 1.35 1.35 1.35	4	10110010
155 -52	60	1.95 1.35 1.35 1.35	opt	10111010

Note: Symbols for switch settings: 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any SW1 to SW4 not in use must have all eight sections set to OFF. All four sections of switch SW5 must be in the ON position.

Information for NT6X60AA voltages appear in the following tables.

NT6X60AA frequency adn dc voltage tolerances

Frequency/dc voltage	Tolerances
25 Hz international	±0.33 Hz
-52V dc	-49.75V to -52.5V dc

NT6X60AA ac voltage tolerances (Sheet 1 of 2)

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8
100	97	103
105	101.9	108.1
110	106.7	113.3
115	111.6	118.4
120	116.4	123.6

NT6X60AA (end)

NT6X60AA ac voltage tolerances (Sheet 2 of 2)

Nominal	Low	High
125	121.2	128.7
130	126.1	133.9
140	135.8	144.2
155	150.3	159.6

NT6X60AA ABI/coin voltages

Output	Limits
+48V	+52V ±2.5V
-48V	-52V ±5V
+130V	+130V ±5V
-130V	-130V ±5V

Power requirements

The NT6X60AA requires -42V to -56V. The NT6X60AA requires a nominal current of 3.5A, to a maximum of 4A. The NT6X60AA consumes 180W of power.

NT6X60AB

Product description

The NT6X60AB contains the NT6X38 card for ringing control and the NT6X37 card for ringing amplification. Ringing signals originate in the NT6X38. The NT6X37 amplifies ringing signals to the required output level.

The NT6X60 operates in conjunction with power control circuits in the NT6X25 in remote line concentrating equipment (RLCE) frame supervisory panel (FSP). The NT6X60 is in the host interface equipment shelf in the RLCE for application in the United Kingdom.

Functional description

The NT6X60AB generates ringing signals and dc voltages for automatic number identification (ANI) and coin functions. The frequency and amplitude of ringing waveforms are fixed for this version of the card.

Ringing control NT6X38

The NT6X38 performs the following functions:

- generates ringing signal
- provides ANI and coin outputs
- monitors ring bus output
- synchronizes dc-to-dc converters
- provides auxiliary supply

Generating ringing signal

The waveform store PROM holds a digital representation of a single cycle of each ringing waveform. The control logic selects the correct timing, frequency, and amplitude. The manual settings determine the selection. Output from the waveform store passes through the digital-to-analog converter (DAC) and the low-pass filter. Output provides the analog input signal for the ringing amplifier card.

Providing ANI and coin outputs

A single dc-to-dc converter provides ±48 V output for ANI functions and ±130 V output for coin functions.

Monitoring ring bus output

The NT6X38 monitors ring bus output from the NT6X37 for output voltage and current. If the NT6X38 detects a ringing overvoltage, the NT6X38 signals the NT6X37 to shut down the amplifier. If the NT6X38 detects an ANI or coin overvoltage, the correct converter shuts down. If both types of overvoltage occur, the FSP disconnects primary power.

NT6X60AB (continued)

The monitor circuit provides transistor-transistor logic (TTL)-level status signals to the RLCM processor. The signals indicate ringing voltage (RMS), ringing current (CUR), and low ANI or coin voltage (ACT). These conditions are combined with three status bits from the control logic. The three status bits are AFO, AF1, and XOVER. The combination is sent through a serial data link to provide isolation of the ground reference.

Synchronization of dc-to-dc converters

The dc-to-dc converters in the NT6X37 must be synchronized to the RLCM system clock. The converter requires 48 kHz synchronization and the RLCM provides 64 kHz synchronization. A phase-locked loop converts the frequency. The Dc isolation of the grounds is provided between the RLCM synchronization feed and the NT6X37 synchronization input.

Provision of auxiliary supply

A small dc-to-dc converter supplies ±15 V and +5 V for the internal circuits of the NT6X60AB. An additional +5 V output referenced to logic ground supplies the monitor and synchronization circuits.

Ringing amplifier

The NT6X37 amplifier is a dc-coupled class B type. This amplifier uses power field-effect transistors as output devices. Two dc-to-dc converters power the amplifier. This condition allows a feedback signal from the ring bus output to independently control the positive and negative supply voltages.

If ringing output is not present, the supply voltages are a minimum of approximately ±20 V. Under normal operation, the feedback from the ringing output causes the positive and negative supply voltages to increase alternately. This condition causes sufficient voltage to be available to produce the required output.

Signaling

Pin numbers

The pin number information for the NT6X60AB card edge connector (P1) and finger connector (P3) appears in the following table.

NT6X60AB pin numbers (Sheet 1 of 3)

P3 pin	P1 pin	Signal
1	55B	AF0
2	60A	LOGIC GND
3	49B	AF1

NT6X60AB pin numbers (Sheet 2 of 3)

P3 pin	P1 pin	Signal
4	60B	LOGIC GND
5	48A	ACT
6	61A	LOGIC GND
7	54B	XOVER
8	61B	LOGIC GND
9	54A	RMS
10	62A	LOGIC GND
11	50B	CUR
12	62B	LOGIC GND
13	63A	LOGIC GND
14	47A	FSPLINK
15	76B, 76A	-48V
16	79A	BR
17	77A	-48V
18	79B	BR
19	77B	-48V
20	80A, 80B	BR
21	58A	ABS-48
22	59B	FSPMON
23	63B	LOGIC GND
24	49A	SYNC 64
25	75B	RRING
26	73A	RTIP
27	75A	RRING

NT6X60AB (continued)

NT6X60AB pin numbers (Sheet 3 of 3)

P3 pin	P1 pin	Signal
28	73B, 56A, 57A, 57B	RTIP
29	53A	-52 V
30	70A	ABS BR
31		
32	55A	+52 V
33		
34	56B	-130 V
35		
36	58B	+130 V

Technical data

The following table contains data on NT6X60AB ringing.

NT6X60AB call ringing

	Voltage		
	ac dc offset	Frequency (Hz)	Cadence (seconds)
United Kingdom	75 ±2 V rms -49.75 to -52.5 V	25 Hz ±1%	1.00 1.00 0.40 0.60
Note: Symbols used for switch settings: 0 = ON, 1 = OFF, X = ON or OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF.			

The following tables provide information on voltages.

NT6X60AB frequency and dc voltage tolerances (Sheet 1 of 2)

Frequency/dc voltage	Tolerances	Switch (SW1-4)	Setting 12345678
25 Hz international	±0.33 Hz	1 to 4	0110111X
16 to 33.33 Hz	±0.33 Hz	1 to 4	0110111X
40 to 66.66 Hz	±1.0%	1 to 4	0110111X

NT6X60AB frequency and dc voltage tolerances (Sheet 2 of 2)

Frequency/dc voltage	Tolerances	Switch (SW1-4)	Setting 12345678
-52 V dc	-49.75 to -52.5 V dc	1 to 4	0110111X
-38 V dc	±2.0 V	1 to 4	0110111X
+38 V dc	±2.0 V	1 to 4	0110111X

NT6X60AB ac voltage tolerances

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8
100	97	103
105	101.9	108.1
110	106.7	113.3
115	111.6	118.4
120	116.4	123.6
125	121.2	128.7
130	126.1	133.9
140	135.8	144.2
155	150.3	159.6

NT6X60AB (end)

NT6X60AE ANI/coin voltages

Output	Limits
+48 V	+52 V, ±2.5 V
-48 V	-52 V, ±5 V
+130 V	+130 V, ±5 V
-130 V	-130 V, ±5 V

Power requirements

The NT6X60AB requires -42 V to -56 V and a nominal current of 3.5 A, to a maximum of 5 A. The NT6X60AB consumes 180 W of power.

NT6X60AE

Product description

The NT6X60AE contains two cards: the NT6X38 ringing control and the NT6X37 ringing amplifier. Ringing signals originate in the NT6X38 and are amplified to the required output level by the NT6X37.

For application in Australia, the NT6X60AE operates with the following. The NT6X60AE operates with power control circuit frame supervisory panel (FSP) NT6X53BA in the remote line concentrating module (RLCM) or FSP NT6X25AA in the remote line concentrating equipment (RLCE).

Functional description

The NT6X60AE generates ringing signals and dc voltages for automatic number identification (ANI) and coin functions. Frequencies and amplitudes of ringing waveform are set manually with dual inline package (DIP) switches or straps, to meet telephone company requirements.

Ringing control NT6X38

The NT6X38 performs the following functions:

- generates ringing signal
- provides ANI and coin outputs
- monitors the ring bus output
- synchronizes dc-to-dc converters
- provides auxiliary supply

Generating ringing signal

A digital representation of a single cycle of each ringing waveform is held in the waveform store PROM. The control logic selects the correct timing, frequency, and amplitude according to the manual settings. The output from the waveform store passes through the digital-to-analog converter and low-pass filter. This procedure provides the analog input signal for the ringing amplifier card.

Providing ANI and coin outputs

A single dc-to-dc converter provides ±52V output for ANI functions and ±130V output for coin functions.

Monitoring ring bus outputs

The NT6X38 monitors ring bus output from the NT6X37 for output voltage and current. If the NTX38 detects a ringing overvoltage, the NTX38 signals the NT6X37 to shut down the amplifier. If the NT6X38 detects an ANI or coin

NT6X60AE (continued)

overvoltage, the correct converter is shut down. If both types of overvoltage occur, the FSP disconnects primary power.

The monitor circuit also provides transistor-transistor logic (TTL)-level status signals to the RLCM processor. The status signals indicate the following: ringing voltage (RMS), ringing current (CUR), and low ANI or coin voltage (ACT). These signals combine with three status bits from the control logic (AFO, AF1, and XOVER). This group is sent through a serial data link to provide isolation of the ground reference.

Synchronizing dc-to-dc converters

The dc-to-dc converters in the NT6X37 ringing amplifier must synchronize to the RLCM system clock. Since the converter requires 48 kHz synchronization and the RLCM provides 64 kHz, a phase-locked loop converts the frequency. Dc isolation of the grounds is provided between the RLCM synchronization feed and the NT6X37 synchronization input.

Providing auxiliary supply

A small dc-to-dc converter supplies ±15V and 5V for the internal circuits of NT6X38. The ±15V is used for the control circuits on the NT6X37.

Ringing amplifier NT6X37

The NT6X37 amplifier is a dc-coupled class B type that uses power field effect transistors as the output devices. Two dc-to-dc converters power the amplifier, allowing separate control for the positive and negative supply voltages. A feedback signal from the ring bus output controls the voltages.

If there is no ringing output, the supply voltages are a minimum of about ±20V. Under normal operation, the feedback from the ringing output causes the positive and negative supply voltages to increase alternately. Voltage is available to produce the required output.

Signaling

Pin numbers

The pin numbers for the NT6X60AE appear in the following table.

NT6X60AE pin numbers (Sheet 1 of 3)

P3 pin	P1 pin	Signal
1	55B	AF0
2	60A	LOGIC GND
3	49B	AF1

NT6X60AE pin numbers (Sheet 2 of 3)

P3 pin	P1 pin	Signal
4	60B	LOGIC GND
5	48A	ACT
6	61A	LOGIC GND
7	54B	XOVER
8	61B	LOGIC GND
9	54A	RMS
10	62A	LOGIC GND
11	50B	CUR
12	62B	LOGIC GND
13	63A	LOGIC GND
14	47A	FSPLINK
15	76B, 76A	-48V
16	79A	BR
17	77A	-48V
18	79B	BR
19	77B	-48V
20	80A, 80B	BR
21	58A	ABS-48
22	59B	FSPMON
23	63B	LOGIC GND
24	49A	SYNC 64
25	75B	RRING
26	73A	RTIP
27	75A	RRING

NT6X60AE (continued)

NT6X60AE pin numbers (Sheet 3 of 3)

P3 pin	P1 pin	Signal
28	73B, 56A, 57A, 57B	RTIP
29	53A	-52V
30	70A	ABS BR
31		
32	55A	+52 V
33		
34	56B	-130 V
35		
36	58B	+130 V

Technical data

Information about ringing appears in the following table.

NT6X60AE call ringing

	Voltage ac dc offset	Freq (Hz)	Cadence (seconds)	Switch (SW1-4)	Setting 12345678
Australia	90 -52	25	1.00 1.00 0.40 0.60	1 to 4	0111111X
Note: The system records the symbols under the heading settings as: 0= ON, 1= OFF, X = either ON or OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. All four sections of switch SW5 must be in the ON position.					

Information about NT6X60AE voltages appears in the following tables.

NT6X60AE frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
25 Hz international	±0.33 Hz
-52 V dc	-49.75 V to -52.5 V dc

NT6X60AE dc voltage tolerances

Nominal	Low	High
90	88	92

NT6X60AE ANI/coin voltages

Output	Limits
+48 V	+52 V, ±2.5 V
-48 V	-52 V, ±5 V
+130 V	+130 V, ±5 V
-130 V	-130 V, ±5 V

Power requirements

The NT6X60AE requires -42 V to -56 V, and a nominal current of 3.5 A, to a maximum of 4 A. The NT6X60AE consumes 180 W of power.

NT6X60BA

Product description

The NT6X60BA contains two cards. Theses cards are the NT6X38AC ringing control and the NT6X37DA ringing amplifier. Ringing signals originate in NT6X38AC. The NT6X37DA amplifies the ringing signals to the required output level.

The NT6X60BA operates with the remote line concentrating module frame supervisory panel (NT6X25).

Location

The NT6X60BA is in the host interface equipment shelf in the remote line concentrating equipment (RLCE).

Functional description

The NT6X60BA generates sinusoidal ringing signals. Use dual inline package (DIP) switches to manually set different frequencies and amplitudes of ringing waveforms. Use DIP switches to meet different telephone company requirements.

Functional blocks

The NT6X60BA contains two printed circuit boards that act as functional blocks: the ringing control (NT6X38AC) and the ringing amplifier (NT6X37DA).

Ringing control NT6X38AC

The NT6X38AC performs the following functions:

- generation of ringing signals
- monitoring ring bus output
- synchronization of dc-to-dc converters
- supply of auxiliary power

The NT6X38AC PROM stores a digital image of a single cycle of each ringing waveform. The control logic selects the correct timing, frequency, and amplitude according to the manual settings of the DIP switches. The output from the waveform store passes through the digital-to-analog converter and the low-pass filter. This procedure provides the analog input signal for the ringing amplifier card.

The NT6X38AC monitors the ring bus output from the NT6X37DA for output voltage and current. If the NT6X38AC detects a ringing overvoltage, the NT6X38AC sends a signal to the NT6X37DA to shut down the amplifier. The

monitor circuit provides transistor-transistor logic (TTL) signals to the processor of the remote line concentrating module (RLCM). The TTL signals indicate ringing voltage (RMS) and ringing current (CUR).

The NT6X38AC synchronizes the dc-to-dc converters in the NT6X37DA to the RLCM system clock. The converters require 48 kHz synchronization. The RLCM provides 64 KHz. A phase-locked loop converts the frequency. The ringing control provides isolation of the grounds between the LCM sync feeds and the NT6X37DA sync input.

The NT6X38AC contains a small dc-to-dc converter that supplies 15V and 5V for the NT6X38AC internal circuits. The 15V is for control circuits on the NT6X37DA.

Ringing amplifier NT6X37DA

The NT6X37DA amplifier is a dc-coupled class-B amplifier that uses power field-effect transistors (FET) as output devices. Two dc-to-dc converters power the amplifier. This power allows the feedback signal from the ring bus output to independently control the positive and negative supply voltages.

The NT6X37DA monitors the positive and negative supply voltages and the combined differential voltage. If any of these voltages exceed the safety threshold, the two high-voltage supplies are not permanently shut down. A soft start follows.

Technical data

The ringing characteristics and DIP switch setting for the NT6X60BA appear in the following table.

Japan ringing characteristics and switch settings

Voltage			Switch	Setting
AC DC offset	**Freq(Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
76 0	16	2 2 1 1	1 to 4	1110111X
Note: The system records the symbols under the heading settings as 0=ON, 1 = OFF, X = either ON or OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. All four sections of switch SW5 must be in the ON position.				

NT6X60BA (end)

Information about NT6X60BA voltages appears in the following tables.

NT6X60BA frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
16 Hz	+ or - 1 Hz
0 V dc	+ or - 2 V dc

NT6X60BA ac voltage tolerances

Nominal	Low	High
76	69	83

Power requirements

The minimum supply voltage for the NT6X60BA is 42 V. The nominal supply current is 3.5 A and the maximum is 4 A.

NT6X60BB

Product description

The NT6X60BB ringing generator is a vertical mount version of the ringing generator intended for the Japanese market. The contains a single card. This single card provides all the required functionality that two cards in the NT6X60BA ringing generator provide. The NT6X60BB is backwards compatible with the NT6X60BA.

Location

The NT6X60BB is in the host interface equipment (HIE) shelf in the remote line concentrating equipment (RLCE).

Functional description

The NT6X60BB generates ringing signal voltages. You manually set the ring output frequency and amplitude during installation with the four dual inline package (DIP) switches. The settings meet Japanese requirements.

Functional blocks

The ringing signal is ground backed. The ringing is centered about ground. The input battery (through a fuse) provides the dc-offset for this market. The dc-offset is applied to the tip side of the bus.

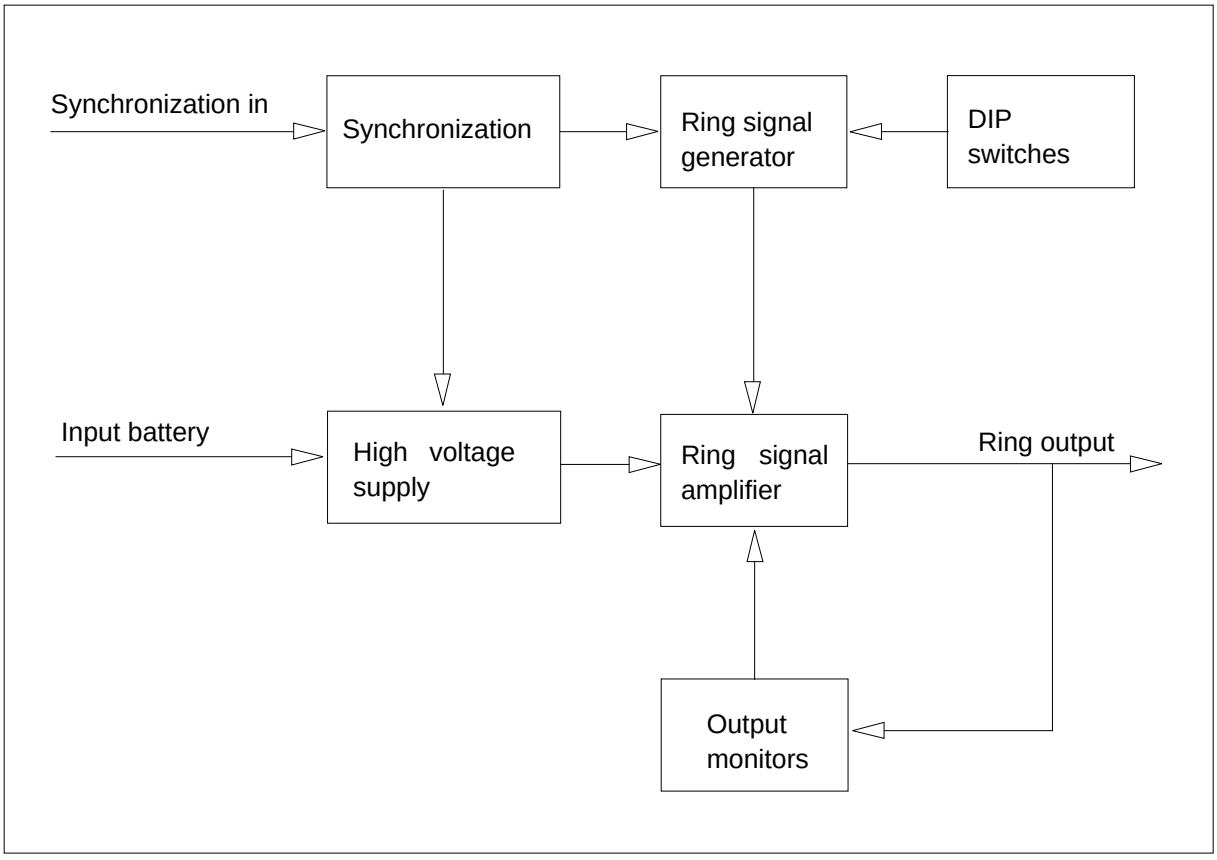
The NT6X60BB has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship of the functional blocks appears in the following figure.

NT6X60BB (continued)

NT6X60BB functional blocks



High voltage supply

The system filters and feeds the raw battery input voltage (-48 V) into a single-transistor isolated boost converter topology. This procedure switches the input voltage into a square wave across the primary of a flyback transformer. The flyback transformer is where the secondary is rectified and filtered. This procedure produces a regulated floating 300 V supply. An isolated output produces the voltages required to power the ringing control and monitor circuits.

Ring signal generator

The card microcontroller stores a digital image of the ringing waveform in the programmable read-only memory (PROM). The microcontroller responds to the DIP switch settings on the card. The microcontroller sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. This information produces a low voltage sinusoidal waveform of the right frequency and reference amplitude to the ring signal amplifier. The reference

amplitude includes dc offset. The microcontroller provides additional information like zero-crossing detect (XOVER) and subcycle cadence information (AF0 and AF1).

Ring signal amplifier

The system feeds the ringing signal from the ring signal generator into a class D amplifier circuit. The amplifier circuit modulates the pulse width to a full bridge switch configuration. This configuration switches the high voltage floating supply alternately to ground on one side for each half cycle of the output waveform. This procedure creates a train of variable width pulses. These pulses produce the required sinusoidal ringing output voltage and dc-offset when filtered. This output is fed out of the ring generator. Comparing a sample of the filtered output to the input reference signal from the ring signal generator circuit regulates output.

Output monitors

The NT6X60BB monitors the ringing output for ac overvoltage and low voltage. The NT6X60BB monitors the dc-offset for both overvoltage and low voltage. In an overvoltage condition, the current must be less than the current limit point to allow shutdown.

The monitor circuits provide electrically isolated transistor-to-transistor logic (TTL) level signals to the line concentrating module (LCM) processor. These signals indicate low ringing voltage (RMS-bit), and excess ringing output current (CUR-bit).

Synchronization

All the dc-dc converters and the ringing amplifier on the NT6X60BB are synchronized. A phase-lock loop to the clock frequency of the LCM at some integer multiple of 8 kHz synchronizes the converters and ringing amplifier. This synchronization is electrically isolated from the clock signal the LCM provides. This synchronization is isolated between the different converters on this card.

NT6X60BB (continued)

Signaling

Pin numbers

The pin number for the NT6X60BB card edge connector (P4) appears in the following table.

NT6X60BB pin numbers (Sheet 1 of 2)

P4 pin	Signal
55B	AF0
60A	LOGIC GND
49B	AF1
60B	LOGIC GND
48A	ACT
61A	LOGIC GND
54B	XOVER
61B	LOGIC GND
54A	RMS
62A	LOGIC GND
50B	CUR
62B	LOGIC GND
63A	LOGIC GND
47A	FSPLINK
76B, 76A	-48 V
79A	BR
77A	-48 V
79B	BR
77B	-48 V
80A, 80B	BR
58A	ABS -48 V

NT6X60BB pin numbers (Sheet 2 of 2)

P4 pin	Signal
59B	FSPMON
63B	LOGIC GND
49A	SYNC 64
75B	RRING
73A	RTIP
75A	RRING
73B, 56A, 57A, 57B	RTIP
53A	NC
70A	ABS BR
55A	NC
56B	NC
58B	NC

Technical data

The card has an output of 16 Hz, with an amplitude of 76V (rms). The correct setting of the DIP switches is 11101110.

The ringing characteristics and DIP switch setting for the NT6X60BB appear in the following table.

NT6X60BB Japan ringing characteristics and switch settings

Voltage		Cadence	Switch	Setting
AC DC offset	**Freq(Hz)**	**(seconds)**	**(SW1-4)**	**12345678**
76 0	16	2 2 1 1	1 to 4	11101110
Note: Interpret the symbols under the heading settings as 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF.				

NT6X60BB (end)

Information about NT6X60BB voltages appear in the following table.

NT6X60BB Japan frequency and dc voltage tolerance

Frequency/dc voltage	Tolerances
16 Hz	+ or - 1 Hz
0 V (dc)	+ or - 2 V (dc)
-48 V (dc)	+ or - 2 V (dc)

NT6X60BB Japan ac voltage tolerances

Nominal	Low	High
76	69	83

Power requirements

The requires -39.5 V to -75 V, and a nominal current of 1 A, to a maximum of 2 A. The card consumes 75W of power.

NT6X60CA

Product description

The NT6X60CA ringing generator is a vertical mount version of the ringing generator intended for the North American market. The NT6X60CA contains a single card. This card provides the required functionality that used to require two cards in the NT6X60AA ringing generator. The NT6X60CA is backwards compatible with the NT6X60AA.

Location

The NT6X60CA operates with the NT6X25 remote line concentrating equipment (RLCE) frame supervisory panel (FSP). The NT6X60CA is in the host interface equipment (HIE) shelf in the RLCE.

Functional description

The NT6X60CA generates ringing signals and the dc voltages that the automatic number identification (ANI) and coin functions require. Set the ring output frequency and amplitude manually, during installation with the four dual inline package (DIP) switches. Set the output frequency and amplitude to meet North American requirements.

Functional blocks

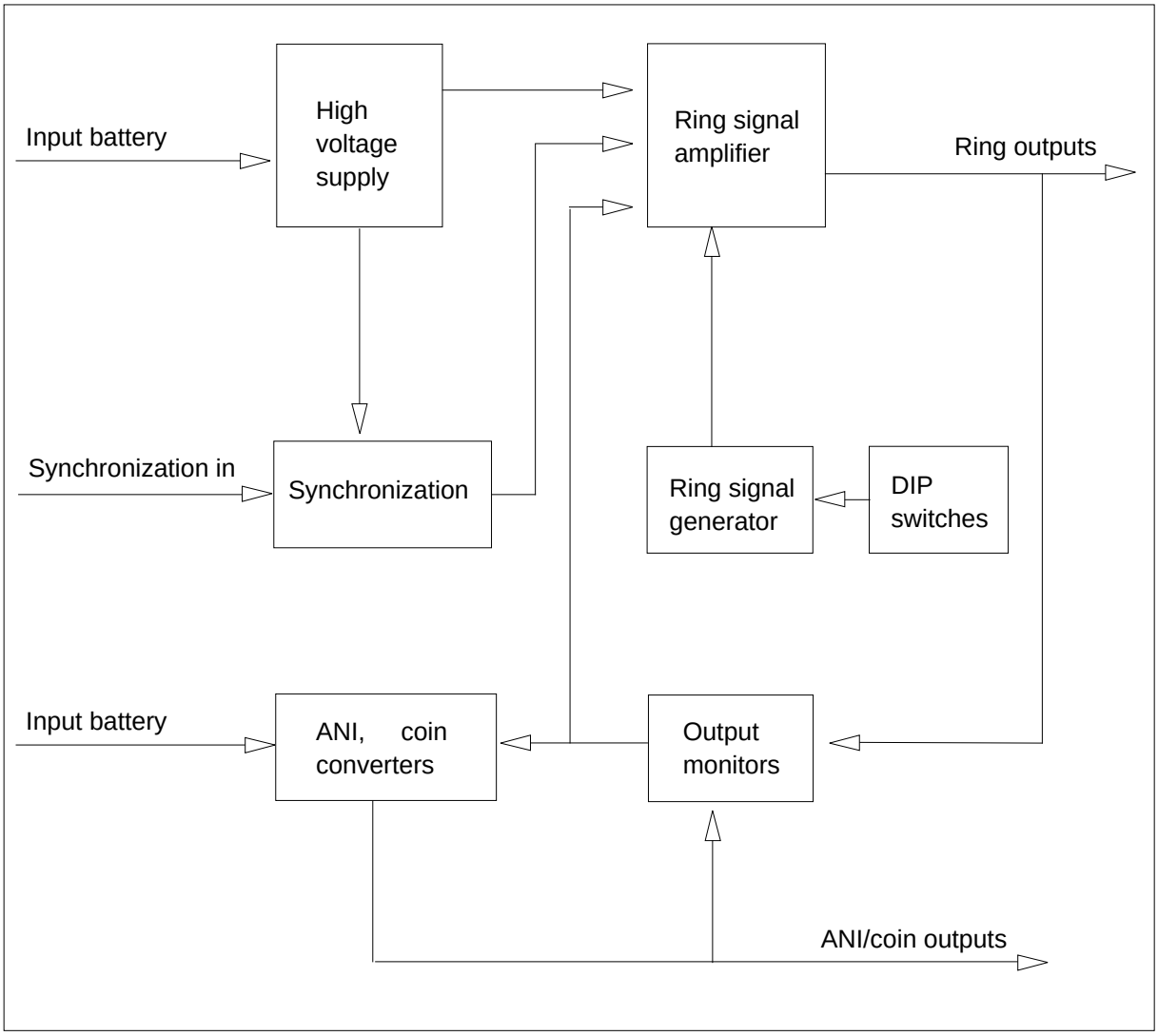
The NT6X60CA has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- ANI, coin converters
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X60CA (continued)

NT6X60CA functional blocks



High voltage supply

The system filters the raw battery input voltage (-48 V) and feeds the power supply to a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of the flyback transformer. The system rectifies the secondary flyback transformer and filters the voltage to produce a regulated floating 300-V supply. An isolated output produces the voltages required to power the ringing control and monitor circuits.

Ring signal generator

The programmable read-only memory (PROM) of the microcontroller of the card stores a digital image of the ringing waveform. The microcontroller responds to the DIP switch settings on the card. The response sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. The DAC circuit produces a low voltage sinusoidal waveform of the right frequency and reference amplitude. The waveform includes the dc offset to the ring signal amplifier. The mircocontroller also provides additional information. The additional information can include zero-crossing detect (XOVER) and cycle cadence information (AF0 and AF1).

Ring signal amplifier

The ringing signal from the ring signal generator feeds to the class D amplifier circuit. The class D amplifier circuit modulates the pulse width to a full-bridge switch configuration. This alternately switches the high voltage floating supply to ground on one side for each half cycle of the output waveform. The result of the filtered train of variable width pulses produce the required sinusoidal ringing output voltage and dc-offset. The sinusoidal ringing output voltage and dc-offset are fed from the ringing generator. Compare a sample of the filtered output to the input reference signal. The input reference signal comes from the ring signal generator circuit.

ANI, coin converters

Two separate single-transistor isolated flyback converters provide dc outputs. Both the ANI feature and the coin feature require the dc output. Linear post regulators regulate the dc outputs.

Output monitors

The output monitor checks the ringing output and dc-offset for ac overvoltage and undervoltage. If the output monitor detects an overvoltage, the system disables the amplifier. If the output monitor detects an undervoltage, the current must be less than the current limit point to allow shutdown.

The output monitor also checks the ANI/Coin outputs for overvoltage and undervoltage conditions. If the output monitor detects an overvoltage condition, the system disables the appropriate converter. If the output monitor detects an undervoltage condition, the system raises an alarm. The card does not shut down completely, unless the ringing output is low.

The monitor circuits provide electrically isolated transistor-transistor logic (TTL) level signals to the LCM processor. The TTL level signals indicate a low ringing voltage (RMS-bit), excess ringing output current (CUR-bit), and ANI/Coin status (ACT-bit).

NT6X60CA (continued)

Synchronization

A phase-lock loop to the clock frequency of the LCM synchronizes all of the dc-dc converters and the ringing amplifier on this card. The dc-dc converters and the ringing amplifier synchronized to an integer multiple of 8 kHz. This synchronization is electrically isolated from the clock signal that the LCM provides. The synchronization is isolated between the different converters on this card.

Technical data

Information about NT6X60CA ringing appears in the following tables.

NT6X60CA Ringing type applications using (Sheet 1 of 2)

Ring type	User	DIP switch setting (Table)
Coded ringing	Bell Canada	
20 Hz	U.S. Bell operating companies (BOC)	Coded and superimposed ringing
Switches 1 to 4		(Line 1,15,16,17)
30 Hz		Code and superimposed ringing
Switches 1 to 4		(Lines 12,13,14)
Superimposed ringing	BOC (U.S.)	
BCS15 or earlier		Coded and superimposed ringing
Switches 1 and 2		(Line 2)
Switches 3 and 4		(Line 3)
BCS16 and later (non-revertive)		Coded and superimposed ringing
Switches 1 and 2		(Line 4)
Switches 3 and 4		(Line 5)
BCS16 and later (revertive)		
Switches 1 and 2		(Line 6)
Switches 3 and 4		(Line 7)

Note: Do not change any DIP switch setting when power is on. Set the appropriate circuit breaker on the NT6X35 FSP to OFF.

NT6X60CA Ringing type applications using (Sheet 2 of 2)

Ring type	User	DIP switch setting (Table)
Superimposed ringing	Rural Electrification Administration (REA)	
BCS16 and later (non-revertive)		Coded and superimposed ringing
Switches 1 and 2		(Line 10)
Switches 3 and 4		(Line 11)
BCS16 and later (revertive)		
Switches 1 and 2		(Line 8)
Switches 3 and 4		(Line 9)
Frequency selective ringing	BOC (U.S.)	
Synchromonic		Synchromonic ringing (BOC)
Harmonic		Harmonic ringing (BOC)
Decimonic		Decimonic ringing (BOC)
	REA	
Synchromonic		Synchromonic ringing (REA)
Harmonic		Harmoinc ringing (REA)
Decimonic		Decimonic ringing (REA)
	International	
Switches 1 to 4		International ringing
Switches 1 to 4	Japan	International ringing
Switches 1 to 4	U.K.	International ringing

Note: Do not change any DIP switch setting when power is on. Set the appropriate circuit breaker on the NT6X35 FSP to OFF.

NT6X60CA (continued)

NT6X60CA international coded and superimposed ringing

Line	Voltage ac dc	Freq (Hz)	Cadence(seconds)	Switch (SW1-4)	Setting 12345678
1	86 -52	20	2 2 1 1	1 to 4	00000000
2	86 -38	20	2 2 1 1	1 & 2	01000000
3	86 +38	20	2 2 1 1	3 & 4	00100000
4	86 -38	20	2 2 1 1	1 & 2	00011110
5	86 +38	20	2 2 1 1	3 & 4	01011110
6	86 -52	20	1.84 1.84 1.84 0.48	1 & 2	10011110
7	86 +52	20	1.84 1.84 1.84 0.48	3 & 4	11011110
8	105 -52	20	1.84 1.84 1.84 0.48	1 & 2	11101100
9	105 +52	20	1.84 1.84 1.84 0.48	3 & 4	11100010
10	105 -52	20	2 2 1 1	1 & 2	01101100
11	105 +52	20	2 2 1 1	3 & 4	01100010
12	95 -52	30	2 2 1 1	1 to 4	00010100
13	110 -52	30	2 2 1 1	1 to 4	01010100
14	120 -52	30	2 2 1 1	1 to 4	00110100
15	90 -52	20	2 2 1 1	1 to 4	00011000
16	105 -52	20	2 2 1 1	1 to 4	01011000
17	120 -52	20	2 2 1 1	1 to 4	00111000

Note: The symbols under the heading settings for 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

NT6X60CA synchromonic ringing (BOC)

	Voltage				Switch	Setting
	ac	dc	Freq (Hz)	Cadence (seconds)	(SW1-4)	12345678
Low	90	-52	16	2 2 1 1	1	00010000
	90	-52	20	2 2 1 1	1	00011000
	95	-52	30	2 2 1 1	2	00010100
	100	-52	42	2 2 1 1	3	00000010
	110	-52	54	2 2 1 1	4	00001010
	125	-52	66	2 2 1 1	opt	00000110
Med	105	-52	16	2 2 1 1	1	01010000
	105	-52	20	2 2 1 1	1	01011000
	110	-52	30	2 2 1 1	2	01010100
	115	-52	42	2 2 1 1	3	01000010
	125	-52	54	2 2 1 1	4	01001010
	140	-52	66	2 2 1 1	opt	01000110
High	120	-52	16	2 2 1 1	1	00110000
	120	-52	20	2 2 1 1	1	00111000
	120	-52	30	2 2 1 1	2	00110100
	130	-52	42	2 2 1 1	3	00100010
	140	-52	54	2 2 1 1	4	00101010
	145	-52	66	2 2 1 1	opt	00100110

Note: The symbols under the heading settings for 0 = ON, 1 = OFF, opt = the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

NT6X60CA (continued)

NT6X60CA decimonic ringing (BOC)

	Voltage				Switch	Setting
	ac	**dc**	**Freq (Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	20	2 2 1 1	1	00011000
	95	-52	30	2 2 1 1	2	00010100
	100	-52	40	2 2 1 1	3	00011100
	110	-52	50	2 2 1 1	4	00010010
	125	-52	60	2 2 1 1	opt	00011010
Med	105	-52	20	2 2 1 1	1	01011000
	110	-52	30	2 2 1 1	2	01010100
	115	-52	40	2 2 1 1	3	01011100
	125	-52	50	2 2 1 1	4	01010010
	140	-52	60	2 2 1 1	opt	01011010
High	120	-52	20	2 2 1 1	1	00111000
	120	-52	30	2 2 1 1	2	00110100
	130	-52	40	2 2 1 1	3	00111100
	140	-52	50	2 2 1 1	4	00110010
	145	-52	60	2 2 1 1	opt	00111010

Note: The symbols under the heading settings for 0 = ON, 1 = OFF, opt = the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

NT6X60CA synchromonic ringing (REA)

	Voltage				Switch	Setting
	ac	**dc**	**Freq (Hz)**	**Cadence (seconds)**	**(SW1-4>**	**12345678**
Low	90	-52	16	1.95 1.35 1.35 1.35	1	10010000
	90	-52	20	1.95 1.35 1.35 1.35	1	10011000
	95	-52	30	1.95 1.35 1.35 1.35	2	10010100
	100	-52	42	1.95 1.35 1.35 1.35	3	10000010
	110	-52	54	1.95 1.35 1.35 1.35	4	10001010
	125	-52	66	1.95 1.35 1.35 1.35	opt	10000110
Med	105	-52	16	1.95 1.35 1.35 1.35	1	11010000
	105	-52	20	1.95 1.35 1.35 1.35	1	11011000
	110	-52	30	1.95 1.35 1.35 1.35	2	11010100
	115	-52	42	1.95 1.35 1.35 1.35	3	11000010
	125	-52	54	1.95 1.35 1.35 1.35	4	11001010
	140	-52	66	1.95 1.35 1.35 1.35	opt	11000110
High	120	-52	16	1.95 1.35 1.35 1.35	1	10110000
	120	-52	20	1.95 1.35 1.35 1.35	1	10111000
	120	-52	30	1.95 1.35 1.35 1.35	2	10110100
	130	-52	42	1.95 1.35 1.35 1.35	3	10100010
	140	-52	54	1.95 1.35 1.35 1.35	4	10101010
	145	-52	66	1.95 1.35 1.35 1.35	opt	10100110

Note: The symbols under the heading settings for 0 = ON, 1 = OFF, opt = the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

NT6X60CA (continued)

NT6X60CA harmonic ringing (REA)

	Voltage				Switch	Setting
	ac	**dc**	**Freq (Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	16-2/3	1.95 1.35 1.35 1.35	1	10001000
	95	-52	25	1.95 1.35 1.35 1.35	2	10000100
	100	-52	33-1/3	1.95 1.35 1.35 1.35	3	10001100
	110	-52	50	1.95 1.35 1.35 1.35	4	10010010
	125	-52	66-2/3	1.95 1.35 1.35 1.35	opt	10010110
Med	105	-52	16-2/3	1.95 1.35 1.35 1.35	1	11001000
	110	-52	25	1.95 1.35 1.35 1.35	2	11000100
	115	-52	33-1/3	1.95 1.35 1.35 1.35	3	11001100
	125	-52	50	1.95 1.35 1.35 1.35	4	11010010
	140	-52	66-2/3	1.95 1.35 1.35 1.35	opt	11010110
High	120	-52	16-2/3	1.95 1.35 1.35 1.35	1	10101000
	120	-52	25	1.95 1.35 1.35 1.35	2	10100100
	130	-52	33-1/3	1.95 1.35 1.35 1.35	3	10101100
	140	-52	50	1.95 1.35 1.35 1.35	4	10110010
	145	-52	66-2/3	1.95 1.35 1.35 1.35	opt	10110110

Note: The symbols under the heading settings for 0 = ON, 1 = OFF, opt = the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

NT6X60CA harmonic ringing (REA)

	Voltage				Switch	Setting
	ac	**dc**	**Freq (Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	20	1.95 1.35 1.35 1.35	1	10011000
	95	-52	30	1.95 1.35 1.35 1.35	2	10010100
	100	-52	40	1.95 1.35 1.35 1.35	3	10011100
	110	-52	50	1.95 1.35 1.35 1.35	4	10010010
	125	-52	60	1.95 1.35 1.35 1.35	opt	10011010
Med	105	-52	20	1.95 1.35 1.35 1.35	1	11011000
	110	-52	30	1.95 1.35 1.35 1.35	2	11010100
	115	-52	40	1.95 1.35 1.35 1.35	3	11011100
	125	-52	50	1.95 1.35 1.35 1.35	4	11010010
	140	-52	60	1.95 1.35 1.35 1.35	opt	11011010
High	120	-52	20	1.95 1.35 1.35 1.35	1	10111000
	120	-52	30	1.95 1.35 1.35 1.35	2	10110100
	130	-52	40	1.95 1.35 1.35 1.35	3	10111100
	140	-52	50	1.95 1.35 1.35 1.35	4	10110010
	145	-52	60	1.95 1.35 1.35 1.35	opt	10111010

Note: The system records the symbols under the heading settings for 0 = ON, 1 = OFF, opt = the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

NT6X60CA (continued)

NT6X60CA international ringing

	Voltage				Switch	Setting
	ac	**dc**	**Freq (Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	67	-52	25	1.95 1.35 1.35 1.35	1 to 4	10001110
Med	75	-52	25	1.95 1.35 1.35 1.35	1 to 4	11001110
High	82	-52	25	1.95 1.35 1.35 1.35	1 to 4	10101110
Low	67	-52	25	2 2 1 1	1 to 4	00001110
Med	75	-52	25	2 2 1 1	1 to 4	01001110
High	82	-52	25	2 2 1 1	1 to 4	00101110
Japan	75	0	16	2 2 1 1	1 to 4	11101110
U.K.	75	-52	25	1 1 0.4 0.6	1 to 4	01101110

Note: The system records the symbols under the heading settings for 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Switch settings for Japan are only for use for Japanese ringing.

NT6X60CA harmonic ringing (BOC) (Sheet 1 of 2)

	Voltage				Switch	Setting
	ac	**dc**	**Freq (Hz)**	**Cadence (seconds)**	**(SW1-4)**	**12345678**
Low	90	-52	16-2/3	2 2 1 1	1	00001000
	95	-52	25	2 2 1 1	2	00000100
	100	-52	33-1/3	2 2 1 1	3	00001100
	110	-52	50	2 2 1 1	4	00010010
	125	-52	66-2/3	2 2 1 1	opt	00010110
Med	105	-52	16-2/3	2 2 1 1	1	01001000

Note: The system records the symbols under the heading settings for 0 = ON, 1 = OFF, opt = the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

NT6X60CA harmonic ringing (BOC) (Sheet 2 of 2)

	Voltage				Switch	Setting
	ac	dc	Freq (Hz)	Cadence (seconds)	(SW1-4)	12345678
	110	-52	25	2 2 1 1	2	01000100
	115	-52	33-1/3	2 2 1 1	3	01001100
	125	-52	50	2 2 1 1	4	01010010
	140	-52	66-2/3	2 2 1 1	opt	01010110
High	120	-52	16-2/3	2 2 1 1	1	00101000
	120	-52	25	2 2 1 1	2	00100100
	130	-52	33-1/3	2 2 1 1	3	00101100
	140	-52	50	2 2 1 1	4	00110010
	145	-52	66-2/3	2 2 1 1	opt	00110110

Note: The system records the symbols under the heading settings for 0 = ON, 1 = OFF, opt = the specified setting can be done on any SW1 to SW4. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use must have all eight sections set to OFF.

Information about tolerances appears in the following tables.

NT6X60CA frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
16 to 33-1/3 Hz	±1/3 Hz
40 to 66-2/3 Hz	±1%
25 Hz international	±1/3 Hz
-52 V (dc)	-49.75 to -52.5 V (dc)
-38 V (dc)	±2 V (dc)
+38 V (dc)	±2 V (dc)

NT6X60CA (continued)

NT6X60CA ac voltage tolerances

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8
100	97	103
105	101.9	108.1
110	106.7	113.3
115	111.6	118.4
120	116.4	123.6
125	121.2	128.7
130	126.1	133.9
140	135.8	144.2
145	140.7	149.3

Information about ANI and coin voltages appear in the following table.

NT6X60CA ANI and coin voltages

Output	Limits
+48 V	+52 V, ±2.5 V
-48 V	-52 V, ±2.5 V
+130 V	+130 V, ±5 V
-130 V	-130 V, ±5 V

Signaling

Pin numbers

The pin number information for the NT6X60CA finger connector (P1) appears in the following table.

NT6X60CA pin numbers (Sheet 1 of 2)

P4 pin	Signal
55B	AF0
60A	LOGIC GND
49B	AF1
60B	LOGIC GND
48A	ACT
61A	LOGIC GND
54B	XOVER
61B	LOGIC GND
54A	RMS
62A	LOGIC GND
50B	CUR
62B	LOGIC GND
63A	LOGIC GND
47A	FSPLINK
76B, 76A	-48 V
79A	BR
77A	-48 V
79B	BR
77B	-48 V
80A, 80B	BR
58A	ABS -48 V

NT6X60CA (end)

NT6X60CA pin numbers (Sheet 2 of 2)

P4 pin	Signal
59B	FSPMON
63B	LOGIC GND
49A	SYNC 64
75B	RRING
73A	RTIP
75A	RRING
73B, 56A, 57A, 57B	RTIP
53A	-52 V
70A	ABS BR
55A	+52 V
56B	-130 V
58B	+130 V

Power requirements

The NT6X60CA requires -39.5 V to -75 V, and a nominal value of 2.5 A to a maximum of 4 A. The NT6X60CA consumes 140 W of power.

NT6X60DA

Product description

The NT6X60DA contains two cards, the NT6X38 ringing control and the NT6X37 ringing amplifier. Ringing signals start in NT6X38. The NT6X37 amplifies signals to the required output level.

The NT6X60DA operates in the remote line concentrating module (RLCM) frame supervisory panel (FSP), NT6X35BA or the remote line concentrating equipment (RLCE) FSP, NT6X25AA.

Functional description

The NT6X60DA generates ringing signals and dc voltages for automatic number identification (ANI) and coin functions. Frequencies and amplitudes of ringing waveform are set manually. To set the ringing waveform use dual inline package (DIP) switches or straps that meet telephone company requirements.

The NT6X30DA contains two printed circuit boards, the ringing control NT6X38DA and the ringing amplifier NT6X37BA. Ringing signals start in the NT6X38DA. The NT6X37BA amplifies signals to the required output level.

Ringing control NT6X38DA

The NT6X38DA performs the following functions:

- generates ringing signal
- provides ANI and coin outputs
- monitors the ring bus output
- synchronizes dc-to-dc converters
- provides auxiliary supply

Generating ringing signal

The system keeps a digital image of a single cycle of each ringing waveform in the waveform store PROM. The control logic selects the correct timing, frequency and amplitude according to the manual settings. The output from the waveform store passes through the digital-to-analog converter and low-pass filter. This action provides the analog input signal for the ringing amplifier card.

Providing ANI and coin outputs

A single dc-to-dc converter provides ±52V and ±130V outputs for ANI and coin functions respectively.

NT6X60DA (continued)

Monitoring ring bus outputs

The NT6X38DA monitors the ring bus output from the NT6X37BA for the output voltage and current. When the system detects ringing overvoltage, the NT6X38DA signals the NT6X37BA to shut down the amplifier. When the system detects ANI or coin overvoltage, the associated converter shuts down. If both events occur, the FSP disconnects primary power.

The monitor circuit also provides transistor-transistor logic (TTL)-level status signals to the RLCM processor. The circuit indicates the ringing voltage (RMS), the ringing current (CUR) and low ANI or coin voltage (ACT). These signals are combined with three status bits from the control logic. The signals and status bits are sent through a serial data link to isolate of the ground reference.

Synchronizing dc-to-dc converters

The dc-to-dc converters in the NT6X37BA must be synchronized to the RLCM system clock. The converter requires 48 KHz synchronization. The RLCM provides 64 KHz. A phase-locked loop converts the frequency. The RLCM synchronization feed and the NT6X37BA synchronization input provides dc isolation of the grounds.

Providing auxiliary supply

A small dc-to-dc converter supplies±15V and 5V for the internal circuits of NT6X38DA. The ±15V is for the control circuits on the NT6X37BA.

Ringing amplifier NT6X37BA

The NT6X37 amplifier is a dc-coupled class B type that uses power FETs as the output devices. Two dc-to-dc converters power the amplifier. The converters allow the ring bus output to independently control the positive and negative supply voltages.

Without ringing output, the supply voltages are at minimum. The minimum is approximately ±20V. Under normal operation, the feedback from the ringing output causes the positive and negative supply voltages to increase alternately. This action occurs so enough voltage is available to produce the required output.

Technical data

Information about ringing appears in the following tables.

International

	Voltage		Freq		Switch	Setting
	ac	dc	(Hz)	Cadence (seconds)	(SW1-4)	12345678
China	86	-52	25	1.25 1.25 1.25 1.25	1 to 4	00111110

Note: The system records symbols under the heading as 0 = ON,1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Switch settings for Japan with LCRLS are for Japanese ringing.

NT6X60DA coded ringing and superimposed ringing

	Voltage		Freq		Switch	Setting
	ac	dc	(Hz)	Cadence (seconds)	(SW1-4)	12345678
1	86	-52	20	2 2 1 1	1 to 4	0000000X
2	86	-38	20	2 2 1 1	1 & 2	0100000X
3	86	+38	20	2 2 1 1	3 & 4	0010000X
4	86	-38	20	2 2 1 1	1 & 2	0001111X
5	86	+38	20	2 2 1 1	3 & 4	0101111X

Information about voltages appears in the following tables.

NT6X60DA frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
16 to 33.33 Hz	+ or - .33 Hz
40 to 66.66 Hz	+ or - 1%
25 Hz international	+ or -.33 Hz
-52V dc	-49.75 to -52.5V dc
-38V dc	+ or - 2V dc
+ 38V dc	+ or - 2V dc

NT6X60DA (end)

NT6X60DA ac voltage tolerances

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8
100	97	103
105	101.9	108.1
110	106.7	113.3
115	111.6	118.4
120	116.4	123.6
125	121.2	128.7
130	126.1	133.9
140	135.8	144.2
155	150.3	159.6

NT6X60DA ANI/coin voltages

Output	Limits
+48V	+ 52V, ±2.5V
- 48V	- 52V, ±5V
+130V	+ 130V, ±5V
-130V	- 130V, ±5V

Power requirements

The NT6X60DA requires -42V to -56V, and a nominal current of 3.5A, to a maximum of 5A. The card consumes 180W of power.

NT6X60DB

Product description

The NT6X60DB ringing generator is a vertical mount version of the ringing generator intended for international markets. The NT6X60DB contains a single card that provides the required functionality. The NT6X60DA (China) and NT6X60AE (Australia) ringing generators required two cards. The is backwards compatible with the NT6X60DA and NT6X60AE.

Location

The NT6X60DB operates in the remote line concentrating module (RLCM) frame supervisory panel (FSP) (NT6X35BA) or the remote line concentrating equipment (RLCE) FSP (NT6X25AA).

Functional description

The NT6X60DB generates the required ringing signals for international markets that include China and Australia.

Functional blocks

To meet international requirements, use the four dual inline package (DIP) switches during installation to manually set ring output frequency and amplitude.

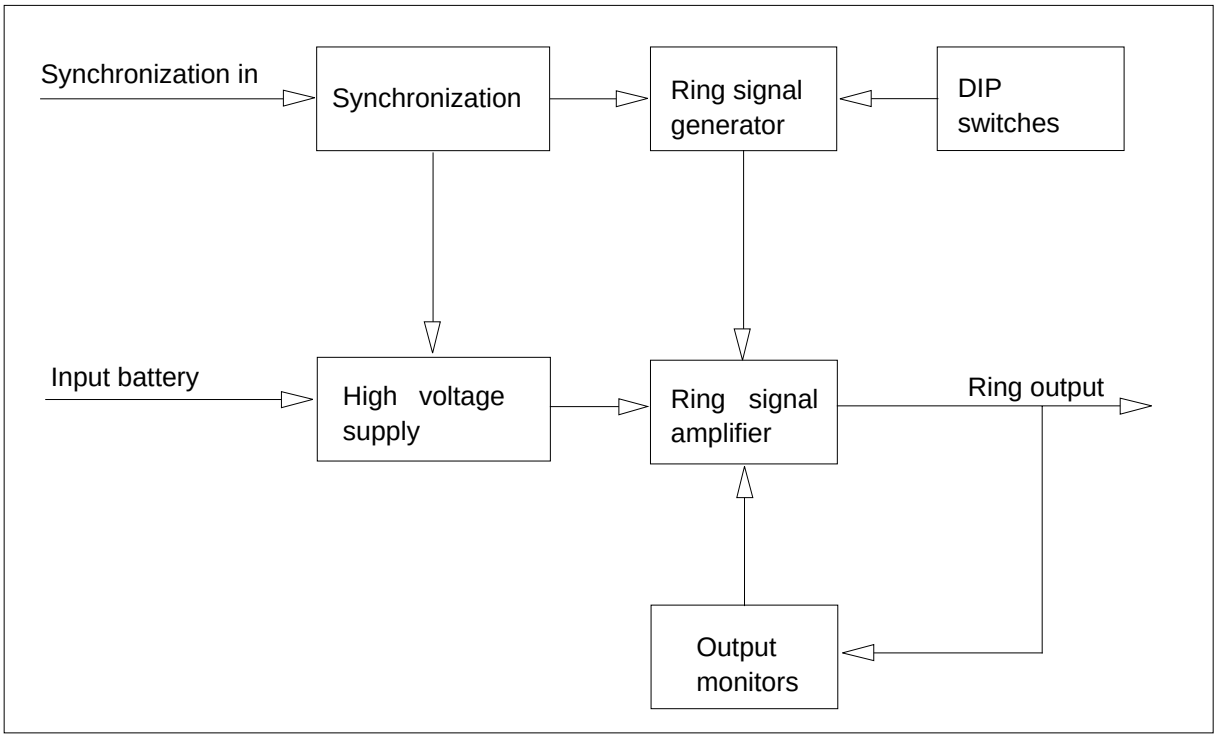
The NT6X60DB contains the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X60DB (continued)

NT6X60DB functional blocks



High voltage supply

The raw battery input voltage is -48V. The system filters the input voltage and feeds the power to a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of a flyback transformer. The system rectifies a secondary flyback transformer and filters the voltage to produce a regulated floating 300V supply. An isolated output produces the voltages to power the ringing control and monitor circuits.

Ring signal generator

A digital image of the ringing waveform is in the programmable read-only memory (PROM) of the microcontroller of the card. The microcontroller sends the correct stream of information to a digital-to-analog converter (DAC) circuit. This action occurs in response to the setting of the DIP switches of the card. The DAC circuit produces a low voltage sinusoidal waveform of the right frequency and right reference amplitude to the ring signal amplifier. This action includes dc offset. The microcontroller provides additional information. The additional information can include zero-crossing detect (XOVER) and cycle cadence information (AF0 and AF1).

Ring signal amplifier

The ringing signal from the ring signal generator is fed to a class D amplifier circuit. This circuit modulates the pulse width to a full-bridge switch configuration. This configuration alternately switches the high voltage floating supply to ground on one side for each half cycle of the output waveform. This action creates a train of variable width pulses. The filtered pulses result in the required sinusoidal ringing output voltage and dc offset. The ringing generator feeds the voltage and dc offset. Compare a sample of the filtered output to the input reference signal from the ring signal generator circuit to regulate this output.

Output monitors

The ringing output and dc offset are monitored for ac overvoltage and undervoltage. If an overvoltage condition occurs, the system disables the ringing amplifier. If an undervoltage condition occurs, the current must be less than the current limit point to allow shutdown.

The monitor circuits provide electrically isolated transistor-transistor logic (TTL) level signals to the RLCM processor. These signals are used to indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the RLCM synchronizes the dc-dc converters and the ringing amplifier on this card. The integer multiple of 8 kHz. This synchronization is electrically isolated from the clock signal that the RLCM provides. This synchronization is isolated between the different converters on this card.

Technical data

Information on NT6X60DB output voltages and tolerances appear in the following tables.

NT6X60DB (continued)

Power requirements

The NT6X60DB requires -39.5V to -75V. The card requires a nominal current of 2A to a maximum of 3A. The card consumes 100W of power.

NT6X60DB international ringing

	Voltage		Freq	Subcycle cadence	Switch	Setting
	ac	dc	(Hz)	(seconds)	(SW1-4)	12345678
Low	67	-52	25	1.95 1.35 1.35 1.35	1 to 4	10001110
Med	75	-52	25	1.95 1.35 1.35 1.35	1 to 4	11001110
High	82	-52	25	1.95 1.35 1.35 1.35	1 to 4	10101110
Low	67	-52	25	2 1 1 1	1 to 4	00001110
Med	75	-52	25	2 1 1 1	1 to 4	01001110
High	82	-52	25	2 1 1 1	1 to 4	00101110
Japan	76	0	16	2 2 1 1	1 to 4	11101110
U.K.	75	-52	25	1 1 0.4 0.6	1 to 4	01101110
China	86	-52	25	1.25 1.25 1.25 1.25	1 to 4	00111110
Brazil	86	-52	25	1.25 1.25 1.25 1.25	1 to 4	00111110
Australia	90	-52	25	1 1 0.40 0.60	1 to 4	01111110
Morocco	80	-52	50	1.70 1.70 0.80 0.80	1 to 4	10111110
Germany	65	-60	25	2 2 1 1	1 to 4	11111110
Philippines	90	-52	20	1.25 1.25 1.25 1.25	1 to 4	11110110

Note: The system records the symbols under the heading as 0 = ON,1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF.

NT6X60DB international coded and superimposed ringing

	Voltage		Freq	Subcycle cadence	Switch	Setting
	ac	dc	(Hz)	(seconds)	(SW1-4)	12345678
1	86	-52	20	2 2 1 1	1 to 4	00000000
2	86	-38	20	2 2 1 1	1 & 2	01000000
3	86	+38	20	2 2 1 1	3 & 4	00100000
4	86	-38	20	2 2 1 1	1 & 2	00011110
5	86	+38	20	2 2 1 1	3 & 4	01011110

Frequency/dc voltage	Tolerances
16 to 33.33 Hz	+ or - .33 Hz
40 to 66.66 Hz	+ or - 1%
25 Hz international	+ or - .33 Hz
-52V (dc)	-49.5 to -53.5V (dc)
-38V (dc)	+ or - 2V (dc)
+ 38V (dc)	+ or - 2V (dc)

NT6X60DB international ac voltage tolerances

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8

NT6X60DB (continued)

Signaling

Pin numbers

The pin numbers for the NT6X60DB card edge connector (P4) appear in the following table.

NT6X60DB pin numbers (Sheet 1 of 2)

P4 pin	Signal
55B	AF0
60A	LOGIC GND
49B	AF1
60B	LOGIC GND
48A	ACT
61A	LOGIC GND
54B	XOVER
61B	LOGIC GND
54A	RMS
62A	LOGIC GND
50B	CUR
62B	LOGIC GND
63A	LOGIC GND
47A	FSPLINK
76B, 76A	-48V
79A	BR
77A	-48V
79B	BR
77B	-48V
80A, 80B	BR
58A	ABS -48V

NT6X60DB pin numbers (Sheet 2 of 2)

P4 pin	Signal
59B	FSPMON
63B	LOGIC GND
49A	SYNC 64
75B	RRING
73A	RTIP
75A	RRING
73B, 56A, 57A, 57B	RTIP
53A	NC
70A	ABS BR
55A	NC
56B	NC
58B	NC

NT6X60EA

Product description

The NT6X60EA ringing generator is a thin vertical mount version of the ringing generator for international markets. The contains a single card that contains all of the requirements.

Location

The NT6X60EA is in one of the shelves of the small remote unit (SRU), a DMS100 product.

Functional description

The NT6X60EA generates the required ringing signals for international markets that include China and Australia.

Functional blocks

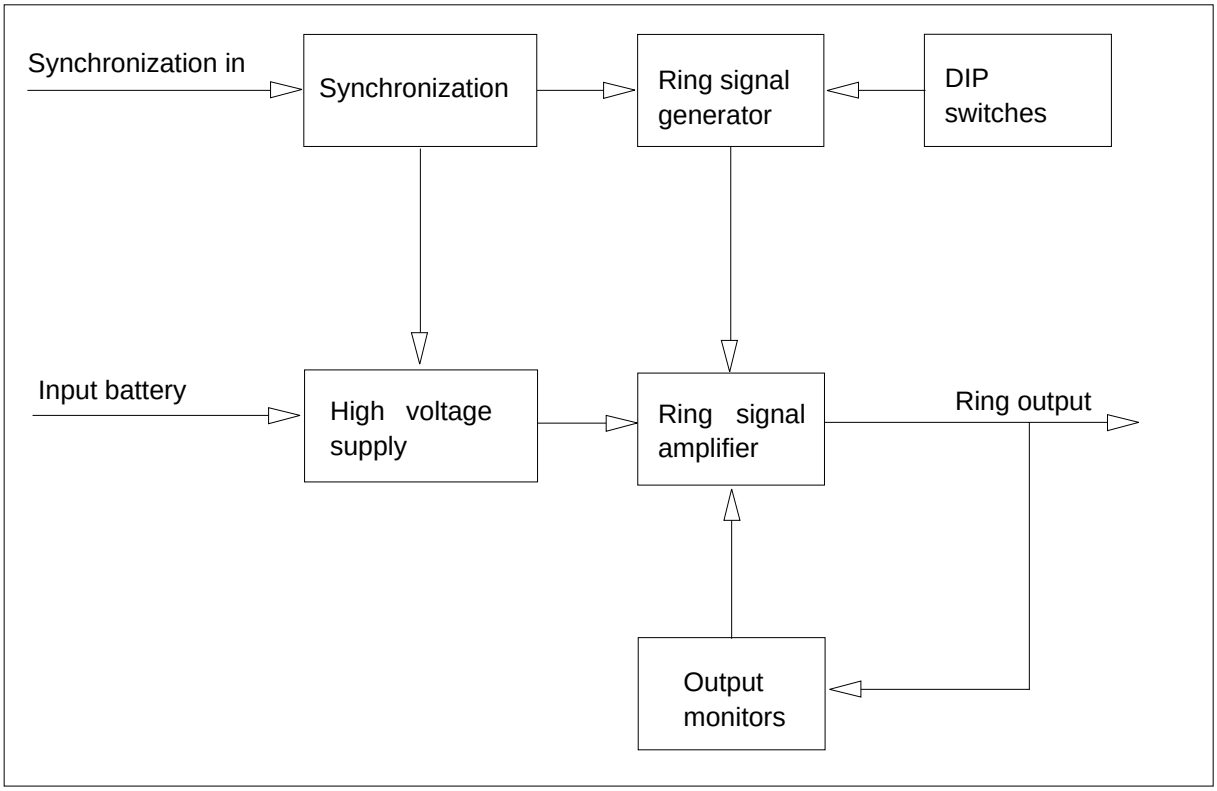
To meet international requirements, the four dual inline package (DIP) switches are set manually during installation, ring output frequency and amplitude.

The NT6X60EA has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X60EA functional blocks



High voltage supply

The the raw battery input voltage is -48V. The system filters and feeds the power supply to a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of a flyback transformer. The system rectifies a secondary flyback transformer and filters the voltage to produce a regulated floating 300V supply. An isolated output produces the voltages required to power the ringing control and monitor circuits.

Ring signal generator

A digital image of the ringing waveform is in the programmable read-only memory (PROM) of the microcontroller of the card. The microcontroller sends the correct stream of digital information to a digital-to-analog converter (DAC) circuit. This action sets the DIP switches of the card. The DAC circuit produces a low voltage sinusoidal waveform of the right frequency and reference amplitude to the ring signal amplifier. This action includes dc offset. The microcontroller provides additional information. The additional information can include zero-crossing detect (XOVER) and cycle cadence information (AF0 and AF1).

NT6X60EA (continued)

Ring signal amplifier

The ringing signal from the ring signal generator is fed to a class D amplifier circuit. The circuit modulates the pulse width to a full-bridge switch configuration. This configuration alternately switches the high voltage floating supply to ground on one side for each half cycle of the output waveform. This action creates a train of variable width pulses. These pulses provide the required sinusoidal ringing output voltage and dc offset. The voltage and dc offset are fed from the ringing generator. Compare a sample of the filtered output to the input reference signal from the ring signal generator circuit to regulate this output.

Output monitors

The system monitors the ringing output and dc offset for ac overvoltage and undervoltage. If an overvoltage condition arises, the system disables ringing amplifier. If an undervoltage condition occurs, the current must be less than the current limit point to allow shutdown.

The monitor circuits provide electrically isolated transistor-transistor logic (TTL) level signals to the line concentrating module (LCM) processor. These signals indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the LCMAll synchronizes the dc-dc converters and the ringing amplifier on this card. The integer is a multiple of 8 kHz. This synchronization is electrically isolated from the clock signal the LCM provides. This synchronization is isolated between the different converters on this card.

Technical data

Information on output voltages appears in the following tables.

Power requirements

The requires -39.5V to -75V, and a nominal current of 2A to a maximum of 3A. The card consumes 100W of power.

NT6X60EA international ringing

	Voltage		Freq	Subcycle cadence	Switch	Setting
	ac	dc	(Hz)	(seconds)	(SW1-4)	12345678
Low	67	-52	25	1.95 1.35 1.35 1.35	1 to 4	10001110
Med	75	-52	25	1.95 1.35 1.35 1.35	1 to 4	11001110
High	82	-52	25	1.95 1.35 1.35 1.35	1 to 4	10101110
Low	67	-52	25	2 1 1 1	1 to 4	00001110
Med	75	-52	25	2 1 1 1	1 to 4	01001110
High	82	-52	25	2 1 1 1	1 to 4	00101110
Japan	76	0	16	2 2 1 1	1 to 4	11101110
U.K.	75	-52	25	1 1 0.4 0.6	1 to 4	01101110
China	86	-52	25	1.25 1.25 1.25 1.25	1 to 4	00111110
Brazil	86	-52	25	1.25 1.25 1.25 1.25	1 to 4	00111110
Australia	90	-52	25	1 1 0.40 0.60	1 to 4	01111110
Morocco	80	-52	50	1.70 1.70 0.80 0.80	1 to 4	10111110
Germany	65	-60	25	2 2 1 1	1 to 4	11111110
Philippines	90	-52	20	1.25 1.25 1.25 1.25	1 to 4	11110110

Note: The symbols under the heading for 0 = ON,1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF.

NT6X60EA (continued)

NT6X60EA international coded and superimposed ringing

	Voltage					
	ac	dc	Freq (Hz)	Subcycle cadence (seconds)	Switch (SW1-4)	Setting 12345678
1	86	-52	20	2 2 1 1	1 to 4	00000000
2	86	-38	20	2 2 1 1	1 & 2	01000000
3	86	+38	20	2 2 1 1	3 & 4	00100000
4	86	-38	20	2 2 1 1	1 & 2	00011110
5	86	+38	20	2 2 1 1	3 & 4	01011110

NT6X60EA international frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
16 to 33.33 Hz	+ or - .33 Hz
40 to 66.66 Hz	+ or - 1%
25 Hz international	+ or - .33 Hz
-52V (dc)	-49.5 to -53.5V (dc)
-38V (dc)	+ or - 2V (dc)
+ 38V (dc)	+ or - 2V (dc)

NT6X60EA international ac voltage tolerances

Nominal	Low	High
67	65	69
75	73	77
82	80	84
86	84	88
90	87.3	92.7
95	92.1	97.8

Signaling

Pin numbers

The pin numbers for the NT6X60EA card edge connector (P4) appear in the following table.

NT6X60EA (Sheet 1 of 2)

P4 pin	Signal
55B	AF0
60A	LOGIC GND
49B	AF1
60B	LOGIC GND
48A	ACT
61A	LOGIC GND
54B	XOVER
61B	LOGIC GND
54A	RMS
62A	LOGIC GND
50B	CUR
62B	LOGIC GND
63A	LOGIC GND
47A	FSPLINK
76B, 76A	-48V
79A	BR
77A	-48V
79B	BR
77B	-48V
80A, 80B	BR
58A	ABS -48V

NT6X60EA (end)

NT6X60EA (Sheet 2 of 2)

P4 pin	Signal
59B	FSPMON
63B	LOGIC GND
49A	SYNC 64
75B	RRING
73A	RTIP
75A	RRING
73B, 56A, 57A, 57B	RTIP
53A	NC
70A	ABS BR
55A	NC
56B	NC
58B	NC

NT6X60FA

Product description

The NT6X60FA ringing generator is a vertical mount version of the ringing generator for the United Kingdom market. The NT6X60FA contains a single card that provides the required functionality. The NT6X60AB ringing generator required two cards. The NT6X60FA is backwards compatible with the NT6X60AB.

Location

The NT6X60DB operates in the remote line concentrating module (RLCM) frame supervisory panel (FSP) (NT6X35BA) or the remote line concentrating equipment (RLCE) FSP (NT6X25AA).

Functional description

The NT6X60FA generates the required ringing signals for the United Kingdom market.

Functional blocks

Ring output frequency and amplitude are set at the factory to meet United Kingdom requirements.

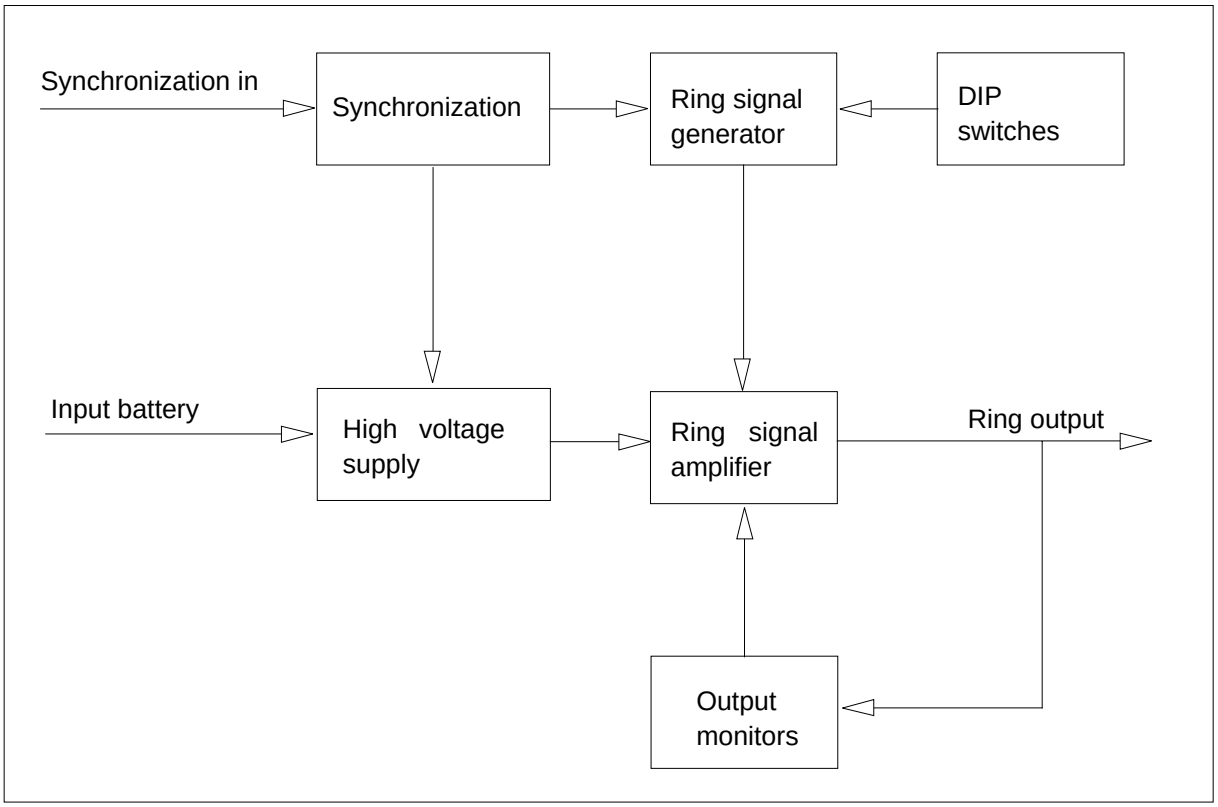
The NT6X60FA has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X60FA (continued)

NT6S60FA functional blocks



High voltage supply

The raw battery input voltage is -48V. The system filters and feeds the power supply into a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of a flyback transformer. The system rectifies a secondary flyback transformer and filters the voltage to produce a regulated floating 300V supply. An isolated output produces the voltages that power the ringing control and monitor circuits.

Ring signal generator

A digital image of the ringing waveform is in the programmable read-only memory (PROM) of the microcontroller of the card. The microcontroller sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. This action is in response to the setting of the DIP switches of the card. The DAC circuit produces a low voltage sinusoidal waveform of the right frequency and right reference amplitude to the ring signal amplifier. This action includes dc offset. The microcontroller provides additional information. The additional information can include zero-crossing detect (XOVER) and cycle cadence information (AF0 and AF1).

Ring signal amplifier

The ringing signal from the ring signal generator is fed into a class D amplifier circuit. The circuit modulates the pulse width to a full-bridge switch configuration. This configuration alternately switches the high voltage floating supply to ground on one side for each half cycle of the output waveform. This action creates a train of variable width pulses. These pulses produce the required sinusoidal ringing output voltage and dc offset. The voltage and dc offset are fed from the ringing generator. Compare a sample of the filtered output to the input reference signal from the ring signal generator circuit to regulate this output.

Output monitors

The ringing output and dc offset are monitored for ac overvoltage and undervoltage. If an overvoltage condition arises, the system disables the ringing amplifier. If an undervoltage condition occurs, the current must be less than the current limit point to allow shutdown.

The monitor circuits provide electrically isolated transistor-to-transistor logic (TTL) level signals to the RLCM processor. The signals are used to indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the RLCM synchronizes all dc-dc converters and the ringing amplifier on this card. The integer is a multiple of 8 kHz. This synchronization is electrically isolated from the clock signal the RLCM provides. This synchronization is isolated between the different converters on this card.

Technical data

Information on NT6X60FA output voltages and tolerances appear in the following tables.

NT6X60FA (continued)

Power requirements

The NT6X60FA requires -39.5V to -75V. The nominal current is 1A to a maximum of 2A. The card consumes 75W of power.

NT6X60FA international ringing

	Voltage		Freq	Subcycle cadence	Switch	Setting
	ac	dc	(Hz)	(seconds)	(SW1-4)	12345678
U.K.	75	-52	25	1 1 0.4 0.6	1 to 4	01101110
Note: The system records the symbols under the heading as 0 = ON,1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF.						

NT6X60FA international frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
25 Hz international	+ or - .33 Hz
-52V (dc)	-49.75 to -52.5V (dc)

NT6X60FA international ac voltage tolerances

Nominal	Low	High
75	73	77

Signaling

Pin numbers

The pin numbers for the NT6X60FA card edge connector (P4) appear in the following table.

NT6X60FA pin numbers (Sheet 1 of 3)

P4 pin	Signal
55B	AF0
60A	LOGIC GND
49B	AF1
60B	LOGIC GND
48A	ACT
61A	LOGIC GND

NT6X60FA pin numbers (Sheet 2 of 3)

P4 pin	Signal
54B	XOVER
61B	LOGIC GND
54A	RMS
62A	LOGIC GND
50B	CUR
62B	LOGIC GND
63A	LOGIC GND
47A	FSPLINK
76B, 76A	-48V
79A	BR
77A	-48V
79B	BR
77B	-48V
80A, 80B	BR
58A	ABS -48V
59B	FSPMON
63B	LOGIC GND
49A	SYNC 64
75B	RRING
73A	RTIP
75A	RRING
73B, 56A, 57A, 57B	RTIP
53A	NC
70A	ABS BR

NT6X60FA (end)

NT6X60FA pin numbers (Sheet 3 of 3)

P4 pin	Signal
55A	NC
56B	NC
58B	NC

NT6X60GA

Product description

The NT6X60GA ringing generator is a thin vertical mount version of the ringing generator intended for the United Kingdom market. The NT6X60GA contains a single card provides all the required functionality.

Location

The MT6X60GA is in one of the shelves of the small remote unit (SRU), a DMS-100 product.

Functional description

The NT6X60GA generates the required ringing signals for the United Kingdom.

Functional blocks

Ring output frequency and amplitude are set at the factory to meet United Kingdom requirements.

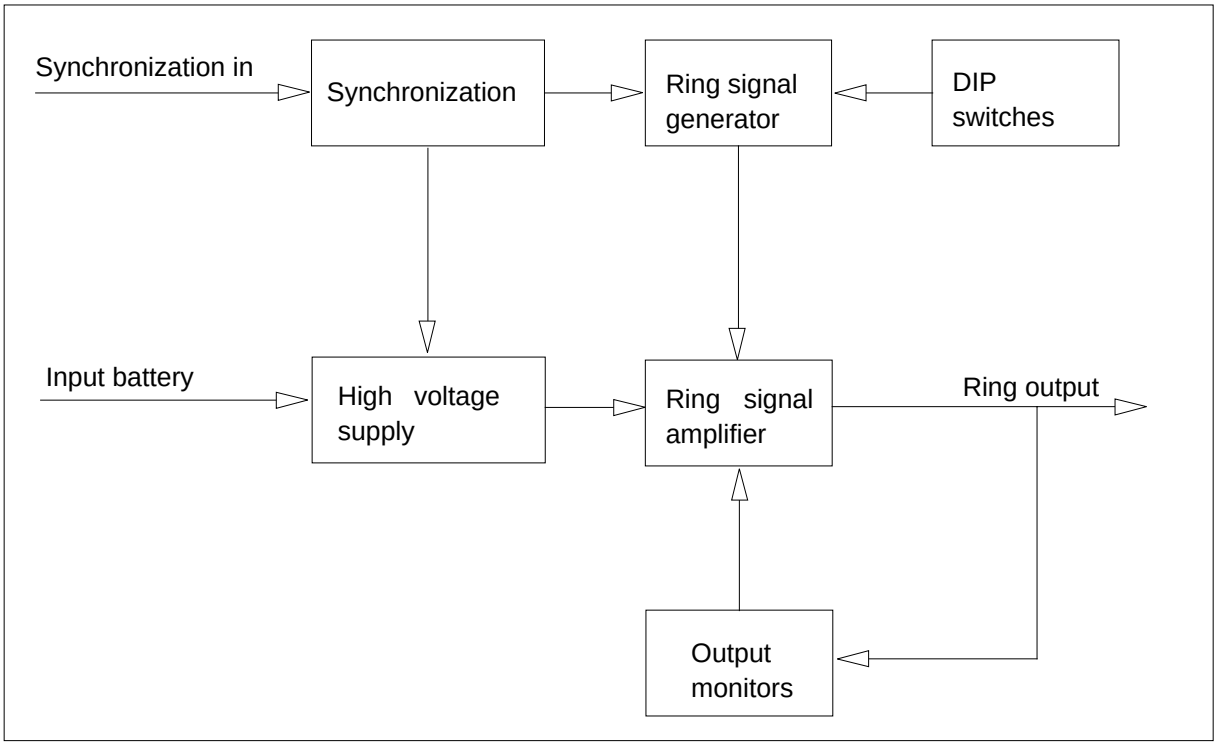
The NT6X60GA has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X60GA (continued)

NT6X60GA functional blocks



High voltage supply

The raw battery input voltage is -48 V. The system filters and feeds the power supply into a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of a flyback transformer. The system rectifies a secondary flyback transformer and filters the voltage to produce a regulated floating 300V supply. An isolated output produces the voltages that power the ringing control and monitor circuits.

Ring signal generator

A digital image of the ringing waveform is in the programmable read-only memory (PROM) of the microcontroller of the card. The microcontroller sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. This action is in response to the setting of the DIP switches of the card. The DAC circuit produces a low voltage sinusoidal waveform of the right frequency and reference amplitude to the ring signal amplifier. This action includes dc offset. The microcontroller provides additional information. The additional information can include zero-crossing detect (XOVER) and cycle cadence information (AF0 and AF1).

Ring signal amplifier

The ringing signal from the ring signal generator is fed into a class D amplifier circuit. The circuit modulates the pulse width to a full-bridge switch configuration. This configuration alternately switches the high voltage floating supply to ground on one side for each half cycle of the output waveform. This action creates a train of variable width pulses. These pulses produce the required sinusoidal ringing output voltage and dc offset. The voltages and dc offset are fed from the ringing generator. Compare a sample of the filtered output to the input reference signal from the ring signal generator circuit to regulate this output.

Output monitors

The ringing output and dc offset are monitored for ac overvoltage and undervoltage. If an overvoltage condition arises, the system disables the ringing amplifier. If an undervoltage condition occurs, the current must be less than the current limit point to allow shutdown.

The monitor circuits provide electrically isolated transistor-to-transistor logic (TTL) level signals to the LCM processor. These signals are used to indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the LCM synchronizes dc-dc converters and the ringing amplifier on this card. The integer is a multiple of 8 kHz. This synchronization is electrically isolated from the clock signal the LCM provides. This synchronization is isolated between the different converters on this card.

Technical data

Information on NT6X60GA output voltages appear in the following tables.

Power requirements

The NT6X60GA requires -39.5V to -75V. The nominal current is 1A to a maximum of 2A. The card consumes 75W of power.

NT6X60GA international ringing

	Voltage		Freq	Subcycle cadence	Switch	Setting
	ac	dc	(Hz)	(seconds)	(SW1-4)	12345678
U.K.	75	-52	25	1 1 0.4 0.6	1 to 4	01101110

Note: The system records the symbols under the heading as 0 = ON,1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF.

NT6X60GA (continued)

NT6X60GA international frequency and dc voltage tolerances

Frequency/dc voltage	Tolerances
25 Hz international	+ or - .33 Hz
-52V (dc)	-49.75 to -52.5V (dc)

NT6X60GA international ac voltage tolerances

Nominal	Low	High
75	73	77

Signaling

Pin numbers

The pin numbers for the NT6X60GA card edge connector (P4) appear in the following table.

NT6X60GA pin numbers (Sheet 1 of 2)

P4 pin	Signal
55B	AF0
60A	LOGIC GND
49B	AF1
60B	LOGIC GND
48A	ACT
61A	LOGIC GND
54B	XOVER
61B	LOGIC GND
54A	RMS
62A	LOGIC GND
50B	CUR
62B	LOGIC GND
63A	LOGIC GND
47A	FSPLINK

NT6X60GA pin numbers (Sheet 2 of 2)

P4 pin	Signal
76B, 76A	-48V
79A	BR
77A	-48V
79B	BR
77B	-48V
80A, 80B	BR
58A	ABS -48V
59B	FSPMON
63B	LOGIC GND
49A	SYNC 64
75B	RRING
73A	RTIP
75A	RRING
73B, 56A, 57A, 57B	RTIP
53A	NC
70A	ABS BR
55A	NC
56B	NC
58B	NC

NT6X60GB

Product description

The NT6X60GB ringing generator is a low-profile, vertical-mount version of the ringing generator intended for the European market. The NT6X60GB contains a single card, which provides the required functionality.

Location

The NT6X60GB is in one of the shelves of the small remote unit (SRU), a DMS-100 MMP product.

Functional description

The NT6X60GB generates a single continuous ringing waveform from a selection of ringing signals that meet the European market requirements.

Functional blocks

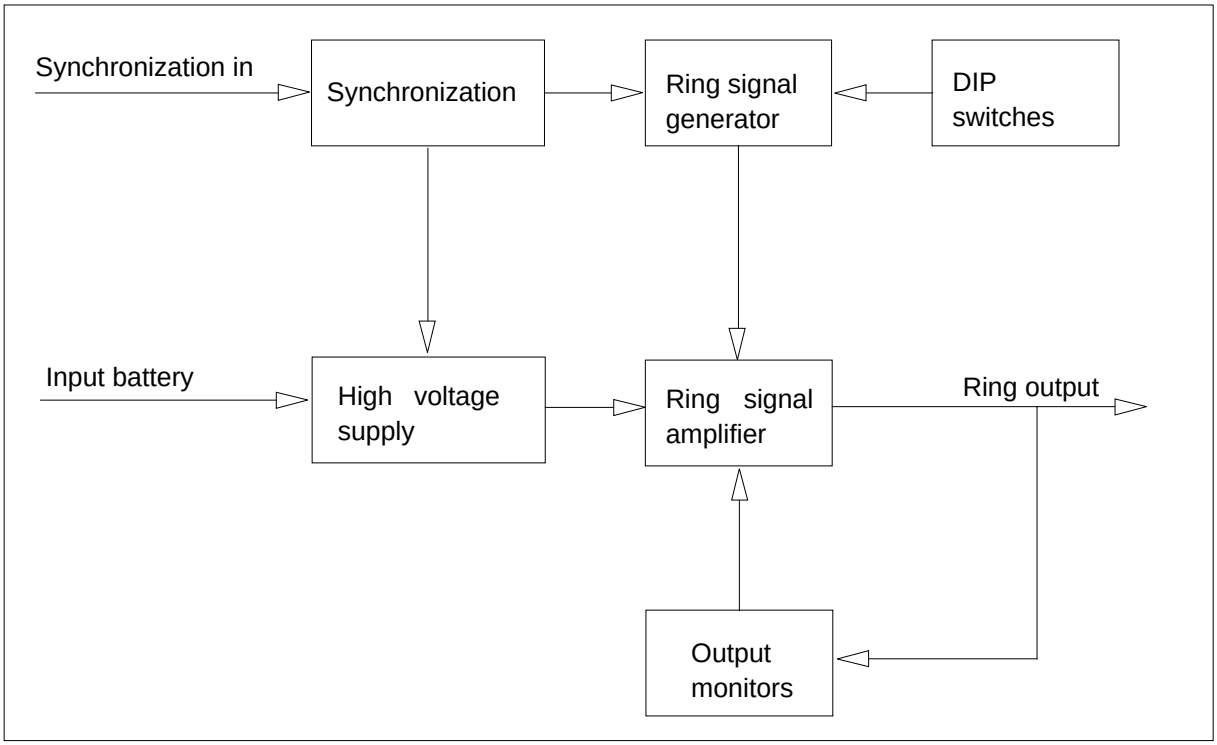
Ring output frequency and amplitude are set at the factory to meet United Kingdom requirements.

The NT6X60GB has the following functional blocks:

- high voltage supply
- ring signal generator
- ring signal amplifier
- output monitors
- synchronization

The relationship between the functional blocks appears in the following figure.

NT6X60GB functional blocks



High-voltage supply

This circuit filters the raw battery voltage (-48 V dc nominal) and feeds this voltage into a single-transistor isolated boost converter topology. This square-wave switches the input voltage across the primary of a flyback transformer. The system rectifies a secondary flyback transformer and filters the voltage to produce a regulated floating 300 V supply. The ringing control and the monitor circuits require separate low voltages for power. Isolated outputs on this supply provide these voltages.

Ring-signal generator

The programmable read-only memory (PROM) of the card's microcontroller stores a digital image that represents the ringing waveform, along with information that allows interpretation of the settings of the on-board dual in-line package (DIP) selection switches. Based on the switch settings, the microcontroller sends the correct stream of digital information to the digital-to-analog converter (DAC) circuit. This action is in response to the setting of the DIP switches of the card. The DAC circuit produces a low voltage sinusoidal waveform of the right frequency and reference amplitude to the ring signal amplifier. This action includes dc offset. The microcontroller

NT6X60GB (continued)

provides additional information. The additional information can include zero-crossing detect (XOVER) and cycle cadence information (AF0 and AF1).

Ring-signal amplifier

The ringing signal from the ring-signal generator is fed into a class D amplifier circuit. The circuit modulates the pulse width to a full-bridge switch configuration. This configuration alternately switches the high voltage floating supply to ground on one side for each half cycle of the output waveform. This action creates a train of variable width pulses. These pulses produce the required sinusoidal ringing output voltage and dc offset. The voltages and dc offset are fed from the ringing generator. A sample of the filtered output is compared to the input reference signal from the ring-signal generator circuit. This comparison is used to regulate the ringing output.

Output monitors

The ringing output and dc offset are monitored for ac overvoltage and undervoltage. If an overvoltage condition arises, the system disables the ringing amplifier. If an undervoltage condition occurs, the current must be less than the current limit point to allow shutdown. These circuits also monitor the output current of the card and send a signal to the system when the load current exceeds approximately ninety percent of its rating. When the load current exceeds the rated load current, the card goes into current limit and the output voltage decreases. The card does not shut down, but continues to try to support the load. If the overload condition is removed, the output voltage is automatically restored to its expected level.

The monitor circuits provide electrically isolated transistor-to-transistor logic (TTL) level signals to the LCM processor. These signals are used to indicate low ringing voltage (RMS-bit) and excess ringing output current (CUR-bit).

Synchronization

A phase-lock loop to the clock frequency of the LCM synchronizes dc-dc converters and the ringing amplifier on this card. The integer is a multiple of 8 kHz. This synchronization is electrically isolated from the clock signal the LCM provides. This synchronization is isolated between the different converters on this card.

Signaling

Pin numbers

The pin numbers for the NT6X60GB card edge connector (P4) appear in the following table.

NT6X60GB pin numbers (Sheet 1 of 2)

P4 pin	Signal
47A	FSPLINK
48A	ACT
49A	SYNC64
49B	AF1
50B	CUR
51B	NC
53A	NC
54A	RMS
54B	XOVER
55A	NC
55B	AF0
56A	RTIP
56B	NC
57A	RTIP
57B	RTIP
58A	LEDPOWER
58B	NC
59A	FSPMON
59B	FSPMON
60A	LOGIC GND
60B	LOGIC GND

NT6X60GB (continued)

NT6X60GB pin numbers (Sheet 2 of 2)

P4 pin	Signal
61A	LOGIC GND
61B	LOGIC GND
62A	LOGIC GND
62B	LOGIC GND
63A	LOGIC GND
63B	LOGIC GND
70A	ABSBR
73A	RTIP
73B	RTIP
74A	RTIP
74B	RTIP
75A	RRING
75B	RRING
76A	-48 V
76B	-48 V
77A	-48 V
77B	-48 V
79A	BR
79B	BR
80A	BR
80B	BR

Technical data

Information on NT6X60GB output voltages appear in the following tables.

Power requirements

The NT6X60GB requires -39.5 V to -75 V, and a nominal current of 2 A to a maximum of 3 A. The NT6X60GB consumes 100 W of power.

NT6X60GB European ring codes

	Voltage		Frequency (Hz)	Subcycle cadence (seconds)	Switch (SW1-4)	Setting 12345678
	ac	dc				
Austria	65	-60	50	2 2 1 1	1 to 4	10000110
Belgium	75	-52	25	0.76 0.76 1 1.48	1 to 4	10000011
Europe (includes Finland, Italy, Luxembourg, Netherlands, Russia)	75	-52	25	1.64 1.64 0.64 1.08	1 to 4	10000000
France/ Slovakia	75	-52	50	1.66 1.66 0.84 0.84	1 to 4	10000010
Germany	65	-60	25	2 2 1 1	1 to 4	01111111
Portugal/ Iceland/ Sweden	75	-52	25	2 2 1 1	1 to 4	10000101
Spain	75	-52	25	1.52 1.52 0.92 0.52	1 to 4	10000100
Switzerland/ Norway/ Czech Republic	70	-52	25	1.64 1.64 0.64 1.08	1 to 4	10000001
UK and Ireland	75	-52	25	1 1 0.4 0.6	1 to 4	01110110

Note: The interpretation of the symbols under the heading settings is 0 = ON, 1 = OFF. The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF.

NT6X62AA

Product description

The NT6X62AA detects the digits necessary to invoke a reorigination feature. The card interfaces with the transmit pulse code modulation (XPCM) parallel speech bus. The card interfaces with the signal processor (SP) bus in the digital trunk controller (DTC). The system returns specialized tone receiver (STR) detection results to the SP through the associated bus.

Location

The NT6X62AA occupies slots 16 or 17 of the DTC.

Functional description

Functional blocks

The NT6X62AA has the following functional blocks:

- parallel speech bus interface
- input tone sample buffer
- digital signal processor (DSP)
- local processor (LP)
- SP interface
- timing and control

Parallel speech bus interface

The system receives tone samples from the XPCM parallel speech bus. The STR can buffer tone information in the DTC. Channels 0 and 16 of the XPCM bus contain control information and are not used for tone reception. Of the other channels, ports 16 through 19 are not normally used for STR tone reception. These ports are for shared resource functions, like tone generation and universal tone receiver tone reception.

Input tone sample buffer

The input buffer collects tone samples for the channels. The buffer is 128 kbytes in size and is divided in 512 channels. The buffer always contains the last 256 samples. During the read process, the system can read the content of RAM every 195 ns. The system can present this content to the DSP during the read process.

The input buffer arbiter takes requests from sources in the following order of priority:

1. read sequencer
2. write sequencer
3. local processor

Digital signal processor

The DSP filters tone samples from the input buffer at selected frequencies. The DSP first evaluates the outputs of these filters for level-related conditions. The LP evaluates the outputs of these filters for timing-related parameters.

The algorithm that the STR DSP uses has the following steps:

1. correlation also known as filtering or modified hilbert transform
2. linear to DB conversion
3. threshold comparison

Local processor

The main functions of the local processor (LP) are as follows:

- update the code map RAM that controls the DSP
- collect DSP evaluation results
- analyze the results
- return results to the SP
- receive instructions from the SP
- service error conditions on the card and, if possible, report the conditions to the SP
- control and service the serial communications link to a diagnostics and control terminal that attaches to the multifunction peripheral chip

Signal processor interface

Communication between the LP and the SP uses a common memory design. The LP main memory allows access from the STR LP and the SP. Use of a bus arbitration technique avoids bus contention.

Communication occurs in one of the following methods:

- the STR uses the report message queue to return digit detection results
- the SP uses the control message queue to issue commands to the LP

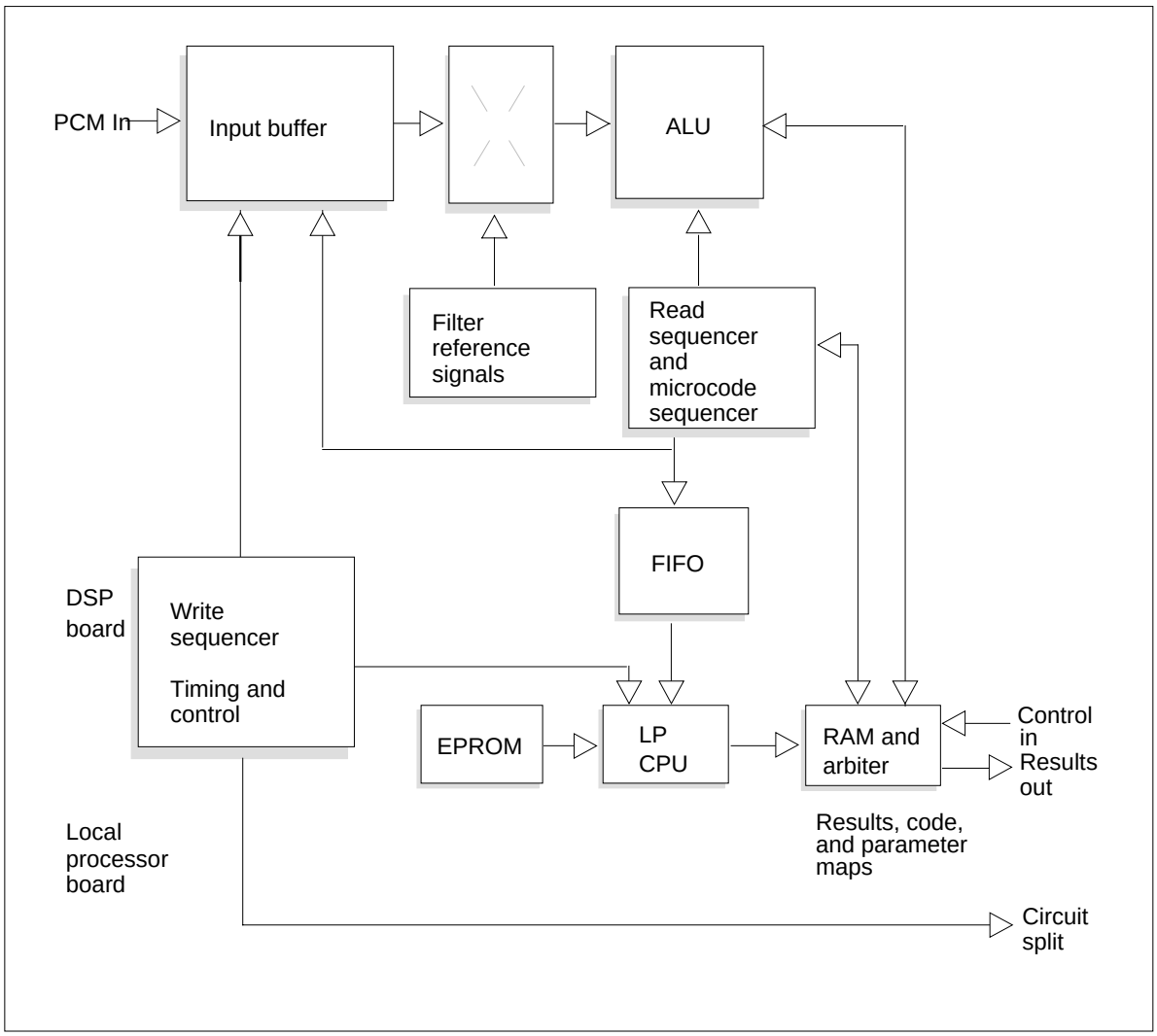
NT6X62AA (continued)

Timing and control

The system extracts tone samples from the parallel speech bus at the appropriate time slot. The input buffer stores the samples. The system passes samples of each channel through the DSP several times. This process, known as filtering, combines frequency conversion and low-pass filtering.

The relationship between the functional blocks appears in the following figure.

NT6X62AA functional blocks

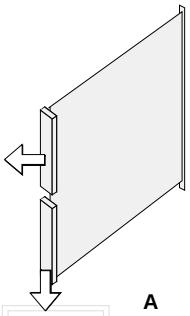


Signaling

Pin numbers

The NT6X62AA pin numbers from card connector P1 on the main printed circuit board appear in the following figure. These pin numbers reflect external connections to the equipment shelf. Card connectors P2 through P5 interface between the main printed circuit board and the daughter board.

NT6X62AA (continued)



	A	B
1A 1B	GND	GND
2A 2B	PWR+5	PWR+5
3A 3B	PWR+5	PWR+5
4A 4B	PWR+5	PWR+5
5A 5B	GND	GND
6A 6B	FP–	C97
7A 7B	GND	GND
8A 8B		
9A 9B		
10A10B		
11A11B	GND	GND
12A12B	SDAS–	
13A13B	SLDS–	
14A14B	SDTACK–	
15A15B	SUDS–	
16A16B	SRWT–	
17A17B		
18A18B	SRSTOUT–	
19A19B		
20A20B		
21A21B	PIN0	
22A22B	PIN1	
23A23B	PIN2	
24A24B	PIN3	
25A25B	PIN4	
26A26B	PIN5	
27A27B	PIN6	
28A28B	PIN7	
29A29B	SADDR01+	
30A30B	SADDR02+	
31A31B	SADDR03+	
32A32B	SADDR04+	
33A33B	SADDR05+	
34A34B	GND	GND
35A35B	SADDR06+	
36A36B	SADDR07+	
37A37B	SADDR08+	
38A38B	SADDR09+	
39A39B	SADDR10+	
40A40B	SADDR11+	RTIME

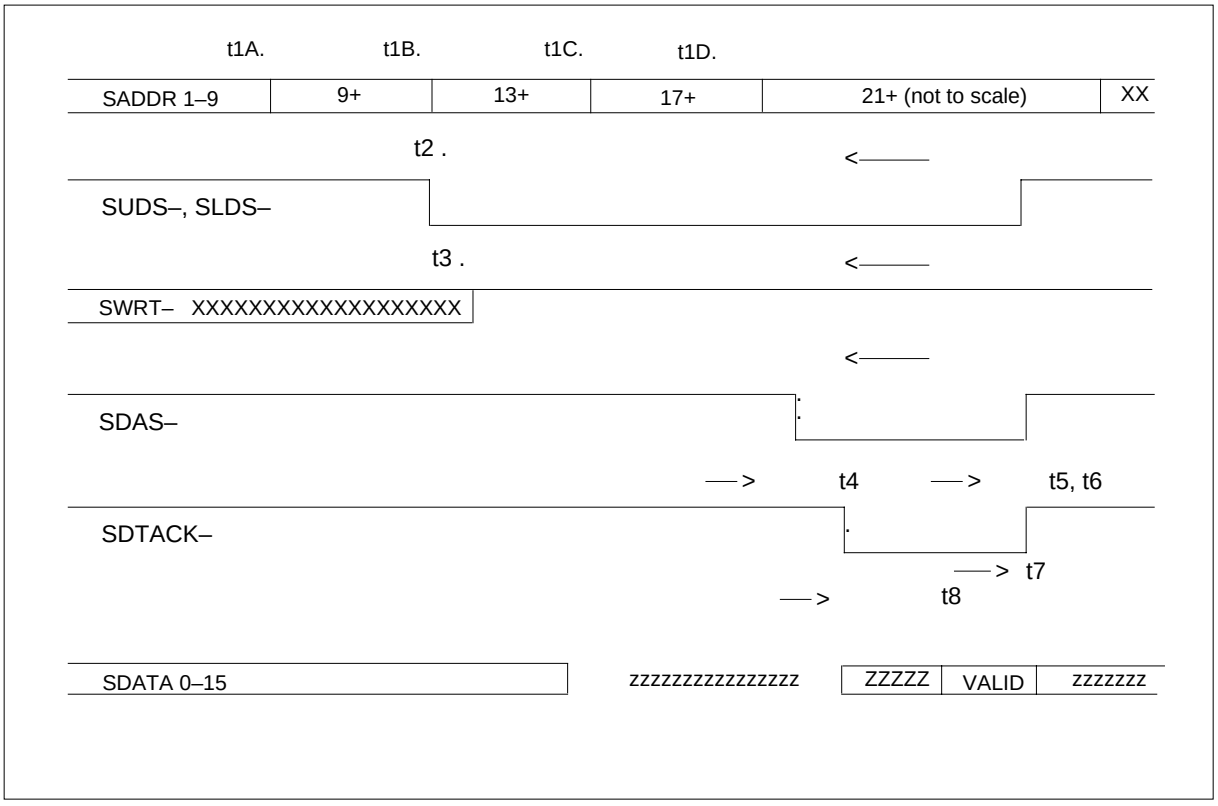
	A	B
41A41B		
42A42B	SADDR12+	
43A43B	SADDR13+	
44A44B	SADDR14+	
45A45B	SADDR15+	
46A46B	SADDR16+	
47A47B	SADDR17+	
48A48B	SADDR18+	ADM17+
49A49B	SADDR19+	ADM18+
50A50B	SADDR20+	ADM19+
51A51B	SADDR21+	
52A52B		
53A53B		
54A54B		
55A55B		
56A56B		
57A57B		
58A58B	SDATA00+	
59A59B	SDATA01+	
60A60B	SDATA02+	
61A61B	SDATA03+	
62A62B	SDATA04+	GND
63A63B	SDATA05+	
64A64B	GND	GND
65A65B	SDATA06+	
66A66B	SDATA07+	
67A67B	SDATA08+	
68A68B	SDATA09+	RXD
69A69B	SDATA10+	
70A70B	SDATA11+	CHSPLIT–
71A71B	SDATA12+	
72A72B	SDATA13+	
73A73B	SDATA14+	
74A74B	SDATA15+	
75A75B		TXD
76A76B	GND	GND
77A77B	PWR+12	PWR+12
78A78B	GND	GND
79A79B	PWR–12	PWR–12
80A80B	GND	GND

Technical data

Timing

The SP basic read-cycle timing diagram for the NT6X62AA appears in the following table.

NT6X62AA SP basic read cycle (asynchronous)



The read-cycle timing values for the NT6X62AA appear in the following table.

Read-cycle timing values (Sheet 1 of 2)

Item	Description	Min	Max
t1A	ADDR(1-9)+ valid to SDAS- low	112	
t1B	ADDR(10-13)+ valid to SDAS- low	47	
t1C	ADDR(14-17)+ valid to SDAS- low	37	
Note: Minimum and maximum times are in nanoseconds unless otherwise noted.			

NT6X62AA (continued)

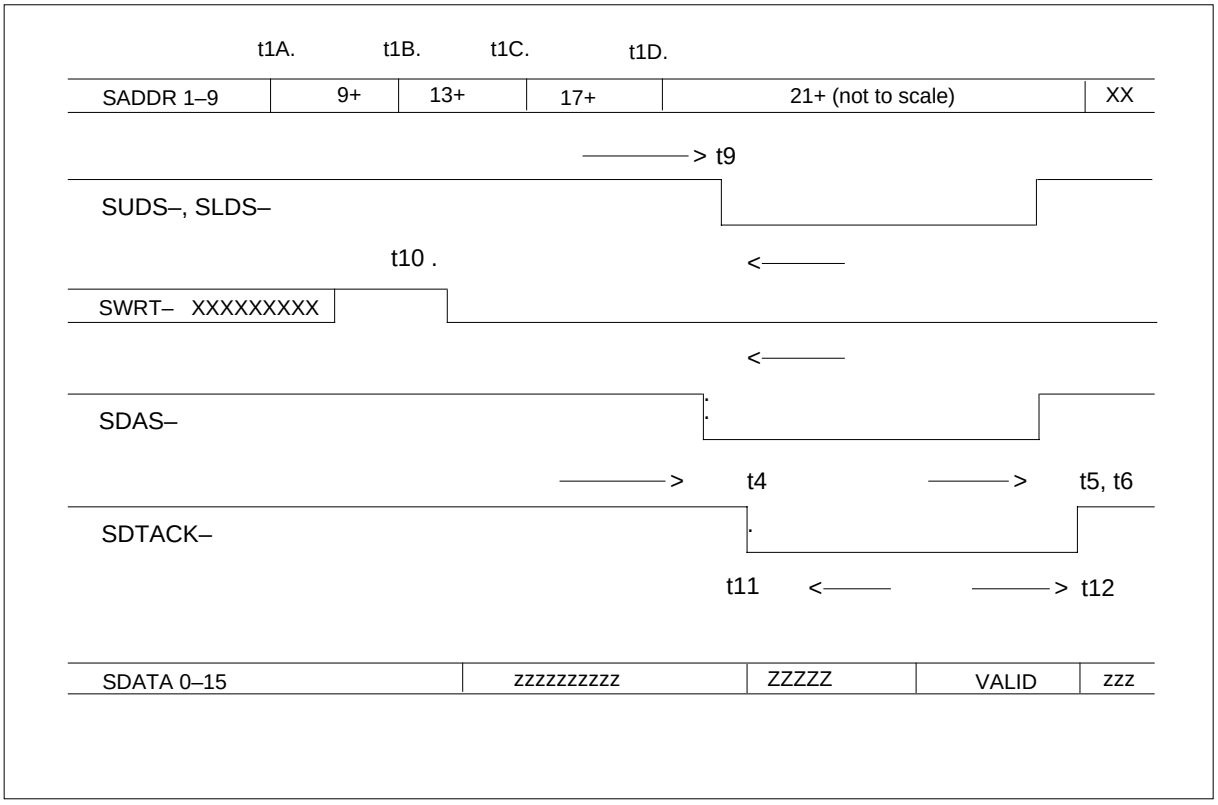
Read-cycle timing values (Sheet 2 of 2)

Item	Description	Min	Max
t1D	ADDR(18-21)+ valid to SDAS- low	27	
t2	SUDS-, SLDS- low to SDAS- low	-65	155
t3	SWRT- high to SDAS- low	21	
t4	SDAS- low to SDTACK- low	0	79µ
t5	SDTACK- hold time after SUDS- high	0	110
t6	SDTACK- hold time after SDAS- high	0	100
t7	SDATA(0-15) hold time after SUDS- high		
t8	SDTACK- low to SDATA(0-15)+ valid		83

Note: Minimum and maximum times are in nanoseconds unless otherwise noted.

The SP basic write-cycle timing diagram for the card appears in the following table.

NT6X62AA timing SP basic write cycle (asynchronous)



The write-cycle timing values for the card appear in the following table.

Write cycle timing values (Sheet 1 of 2)

Item	Description	Min	Max
t1A	ADDR(1-9)+ valid to SDAS- low	112	
t1B	ADDR(10-13)+ valid to SDAS- low	47	
t1C	ADDR(14-17)+ valid to SDAS- low	37	
t1D	ADDR(18-21)+ valid to SDAS- low	27	
t4	SDAS- low to SDTACK- low	0	79µ
t5	SDTACK- hold time after SUDS- high	0	110
t6	SDTACK- hold time after SDAS- high	0	100
Note: Minimum and maximum times are in nanoseconds unless otherwise noted.			

NT6X62AA (end)

Write cycle timing values (Sheet 2 of 2)

Item	Description	Min	Max
t9	SDAS- low to SUDS-, SLDS- low	-20	195
t10	SWRT- low to SDAS- low	21	
t11	SDATA(0-15)+ valid to SDAS- low	12	
t12	SDAS- high to SDATA(0-15)+ invalid	10	
Note: Minimum and maximum times are in nanoseconds unless otherwise noted.			

Power requirements

The NT6X62AA requires +5V, +12V, and -12 V dc of power.

NT6X62AB

Product description

The NT6X62AB specialized tone receiver (STR) is a digital signal processing tone receiver. Applications, in which long circuit-holding times make the use of standard tone receivers impractical, use the NT6X62AB. Long holding times of 30 s or more occur in applications like call reorigination and blue box fraud detection.

The NT6X62AB is equipped in the extended multiprocesssor system (XMS)-based peripheral module (XPM) to monitor 480 active speech channels. The NT6X62AB has enough capacity to make sure that the XPM is the limiting operational factor.

The NT6X62AB scans every trunk that connects to the XPM for call reorigination attempts or indication of blue box use. For call reoriginations, the subscriber can dial a new sequence of digits to direct the call to another destination or feature. For false dialing attempts, the NT6X62AB detects the wrong tones that the subscriber introduced. The NT6X62AB forwards the information to the signal processor (SP) for disposition.

Call reorigination

Dual-tone multifrequency (DTMF) signaling makes the Call Reorigination feature possible. This feature allows legal interruption of a network call and provision of a second dial tone. The subscriber can dial another sequence of digits to access a new feature or termination. These steps do not terminate the original call. The subscriber does not need to access the system again or introduce a new authorization code.

The NT6X62AB monitors calls after dialing for a star (*) or an octothorpe (#). These digits signal a reorigination request. The maintains contact with the connection, decodes the * or # signal, and forwards the signal to the SP circuit for processing.

Blue box fraud

Blue box fraud occurs when long distance calls are placed to escape detection for billing. The NT6X62AB uses single-frequency (SF) and multifrequency (MF) signal detection. Every trunk circuit in the system shares NT6X62AB. The NT6X62AB monitors the trunk connections continuously to detect the use of a false SF signal to perform the following:

- disconnect a call after cut-through
- redirect the call from an intermediate point in the network

The local processor forwards samples of false signals to the SP where analysis and processing occurs. When the system verifies a blue box fraud, the system

NT6X62AB (continued)

generates a call disposition. The system generates a call disposition to apply an announcement, inject howler tone, or disconnect the call without noise.

Functional description

The NT6X62AB performs the following functions:

- monitors trunk connections for * and # signals that indicate a reorigination attempt
- detects SF and MF signals that are not authorized that can indicate a blue box fraud attempt
- forwards indication of blue box fraud attempts to the SP for analysis and disposition
- provides multiple options to dispose of calls trapped in the process of illegitimately manipulating a call

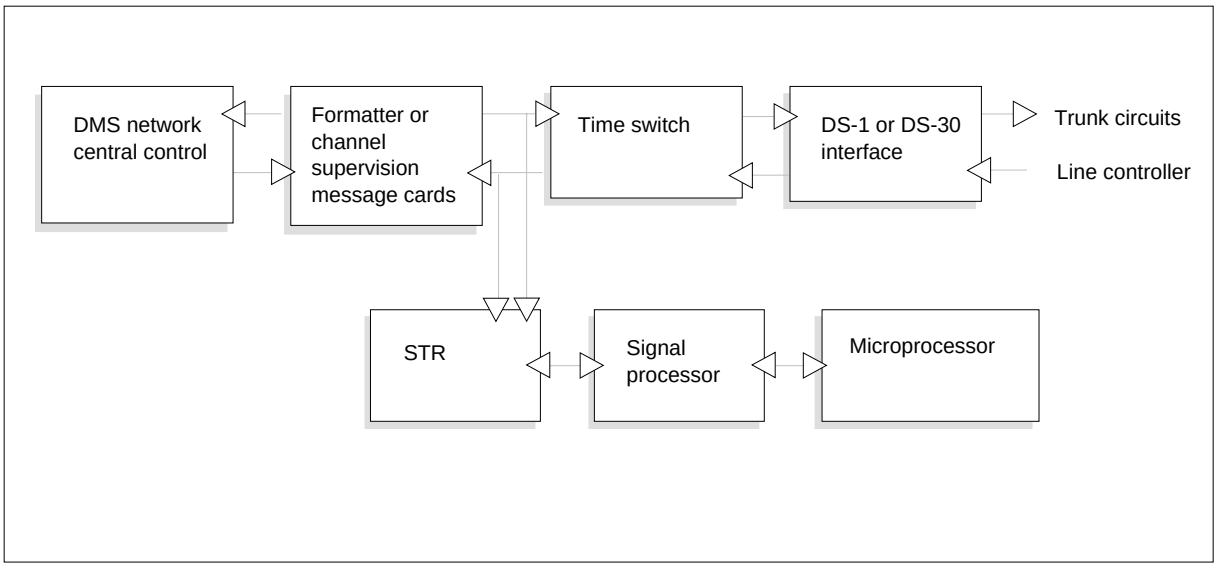
The NT6X62AB contains a digital signal processor and a local processor. The NT6X62AB detects tones on any of the 480 channels of the parallel speech bus in the XPM. The digital signal processor operates as a pipelined bit-slice arithmetic logic unit (ALU), sequencer, and address generator combined with a PROM multiplier. The local processor is a 10 MHz 68000-type processor that uses a shared memory to interface with the XPM signaling processor.

The NT6X62AB continuously monitors audio samples from the incoming parallel speech bus. The system sends suspicious samples to the XPM SP for evaluation. The system collects samples on a time-divided basis. Because one NT6X62AB can serve a maximum of 480 channels at one time, the NT6X62ABs are cost effective. The NT6X62ABs monitor every speech path in the system for reorigination requests or attempts at blue box fraud.

The NT6X62AB uses a 68000-type microprocessor with 128 kbytes of RAM and 128 kbytes of PROM. Communication between the cards and the SP occurs through a 16 bit wide area of common memory. The NT6X62AB local processor uses control signals, a shared memory, and a first-in-first-out (FIFO) interface to communicate with the digital signal processor. The digital signal interface is on a daughter board.

The NT6X62AB interface in the DMS switch appears in the following figure.

NT6X62AB functional blocks



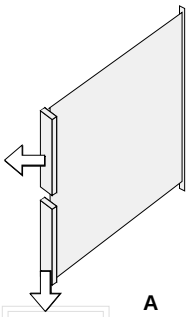
Signaling

Pin numbers

The NT6X62AB pin numbers from connector P1 on the main printed circuit board appear in the following figure. The pin numbers reflect external connections to the equipment shelf. The other card connectors, P2 to P5, interface between the main printed circuit board and the daughter board.

NT6X62AB (continued)

NT6X62AB pin numbers



	A	B
1A 1B	GND	GND
2A 2B	+5V	+5V
3A 3B	+5V	+5V
4A 4B	GND	GND
5A 5B	GND	GND
6A 6B		
7A 7B	GND	GND
8A 8B		
9A 9B		
10A 10B		
11A 11B	GND	GND
12A 12B		
13A 13B		
14A 14B	SPDTACK	
15A 15B		
16A 16B		
17A 17B		
18A 18B		
19A 19B		
20A 20B		
21A 21B		
22A 22B		
23A 23B		
24A 24B		
25A 25B		
26A 26B		
27A 27B		
28A 28B		
29A 29B	A1	
30A 30B		
31A 31B	A3	
32A 32B		
33A 33B	A5	
34A 34B		GND
35A 35B		
36A 36B	A7	
37A 37B		
38A 38B	A9	
39A 39B		
40A 40B	A11	

	A	B
41A 41B		
42A 42B		
43A 43B	A13	
44A 44B		
45A 45B	A15	
46A 46B		
47A 47B	A17	
48A 48B		ADM17
49A 49B	A19	ADM18
50A 50B		ADM19
51A 51B	A21	
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B		
58A 58B	D0	
59A 59B		
60A 60B	D2	
61A 61B		
62A 62B	D4	
63A 63B		
64A 64B	GND	GND
65A 65B	D6	
66A 66B		
67A 67B	D8	
68A 68B		RXD
69A 69B	D10	
70A 70B		
71A 71B	D12	
72A 72B		
73A 73B	D14	
74A 74B		
75A 75B		
76A 76B	GND	GND
77A 77B	+12V	+12V
78A 78B	GND	GND
79A 79B	–12V	– 12V
80A 80B	GND	GND

Technical data

Physical description

A single-slot dual-board XPM printed wiring board houses the NT6X62AB. The NT6X62AB consists of a standard 229 mm (9 in.) by 317 mm (12.5 in.) DMS-100 card with a 216 mm (8.5 in.) by 317 mm (12.5 in.) daughter board assembly for the digital signal processor and input buffer. Maximum weight of the NT6X62AB assembly is 1.702 kg (60 oz).

Power requirements

Maximum power consumption for the NT6X62AB is 16W. The NT6X62AB uses +5V, +12V, and -12V of dc power. The maximum current drain appears in the following table.

Maximum current drain

Supply	Current
+5V	3A
+12V	40mA
-12V	40mA

Technology

The technology for the NT6X62AB circuit is through-hole standard integrated circuits. These circuits use advanced high-speed complementary metal-oxide semiconductor (CMOS) logic, memories, processors, ALUs, and sequencers.

NT6X62DA

Product description

The NT6X62DA specialized tone receiver (STR) card is a development of the NT6X62AB STR, with firmware added. The firmware can detect CCITT Signaling System 5 (CCITT N5) line signaling tones. These tones occur on all 480 channels of a PCM-30 digital trunk controller (PDTC). International networks use the N5 tones (2400 Hz and 2600 Hz) for circuit supervisory functions.

To provide digital N5 signaling on DMS-300 equipment, the PDTC must include the NT6X62DA and the following three cards:

- the NT6X42CA (enhanced channel supervision message (CSM))
- the NT6X92CA (universal tone receiver (UTR) tone detection)
- the NT6X69LA (CPP message protocol and tones)

The call processing capacity of the PDTC host limits the capacity of the STR to process CCITT N5 line signaling.

The NT6X62DA is not backward compatible. The card does not support associated features for the signal processing tone receiver (STR), like Blue Box Fraud and Reorigination.

Use of the STR occurs in applications in which long circuit-holding times make the of use standard tone receivers impractical.

The extended microprocessor system (XMS)-based peripheral module (XPM) uses the NT6X62DA to monitor 480 active speech channels. The XPM can handle approximately six call attempts each second. The STR can monitor for N5 tones at the same time on approximately 300 channels of the speech bus.

The features of the NT6X62DA follow:

- detects CCITT N5 tones
- generates the split signal CHSPLIT and sends the split signal to the CSM card

Location

The NT6X62DA fits in slots 8, 9 or 11 of a PDTC.

Functional description

The main function of the NT6X62DA STR is detection of CCITT N5 line signaling tones. The STR detects in-band line signaling tones that occur during call set-up. The STR monitors the incoming speech bus only.

The tone detection application involves a constant monitor of in-service channels for the N5 tones. The NT6X62DA requires the ability to split the channel for each call. The split of a channel prevents the leak of tones to exchanges later in the link-by-link signaling path. The system uses a CHSPLIT signal that the STR supplies to complete a splitting function on the NT6X42CA CSM card.

The NT6X69LA card (CPP message protocol and tones) generates CCITT N5 line and register signaling tones.

Functional blocks

The NT6X62DA uses a 68000-type microprocessor equipped with 128 Kbytes of RAM and 128 Kbytes of PROM. Communication between the cards and the SP occurs through a 16-bit-wide area of common memory. The NT6X62DA local processor uses the following parts to communicate with the digital signal processor:

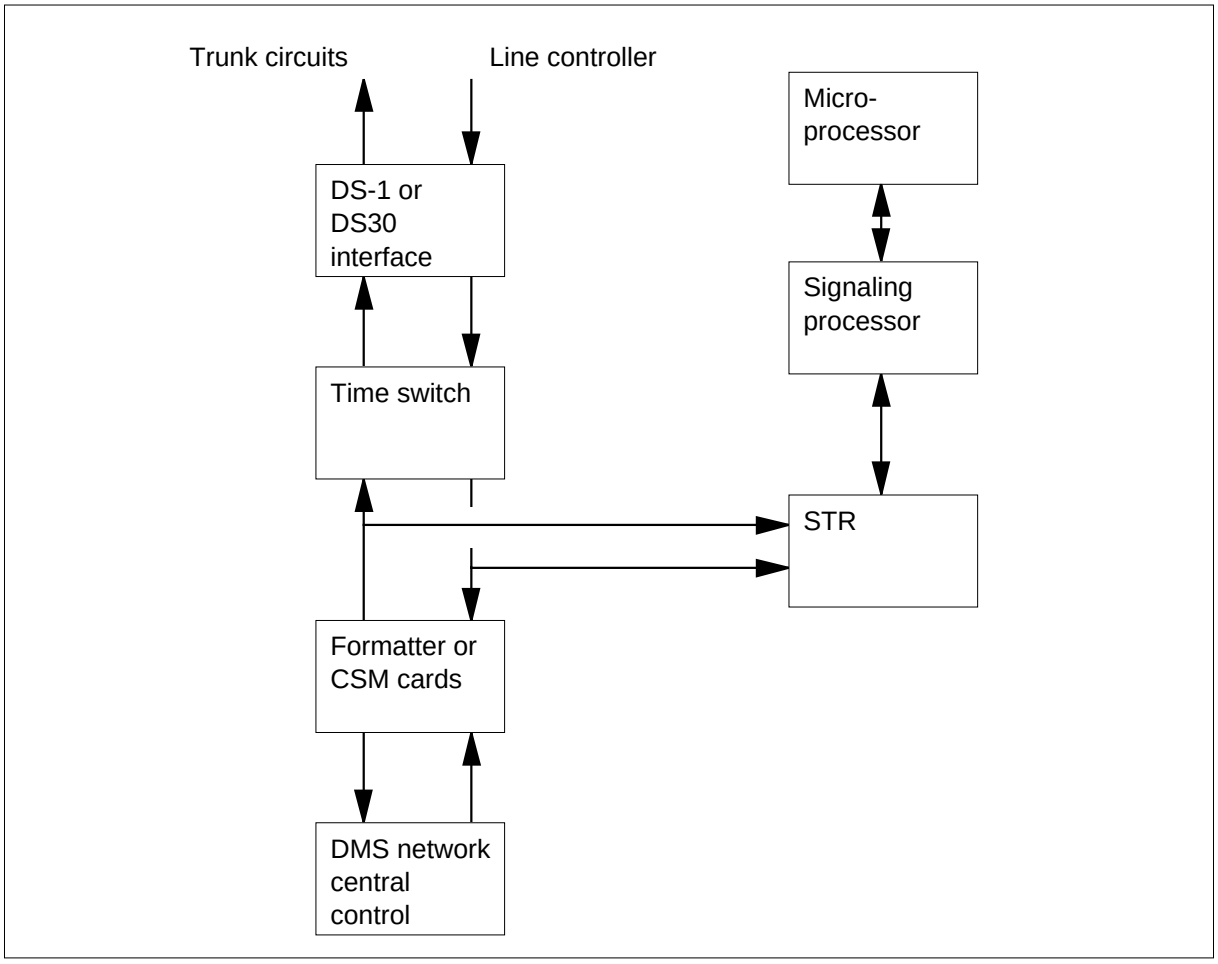
- control signals
- a shared memory
- first-in-first-out (FIFO) protocol

A secondary circuit board contains the digital signal interface.

The NT6X62AB in the XPM appears in the following figure.

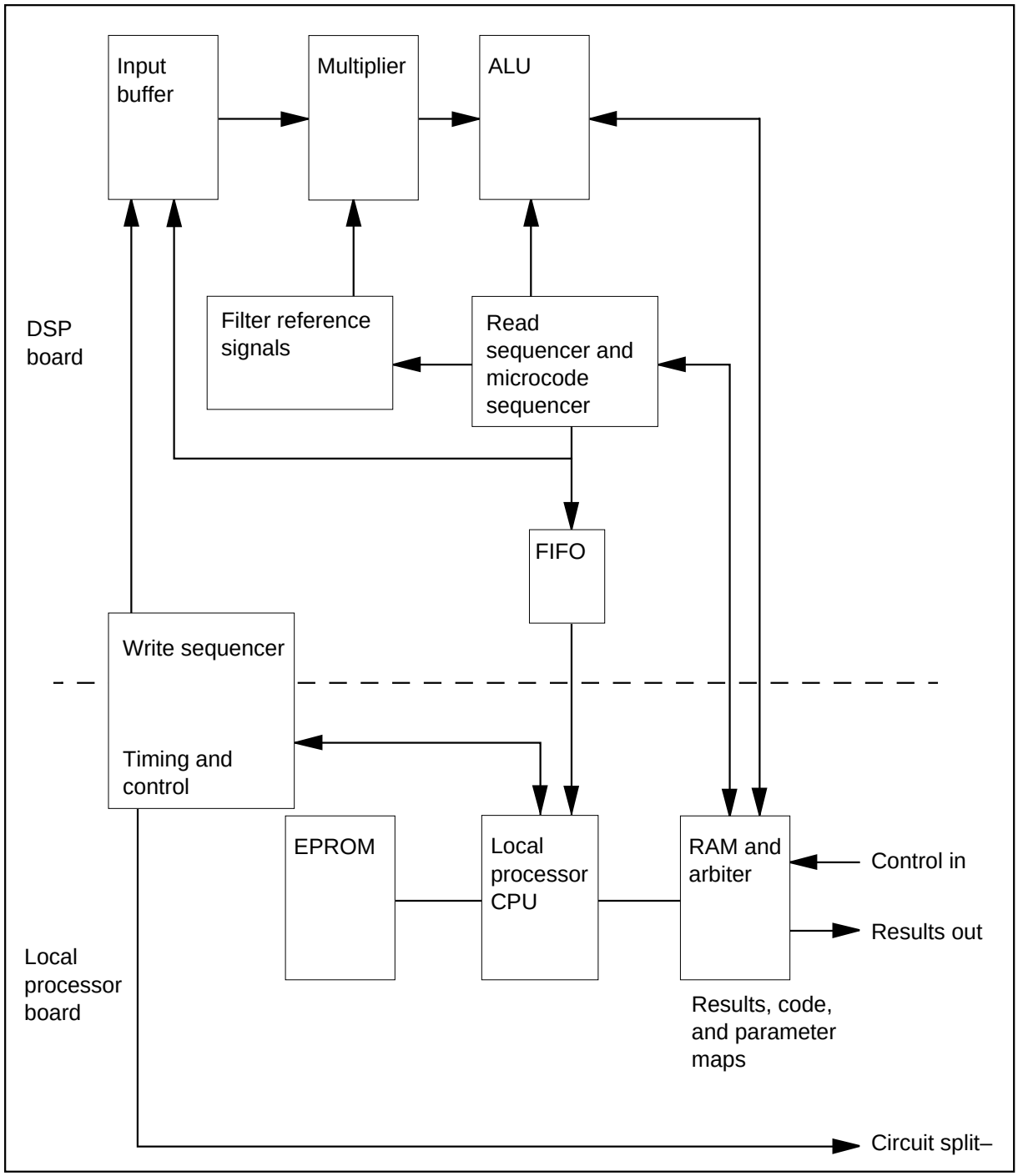
NT6X62DA (continued)

NT6X62DA XPM configuration



The relationship between the functional blocks appears in the following figure.

NT6X62DA functional blocks



NT6X62DA (continued)

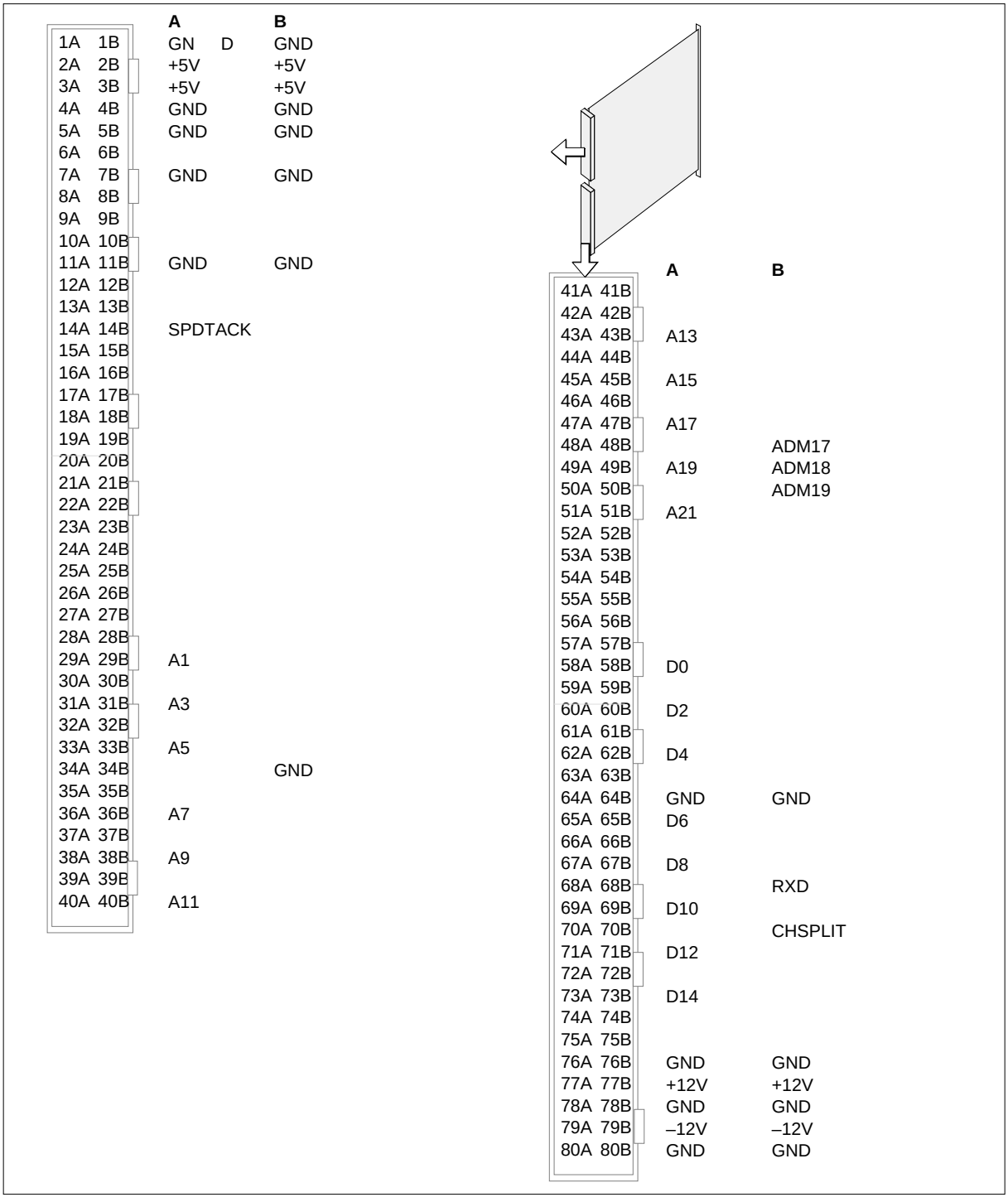
Signaling

Pin numbers

The NT6X62DA pin numbers from connector P1 on the main printed circuit board appear in the following figure. These pin numbers reflect external connections to the equipment shelf. Card connectors P2 to P5 connect the main printed circuit board to the secondary circuit board.

NT6X62DA (continued)

NT6X62DA pin numbers



NT6X62DA (continued)

Technical data

Description

A single-slot dual-board XPM printed wiring board contains the NT6X62DA. The NT6X62DA contains a standard DMS-100 card with a secondary circuit board for the digital signal processor and input buffer. The DMS-100 card measures 229 mm (9 in.) by 317 mm (12.5 in.). The secondary circuit board assembly measures 216 mm (8.5 in.) by 317 mm (12.5 in.). Maximum weight of the NT6X62DA assembly is 1702.5 g (60 oz).

Power requirements

Maximum power use for the NT6X62DA is 32 W. The NT6X62DA uses +5 V, +12 V, and -12 V of dc power. The maximum current use appears in the following table.

Maximum current use

Supply	Current
+5 V	4 to 6 A
+12 V	40 mA
-12 V	40 mA

Technology

The technology for the NT6X62DA circuit is through-hole standard integrated circuits that use the following items:

- advanced high-speed complementary metal-oxide semiconductor (CMOS) logic
- memories
- processors
- arithmetic and logic unit (ALUs)
- sequencers

Configuration

The STR configuration requires that both units of the PDTC include STRs. Both units of the PDTC must include CSM cards, like the NT6X42CA, that are able to complete the splitting function.

The backplanes of both units of the PDTC must be fitted with a backplane strap. This strap transmits the CHSPLIT signal from the STR to the CSM.

Traffic capacity

The STR can monitor all 496 active speech channels. The STR cannot monitor all the channels at the same time. The call and trunk mix determines the number of calls that the STR can handle at the same time. The STR does not reduce the call-processing ability of the PDTC.

NT6X62EA

Product description

The NT6X62EA specialized tone receiver (STR) card is a firmware that detects CCITT Signaling System 5 (CCITT N5) line signaling tones. These tones occur on all 480 channels of a PCM-30 digital trunk controller (PDTC). International networks use the N5 tones (2400 Hz and 2600 Hz) for circuit supervisory functions.

To provide digital N5 signaling on DMS-300 equipment, the PDTC must include the NT6X62EA and the following three cards:

- the NT6X42CA (enhanced channel supervision message (CSM))
- the NT6X92CA (universal tone receiver (UTR) tone detection)
- the NT6X69LA (CPP message protocol and tones)

The call processing capacity of the PDTC host limits the capacity of the STR to process CCITT N5 line signaling.

The NT6X62EA is an optional digital processing tone receiver used in applications in which long circuit-holding times make the use of standard tone receivers impractical. Long holding times occur in such applications as call reorgination and other midcall features involving DTMF reception during the talking state of a call.

The NT6X62EA is not backwards compatible with existing STRs such as the NT6X62AB or NT6X62DA and is not a plug in replacement. The new pack is backwards compatible with all XPM software and hardware. The NT6X62EA is an STR family circuit pack with LSSGR compliant DTMF reception and no Blue Box Fraud (BBF) detection.

The extended microprocessor system (XMS)-based peripheral module (XPM) uses the NT6X62EA to monitor 480 active speech channels. The XPM can handle approximately six call attempts each second. The STR can monitor for N5 tones at the same time on approximately 300 channels of the speech bus.

The features of the NT6X62EA follow:

- detects CCITT N5 tones
- generates the split signal CHSPLIT and sends the split signal to the CSM card
- provides call reorigination tone detection capability

The NT6X62EA differs from previous STR releases in that it complies with LSSGR requirements for DTMF reception TR-NWT-000506, Section 6 Issue

3, 1991 (tone detection algorithm). Specifically, it detects DTMF digits as short as 40 milliseconds in duration with a 40 millisecond silence following. It also meets other LSSGR requirements.

The NT6X62EA is a single printed circuit pack (PCP) and a general purpose digital signal processor (DSP). The NT6X62EA is not backwards compatible with existing STRs such as the NT6X62AB or the NT6X62DA. It is not a plug-in replacement. The NT6X62EA is backwards compatible with all XPM software and hardware. There is no Blue Box Fraud (BBF) detection.

Location

The NT6X62EA requires a single XPM slot, containing two full-sized PCPs with a ribbon cable connecting them.

Functional description

The main function of the NT6X62EA STR is detection of CCITT N5 line signaling tones. The STR detects in-band line signaling tones that occur during call set-up. The STR monitors the incoming speech bus only.

The tone detection application involves a constant monitor of in-service channels for the N5 tones. The NT6X62EA requires the ability to split the channel for each call. The NT6X62EA split of a channel prevents the leak of tones to exchanges later in the link-by-link signaling path. The system uses a CHSPLIT signal that the STR supplies to complete a splitting function on the NT6X42CA CSM card.

The NT6X69LA card (CPP message protocol and tones) generates CCITT N5 line and register signaling tones.

Functional blocks

The NT6X62EA uses a 68000-type microprocessor equipped with 128 Kbytes of RAM and 128 Kbytes of PROM. Communication between the cards and the SP occurs through a 16-bit-wide area of common memory. The NT6X62EA local processor uses the following parts to communicate with the digital signal processor:

- control signals
- a shared memory
- first-in-first-out (FIFO) protocol
- XPM speech bus interface

NT6X62EA (continued)

XPM speech bus interface

The XPM speech bus runs along the backplane. It is available for all the speech bus option cards. Since the STR is considered an XPM option card, it has access to the PCM data on the speech bus. The STR only monitors or operates on PCM voice channels. In the XPM this means the STR considers ports 0-15 active.

The STR only has read access to the XPM speech bus. It can only access PCM data on the incoming path. For example, data coming into the XPM from the P-side interface which is typically routed to the C-side of the XPM toward the DMS-100 network.

PAC (PCM/A-Bus controller

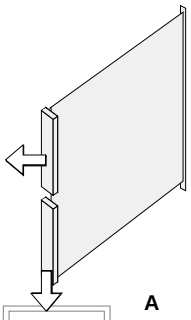
The PAC block provides the interface and control between the local STR resources and the XPM speech bus (PCM) and the XPM A bus.

Signaling

Pin numbers

The NT6X62EA pin numbers from connector P1 on the main printed circuit board appear in the following figure. These pin numbers reflect external connections to the equipment shelf. Card connectors P2 to P5 connect the main printed circuit board to the secondary circuit board.

NT6X62EA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	+5V	+5V
3A 3B	+5V	+5V
4A 4B	+5V	+5V
5A 5B	GND	GND
6A 6B	FP–	C97
7A 7B	GND	GND
8A 8B		
9A 9B		
10A 10B		
11A 11B	GND	GND
12A 12B	SDAS–	
13A 13B	SLDS–	
14A 14B	SDTACK–	
15A 15B	SUDS–	
16A 16B	SRWT–	
17A 17B		
18A 18B	SRSTOUT–	
19A 19B		
20A 20B		
21A 21B	PIN0	
22A 22B	PIN1	
23A 23B	PIN2	
24A 24B	PIN3	
25A 25B	PIN4	
26A 26B	PIN5	
27A 27B	PIN6	
28A 28B	PIN7	
29A 29B	SADDR01	
30A 30B	SADDR02	
31A 31B	SADDR03	
32A 32B	SADDR04	
33A 33B	SADDR05	
34A 34B	GND	GND
35A 35B	SADDR06	
36A 36B	SADDR07	
37A 37B	SADDR08	
38A 38B	SADDR09	
39A 39B	SADDR10	
40A 40B	SADDR11	RTIME

	A	B
41A 41B		
42A 42B	SADDR12	
43A 43B	SADDR13	
44A 44B	SADDR14	
45A 45B	SADDR15	
46A 46B	SADDR16	
47A 47B	SADDR17	
48A 48B	SADDR18	ADM17
49A 49B	SADDR19	ADM18
50A 50B	SADDR20	ADM19
51A 51B	SADDR21	
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B		
58A 58B	SDATA00	
59A 59B	SDATA01	
60A 60B	SDATA02	
61A 61B	SDATA03	
62A 62B	SDATA04	GND
63A 63B	SDATA05	
64A 64B	GND	GND
65A 65B	SDATA06	
66A 66B	SDATA07	
67A 67B	SDATA08	
68A 68B	SDATA09	RXD
69A 69B	SDATA10	
70A 70B	SDATA11	CHSPLIT–
71A 71B	SDATA12	
72A 72B	SDATA13	
73A 73B	SDATA14	
74A 74B	SDATA15	
75A 75B		TXD
76A 76B	GND	GND
77A 77B	+12V	+12V
78A 78B	GND	GND
79A 79B	–12V	–12V
80A 80B	GND	GND

NT6X62EA (continued)

Technical data

Description

A single-slot dual-board XPM printed wiring board contains the NT6X62EA. The NT6X62EA contains a standard DMS-100 card with a secondary circuit board for the digital signal processor and input buffer. The DMS-100 card measures 229 mm (9 in.) by 317 mm (12.5 in.). The secondary circuit board assembly measures 216 mm (8.5 in.) by 317 mm (12.5 in.). Maximum weight of the NT6X62EA assembly is 1702.5 g (60 oz).

Power requirements

The XPM supplies the +5V rail to the STR card. The maximum wattage dissipated by the is 7.10W @ +5V. The 2.5V rail, which the +5V power supply generates, dissipates 5W. The 3.3V rail, which the +5V power supply generates, dissipates 1.32W.

Absolute maximum power requirements

Parameters	Min	Nom	Max	Units	Comments
Supply Voltage 5V			7	Volts	From XPM backplane
Supply Current 5V			5	Amps	Based on rating of fuse on +5V rail into board
Supply Voltage 2.5V	-0.3		3	Volts	Range tolerable by DSP (generated from on-board switchers)
Supply Current 2.5V			3	Amps	Based on rating of fuse on +2.5V rail from switchers
Supply Voltage 3.3V	-0.3		4	Volts	From on-board switchers
Supply Current 3.3V			2	Amps	Based on rating of fuse on +3.3V rail from switchers

Operating power specifications (Sheet 1 of 2)

Parameters	Min	Nom	Max	Units	Comments
Supply Voltage 5V	4.5*	5.0	5.5	Volts	*Reset supervisor resets at minimum voltage
Supply Current 5V			1.42	Amps	Based on testing of 1W prototypes running at minimum and full capacity
Supply Voltage 2.5V	2.38	*2.50	2.62	Volts	

Operating power specifications (Sheet 2 of 2)

Parameters	Min	Nom	Max	Units	Comments
Supply Current 2.5V			2.0	Amps	Based on rating of fuse on +2.5V rail from switchers
Supply Voltage 3.3V	3.14*	3.3	3.46	Volts	
Supply Current 3.3V			0.4	Amps	Based on rating of fuse on +3.3V rail from switchers

Technology

The technology for the NT6X6EA circuit is through-hole standard integrated circuits that use the following items:

- advanced high-speed complementary metal-oxide semiconductor (CMOS) logic
- memories
- processors
- arithmetic and logic unit (ALUs)
- sequencers

Configuration

The STR configuration requires that both units of the PDTC include STRs. Both units of the PDTC must include CSM cards, like the NT6X42CA, that are able to complete the splitting function.

The backplanes of both units of the PDTC must be fitted with a backplane strap. This strap transmits the CHSPLIT signal from the STR to the CSM.

Traffic capacity

The STR can monitor all 496 active speech channels. The STR cannot monitor all the channels at the same time. The call and trunk mix determines the number of calls that the STR can handle at the same time. The STR does not reduce the call-processing ability of the PDTC.

NT6X65AA

Product description

The NT6X65AA common channel interoffice signaling (CCIS) terminal card sends and receives signaling data. The NT6X65AA transmits signaling data between a Digital Multiplex System (DMS)-100 switch and the CCIS and CCITT6 transmission links.

Location

A standard card can hold the NT6X65AA.

Functional description

The NT6X65AA sends and receives high-level data link functions and communications to and from the message switch and buffer 6 (MSB6) and the modem. The card checks the serial bit stream data for correct format and detects errors.

Functional blocks

The NT6X65AA includes the following functional blocks:

- the dynamic random access memory (RAM) (D-RAM)
- the parity checking/generation circuit
- the D-RAM access and timing circuit
- the arbiter
- the refresh circuit
- the control bit interface
- the two processor circuits
- the two erasable programmable read-only memory (EPROM) circuits
- the wait state generator
- the watchdog timer
- the input/output (I/O) control status circuit
- the test card interface
- the port circuit
- the static RAM (S-RAM)
- the S-RAM timer
- the data link interface (DLI) register
- the universal synchronous-asynchronous receiver-transmitter (USART) circuit

- the Electronic Industries Association (EIA) driver
- the EIA receiver

The D-RAM

The dynamic-RAM (D-RAM) contains the memory that allows the circuit to assemble signaling messages. The circuit assembles the messages in sequence. A 16-bit memory address accesses the memory.

Parity checking/generation circuit

The parity checking/generation circuit generates parity bits on all write operations to the D-RAM from the master processor (MP) system. This circuit checks the parity bits for errors in all read operations from the D-RAM. The circuit sends an error message to the MSB6 when the circuit detects a parity error.

The D-RAM access and timing circuit

The D-RAM access and timing circuit controls MSB6 and MP access to the memory.

Arbiter

The arbiter uses an internal MP processor clock to sort requests for memory access from the following:

- the MP bus system
- the refresh circuit
- the MSB6

The arbiter gives highest priority to MSB6 requests and lowest priority to MP system bus requests.

Refresh circuit

The refresh circuit makes sure that memory requests are completed correctly. The circuit is separate from the D-RAM to prevent corruption during an interrupt.

Control bit interface

The control bit interface receives a card access request from the MSB6 and sends the request to the arbiter for scheduling.

Processor circuits

The processor circuits in the MP system control the scheduling of data between the MSB6 and the modems. The processor in the data link processor (DLP) system provides processing functions to check the data.

NT6X65AA (continued)

The EPROM circuits

The EPROM circuits contain the operating instructions for the processors in the MP and DLP systems. The EPROM in the MP system provides the procedures for the following operations:

- self-testing
- the D-RAM data loading
- signaling data collection

Wait state generator

The wait state generator provides a timed wait in every processor machine cycle. This timed wait allows the processing of access requests.

Watchdog timer

The watchdog timer generates a trap interrupt to the call processing software. The card cannot continue in a loop when this trap interrupt occurs.

The I/O control status circuit

The input/output (I/O) control status circuit receives signals from the port circuits in the DLP system. The I/O control status circuit indicates when incoming or outgoing signals are present.

Test card interface

The test card interface provides an interface to test the NT6X65AA.

Port circuit

The port circuit sends interrupt communication between the DLP system and the MP system.

The S-RAM

The static-RAM (S-RAM) provides memory to store signaling messages to and from the transmission link.

The S-RAM timer

The S-RAM timer generates timing signals for the processor in the DLP system.

The DLI register

The data link interface (DLI) register controls the transmission link modem and sends status signals to the MP system.

The USART circuit

The USART circuit converts data to the transmission link modem from parallel to serial format. The USART converts data from the modem from serial to parallel format.

The EIA driver

The Electronic Industries Association (EIA) driver includes the following functions:

- reception of data from the USART circuit
- conversions of voltage levels
- transmission of the data to the modem

The data corresponds to EIA standards.

The EIA receiver

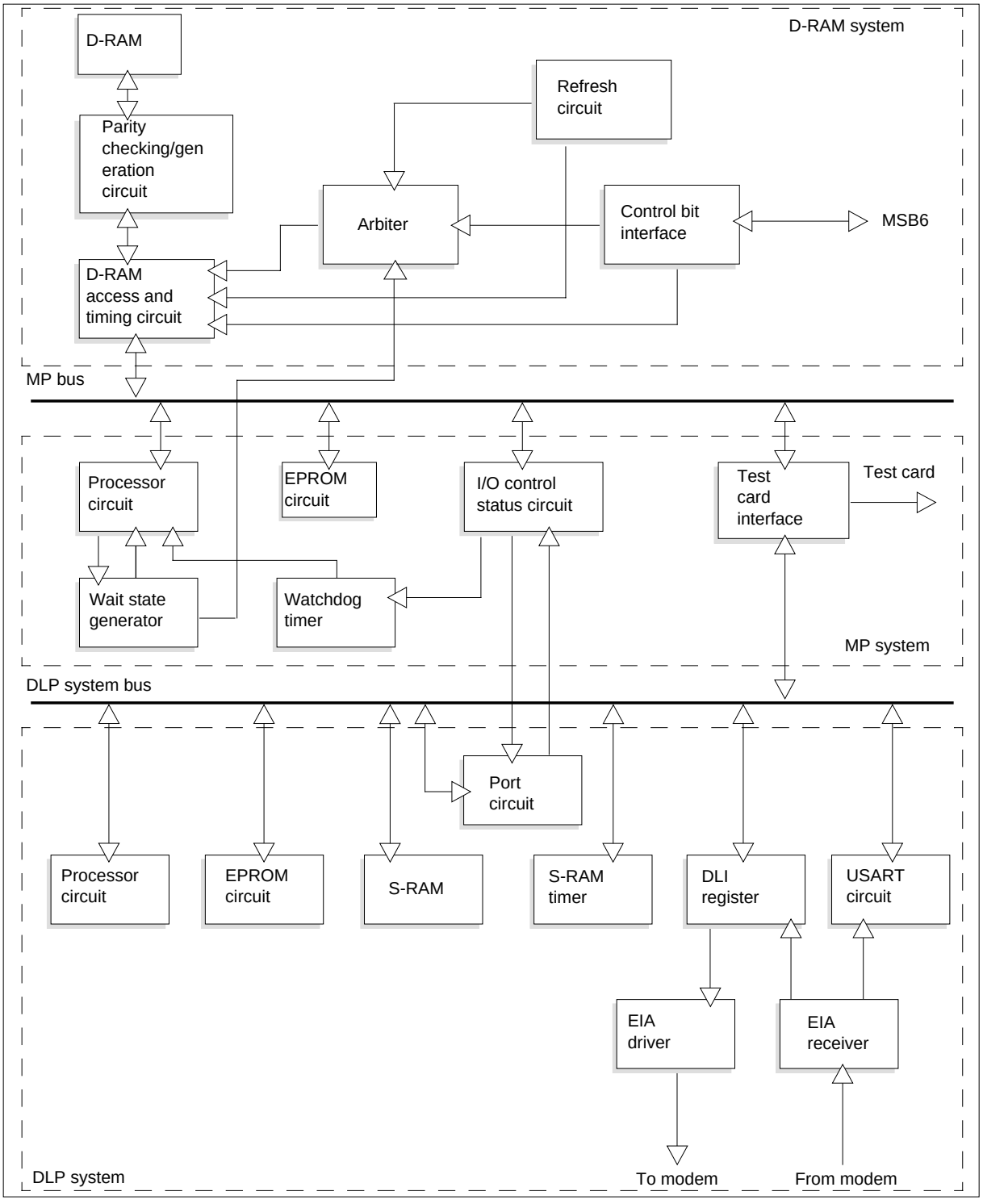
The EIA receiver includes the following functions:

- reception of data from the modem
- conversion of voltage levels
- transmission of data to the USART circuit and the DLI register for transmission to the card

The relationship between the functional blocks appears in the following diagram.

NT6X65AA (continued)

The NT6X65AA functional blocks



Technical data

The data transmission rate for the is 2400 bps.

Dimensions

The dimensions of the NT6X65AA follow:

- height: 318 mm (12.5 in.)
- width: 254 mm (10.0 in.)

Power requirements

The card requires 13W of power.

NT6X66AA

Product description

The NT6X66AA common channel signaling no. 7 (CCS7) terminal card sends and receives signaling data over CCS7 transmission links. The NT6X66AA implements the CCS7 link protocol and monitors signaling link performance.

Location

The NT6X66AA is on a standard card.

Functional description

The NT6X66AA provides an interface to the message switch and buffer 7 (MSB7). The NT6X66AA formats the messages transmitted to the card. The card checks the serial bit stream data for the correct format and detects errors.

Functional blocks

The NT6X66AA consists of the following functional blocks:

- message switch and buffer (MSB) interface control
- interface random access memory (RAM)
- two processor circuits
- static RAM (S-RAM)
- wait state control circuit
- two erasable programmable read-only memory (EPROM) circuits
- control/status circuit
- watchdog and program timer
- terminal and IBM interface circuit
- master processor (MP)/data link processor (DLP) interface RAM
- the MP/DLP interface control
- data link interface
- multiprotocol serial controller (MPSC)

The MSB interface control

The MSB interface control regulates the transmission link data between the MSB7 and the card. The circuit contains an arbiter to schedule memory requests from the MP and the MSB7.

Interface RAM

The interface RAM stores the requests for S-RAM memory access.

Processor circuits

The processor circuit in the S-RAM system assembles the signaling messages in read operations from and write operations to the S-RAM. The processor circuit in the DLP system assembles the messages in sequence to check errors and manipulate checksums.

The S-RAM

The static-RAM (S-RAM) contains the memory for the card to assemble signaling messages. You can use a 16-bit memory address to access the S-RAM.

Wait state control circuit

The wait state control circuit generates a timed wait in every processor machine cycle. This timed wait allows the processing of access requests.

The EPROM circuits

The EPROM in the S-RAM system contains procedures to self-test and to load the processor program. The EPROM in the DLP system provides the memory for the processor program.

Control/status circuit

The control/status circuit sends control and status signals to the processor in the S-RAM system.

Watchdog and program timer

The watchdog and program timer supplies the timing intervals for the processor and provides the watchdog process. The watchdog process generates a trap interrupt to the call processing software. The card cannot continue in a loop when this trap interrupt occurs.

Terminal and IBM interface circuit

The terminal and IBM interface circuit provides an interface to test and develop the card.

The MP/DLP interface RAM

The MP/DLP interface RAM provides memory to control the signaling messages.

The MP/DLP interface control

The MP/DLP interface control generates timing signals to schedule signaling messages.

NT6X66AA (continued)

Data link interface

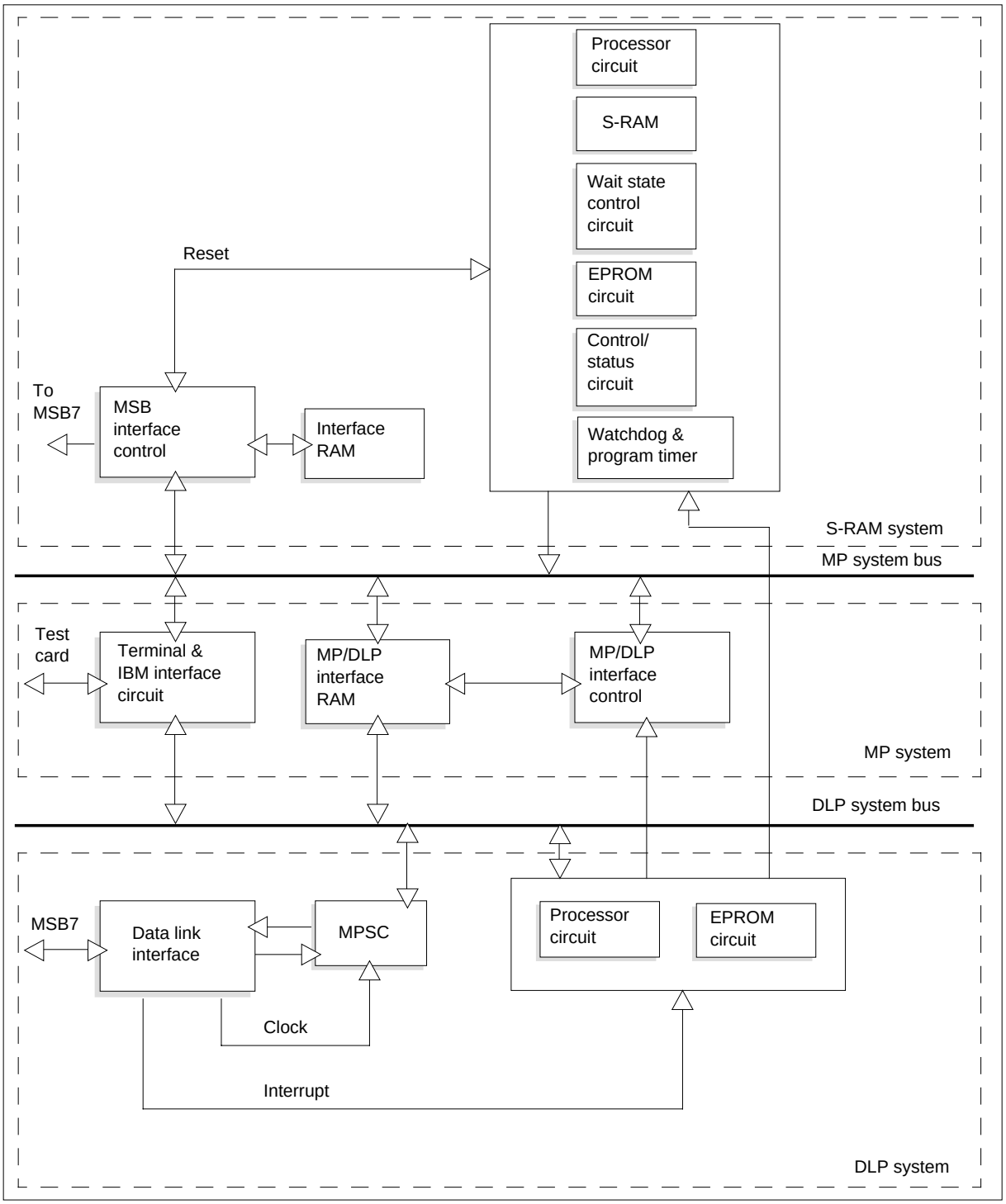
The data link interface (DLI) provides an interface between the MSB7 data bus and the MPSC.

The MPSC

The multiprotocol serial controller (MPSC) detects errors on the signaling messages and manipulates the checksum digits on the messages. The MPSC functions as an interface between the data link interface and the DLP bus.

The relationship between the functional blocks appears in the following diagram.

The NT6X66AA functional blocks



NT6X66AA (end)

Technical data

The data transmission rate for the NT6X66AA is 56 kbps.

Dimensions

The dimensions of the NT6X66AA are as follows:

- height: 318 mm (12.5 in.)
- width: 254 mm (10.0 in.)

Power requirements

The card requires 13W of power.

NT6X66AB

Product description

The NT6X66AB common channel signaling no. 7 (CCS7) terminal card sends and receives signaling data over CCS7 transmission links. The NT6X66AB implements the CCS7 link protocol and monitors signaling link performance.

Location

The NT6X66AB is on a standard card.

Functional description

The NT6X66AB provides an interface to the message switch and buffer 7 (MSB7). The NT6X66AB formats messages transmitted to the card. The card checks the serial bit stream data for the correct format and detects errors.

Functional blocks

The NT6X66AB has the following functional blocks:

- message switch and buffer (MSB) interface control
- interface random access memory (RAM)
- two processor circuits
- static-RAM (S-RAM)
- wait state control circuit
- two erasable programmable read-only memory (EPROM) circuits
- control/status circuit
- watchdog and program timer
- terminal and IBM interface circuit
- master processor (MP)/data link processor (DLP) interface RAM
- the MP/DLP interface control
- data link interface (DLI)
- multiprotocol serial controller (MPSC)

Message switch and buffer interface control

The MSB interface control regulates the transmission link data between the MSB7 and the card. The circuit contains an arbiter to schedule memory requests from the MP and the MSB7.

Interface RAM

The interface RAM stores the requests for S-RAM memory access.

NT6X66AB (continued)

Processor circuits

The processor circuit in the S-RAM system assembles the signaling messages in read operations from and write operations to the S-RAM. The processor in the DLP system assembles messages in sequence to check errors and manipulate checksums.

The S-RAM

The static-RAM (S-RAM) contains the memory for the card to assemble signaling messages. A 16-bit memory address can access the S-RAM.

Wait state control circuit

The wait state control circuit generates a timed wait in every processor machine cycle. This timed wait allows the processing of access requests.

The EPROM circuits

The EPROM in the S-RAM system contains procedures to self-test and to load the processor program. The EPROM in the DLP system provides the memory for the processor program.

Control/status circuit

The control/status circuit sends control and status signals to the processor in the S-RAM system.

Watchdog and program timer

The watchdog and program timer supplies the timing intervals for the processor and provides the watchdog process. The watchdog process generates a trap interrupt to the call processing software. The card cannot continue in a loop when a trap interrupt occurs.

Terminal and IBM interface circuit

The terminal and IBM interface circuit provides an interface to test and develop the card.

The MP/DLP interface RAM

The MP/DLP interface RAM provides memory to control the signaling messages.

The MP/DLP interface control

The MP/DLP interface control generates timing signals to schedule signaling messages.

Data link interface

The data link interface provides an interface between the MSB7 data bus and the MPSC.

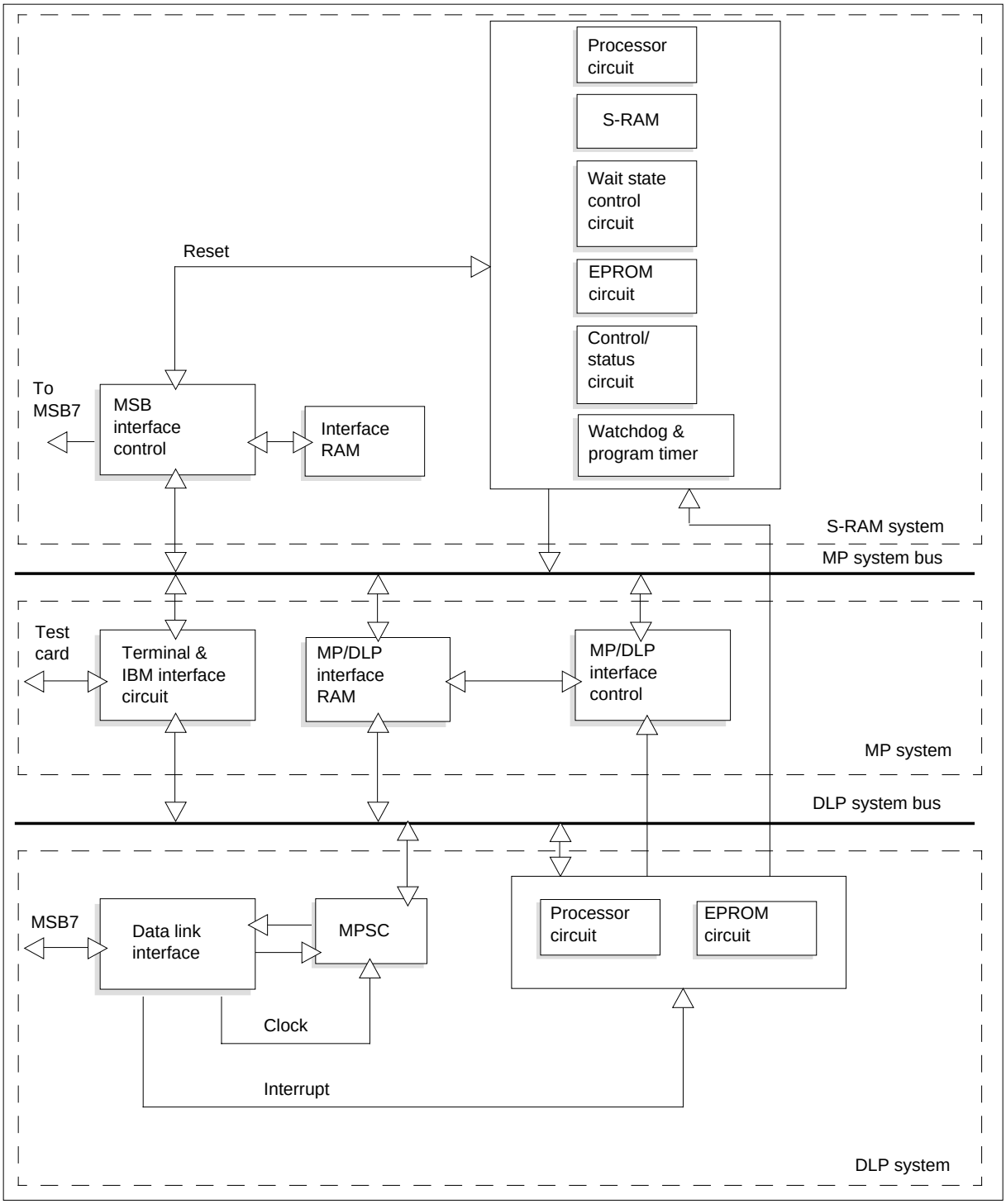
The MPSC

The multiprotocol serial controller (MPSC) detects errors on the signaling messages and manipulates the checksum digits on the messages. The MPSC functions as an interface between the data link interface and the DLP bus.

The relationship between the functional blocks appears in the following figure.

NT6X66AB (continued)

The NT6X66AB functional blocks



Technical data

The data transmission rate for the NT6X66AB is 56 kbps.

Dimensions

The dimensions of the NT6X66AB are as follows:

- height: 318 mm (12.5 in.)
- width: 254 mm (10.0 in.)

Power requirements

The card requires 13W of power.

NT6X66AC

Product description

The NT6X66AC common channel signaling 7 (CCS7) signaling terminal (ST) transmits and receives signaling data over the CCS7 transmission links. The NT6X66AC implements the CCS7 level-2 link protocol and monitors signaling link performance.

Functional description

A single card can hold the NT6X66AC. The NT6X66AC has the following features:

- error check of transmission link data
- automatic circuit check
- dual processor design

Functional blocks

The NT6X66AC has the following functional blocks:

- wait state control
- static random access memory (RAM) (S-RAM)
- erasable programmable read-only memory (EPROM)
- control and status
- watchdog and program timer
- message switching buffer (MSB) interface control
- the MSB interface RAM
- terminal and IBM interface
- master processor to data link processor (MP-DLP) interface RAM
- the MP-DLP interface control
- data link interface
- multiprotocol service controller (MPSC)

Wait state control

The wait state control provides a timed wait that every processor machine cycle requires. The timed wait allows the processing of access requests.

Static RAM

The S-RAM contains the memory for the NT6X66AC and the interface to the MSB. Parity checking and an arbiter support the memory. The arbiter schedules the memory requests.

The EPROM

The MP of each EPROM contains the procedures to self-test and to load the processor program.

Control and status

The control and status sends control and status signals to the processor.

Watchdog timer and program timer

The watchdog timer and program timer provide the timing intervals for the processor and the watchdog process.

Message switching buffer interface control

The MSB interface control directs transmission link data between the MSB7 and the NT6X66AC. This card also contains the arbiter to schedule memory requests.

Message switching buffer interface RAM

The MSB interface RAM is the storage area for requests for memory access.

Terminal and IBM interface

The terminal and IBM interface test and develop the signaling terminal.

Master processor to data link processor interface RAM

The MP-DLP interface RAM provides memory to control the signaling messages.

Master processor to data link processor interface control

The MP-DLP interface control provides the timing signals to schedule signaling messages.

Data link interface

The data link interface is the link between the data bus of the MSB and the MPSC.

Multiprotocol service controller

The MPSC is a full duplex interface between the data link interface and the DLP bus. The MPSC detects errors on the signaling messages and manipulates the cyclic redundancy check digits on the messages.

The relationship between the functional blocks appears in the following figure.

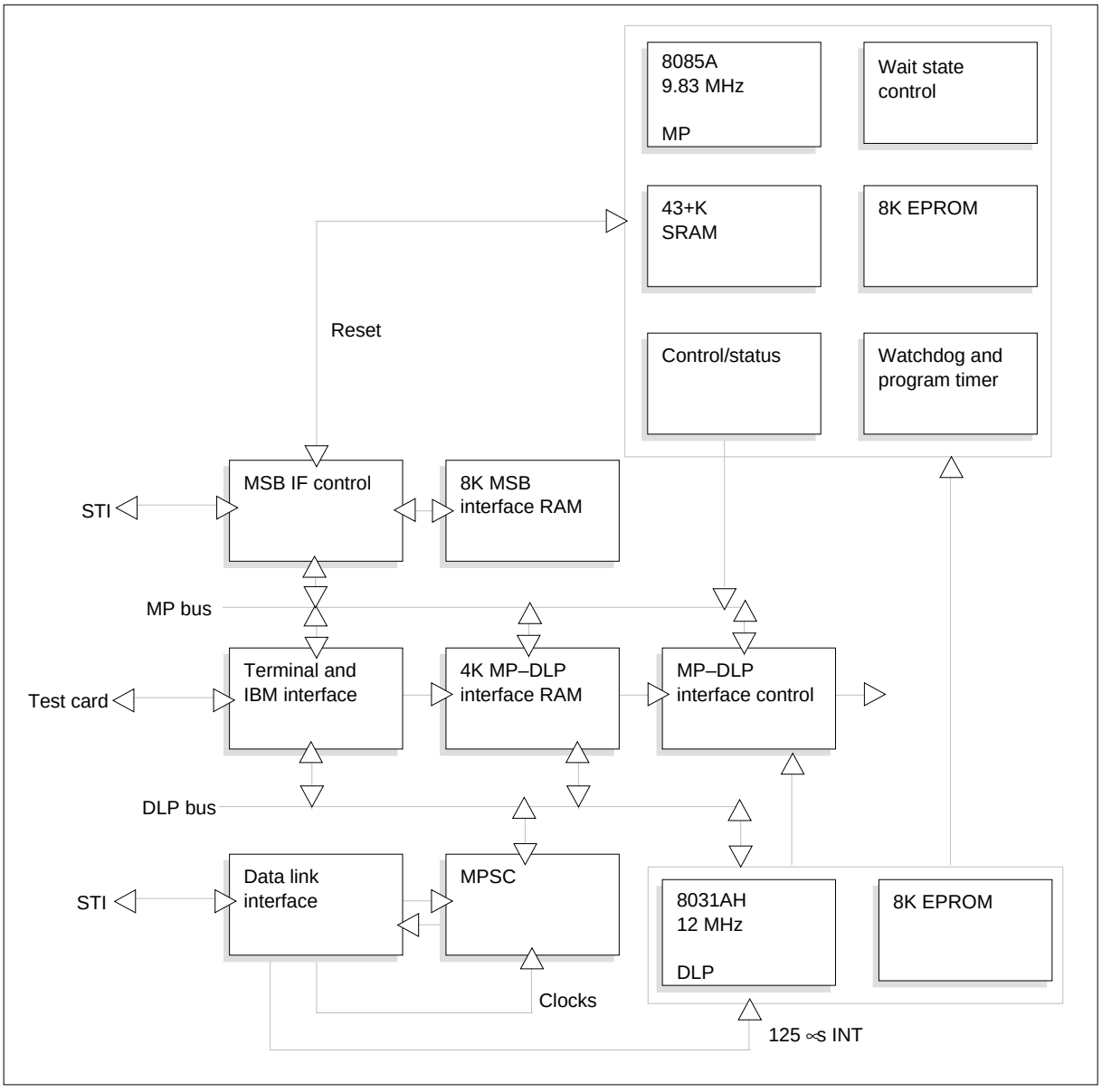
NT6X66AC (end)

Technical data

Power requirements

The NT6X66AC requires 13W.

The NT6X66AC functional blocks



NT6X69AA

Product description

The NT6X69AA common peripheral processor (CPP) message protocol circuit (MPC) interprets and transfers signaling and control messages. The network and the NT6X69AA following peripheral modules (PM) exchange the messages:

- message switch and buffer (MSB)
- line group controller (LGC)
- line trunk controller (LTC)
- digital trunk controller (DTC)
- international DTC (IDTC)
- line concentrating module (LCM)
- remote LCM (RLCM)
- remote cluster controller (RCC)

The card must operate with the NT6X79AA CPCE tone generator circuit (TGC) to generate tones.

Location

The card occupies specified slots in the PMs.

Functional description

The NT6X69AA card receives and transfers messages between the associated PM and the network. The card converts parallel data received from the network to serial data for transmission to the PM. The card converts serial data to parallel data for transmission to the network. The PM sends the serial data.

Functional blocks

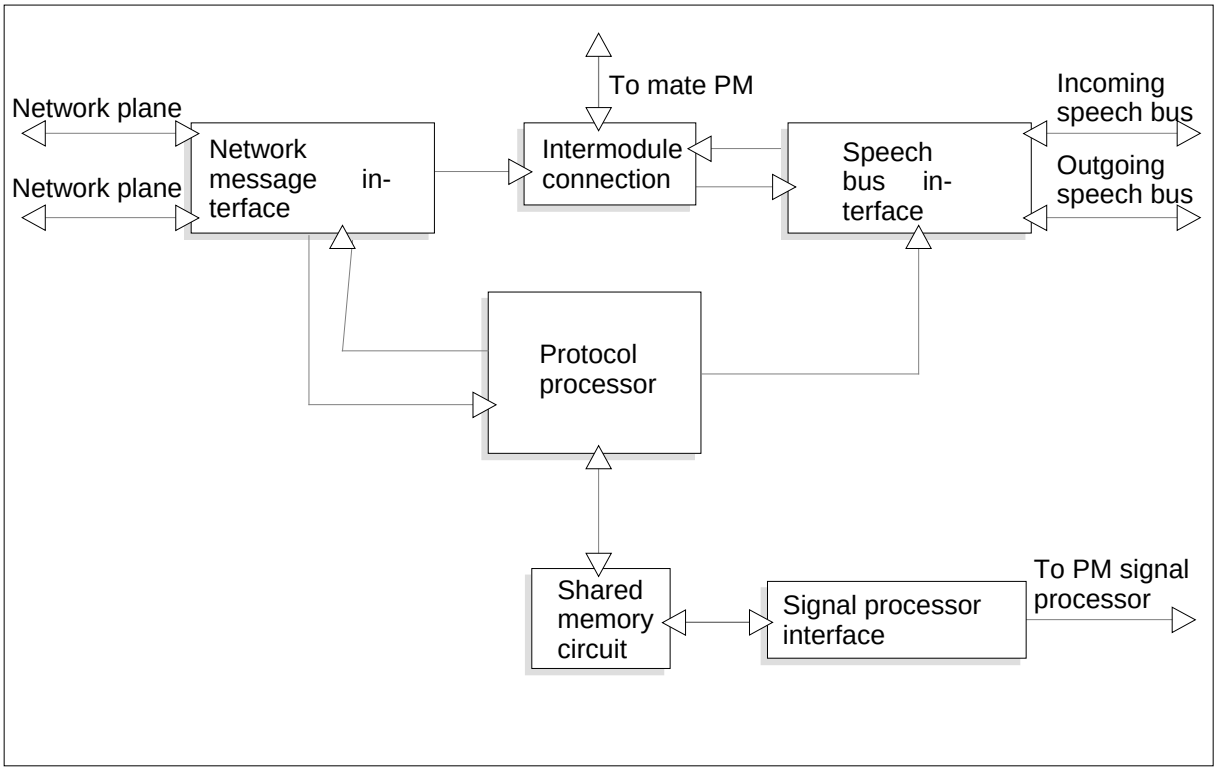
The NT6X69AA card contains the following functional blocks:

- the network message interface
- the intermodule connection
- the speech bus interface
- the protocol processor (PP)
- the shared memory circuit

the signal processor (SP) interface

NT6X69AA (continued)

NT6X69AA functional blocks



Network message interface

The network message interface uses holding registers to transmit and receive parallel data. The network message interface uses shift registers to convert the parallel data to serial data. The circuit contains the following components for each network plane that enters the circuit:

- transmit holding register
- transmit shift register
- receive holding register
- receive shift register

Intermodule connection

The intermodule connection provides a 64-kbps link to the mate unit. The circuit appears to the PP as a speech bus time slot. The SP assigns the speech bus time slot through the speech bus interface.

Speech bus interface

The speech bus interface contains transmit and receive RAM circuits. These circuits allow the protocol processor to communicate with the incoming and outgoing speech buses.

Protocol processor

The protocol processor receives messages from the associated PM or network and interprets the protocol. The PP works with the following functional blocks to transmit and receive messages:

- shared memory circuit
- network message interface
- speech bus interface

Shared memory circuit

The 8-bit, 8-Kbyte shared memory circuit provides work space for the PP. The shared memory circuit provides a buffer for messages between the PP and the SP in the associated PM. The circuit also provides an origination point code (OPC) area for the SP. The SP uses the OPC to generate messages to the network message or the speech bus interfaces.

Signal processor interface

The signal processor interface allows communication between the SP and the MPC.

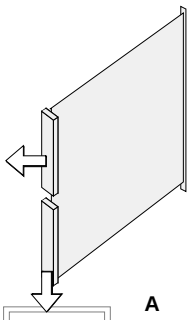
Signaling

Pin numbers

The pin number diagram for the NT6X69AA card appears in the following figure.

NT6X69AA (continued)

NT6X69AA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	5V	5V
3A 3B	5V	5V
4A 4B	5V	5V
5A 5B	GND	GND
6A 6B	FP–	C97T
7A 7B	GND	GND
8A 8B	–ACT	
9A 9B	C195TB	
10A 10B	CPROS–	
11A 11B	GND	GND
12A 12B	DAS–	
13A 13B	LDS–	C97–B
14A 14B	DTACK–	CPROCB
15A 15B	UDS–	RUN
16A 16B	WRT–	TCEN–
17A 17B	IMCOUT	IMCIN
18A 18B	GNDI	NT4REQ
19A 19B		
20A 20B		
21A 21B	PIN0	POUT0
22A 22B	PIN1	POUT1
23A 23B	PIN2	POUT2
24A 24B	PIN3	POUT3
25A 25B	PIN4	POUT4
26A 26B	PIN5	POUT5
27A 27B	PIN6	POUT6
28A 28B	PIN7	POUT7
29A 29B	ADDR01+	
30A 30B	ADDR02+	
31A 31B	ADDR03+	
32A 32B	ADDR04+	
33A 33B	ADDR05+	
34A 34B	GND	GND
35A 35B	ADDR06+	–FPM
36A 36B	ADDR07+	GND
37A 37B	ADDR08+	C97M+
38A 38B	ADDR09+	GND
39A 39B	ADDR10+	CH0T
40A 40B	ADDR11+	CH0M

	A	B
41A 41B	GND	GND
42A 42B	ADDR12+	
43A 43B	ADDR13+	D0
44A 44B	ADDR14+	D1
45A 45B	ADDR15+	D2
46A 46B	ADDR16+	D3
47A 47B	ADDR17+	D4
48A 48B	ADDR18+	D5
49A 49B	ADDR19+	D6
50A 50B	ADDR20+	D7
51A 51B	ADDR21+	
52A 52B	SEN0	DESTXT0–
53A 53B	SEN1	DESTXT1–
54A 54B	SEN2	
55A 55B	PSPEN+	SRCXT0–
56A 56B	CSPEN+	SRCXT1–
57A 57B	GND	GND
58A 58B	DATA00+	SRC0
59A 59B	DATA01+	SRC1
60A 60B	DATA02+	SRC2
61A 61B	DATA03+	SRC3
62A 62B	DATA04+	SRC4
63A 63B	DATA05+	SRC5
64A 64B	GND	SRC6
65A 65B	DATA06+	SRC7
66A 66B	DATA07+	
67A 67B	CH0S0	
68A 68B	CH0R0	
69A 69B	CH0S1	
70A 70B	CH0R1	
71A 71B	T1	
72A 72B	T2	
73A 73B	T3	
74A 74B	AUXRST–	
75A 75B	MODRST–	
76A 76B	GND	GND
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

Technical data

The card exchanges messages at a rate of 300 each second.

Physical dimensions

The physical dimensions of the NT6X69AA card are as follows:

- height: 317.5 mm (12.5 in.)
- width: 254.0 mm (10.0 in.)

Power requirements

The power use of the card is 18.75 W. The converter voltage is +5 V ± 0.25 V.

NT6X69AB

Product description

The NT6X69AB common peripheral processor (CPP) message protocol and tone circuit (MPC) interprets and transfers signaling and control messages. The network and the following peripheral modules (PM) exchange the messages:

- message switch and buffer (MSB)
- line group controller (LGC)
- line trunk controller (LTC)
- digital trunk controller (DTC)
- international DTC (IDTC)
- line concentrating module (LCM)
- remote line controller (RLCM)
- remote cluster controller (RCC)

Location

The card occupies specified slots in the PMs.

Functional description

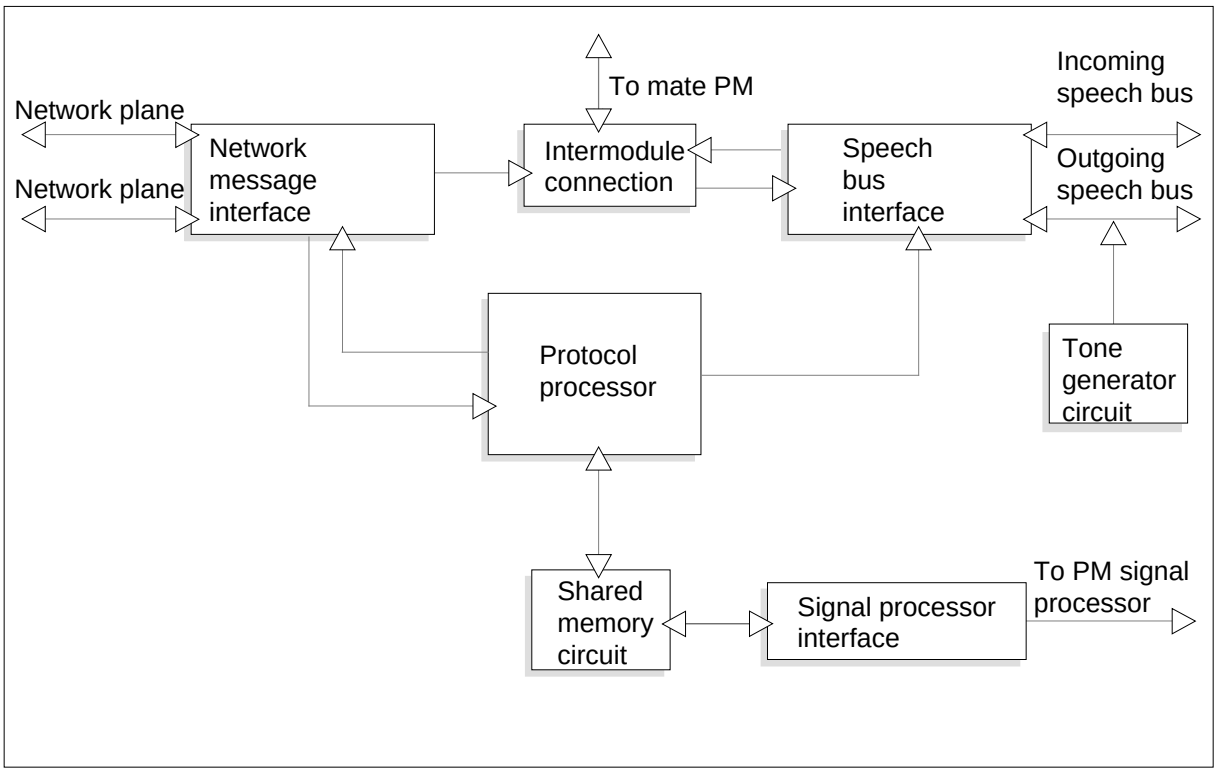
The NT6X69AB card receives and transfers messages between the associated PM and the network. The card converts parallel data from the network to serial data for transmission to the PM. The card converts serial data to parallel data for transmission to the network. The PM sends the serial data.

Functional blocks

The NT6X69AB card contains the following functional blocks:

- network message interface
- intermodule connection
- speech bus interface
- tone generator circuit
- protocol processor (PP)
- shared memory circuit
- signal processor (SP) interface

NT6X69AB functional blocks



Network message interface

The network message interface uses holding registers to transmit and receive parallel data. The network message interface uses shift registers to convert the parallel data to serial data. The circuit contains the following components for each network plane that enters the circuit:

- transmit holding register
- transmit shift register
- receive holding register
- receive shift register

Intermodule connection

The intermodule connection provides a 64-Kbps link to the mate unit. The circuit appears to the PP as a speech bus time slot. The SP assigns the speech bus time slot through the speech bus interface.

NT6X69AB (continued)

Speech bus interface

The speech bus interface contains transmit and receive RAM circuits. These circuits allow the protocol processor to communicate with the incoming and outgoing speech buses.

Tone generator circuit

The tone generator circuit uses the following components to generate and store tones:

- tone generating chip
- EPROM
- holding register

Protocol processor

The PP receives messages from the associated PM or network and interprets the protocol. The PP works with the shared memory circuit, the network message interface, and the speech bus interface to transmit and receive messages.

Shared memory circuit

The 8-bit, 8-kbyte shared memory circuit provides work space for the PP. The circuit provides a buffer for messages sent between the PP and the SP in the associated PM. The circuit also provides an origination point code (OPC) area. The SP uses the OPC to generate messages to the network message or the speech bus interfaces.

Signal processor interface

The signal processor interface allows communication between the SP and the MPC.

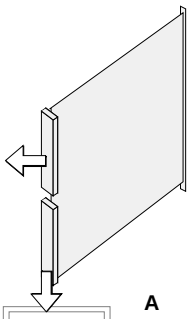
Signaling

Pin numbers

The pin numbers for the NT6X69AB card appear in the following figure.

NT6X69AB (continued)

NT6X69AB pin numbers



	A	B
1A 1B	GND	GND
2A 2B	5V	5V
3A 3B	5V	5V
4A 4B	5V	5V
5A 5B	GND	GND
6A 6B	FP–	C97T
7A 7B	GND	GND
8A 8B	–ACT	
9A 9B	C195TB	
10A 10B	CPROS–	
11A 11B	GND	GND
12A 12B	DAS–	
13A 13B	LDS–	C97–B
14A 14B	DTACK–	CPROCB
15A 15B	UDS–	RUN
16A 16B	WRT–	TCEN–
17A 17B	IMCOUT	IMCIN
18A 18B	GND	INT4REQ
19A 19B		
20A 20B		
21A 21B	PIN0	POUT0
22A 22B	PIN1	POUT1
23A 23B	PIN2	POUT2
24A 24B	PIN3	POUT3
25A 25B	PIN4	POUT4
26A 26B	PIN5	POUT5
27A 27B	PIN6	POUT6
28A 28B	PIN7	POUT7
29A 29B	ADDR01+	
30A 30B	ADDR02+	
31A 31B	ADDR03+	
32A 32B	ADDR04+	
33A 33B	ADDR05+	
34A 34B	GND	GND
35A 35B	ADDR06+	–FPM
36A 36B	ADDR07+	GND
37A 37B	ADDR08+	C97M+
38A 38B	ADDR09+	GND
39A 39B	ADDR10+	CH0T
40A 40B	ADDR11+	CH0M

	A	B
41A 41B	GND	GND
42A 42B	ADDR12+	
43A 43B	ADDR13+	D0
44A 44B	ADDR14+	D1
45A 45B	ADDR15+	D2
46A 46B	ADDR16+	D3
47A 47B	ADDR17+	D4
48A 48B	ADDR18+	D5
49A 49B	ADDR19+	D6
50A 50B	ADDR20+	D7
51A 51B	ADDR21+	
52A 52B	SEN0	DESTXT0–
53A 53B	SEN1	DESTXT1–
54A 54B	SEN2	
55A 55B	PSPEN+	SRCXT0–
56A 56B	CSPEN+	SRCXT1–
57A 57B	GND	GND
58A 58B	DATA00+	SRC0
59A 59B	DATA01+	SRC1
60A 60B	DATA02+	SRC2
61A 61B	DATA03+	SRC3
62A 62B	DATA04+	SRC4
63A 63B	DATA05+	SRC5
64A 64B	GND	SRC6
65A 65B	DATA06+	SRC7
66A 66B	DATA07+	
67A 67B	CH0S0	
68A 68B	CH0R0	
69A 69B	CH0S1	
70A 70B	CH0R1	
71A 71B	T1	
72A 72B	T2	
73A 73B	T3	
74A 74B	AUXRST–	
75A 75B	MODRST–	
76A 76B	GND	GND
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

NT6X69AB (end)

Technical data

The card exchanges messages at a rate of 300 each second.

Physical dimensions

The physical dimensions of the NT6X69AB card are as follows:

- height: 317.5 mm (12.5 in.)
- width: 254.0 mm (10.0 in.)

Power requirements

The power use of the card is 20 W. The converter voltage is +5 V $\pm$ 0.25 V.

NT6X69AC

Product description

The NT6X69AC card performs the same functions as the NT6X69AB and has the following additional capabilities:

- an application-specific integrated circuit (ASIC)
- compatibility with the fibre optics extended multiprocessor system (XMS)-based peripheral module (XPM)
- compatibility with the enhanced network (ENET)

The NT6X69AB replaces the NT6X43AA (message interface card) in the domestic market. The NT6X69 processor card contains the same capabilities of the NT6X43 and can process message protocols.

Functional description

Functional blocks

The NT6X69AC contains the following functional blocks:

- parallel speech bus (SB) message interface
- SB connection memory (CM)
- intermodule connection (IMC) interface
- interrupt generator
- tone generator
- protocol processor (PP)
- signaling processor (SP) and PP shared memory
- shelf reset generator
- cyclic redundancy check (CRC) ROM
- process timing ROM
- SP interface
- power-up circuitry

Parallel speech bus message interface

The parallel SB message interface in the NT6X69 differs from the equivalent in the NT6X43. In the NT6X43, the asynchronous SP sends messages to the synchronous SB. Synchronizing circuits are necessary. Synchronizing circuits include a frame level interrupt and a double buffer. In the NT6X69, the synchronous PP sends the message. The PP sends the message so that the PP can use a transmit (Tx) RAM and holding registers, and a receive (Rx) RAM and holding registers. The holding register pairs are the outgoing SB Tx/Rx

NT6X69AC (continued)

pair and the IMC Tx/Rx pair. The CM controls the gating of register output for each time slot. The first half of the instruction concerns the PP and the write to Tx RAM or the read from Rx RAM. In the second half, the system latches the data to the Tx holding register from the Tx RAM. The system latches the data according to the port/channel counter. Similarly, data writes to the Rx RAM from the Rx holding register.

Speech bus connection memory

The CM arbitrates the access of different service cards to the SB for each time slot. The SP accesses the CM in the same way that the SP and PP share memory. The PP does not have access to the CM. During the first half of the instruction cycle, the port/channel counter addresses the CM in a holding register. The system latches the data. The data in the holding register addresses the CM decoding PROM. This action enables the tone drivers, SB drivers and receivers, and an IMC register on the NT6X69. The system feeds two bits from the holding register to the formatter and the time switch through the backplane. Three other bits from the holding register are accessible through spare slots on the backplane.

Note: The T bits do not function in the same way as the bits of the NT6X43 card. The bits are not the same because the decoding circuitry includes additional functions, like IMC messaging and the tone checksum.

Intermodule connection interface

The IMC interface provides a 64-kbps link to the mate unit. The link appears to the PP as an SB time slot. The SP assigns the specified time slot through the CM.

The IMC circuitry is a shift register that the system loads with data from the IMC holding register. The IMC holding register is in the SB interface. The CM enables the system to load the IMC circuitry. An exchange of data occurs between the two shelves during the active channel 0 (CH0) time. The active clock gates the data. The IMC timeslot must be assigned away from the CH0 time to avoid data corruption. The IMC link does not use the SB. The IMC time slot on the SB remains available for pulse code modulation (PCM) or tones.

Errors can occur in the IMC link when the two shelves are not in synchronization for the following reasons:

- the CM circuitry on the inactive unit runs on the inactive clock. Slippage between the two units can cause the inactive IMC time slot to occur at the active CH0 time.
- the PP is frame synchronized to the PP shelf. The shelf can miss or double-read the register when slippage occurs between two units.

Interrupt generator

The interrupt generator works with the PP to signal the SP to relieve the SP from polling the message queue pointers. The PP accesses the INTSTB strobe to initiate a level 4 interrupt.

Tone generator

Tone generation circuitry on the NT6X69 card contains the following components:

- R09 generating chip
- tone PROM
- tone holding register

The T0, T1, and T2 bits from the connection memory are mapped to two tone control bits on the R09. The bits are mapped to the tone control bits to specify the type of the time slot. Eight-bit data from the R09 latches to the holding register. The CM circuitry controls gating of the contents of the holding register to the outgoing SB.

Protocol processor

A 32-bit instruction from microstore ROM latches to the micro-instruction register during each processor cycle. The micro-instruction register controls the following components:

- CPU
- CPU data multiplexer
- zero/not-zero conditional code
- skip instruction decoder
- destination/source (DEST/SRC) decoder
- sequencer
- sequencer data multiplexer

The CPU receives instructions from the instruction register (INST REG). The CPU produces an 8-bit result on the designation bus and a 1-bit zero conditional code. Direct data input from the multiplexer can be from the INST REG for immediate data, or from the SRC bus for external data. The instruction type determines the data source. The DEST/SRC decoders arbitrate the different external registers that place data on the SRC bus. The decoders provide strobes to other registers. This action allows a register to receive data from the DEST bus. The firmware uses two of the DEST strobes to aid testing. Bit 0 of the micro-instruction register determines if the user can toggle the conditional code that the CPU produces. The system feeds the conditional

NT6X69AC (continued)

code that results to the sequencer and the skip instruction decoder. Sequencer control ROM translates the 4 bits from the instruction register, the reset bit, and the skip bit. Sequencer control ROM translates these bits to formulate a 4-bit instruction that feeds to the sequencer. The skip instruction decoder examines bits 1 to 3 of the micro-instruction register and the conditional code. When the skip condition is correct, either of the following can occur to set the skip bit:

- the system suppresses the clock to the CPU during the next cycle time. An update of the CPU internal register does not occur because of this action.
- the equivalent of a continue instruction from the sequencer control ROM

The system accesses and executes the next instruction. The system does not store the result. A skip instruction cannot be skipped. The execution of the first skip instruction sets the skip bit and informs the internal CPU register not to store the result of the next instruction. The second skip instruction executes and sets the skip bit again. The instruction register or the DEST bus can provide sequencer data. The instruction bit that controls the multiplexer determines the data source. Output of the sequencer addresses microstore ROM that produces the next instruction bits that the micro-instruction register latches.

The PP accesses the following functional blocks:

- RAM shared with the SP
- CRC ROM for CRC calculation that DMS-X protocol requires
- the process timing ROM, that allows the firmware to synchronize to the frame
- the RSTGEN, that allows the PP to initiate a shelf reset from the NT6X46 card
- the interrupt generator, that allows the PP to initiate a level 4 interrupt to the SP
- the network module (NM) interface
- the SB interface
- the IMC interface

SP and PP shared memory

The SP and PP communicate through an 8KX8 block of RAM. The two processors share this block of RAM transparently. This block of shared memory provides the following:

- a work space for the PP
- a buffer for messages that the PP receives for the SP

- a buffer for messages that the SP places in a queue for the PP
- an opcode area

The SP cannot exercise the NM interface, the SB interface, and other interfaces any longer. The PP firmware provides a set of opcodes that allow the SP to exercise these interfaces indirectly.

The first half of the instruction cycle concerns the PP read and write access. The read and write access makes the access of this RAM transparent to the PP and the SP. The second half of the cycle concerns SP interface access. The two processors have read and write access over the address range of the memory. You must be careful when you perform a memory test on one processor. Make sure that the other processor does not write to the memory.

Shelf reset generator

To initiate a shelf reset, the PP performs the following sequence:

1. The PP clocks access the auxiliary reset to the reset flip-flop.
2. Output of the reset flip-flop goes to the backplane and connects to the NT6X46 card.
3. The NT6X46 card stops activity and issues the module reset signal to the the shelf that remains to acknowledge the reset.
4. The module reset that the NT6X46 card issues, clears the reset flip-flop on the NT6X69 card.

Cyclic redundancy check ROM

The cyclic redundancy check ROM contains two tables. Each table contains 256 bytes. A two-stage CRC accumulation process uses these tables.

Process timing ROM

Process timing ROM allows the PP to synchronize each process time slot for the frame boundary. The port/channel counter addresses PROM that the PP can read at an instruction cycle.

Signaling processor interface

The SP memory map is standard on most cards that provide interface to the SP. The address and control signals are buffered. An access sequence synchronizes SP requests and generates a read or write access cycle. An access sequence performs these actions when a correct address falls in the range assigned to this card type. The interface is asynchronous and an acknowledge signal indicates the end of the access cycle.

NT6X69AC (continued)

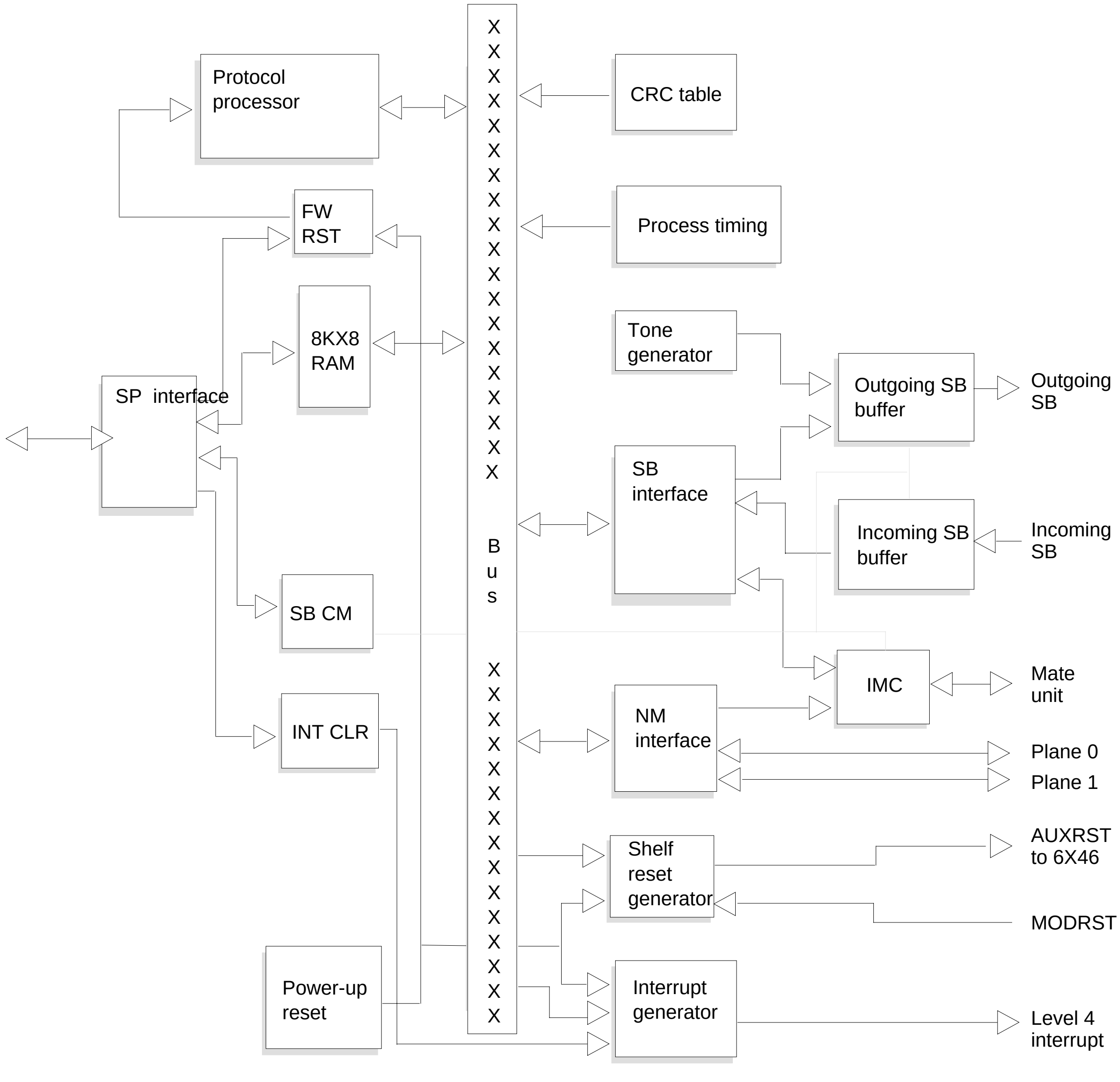
Power-up circuitry

A simple recording completing circuit resets the firmware and clears the INTGEN and auxiliary reset (AUXRST) flip-flops during a power-up.

The functional relationship between these blocks appears in the following figure.

NT6X69AC (continued)

NT6X69AC functional blocks



Note: CM enable signal

Signaling

Pin numbers

The pin numbers for the NT6X69AC appear in the following figure.

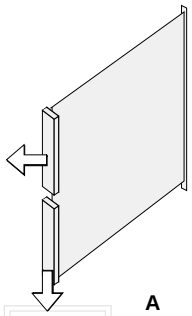
NT6X69AC (end)

NT6X69AC pin numbers

	A	B
1A 1B	GND	GND
2A 2B	5V	5V
3A 3B	5V	5V
4A 4B	5V	5V
5A 5B	GND	GND
6A 6B	FP–	C97T
7A 7B	GND	GND
8A 8B	–ACT	
9A 9B	C195TB*	
10A 10B	CPROCS–*	
11A 11B	GND	GND
12A 12B	DAS–	
13A 13B	LDS–	C97–B
14A 14B	DTRACK–	CPROCB
15A 15B	UDS–	RUN*
16A 16B	WRT–	TCEN–*
17A 17B	IMCOUT**	IMCIN**
18A 18B	GND	INT4REQ**
19A 19B		
20A 20B		
21A 21B	PIN0	POUT0
22A 22B	PIN1	POUT1
23A 23B	PIN2	POUT2
24A 24B	PIN3	POUT3
25A 25B	PIN4	POUT4
26A 26B	PIN5	POUT5
27A 27B	PIN6	POUT6
28A 28B	PIN7	POUT7
29A 29B	ADDR01+	
30A 30B	ADDR02+	
31A 31B	ADDR03+	
32A 32B	ADDR04+	
33A 33B	ADDR05+	
34A 34B	GND	GND
35A 35B	ADDR06+	–FPM
36A 36B	ADDR07+	GND
37A 37B	ADDR08+	C97M+
38A 38B	ADDR09+	GND
39A 39B	ADDR10+	CHOT
40A 40B	ADDR11+	CHOM

Notes:

1 * test channel signals, backplane connection not required
2 ** additional signals on the NT6902 card, but not on the NT6901



	A	B
41A 41B	GND	GND
42A 42B	ADDR12+	
43A 43B	ADDR13+	D0*
44A 44B	ADDR14+	D1*
45A 45B	ADDR15+	D2*
46A 46B	ADDR16+	D3*
47A 47B	ADDR17+	D4*
48A 48B	ADDR18+	D5*
49A 49B	ADDR19+	D6*
50A 50B	ADDR20+	D7*
51A 51B	ADDR21+	
52A 52B	SEN0	DESTXT0–
53A 53B	SEN1	DESTXT1–
54A 54B	SEN2	
55A 55B	PSPEN+	SRCXTO–
56A 56B	CSPEN+	SRCXT1–
57A 57B	GND	GND
58A 58B	DATA00+	SRC0*
59A 59B	DATA01+	SRC1*
60A 60B	DATA02+	SRC2*
61A 61B	DATA03+	SRC3*
62A 62B	DATA04+	SRC4*
63A 63B	DATA05+	SRC5*
64A 64B	GND	SRC6*
65A 65B	DATA06+	SRC7*
66A 66B	DATA07+	
67A 67B		CHOS0
68A 68B		CHOR0
69A 69B		CHOS1
70A 70B		CHOR1
71A 71B		
72A 72B		
73A 73B		
74A 74B		AUXRST–**
75A 75B		MODRST–**
76A 76B	GND	GND
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

NT6X69AD

Product description

The NT6X69AD performs the same functions as the NT6X69AB and has the following additional capabilities:

- an application-specific integrated circuit (ASIC)
- compatibility with the fibre optics extended multiprocessor system (XMS)-based peripheral module (XPM)
- compatibility with the enhanced network (ENET)

The NT6X69AB replaces the NT6X43AA (message interface card) in the domestic market. The NT6X69 processor board contains the same capabilities as the NT6X43 and can process message protocols.

Functional description

Functional blocks

The NT6X69AD contains the following functional blocks:

- parallel speech bus (SB) message interface
- SB connection memory (CM)
- intermodule connection (IMC) interface
- interrupt generator
- tone generator
- protocol processor (PP)
- signaling processor (SP) and PP shared memory
- shelf reset generator
- cyclic redundancy check (CRC) ROM
- process timing ROM
- SP interface
- power-up circuitry

Parallel speech bus message interface

The parallel SB message interface in the NT6X69 differs from the equivalent in the NT6X43. In the NT6X43, the asynchronous SP sends messages to the synchronous SB. Synchronizing circuits are necessary. Synchronizing circuits include a frame level interrupt and a double buffer. In the NT6X69, the synchronous PP sends the message. The PP sends a message so that the PP requires a transmit (Tx) RAM and holding registers. The PP also requires a receive (Rx) RAM and holding registers. The holding register pairs are the

NT6X69AD (continued)

outgoing SB Tx/Rx pair and the IMC Tx/Rx pair. The CM controls the gating of register output for each time slot. The first half of the instruction concerns PP and the write to Tx RAM or the read from Rx RAM. In the second half, the system latches data to the Tx holding register from the Tx RAM. The system latches according to the port/channel counter. Similarly, data writes to the Rx RAM from the Rx holding register.

Speech bus connection memory

The CM arbitrates the access of different service cards to the SB for each time slot. The SP accesses the CM in the same way that the SP and PP share memory. The PP does not have access to the CM. During the first half of the instruction cycle, the port/channel counter addresses the CM in a holding register. The system latches the data. The data in the holding register addresses the CM decoding PROM. This action enables the tone driver, the SB drivers and receivers, and an IMC register on the NT6X69. The system feeds two bits from the holding register to the formatter and the time switch through the backplane. Three other bits from the holding register are accessed through spare slots on the backplane.

Note: The T bits do not function in the same way as the bits of the NT6X43 card. The bits are not the same because the decoding circuitry includes additional functions, like IMC messaging and the tone checksum.

Intermodule connection interface

The IMC interface provides a 64-Kbps link to the mate unit. The link appears to the PP as an SB time slot. The SP assigns the specified time slot through the CM.

The IMC circuitry is a shift register that contains data from the IMC holding register in the SB interface. The shift register contains data when the CM enables the register. Data between the two shelves exchange during the active channel 0 (CH0) time. The active clock gates the data. The IMC time slot must be assigned away from the CH0 time to avoid data corruption. The IMC link does not use the SB. The IMC time slot on the SB remains available for pulse code modulation (PCM) or tones.

Errors can occur in the IMC link when the two shelves are not in synchronization for the following reasons:

- the CM circuitry on the inactive unit runs on the inactive clock. The slippage between the two units can cause the inactive IMC time slot to occur at the active CH0 time.
- the PP is frame synchronized to the PP shelf. The shelf can miss or double-read the register when slippage occurs between two units.

Interrupt generator

The interrupt generator works with the PP to signal to the SP to relieve the SP from polling the message queue pointers. The PP accesses the INTSTB strobe to initiate a level 4 interrupt.

Tone generator

Tone generation circuitry on the NT6X69 card contains the following:

- R09 generating chip
- tone PROM
- tone holding register

The T0, T1, and T2 bits from the connection memory are mapped to two tone control bits on the R09. The bits are mapped to specify the type of the time slot. Eight-bit data from the R09 latches to the holding register. The CM circuitry controls gating of the contents of the holding register to the outgoing SB.

Protocol processor

A 32-bit instruction from the microstore ROM latches into the micro-instruction register during each processor cycle. The micro-instruction register controls the following components:

- CPU
- CPU data multiplexer
- zero/not-zero conditional code
- skip instruction decoder
- destination/source (DEST/SRC) decoder
- sequencer
- sequencer data multiplexer

The CPU receives instructions from the instruction register (INST REG). The CPU produces an 8-bit result on the designation bus and a 1-bit zero conditional code. Direct data input from the multiplexer can be from the INST REG for immediate data, or the SRC bus for external data. The instruction type determines the data source. The DEST/SRC decoders arbitrate the various external registers that place data on the SRC bus. The decoders provide strobes to other registers. This condition allows a register to receive data from the DEST bus. The firmware uses two of the DEST strobes to aid testing. Bit 0 of the micro-instruction register determines if the user can toggle the conditional code that the CPU produces. The system feeds the conditional code that results to the sequencer and the skip instruction decoder. Sequencer control ROM translates the 4 bits from the instruction register, the reset bit, and the skip bit.

NT6X69AD (continued)

Sequencer translates the bits to formulate a 4-bit instruction that feeds to the sequencer. The skip instruction decoder examines bits 1 to 3 of the micro-instruction register and the conditional code. When the skip condition is correct, either of the following events can set the skip bit:

- the suppression of the clock to the CPU during the next cycle time sets the skip bit. An update of the CPU internal registers does not occur because of this condition.
- the equivalent of a continue instruction from the sequencer control ROM

The system accesses and executes the next instruction. The system does not store the result. A skip instruction cannot be skipped. The execution of the first skip instruction sets the skip bit and informs the internal CPU register that the register cannot store the result of the next instruction. The second skip instruction executes and sets the skip bit again. Sequencer data can come from the instruction register or from the DEST bus. The instruction bit that controls the multiplexer determines the data source. Output of the sequencer addresses the microstore ROM that produces the next instruction bits that the micro-instruction register latches.

The PP accesses the following functional blocks:

- the RAM shared with the SP
- the CRC ROM for CRC calculation that DMS-X protocol requires
- the process timing ROM, that allows the firmware to synchronize to the frame
- the RSTGEN, that allows the PP to initiate a shelf reset from the NT6X46 card
- the interrupt generator, that allows the PP to initiate a level 4 interrupt to the SP
- the network module (NM) interface
- the SB interface
- the IMC interface

SP and PP shared memory

The SP and PP communicate through an 8KX8 block of RAM. The two processes share this RAM transparently. This block of shared memory provides the following:

- work space for the PP
- a buffer for messages that the PP receives for the SP

- a buffer for messages that the SP places in a queue for the PP
- opcode area

The SP cannot continue to exercise the NM interface, the SB interface, and other interfaces. The PP firmware provides a set of opcodes that allow the SP to exercise these interfaces indirectly.

The first half of the instruction cycle concerns the PP read and write access. The first half of the instruction cycle makes the access of this RAM transparent to the PP and the SP. The second half of the cycle concern SP interface access. The two processors have read and write access over the whole address range of the memory. You must be careful when you perform a memory test on one processor. Make sure that the other processor does not write to the memory.

Shelf reset generator

To initiate a shelf reset, the PP performs the following sequence:

1. The PP clocks accesses the auxiliary reset strobe to reset the flip-flop.
2. Output of the reset flip-flop is driven to the backplane and connects to the NT6X46 card.
3. The NT6X46 card stops activity and issues the module reset signal to the the shelf that remains to acknowledge the reset.
4. The module reset that the NT6X46 card issues, clears the reset flip-flop on the NT6X69 card.

Cyclic redundancy check ROM

The CRC ROM contains two tables. Each table contains 256 bytes. A two-stage CRC accumulation process uses these tables.

Process timing ROM

Process timing ROM allows the PP to synchronize each process time slot for the frame boundary. The port/channel counter addresses the PROM that the PP can read at an instruction cycle.

Signaling processor interface

The SP memory map is standard on most cards that provide interface to the SP. The address and control signals are buffered. An access sequence synchronizes SP requests and generates a read or write access cycle. An access sequence performs these actions when a correct address appears in the range assigned to this card type. The interface is asynchronous and an acknowledge signal indicates the end of the access cycle.

NT6X69AD (continued)

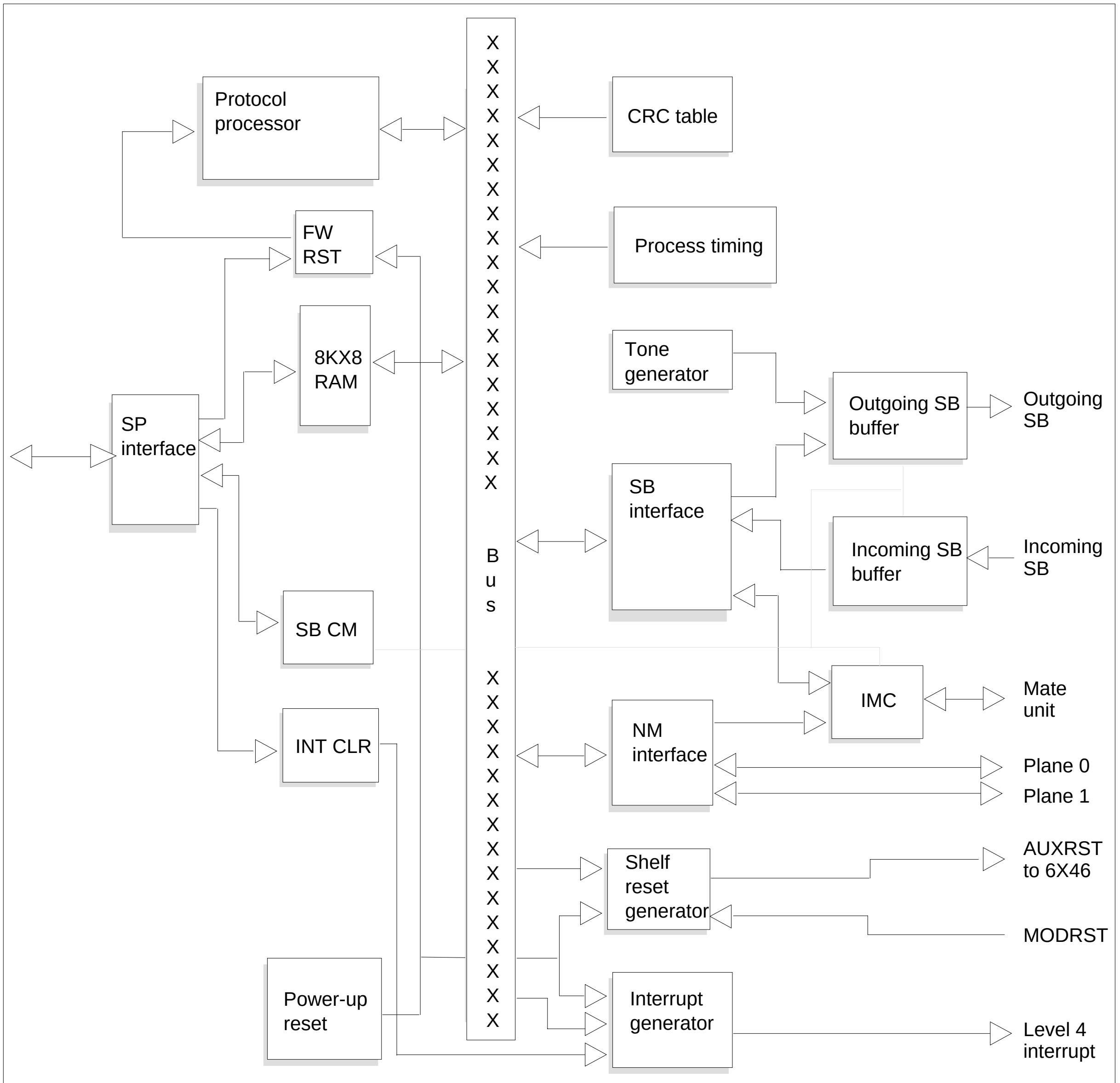
Power-up circuitry

A simple recording completing circuit resets the firmware and clears the INTGEN and auxiliary reset (AUXRST) flip-flops during a power-up.

The functional relationship between these blocks appears in the following figure.

NT6X69AD (continued)

NT6X69AD functional blocks



Note: CM enable signal

Signaling

Pin numbers

The pin numbers for the appear in the following figure.

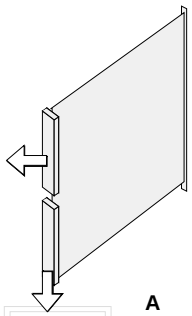
NT6X69AD (end)

NT6X69AD pin numbers

	A	B
1A 1B	GND	GND
2A 2B	5V	5V
3A 3B	5V	5V
4A 4B	5V	5V
5A 5B	GND	GND
6A 6B	FP–	C97T
7A 7B	GND	GND
8A 8B	–ACT	
9A 9B	C195TB*	
10A 10B	CPROCS–*	
11A 11B	GND	GND
12A 12B	DAS–	
13A 13B	LDS–	C97–B
14A 14B	DTRACK–	CPROCB
15A 15B	UDS–	RUN*
16A 16B	WRT–	TCEN–*
17A 17B	IMCOUT**	IMCIN**
18A 18B	GND	INT4REQ**
19A 19B		
20A 20B		
21A 21B	PIN0	POUT0
22A 22B	PIN1	POUT1
23A 23B	PIN2	POUT2
24A 24B	PIN3	POUT3
25A 25B	PIN4	POUT4
26A 26B	PIN5	POUT5
27A 27B	PIN6	POUT6
28A 28B	PIN7	POUT7
29A 29B	ADDR01+	
30A 30B	ADDR02+	
31A 31B	ADDR03+	
32A 32B	ADDR04+	
33A 33B	ADDR05+	
34A 34B	GND	GND
35A 35B	ADDR06+	–FPM
36A 36B	ADDR07+	GND
37A 37B	ADDR08+	C97M+
38A 38B	ADDR09+	GND
39A 39B	ADDR10+	CHOT
40A 40B	ADDR11+	CHOM

Notes:

1 * test channel signals, backplane connection not required
2 ** additional signals on the NT6902 card, but not on the NT6901



	A	B
41A 41B	GND	GND
42A 42B	ADDR12+	
43A 43B	ADDR13+	D0*
44A 44B	ADDR14+	D1*
45A 45B	ADDR15+	D2*
46A 46B	ADDR16+	D3*
47A 47B	ADDR17+	D4*
48A 48B	ADDR18+	D5*
49A 49B	ADDR19+	D6*
50A 50B	ADDR20+	D7*
51A 51B	ADDR21+	
52A 52B	SEN0	DESTXT0–
53A 53B	SEN1	DESTXT1–
54A 54B	SEN2	
55A 55B	PSPEN+	SRCXTO–
56A 56B	CSPEN+	SRCXT1–
57A 57B	GND	GND
58A 58B	DATA00+	SRC0*
59A 59B	DATA01+	SRC1*
60A 60B	DATA02+	SRC2*
61A 61B	DATA03+	SRC3*
62A 62B	DATA04+	SRC4*
63A 63B	DATA05+	SRC5*
64A 64B	GND	SRC6*
65A 65B	DATA06+	SRC7*
66A 66B	DATA07+	
67A 67B		CHOS0
68A 68B		CHOR0
69A 69B		CHOS1
70A 70B		CHOR1
71A 71B		
72A 72B		
73A 73B		
74A 74B		AUXRST–**
75A 75B		MODRST–**
76A 76B	GND	GND
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

DMS-100 Family

Hardware Description Manual

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