Critical Release Notice

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The content of this customer NTP supports the SN06 (DMS) software release.

Bookmarks used in this NTP highlight the changes between the LEC0015 baseline and the current release. The bookmarks provided are color-coded to identify release-specific content changes. NTP volumes that do not contain bookmarks indicate that the LEC0015 baseline remains unchanged and is valid for the current release.

Bookmark Color Legend

Black: Applies to new or modified content for LEC0015 that is valid through the current release.

Red: Applies to new or modified content for SN04 (DMS) that is valid through the current release.

Blue: Applies to new or modified content for SN05 (DMS) that is valid through the current release.

Green: Applies to new or modified content for SN06 (DMS) that is valid through the current release.

Attention!
Adobe® Acrobat® Reader™ 5.0 or higher is required to view bookmarks in color.

Publication History

June 2005

Standard release 11.03 for software release SN06 (DMS). Updates made for this release are shown below:

Volume 5

Added NTDX16AA (Q00946403)

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Standard release 11.02 for software release SN06 (DMS). Updates made for this release are shown below:

Volumes 1 – 3

No changes

Volume 4

Card NT9X30AB is Manufacture Discontinued and is replaced by new card NT9X30AC.

Volume 5

No changes

September 2003

Standard release 11.01 for software release SN06 (DMS). Updates made for this release are shown below:

Volumes 1 – 4

No changes

Volume 5

Updates were made to NT9X76AA according to CR Q00177945.

297-8991-805

DMS-100 Family

Hardware Description Manual

Volume 4 of 5

2001Q1 Standard 09.01 March 2001

NORTEL NETWORKS

How the world shares ideas.

DMS-100 Family

Hardware Description Manual

Volume 4 of 5

Publication number: 297-8991-805
Product release: 2001Q1
Document release: Standard 09.01
Date: March 2001

Contents

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1 NT6Xnnaa (continued)

NT6X69DA through NT6X99AA (continued from Vol. 3)

NT6X69DA

Product description

The NT6X69DA replaces the NT6X43DA message interface card in the international market. The NT6X69 has the capabilities of the NT6X43. The NT6X69 can process message protocols.

Functional description

Functional blocks

The NT6X69DA contains the following functional blocks:

- parallel speech bus (SB) message interface
- SB connection memory (CM)
- inter module connection (IMC) interface
- interrupt generator
- tone generator
- protocol processor (PP)
- signaling processor (SP) and PP shared memory
- shelf reset generator
- cyclic redundancy check (CRC) ROM
- process timing ROM
- SP interface
- power–up circuits

Parallel speech bus message interface

The parallel SB message interface in the NT6X69 differs from the SB message interface in the NT6X43. In the NT6X43, the asynchronous SP sends messages on the synchronous SB. The system requires circuits that synchronize. Synchronizing circuits consist of a frame level interrupt and a double buffer. In the NT6X69, the synchronous PP sends the message so that all the NT6X69 needs is the following. The NT6X69 needs a transmit (Tx) RAM and holding registers, and a receive (Rx) RAM and holding registers. The holding register pairs are the outgoing SB Tx/Rx pair and the IMC Tx/Rx pair. The CM controls gating of register output for each time slot. The system dedicates the first half of the instruction to PP to write to Tx RAM or to read from Rx RAM. In the second half, data latches in the Tx holding register from the Tx RAM according to the port/channel counter. The system writes data to the Rx RAM from the Rx holding register.

Speech bus connection memory

The CM arbitrates the access of different service cards to the SB on a time slot condition. The SP accesses the CM in the same way as the SP and PP shared memory. The PP cannot access the CM. In the first half of the instruction cycle, the port/channel counter addresses the CM. The data latches to a holding register. The data in the holding register addresses CM decoding PROM. This action enables the tone driver, SB drivers and receivers, and an IMC register on the NT6X69. Two bits from the holding register are fed to the formatter and the time switch through the backplane. Three other bits from the holding register are accessible through spare slots on the backplane.

Note: T bits are not identical to the bits of the NT6X43 card. There are more functions in the decoding circuits like IMC messaging and the tone checksum.

Intermodule connection interface

The IMC interface provides a 64 kbps link to the mate unit. The link appears to the PP as an SB time slot. The SP assigns the time slot through the CM.

The IMC circuits is a shift register loaded with data. The IMC holding register loads the data in the SB interface when the CM enables the SB. Data exchanges occur between the two shelves during the active channel 0 (CH0) time. The active clock gates the data exchange. The system can assign the IMC time slot away from the CH0 time to avoid data corruption. The IMC link does not use the SB. The IMC time slot on the SB is available for pulse code modulation (PCM) or tones.

Errors can occur with the IMC link when the two shelves are out of synchronization. The reasons for these errors are as follows:

- The CM circuits on the inactive unit runs on the inactive clock. If the units slip, the inactive IMC time slot can occur at the active CH0 time.
- The PP is frame synchronized to the PP shelf. The PP can miss or double–read the register when the units slip.

Interrupt generator

The system provides interrupt generation for the PP to signal to the SP. The interrupt generation relieves the SP from polling the message queue pointers. The PP can access the INTSTB strobe to initiate a level 4 interrupt.

Tone generator

Tone generation circuits on the NT6X69 card contain the R09 generating chip, the tone PROM, and the tone holding register. The system maps T0, T1, and T2 bits from the connection memory to two tone control bits on the R09. The

NT6X69DA (continued)

system maps the bits to specify the type of time slot. Eight–bit data from the R09 latches to the holding register. The CM circuits control gating of the contents of the holding register to the outgoing SB.

Protocol processor

A 32–bit instruction from microstore ROM latches to the micro–instruction register every processor cycle. The micro–instruction register controls the following:

- CPU
- CPU data multiplexer
- zero/not–zero conditional code
- skip instruction decoder
- destination/source (DEST/SRC) decoder
- sequencer
- sequencer data multiplexer

The CPU receives instructions from the instruction register (INST REG). The CPU produces an 8–bit result on the designation bus and a 1–bit zero conditional code. Direct data input from the multiplexer can be from the INST REG for immediate data. Direct data from the muliplexer can be from the SRC bus for external data. Data beginning depends on the instruction type. The DEST/SRC decoders arbitrate the different external registers that put data on the SRC bus, and provide strobes to other registers. This condition allows one register to receive data from the DEST bus. The firmware uses two of the DEST strobes to aid tests. The CPU produces a conditional code. This code can toggle and depends on bit 0 of the micro–instruction register. The conditional code that results feeds to the sequencer and to the skip instruction decoder. Sequencer control ROM translates the four bits from the instruction register, the reset bit, and the skip bit. The sequencer control ROM formulates a 4–bit instruction fed to the sequencer. The skip instruction decoder examines bits 1 to 3 of the micro–instruction register and the conditional code. When the skip condition is valid, the skip bit is set by the suppression of the clock to the CPU. The skip bit is set during the next cycle time, as a result, the CPU internal registers are not updated. The skip bit can be set by the equivalent of a continue instruction from the sequencer control ROM.

The system accesses and executes the next instruction. The system does not store the result. The system cannot skip an instruction. The execution of the first skip instruction sets the skip bit. The execution tells the internal CPU register not to store the result of the next instruction. The second skip instruction executes and sets the skip bit again. Sequencer data can come from

the instruction register or from the DEST bus. Where the sequencer data comes from depends on the instruction bit that controls the multiplexer. Output of the sequencer addresses microstore ROM that produces the next instruction bits that the micro–instruction register catches.

The PP accesses the following functional blocks:

- RAM shared with the SP
- CRC ROM for CRC calculation the DMS–X protocol requires
- process timing ROM, that allows the firmware to synchronize to the frame
- shelf reset generator that allows the PP to initiate a shelf reset from the NT6X46 card
- interrupt generator that allows the PP to initiate a level 4 interrupt to the SP
- network module (NM) interface
- SB interface
- IMC interface

SP and PP shared memory

The SP and PP communicate through an 8KX8 block of RAM that the two processors share. This block of shared memory serves as:

- workspace for the PP
- buffer for messages the PP receives for the SP
- buffer for messages the SP queues for the PP
- opcode area

The SP cannot directly apply the NM interface, the SB interface and other interfaces. The PP firmware provides a set of opcodes that allow the SP to apply these interfaces indirectly.

The first half of the instruction cycle is for PP read and write access. The first half of the cycle makes the access of this RAM transparent to the PP and the SP. The second half of the cycle is for access by the SP interface. Both processors have read and write access over the complete address range of the memory. When the system performs a memory test for one processor, the other processor must not write the memory.

NT6X69DA (continued)

Shelf reset generator

The PP performs the following sequence to initiate a shelf reset:

1. The PP accesses the auxiliary reset strobe to clock the reset flip–flop.
2. Output of the reset flip–flop is driven to the backplane and connects to the NT6X46 card.
3. The NT6X46 card ceases activity and issues the module reset signal to the rest of the shelf to acknowledge the reset.
4. The module reset the NT6X46 card issues clears the reset flip–flop on the NT6X69 card.

Cyclic redundancy check ROM

The CRC ROM has two tables. Each table contains 256 bytes. A two–stage CRC accumulation process uses these tables.

Process timing ROM

Process timing ROM allows the PP to synchronize each process time slot for the frame limit. The port/channel counter addresses PROM that the PP can read at any instruction cycle.

Signaling processor interface

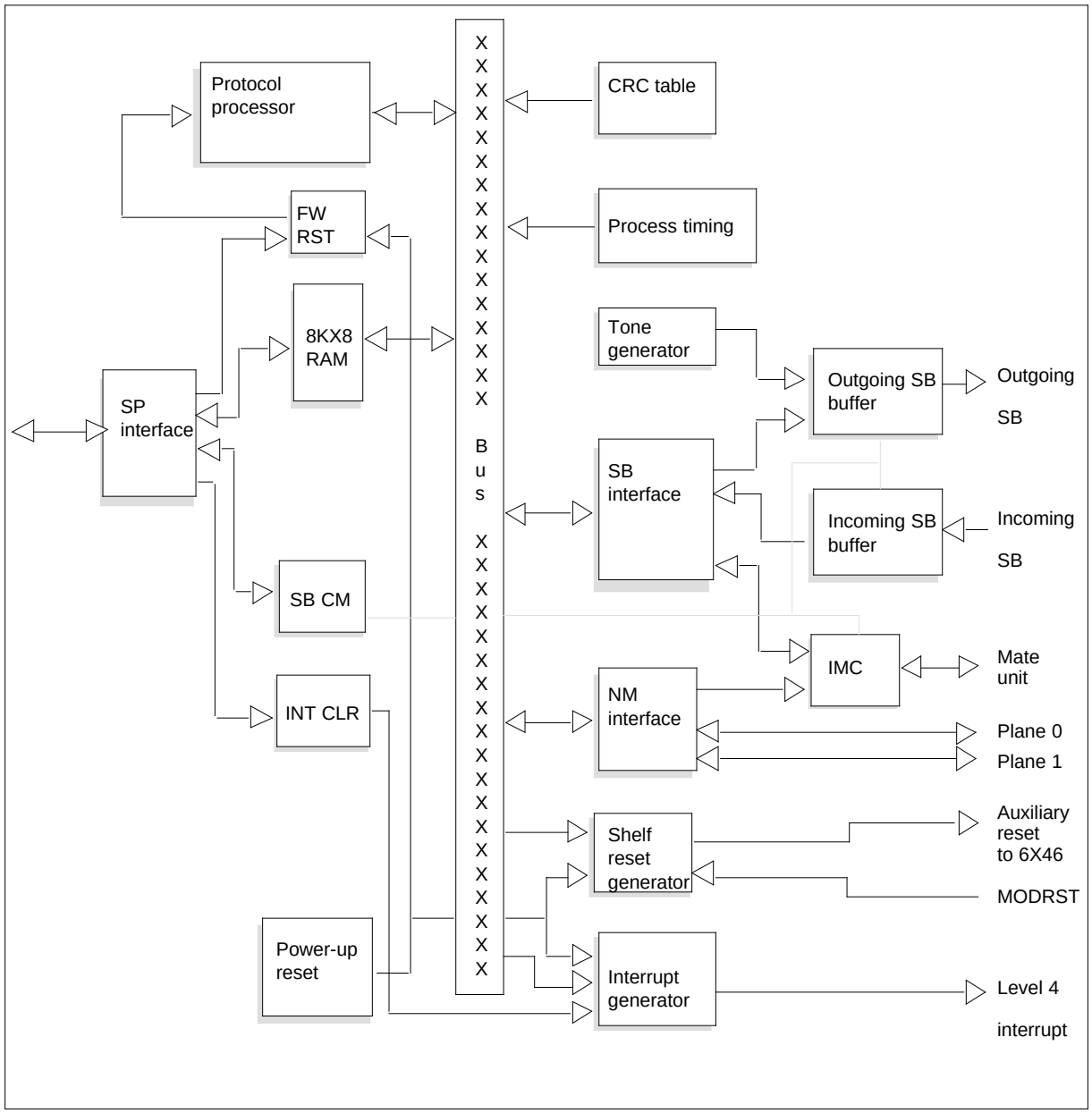
The SP memory map is standard on the cards that interface to the SP. Address and control signals are buffered. An access sequence synchronizes SP requests and generates a read or write access cycle. This condition occurs when a valid address falls in the range that the system assigns to this card type. The interface is asynchronous and an acknowledge signal indicates the end of the access cycle.

Power–up circuits

A simple recording completing (RC) circuit resets the firmware and clears the interrupt generator and auxiliary reset flip–flops during power–up.

The working relationship between the above blocks appears in the following figure.

NT6X69DA functional blocks



Signaling

Pin numbers

The pin numbers for the NT6X69DA appear in the following figure.

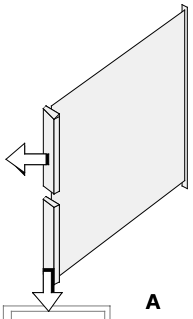
NT6X69DA (end)

NT6X69DA pin numbers

		A	B
1A	1B	GND	GND
2A	2B	5V	5V
3A	3B	5V	5V
4A	4B	5V	5V
5A	5B	GND	GND
6A	6B	FP-	C97T
7A	7B	GND	GND
8A	8B	-ACT	
9A	9B	C195TB*	
10A	10B	CPROCS-*	
11A	11B	GND	GND
12A	12B	DAS-	
13A	13B	LDS-	C97-B
14A	14B	DTRACK-	CPROCB
15A	15B	UDS-	RUN*
16A	16B	WRT-	TCEN-*
17A	17B	IMCOUT**	IMCIN**
18A	18B	GNDI	NT4REQ**
19A	19B		
20A	20B		
21A	21B	PIN0	POUT0
22A	22B	PIN1	POUT1
23A	23B	PIN2	POUT2
24A	24B	PIN3	POUT3
25A	25B	PIN4	POUT4
26A	26B	PIN5	POUT5
27A	27B	PIN6	POUT6
28A	28B	PIN7	POUT7
29A	29B	ADDR01+	
30A	30B	ADDR02+	
31A	31B	ADDR03+	
32A	32B	ADDR04+	
33A	33B	ADDR05+	
34A	34B	GND	GND
35A	35B	ADDR06+	-FPM
36A	36B	ADDR07+	GND
37A	37B	ADDR08+	C97M+
38A	38B	ADDR09+	GND
39A	39B	ADDR10+	CHOT
40A	40B	ADDR11+	CHOM

Notes:
1 * test channel signals, no backplane connection needed

2 ** additional signals on the NT6902 card, but not on the NT6901



		A	B
41A	41B	GND	GND
42A	42B	ADDR12+	
43A	43B	ADDR13+	D0*
44A	44B	ADDR14+	D1*
45A	45B	ADDR15+	D2*
46A	46B	ADDR16+	D3*
47A	47B	ADDR17+	D4*
48A	48B	ADDR18+	D5*
49A	49B	ADDR19+	D6*
50A	50B	ADDR20+	D7*
51A	51B	ADDR21+	
52A	52B	SEN0	DESTXT0-
53A	53B	SEN1	DESTXT1-
54A	54B	SEN2	
55A	55B	PSPEN+	SRCXTO-
56A	56B	CSPEN+	SRCXT1-
57A	57B	GND	GND
58A	58B	DATA00+	SRC0*
59A	59B	DATA01+	SRC1*
60A	60B	DATA02+	SRC2*
61A	61B	DATA03+	SRC3*
62A	62B	DATA04+	SRC4*
63A	63B	DATA05+	SRC5*
64A	64B	GND	SRC6*
65A	65B	DATA06+	SRC7*
66A	66B	DATA07+	
67A	67B	CHOS0	
68A	68B	CHOR0	
69A	69B	CHOS1	
70A	70B	CHOR1	
71A	71B		
72A	72B		
73A	73B		
74A	74B	AUXRST-**	
75A	75B	MODRST-**	
76A	76B	GND	GND
77A	77B		
78A	78B	GND	GND
79A	79B		
80A	80B	GND	GND

NT6X69LA

Product description

The NT6X69LA replaces any of the international variants of the NT6X69AB North American base pack. The NT6X69LA replaces the NT6X69BB (Turkey), the NT6X69DA (UK), the NT6X69FA (CEP), and the NT6X69KA (China). These variants differ only in the contents of the EPROM U20. The EPROM U20 holds the tone sets.

The NT6X69LA has 128 kbytes of RAM, with circuit support that replaces the 64 kbytes EPROM U20. This condition allows software to create and load tone sets.

The NT6X69LA has the ability to process message protocol and receive variable tone sets from the CC.

Location

The NT6X69LA is in slot 10.

Functional description

Functional blocks

The NT6X69LA has the following functional blocks:

- network message (NM) interface
- parallel speech bus (SB) message interface
- SB connection memory
- intermodule connection (IMC) interface
- tone generator and tone RAM
- protocol processor (PP)
- facilities processor (FP) and PP shared memory
- shelf reset generator
- cyclic redundancy check (CRC) ROM
- process timing ROM
- FP interface

Network message interface

The channel 0 (CH0) signal from the active formatter tells data to leave and enter the shift registers. The CHO signal tells data to enter the NM interface serially. Data from the transmit hold register loads to the shift register before the CH0 time in every frame. After the CH0 time, data loads to the receive

NT6X69LA (continued)

holding register from the shift register. The PP can read from or write to the holding registers at any time but during CH0.

Parallel speech bus message interface

The synchronous PP in the SB interface transmits the message. The first half of the instruction cycle is for the PP. The PP writes to the transmit RAM or reads from the receive RAM. In the second half of the instruction cycle, the system puts data in the transmit holding register from the transmit RAM. This condition occurs according to the port/channel counter. Data writes to the receive RAM from the receive holding register.

Speech bus connection memory

The connection memory arbitrates the access of the different service cards to the SB on a time slot condition. The FP accesses the connection memory in the same way as the PP/FP shared memory. The PP cannot access the connection memory.

Intermodule connection interface

The IMC interface appears to the PP as a SB time slot. The FP assigns the time slot through the connection memory. The system exchanges data between the two shelves during the active CH0 time. The active clock gates the data exchange. Errors can occur with the IMC link when the two shelves are out of synchronization.

Tone generator and tone RAM

Tone generation circuits on the NT6X69LA card have the following:

- R09 tone generation chip
- tone RAM
- supporting circuits that provide for expansion of tone sample memory from 64 kbytes to 128 kbytes
- tone holding register

Protocol processor

The functional blocks that the protocol processor (PP) accesses appear below:

- 8K× 8 RAM shared with the FP
- CRC ROM for CRC calculation the DMS–X protocol requires
- process timing ROM that allows the firmware to synchronize to the frame
- RSTGEN that allows the PP to initiate a shelf reset (MODRST) from the NT6X46 card (signaling processor memory plus card)
- INTGEN that allows the PP to initiate a level–four interrupt to the FP

- NM interface
- speech bus interface
- IMC interface

Facilities processor and protocol processor shared memory

The SP and PP communicate through an 8K×8 block of RAM that the two processors transparently share. This block serves as:

- a work space for the PP
- a buffer for messages the PP receives for the SP, and for messages the SP queues for the PP
- an opcode area that allows the SP to apply the interfaces indirectly

Shelf reset generator

The PP can initiate a shelf reset with the following sequence:

- the PP accesses the auxiliary reset strobe to clock the reset flip–flop
- the output of the reset flip–flop is driven to the backplane and connects to the NT6X46 card
- the NT6X46 card stops activity and issues the module reset signal to the rest of the shelf to acknowledge the reset
- the module reset that the NT6X46 card issues clears the reset flip–flop on the NT6X69 card

Cyclic redundancy check ROM

This ROM contains two tables used in a two–stage CRC accumulation process. To access the upper page, the PP can use the CRCL strobe that the CRCH strobe follows. To access the lower page, the PP only uses the CRCL strobe.

Process timing ROM

Process timing PROM allows the PP to synchronize each process time slot for the frame limit. The port/channel counter addresses the PROM. The PP can read the PROM during any instruction cycle.

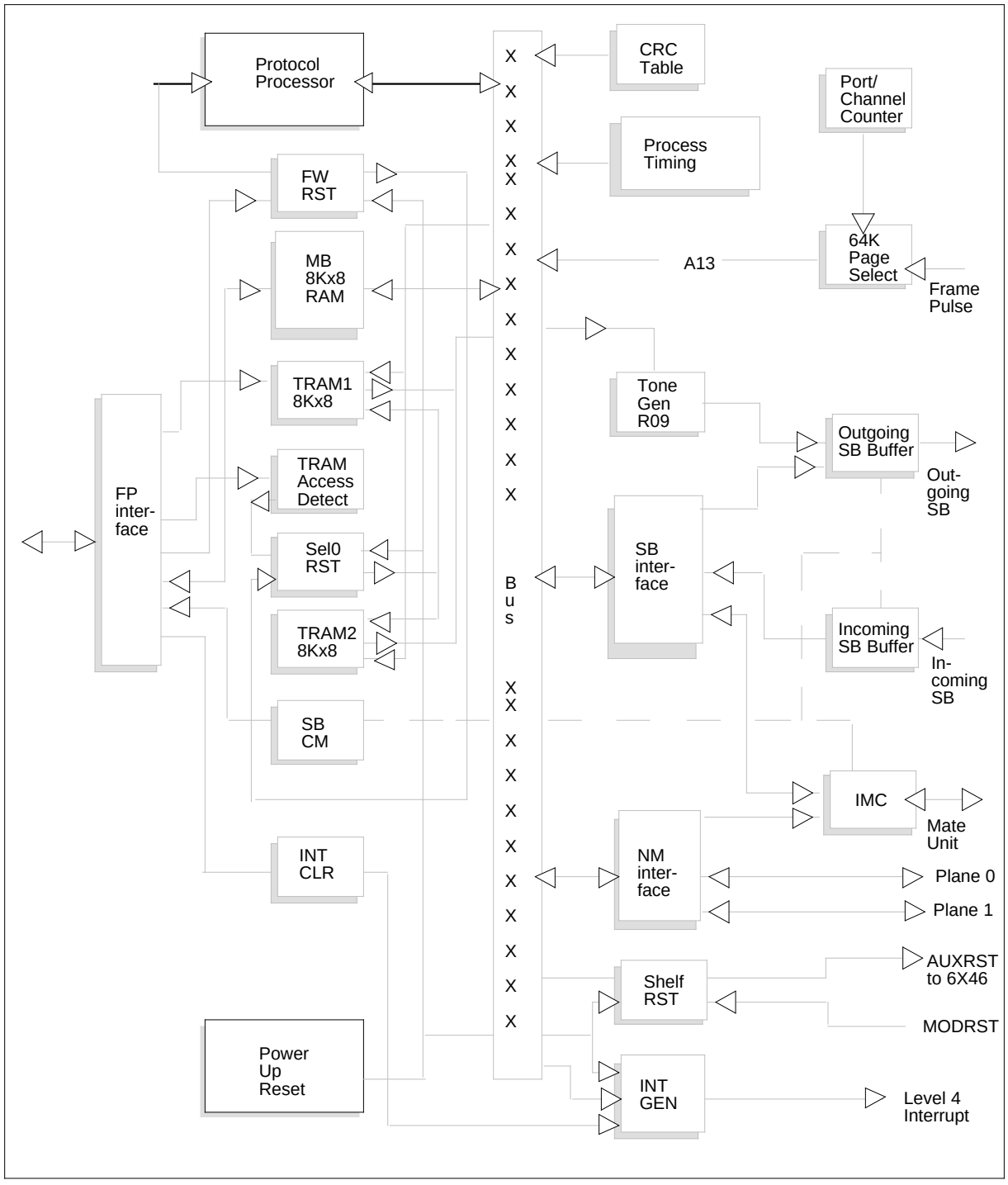
Facilities processor interface

Address and control signals are buffered. An access sequence synchronizes FP requests and generates a read or write access cycle. This action occurs when a valid address falls in the range that the system assigns to this card type. The interface is asynchronous and an acknowledge signal indicates the end of the access cycle.

The relationship between the functional blocks appears in the following figure.

NT6X69LA (continued)

NT6X69LA functional blocks



Signaling

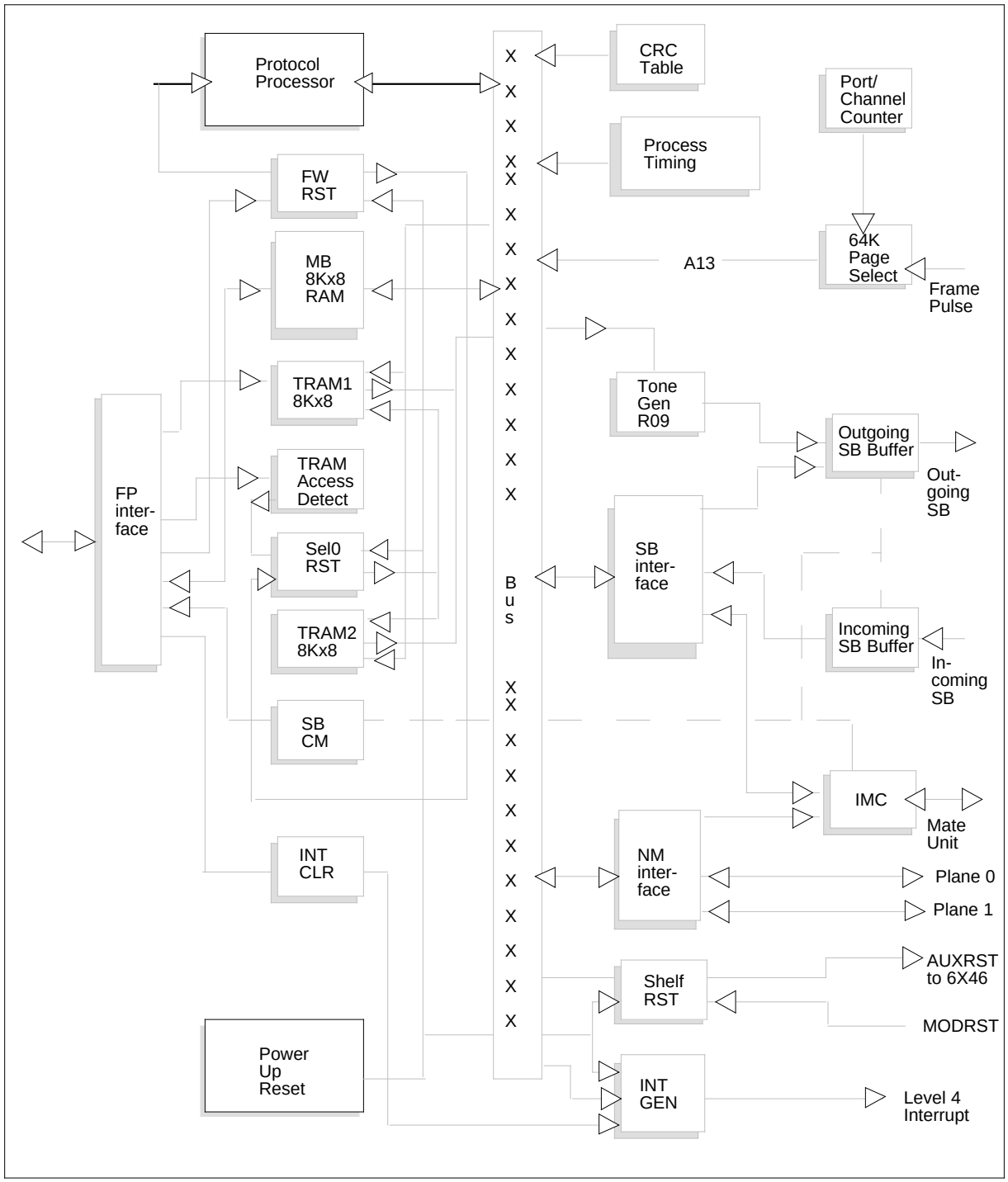
Pin numbers

The following figure shows the pin numbers for NT6X69LA.

Note: * denotes test channel signals, no backplane connection needed. ** denotes additional signals on the 6902 card but not on the 6901. *** denotes temporary signals that the NT6X79 card requires.

NT6X69LA (continued)

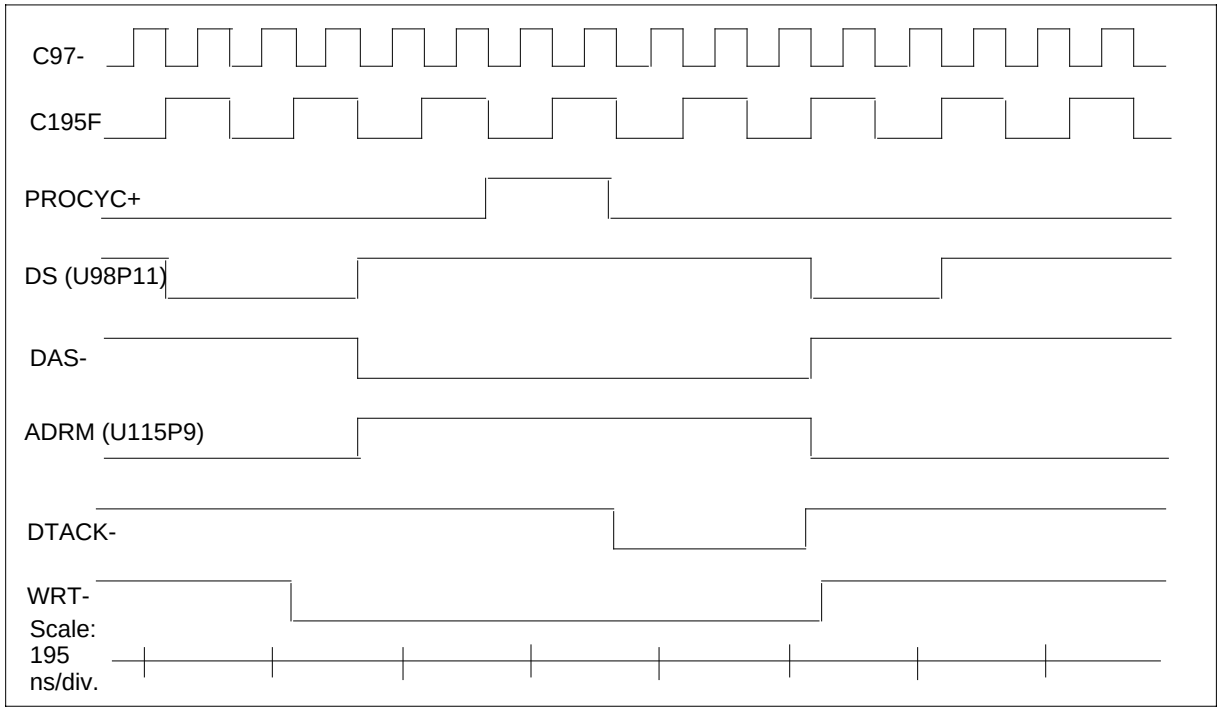
NT6X69LA pin numbers



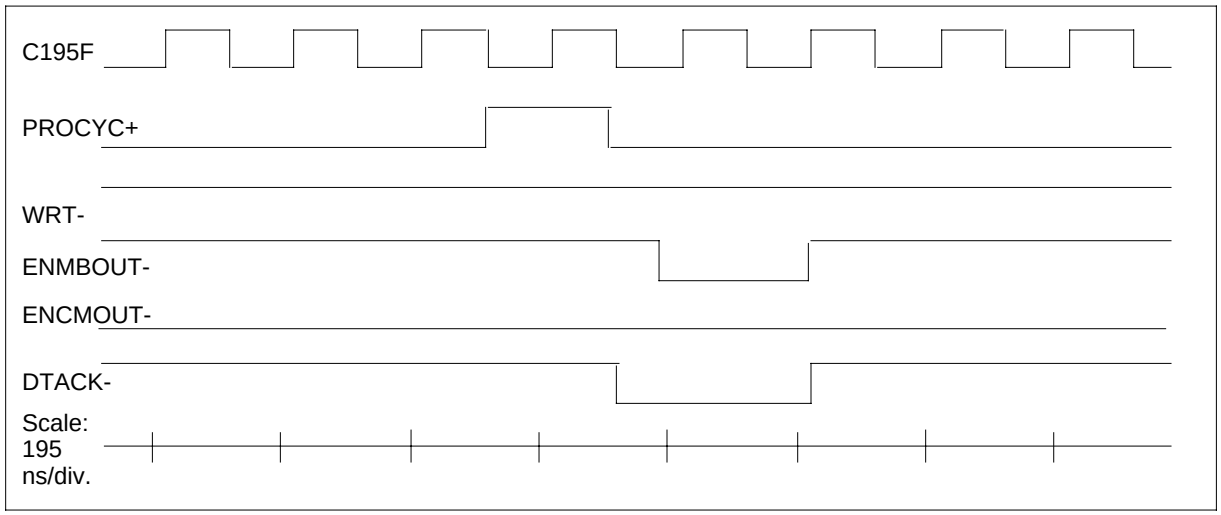
Timing

The timing for the NT6X69LA appear in the following figures.

NT6X69LA A–bus interface timing: FP write cycle

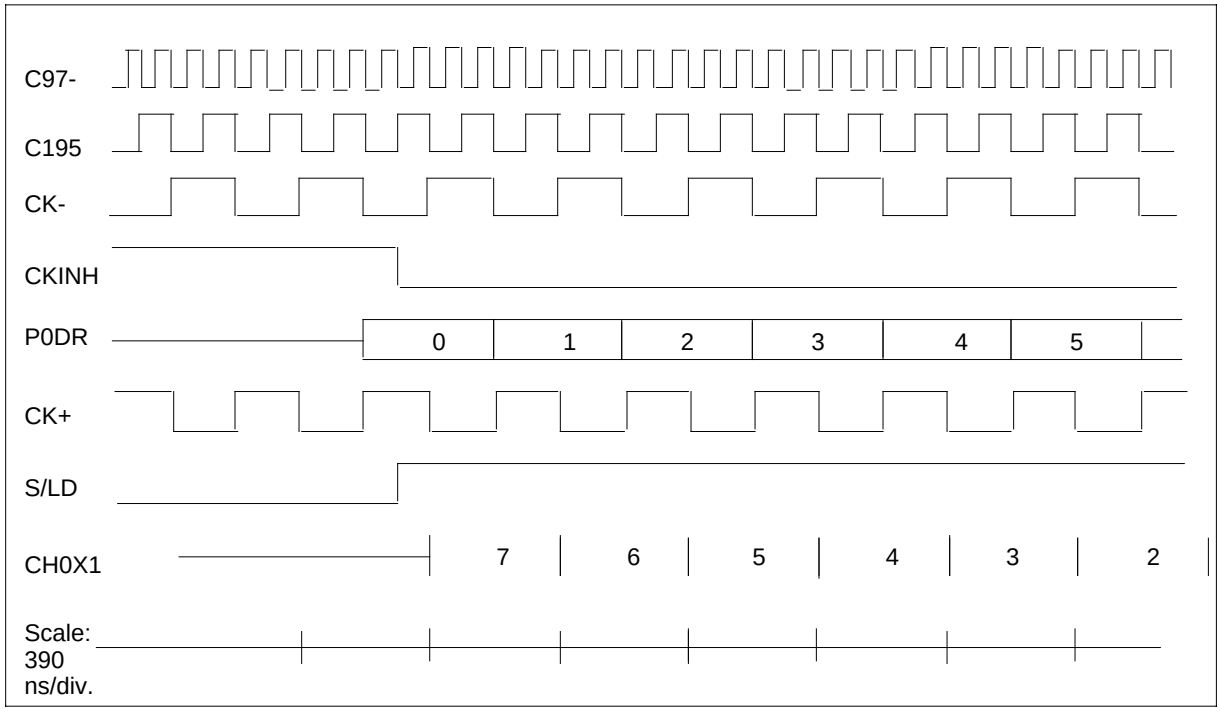


NT6X69LA A–bus interface timing: FP read cycle



NT6X69LA (end)

NT6X69LA network module interface timing



NT6X69LB

Product description

The system uses the NT6X69LB CPP message protocol and downloadable tones card. This card replaces any of the international variants of the NT6X69AB North American base pack. These variants are the NT6X69BB (Turkey), the NT6X69DA (UK), the NT6X69FA (CEP), and the NT6X69KA (China). These variants differ only in the contents of the EPROM U20. The EPROM U20 holds the tone sets.

The NT6X69LB has 128 kbytes of RAM with supporting circuits that replace the 64 kbyte EPROM U20. This RAM allows software to create and load tone sets.

The NT6X69LB processes message protocol and receives variable tone sets from the central control (CC).

Location

The NT6X69LB is in slot 10.

Functional description

Functional blocks

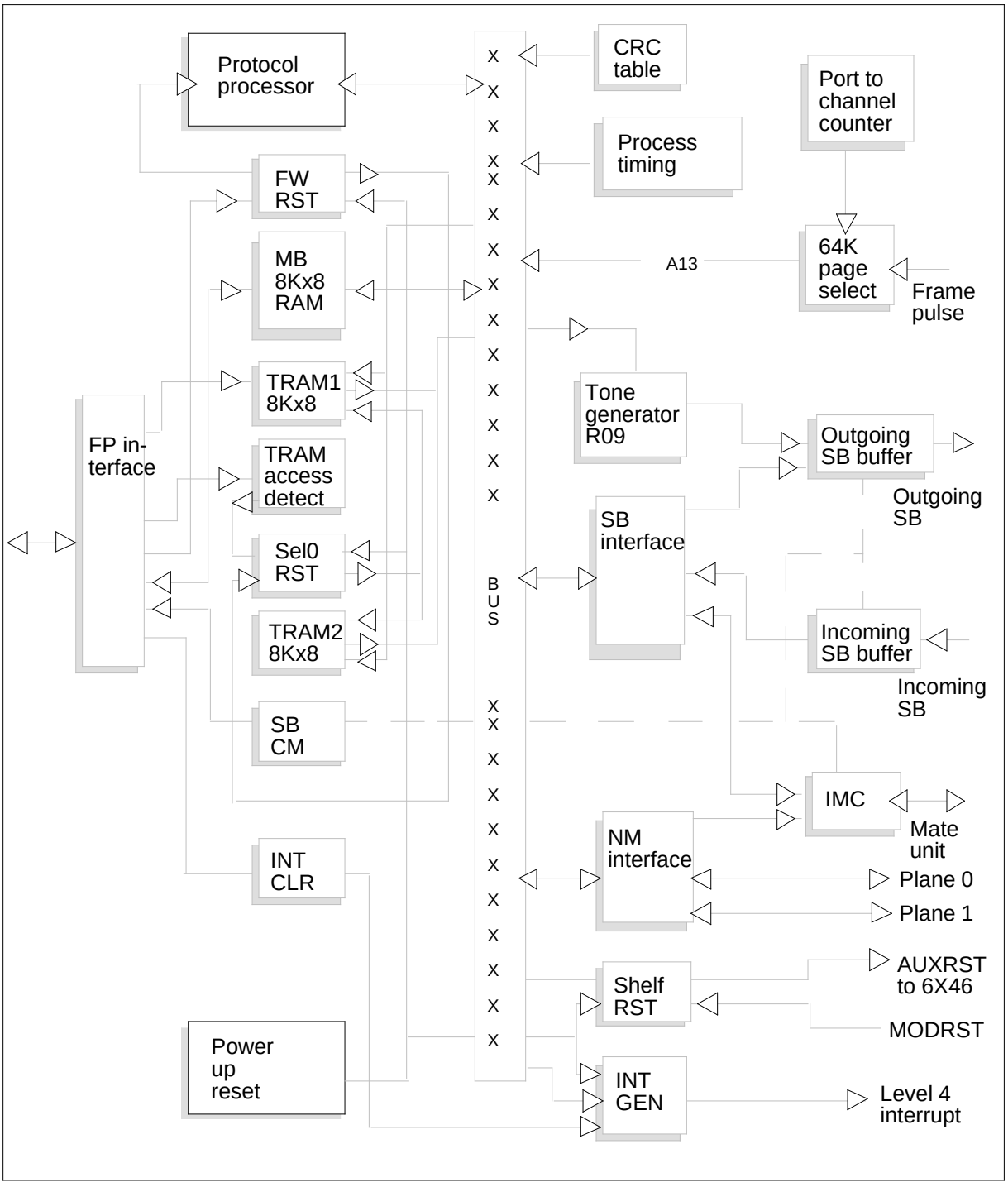
The NT6X69LB contains the following functional blocks:

- network message (NM) interface
- parallel speech bus (SB) message interface
- SB connection memory
- inter–module connection (IMC) interface
- interrupt generator
- tone generator and tone RAM
- protocol processor (PP)
- facilities processor (FP) and PP shared memory
- shelf reset generator
- cyclic redundancy check (CRC) ROM
- process timing ROM
- FP interface

The relationship between the functional blocks appears in the following figure.

NT6X69LB (continued)

NT6X69LB functional blocks



Network message interface

The channel 0 (CH0) signal from the active formatter tells data to leave and enter the NM interface shift registers serially. Data from the transmit hold register loads to the shift register in every frame before the CH0 time. Data from the shift register loads into the receive holding register in every frame after the CH0 time. The PP can read from or write to the holding registers at any time other than CH0.

Parallel speech bus message interface

The synchronous PP in the SB interface sends out the message. The first half of the instruction cycle is for the PP. This part is for the PP to write to the transmit RAM or to read from the receive RAM. In the second half of the instruction cycle, data is put in the transmit holding register. The port and channel counter determines how the data is put in the transmit holding register from the transmit RAM. The receive holding register writes data to the receive RAM.

Speech bus connection memory

The connection memory controls access of the different service cards to the SB on a time–slot condition. The FP accesses the connection memory in the same way as the PP/FP shared memory. The PP cannot access the connection memory.

Inter–module connection interface

The IMC interface appears to the PP as an SB time slot. The FP assigns the time slot through the connection memory. The system exchanges data between the two shelves during the active CH0 time. The active clock gates the data exchange. Errors can occur with the IMC link when the two shelves are out of synchronization.

Tone generator and tone RAM

Tone generation circuits on the NT6X69LB card have the following:

- R09
- tone generation chip
- tone RAM
- supporting circuits, to provide for expansion of tone sample memory from 64 kbyte to 128 kbyte
- tone holding register

NT6X69LB (continued)

Protocol processor

The PP accesses the following functional blocks:

- 8–kbyte–by–8 RAM shared with the FP
- CRC ROM for CRC calculation the DMS-X protocol requires
- process timing ROM that allows the firmware to synchronize to the frame
- RSTGEN that allows the PP to initiate a shelf reset (MODRST) from the NT6X46 card
- INTGEN that allows the PP to initiate a level–four interrupt to the FP
- NM interface
- speech bus interface
- IMC interface

Facilities processor and protocol processor shared memory

The FP and PP communicate through an 8–kbyte–by–8 block of RAM that the two processors transparently share.

This block serves several functions:

- a work space for the PP
- a buffer for messages the PP receives for the FP and for messages the FP queues for the PP
- an opcode area that allows the FP to access the interfaces indirectly

Shelf reset generator

The PP can initiate a shelf reset with the following sequence:

1. The PP accesses the auxiliary reset strobe to clock the reset flip–flop.
2. The output of the reset flip–flop is driven to the backplane and connects to the NT6X46 card.
3. The NT6X46 card gives up activity and issues the module reset signal to the rest of the shelf to acknowledge the reset.
4. The module reset that the NT6X46 card issues clears the reset flip–flop on the NT6X69 card.

Cyclic redundancy ROM

A two–stage CRC accumulation process uses the two tables in this ROM. To access the upper page, the PP can use the CRCL strobe followed by the CRCH strobe. To access the lower page, the PP uses the CRCL strobe only.

Process timing ROM

Process timing PROM allows the PP to synchronize each process time slot according to the frame limit. The port and channel counter addresses the PROM. The PP can read the PROM during any instruction cycle.

Facilities processor interface

Address and control signals are buffered. An access sequence synchronizes FP requests and generates a read or write access cycle. This action occurs when a valid address falls in the range that the system assigns to this card type. The interface is asynchronous and an acknowledge signal indicates the end of the access cycle.

Signaling

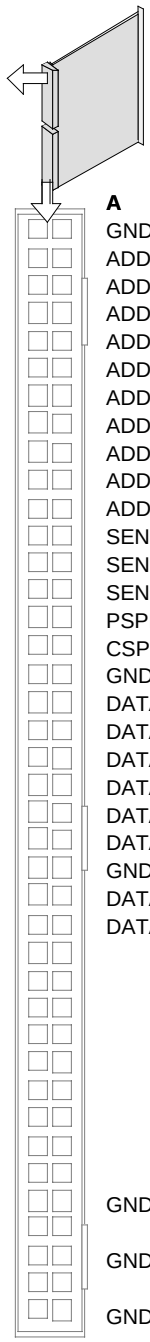
Pin numbers

The pin numbers for NT6X69LB appear in the following figure.

NT6X69LB (continued)

NT6X69LB pin numbers

	A	B
1	GND	GND
2	5V	5V
3	5V	5V
4	5V	5V
5	GND	GND
6	FP–	C97T
7	GND	GND
8	–ACT	
9	C195TB*	
10	CPROCS–*	
11	GND	GND
12	DAS–	
13	LDS–	C97–B
14	DTACK–	CPROCB
15	UDS–	RUN*
16	WRT–	TCEN–*
17	IMCOUT**	IMCIN**
18	GND	INT4REQ**
19		
20		
21	PIN0	POUT0
22	PIN1	POUT1
23	PIN2	POUT2
24	PIN3	POUT3
25	PIN4	POUT4
26	PIN5	POUT5
27	PIN6	POUT6
28	PIN7	POUT7
29	ADDR01+	
30	ADDR02+	
31	ADDR03+	
32	ADDR04+	
33	ADDR05+	
34	GND	GND
35	ADDR06+	–FPM
36	ADDR07+	GND
37	ADDR08+	C97M+
38	ADDR09+	GND
39	ADDR10+	CH0T
40	ADDR11+	CH0M



	A	B
41	GND	GND
42	ADDR12+	
43	ADDR13+	D0*
44	ADDR14+	D1*
45	ADDR15+	D2*
46	ADDR16+	D3*
47	ADDR17+	D4*
48	ADDR18+	D5*
49	ADDR19+	D6*
50	ADDR20+	D7*
51	ADDR21+	
52	SEN0	DESTXT0–
53	SEN1	DESTXT1–
54	SEN2	
55	PSPEN+	SRCXT0–
56	CSPEN+	SRCXT1–
57	GND	GND
58	DATA00+	SRC0*
59	DATA01+	SRC1*
60	DATA02+	SRC2*
61	DATA03+	SRC3*
62	DATA04+	SRC4*
63	DATA05+	SRC5*
64	GND	SRC6*
65	DATA06+	SRC7*
66	DATA07+	
67		CH0S0
68		CH0R0
69		CH0S1
70		CHOR1
71		(T1***)
72		(T2***)
73		T3***)
74		AUXRST–**
75		MODRST–**
76	GND	GND
77		
78	GND	GND
79		
80	GND	GND

* = test channel signals, no backplane connection needed.

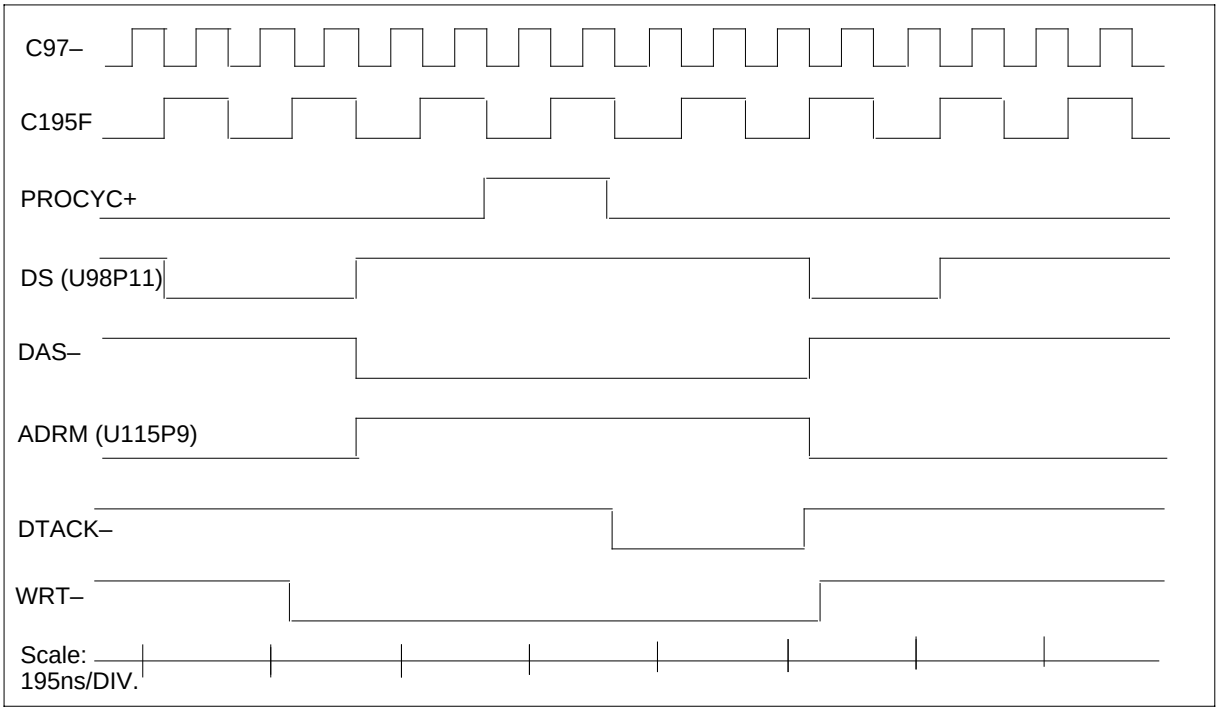
** = additional signals on the 6902 card but not on the 6901.

*** = temporary signals that the NT6X79 card requires.

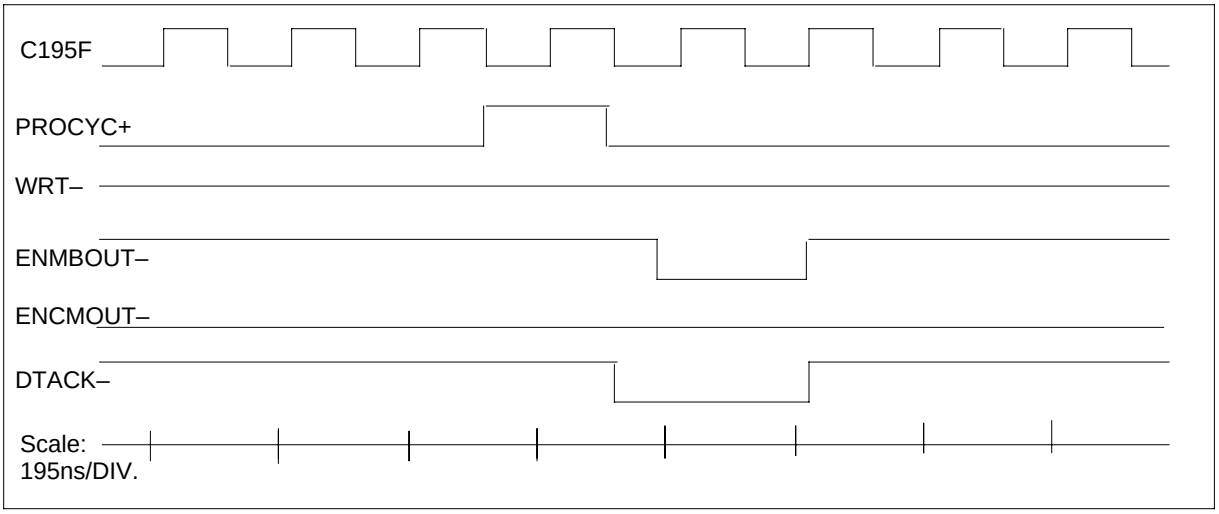
Timing

The timing for the NT6X69LB appears in the following figures.

NT6X69LB A–bus interface timing: FP write cycle

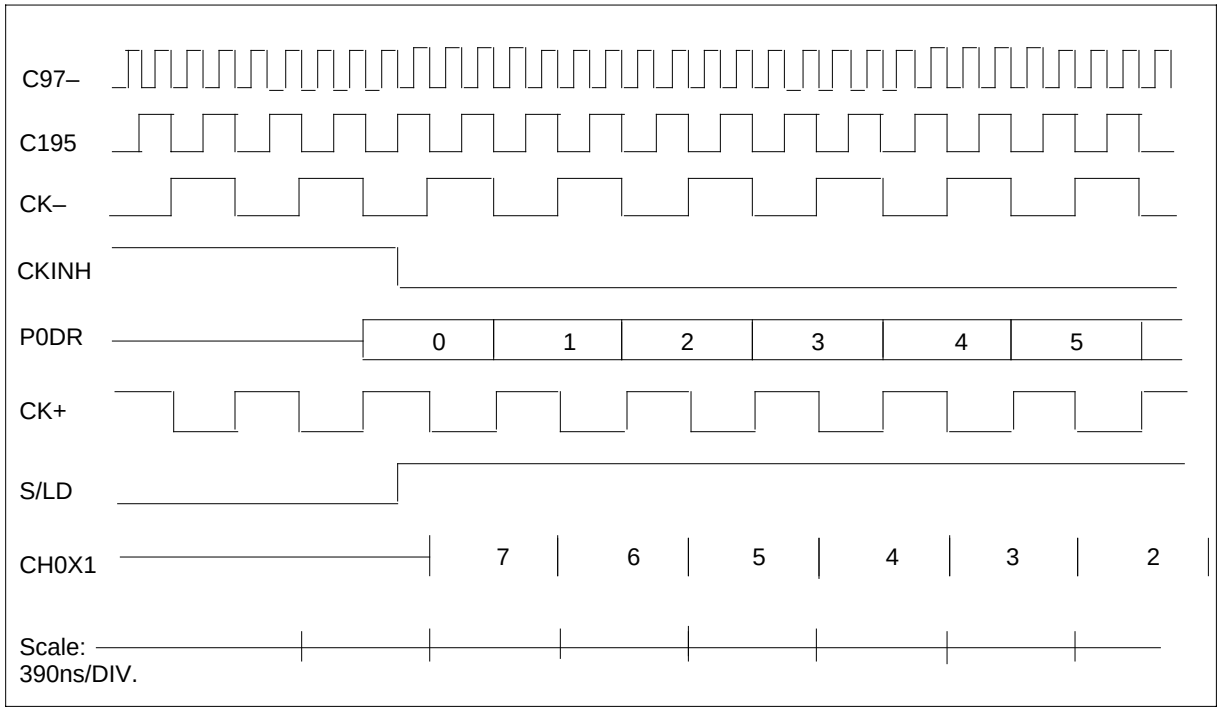


NT6X69LB A–bus interface timing: FP read cycle



NT6X69LB (end)

NT6X69LB network module interface timing



NT6X69MA

Product description

The NT6X69MA card is almost identical to the NT6X69AB in structure. The wait–for–start–of–message (WAM) timeout value and the wait–for–acknowledge (WACK) timeout values for the NT6X69MA and the NT6X69AB are different. The WAM and WACK timeout values for the NT6X69AB are 1 ms. The WAM and WACK timeout values for the NT6X69MA are 50 ms. This change makes the card compatible with the enhanced network (ENET).

The NT6X69AB (CPP message protocol and tone card) incorporates the functionality of the NT6X79AA (CPCE tone generator card) into the NT6X69AA (CPP message protocol card).

Location

The NT6X69MA is in slot 18 in a host XPM and slot 17 in an RCC.

Functional description

Functional blocks

The NT6X69MA consists of the following functional blocks:

- network message (NM) interface
- parallel speech bus (SB) message interface
- SB connection memory
- intermodule connection (IMC)
- tone generator and tone RAM
- protocol processor (PP)
- signaling processor (SP) and PP shared memory
- shelf reset generator
- cyclic redundancy check (CRC) ROM
- process timing ROM
- SP interface

Network message interface

Data leaves and enters the shift registers of the NM interface in series. The channel 0 (CH0) signal from the active formatter prescribes the data movement. Before the CH0 time in each frame, data from the transmit hold register is loaded into the shift register. Before the CH0 time, data from the shift register is loaded into the receive holding register from the shift register.

NT6X69MA (continued)

The PP can read from or write into the holding registers at any time. The PP cannot perform this action during CH0.

Parallel speech bus message interface

The synchronous PP in the SB interface sends the message. The first half of the instruction cycle is dedicated to the PP to write to the transmit RAM or read from the receive RAM. In the second half of the instruction cycle, the system latches data to the transmit holding register from the transmit RAM. This event occurs according to the port/channel counter. The PP writes to the receive RAM from the receive holding register.

Speech bus connection memory

The connection memory arbitrates the access of the different service cards to the SB by each time slot. The SP accesses the connection memory with the same method as the PP/SP shared memory. The PP does not have access to the connection memory.

Intermodule connection interface

The IMC interface provides a 64 Kbit/s link to the mate unit. This link appears to the PP as an SB time slot. The FP assigns the particular time slot through the connection memory. The exchange of data occurs between the two shelves during the active CH0 time. The active clock gates the exchange. Errors can occur with the IMC link when the two shelves are not in synchronization.

Tone generator and tone PROM

Tone generation circuits on the NT6X69MA card consist of the R09 tone generation chip and the tone PROM.

Protocol processor

The PP accesses the following functional blocks:

- 8K×8 RAM shared with the SP
- CRC ROM for CRC calculation that the DMS–X protocol requires
- process timing ROM, which allows the firmware to synchronize to the frame
- RSTGEN, which allows the PP to initiate a shelf reset (MODRST) from the NT6X46 card (signaling processor memory plus card)
- INTGEN, which allows the PP to initiate a level–four interrupt to the SP
- NM interface
- speech bus interface
- IMC interface

SP and PP shared memory

The SP and PP communicate through an 8K×8 block of RAM. The two processors share this block of RAM transparently. This block serves the following purposes:

- creates a work space for the PP
- provide a buffer for messages that the PP receives for the SP, and for messages that the SP queues for the PP
- provides an opcode area that allows the SP to apply the interfaces in an indirect method

Shelf reset generator

The PP initiates a shelf reset with the use of the following sequence:

1. The PP clocks the reset flip–flop when the PP accesses the auxiliary reset strobe.
2. The output of the reset flip–flop transmits to the backplane and connected to the 6X46 card.
3. The NT6X46 card acknowledges the reset when the card loses activity. The NT6X46 card issues the module reset signal to the rest of the shelf.
4. The module reset that the NT6X46 card issues clears the reset flip–flop on the NT6X69 card.

Cyclic redundancy check ROM

This ROM contains two tables. A two–stage CRC accumulation process uses these two tables. To access the upper page of the table, the PP must use the CRCL strobe followed by the CRCH strobe. To access the lower page, the PP must use the CRCL strobe.

Process timing ROM

Process timing ROM allows the PP to synchronize each process time slot to the frame boundary. The port/channel counter addresses the programmable read only memory (PROM). The PP can read the PROM during any instruction cycle.

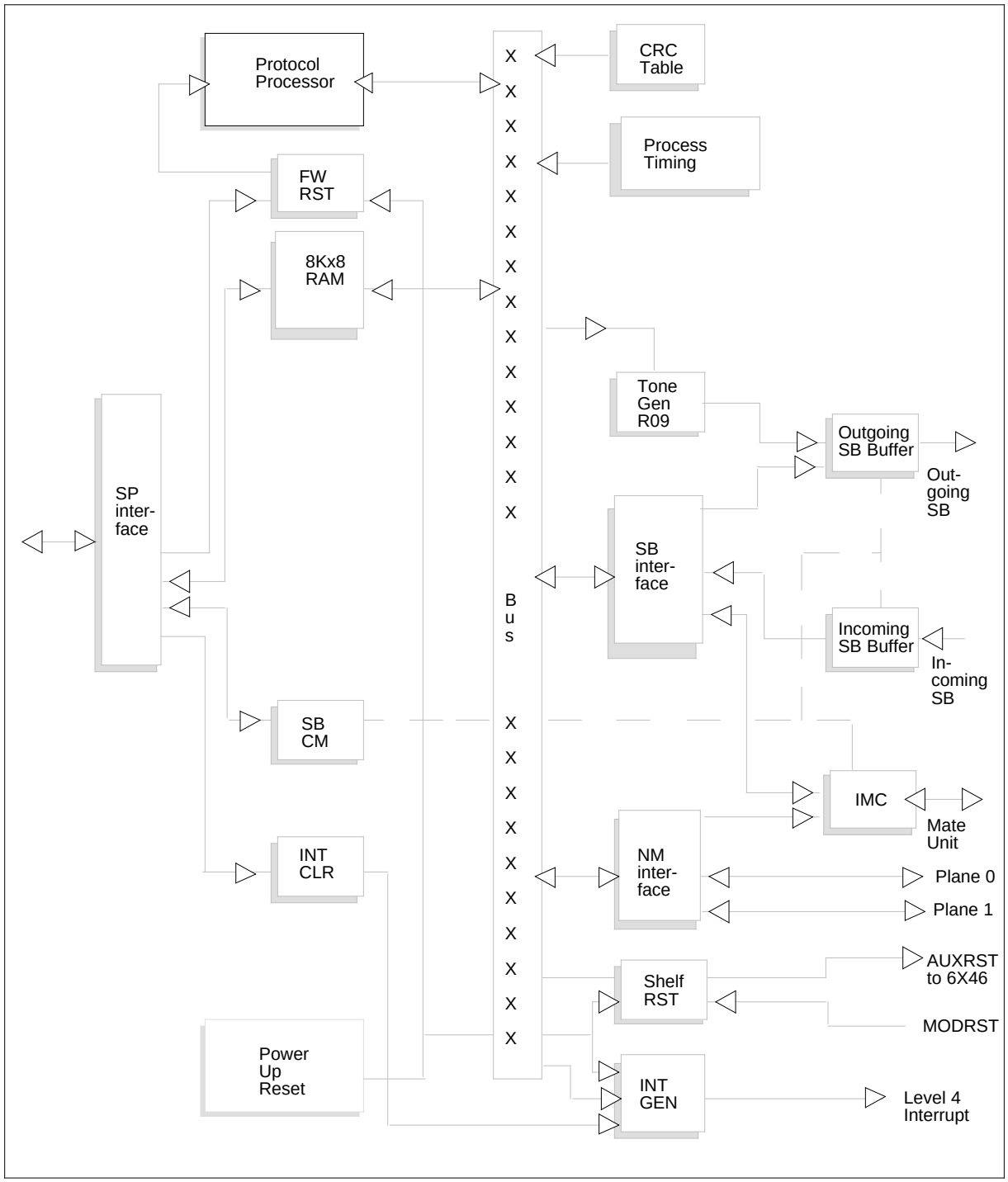
Signaling processor interface

All address and control signals are buffered. An access sequence synchronizes SP requests and generates a read or write access cycle. This event occurs when a valid address falls in the range assigned to this card type. The interface is asynchronous and an acknowledge signal indicates the end of the access cycle.

The relationship between the functional blocks appears in the following figure. A dashed line denotes the CM enable signal.

NT6X69MA (continued)

NT6X69MA functional blocks



Signaling

Pin numbers

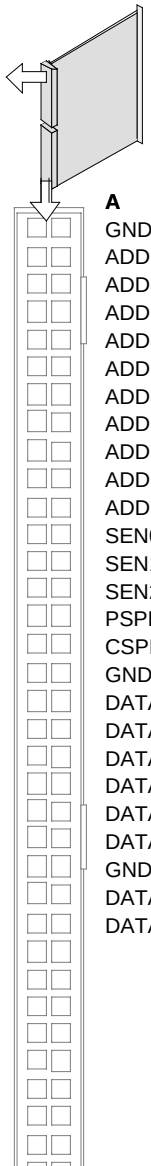
The pin numbers for NT6X69MA appear in the following figure.

Note: * denotes test channel signals, backplane connection not needed. ** denotes additional signals on the 6902 card but not on the 6901. *** denotes temporary signals required by the NT6X79 card.

NT6X69MA (continued)

NT6X69MA pin numbers

	A	B
1	GND	GND
2	5V	5V
3	5V	5V
4	5V	5V
5	GND	GND
6	FP-	C97T
7	GND	GND
8	-ACT	
9	C195TB*	
10	CPROCS-*	
11	GND	GND
12	DAS-	
13	LDS-	C97-B
14	DTACK-	CPROCB
15	UDS-	RUN*
16	WRT-	TCEN-*
17	IMCOUT**	
18	GND	INT4REQ**
19		
20		
21	PIN0	POUT0
22	PIN1	POUT1
23	PIN2	POUT2
24	PIN3	POUT3
25	PIN4	POUT4
26	PIN5	POUT5
27	PIN6	POUT6
28	PIN7	POUT7
29	ADDR01+	
30	ADDR02+	
31	ADDR03+	
32	ADDR04+	
33	ADDR05+	
34	GND	GND
35	ADDR06+	-FPM
36	ADDR07+	GND
37	ADDR08+	C97M+
38	ADDR09+	GND
39	ADDR10+	CH0T
40	ADDR11+	CH0M

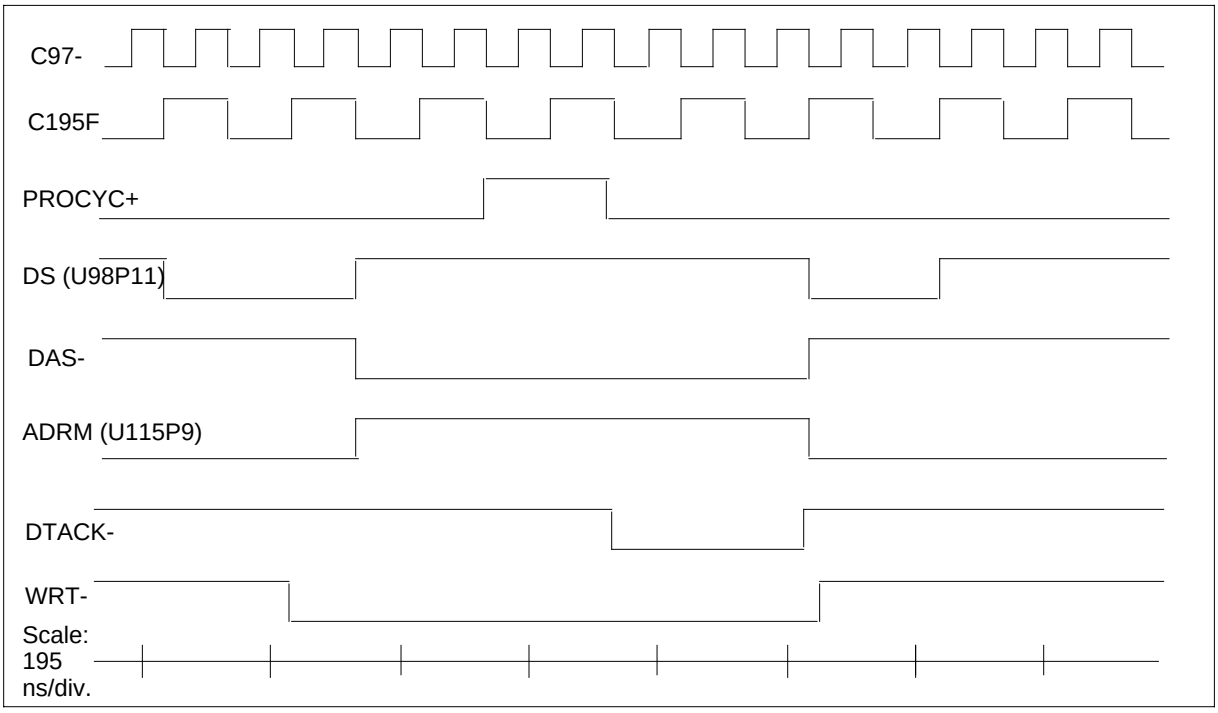


	A	B
41	GND	GND
42	ADDR12+	
43	ADDR13+	D0*
44	ADDR14+	D1*
45	ADDR15+	D2*
46	ADDR16+	D3*
47	ADDR17+	D4*
48	ADDR18+	D5*
49	ADDR19+	D6*
50	ADDR20+	D7*
51	ADDR21+	
52	SEN0	DESTXT0-
53	SEN1	DESTXT1-
54	SEN2	
55	PSPEN+	SRCXT0-
56	CSPEN+	SRCXT1-
57	GND	GND
58	DATA00+	SRC0*
59	DATA01+	SRC1*
60	DATA02+	SRC2*
61	DATA03+	SRC3*
62	DATA04+	SRC4*
63	DATA05+	SRC5*
64	GND	SRC6*
65	DATA06+	SRC7*
66	DATA07+	
67		CH0S0
68		CH0R0
69		CH0S1
70		CHOR1
71		(T1***)
72		(T2***)
73		(T3***)
74		AUXRST-**
75		MODRST-**
76	GND	GND
77		
78	GND	GND
79		
80	GND	GND

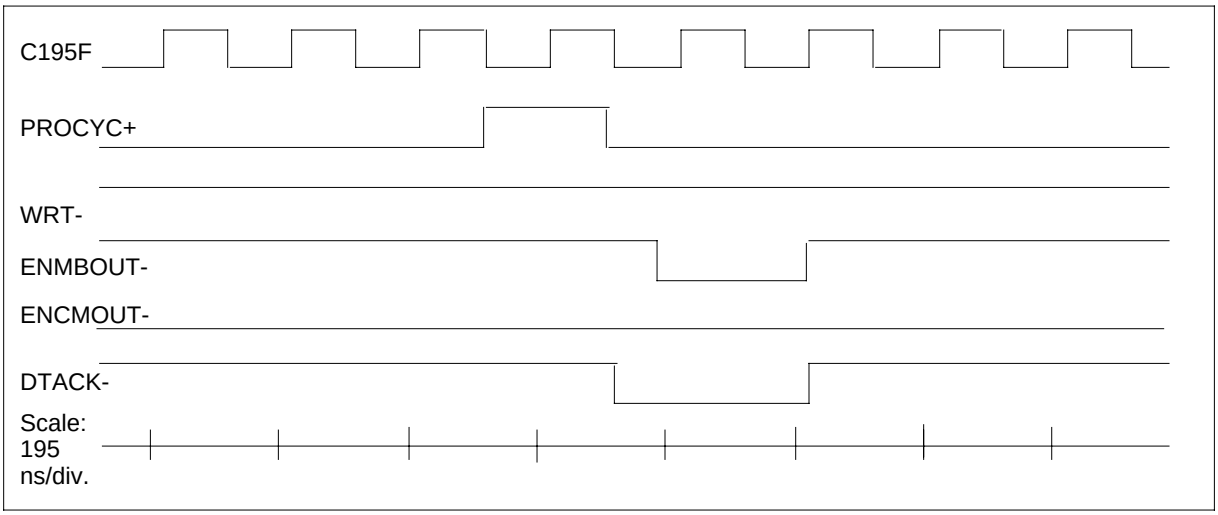
Timing

The timing for the NT6X69MA appears in the following figures.

NT6X69MA A–bus interface timing: SP write cycle

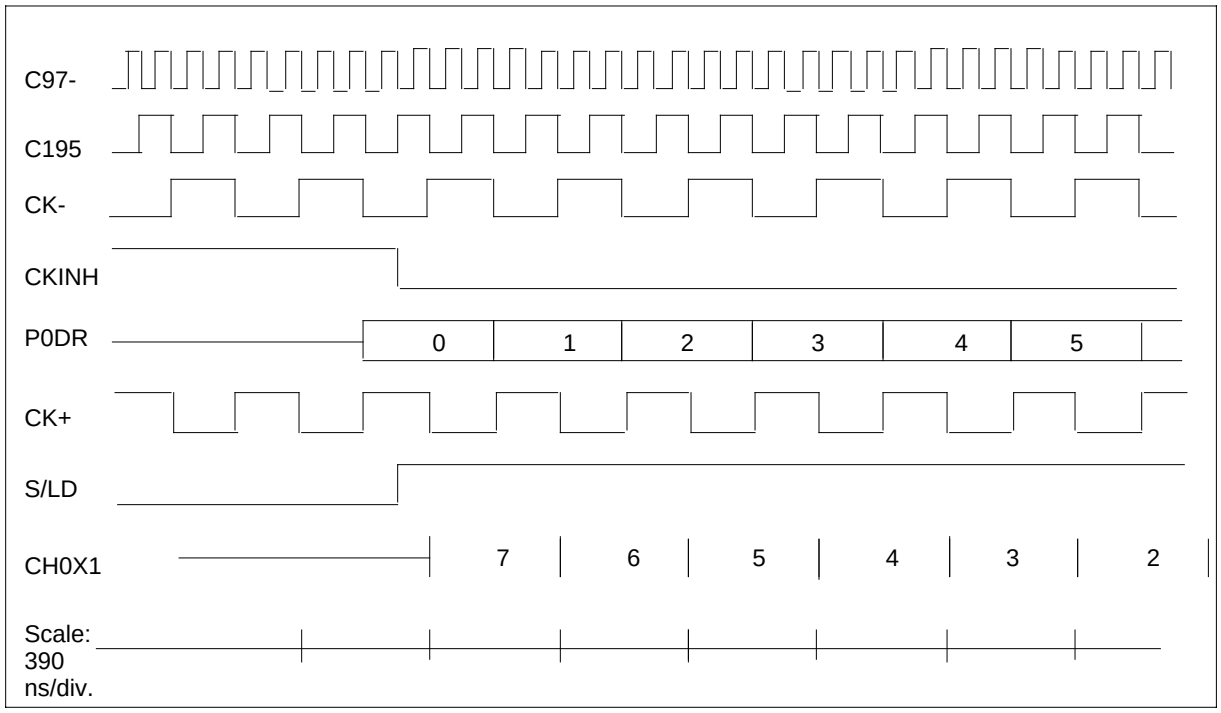


NT6X69MA A–bus interface timing: SP read cycle



NT6X69MA (end)

NT6X69MA network module interface timing



NT6X69QA

Product description

The NT6X69QA card is almost identical to the NT6X69AB in structure. The wait–for–start–of–message (WAM) timeout value and the wait–for–acknowledge (WACK) timeout values for the NT6X69QA and the NT6X69AB are different. The WAM and WACK timeout values for the NT6X69AB are 1 ms. The WAM and WACK timeout values for the NT6X69QA are 50 ms. This change makes the card compatible with the enhanced network (ENET).

The NT6X69AB (CPP message protocol and tone card) incorporates the functionality of the NT6X79AA (CPCE tone generator card) into the NT6X69AA (CPP message protocol card).

Location

The NT6X69QA is in slot 18 in a host XPM and slot 17 in an RCC.

Functional description

Functional blocks

The NT6X69QA consists of the following functional blocks:

- network message (NM) interface
- parallel speech bus (SB) message interface
- SB connection memory
- intermodule connection (IMC)
- tone generator and tone RAM
- protocol processor (PP)
- signaling processor (SP) and PP shared memory
- shelf reset generator
- cyclic redundancy check (CRC) ROM
- process timing ROM
- SP interface

Network message interface

Data leaves and enters the shift registers of the NM interface in series. The channel 0 (CH0) signal from the active formatter prescribes the data movement. Before the CH0 time in each frame, data from the transmit hold register is loaded into the shift register. Before the CH0 time, data from the shift register is loaded into the receive holding register from the shift register.

NT6X69QA (continued)

The PP can read from or write into the holding registers at any time. The PP cannot perform this action during CH0.

Parallel speech bus message interface

The synchronous PP in the SB interface sends the message. The first half of the instruction cycle is dedicated to the PP to write to the transmit RAM or read from the receive RAM. In the second half of the instruction cycle, the system latches data to the transmit holding register from the transmit RAM. This event occurs according to the port/channel counter. The PP writes to the receive RAM from the receive holding register.

Speech bus connection memory

The connection memory arbitrates the access of the different service cards to the SB by each time slot. The SP accesses the connection memory with the same method as the PP/SP shared memory. The PP does not have access to the connection memory.

Intermodule connection interface

The IMC interface provides a 64 Kbit/s link to the mate unit. This link appears to the PP as an SB time slot. The FP assigns the particular time slot through the connection memory. The exchange of data occurs between the two shelves during the active CH0 time. The active clock gates the exchange. Errors can occur with the IMC link when the two shelves are not in synchronization.

Tone generator and tone PROM

Tone generation circuits on the NT6X69QA card consist of the R09 tone generation chip and the tone PROM.

Protocol processor

The PP accesses the following functional blocks:

- 8K×8 RAM shared with the SP
- CRC ROM for CRC calculation that the DMS–X protocol requires
- process timing ROM, which allows the firmware to synchronize to the frame
- RSTGEN, which allows the PP to initiate a shelf reset (MODRST) from the NT6X46 card (signaling processor memory plus card)
- INTGEN, which allows the PP to initiate a level–four interrupt to the SP
- NM interface
- speech bus interface
- IMC interface

SP and PP shared memory

The SP and PP communicate through an 8K×8 block of RAM. The two processors share this block of RAM transparently. This block serves the following purposes:

- creates a work space for the PP
- provide a buffer for messages that the PP receives for the SP, and for messages that the SP queues for the PP
- provides an opcode area that allows the SP to apply the interfaces in an indirect method

Shelf reset generator

The PP initiates a shelf reset with the use of the following sequence:

1. The PP clocks the reset flip–flop when the PP accesses the auxiliary reset strobe.
2. The output of the reset flip–flop transmits to the backplane and connected to the 6X46 card.
3. The NT6X46 card acknowledges the reset when the card loses activity. The NT6X46 card issues the module reset signal to the rest of the shelf.
4. The module reset that the NT6X46 card issues clears the reset flip–flop on the NT6X69 card.

Cyclic redundancy check ROM

This ROM contains two tables. A two–stage CRC accumulation process uses these two tables. To access the upper page of the table, the PP must use the CRCL strobe followed by the CRCH strobe. To access the lower page, the PP must use the CRCL strobe.

Process timing ROM

Process timing ROM allows the PP to synchronize each process time slot to the frame boundary. The port/channel counter addresses the programmable read only memory (PROM). The PP can read the PROM during any instruction cycle.

Signaling processor interface

All address and control signals are buffered. An access sequence synchronizes SP requests and generates a read or write access cycle. This event occurs when a valid address falls in the range assigned to this card type. The interface is asynchronous and an acknowledge signal indicates the end of the access cycle.

NT6X69QA (continued)

Signaling

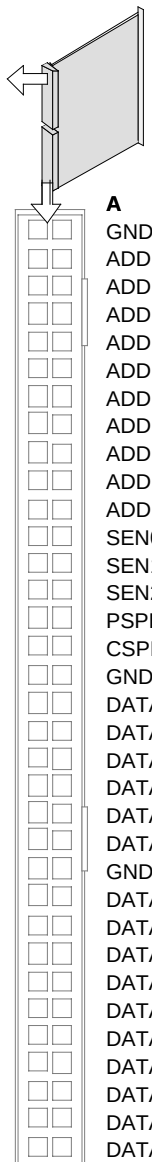
Pin numbers

The pin numbers for NT6X69QA appear in the following figure.

Note: * denotes signals defined in previous versions of the NT6X69, but are no longer required. ** denotes signals defined in NT6X69AA versions that were configured with NT6X79 circuit packs. *** denotes signals that are not used on the NT6X69QA, but are defined on the backplane at the slot occupied by the NT6X69QA in either an XPM or an RSCS (CPM).

NT6X69QA pin numbers

	A	B
1	GND	GND
2	5V	5V
3	5V	5V
4	5V	5V
5	GND	GND
6	FP–	C97T
7	GND	GND
8	–ACT	
9	C195TB*	FP40–/i***
10	CPROCS–*	
11	GND	GND
12	DAS–	PERINT3–***
13	LDS–	C97–B*
14	DTACK–	CPROCB*
15	UDS–	RUN*
16	RDWRT–	TADDR
17	IMCTX	IMCRX
18	GND	INT4REQ–
19	PINA***	POUTA***
20	PINB***	POUTB***
21	PIN0	POUT0
22	PIN1	POUT1
23	PIN2	POUT2
24	PIN3	POUT3
25	PIN4	POUT4
26	PIN5	POUT5
27	PIN6	POUT6
28	PIN7	POUT7
29	ADDR01	CMSGOUT0***
30	ADDR02	CMSGIN0***
31	ADDR03	CMSGOUT2***
32	ADDR04	CMSGIN2***
33	ADDR05	–HOST/REM***
34	GND	GND
35	ADDR06	–FPM
36	ADDR07	GND
37	ADDR08	C97M+
38	ADDR09	GND
39	ADDR10	CH0TIN
40	ADDR11	CH0MIN



	A	B
41	GND	GND
42	ADDR12	
43	ADDR13	DEST00
44	ADDR14	DEST01
45	ADDR15	DEST02
46	ADDR16	DEST03
47	ADDR17	DEST04
48	ADDR18	DEST05
49	ADDR19	DEST06
50	ADDR20	DEST07
51	ADDR21	
52	SEN0	DESTXT0
53	SEN1	DESTXT1
54	SEN2	
55	PSPEN+	SRCXT0–*
56	CSPEN+	SRCXT1–*
57	GND	GND
58	DATA00	SRC0*
59	DATA01	SRC1*
60	DATA02	SRC2*
61	DATA03	SRC3*
62	DATA04	SRC4*
63	DATA05	SRC5*
64	GND	SRC6*
65	DATA06	SRC7*
66	DATA07	
67	DATA08	CH0S0
68	DATA09	CH0R0
69	DATA10	CH0S1
70	DATA11	CH0R1
71	DATA12	T1**
72	DATA13	T2**
73	DATA14	T3**
74	DATA15	MODRST–
75		AUXRST–
76	GND	GND
77	+12***	+12***
78	GND	GND
79	–12***	–12***
80	GND	GND

NT6X70AA

Product description

The NT6X70AA continuity tone detector (CTD) card verifies the continuity of the voice/data path between digital trunk controllers (DTC). To verify the continuity, the NT6X70AA detects tones in the common channel interoffice signaling (CCIS) call process.

Location

The NT6X70AA occupies one position in a DTC.

Functional description

The NT6X70AA monitors the 32 channels of port 16 on the incoming 8–bit parallel data bus and records tone frequency and level. The NT6X70AA stores this data for use by the DTC signaling processor (SP). The NT6X70AA monitors the channels continuously between the time switch (TS) to the network interfaces in the DTC.

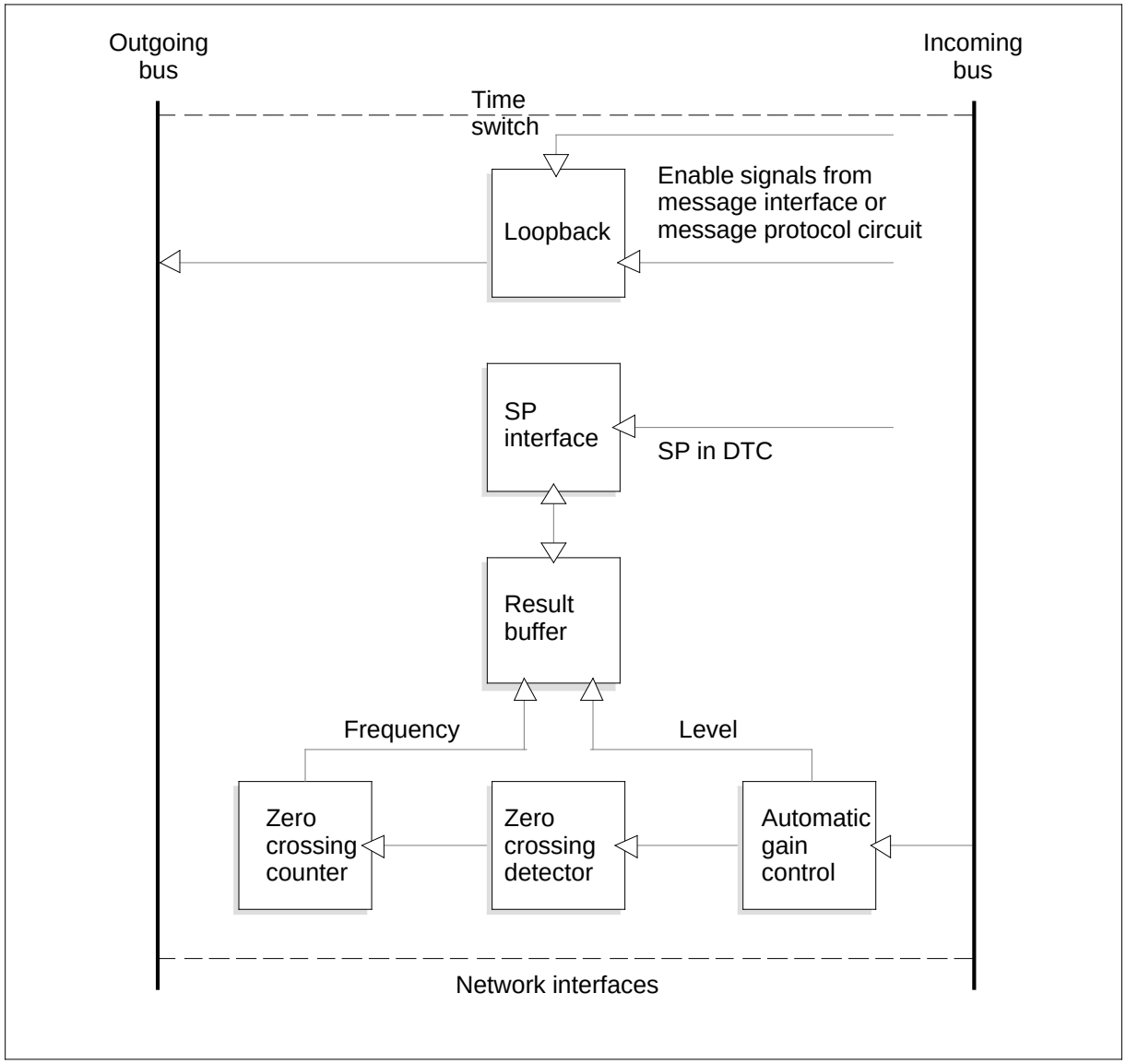
Functional blocks

The NT6X70AA consists of the following functional blocks:

- automatic gain control (AGC)
- zero crossing detector
- zero crossing counter
- result buffer

- signaling processor (SP)
- loopback feature

NT6X70AA functional blocks



AGC

The AGC receives a continuity tone from a far end DTC and measures each channel tone. To measure each channel tone, the AGC compares the tone with a table of upper and lower values. The AGC stores the measured level in the result buffer.

NT6X70AA (continued)

Zero crossing detector

The zero crossing detector sends a signal to the zero crossing counter when a single–frequency tone passes zero amplitude.

Zero crossing counter

The zero crossing counter measures the frequency of the tone. To measure the frequency of the tone, the zero crossing counter counts the number of zero crossing events during each channel time. The zero crossing counter stores the count in the result buffer.

Result buffer

The result buffer stores the tone level and the frequency data. The result buffer is accessible through the SP. The buffer is updated at intervals of 10 ms for all channels.

Signaling processor

The SP checks the tone level and the frequency data. When the tone level and the frequency data are correct, the CCIS call sequence proceeds. The SP initiates recovery or maintenance action in the DTC when the data is not present or is not correct.

Loopback feature

The loopback feature performs testing. This feature loops any channel on the incoming bus back to the TS to perform testing. The loopback feature uses of the outgoing 8–bit parallel data bus. Enable signals select and activate the loopback for a specific channel. These enable signals occur from the NT6X43 message interface circuit in the DTC or from the NT6X69 message protocol circuit

Technical data

Tones transmitted

Tones that transmit from the far–end DTC appear in the following table.

Tones transmitted

Frequency	Level
2010 $\pm$ 8 Hz	- 12 $\pm$ 1 dBm0
2010 $\pm$ 8 Hz	- 15 $\pm$ 1 dBm0
1780 $\pm$ 8 Hz	- 12 $\pm$ 1 dBm0
1780 $\pm$ 8 Hz	- 15 $\pm$ 1 dBm0

Tone detector range

A list of the tone detector range appears in the following table.

Tone detector range

	Frequency	Level (dBm0)
Operate	2010 ± 30 Hz	- 18.0
	1780 ±30 Hz	- 19.5
		- 21.2
		- 23.0
		- 25.0
		- 29.0
Non–operate	2010 ± 200 Hz	- 22.0
	1780 ±200 Hz	- 23.5
		- 25.2
		- 27.0
		- 29.0
		- 33.0
Note: The type of trunk determines the required operate/non-operate levels.		

Physical dimensions

The physical dimensions of the NT6X70AA card follow:

- overall height: 353 mm (13.9 in.)
- overall depth: 277 mm (10.9 in.)
- overall width: 20 mm (.78 in.)

Power requirements

The power requirements are from the NT2X70 power converter in the DTC. The power requirements for the NT6X70AA are a voltage of +5V and current of 2 A.

NT6X70CA

Product description

The NT6X70AA continuity tone detector (CTD) card verifies the continuity of the voice/data path between digital trunk controllers (DTC). To verify the continuity, the NT6X70AA detects tones in the common channel interoffice signaling (CCIS) call process.

The NT6X70CA provides the same functionality as the NT6X70AA but incorporates an electrical modification to reduce noise within the DTC02 shelf.

Location

The NT6X70CA occupies one position in a DTC.

Functional description

The NT6X70CA is functionally identical to the NT6X70AA. It monitors the 32 channels of port 16 on the incoming 8–bit parallel data bus and records tone frequency and level. The NT6X70CA stores this data for use by the DTC signaling processor (SP) and monitors the channels continuously between the time switch (TS) to the network interfaces in the DTC. The NT6X70CA incorporates an electrical modification which reduces shelf noise within the DTC02 shelf.

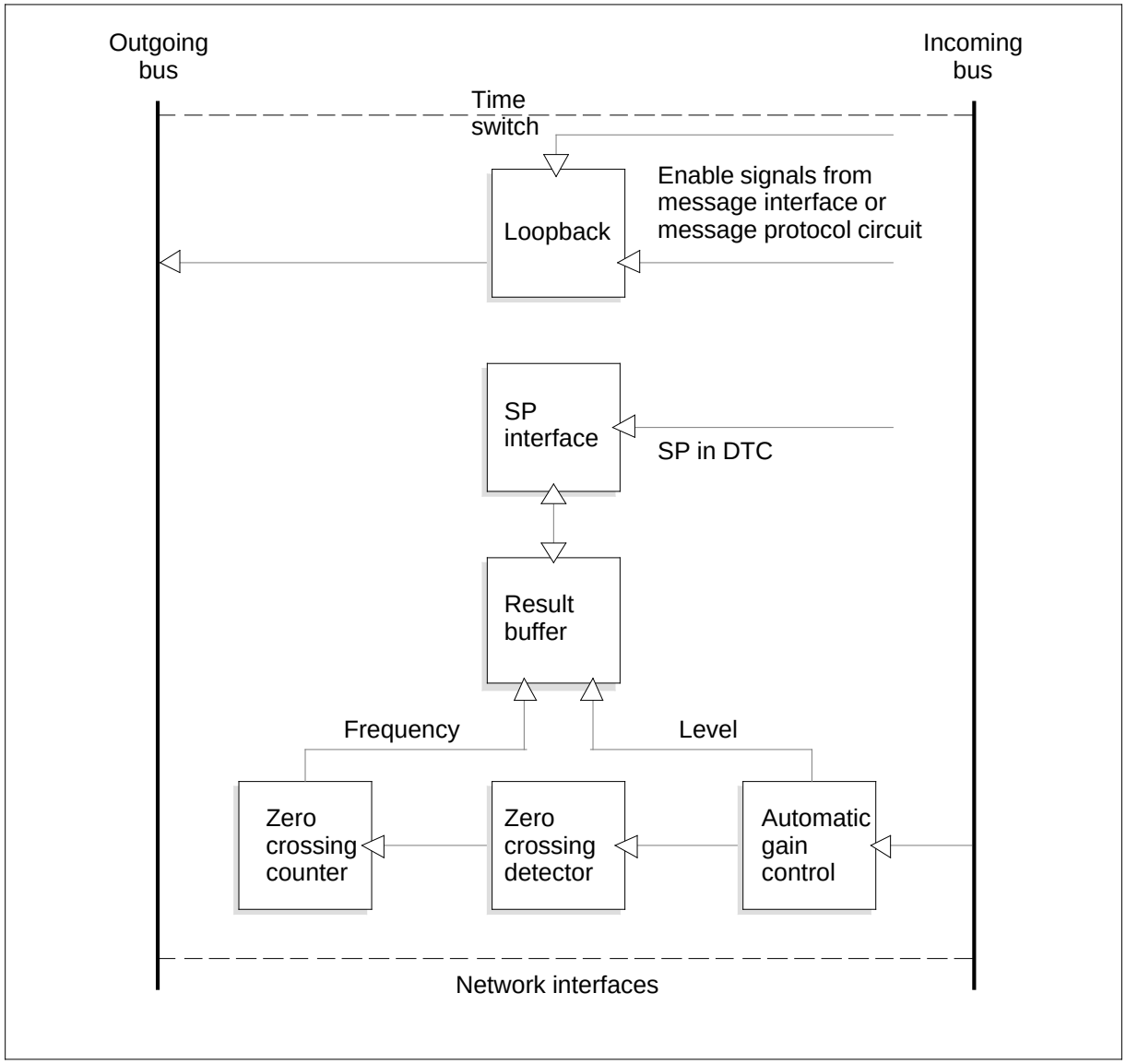
Functional blocks

The NT6X70CA is identical to the NT6X70AA from a functional block diagram perspective. The NT6X70CA consists of the following functional blocks:

- automatic gain control (AGC)
- zero crossing detector
- zero crossing counter
- result buffer

- signaling processor (SP)
- loopback feature

NT6X70CA functional blocks



AGC

The AGC receives a continuity tone from a far end DTC and measures each channel tone. To measure each channel tone, the AGC compares the tone with a table of upper and lower values. The AGC stores the measured level in the result buffer.

NT6X70CA (continued)

Zero crossing detector

The zero crossing detector sends a signal to the zero crossing counter when a single–frequency tone passes zero amplitude.

Zero crossing counter

The zero crossing counter measures the frequency of the tone. To measure the frequency of the tone, the zero crossing counter counts the number of zero crossing events during each channel time. The zero crossing counter stores the count in the result buffer.

Result buffer

The result buffer stores the tone level and the frequency data. The result buffer is accessible through the SP. The buffer is updated at intervals of 10 ms for all channels.

Signaling processor

The SP checks the tone level and the frequency data. When the tone level and the frequency data are correct, the CCIS call sequence proceeds. The SP initiates recovery or maintenance action in the DTC when the data is not present or is not correct.

Loopback feature

The loopback feature performs testing. This feature loops any channel on the incoming bus back to the TS to perform testing. The loopback feature uses of the outgoing 8–bit parallel data bus. Enable signals select and activate the loopback for a specific channel. These enable signals occur from the NT6X43 message interface circuit in the DTC or from the NT6X69 message protocol circuit

Technical data

Tones transmitted

Tones that transmit from the far–end DTC appear in the following table.

Tones transmitted

Frequency	Level
2010 $\pm$ 8 Hz	- 12 $\pm$ 1 dBm0
2010 $\pm$ 8 Hz	- 15 $\pm$ 1 dBm0
1780 $\pm$ 8 Hz	- 12 $\pm$ 1 dBm0
1780 $\pm$ 8 Hz	- 15 $\pm$ 1 dBm0

Tone detector range

A list of the tone detector range appears in the following table.

Tone detector range

	Frequency	Level (dBm0)
Operate	2010 ± 30 Hz	- 18.0
	1780 ±30 Hz	- 19.5
		- 21.2
		- 23.0
		- 25.0
		- 29.0
Non–operate	2010 ± 200 Hz	- 22.0
	1780 ±200 Hz	- 23.5
		- 25.2
		- 27.0
		- 29.0
		- 33.0
Note: The type of trunk determines the required operate/non-operate levels.		

Physical dimensions

The physical dimensions of the NT6X70CA card follow:

- overall height: 353 mm (13.9 in.)
- overall depth: 277 mm (10.9 in.)
- overall width: 20 mm (.78 in.)

Power requirements

The power requirements are from the NT2X70 power converter in the DTC. The power requirements for the NT6X70CA are a voltage of +5V and current of 2A.

NT6X71AA

Product description

The NT6X71AA data line card (DLC) DMS–100/SL–100 provides an interface. The interface is between the two–wire loop from a data unit (DU) and one channel of the four–wire, 32–channel, 2.5Mbit/s digital bit stream of the DMS–100 or SL–100.

Location

The card occupies two line circuit (LC) card positions in a line concentrating module (LCM) drawer. One 64–position LCM drawer can support a maximum of 32 cards.

Functional description

The card uses a bidirectional bus and an enable signal to transfer messages between the LCM and the DU. Clock signals provide timing for the data transmission. Clock signals provide synchronization of time compression multiplex (TCM) frames on all data lines in the LCM drawer.

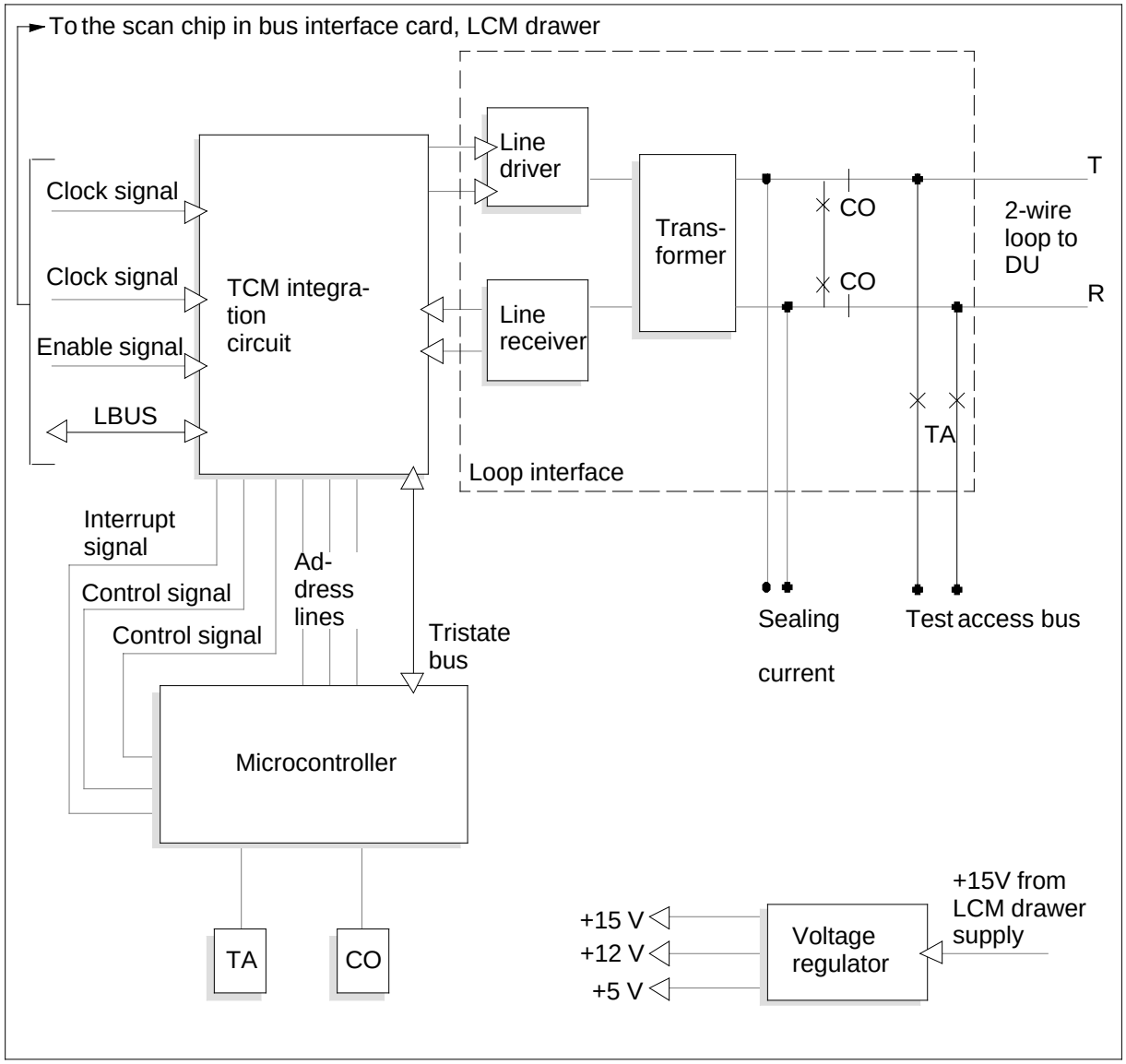
Functional blocks

The NT6X71AA card consists of the following functional blocks:

- TCM integration circuit
- line driver
- line receiver
- transformer
- microcontroller

- relays
- voltage regulator

NT6X71AA functional blocks



TCM integration circuit

The TCM integration circuit uses a bidirectional bus and an enable signal to perform data conversion between the LCM and the loop interface. A clock signal provides 1–kHz pulses. The pulses synchronize the 1–ms TCM frames on all data lines in the LCM drawer.

NT6X71AA (continued)

In the transmit direction, the circuit receives data from the LCM and transmits this data to the loop interface circuit. This transmission occurs at a rate of 160 Kbit/s. In the receive direction, the circuit receives data from the loop and transmits the data to the LCM. This transmission occurs with the use of a 64 Kbit/s interface. A clock signal provides the 160–kHz and 2.56–MHz clock pulses required for data recovery.

Line driver

The line driver converts unipolar, transistor–transistor logic (TTL) signals. The line driver converts these signals into an alternate mark inversion (AMI) bipolar, return–to–zero, 50% modulated signal for transmission to the loop.

Line receiver

The line receiver recovers data from the bipolar signal received over the two–wire metallic loop. The line receiver equalizes for loop losses that range from 0 through 45 dB m at 80 kHz. The circuit compensates for bridged taps and provides filtering to reduce the effects of impulse and random noise.

Transformer

The transformer provides an interface between the line driver and the line receiver in the card and the DU. In the transmit direction, the transformer receives the signal from the transmit circuit. The transformer sends the converted signals over the tip (T) and ring (R) leads. In the receive direction, the transformer converts the signals on the T and R leads to one signal. The receive circuit processes these signals.

The transformer contains a balancing network to provide line balancing.

Microcontroller

The microcontroller performs reset functions and implements the communications protocol. The two reset functions are the power–up reset and the LCM reset. The reset functions can perform the following functions:

- clear all messages, controls and loopbacks
- stop autonomous synchronization reporting
- select automatic bipolar violation (BPV) reporting

The circuit uses an interrupt signal, two control signals, and three address lines to control read and write pulses. The circuit reads and writes these pulses to the TCM integration circuit and the external memory. The circuit controls messages between the loop, LCM and microcontroller with the use of a parallel 8–bit, bidirectional tristate bus.

Relays

Two relays are present for maintenance purposes. A list of the relays and relay operated and released functions appear in the following table.

Relay operation

Relay	Operated	Released
CO	Allows a complete integrity check of the DLC using DLC–to–loop isolation and analog loopback	Normal operation
TA	Connects the loop to the system test access bus	Normal operation

Voltage regulator

The voltage regulator receives a +15V power supply from the LCM drawer. The voltage regulator regulates this voltage to provide +12V and +5V power to the card.

Technical data

The microcontroller contains the following parts:

- an 80C39 microprocessor with an address latch and internal RAM
- a memory circuit with 2–Kbyte EPROM and 256 bytes RAM
- a 2.5 µs instruction cycle time

A list of the LCM interface characteristics appears in the following table.

LCM interface characteristics (Sheet 1 of 2)

Characteristic	Value
Clock signal	2.56 MHz
Synchronization signal	1 kHz, synchronizes the 1–ms TCM frames on all data lines in an LCM drawer

NT6X71AA (continued)

LCM interface characteristics (Sheet 2 of 2)

Characteristic	Value
Enable signal	0 selects intelligent functions, 1 selects plain ordinary telephone service (POTS) functions
Bidirectional bus	2.56 Mbit/s, transfers 10 bits of bidirectional data out of a complete transaction of 20.5 bits. The structure is as follows: • 1 start bit • 1 mode bit, 0 = data, 1 = signaling • 8 transmit data bits • half bit, delay for bus reversal • 8 receive data bits • 2 supervision bits

A list of the loop interface characteristics appears in the following table.

Loop interface characteristics

Characteristic	Value
Transmission type	Full duplex TCM
Frame rate	1 kHz
Data rate	160 Kbit/s
Frame structure	Transmit and receive, each with the following: • 1 start bit • 8 signaling bits • 64 data bits • 1 stop bit
Transmission distance	5.4 km maximum with a maximum loss of 45 dB at 80 kHz

Dimensions

The dimensions of the NT6X71AA card follow:

- overall height: 152 mm (6 in.)
- overall depth: 89 mm (3.5 in.)
- overall width: 20 mm (0.8 in.)

Power requirements

The power requirements for the NT6X71AA appear in the following table.

Power requirements

Voltage	Current
+15V	46 mA
-48V	6 mA
+12.7V	0.5 mA

NT6X71AB

Product description

The NT6X71AB data line card (DLC) provides an interface. The interface occurs between the two-wire loop from a data unit (DU) and one channel of the four-wire, 32-channel, 2.5 Mbit/s digital bit stream of the DMS-100 or SL-100.

The card provides profile downloading to override some user-option switch settings in the DU. Profile downloading activates or deactivates DU features not directly under user control.

Location

The card occupies two line circuit (LC) card positions in a line concentrating module (LCM) drawer. One 64-position LCM drawer can support a maximum of 32 cards.

Functional description

The NT6X71AB card uses a bidirectional bus and an enable signal to transfer messages between the LCM and the DU. Clock signals provide timing for the data transmission. Clock signals provide synchronization of time compression multiplex (TCM) frames on all data lines in the LCM drawer. A profile downloading feature in the microcontroller enables the switching system to control the operating parameters of the DU. The switching system controls these parameters with the use of the LCM and DLC.

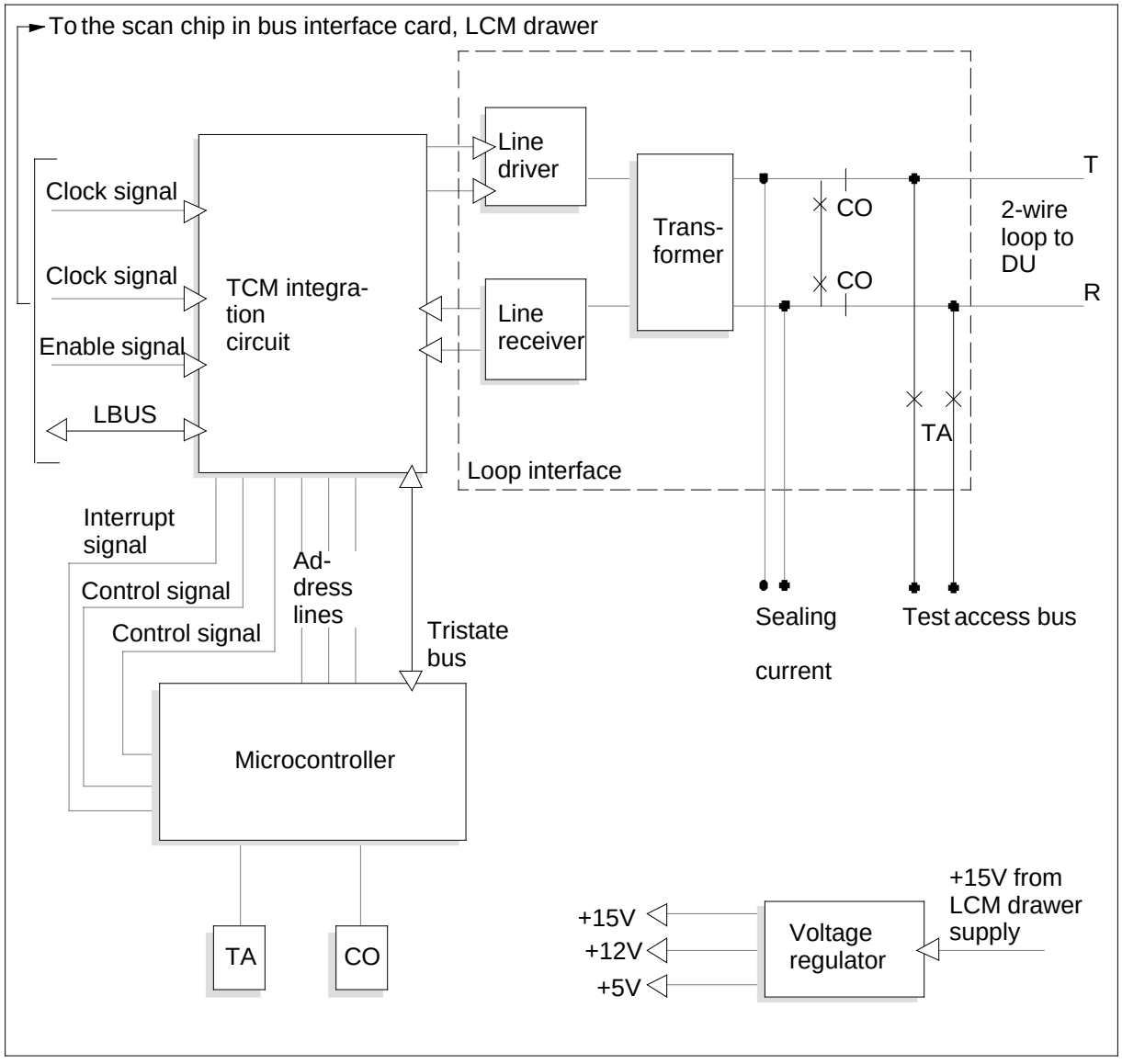
Functional blocks

The NT6X71AB card consists of the following functional blocks:

- TCM integration circuit
- line driver
- line receiver
- transformer
- microcontroller

- relays
- voltage regulator

NT6X71AB functional blocks



TCM integration circuit

The TCM integration circuit uses a bidirectional bus and an enable signal to perform data conversion. The data conversion occurs between the LCM and the loop interface. A clock signal provides 1-kHz pulses to synchronize the 1-ms TCM frames on all data lines in the LCM drawer.

NT6X71AB (continued)

In the transmit direction, the circuit receives data from the LCM and transmits this data to the loop interface circuit. The transmission occurs at a rate of 160 Kbit/s. In the receive direction, the circuit receives data from the loop and transmits the data to the LCM. The data transmission occurs with the use of a 64-Kbit/s interface. A clock signal provides the 160-kHz and 2.56-MHz clock pulses required for data recovery.

Line driver

The line driver converts unipolar, transistor-transistor logic (TTL) signals. The line driver converts these signals into an alternate mark inversion (AMI) bipolar, return-to-zero, 50% modulated signal for transmission to the loop.

Line receiver

The line receiver recovers data from the bipolar signal received over the two-wire metallic loop. The line receiver equalizes for loop losses that range from 0 through 45 dBm at 80 kHz. The circuit compensates for bridged taps and provides filters to reduce the effects of impulse and random noise.

Transformer

The transformer provides an interface between the line driver and the line receiver in the card and the DU. In the transmit direction, the transformer receives the signal from the transmit circuit. The transformer sends the converted signals over the tip (T) and ring (R) leads. In the receive direction, the transformer converts the signals on the T and R leads to one signal. The receive circuit processes this signal.

The transformer contains a balancing network to provide line balancing.

Microcontroller

The microcontroller performs reset functions and implements the communications protocol. The two reset funtions are the power-up reset and the LCM reset. The reset functions can perform the following functions:

- clear all messages, controls, and loopbacks
- stop autonomous synchronization reporting
- select automatic bipolar violation (BPV) reporting

The circuit uses an interrupt signal, two control signals, and three address lines to control read and write pulses. The circuit reads and writes these signals to the TCM integration circuit and the external memory. The circuit controls messages between the loop, LCM and microcontroller. To control the messages, the circuit control uses a parallel 8-bit, bidirectional, tristate bus.

The EPROM of the microcontroller contains improved firmware to provide profile download, incoming message control and self-test functions. The profile download function enables the switching system to control the operating parameters of the DU. The profile download refreshes the DU memory during synchronization after a power outage.

The incoming message control feature controls the flow of messages from the DLC to the switching system. The incoming message control controls the self-test feature that checks the operation of the microcontroller RAM and EPROM.

Relays

Two relays are present for maintenance purposes. A list of the relays and the relay operated and released functions appears in the the following table.

Relay operation

Relay	Operated	Released
CO	Allows a complete integrity check of the DLC with the use of DLC-to-loop isolation and analog loopback.	Normal operation
TA	Connects the loop to the system test access bus.	Normal operation

Voltage regulator

The voltage regulator receives a +15V power supply from the LCM drawer. The voltage regulator regulates this voltage to provide +12V and +5V power in the card.

Technical data

The microcontroller contains the following parts:

- an 80C39 microprocessor with an address latch and internal RAM
- a memory circuit with a 2-kbyte EPROM and 256 bytes RAM
- a 2.5 µs instruction cycle time

NT6X71AB (continued)

A list of the LCM interface characteristics appears in the following table.

LCM interface characteristics

Characteristic	Value
Clock signal	2.56 MHz
Synchronization signal	1 kHz, Synchronizes the 1 ms TCM frames on all data lines in an LCM drawer.
Enable signal	0 selects intelligent functions, 1 selects plain ordinary telephone service (POTS) functions
Bidirectional bus	2.56 Mbps, Transfers 10 bits of bidirectional data out of a complete transaction of 20.5 bits. The structure is as follows: • 1 start bit • 1 mode bit, 0 = data, 1 = signaling • 8 transmit data bits • 1/2 bit, delay for bus reversal • 8 receive data bits • 2 supervision bits

A list of the loop interface characteristics appears in the following table.

Loop interface characteristics (Sheet 1 of 2)

Characteristic	Value
Transmission type	Full duplex TCM
Frame rate	1 kHz
Data rate	160 kbits/s

Loop interface characteristics (Sheet 2 of 2)

Characteristic	Value
Frame structure	Transmit and receive, each with the following: • 1 start bit • 8 signaling bits • 64 data bits • 1 stop bit
Transmission distance	5.4 km maximum with a maximum loss of 45 dB at 80 kHz

Dimensions

The physical dimensions of the NT6X71AB card follow:

- overall height: 152 mm (6 in.)
- overall depth: 89 mm (3.5 in.)
- overall width: 20 mm (0.8 in.)

Power requirements

The power requirements for the NT6X71AB appear in the following table.

Power requirements

Voltage	Current
+15V	46 mA
-48V	6 mA
+12.7V	0.5 mA

NT6X71AC

Product description

The data line card (DLC) forms part of a data facility like the Datapath. The DLC provides circuit–switched data on the DMS/SL–100 families of DMS. The DLC interfaces data units through a two–wire subscriber loop to the DMS/SL–100 switch. Examples of data units include coax eliminators and low-speed and high-speed data units.

Location

The DLC is in the line concentrating module (LCM) drawer of the DMS/SL–100. The DLC is in two slots in a standard line card drawer where the DLC obtains the following:

- power
- subscriber loop tip–and–ring connections
- interfaces to the line card bus interface card (BIC)

The BIC is an interface to the rest of the network.

Functional description

The DLC provides an interface between the data unit and the switch. The DLC provides buffering/flow control for switch to data unit messaging. The DLC provides improved front–end loop interface protection circuitry to support the CSA/UL 600–V power cross safety specifications.

Functional blocks

The NT6X71ACcontains the following functional blocks:

- the loop interface circuit
- the time compression multiplex (TCM)–large scale integration (LSI) (X14)
- the microcomputer

Loop interface circuit

The DLC loop interface provides high–speed data transmission over a non–loaded, two–wire metallic facility.

TCM–LSI (X14)

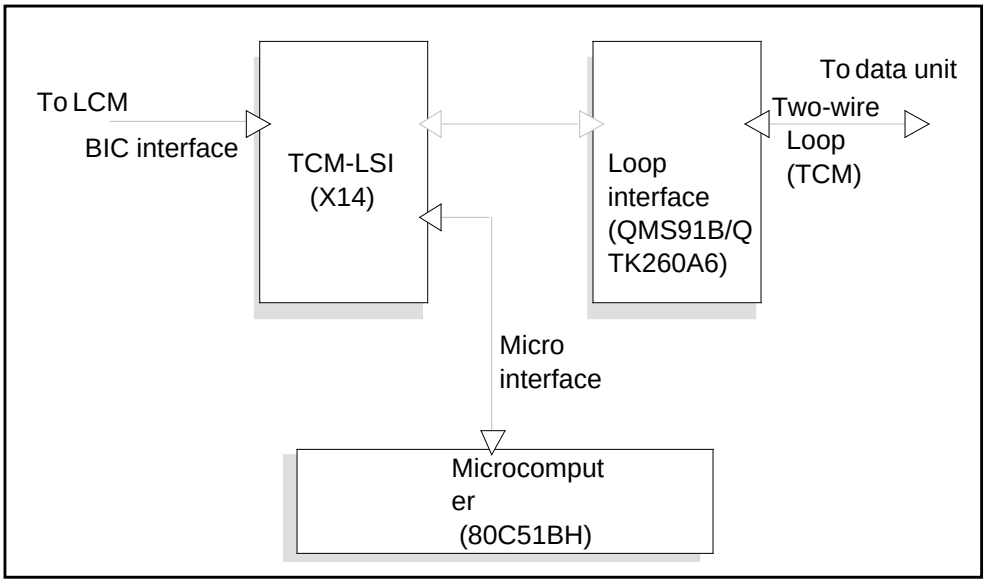
The TCM–LSI provides a signaling channel for processing messages between the switch and the data unit. The DLC microcomputer communicates to the TCM–LSI device through an 8–bit data bus. This interface passes LCM and data unit signaling information, and line card controls.

Microcomputer

The 80C51BH single–chip microcomputer interfaces directly to the TCM–LSI. The 80C51BH provides buffering and flow control and protocol conversion for messaging between the data unit and the switch.

The relationship between the functional blocks appears in the following figure.

NT6X71AC functional blocks



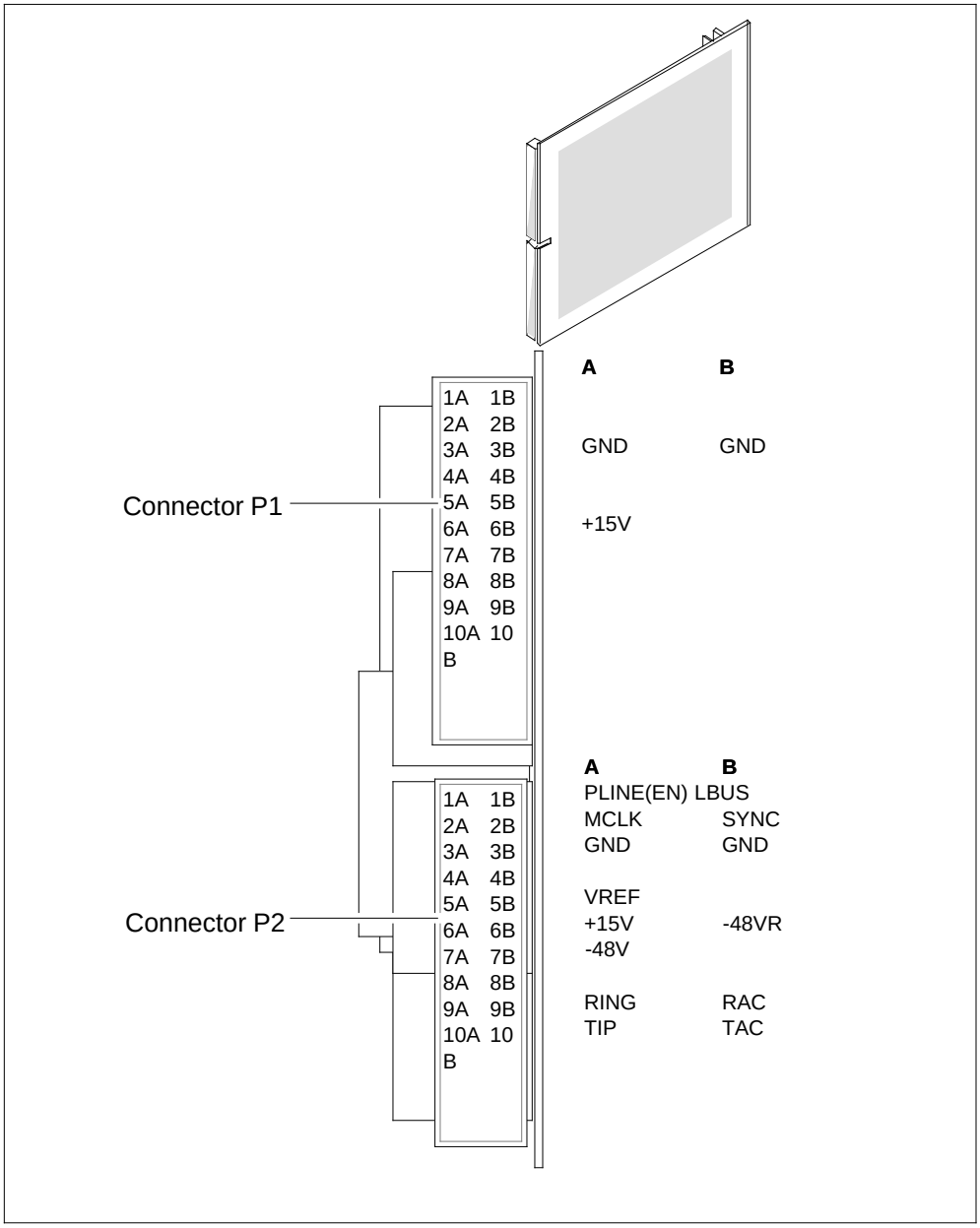
Signaling

Pin numbers

The pin numbers for NT6X71AC appear in the following figure.

NT6X71AC (continued)

NT6X71AC pin numbers



Technical data

Power requirements

The DLC receives power through the connector to the line drawer. This connector provides +15V, +5V, and -48V. The DLC does not use the +5V connector from the LCM drawer. The system generates the DLC digital logic +5V supply from the +15V supply through a 78C05 series linear voltage

regulator. The +12.7V reference voltage is also present. The required currents for the appear in the following table.

NT6X71AC required currents

Current	Voltage
48.3 mA	+15V
6 mA	-48V
0.5 mA	+12.7V

NT6X71BA

Product description

The NT6X71BA forms part of a Datapath facility that provides circuit--switched data on the DMS and SL-100 group of switches. The data line card (DLC) provides an interface for low speed and high speed data units and coaxial eliminators. The DLC provides the interface through a two-wire subscriber loop to the switch. The circuits are on a standard one-slot line card 8.89 cm by 7.62 cm (3.5 in. by 3 in.). The card receives power from a supply voltage of +15V. The line concentrating module (LCM) line drawer backplane supplies this voltage.

The NT6X71BA operates the same as the NT6X71AB. The NT6X71BA supports the same customer premises equipment and features.

Location

The NT6X71BA is in the LCM drawer of DMS or SL-100 switches. The NT6X71BA is in one slot in a standard line card drawer where the NT6X71BA obtains the following:

- power
- subscriber loop tip and ring connections
- an interface to the line card bus interface card

The bus interface card provides an interface to the rest of the network.

Functional description

The primary function of the is to provide a Datapath loop interface. This interface enables switched data on the DMS and SL-100 group of switches.

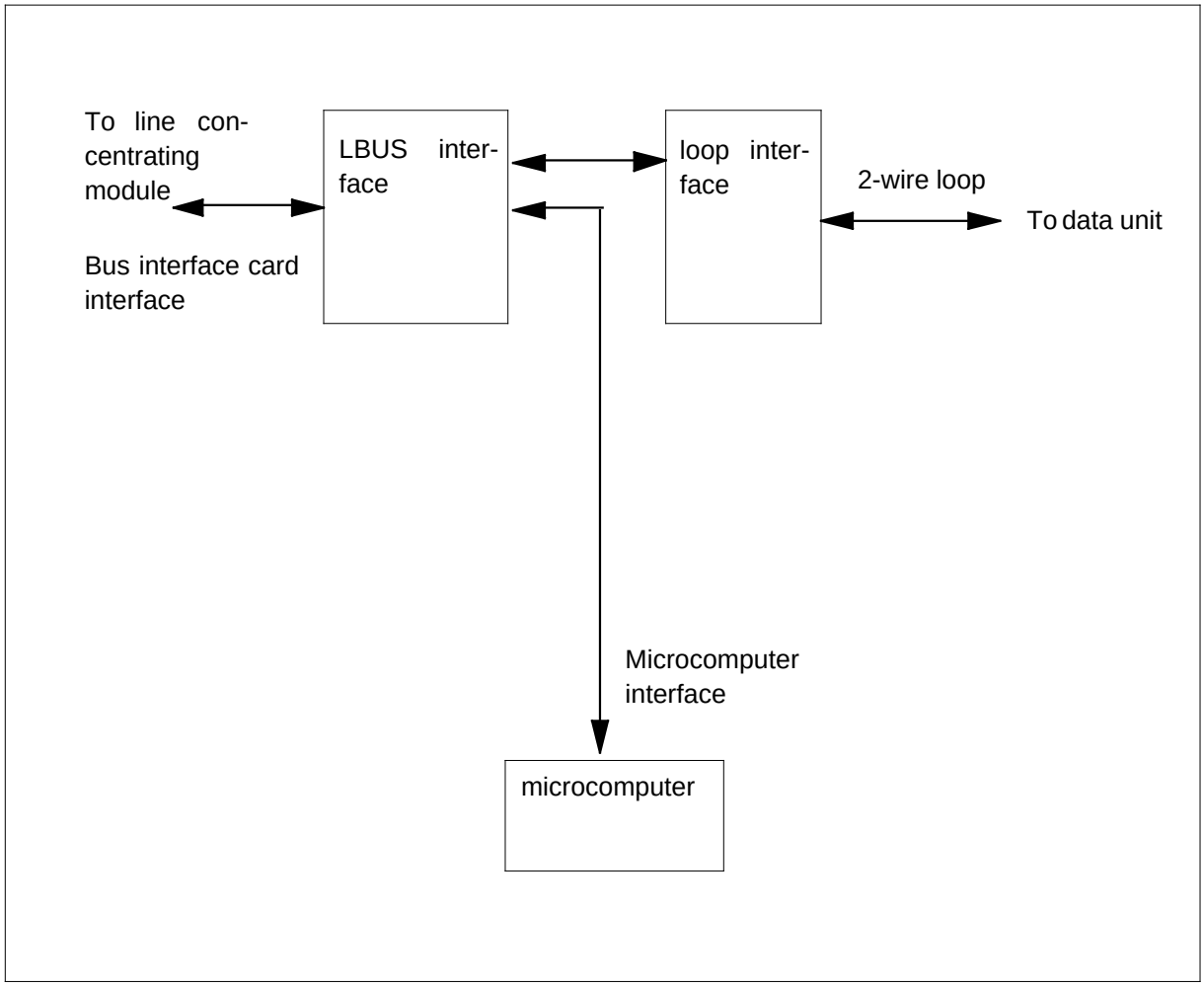
Functional blocks

The NT6X71BA contains three major subsystems:

- the LBUS interface
- the TCM loop interface
- the microcomputer

The relationship with the functional blocks appears in the following figure.

NT6X71BA functional blocks



LBUS interface

The LBUS interface connects the NT6X71BA to the switch. This interface is a standardized drawer-level interface for all line cards in a LCM.

The signaling interface between the card and the LCM needs four signals from the connector (P1) of the LCM connector:

- MCLK
- PLINE
- LBUS
- SYNC

NT6X71BA (continued)

TCM loop interface

The loop interface uses time compression multiplexing technology to provide high speed data full-duplex transmission. The frame rate is 1 kHz with a data rate of 160 kbit/s. During each frame, this frame rate provides a bidirectional exchange of 2 framing bits, 8 signaling bits and 64 data bits.

Microcomputer

The single-chip microcontroller is for messaging, relay control, and power-on initialization of the hardware. The single-chip microcontroller contains the following features:

- 128 bytes of internal data RAM
- 4 kbytes of internal masked ROM program memory
- low power, idle standby mode accessed through the IDL instruction
- boolean processor
- 32 programmable input-output lines

Signaling

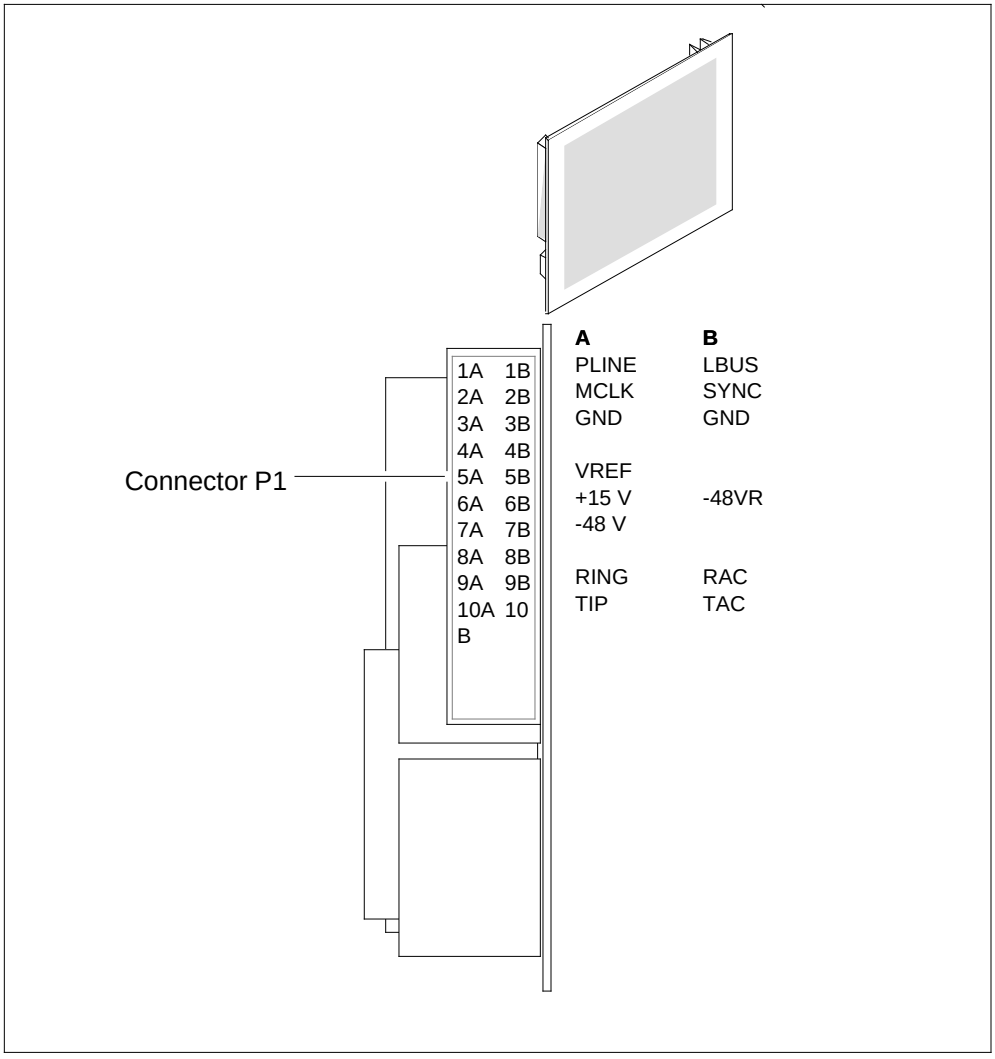
The NT6X71BA connects to the DMS switch through the LCM drawer interface. The DLC is in a single slot position in an LCM drawer. The DLC uses one 20-pin connector to provide mechanical, power and electrical signal interfacing.

Pin numbers

The system supplies 20 pin connections. The DLC only uses 14 pin connections.

The pin numbers for the NT6X71BA appear in the following figure.

NT6X71BA pin numbers



Technical data

The NT6X71BA is a single slot version of the NT6X71AB data line card.

To reduce size and power use, the BA version uses the following current modules:

- line equalizer implemented in an analog ASIC
- single chip, masked ROM microcontroller
- +15V to +5V switched capacitor voltage regulator
- discrete surface mount components

NT6X71BA (end)

The NT6X71BA front end complies with the Bellcore 2500V first level lightning and the CSA/UL 600V power cross specifications.

Power requirements

The NT6X71BA receives +15V, +5V and -48V power through the connector to the line drawer. The DLC does not use the +5V from the line drawer. The DLC uses a switched capacitor voltage converter and a linear voltage regulator. The DLC uses these components to convert the 15-V power feed to +5V and power the microcomputer and the LBUS interface controller. The NT6X71BA meets the power limits of the line drawer single slot line card.

NT6X72AA

Product description

The remote cluster controller (RCC) shares a common hardware structure with the line trunk controller (LTC). The RCC does not share this structure with the NT6X72AA formatter card, network side DS–1 cards, or a custom backplane. The user can make all functional changes to adapt network side communication ports from DS30 to DS–1. To make the changes, replace the NT6X41 speech bus formatter card with the NT6X72AA.

The NT6X72AA is based on the NT6X41 card, with the following changes:

- modification to the timing of transmit pulse code modulation (XPCM) and receive pulse code modulation (RPCM) paths. The modification matches the timing of the NT6X50 DS–1 interface card.
- the network interface communication link on ports 0, 1, 2 and 3 on channel 1
- A/B bit transparency between host and peripheral side (P–side) DS–1 cards

Location

The NT6X72AA is between the 16 network side DS–1 ports and the parallel speech buses (SB) in the RCC.

Functional description

The NT6X72AA meets the following functional requirements:

- RPCM serial–to–parallel conversion
- XPCM parallel–to–serial conversion
- network message interface
- shelf clock generation
- raw T1 clock generation
- signaling processor (SP) interface

RPCM serial–to–parallel conversion

The NT6X72AA receives eight serial port multiplexed DS60 signals from network side DS–1 ports. For each port or channel, each data stream can merge selectively with looped–around XPCM data. The system latches this data stream and presents the data stream to the W–72 formatter chip. The W–72 formatter chip translates the serial data into a parallel format. The system latches the signals on the edge of the C195+ that rises and buffers the signals before driving the RPCM SB.

NT6X72AA (continued)

The connection memory (CM) on the message card allows the NT6X72AA formatter to drive the RPCM SB. The NT6X72AA provides a separate enable input to allow another card to bridge the RPCM SB. To bridge the RPCM, the other card locally does not allow the formatter card to drive the SB.

XPCM parallel–to–serial conversion

In the XPCM speech path, the system takes parallel data from the SB and translates the data to a serial port multiplexed DS60 format. The system delays the data to meet external timing requirements. The system latches the parallel data from the XPCM SB and presents the data to the W–72 formatter chip. An A/B bit overwrites the least significant bit that latches on a port–per–channel basis. The time switch card provides the A/B bit. On a port–per–channel basis, the system can insert this bit on every sixth frame or on each frame. The selection of bit functionality originates from the control memory on the formatter card.

The W–72 formatter chip translates the parallel format of the latched data to eight serial DS60 data streams. The system latches the data and writes the data to two sets of delay RAM. One RAM bank delays the data before the data is output to the network DS–1 ports. The second RAM bank delays the data before the system presents the data to the looparound RPCM path.

Network message interface

The network side of the network message interface channel integrates to the NT6X72AA. Two or four of the 640 network face port/channels can function as a messaging facility. The face port/channels can function as a messaging facility between the central control and the SP. Channel 1 of ports 0 and 2 is the primary messaging channel. The system always enables these channels for messaging. Channel 1 of ports 1 and 3 is the secondary messaging channel. These card can use these channels selectively for pulse code modulation (PCM) or messaging. The system latches these specified messaging channels in a shift register. These channels can shift out of the NT6X72AA card when enabled. The system generates the enable when data received from the message interface card is directly inserted in the outgoing PCM.

Data from channel 1 of ports 1 and 3 and the primary port data can be inserted in the outgoing PCM. This condition occurs if the system enables secondary port messaging. If the system disables secondary port messaging, the message byte does not overwrite channel 1 of ports 1 and 3. Data contention cannot occur because the XPCM data stream is advanced in time for RPCM data. The system latches data out on the edge of C390+ that rises, and passes data through the formatter card. The system latches the data to the DS–1 card on the edge of C195+ that rises.

The timing of a message channel is based on the active shelf. The inactive shelf can message to the central control through the active formatter. Message ports assigned to each shelf are divided between the DS–1 cards to improve reliability.

Shelf clock generation

Shelf clock generation in the RCC is based on a phase–locked loop technique. Shelf clock generation uses voltage–controlled oscillator (VCO), digital filter, and phase comparators. The generation of the master clock is based on one of the two primary messaging ports or the mate shelf. The generation includes the superframe of the mate. The digital filter in the SP uses digital phase measurements as an input. Output of the digital filter passes through a digital–to–analog converter to control the VCO.

The system can make a phase comparison between the selected reference and shelf clocks. To make a phase comparison, the system latches the reference frame pulse with the state of a counter string. The shelf clock toggles the state of a counter string. The SP accesses these latches to obtain the input data for the digital filter algorithm. The system writes the calculation to the converter. A 12–bit binary counter string activates the converter. This string is loaded with data output from the digital filter algorithm one time for each frame. The shelf clock toggles the counter at a C97 clock rate. When the most significant (MS) counter reaches the terminal count, the system disables the counter. The indication of the terminal state of the MS counter produces an 8–kHz pulse width modulated signal. This signal is filtered and controls modulation input of the VCO.

Raw T1 clock generator

Raw T1 clock generation on the NT6X72AA occurs through the use of a look–up PROM. The raw T1 generator addresses the PROM from a counter string driven at a C195 rate. The generator routes waveform that a single bit output caused, to all DS–1 cards. The DS–1 cards filter the waveform.

Signaling processor interface

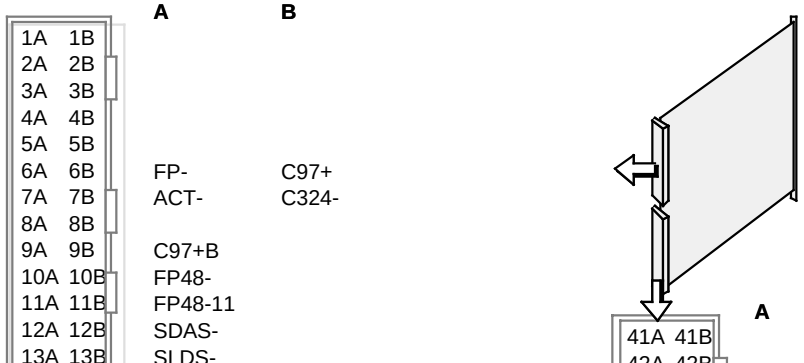
The SP controls shelf clock generation and the intra–call looparound selection circuit on the NT6X72AA. The SP address and data buses are buffered before the buses enter the card. Address decoding logic generates device selects for the card and the handshaking signals that the 68000 microprocessor requires.

Signaling

Pin numbers

The pin numbers for the NT6X72AA appear in the following figure.

NT6X72AA (end)



	A	B	
1A 1B			
2A 2B			
3A 3B			
4A 4B			
5A 5B			
6A 6B	FP-	C97+	
7A 7B	ACT-	C324-	
8A 8B			
9A 9B	C97+B		
10A 10B	FP48-		
11A 11B	FP48-11		
12A 12B	SDAS-		
13A 13B	SLDS-		
14A 14B	SDTACK-		
15A 15B	SUDS-		
16A 16B	SWRT-		
17A 17B			
18A 18B	C324/0		
19A 19B			
20A 20B	PCMOUT01/0		
21A 21B	PCMOUT23/0		
22A 22B	PCMOUT45/0		
23A 23B	PCMOUT67/0	FP48H-	
24A 24B	PCMOUT89/0	HFP48-11	
25A 25B	PCMOUTAB/0		
26A 26B	PCMOUTCD/0		
27A 27B	PCMOUTEF/0		
28A 28B			
29A 29B			
30A 30B			
31A 31B			
32A 32B			
33A 33B			
34A 34B			
35A 35B			
36A 36B			
37A 37B			
38A 38B			
39A 39B	CHIT-		
40A 40B	CHIT-/0		

	A	B
41A 41B		
42A 42B		PINB
43A 43B		POUTA
44A 44B		POUTB
45A 45B		HODRST-
46A 46B		
47A 47B		
48A 48B		
49A 49B		
50A 50B		PCMIN01/0
51A 51B		PCMIN23/0
52A 52B	SVBIT	PCMIN45/0
53A 53B	SBIT	PCMIN67/0
54A 54B	FOUTE+	PCMIN89/0
55A 55B	PINA	PCMINAB/0
56A 56B	CSPEN+	PCMINCD/0
57A 57B	C97+AM/0	PCMINEF/0
58A 58B		MSGIN0
59A 59B		MSGOUT0
60A 60B		MSGIN1
61A 61B		MSGOUT1
62A 62B		MSGIN2
63A 63B		MSGOUT2
64A 64B		MSGIN3
65A 65B		MSGOUT3
66A 66B		FP-N
67A 67B		FPRCO/1
68A 68B		FPRCO/0
69A 69B		OFP240-
70A 70B		IFP240-
71A 71B		FP-A
72A 72B		C97+A
73A 73B		FP-/0
74A 74B		
75A 75B	SWACK+	C97+M/0
76A 76B		
77A 77B		
78A 78B		
79A 79B		
80A 80B		

NT6X72BA

Product description

The NT6X72BA and the backplane account for the difference between the following:

- remote cluster controller offshore (RCCO)
- ISDN remote cluster controller (RCCI)

Location

The NT6X72BA card is between the 16 network–side PCM30 ports and the parallel speech buses (SB) in the RCCO.

Functional description

The NT6X72BA performs the following functions:

- performs receive pulse code modulation (RPCM) serial–to–parallel conversion
- performs transmit pulse code modulation (XPCM) parallel–to–serial conversion
- performs a network message interface
- generates a shelf clock
- resets a power–up
- maps time slots
- provides a central side (C–side) control time slot 0 (CTS 0) PCM30 control and status register interface
- provides a signaling processor (SP) interface

RPCM serial–to–parallel conversion

The NT6X72BA card receives DS60 signals from network side PCM30 ports. For each port or channel, each data stream can merge selectively with looped–around XPCM data. The card latches and presents this data stream to the N0–2 formatter chip. The N0–2 formatter chip translates serial data streams to a parallel format. The card latches and buffers the signals before the system drives the RPCM SB.

The system drives the RPCM SB from the NT6X72BA formatter when the connection memory (CM) enables the RPCM SB on the message card. The NT6X72BA provides a separate cable input so another card can bridge the RPCM SB. The NT6X72BA does not allow the formatter card to drive the SB. The card locally disables the formatter card to allow a card to bridge the RPCM SB. A packet assembler/disassembler (PAD) is available on a separate local copy of the SB that the NT6X72BA presents for future use.

NT6X72BA (continued)

XPCM parallel–to–serial conversion

The card takes parallel data from the SB and translates the data to a serial port multiplexed DS60 format. A delay occurs so the data can meet external timing requirements.

The N0–2 formatter chip translates the parallel format of the latched data to eight serial DS60 data streams. The card latches and writes the data to two sets of delay RAM. One RAM bank delays the data before the data is output to the network PCM30 ports. The other RAM bank delays the data before the data goes to the looparound RPCM path.

Network message interface

The architecture of the line trunk controller (LTC) changes to produce a remote cluster controller (RCC). The network side of the network message interface channel is integrated to the NT6X72BA.

The active shelf determines the timing of a message channel. The inactive shelf can message to the central control (CC) through the active formatter. Message ports assigned to each shelf are split between the PCM30 cards to improve reliability.

Shelf clock generation

Shelf clock generation in the RCCO follows a phase–locked loop technique. The NT6X72BA uses voltage–controlled oscillator (VCO), digital filter, and phase comparators. The generation of the master clock follows one the following reference inputs:

- one of the two primary messaging ports
- the mate shelf, including the superframe of the mate

Power–up reset

To initialize the RCCO, the PCM30 links must open. The NT6X72BA provides the required byte.

Time slot mapping

For compatibility with current RCC software, NT6X72BA maps time slot 1 to time slot 16. The NT6X72BA changes the on–board EPROM that creates the channel 1 signal. This EPROM is clocked and labeled channel 97.

C–side CTS 0 PCM30 control and status register interface

These circuits allow communication between the RCC and the host line group controller (LGC) through PCM30 links. These circuits use the NT6X27 trunk interface cards to establish communication.

Control and status information use two RAMS to exchange between the SP and the PCM30 interface card. Examples of control and status information include international signaling, loopback control, and maintenance commands. The lower half of the RAMs contains the command bytes and the upper half contains the status bytes.

During CTS 0, the NT6X72BA extracts status bytes from the RPCM SB. The NT6X72BA inserts command bytes in the XPCM SB. Each CTS 0 contains control and status bytes for one register.

Signaling processor interface

The SP controls shelf clock generation and the intra–call, looparound selection circuit on the NT6X72BA. The NT6X72BA buffers the SP address and data buses before the buses enter the card. The address decoding logic generates device selects for the card and the handshaking signals that the 68000 microprocessor requires.

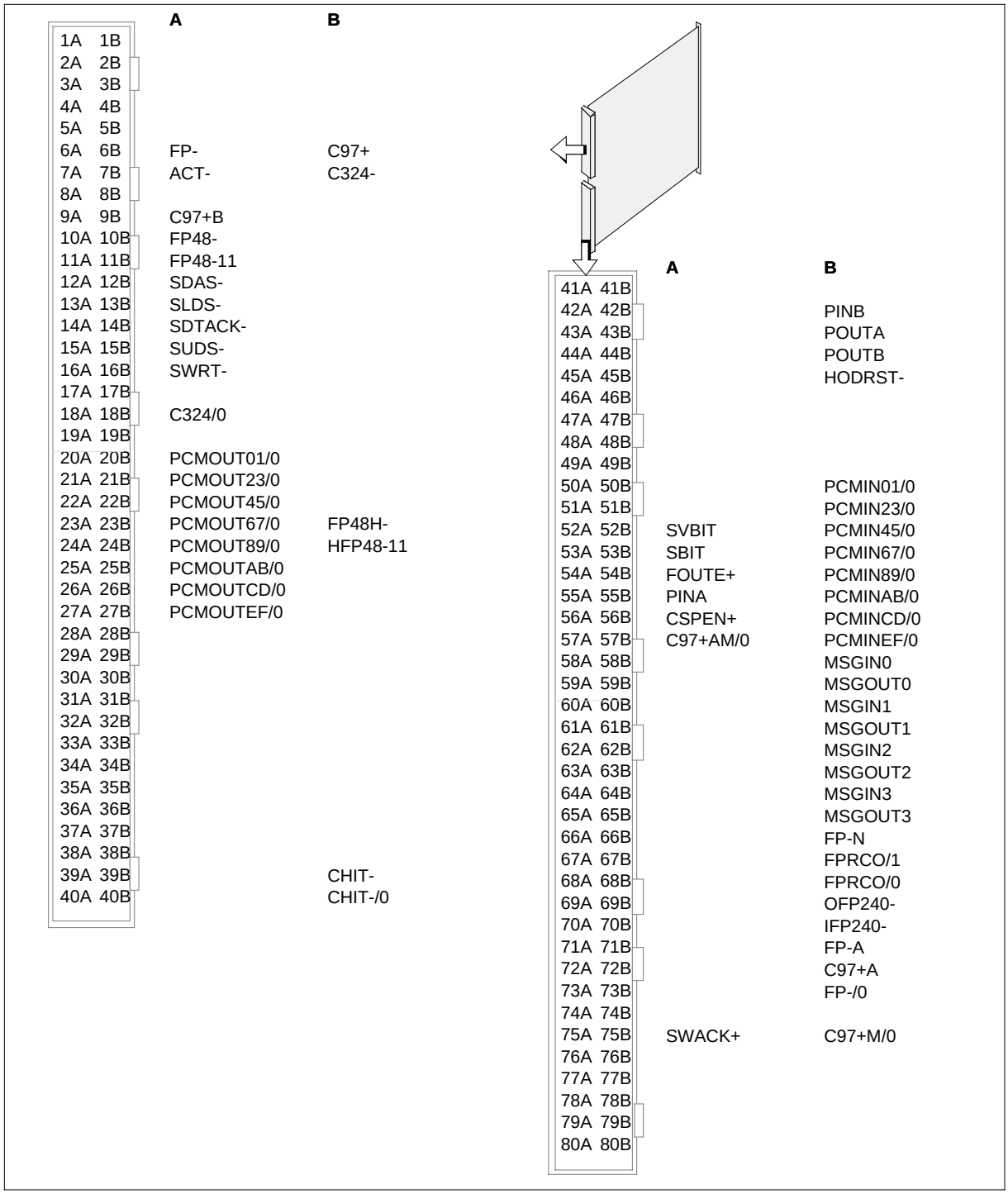
Signaling

Pin numbers

The pin numbers for the NT6X72BA appear in the following figure.

NT6X72BA (end)

NT6X72BA pin numbers



NT6X73AA

Product description

The Link Control Card (LCC) NT6X73AA is used in the North American or DS1 markets.

The NT6X73AA circuit pack provides an interface between the DS1 interface cards and the Line Concentrating Module (LCM) unit for remote LCM (RLCM) operations. If the NT6X73AA fails, the associated LCM is taken down. Intra-calling at the remote site is possible. An additional interface on the NT6X73AA connects to optional Emergency Stand-Alone (ESA) equipment.

Functional description

The NT6X73AA card consists of the following functional blocks:

- port assignment
- intra-calling
- remote maintenance module connection
- clock structure
- emergency stand-alone

Port assignment

Eight DS30A ports connect the NT6X73AA to the LCM digroup control card (NT6X52). The ports are labelled from 0 to 7. The NT6X73AA port assignments appear in the next table.

NT6X73AA port assignment (Sheet 1 of 2)

Port labels	Port assignment
0	Primary DS1 Port 0
1	Primary DS1 Port 1
2	Primary DS1 Port 2
3	Secondary DS1 Port 0
4	Secondary DS1 Port 1
5	Secondary DS1 Port 2

Note 1: Primary refers to ports normally used to access DS1 links.

Note 2: Secondary refers to backup ports which become active in LCC-LCM when the mate has dropped activity.

NT6X73AA (end)

NT6X73AA port assignment (Sheet 2 of 2)

Port labels	Port assignment
6	LCM to LCM inter-unit calling
7	Remote Maintenance Module
Note 1: Primary refers to ports normally used to access DS1 links.	
Note 2: Secondary refers to backup ports which become active in LCC-LCM when the mate has dropped activity.	

Intra-calling

NT6X73AA provides intra-calling that allows two subscribers served by the same RLCM to be switched within the RLCM. Intra-Calling reduces the occupancy of the DS1 links.

Remote Maintenance Module connection

The NT6X73AA provides connection to the Remote Maintenance Module (RMM) by duplicated paths through port 7 of the LCM. If the RMM is not provided, port 7 is not used.

Clock structure

The NT6X73AA provides the clock source for the RLCM. The RLCM clock configuration is based on a hot-standby arrangement. The clock source of the NT6X73AA is frequency locked to its primary DS1 link.

Emergency Stand-Alone

The NT6X73AA acts as an entry point for the optional Emergency Stand-Alone (ESA) package to gain access to message channels. If a DS1 line is cut, the RLCM can operate independently from the DS1. Only calls within the RLCM are completed and custom calling features will not function.

NT6X73BA

Product description

The Link Control Card (LCC) NT6X73BA is used in the International or PCM30 markets.

The NT6X73BA circuit pack provides an interface between the PCM30 interface cards and the Line Concentrating Module (LCM) unit for remote LCM (RLCM) operations. If the NT6X73BA fails, the associated LCM is taken down. Intra-calling at the remote site is possible. An additional interface on the NT6X73BA connects to optional Emergency Stand-Alone (ESA) equipment.

Functional description

The NT6X73BA card consists of the following functional blocks:

- port assignment
- intra-calling
- remote maintenance module connection
- clock structure
- emergency stand-alone

Port assignment

Eight PCM30A ports connect the NT6X73BA to the LCM digroup control card (NT6X52). The ports are labelled from 0 to 7. The NT6X73BA port assignments appear in the next table.

NT6X73BA port assignment (Sheet 1 of 2)

Port labels	Port assignment
0	Primary PCM30 Port 0
1	Primary PCM30 Port 1
2	Primary PCM30 Port 2
3	Secondary PCM30 Port 0
4	Secondary PCM30 Port 1
5	Secondary PCM30 Port 2
Note 1: Primary refers to ports normally used to access PCM30 links.	
Note 2: Secondary refers to backup ports which become active in LCC-LCM when the mate has dropped activity.	

NT6X73BA (end)

NT6X73BA port assignment (Sheet 2 of 2)

Port labels	Port assignment
6	LCM to LCM inter-unit calling
7	Remote Maintenance Module
Note 1: Primary refers to ports normally used to access PCM30 links. ***Note 2:*** Secondary refers to backup ports which become active in LCC-LCM when the mate has dropped activity.	

Intra-calling

NT6X73BA provides intra-calling that allows two subscribers served by the same RLCM to be switched within the RLCM. Intra-Calling reduces the occupancy of the PCM30 links.

Remote Maintenance Module connection

The NT6X73BA provides connection to the Remote Maintenance Module (RMM) by duplicated paths through port 7 of the LCM. If the RMM is not provided, port 7 is not used.

Clock structure

The NT6X73BA provides the clock source for the RLCM. The RLCM clock configuration is based on a hot-standby arrangement. The clock source of the NT6X73BA is frequency locked to its primary PCM30 link.

Emergency Stand-Alone

The NT6X73BA acts as an entry point for the optional Emergency Stand-Alone (ESA) package to gain access to message channels. If a PCM30 line is cut, the RLCM can operate independently from the PCM30. Only calls within the RLCM are completed and custom calling features will not function.

NT6X75AA

Product description

The optional emergency stand alone (ESA) clock and tone circuit card (NT6X75AA) provides a clock and tone source for the remote line concentrating module/outside plant module (RLCM/OPM) equipped with ESA. The NT6X75AA circuit card also provides an interface between the RLCM pulse code modulation (PCM) message paths and the ESA processor. The NT6X75AA circuit card provides a frame pulse to replace the lost DS-1 frame pulse from the host.

The NT6X75AA circuit card is in the RLCM/OPM host interface equipment (HIE). The NT6X75AA circuit card generates the clock signal for the line group controller (LGC) and digital trunk controller (DTC) processor, which enables the link control card (LCC) NT6X73AA to keep in sync. The NT6X75AA circuit card also provides the tones; dial, busy, reorder, receiver-off-hook, audible ringback and electronic business set ring-down required for ESA operation. During ESA the NT6X75AA circuit card communicates with both units of the line concentrating module (LCM) and remote maintenance module (RMM).

Functional description

The NT6X75AA circuit card provides the functions listed below, when its associated RLCM is in ESA mode:

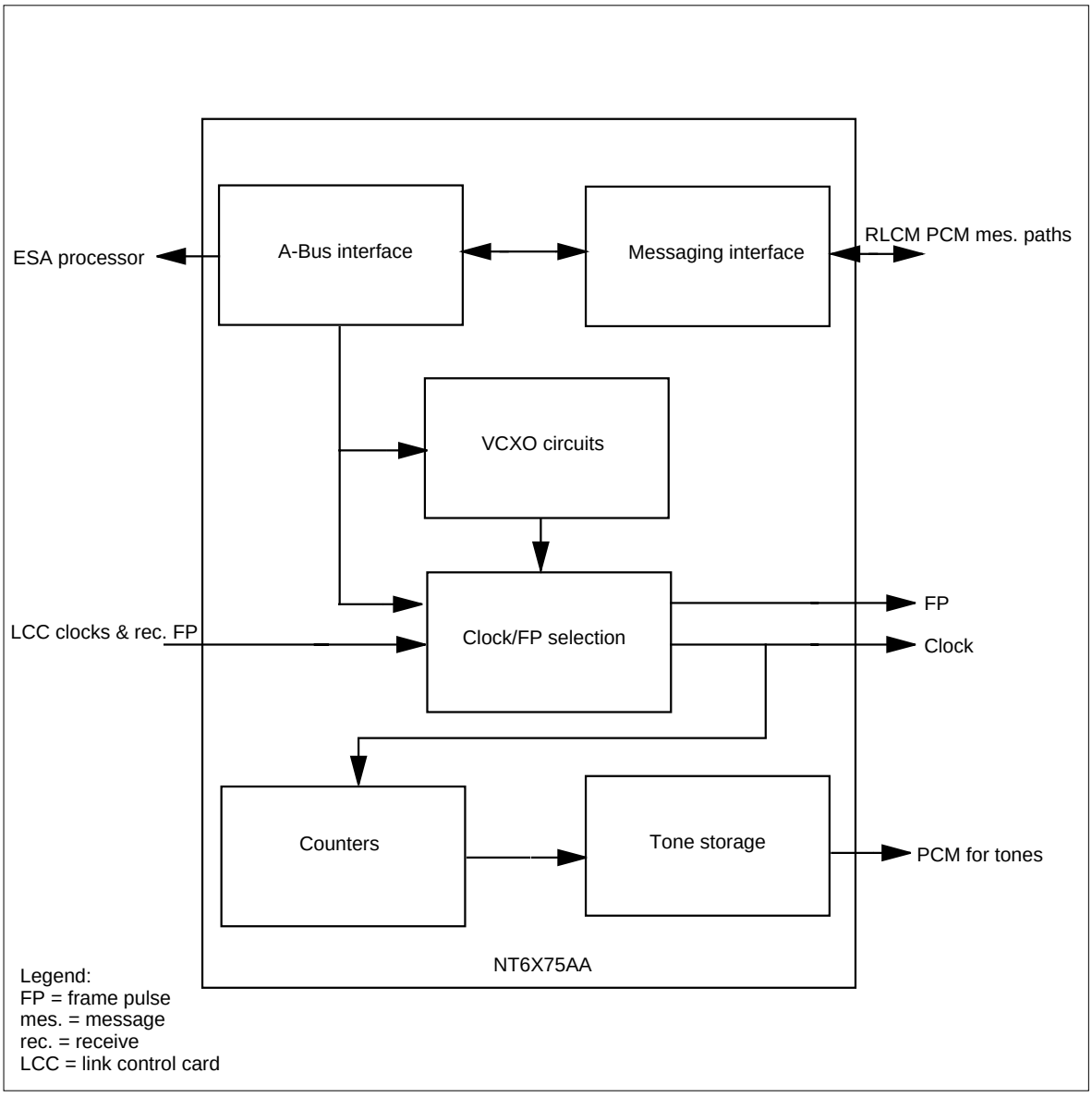
- clock sourcing
- tone sourcing
- interface between the RLCM PCM message paths and the ESA processor

Block diagram

This section provides a block diagram that displays the major functional blocks of the NT6X75AA circuit card, with interconnecting busses and signals.

NT6X75AA (continued)

NT6X75AA functional block diagram



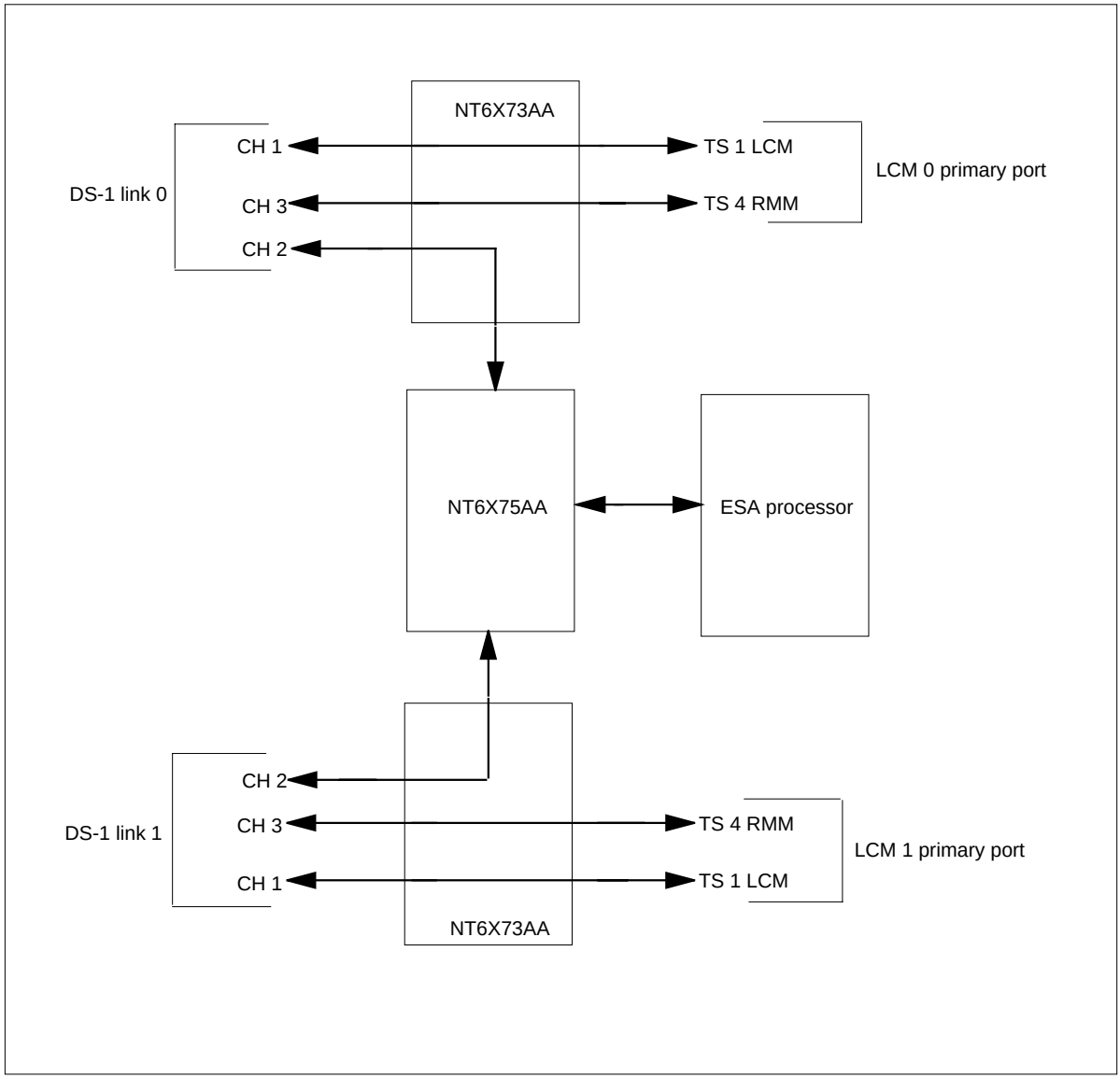
The NT6X75AA circuit card interfaces with the ESA processor in the ESA subsystem. This interface occurs through circuits on the NT6X75AA circuit card which conforms to the A-Bus standard. The ESA processor provides control information for adjusting the voltage controlled crystal oscillator (VCXO) and selection data for selecting the clock source which synchronizes the VCXO, clock and frame pulse signals.

The VCXO circuits contain counters and other circuit components that allow the ESA processor to set up counters to create the required control voltage to enable the VCXO to sync to a received frame pulse. Software continuously monitors and logs the phase of this frame pulse. The information gathered by this continuous monitoring aligns the VCXO generated frame pulse to minimize phase hits. This action occurs on entry of an ESA mode.

Link control card

The next diagram displays the NT6X75AA in normal operation.

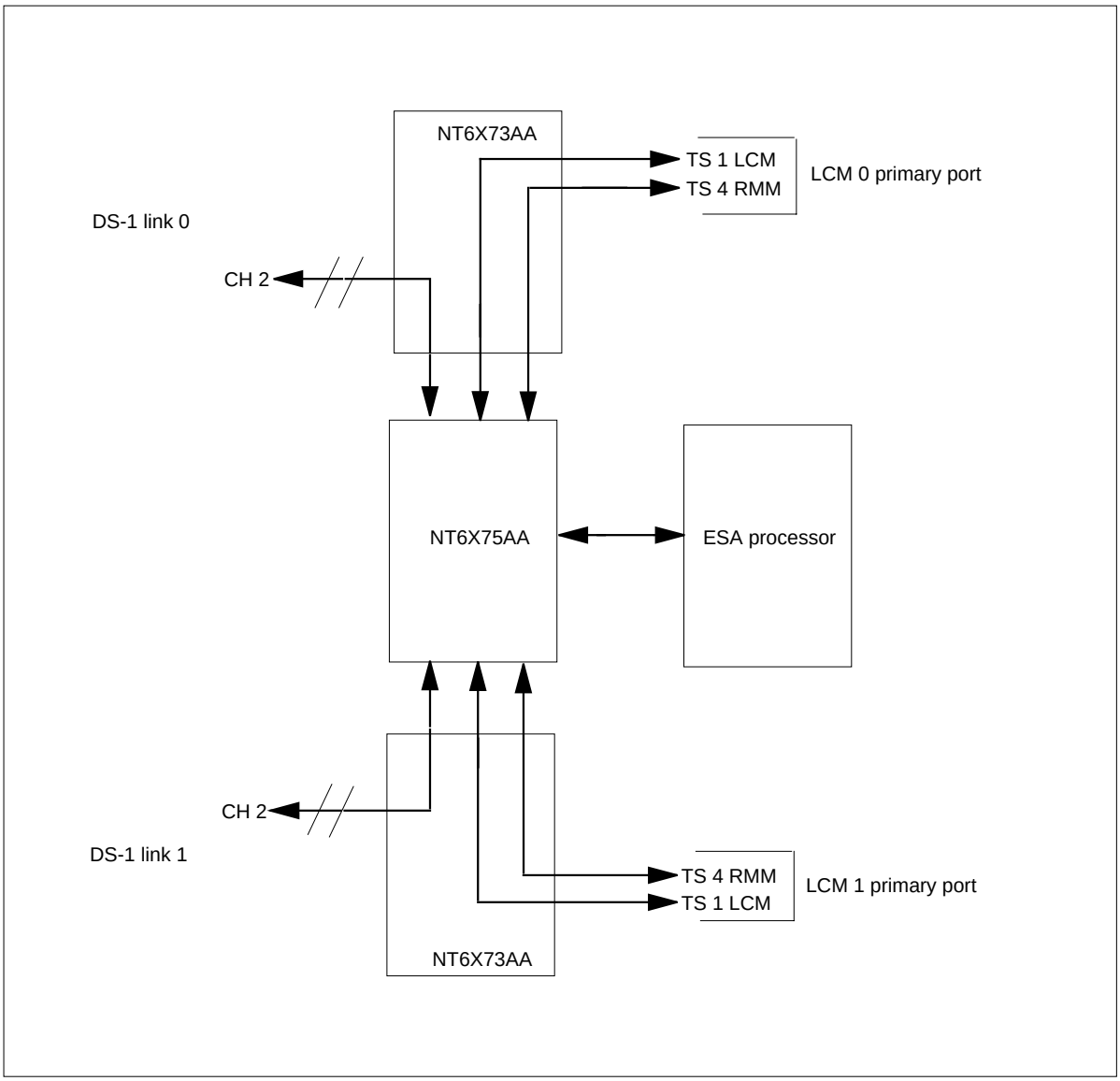
NT6X75AA message paths in normal mode



NT6X75AA (continued)

Under normal operation, an ESA uses time slot 3 (DS-1 channel 2) on DS-1 link 0 or 1 to host the DMS-X message channel. The next diagram displays the NT6X75AA in ESA mode.

NT6X755AA message paths in ESA mode



When the LCC is in ESA mode, time slot 1 from each LCM switches to the NT6X75AA from its normal DS-1 path. The ESA processor replaces the LGC as the host and the LCM continues to function as before.

Remote maintenance module

The RMM handles like the LCC in normal operation and in ESA mode. In ESA mode time slot 4 switches to the NT6X73AA circuit card. Time slot 4 provides a message channel to the RMM by way of the normal loop-around path in the LCM.

A-bus

The bus connections between the NT6X75AA circuit card and the ESA processor conform to the extended multi-processor system (XMS) A-Bus specification. The A-Bus terminates using balanced resistor network terminators, which ensure the integrity of the A-Bus under different environmental conditions.

Addressing

An address space of 32 bytes is in the NT6X75AA circuit card, using the five lowest order address bits. The NT6X75AA circuit card hardware and the ESA processor share the same bus for accessing messaging random access memory (RAM). An interlock prevents the ESA processor from interrupting with ordered hardware messaging operations.

Tones

A 64 kbit erasable programmable read-only memory (EPROM) stores tone samples for use during ESA. The eight maximum data lines store these tones in serial. The next table contains the tone allocation for the NT6X75AA circuit card.

Tone allocation

Lead	LCM port	Tone
Tone 0	7	Dial
Tone 1	1	Busy/reorder
Tone 2	4	Audible ringback
Tone 3	2	Receiver off-hook
Tone 4	5	P-phone ringing

NT6X75AA (continued)

The next table contains NT6X75AA tone frequencies and levels.

NT6X75AA tone frequencies and levels

Tone	Frequency (Hz)	Individual power (dBm)	Total power (dB)
Dial	350+	-13	-10
	440	-13	
Busy/reorder	480+	-24	-21
	620	-24	
Audible ringback	440+	-19	-16
	480	-19	
Receiver off-hook	1440+	-6	0.0
	2066+	-6	
	2466+	-6	
	2600	-6	
P-phone	516	-15	-15

Clock source

The NT6X75AA circuit card must operate in sync with the LCCs to transmit and receive message bytes. The clock sources are the LCCs. A multiplexer selects the C390 clock and FP48 multiframe pulse from one of the two LCCs. The clock source on the LCC is not appropriate for operation in ESA mode. The clock source on the LCC run 200 ppm above nominal frequency when the source of sync from the host is lost.The NT6X75AA circuit card contains an accurate VCXO clock to remedy this problem.

VCXO circuit

The VCXO circuit is followed by two sets of counters. One set of counters counts from 0 to 1279 before the signal VFP- resets the counter. VFP- is also sent to a D flip-flop that produces FP-ESA. FP-ESA is the frame pulse sent to the LCC, replacing the failed sync pulses from the DS-1 lines and becoming the system sync source.

The other set of counters load from a data bus. This second set of counters generate a frame pulse with a width variable from 1 to 1,280 97ns-wide clock pulses. The variable pulse generates by way of a low-pass filter an analog voltage that is applied to a 10.24 MHz VCXO.

Technical data

This section contains power requirements and signaling data for the NT6X75AA circuit card.

Power requirements

Power consumption for the NT6X75AA is 7.5 watts. Calculate the power consumption by multiplying the nominal voltage and current values from the next table.

Power specifications

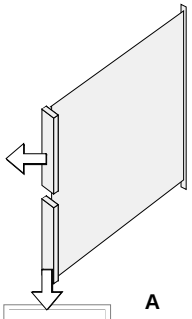
Parameter	Minimum	Nominal	Maximum	Units
Supply voltage	4.75	5.0	5.25	Volts
Supply noise		45		mV
Supply current	1.4	1.5	1.6	Amps

Signaling

The next table contains the backplane pin numbers for the NT6X75AA circuit card.

NT6X75AA (end)

NT6X75AA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	PWR+5V	PWR+5V
3A 3B	PWR+5V	PWR+5V
4A 4B	PWR+5V	PWR+5V
5A 5B	GND	GND
6A 6B	C390.0+	C390.1+
7A 7B	FP48.0	FP48.1–
8A 8B	OUTBYTE0	OUTBYTE1
9A 9B	HOSTESA0	HOSTESA1
10A 10B	FLCM0	FLCM1
11A 11B	ESA0	ESA1
12A 12B	DAS–	HSTCHEN1
13A 13B		HSTCHEN0
14A 14B	DTACK–	
15A 15B	UDS–	
16A 16B	WRT–	
17A 17B		
18A 18B	ESAIRQ–	
19A 19B	MODRST–	RSTOUT–
20A 20B	GND	
21A 21B		
22A 22B		ADDR06
23A 23B		ADDR07
24A 24B		ADDR08
25A 25B		ADDR09
26A 26B		ADDR10
27A 27B		
28A 28B		
29A 29B		
30A 30B		
31A 31B	ACTMON0	ACTMON1
32A 32B		ADDR01
33A 33B	TONE0	ADDR02
34A 34B	TONE1	ADDR03
35A 35B	TONE2	ADDR04
36A 36B	TONE3	ADDR05
37A 37B	TONE4	
38A 38B	TONE5	
39A 39B		
40A 40B	GND	GND

	A	B
41A 41B		
42A 42B		
43A 43B		
44A 44B		
45A 45B		
46A 46B		
47A 47B		
48A 48B		
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B	DATA00+	
58A 58B	DATA01+	
59A 59B	DATA02+	
60A 60B	DATA03+	ADDR11
61A 61B	DATA04+	GND
62A 62B	DATA05+	ADDR12
63A 63B	DATA06+	ADDR13
64A 64B	DATA07+	ADDR14
65A 65B		ADDR15
66A 66B		
67A 67B	DATA08+	
68A 68B	DATA09+	
69A 69B	DATA10+	ADDR16
70A 70B	DATA11+	ADDR17
71A 71B	DATA12	ADDR18
72A 72B	DATA13	ADDR19
73A 73B	DATA14	ADDR20
74A 74B	DATA15	ADDR21
75A 75B		FP-ESA
76A 76B	RECFP0	RECFP1
77A 77B		
78A 78B	GND	GND
79A 79B	ESAEN–	
80A 80B	GND	GND

NT6X75DA

Product description

The optional emergency stand alone (ESA) clock and tone circuit card (NT6X75DA) provides a clock and tone source for the international remote line concentrating module/outside plant module (IRLCM/OPM) equipped with ESA. The NT6X75DA circuit card also provides an interface between the IRLCM pulse code modulation (PCM) message paths and the ESA processor. The NT6X75DA circuit card provides a frame pulse to replace the lost PCM30 frame pulse from the host.

The NT6X75DA circuit card is in the IRLCM/OPM host interface equipment (HIE). The NT6X75DA circuit card generates the clock signal for the PCM30 line group controller (PLGC/ILGC) and PCM30 digital trunk controller (PDTC) processor, which enables the link control card (LCC) NT6X73BA to keep in sync. The NT6X75DA circuit card also provides the tones; dial, busy, reorder, receiver-off-hook, audible ringback and electronic business set ring-down required for ESA operation. During ESA the NT6X75DA circuit card communicates with both units of the PCM30 line concentrating module (ILCM) and remote maintenance module (RMM).

The NT6X75DA circuit card is for the Conference of European Postal and Telecommunications (CEPT) Administrations market. Where reference occurs to the IRLCM in this document, the same information applies to the international outside plant cabinet (IOPAC). Where reference occurs to the PLGC in this document, the same information applies to the international line group controller (ILGC).

Functional description

The NT6X75DA circuit card provides the functions listed below, when its associated RLCM is in ESA mode:

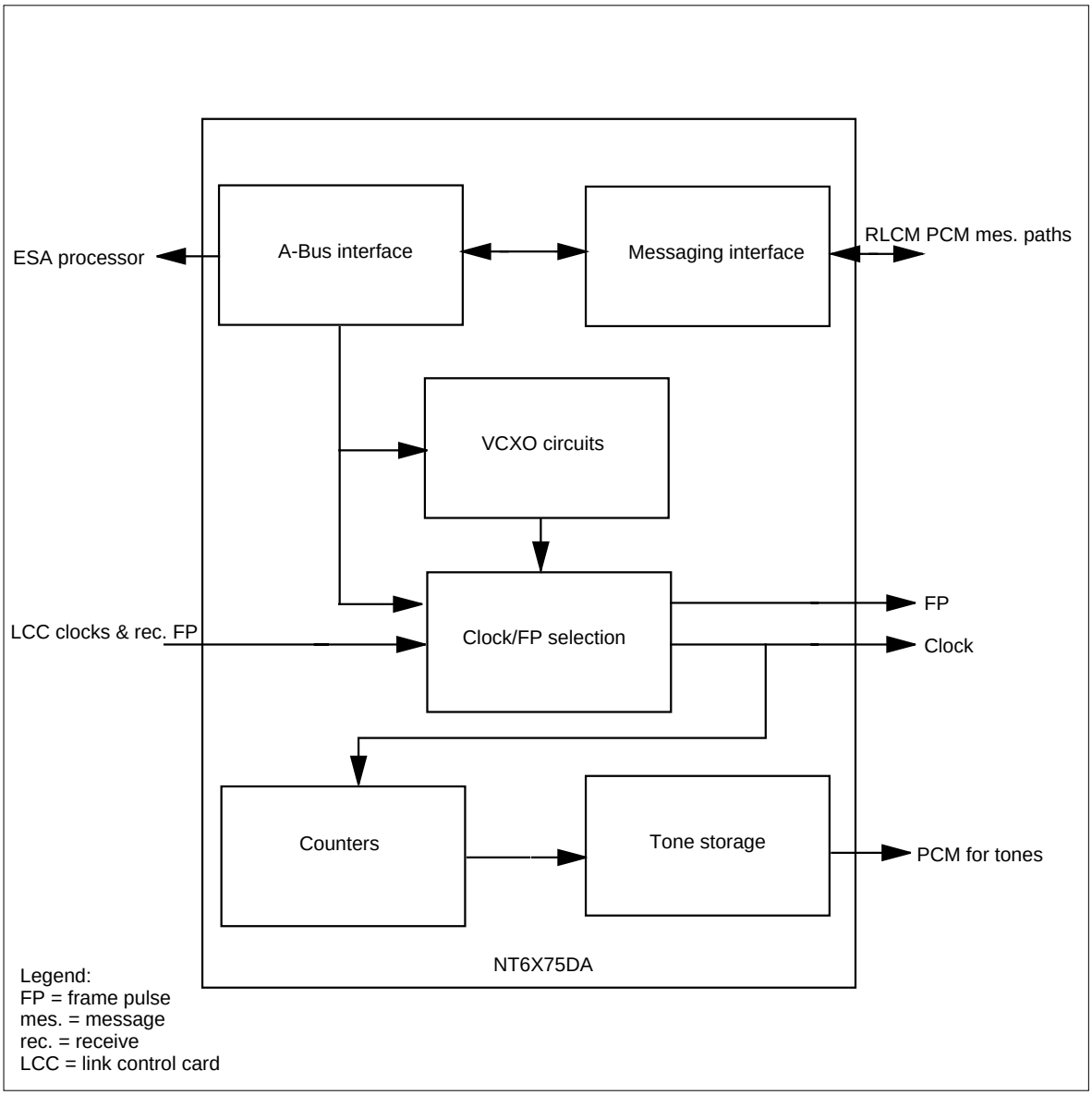
- clock sourcing
- tone sourcing
- interface between the IRLCM PCM message paths and the ESA processor

Block diagram

This section provides a block diagram that displays the major functional blocks of the NT6X75DA circuit card, with interconnecting busses and signals.

NT6X75DA (continued)

NT6X75DA functional block diagram



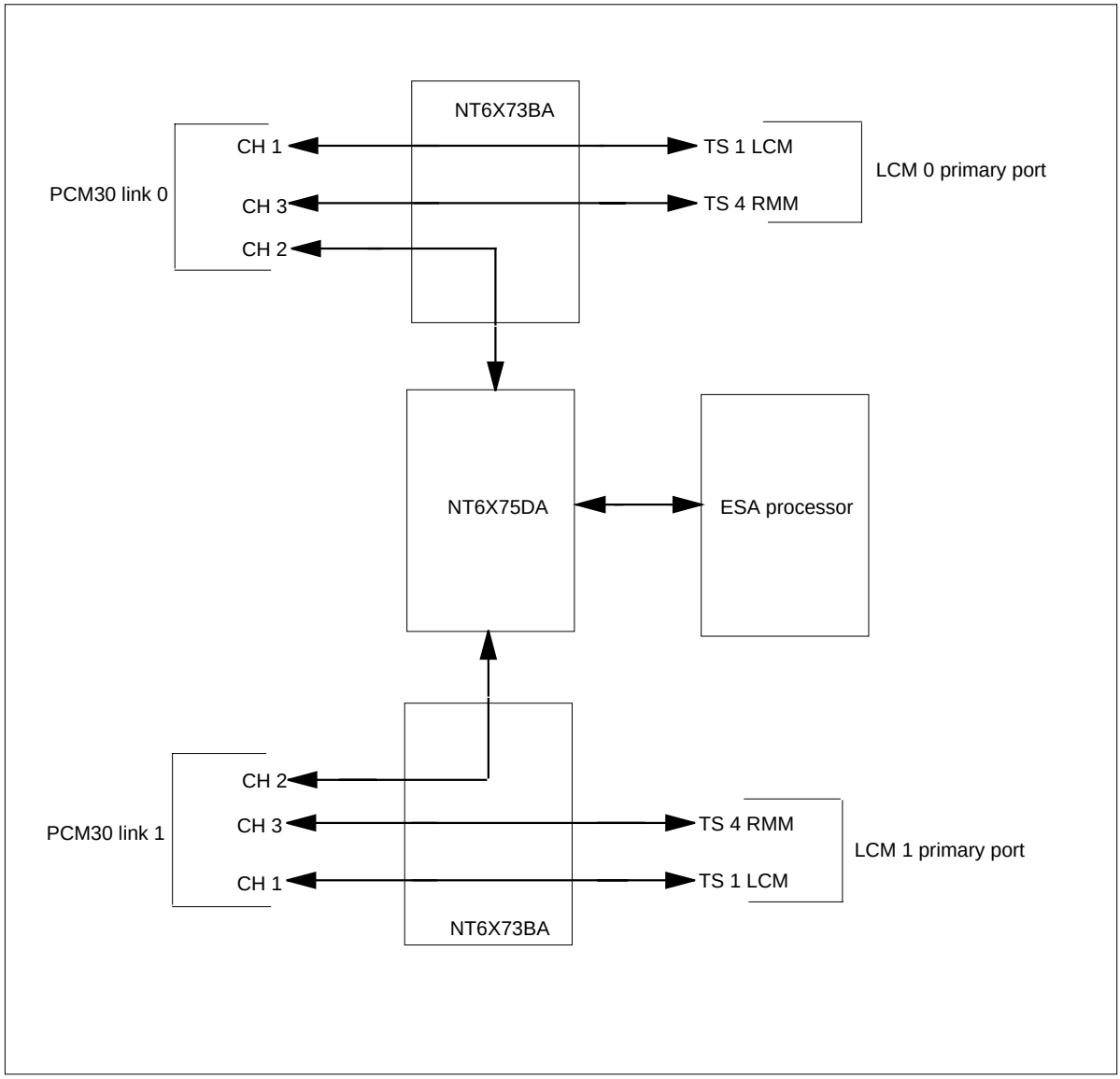
The NT6X75DA circuit card interfaces with the ESA processor in the ESA subsystem. This interface occurs through circuits on the NT6X75DA circuit card which conforms to the A-Bus standard. The ESA processor provides control information for adjusting the voltage controlled crystal oscillator (VCXO) and selection data for selecting the clock source which synchronizes the VCXO, clock and frame pulse signals.

The VCXO circuits contain counters and other circuit components that allow the ESA processor to set up counters to create the required control voltage to enable the VCXO to sync to a received frame pulse. Software continuously monitors and logs the phase of this frame pulse. The information gathered by this continuous monitoring aligns the VCXO generated frame pulse to minimize phase hits. This action occurs on entry of an ESA mode.

Link control card

The next diagram displays the NT6X75DA in normal operation.

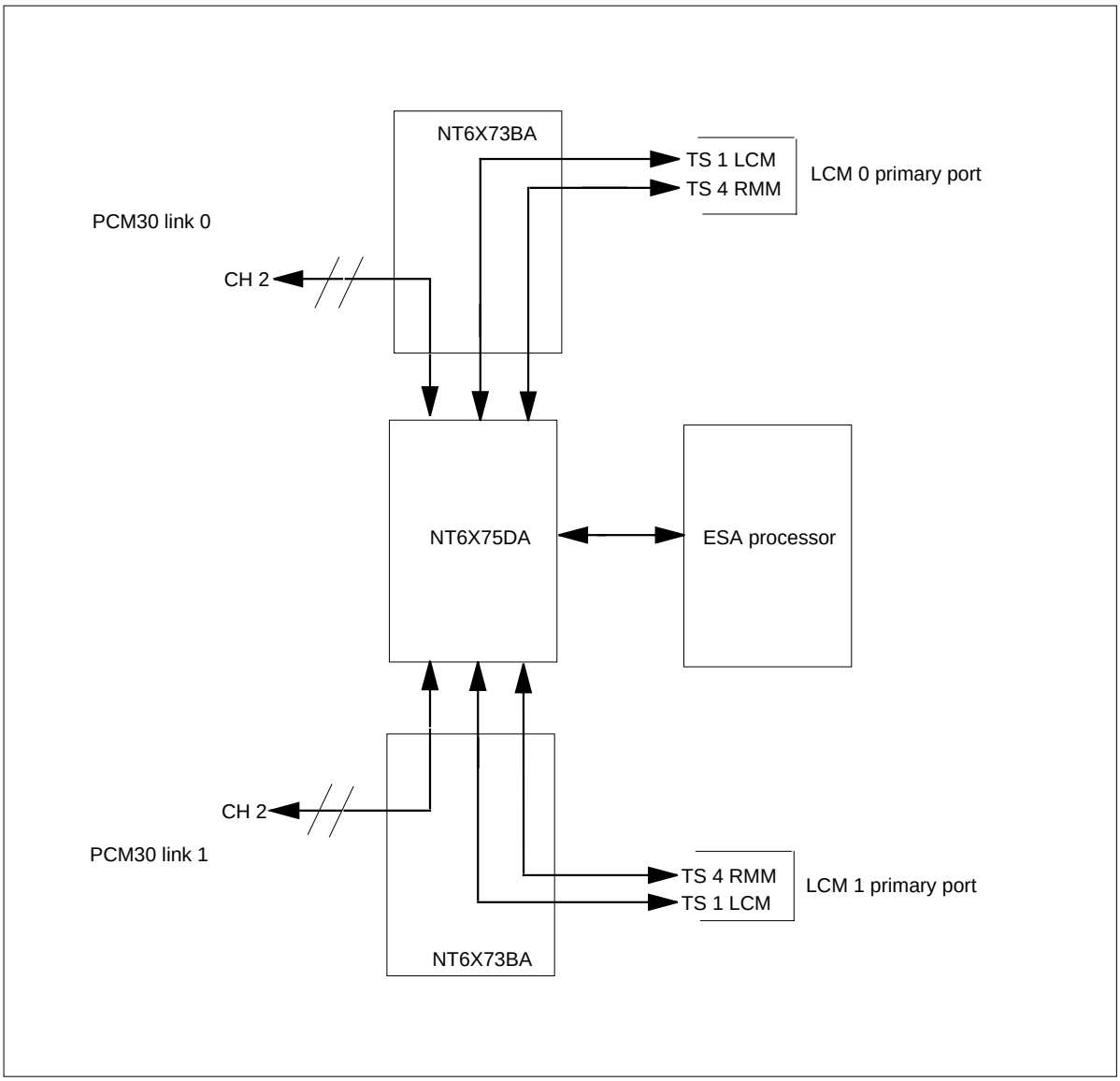
NT6X75DA message paths in normal mode



NT6X75DA (continued)

Under normal operation, an ESA uses time slot 3 (PCM30 channel 2) on PCM30 link 0 or 1 to host the DMS-X message channel. The next diagram displays the NT6X75DA in ESA mode.

NT6X755DA message paths in ESA mode



When the LCC is in ESA mode, time slot 1 from each LCM switches to the NT6X75DA from its normal PCM30 path. The ESA processor replaces the LGC as the host and the LCM continues to function as before.

Remote maintenance module

The RMM handles like the LCC in normal operation and in ESA mode. In ESA mode time slot 4 switches to the NT6X73BA circuit card. Time slot 4 provides a message channel to the RMM by way of the normal loop-around path in the LCM.

A-bus

The bus connections between the NT6X75DA circuit card and the ESA processor conform to the extended multi-processor system (XMS) A-Bus specification. The A-Bus terminates using balanced resistor network terminators, which ensure the integrity of the A-Bus under different environmental conditions.

Addressing

An address space of 32 bytes is in the NT6X75DA circuit card, using the five lowest order address bits. The NT6X75DA circuit card hardware and the ESA processor share the same bus for accessing messaging random access memory (RAM). An interlock prevents the ESA processor from interrupting with ordered hardware messaging operations.

Tones

A 64 kbit erasable programmable read-only memory (EPROM) stores tone samples for use during ESA. The eight maximum data lines store these tones in serial. The next table contains the tone allocation for the NT6X75DA circuit card.

Tone allocation

Lead	LCM port	Tone
Tone 0	7	Dial
Tone 1	1	Busy/reorder
Tone 2	4	Audible ringback
Tone 3	2	Receiver off-hook

NT6X75DA (continued)

The next table contains NT6X75DA tone frequencies and levels.

NT6X75DA tone frequencies and levels

Tone	Frequency (Hz)	Individual power (dBm)	Total power (dB)
Dial	350+	-13	-10
	440	-13	
Busy/reorder	480+	-13	-10
	620	-13	
Audible ringback	440+	-13	-10
	480	-13	
Receiver off-hook	1440+	-6	0.0
	2066+	-6	
	2466+	-6	
	2600	-6	

Clock source

The NT6X75DA circuit card must operate in sync with the LCCs to transmit and receive message bytes. The clock sources are the LCCs. A multiplexer selects the C390 clock and FP48 multiframe pulse from one of the two LCCs. The clock source on the LCC is not appropriate for operation in ESA mode. The clock source on the LCC run 200 ppm above nominal frequency when the source of sync from the host is lost. The NT6X75DA circuit card contains an accurate VCXO clock to remedy this problem.

VCXO circuit

The VCXO circuit is followed by two sets of counters. One set of counters counts from 0 to 1279 before the signal VFP- resets the counter. VFP- is also sent to a D flip-flop that produces FP-ESA. FP-ESA is the frame pulse sent to the LCC, replacing the failed sync pulses from the PCM30 lines and becoming the system sync source.

The other set of counters load from a data bus. This second set of counters generate a frame pulse with a width variable from 1 to 1,280 97ns-wide clock pulses. The variable pulse generates by way of a low-pass filter an analog voltage that is applied to a 10.24-MHz VCXO.

Technical data

This section contains power requirements and signaling data for the NT6X75DA circuit card.

Power requirements

Power consumption for the NT6X75DA is 7.5 watts. Calculate the power consumption by multiplying the nominal voltage and current values from the next table.

Power specifications

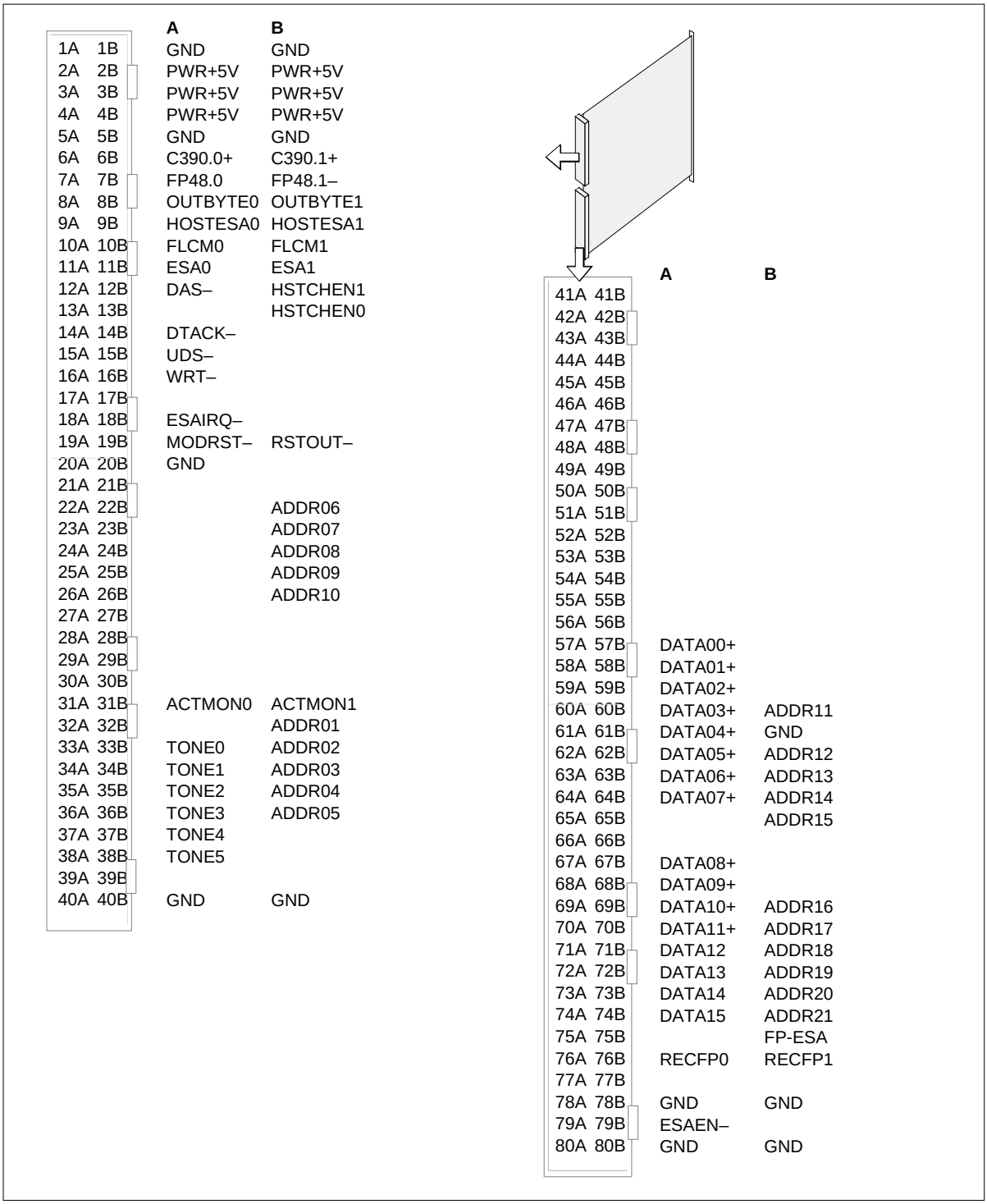
Parameter	Minimum	Nominal	Maximum	Units
Supply voltage	4.75	5.0	5.25	Volts
Supply noise		45		mV
Supply current	1.4	1.5	1.6	Amps

Signaling

The next table contains the backplane pin numbers for the NT6X75DA circuit card.

NT6X75DA (end)

NT6X75DA pin numbers



NT6X75EA

Product description

The optional emergency stand alone (ESA) clock and tone circuit card (NT6X75EA) provides a clock and tone source for the international remote line concentrating module/outside plant module (IRLCM/OPM) equipped with ESA. The NT6X75EA circuit card also provides as an interface between the IRLCM pulse code modulation (PCM) message paths and the ESA processor. The NT6X75EA circuit card provides a frame pulse to replace the lost PCM30 frame pulse from the host.

The NT6X75EA circuit card is in the IRLCM/OPM host interface equipment (HIE). The NT6X75EA circuit card generates the clock signal for the PCM30 line group controller (PLGC) and PCM30 digital trunk controller (PDTC) processor, which enables the link control card (LCC) NT6X73BA to keep in sync. The NT6X75EA circuit card also provides the tones; dial, busy, reorder, receiver-off-hook, audible ringback and electronic business set ring-down required for ESA operation. During ESA the NT6X75EA circuit card communicates with both units of the PCM30 line concentrating module (ILCM) and remote maintenance module (RMM).

The NT6X75EA circuit card is for the United Kingdom (UK) only. Where reference occurs to the IRLCM in this document, the same information applies to the international outside plant cabinet (IOPAC). Where reference occurs to the PLGC in this document, the same information applies to the international line group controller (ILGC).

Functional description

The NT6X75EA circuit card provides the functions listed below, when its associated RLCM is in ESA mode:

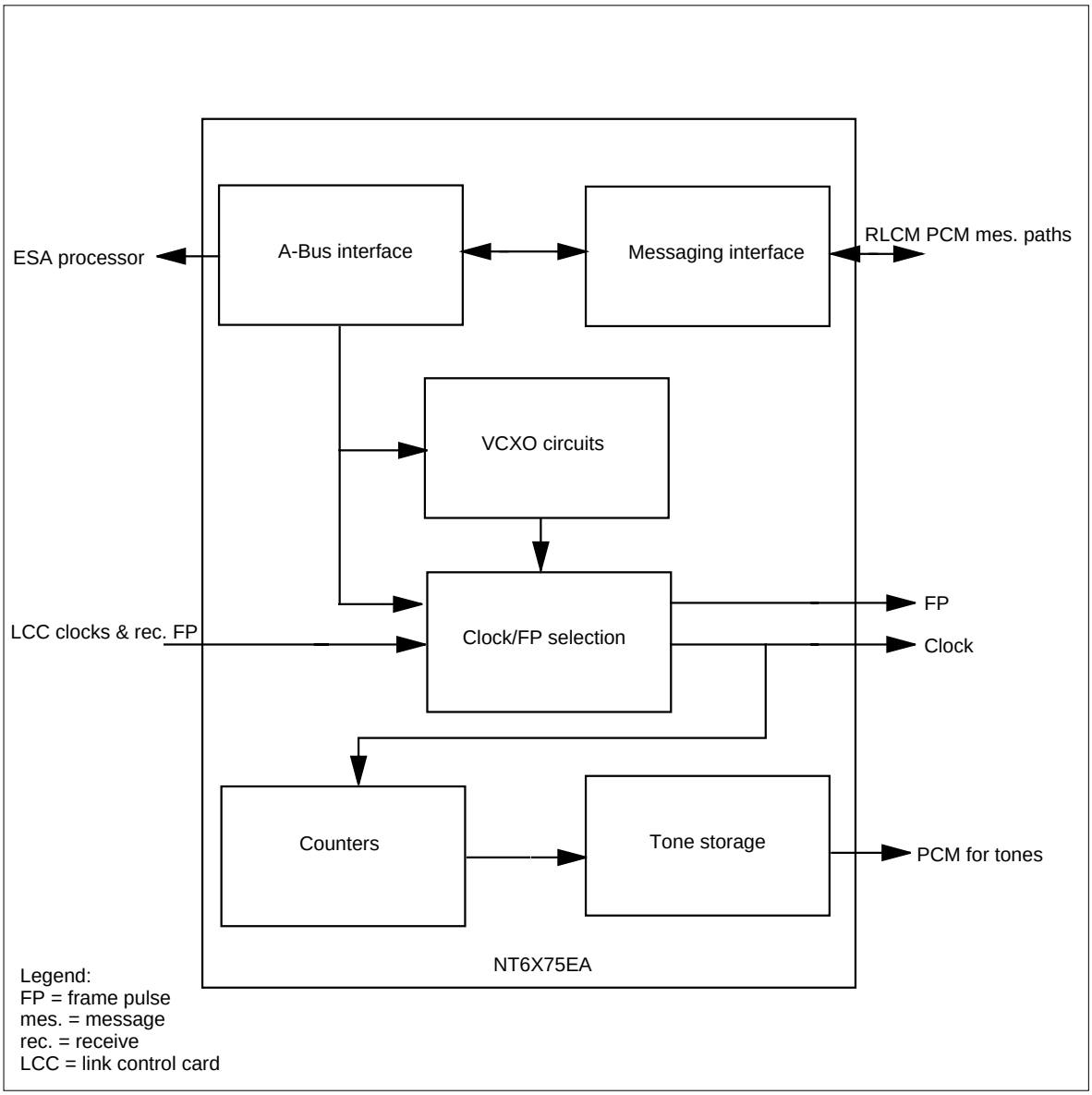
- clock sourcing
- tone sourcing
- interface between the IRLCM PCM message paths and the ESA processor

Block diagram

This section provides a block diagram that displays the major functional blocks of the NT6X75EA circuit card, with interconnecting busses and signals.

NT6X75EA (continued)

NT6X75EA functional block diagram



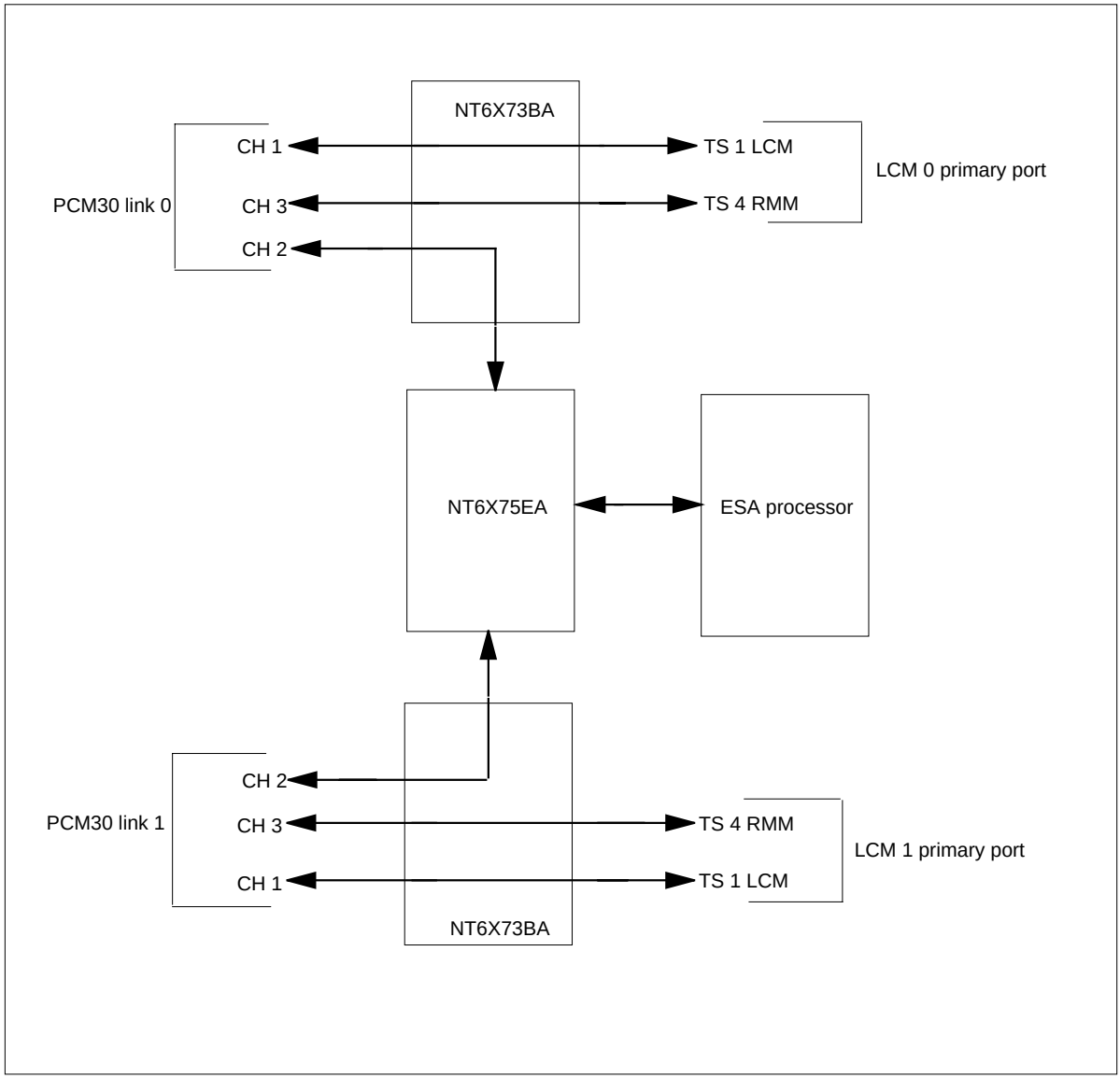
The NT6X75EA circuit card interfaces with the ESA processor in the ESA subsystem. This interface occurs through circuits on the NT6X75EA circuit card which conforms to the A-Bus standard. The ESA processor provides control information for adjusting the voltage controlled crystal oscillator (VCXO) and selection data for selecting the clock source which synchronizes the VCXO, clock and frame pulse signals.

The VCXO circuits contain counters and other circuit components that allow the ESA processor to set up counters to create the required control voltage to enable the VCXO to sync to a received frame pulse. Software continuously monitors and logs the phase of this frame pulse. The information gathered by this continuous monitoring aligns the VCXO generated frame pulse to minimize phase hits. This action occurs on entry of an ESA mode.

Link control card

The next diagram displays the NT6X75EA in normal operation.

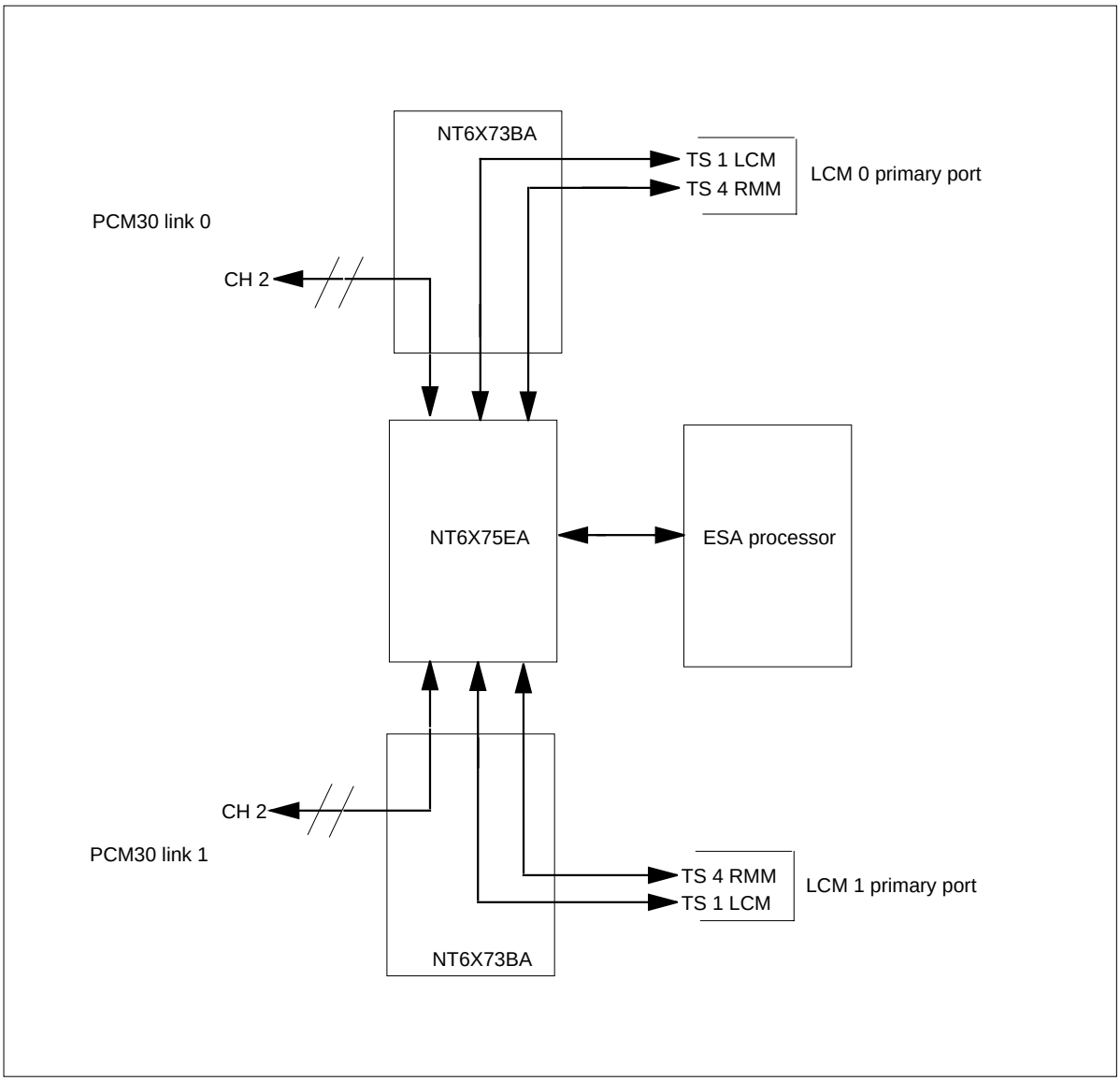
NT6X75EA message paths in normal mode



NT6X75EA (continued)

Under normal operation, an ESA uses time slot 3 (PCM30 channel 2) on PCM30 link 0 or 1 to host the DMS-X message channel. The next diagram displays the NT6X75EA in ESA mode.

NT6X75EA message paths in ESA mode



When the LCC is in ESA mode, time slot 1 from each LCM switches to the NT6X75EA from its normal PCM30 path. The ESA processor replaces the LGC as the host and the LCM continues to function as before.

Remote maintenance module

The RMM handles like the LCC in normal operation and in ESA mode. In ESA mode time slot 4 switches to the NT6X73BA circuit card. Time slot 4 provides a message channel to the RMM by way of the normal loop-around path in the LCM.

A-bus

The bus connections between the NT6X75EA circuit card and the ESA processor conform to the extended multi-processor system (XMS) A-Bus specification. The A-Bus terminates using balanced resistor network terminators, which ensure the integrity of the A-Bus under different environmental conditions.

Addressing

An address space of 32 bytes is in the NT6X75EA circuit card, using the five lowest order address bits. The NT6X75EA circuit card hardware and the ESA processor share the same bus for accessing messaging random access memory (RAM). An interlock prevents the ESA processor from interrupting with ordered hardware messaging operations.

Tones

A 64 kbit erasable programmable read-only memory (EPROM) stores tone samples for use during ESA. The eight maximum data lines store these tones in serial. The next table contains the tone allocation for the NT6X75EA circuit card.

Tone allocation

Lead	LCM port	Tone
Tone 0	7	Dial
Tone 1	1	Busy/reorder
Tone 2	4	Audible ringback
Tone 3	2	Receiver off-hook
Tone 4	5	P-phone ringing

NT6X75EA (continued)

The next table contains NT6X75EA tone frequencies and levels.

NT6X75EA tone frequencies and levels

Tone	Frequency (Hz)	Individual power (dBm)	Total power (dB)
Dial	350+	-13	-10
	440	-13	
Busy/reorder	480+	-13	-10
	620	-13	
Audible ringback	440+	-13	-10
	480	-13	
Receiver off-hook	1440+	-6	0.0
	2066+	-6	
	2466+	-6	
	2600	-6	
P-phone	516	-15	-15

Clock source

The NT6X75EA circuit card must operate in sync with the LCCs to transmit and receive message bytes. The clock sources are the LCCs. A multiplexer selects the C390 clock and FP48 multiframe pulse from one of the two LCCs. The clock source on the LCC is not appropriate for operation in ESA mode. The clock source on the LCC run 200 ppm above nominal frequency when the source of sync from the host is lost. The NT6X75EA circuit card contains an accurate VCXO clock to remedy this problem.

VCXO circuit

The VCXO circuit is followed by two sets of counters. One set of counters counts from 0 to 1279 before the signal VFP- resets the counter. VFP- is also sent to a D flip-flop that produces FP-ESA. FP-ESA is the frame pulse sent to the LCC, replacing the failed sync pulses from the PCM30 lines and becoming the system sync source.

The other set of counters load from a data bus. This second set of counters generate a frame pulse with a width variable from 1 to 1,280 97ns-wide clock pulses. The variable pulse generates by way of a low-pass filter an analog voltage that is applied to a 10.24-MHz VCXO.

Technical data

This section contains power requirements and signaling data for the NT6X75EA circuit card.

Power requirements

Power consumption for the NT6X75EA is 7.5 watts. Calculate the power consumption by multiplying the nominal voltage and current values from the next table.

Power specifications

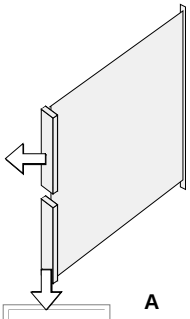
Parameter	Minimum	Nominal	Maximum	Units
Supply voltage	4.75	5.0	5.25	Volts
Supply noise		45		mV
Supply current	1.4	1.5	1.6	Amps

Signaling

The next table contains the backplane pin numbers for the NT6X75EA circuit card.

NT6X75EA (end)

NT6X75EA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	PWR+5V	PWR+5V
3A 3B	PWR+5V	PWR+5V
4A 4B	PWR+5V	PWR+5V
5A 5B	GND	GND
6A 6B	C390.0+	C390.1+
7A 7B	FP48.0	FP48.1–
8A 8B	OUTBYTE0	OUTBYTE1
9A 9B	HOSTESA0	HOSTESA1
10A 10B	FLCM0	FLCM1
11A 11B	ESA0	ESA1
12A 12B	DAS–	HSTCHEN1
13A 13B		HSTCHEN0
14A 14B	DTACK–	
15A 15B	UDS–	
16A 16B	WRT–	
17A 17B		
18A 18B	ESAIRQ–	
19A 19B	MODRST–	RSTOUT–
20A 20B	GND	
21A 21B		
22A 22B		ADDR06
23A 23B		ADDR07
24A 24B		ADDR08
25A 25B		ADDR09
26A 26B		ADDR10
27A 27B		
28A 28B		
29A 29B		
30A 30B		
31A 31B	ACTMON0	ACTMON1
32A 32B		ADDR01
33A 33B	TONE0	ADDR02
34A 34B	TONE1	ADDR03
35A 35B	TONE2	ADDR04
36A 36B	TONE3	ADDR05
37A 37B	TONE4	
38A 38B	TONE5	
39A 39B		
40A 40B	GND	GND

	A	B
41A 41B		
42A 42B		
43A 43B		
44A 44B		
45A 45B		
46A 46B		
47A 47B		
48A 48B		
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B	DATA00+	
58A 58B	DATA01+	
59A 59B	DATA02+	
60A 60B	DATA03+	ADDR11
61A 61B	DATA04+	GND
62A 62B	DATA05+	ADDR12
63A 63B	DATA06+	ADDR13
64A 64B	DATA07+	ADDR14
65A 65B		ADDR15
66A 66B		
67A 67B	DATA08+	
68A 68B	DATA09+	
69A 69B	DATA10+	ADDR16
70A 70B	DATA11+	ADDR17
71A 71B	DATA12	ADDR18
72A 72B	DATA13	ADDR19
73A 73B	DATA14	ADDR20
74A 74B	DATA15	ADDR21
75A 75B		FP-ESA
76A 76B	RECFP0	RECFP1
77A 77B		
78A 78B	GND	GND
79A 79B	ESAEN–	
80A 80B	GND	GND

NT6X75KA

Product description

The optional emergency stand alone (ESA) clock and tone circuit card (NT6X75KA) provides a clock and tone source for the international remote line concentrating module/outside plant module (IRLCM/OPM) equipped with ESA. The NT6X75KA circuit card also provides as an interface between the IRLCM pulse code modulation (PCM) message paths and the ESA processor. The NT6X75KA circuit card provides a frame pulse to replace the lost PCM30 frame pulse from the host.

The NT6X75KA circuit card is in the IRLCM/OPM host interface equipment (HIE). The NT6X75KA circuit card generates the clock signal for the PCM30 line group controller (PLGC) and PCM30 digital trunk controller (PDTC) processor, which enables the link control card (LCC) NT6X73BA to keep in sync. The NT6X75KA circuit card also provides the tones; dial, busy, reorder, receiver-off-hook, audible ringback and electronic business set ring-down required for ESA operation. During ESA the NT6X75KA circuit card communicates with both units of the PCM30 line concentrating module (ILCM) and remote maintenance module (RMM).

The NT6X75KA circuit card is for China only. Where reference occurs to the IRLCM in this document, the same information applies to the international outside plant cabinet (IOPAC). Where reference occurs to the PLGC in this document, the same information applies to the international line group controller (ILGC).

Functional description

The NT6X75KA circuit card provides the functions listed below, when its associated RLCM is in ESA mode:

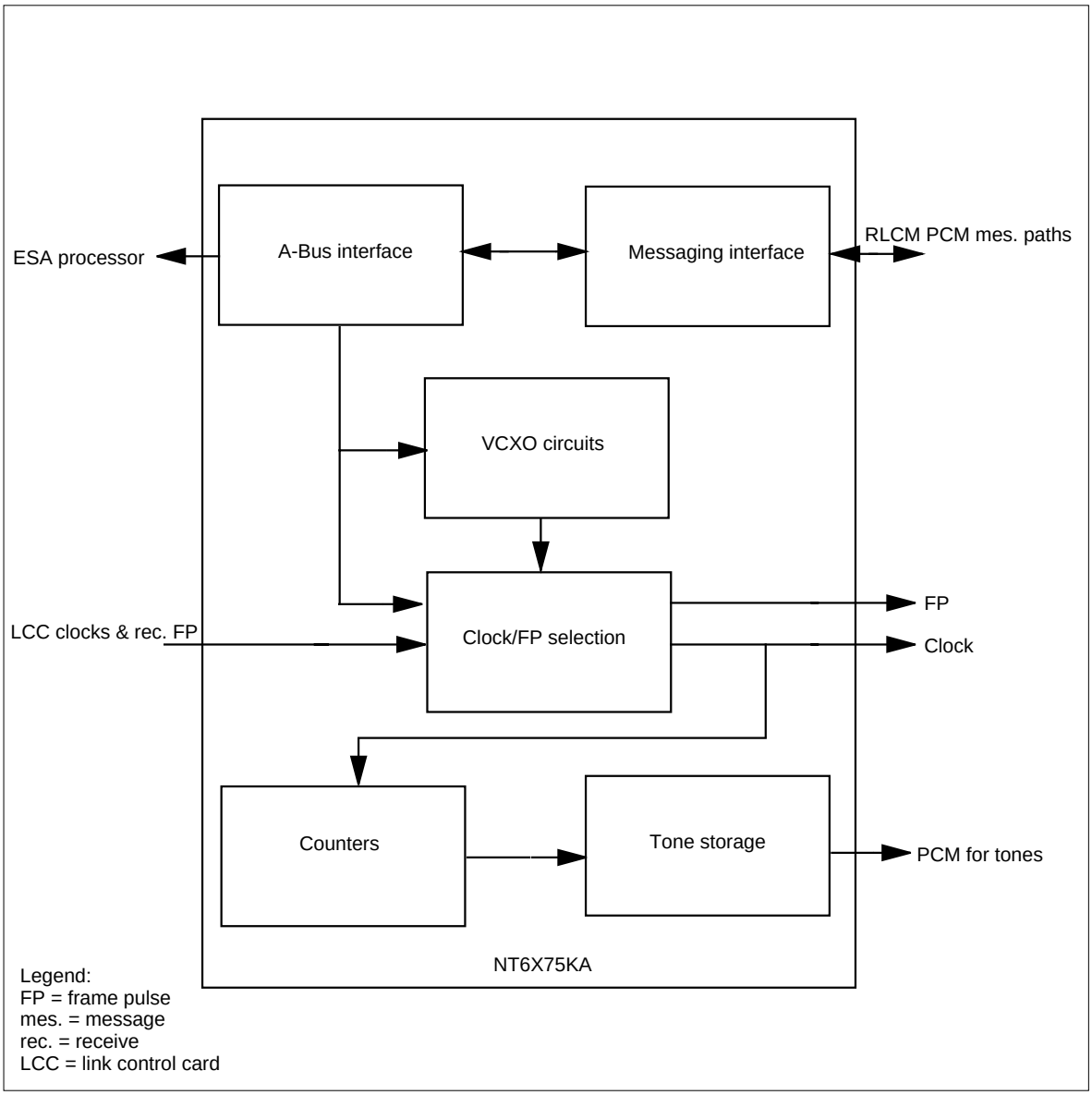
- clock sourcing
- tone sourcing
- interface between the IRLCM PCM message paths and the ESA processor

Block diagram

This section provides a block diagram that displays the major functional blocks of the NT6X75KA circuit card, with interconnecting busses and signals.

NT6X75KA (continued)

NT6X75KA functional block diagram



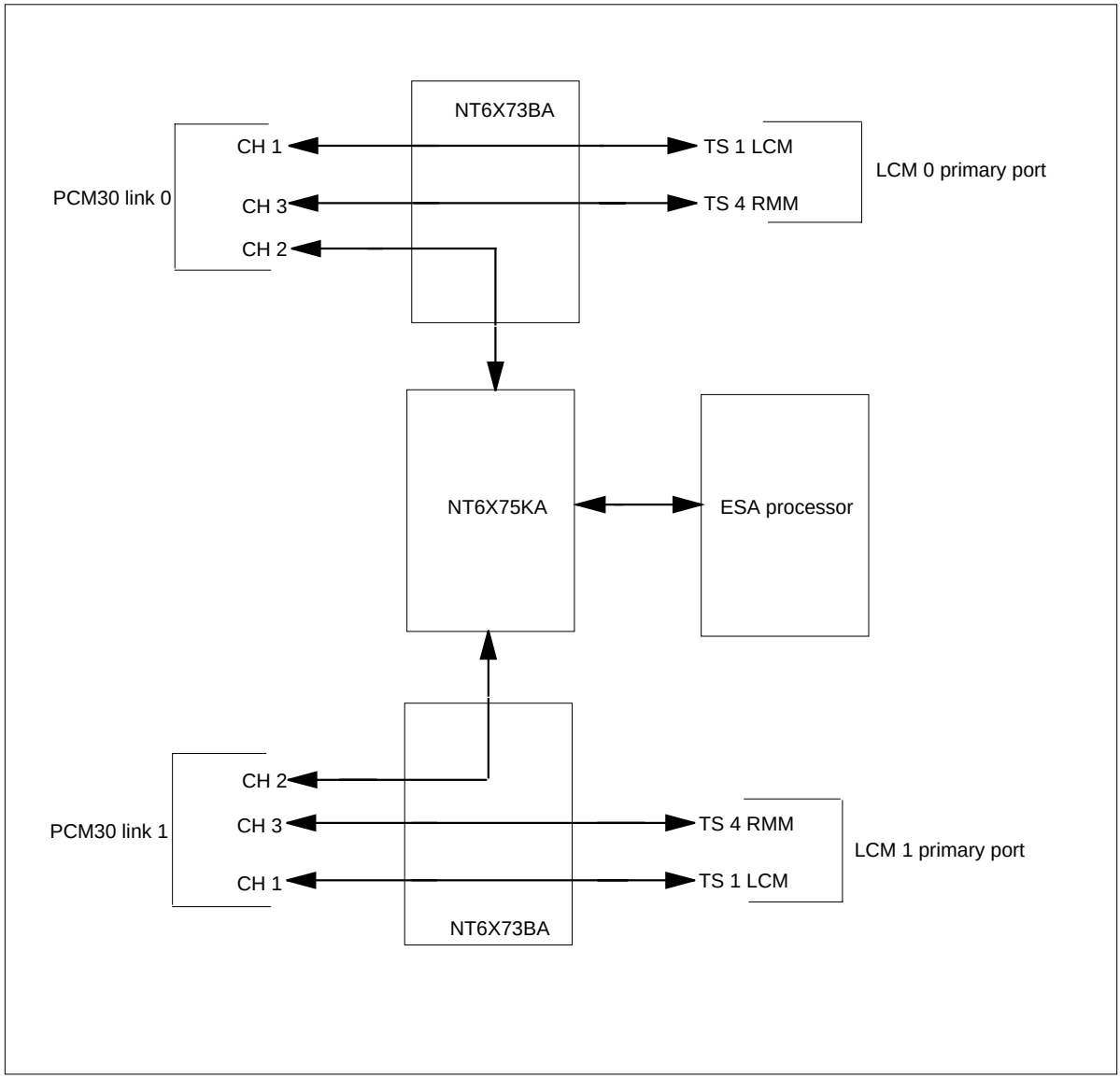
The NT6X75KA circuit card interfaces with the ESA processor in the ESA subsystem. This interface occurs through circuits on the NT6X75KA circuit card which conforms to the A-Bus standard. The ESA processor provides control information for adjusting the voltage controlled crystal oscillator (VCXO) and selection data for selecting the clock source which synchronizes the VCXO, clock and frame pulse signals.

The VCXO circuits contain counters and other circuit components that allow the ESA processor to set up counters to create the required control voltage to enable the VCXO to sync to a received frame pulse. Software continuously monitors and logs the phase of this frame pulse. The information gathered by this continuous monitoring aligns the VCXO generated frame pulse to minimize phase hits. This action occurs on entry of an ESA mode.

Link control card

The next diagram displays the NT6X75KA in normal operation.

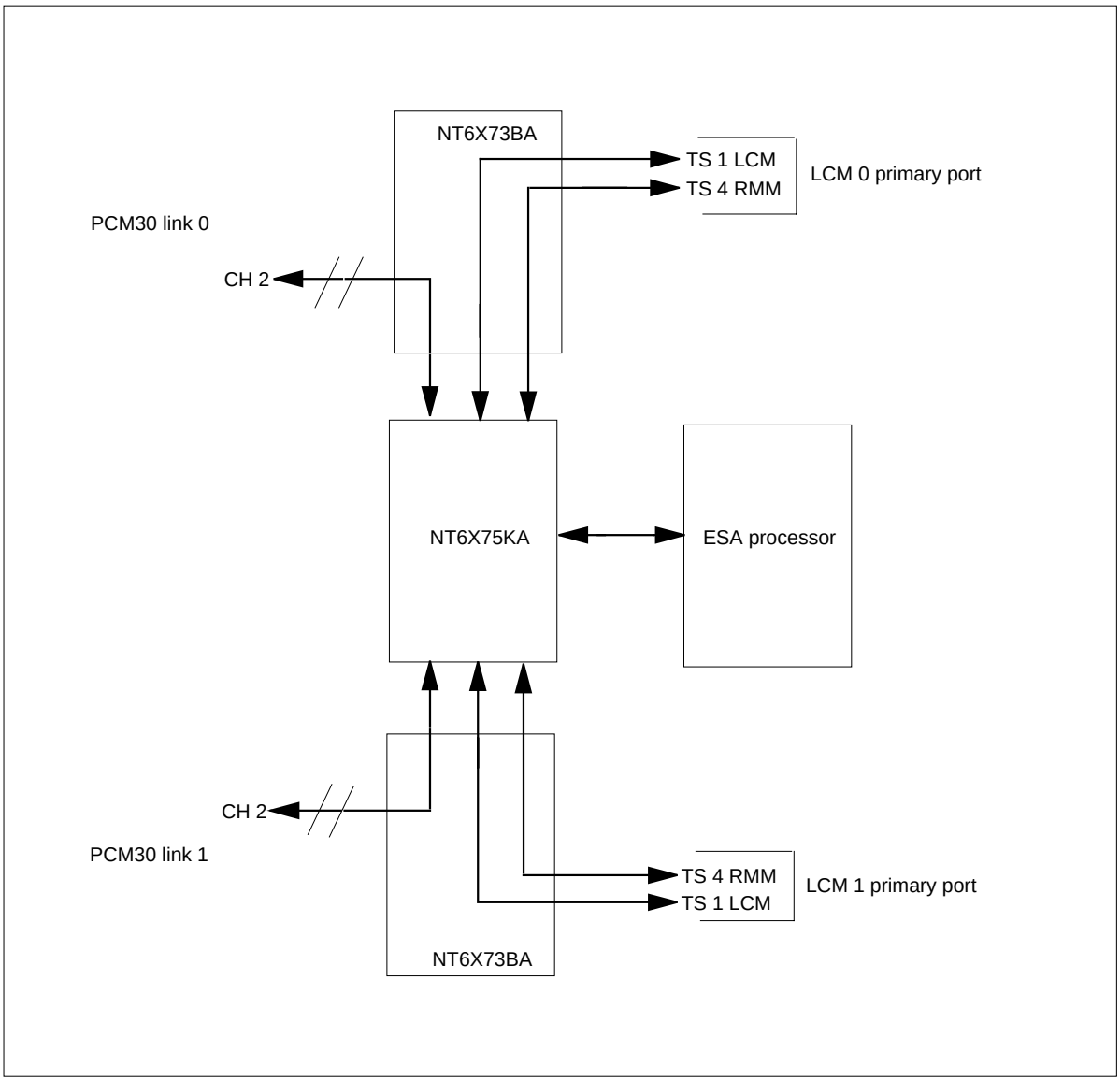
NT6X75KA message paths in normal mode



NT6X75KA (continued)

Under normal operation, an ESA uses time slot 3 (PCM30 channel 2) on PCM30 link 0 or 1 to host the DMS-X message channel. The next diagram displays the NT6X75KA in ESA mode.

NT6X75KA message paths in ESA mode



When the LCC is in ESA mode, time slot 1 from each LCM switches from its normal PCM30 path to the NT6X75KA. The ESA processor replaces the LGC as the host and the LCM continues to function as before.

Remote maintenance module

The RMM handles like to the LCC in normal operation and in ESA mode. In ESA mode time slot 4 switches to the NT6X73BA circuit card. Time slot 4 provides a message channel to the RMM by way of the normal loop-around path in the LCM.

A-bus

The bus connections between the NT6X75KA circuit card and the ESA processor conform to the extended multi-processor system (XMS) A-Bus specification. The A-Bust terminates using balanced resistor network terminators, which ensure the integrity of the A-Bus under different environmental conditions.

Addressing

An address space of 32 bytes is in the NT6X75KA circuit card, using the five lowest order address bits. The NT6X75KA circuit card hardware and the ESA processor share the same bus for accessing messaging random access memory (RAM). An interlock prevents the ESA processor from interrupting with ordered hardware messaging operations.

Tones

A 64 kbit erasable programmable read-only memory (EPROM) stores tone samples for use during ESA. The eight maximum data lines store these tones in serial. The next table contains the tone allocation for the NT6X75KA circuit card.

Tone allocation

Lead	LCM port	Tone
Tone 0	7	Dial
Tone 1	1	Busy/reorder
Tone 2	4	Audible ringback
Tone 3	2	Receiver off-hook
Tone 4	5	P-phone ringing

NT6X75KA (continued)

The next table contains NT6X75KA tone frequencies and levels.

NT6X75KA tone frequencies and levels

Tone	Frequency (Hz)	Individual power (dBm)	Total power (dB)
Dial	450	-10	-10
Busy/reorder	450	-10	-10
Audible ringback	450	-10	-10
Receiver off-hook	1440+	-6	0.0
	2066+	-6	
	2467+	-6	
	2600	-6	
P-phone	516+	0.0	0.0
	648	0.0	

Clock source

The NT6X75KA circuit card must operate in sync with the LCCs to transmit and receive message bytes. The clock sources are the LCCs. A multiplexer selects the C390 clock and FP48 multiframe pulse from one of the two LCCs. The clock source on the LCC is not appropriate for operation in ESA mode. The clock source on the LCC run 200 ppm above nominal frequency when the source of sync from the host is lost. The NT6X75KA circuit card contains an accurate VCXO clock to remedy this problem.

VCXO circuit

The VCXO circuit is followed by two sets of counters. One set of counters counts from 0 to 1279 before the signal VFP- resets the counter. VFP- is also sent to a D flip-flop that produces FP-ESA. FP-ESA is the frame pulse sent to the LCC, replacing the failed sync pulses from the PCM30 lines and becoming the system sync source.

The other set of counters load from a data bus. This second set of counters generate a frame pulse with a width variable from 1 to 1,280 97ns-wide clock pulses. The variable pulse generates by way of a low-pass filter an analog voltage that is applied to a 10.24-MHz VCXO.

Technical data

This section contains power requirements and signaling data for the NT6X75KA circuit card.

Power requirements

Power consumption for the NT6X75KA is 7.5 watts. Calculate the power consumption by multiplying the nominal voltage and current values from the next table.

Power specifications

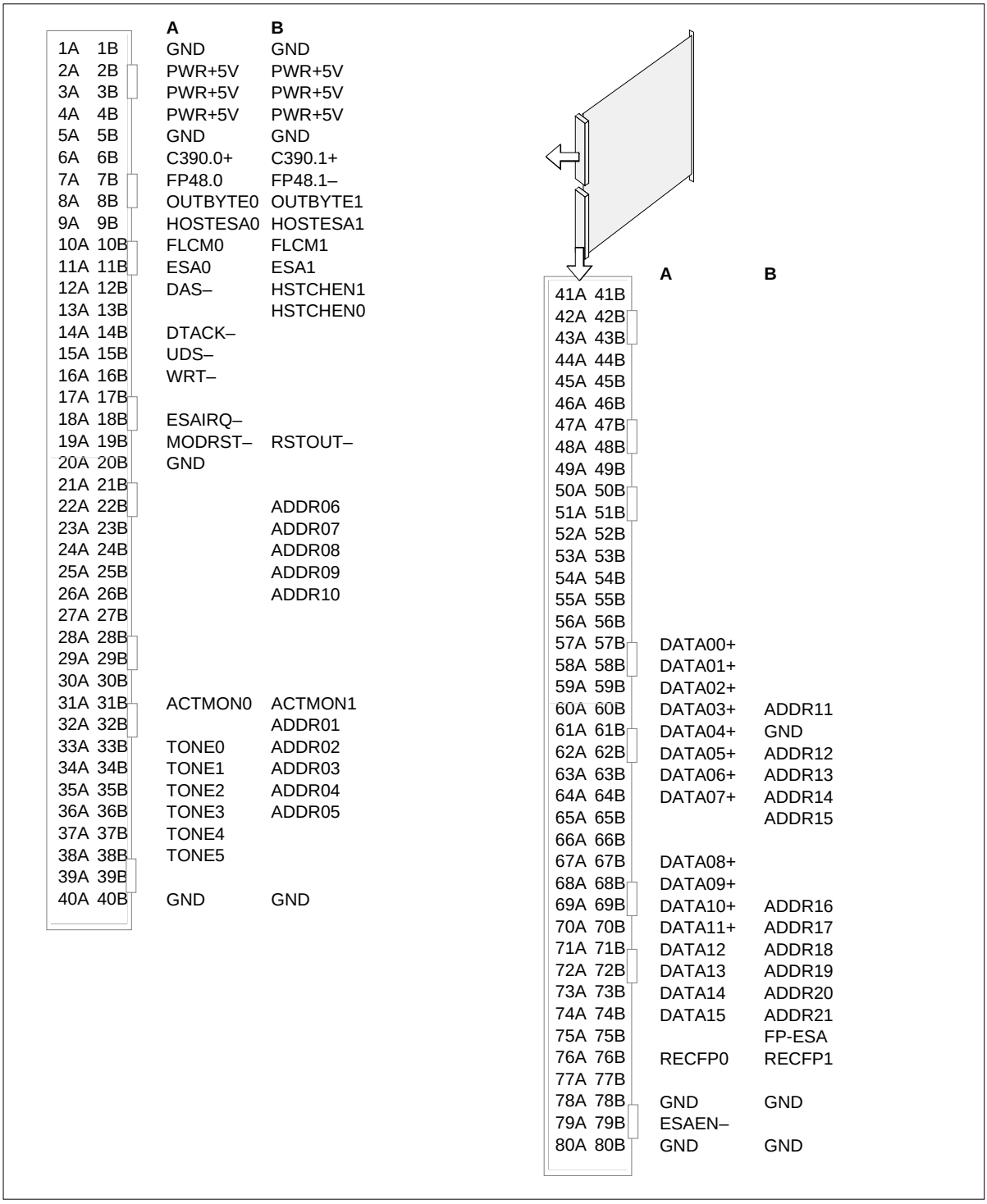
Parameter	Minimum	Nominal	Maximum	Units
Supply voltage	4.75	5.0	5.25	Volts
Supply noise		45		mV
Supply current	1.4	1.5	1.6	Amps

Signaling

The next table contains the backplane pin numbers for the NT6X75KA circuit card.

NT6X75KA (end)

NT6X75KA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	PWR+5V	PWR+5V
3A 3B	PWR+5V	PWR+5V
4A 4B	PWR+5V	PWR+5V
5A 5B	GND	GND
6A 6B	C390.0+	C390.1+
7A 7B	FP48.0	FP48.1–
8A 8B	OUTBYTE0	OUTBYTE1
9A 9B	HOSTESA0	HOSTESA1
10A 10B	FLCM0	FLCM1
11A 11B	ESA0	ESA1
12A 12B	DAS–	HSTCHEN1
13A 13B		HSTCHEN0
14A 14B	DTACK–	
15A 15B	UDS–	
16A 16B	WRT–	
17A 17B		
18A 18B	ESAIRQ–	
19A 19B	MODRST–	RSTOUT–
20A 20B	GND	
21A 21B		
22A 22B		ADDR06
23A 23B		ADDR07
24A 24B		ADDR08
25A 25B		ADDR09
26A 26B		ADDR10
27A 27B		
28A 28B		
29A 29B		
30A 30B		
31A 31B	ACTMON0	ACTMON1
32A 32B		ADDR01
33A 33B	TONE0	ADDR02
34A 34B	TONE1	ADDR03
35A 35B	TONE2	ADDR04
36A 36B	TONE3	ADDR05
37A 37B	TONE4	
38A 38B	TONE5	
39A 39B		
40A 40B	GND	GND

	A	B
41A 41B		
42A 42B		
43A 43B		
44A 44B		
45A 45B		
46A 46B		
47A 47B		
48A 48B		
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B	DATA00+	
58A 58B	DATA01+	
59A 59B	DATA02+	
60A 60B	DATA03+	ADDR11
61A 61B	DATA04+	GND
62A 62B	DATA05+	ADDR12
63A 63B	DATA06+	ADDR13
64A 64B	DATA07+	ADDR14
65A 65B		ADDR15
66A 66B		
67A 67B	DATA08+	
68A 68B	DATA09+	
69A 69B	DATA10+	ADDR16
70A 70B	DATA11+	ADDR17
71A 71B	DATA12	ADDR18
72A 72B	DATA13	ADDR19
73A 73B	DATA14	ADDR20
74A 74B	DATA15	ADDR21
75A 75B		FP-ESA
76A 76B	RECFP0	RECFP1
77A 77B		
78A 78B	GND	GND
79A 79B	ESAEN–	
80A 80B	GND	GND

NT6X76AA

Product description

The NT6X76AA asynchronous interface line card (AILC) provides an interface. The interface is between a four-wire RS-422 line and one channel of the 32-channel, 2.56-Mbps digital bit stream of the SL-100 private automatic branch exchange (PABX).

Data flow between the digital trunk controller (DTC) and the AILC is through an external asynchronous interface module (AIM). Data flow in this manner if the DTC is not compatible with the RS-422. Data flow is direct if the DTC conforms to RS-422 specifications.

Location

The card occupies two adjacent plug-in line circuit (LC) card positions in a line concentrating module (LCM) line drawer (LD).

Functional description

The NT6X76AA card receives and transfers transistor-transistor logic (TTL) and RS-422-compatible signals. The card receives and transfers signals between the RS-422 and the bus interface card (BIC). The card uses a relay circuit to perform internal testing and an enable signal to select the control format.

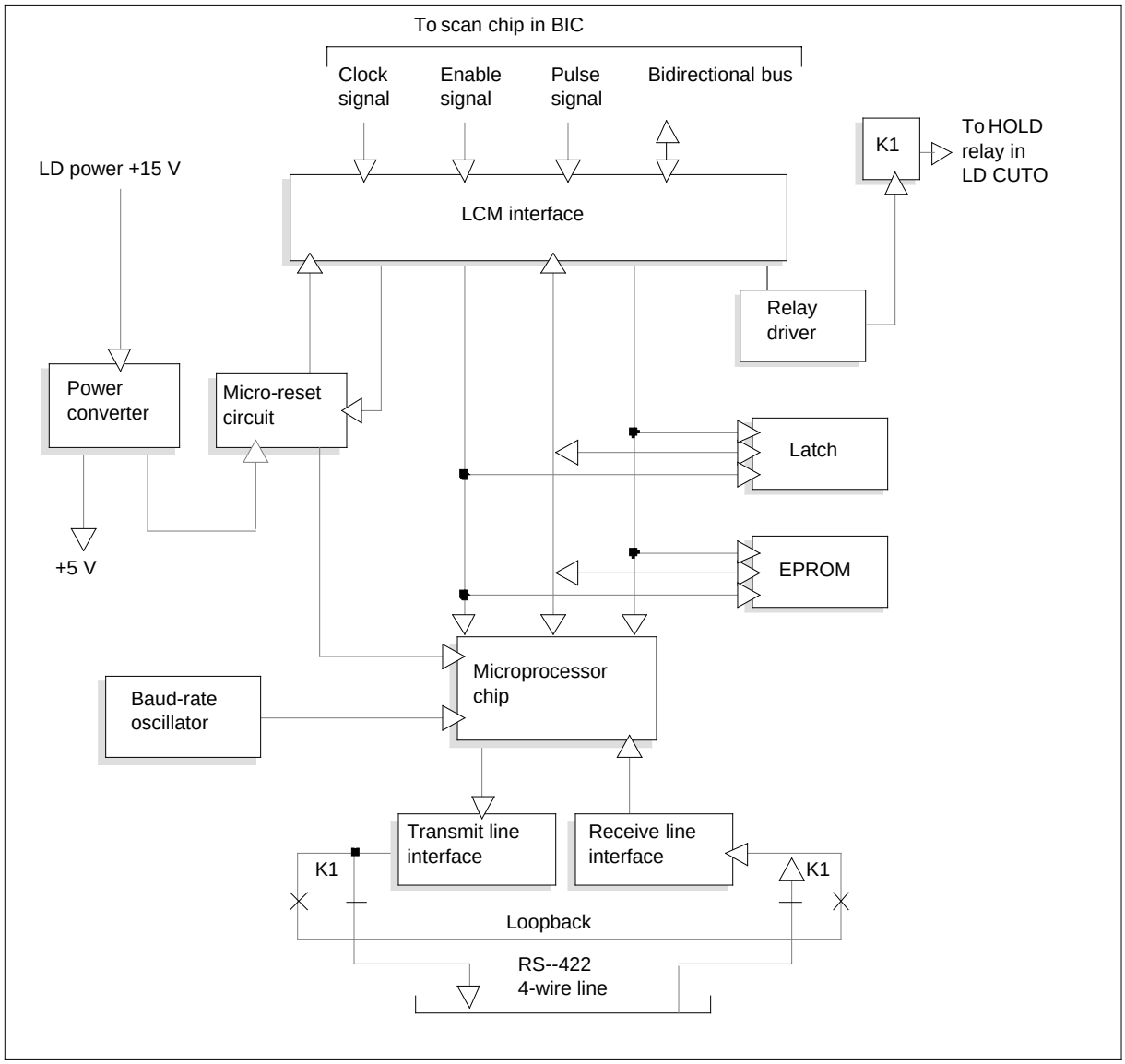
Functional blocks

The NT6X76AA card consists of the following functional blocks:

- LCM interface
- relay driver
- relay
- microprocessor chip
- EPROM
- latch
- baud-rate oscillator
- transmit line interface
- receive line interface
- power converter
- microreset circuit

NT6X76AA (continued)

NT6X76AA functional blocks



LCM interface

The LCM interface uses a bidirectional bus and an enable signal to control bidirectional data transmission. The enable signal selects a 0 for intelligent control or a 1 for nonintelligent control to choose the control format. The interface receives a 2.56-MHz clock signal to synchronize the AILC functions. The interface receives a 1-kHz master frame pulse to time AILC functions.

The LCM interface generates an address bus to carry a 15-bit address signal to address data that the EPROM stores. The LCM interface generates an address bus to access data in the latch and in the microprocessor chip. The interface also provides a cutover operating signal to the relay driver circuit.

Relay driver

The relay driver uses a cutover signal from the LCM interface to energize the relay circuit.

Relay

When the relay operates, the relay provides an analog loopback path for testing. The relay disconnects the line driver circuit from the transmit line interface. The driver connects to the corresponding input on the receive line interface. If the relay does not operate, the transmit and receive line interfaces connect to the tip (T) and ring (R) leads of the correct lines.

Microprocessor chip

The 80C31 microprocessor chip implements communications protocol between the microprocessor transmit and receive ports and the transmit and receive line interfaces. The chip manages the flow of PCM data and signaling messages between the LCM interface data bus and the universal asynchronous receiver-transmitter (UART). The chip uses a 12-MHz internal clock to maintain the flow of data and signaling messages.

EPROM

The uses signals and address information from the LCM interface EPROM to provide data storage and retrieval. The EPROM, which has a capacity of 8 or 16 Kbyte, is not active if the latch is addressed.

Latch

The latch accesses data in the LCM interface registers and responds to low-order address bits from the LCM interface. The latch is not active if the EPROM is addressed.

Baud-rate oscillator

The baud-rate oscillator provides crystal-controlled drive signals to the microprocessor to generate a baud-rate clock pulse for the UART.

Transmit line interface

The transmit line interface receives TTL data from the microprocessor. The transmit line applies the data to a line driver circuit that converts the data to RS-422 line specifications.

NT6X76AA (continued)

The interface works with the relay to provide an analog loopback path for testing. Safety circuits protect the interface from damage. Transient voltages and currents on the T and R leads can cause damage. The transmit line interface is active when the microprocessor sends the correct signal.

Receive line interface

The receive line interface receives RS-422-compatible data. The receive line interface applies the data to a line receiver circuit. The line receiver circuit converts the data to TTL format and sends the data to the microprocessor.

The interface works with the relay to provide an analog loopback path for testing. Safety circuits protect the interface from damage. Transient voltages and currents on the T and R leads can cause damage. The receive line interface is active when the microprocessor sends the correct signal.

Power converter

The power converter receives a +15V supply from the LD. The power converter converts the voltage to a regulated, filtered +5V supply for critical applications in the AILC.

Microreset circuit

The microreset circuit monitors the +5V output from the power converter. The circuit resets the microprocessor and initializes the LCM interface when the +5V output rises during power-up.

The circuit also monitors for a reset signal that the LCM originates. The reset signal appears on the bidirectional bus. If this signal is present, the circuit initiates a reset.

Technical data

The NT6X76AA card has a baud-rate oscillator frequency of 307.2 kHz ±5%. The card a RS-422 line transmission distance of 1200 m (4000 ft) for rates of a maximum of 19.2 Kbps.

The LCM interface characteristics appear in the following table.

LC interface characteristics (Sheet 1 of 2)

Characteristics	Value
Clock signal	2.56 MHz
Synchronization	1 kHz
Enable control type	0 = intelligent, 1 = nonintelligent

LC interface characteristics (Sheet 2 of 2)

Characteristics	Value
Data bus synchronization to clock	
Transmission rate	64 kbps
Data transmission structure	
Start	1 bit
Mode (0 = PCM, 1 = signaling)	1 bit
Data (from LCM)	8 bits
Delay for bidirectional bus reversal	$^1/_2$ bits
Data (to LCM)	8 bits
Supervision (buffer full)	1 bit
Supervision (data ready)	1 bit

The line interface characteristics appear in the following table.

Line interface characteristics

Characteristic	Value
Termination impedance	100 Ω
Differential signal voltage	5 V peak to peak
Driver type (transmit line interface)	26LS31
Receiver type (receive line interface)	26LS32
Data type	ASCII
Signal format	Asynchronous, start-stop
Number of bits	8 (7 + parity)
Parity	Mark, space odd or even
Data rates	
2 stop bits	110 bps
1 stop bit	150, 300, 600, 1200
	2400, 4800, 9600, 19,200 bps

NT6X76AA (end)

Physical dimensions

The physical dimensions of the

card are:

- height: 152 mm (6 in.)
- depth: 89 mm (3.5 in.)
- width: 20 mm (0.8 in.)

Power requirements

The power requirements for the appear in the following table.

Power requirements

	Voltage	Current
From LD	+15 V	20 mA
From power converter	+5 V	170 mA

NT6X76AC

Product description

The asynchronous interface line card (AILC) NT6X76AC is a Datapath product. The NT6X76AC card provides a circuit switched data facility on the DMS/SL-100. The use of the AILC is enhanced from the original AILC (NT6X76AA) for use in the DMS integrated access local area network (DiaLAN) service. The DiaLAN service provides integrated voice and data access to the DMS/SL-100 over current voice lines.

The AILC forms part of a facility that provides circuit-switched data on a DMS/SL-100 central office switch. The AILC provides a four-wire, RS-422 compatible interface. The AILC can be used with an RS-422 to RS-232 signal converter. This card can interface RS-232 compatible data terminal equipment (DTE) to the DMS. If the DTE is RS-422 compatible, the signal converter is not required. You can connect the four-wire line directly to the DTE.

Location

The AILC operates in a line concentrating module (LCM) line card drawer of the DMS. The bus interface card (BIC) provides an interface between the AICL and the LCM. A four-wire line provides an interface between AILC and the DTE of the user. The AILC occupies a double line card slot.

Functional description

The AILC provides an interface between the DTE of the user and the DMS switch. The AILC line interface provides asynchronous data transmission at bit rates that range from 110 bit/s to 19.2 Kbit/s. The AILC data facility represents a cost-reduced version of a data line card (DLC) data unit (DU) data facility with limited feature capabilities.

The NT6X76AC is functionally equivalent to the original AILC (NT6X76AA) with the following additional features:

- a Datapath closed user group
- an idle time-out for call disconnection
- DiaLAN system maintenance

The AILC keyboard dialing firmware provides the following features to the user:

- call origination to local host
- auto dialing capability for calls to local hosts
- speed call calling
- resource calling (modem pooling)

NT6X76AC (continued)

- ring again capability
- termination of incoming calls

Functional blocks

The NT6X76AC consists of four functional blocks:

- the line interface
- the LCM interface
- the microprocessor subsystem
- the power converter circuits

Line interface

The line interface consists of the following:

- an RS-422 line driver and a line receiver
- zener diodes and resistors to protect against line transient
- a 4-Form-C cutover relay
- relay driver circuits

Line concentrating module interface

The LCM interface consists of the R28 custom LSI chip that interfaces directly to the BIC.

Microprocessor subsystem

The microprocessor subsystem provides the intelligence on the AILC. The microprocessor subsystem consists of the following components:

- an 80C51FA microprocessor (like RAM)
- timers
- a universal asynchronous receiver/transmitter (UART))
- a 27C64 8-Kbyte EPROM
- a discrete baud-rate oscillator
- power-up reset ability
- associated circuits

Power converter subsystem

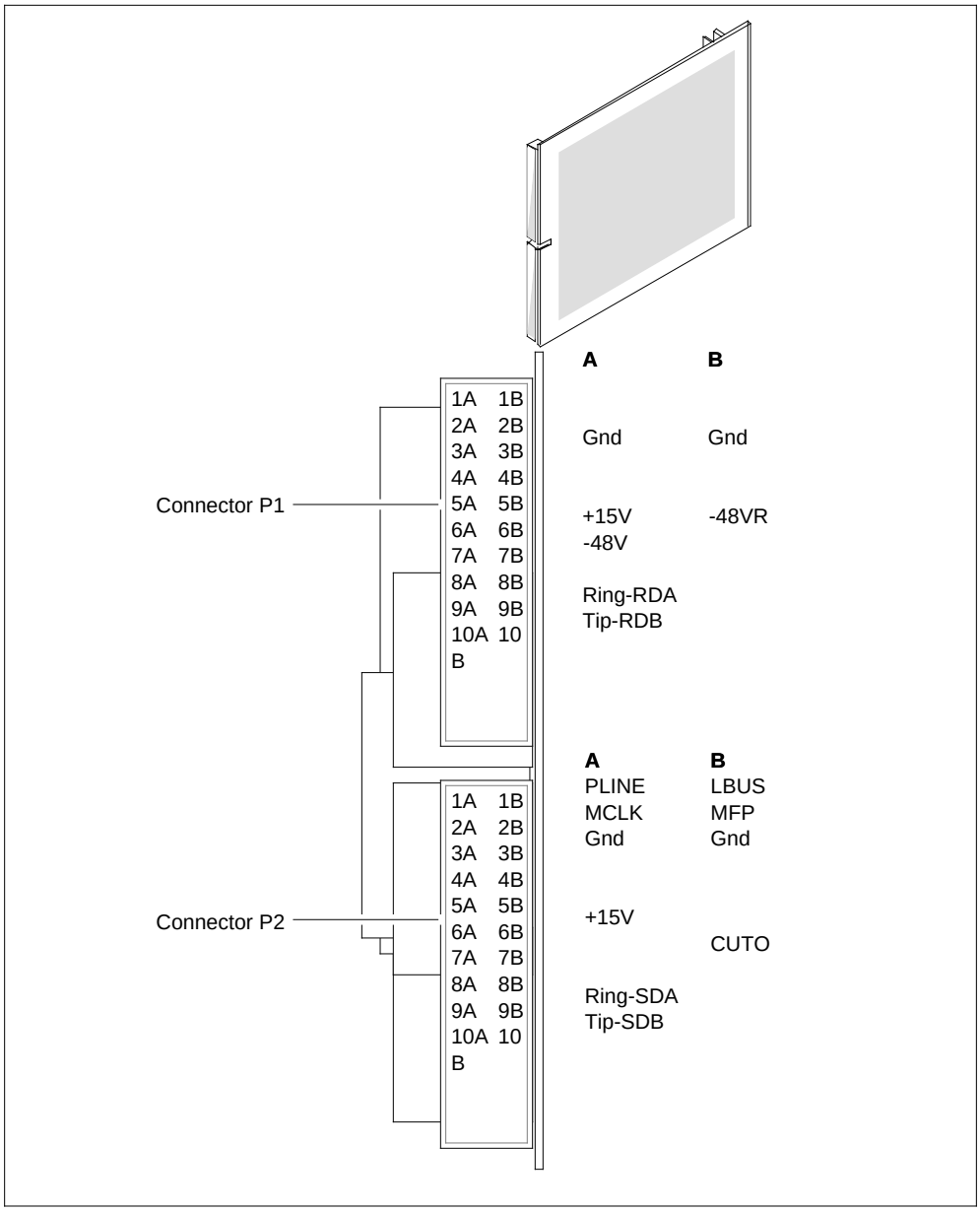
The power converter subsystem consists of the 15V to 5V integrated switching power converter. The integrated switching power converter has decoupling capacitors at the 15V input and at the 5V output.

Signaling

Pin numbers

The pin numbers for NT6X76AC appear in the following figure.

NT6X76AC pin numbers



NT6X76AC (end)

Technical data

Physical characteristics

The AILC is a single card with approximate dimensions of 90 mm (3.54 in.) by 150 mm (5.91 in.). The AILC occupies a double-slot position in the LCM line drawer. The AILC follows the mechanical specifications that the common features drawing of the LCM line card for 2-slot line cards defines.

Power requirements

The approximate power requirements for the AILC with complimentary metal oxide semiconductor (CMOS) components are:

- 170mA at +5V when the 80C51FA processor on the AILC runs. This requirement is reduced to 155mA when the processor is placed in the idle mode.
- 20mA at +15V when the cutover relay operates. This requirement can be reduced to approximately 7mA during cutover, and is 0mA when the relay is in a normal released state.

Operating characteristics

The AILC can transmit and receive data through the four-wire line and the optional RS-422 signal converter. The DTEs have the following characteristics:

- the data type is ASCII
- the signal format is asynchronous, start-stop
- 8 bits that include parity bit, or 7 bits plus parity bit
- the parity is mark, space, odd or even
- the data rates are 110, 150, 300, 600, 1200, 2400, 4800, 9600, and 19 200 bit/s
- the stop bits are 2 stop bits for 110 bps, 1 stop bit for all other speeds
- the clock is internal, ± 1% frequency tolerance

NT6X76AD

Product description

The Hayes-supported asynchronous interface line card (AILC) NT6X76AD is a Datapath product. The NT6X76AD card provides a circuit switched data facility on the DMS SL-100. The NT6X76AC was upgraded to add the Hayes command set. The Hayes command set is required for DiaLAN applications in the United States. The AILC is used in the DMS integrated access local area network (DiaLAN) service. The DiaLAN service provides integrated voice and data access to the DMS SL-100 over voice lines.

The AILC forms part of a facility that provides circuit switched data on a DMS SL-100 central office switch. The AILC provides a four-wire, RS-422 compatible interface. Use the AILC with an RS-422 to RS-232 signal converter. Use this unit to interface RS-232 compatible data terminal equipment to the DMS switch. If the data terminal equipment is RS-422 compatible, the signal converter is not required. The four-wire line can connect directly to the data terminal equipment.

Location

The AILC operates in a line concentrating module line card drawer of the DMS switch. The AILC interfaces to the line concentrating module through the drawer-level bus interface card. The AILC interfaces to the user data terminal equipment through a four-wire line. The AILC occupies a double line card slot.

Functional description

The NT6X76AD is an interface between the data terminal equipment of the user and the DMS switch. The NT6X76AD provides asynchronous data transmission at bit-rates that range from 110 bit/s to 19.2 kbit/s. The NT6X76AD is a cost-reduced version of a combined data line card and data unit with limited feature capabilities.

The NT6X76AD is functionally equivalent to the NT6X76AC with the following additional features:

- support of Hayes command set
- increased static memory

The AILC NT symbolic keyboard dialing firmware provides the following features:

- call origination to local host
- auto dialing capability for calls to local hosts
- speed call calling

NT6X76AD (continued)

- resource calling (modem pooling)
- ring again capability
- termination of incoming calls

Functional blocks

The NT6X76AD consists of four functional blocks:

- line interface
- line concentrating module interface
- microprocessor subsystem
- power converter circuits

Line interface

The line interface consists of:

- RS-422 line driver and a line receiver
- zener diodes and resistors to protect against line transients
- 4-Form-C cutover relay
- relay driver circuits

Line concentrating module interface

The LCM interface consists of the R28 custom LSI chip that interfaces directly to the bus interface card.

Microprocessor subsystem

The microprocessor subsystem provides the intelligence on the AILC. The microprocessor subsystem consists of:

- 80C528 microprocessor with 512 bytes of RAM
- timers
- universal asynchronous receiver-transmitter
- 27C64 32-kbyte EPROM
- discrete baud-rate oscillator
- power-up reset
- associated circuits

Power converter subsystem

The power converter subsystem consists of the 15-V to 5-V integrated switching power converter, with decoupling capacitors. The decoupling capacitors are at the 15-V input and at the 5-V output.

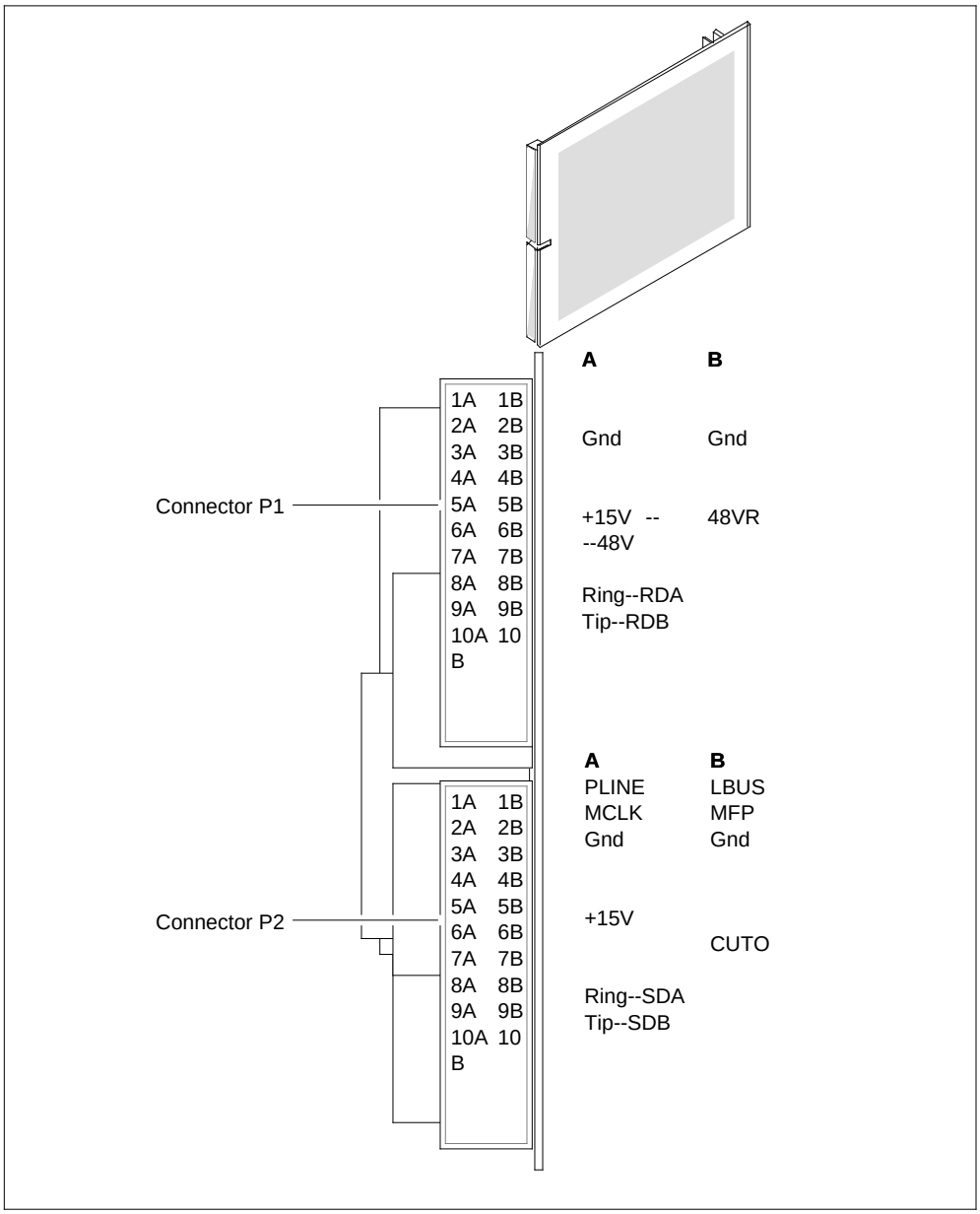
Signaling

Pin numbers

The pin numbers for NT6X76AD appear in the following figure.

NT6X76AD (continued)

NT6X76AD pin numbers



Technical data

Physical characteristics

The NT6X76AD is approximately 90 mm by 150 mm. The NT6X76AD occupies a double-slot position in the line concentrating module line drawer. The AILC follows the mechanical specifications that the line concentrating module line card common features drawing for two-slot line cards defines.

Power requirements

The approximate power requirements for the AILC with metal oxide semiconductor (CMOS) components are:

- 170 mA at +5 V when the 80C528 processor on the AILC is running. This requirement is reduced to 155 mA when the processor is in the idle mode.
- 20 mA at +15 V when the cutover relay operates. This requirement can be reduced to approximately 7 mA during cutover. This requirement is 0 mA when the relay is in a normal released state.

Operating characteristics

The NT6X76AD transmits and receives data through the four-wire line and optional RS-422 signal converter. The data terminal equipment has the following characteristics:

- data type: ASCII
- signal format: asynchronous, start-stop
- 8 bits that include parity bit, or 7 bits plus parity bit
- parity: mark, space, odd or even
- data rates: 110, 150, 300, 600, 1200, 2400, 4800, 9600, and 19 200 bps
- stop bits: 2 stop bits for 110 bps, 1 stop bit for all other speeds
- clock: internal, ± 1% frequency tolerance

NT6X78AA

Product description

The NT6X78AA custom local area signaling service (CLASS) modem resource (CMR) card resides in the extended multiprocessor system (XMS)-based peripheral module (XPM) of the DMS/SL-100. This card plugs into a spare slot of the XPM. This card has direct access to the address bus (A-bus) of the XPM signaling processor (SP). This card also has access to the pulse code modulation (PCM) speech bus. The card accommodates 32 transmit-only modem resources and 32 ring-detector resources. The resources connect to specific PCM channels at specified times under software control.

Functional description

The CMR card implements the calling number delivery (CND) feature. The card generates PCM samples of the 202 modem signals according to messaging from the XPM signaling processor (SP). The system passes these samples to the plain ordinary telephone service (POTS) line card in the line concentrating module (LCM). The system converts the samples to analog modem signals and sends the samples along the loop to the CLASS subscriber. The CMR card identifies the ringing intervals on the subscriber loops to determine when to transmit the modem signals.

Compatibility

The CMR card is compatible with DMS software loads from BCS27 or higher.

Functional blocks

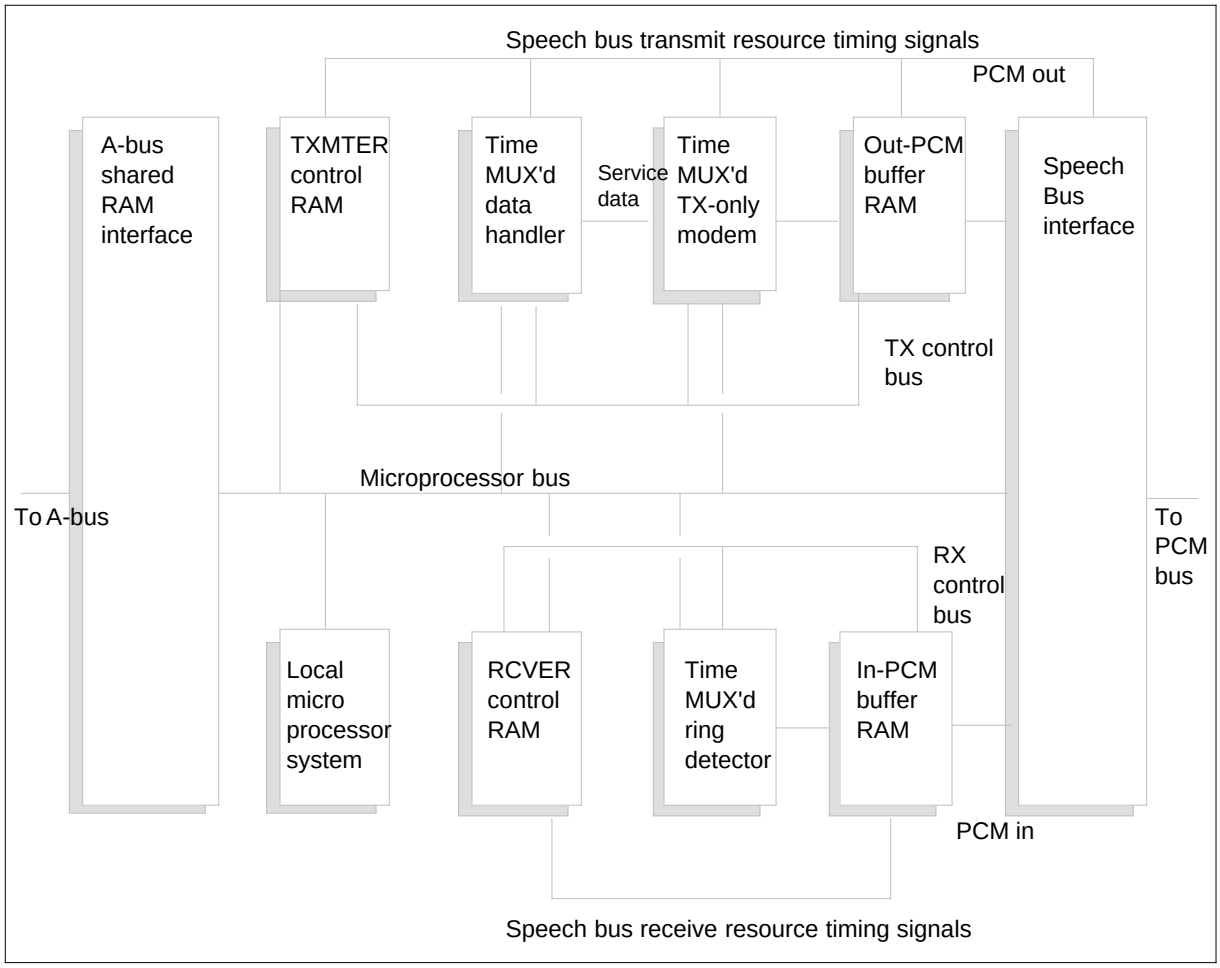
The NT6X78AA consists of the following functional blocks:

- A-bus shared RAM interface
- local microprocessor subsystem
- transmitter control RAM
- receiver control RAM
- time-multiplexed data handler
- time-multiplexed transmit-only modem
- outgoing PCM buffer RAM
- speech bus interface
- incoming PCM buffer RAM
- time-multiplexed ringing detector

The functional relationship between these blocks appears in the following figure.

NT6X78AA (continued)

NT6X78AA functional blocks



A-bus shared RAM interface

The A-bus shared RAM interface is the communications interface between the XPM signaling processor and the CMR card.

Local microprocessor subsystem

The local microprocessor subsystem handles the messaging protocol with, for example, the SP, CND, diagnostics, and supervision of card resources.

Transmitter control RAM

The transmitter control RAM provides storage for control, data, and status information for the other subsystems that connect to the transmit control bus. The transmitter control RAM is accessible by the local processor.

NT6X78AA (continued)

Receiver control RAM

The receiver control RAM provides storage for control and status information for the other subsystems that connect to the receive control bus. The receiver control RAM is accessible by the local processor.

Time-multiplexed data handler

The time-multiplexed data handler provides a universal asynchronous receiver/transmitter (UART) transmit function, with the capability of multiple transmissions of the same character.

Time-multiplexed transmit-only modem

The time-multiplexed transmit-only modem uses a table of sample values to convert the serial binary data output of the data handler. The modem converts the output to PCM samples of a 202 modem signal. The ROM stores the sample values.

Outgoing pulse code modulation buffer RAM

The outgoing PCM buffer RAM facilitates the transmission of the PCM samples from the modem to a speech bus port and channel. The PCM buffer RAM performs a 32-in-to-640-out time switch function.

Speech bus interface

The speech bus interface interacts with the upstream and downstream parallel PCM signals on the speech bus. The speech bus interface generates correct timing signals for the transmit and receive subsystem.

Incoming PCM buffer RAM

The incoming PCM buffer RAM provides the capability to choose 32 out of 640 incoming 64-Kbps PCM streams. The PCM buffer uses the PCM streams to perform ringing detection.

Time-multiplexed ringing detector

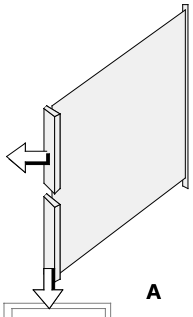
The time-multiplexed ringing detector detects the instances of ringing on a particular subscriber loop. The detection of ringing helps to establish when to send the CND message.

Signaling

Pin numbers

The pin numbers for the NT6X78AA appear in the following table.

NT6X78AA pin numbers



	A	B
1A 1B	Gnd	Gnd
2A 2B	+5 V	+5 V
3A 3B	+5 V	+5 V
4A 4B	+5 V	+5 V
5A 5B	Gnd	Gnd
6A 6B	FP-	C97+
7A 7B		
8A 8B		
9A 9B		
10A 10B		
11A 11B		
12A 12B	DAS-	
13A 13B	LDS-	
14A 14B	SPDTACK-	
15A 15B	UDS-	
16A 16B	WRT-	
17A 17B		
18A 18B	RST.IN	
19A 19B		
20A 20B		
21A 21B	PCMIN0	PCMOUT0
22A 22B	PCMIN1	PCMOUT1
23A 23B	PCMIN2	PCMOUT2
24A 24B	PCMIN3	PCMOUT3
25A 25B	PCMIN4	PCMOUT4
26A 26B	PCMIN5	PCMOUT5
27A 27B	PCMIN6	PCMOUT6
28A 28B	PCMIN7	PCMOUT7
29A 29B	ADDR01+	
30A 30B	ADDR02+	
31A 31B	ADDR03+	
32A 32B	ADDR04+	
33A 33B	ADDR05+	
34A 34B		
35A 35B	ADDR06+	
36A 36B	ADDR07+	
37A 37B	ADDR08+	
38A 38B	ADDR09+	*D0
39A 39B	ADDR10+	*D1
40A 40B	ADDR11+	*D2

*Paddle board interface pin

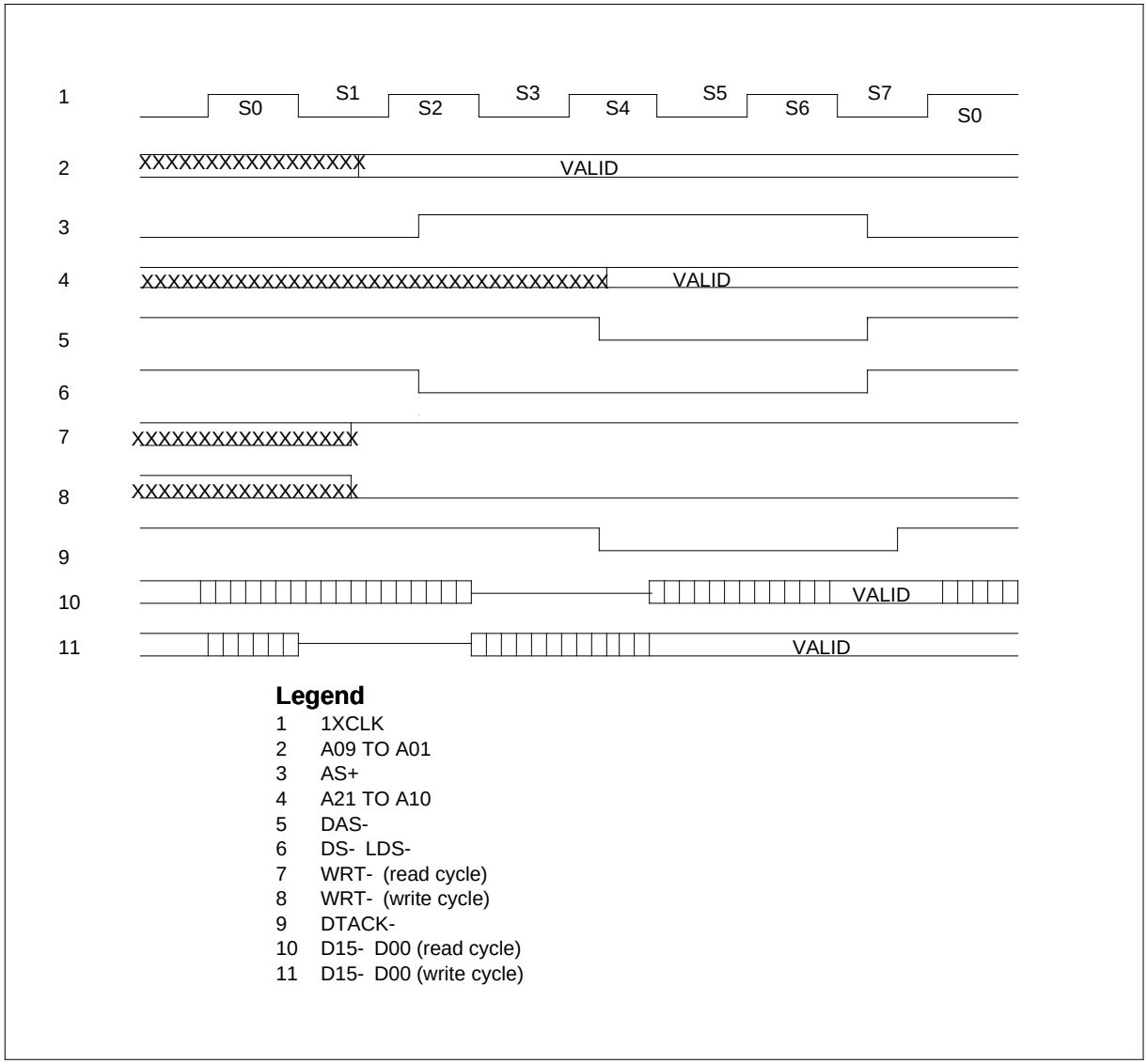
	A	B
41A 41B		*D3
42A 42B	ADDR12+	*D4
43A 43B	ADDR13+	*D5
44A 44B	ADDR14+	*D6
45A 45B		*D7
46A 46B	*	R/W-
47A 47B	ADDR17+	*SETPAD-
48A 48B	ADDR18+	POS0
49A 49B	ADDR19+	POS1
50A 50B	ADDR20+	POS2
51A 51B	ADDR21+	*HXCS-
52A 52B	SEN0	*USARCS-
53A 53B	SEN1	
54A 54B	SEN2	
55A 55B		
56A 56B		*A1
57A 57B		*A2
58A 58B		
59A 59B		
60A 60B		
61A 61B		
62A 62B		*UARACK-
63A 63B		
64A 64B		
65A 65B		
66A 66B		*UARINT-
67A 67B	DATA08	*RESET-
68A 68B	DATA09	*ENPB
69A 69B	DATA10	
70A 70B	DATA11	
71A 71B	DATA12	
72A 72B	DATA13	
73A 73B	DATA14	
74A 74B	DATA15	
75A 75B		
76A 76B		
77A 77B		
78A 78B	Gnd	Gnd
79A 79B		
80A 80B	Gnd	Gnd

NT6X78AA (continued)

Timing

The timing for the NT6X78AA A-bus signals appears in the following figure.

NT6X78AA timing of A-bus signals



Legend

1 1XCLK
2 A09 TO A01
3 AS+
4 A21 TO A10
5 DAS-
6 DS- LDS-
7 WRT- (read cycle)
8 WRT- (write cycle)
9 DTACK-
10 D15- D00 (read cycle)
11 D15- D00 (write cycle)

Technical data

Physical characteristics

The CMR card resides in the XPM of the DMS/SL-100. This card plugs into a spare slot of the XPM. This card has direct access to the A-bus of the XPM signaling processor (SP) and the PCM speech bus. The card accommodates 32

transmit-only resources and 32 ring-detector resources. These resources connect to specified PCM channels at specified times under software control.

A standard DMS-size multi-layered circuit board accommodates the circuits of the CMR card. Standard through-hole components are used. This card does not have light-emitting diodes (LED). This card has a standard blank faceplate with the product engineering code (PEC) information.

The CMR card is the only hardware component required to implement the calling number delivery (CND) function on the DMS/SL-100.

Power requirements

The power requirements of the CMR card are approximately 5 A at +5V (average of typical and maximum). The XPM shelf supply provides 50A at +5V for each card in the shelf.

NT6X78AB

Product description

The NT6X78AB custom local area signaling services (CLASS) modem resource (CMR) card replaces the NT6X78AA version in every application. This card provides different CLASS features, like calling number delivery (CND). The CND uses a voiceband data link to supply network information to the user.

Location

The NT6X78AB is in the extended multiprocessor system (XMS) peripheral module (XPM) of the DMS–100. The NT6X78AB plugs into a spare card slot of the XPM.

Functional description

The NT6X78AB card generates pulse code modulation (PCM) samples of 202 modem signals to implement the CND feature. The PCM samples are based on messaging from the XPM signaling processor. The system passes the PCM samples to the plain old telephone service (POTS) line card in the line concentrating module (LCM). In the LCM, the samples convert to analog voiceband modem signals. After the LCM, the system sends the samples to the CLASS subscriber.

The NT6X78AB card uses four application–specific integrated circuits (ASICS) to embed most of the circuitry. This arrangement eliminates the use of almost every programmable array logic (PAL) blocks of the previous version. One PAL block remains. This new version does not support a paddleboard interface.

Functional blocks

The NT6X78AB contains the following functional blocks:

- an A–bus shared random access memory (RAM) interface
- local microprocessor subsystem
- speech–bus interface
- a PCM receive section
- a PCM transmit section

The A–bus shared RAM interface

The A–bus shared RAM interface is the communication interface between the XPM signaling processor and the CMR card.

Local microprocessor subsystem

The microprocessor subsystem performs the following processing functions of the CMR card:

- messaging protocol with the signaling processor and the CND feature
- diagnostics
- supervision of card resources

Speech–bus interface

The speech–bus interface interacts with the parallel PCM signals on the XPM speech bus. The speech–bus interface generates timing signals for the PCM transmit and PCM receive sections.

The PCM receive section

The PCM receive section provides 32 receive resources that identify the instances of ringing on selected subscriber lines. To identify ringing, the receive resources use the PCM receive stream on specified speech–bus time slots. This operation establishes the times when the system can send the CND message.

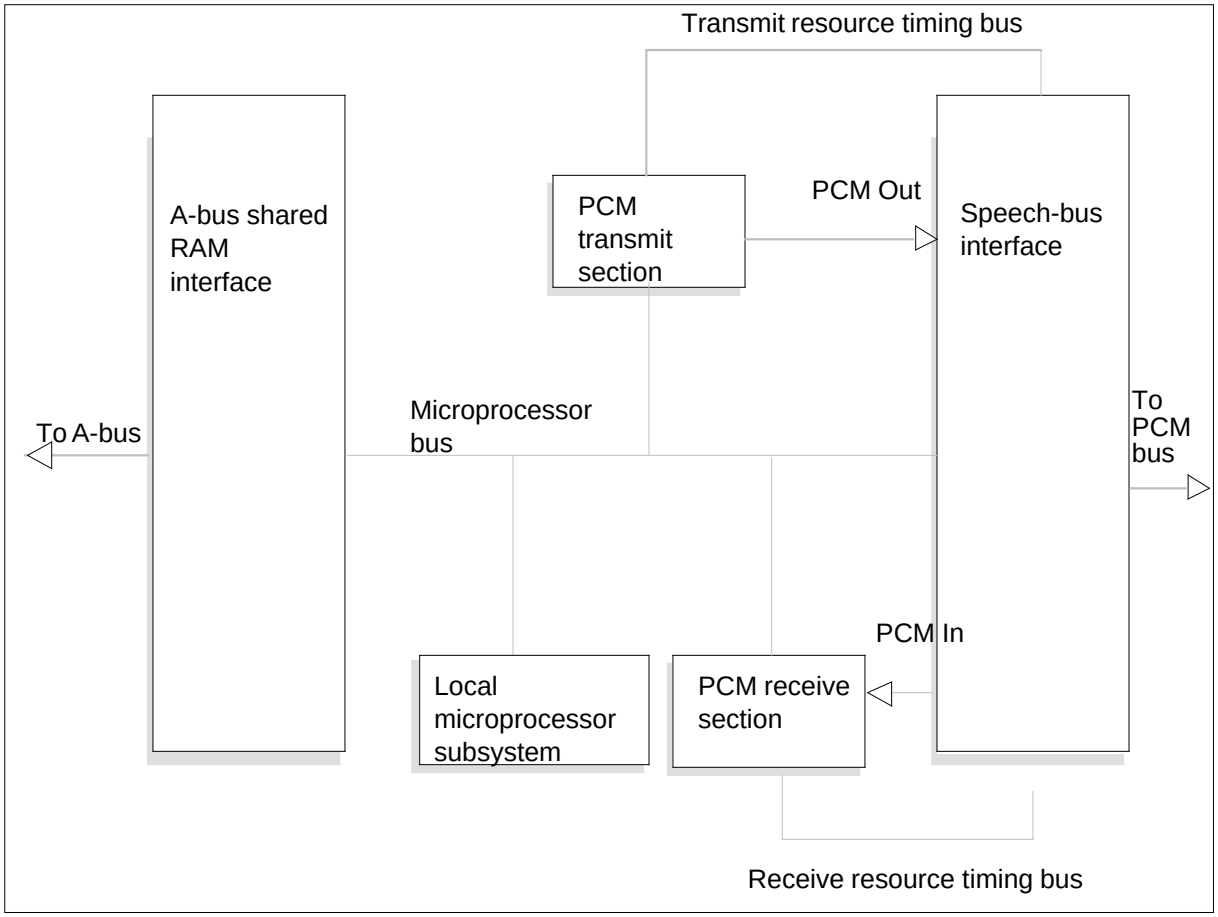
The PCM transmit section

The PCM transmit section converts the CND data to PCM samples of voiceband data signals. This section applies the voiceband data signals to a speech–bus PCM time slots. The number of available time slots is 640

The functional relationship between the blocks appears in the following figure.

NT6X78AB (continued)

The NT6X78AB functional blocks

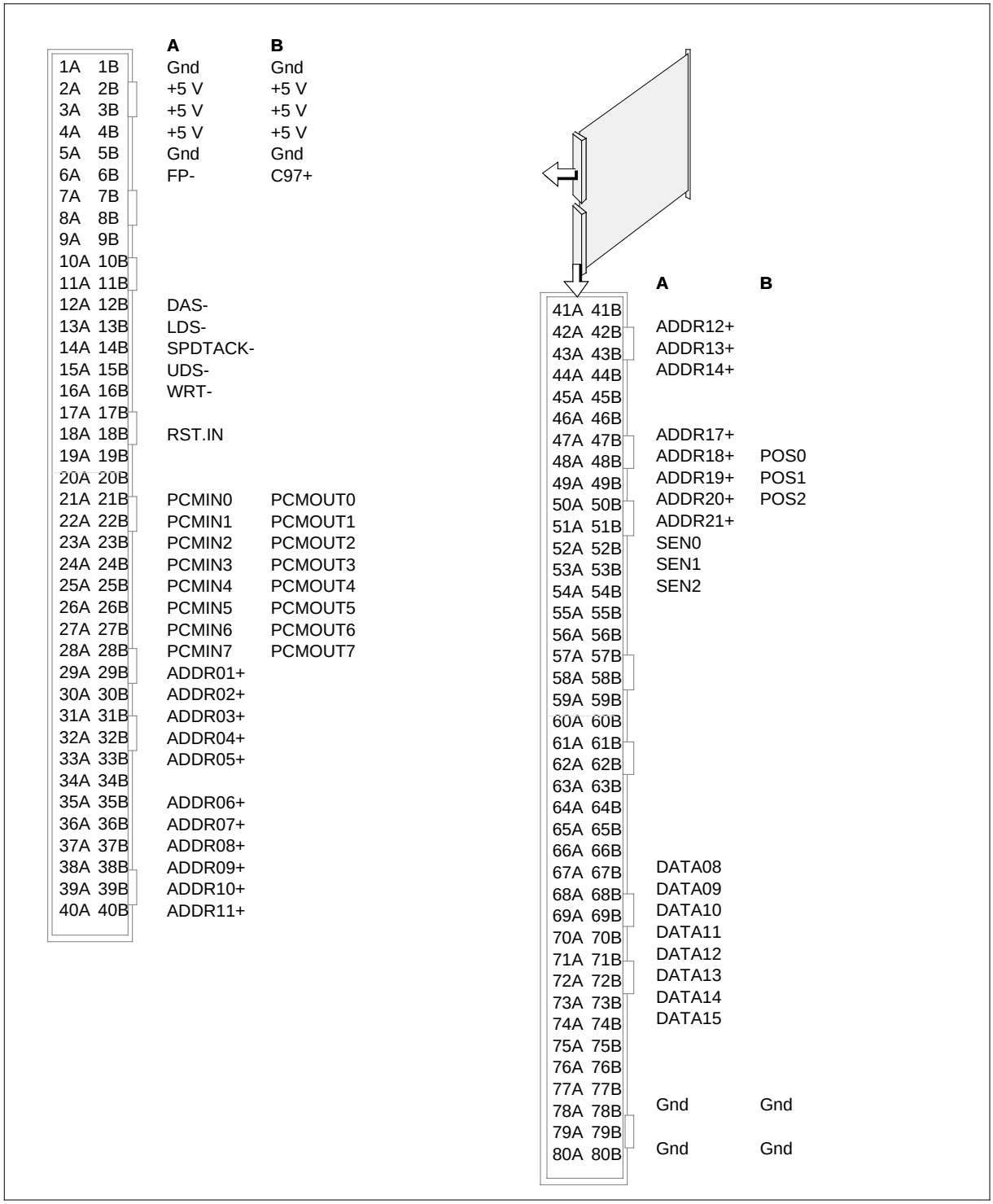


Signaling

Pin numbers

The following pin numbers for the NT6X78AB appear in the following figure.

The NT6X78AB pin numbers

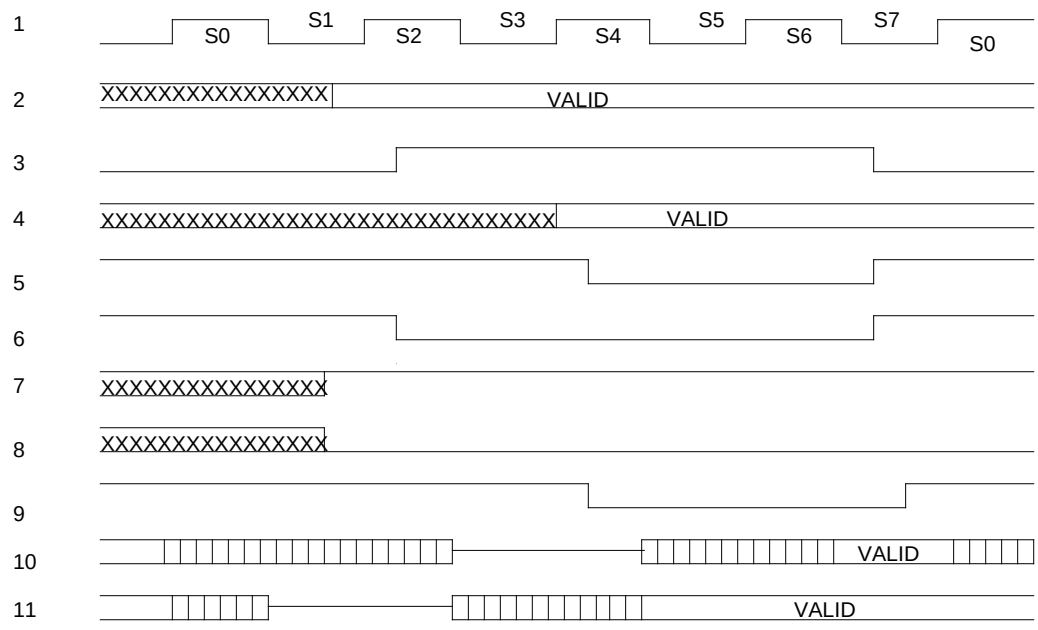


NT6X78AB (end)

Timing

The timing appears in the following figure.

The NT6X78AB timing



Legend

1. 1XCLK
2. A09 TO A01
3. AS+
4. A21 TO A10
5. DAS-
6. UDS- LDS-
7. WRT- (read cycle)
8. WRT- (write cycle)
9. DTACK-
10. D15- D00 (read cycle)
11. D15- D00 (write cycle)

Technical data

Power requirements

The power requirements of the NT6X78AB are 1.0 A at +5 V.

NT6X78BA

Product description

The CLASS modem resource (CMR) card provides the installation for the Calling Number Delivery feature. The card generates pulse code modulation (PCM) samples of V.23 modem signals, that are based on messages from the XPM signaling processor (SP). These PCM samples pass to the POTS line card in the LCM, where the samples convert to analog voice-band modem signals and sent along the loop to the CLASS subscriber. The CMR card also identifies the ring intervals on the subscriber loops, to determine when to transmit the modem signals.

Note: The NT6X78BA card is for non North American use only.

Location

The NT6X78BA is in the extended multiprocessor system (XMS) peripheral module (XPM) on the DMS-100. The NT6X78BA plugs into a spare card slot of the XPM.

Functional description

The functional description of the CMR card follows.

Functional blocks

NT6X78BA includes the functional blocks that follow:

- A-bus shared RAM interface
- local microprocessor subsystem
- speech-bus interface
- PCM receive section
- PCM transmit section
- clock tree section
- power-up section

A-bus shared RAM interface

The A-bus shared RAM interface is the main communications interface for the CMR card. The A-bus provides an interface between the XPM signaling processor and the CMR card. All messages between the XPM and the CPM card occur through the A-bus.

Local microprocessor subsystem

The local microprocessor subsystem provides the intelligence of the CMR card. The microprocessor handles the message protocol with the signaling

NT6X78BA (continued)

processor, the Calling Number Delivery feature, the diagnostics, and the supervision of card resources.

Speech-bus interface

The speech-bus interface links with the upstream and downstream parallel PCM signals on the XPM speech-bus. The speech-bus interface generates correct timing buses for the PCM transmit and PCM receive sections.

PCM receive section

The PCM receive section uses the PCM receive data on exact speech-bus time-slots. This data identifies the instances of ring on selected subscriber lines. This comparison is done to establish the transmission instances for the CND message.

PCM transmit section

The PCM transmit section converts CND data into PCM samples of voice-band data signals. The CMR card applies these signals to any of the 640 speech-bus time-slots.

Clock tree section

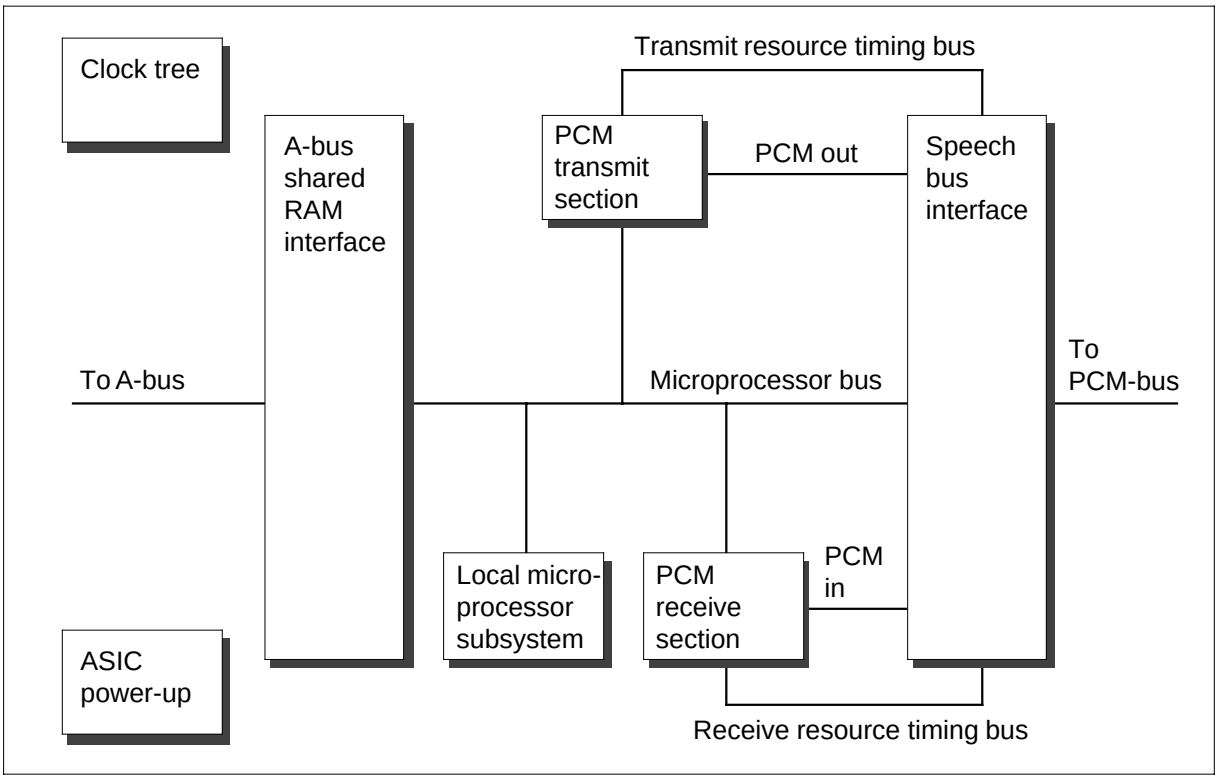
The clock tree section contains a 25 MHz crystal-oscillator, and a D-type flip-flop divide-by-two stage.

Power-up section

The power-up section contains a voltage supervisor/power-up circuit.

The figure that follows shows the relationship of the functional blocks.

NT6X78BA functional blocks



Signaling

All signals are compatible with XPM interconnect schematics for the common peripheral controller (CPC) equipment frame and the remote cluster controller shelf. The NT6X78BA card does not support the paddle board.

Pin outs

The table that follows shows the pin outs for NT6X78BA.

NT6X78BA pin outs (Sheet 1 of 5)

Pin	Signal	Pin	Signal
1A	GND	1B	GND
2A	+5V	2B	+5V
3A	+5V	3B	+5V

Note: "*" denotes a paddleboard terminal interface pin and "-" denotes a pin not used by the CMR card.

NT6X78BA (continued)

NT6X78BA pin outs (Sheet 2 of 5)

Pin	Signal	Pin	Signal
4A	+5V	4B	+5V
5A	GND	5B	GND
6A	FP-	6B	C97+
7A	-	7B	-
8A	-	8B	-
9A	-	9B	-
10A	-	10B	-
11A	-	11B	-
12A	DAS-	12B	-
13A	LDS-	13B	-
14A	SPDTACK-	14B	-
15A	UDS-	15B	-
16A	WRT-	16B	-
17A	-	17B	-
18A	RST. IN	18B	-
19A	-	19B	-
20A	-	20B	-
21A	PCMIN0	21B	PCMOUT0
22A	PCMIN1	22B	PCMOUT1
23A	PCMIN2	23B	PCMOUT2
24A	PCMIN3	24B	PCMOUT3
25A	PCMIN4	25B	PCMOUT4
26A	PCMIN5	26B	PCMOUT5

Note: "*" denotes a paddleboard terminal interface pin and "-" denotes a pin not used by the CMR card.

NT6X78BA pin outs (Sheet 3 of 5)

Pin	Signal	Pin	Signal
27A	PCMIN6	27B	PCMOUT6
28A	PCMIN7	28B	PCMOUT7
29A	ADDR01+	29B	-
30A	ADDR02+	30B	-
31A	ADDR03+	31B	-
32A	ADDR04+	32B	-
33A	ADDR05+	33B	-
34A	-	34B	-
35A	ADDR06+	35B	-
36A	ADDR07+	36B	-
37A	ADDR08+	37B	-
38A	ADDR09+	38B	* D0
39A	ADDR10+	39B	* D1
40A	ADDR11+	40B	* D2
41A	-	41B	* D3
42A	ADDR12+	42B	* D4
43A	ADDR13+	43B	* D5
44A	ADDR14+	44B	* D6
45A	-	45B	* D7
46A	-	46B	* R/W-
47A	ADDR17+	47B	* SETPAD-
48A	ADDR18+	48B	POS0
49A	ADDR19+	49B	POS1

Note: "*" denotes a paddleboard terminal interface pin and "-" denotes a pin not used by the CMR card.

NT6X78BA (continued)

NT6X78BA pin outs (Sheet 4 of 5)

Pin	Signal	Pin	Signal
50A	ADDR20+	50B	POS2
51A	ADDR21+	51B	* HXCS-
52A	SEN0	52B	* USARCS-
53A	SEN1	53B	-
54A	SEN2	54B	-
55A	-	55B	-
56A	-	56B	* A1
57A	-	57B	* A2
58A	-	58B	-
59A	-	59B	-
60A	-	60B	-
61A	-	61B	-
62A	-	62B	* UARINT-
63A	-	63B	* PRESET-
64A	-	64B	* ENPB
65A	-	65B	-
66A	-	66B	-
67A	DATA08	67B	-
68A	DATA09	68B	-
69A	DATA10	69B	-
70A	DATA11	70B	-
71A	DATA12	71B	-
72A	DATA13	72B	-

Note: "*" denotes a paddleboard terminal interface pin and "-" denotes a pin not used by the CMR card.

NT6X78BA pin outs (Sheet 5 of 5)

Pin	Signal	Pin	Signal
73A	DATA14	73B	-
74A	DATA15	74B	-
75A	-	75B	-
76A	-	76B	-
77A	-	77B	-
78A	GND	78B	GND
79A	-	79B	-
80A	GND	80B	GND

Note: "*" denotes a paddleboard terminal interface pin and "-" denotes a pin not used by the CMR card.

Timing

Functional descriptions and timings of the A-bus and the speech-bus appear in the sections that follow.

A-bus

The A-bus interface of the CMR card to the XPM signaling processor meets the A-bus specifications.

The bus includes the group of lines that follow:

Address

Address lines A21 to A1 provide a 4 Mb address space. The data strobes (UDS- and LDS-) provide the information that address line A0 would provide. The CMR card uses a part of of the address lines.

Data

The CMR card provides data lines DATA15 to DATA00. The CMR card uses the upper eight data lines (that is, DATA15 to DATA08).

SP control outputs

The CMR card uses the signaling lines that follow:

- WRT-: Write Enable
- DAS-: Delayed Address Strobe

NT6X78BA (continued)

- UDS-: Upper Data Strobe
- LDS-: Lower Data Strobe

SP control inputs

The main SP control input signal is the SPDTACK- (SP Data Transfer Acknowledge). Bus slaves, such as the CMR card, use this signal to extend the period of a bus transaction if required.

System supervision

Although the CMR card does not uses supervision signals, the XPM signaling processor provides the supervision signals that follow:

- 1XCLK+: One Times Clock (8 or 10 MHz)
- RST.OUT-: Reset Out (from the XPM signaling processor)

System status

Although the CMR card does not use function codes, the XPM signaling processor provides three function code lines (FC2 to FC0) with buffers.

Transfer to bus master

Several additional lines provide for the smooth transfer of control of the A-bus from one bus master to another. For example, the A-bus moves from the XPM signaling processor to a DMA device, or reversed. The CMR card does not use these lines because it is a permanent slave to the A-bus.

Shelf supervision

The CMR card uses the shelf reset signal (RST.IN) that also resets the other cards on the XPM shelf.

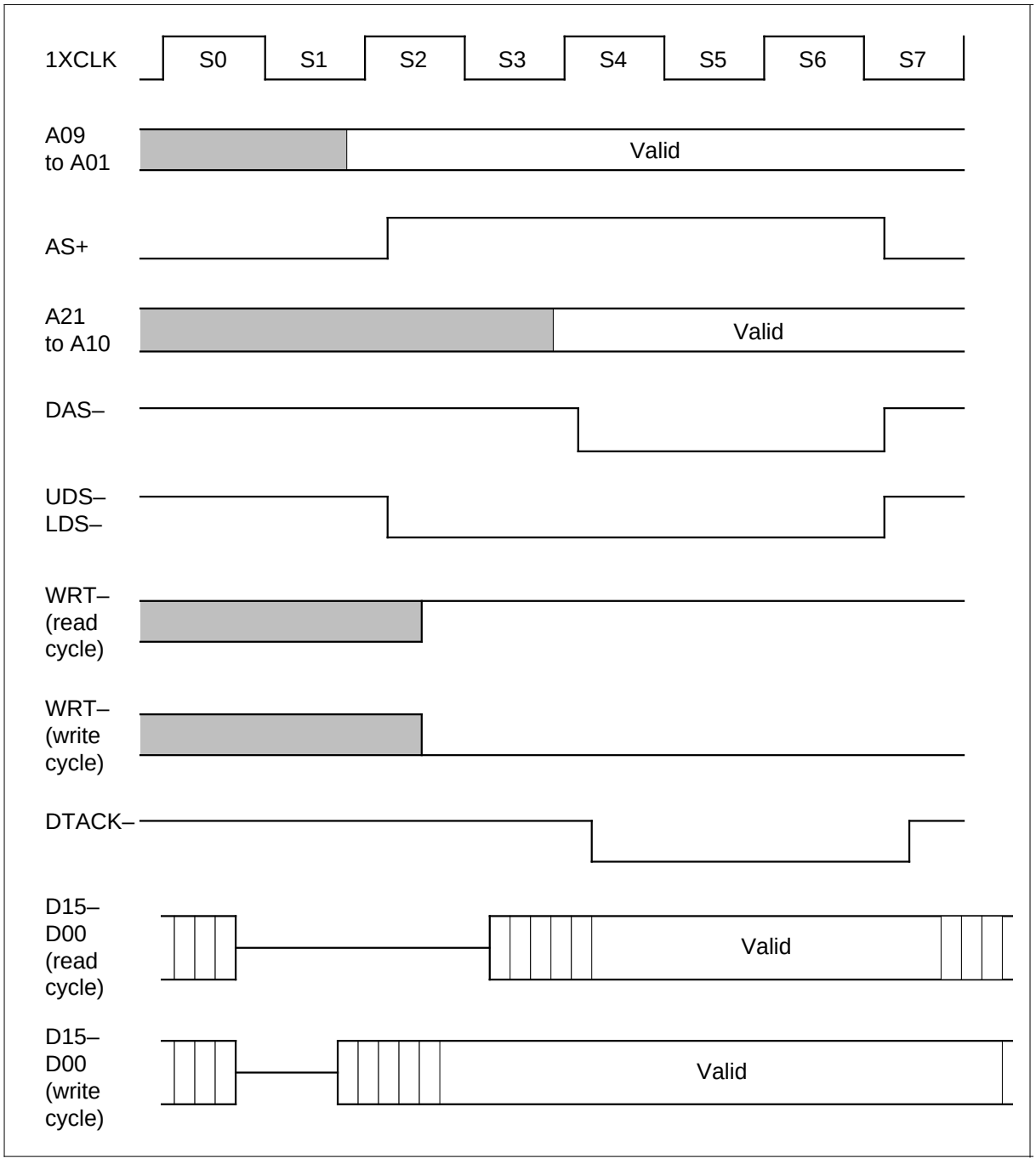
Power

The A-bus provides +5V and +/-12V power lines. The CMR card uses only the +5V supply pins on the A-bus. The CMR card uses a 3 ampere fuse on the +5V circuits to protect against an overload.

The figure that follows shows the timing relationship of the A-bus signals.

NT6X78BA (continued)

A-bus signal timing



NT6X78BA (continued)

Speech-bus

The Speech-bus interface of the CMR card meets the LGC/DTC Speech-bus specification.

The speech-bus includes the group of lines that follow:

Timing signals

The timing signals include:

- a 10.24 MHz 50% duty-cycle clock
- a C97+ clock
- an active-low frame pulse (FP-) with a 125 micro-second period

The C97+ clock signal divides by two on the CMR card to generate a C195+ clock signal with a period of 195 ns.

PCM receive lines

Pulse code modulation (PCM) receive lines PCMIN7 to PCMIN0 carry the PCM bytes for the 640 channels in the upstream, or incoming direction (that is, towards the DMS-100 network).

PCM transmit lines

The PCM transmit lines PCMOUT7 to PCMOUT0 carry the PCM bytes for the 640 channels in the downstream or outgoing direction. The PCM transmit line direction is towards the LCM and subscriber loop.

Card transmit enable signals

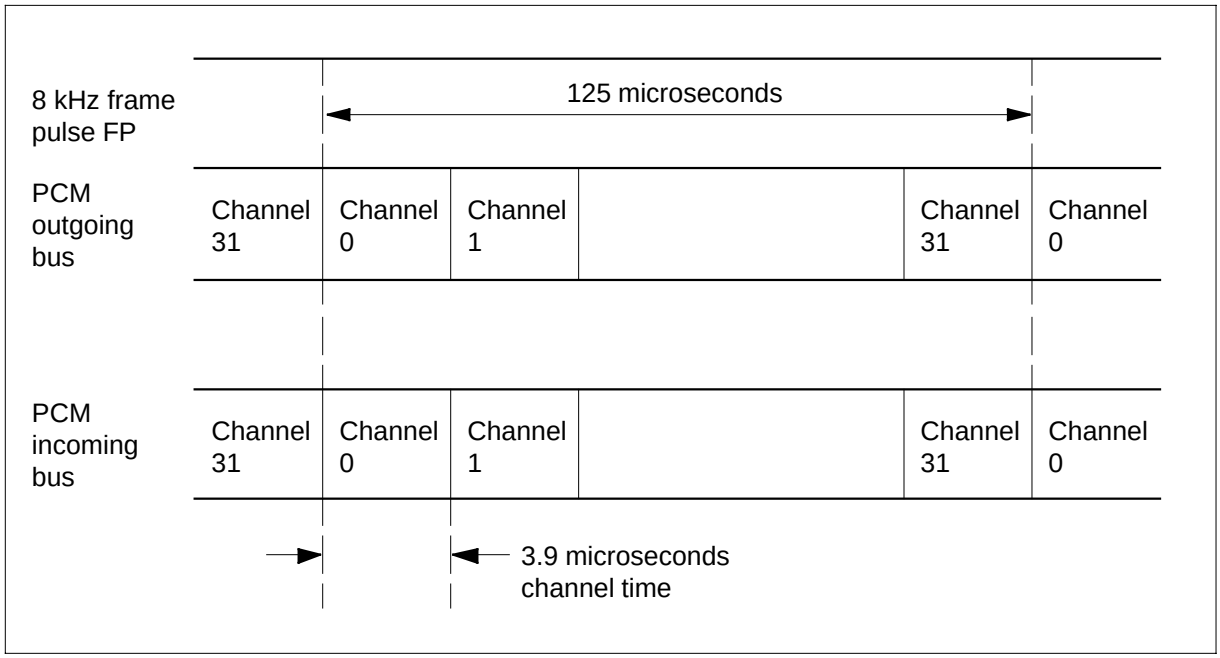
The SEN0 to SEN2 lines allow the CMR card to transmit PCM bytes on the outgoing or downstream PCM bus. The enable signals occur one time-slot (195 ns) earlier.

Card slot ID signals

The POS0 to POS2 lines identify the XPM spare card slot where the CMR card resides. The ID signals map the shared RAM from the XPM signaling processor side. The ID signals also compare the transmit enable signals to determine when to transmit on the speech-bus.

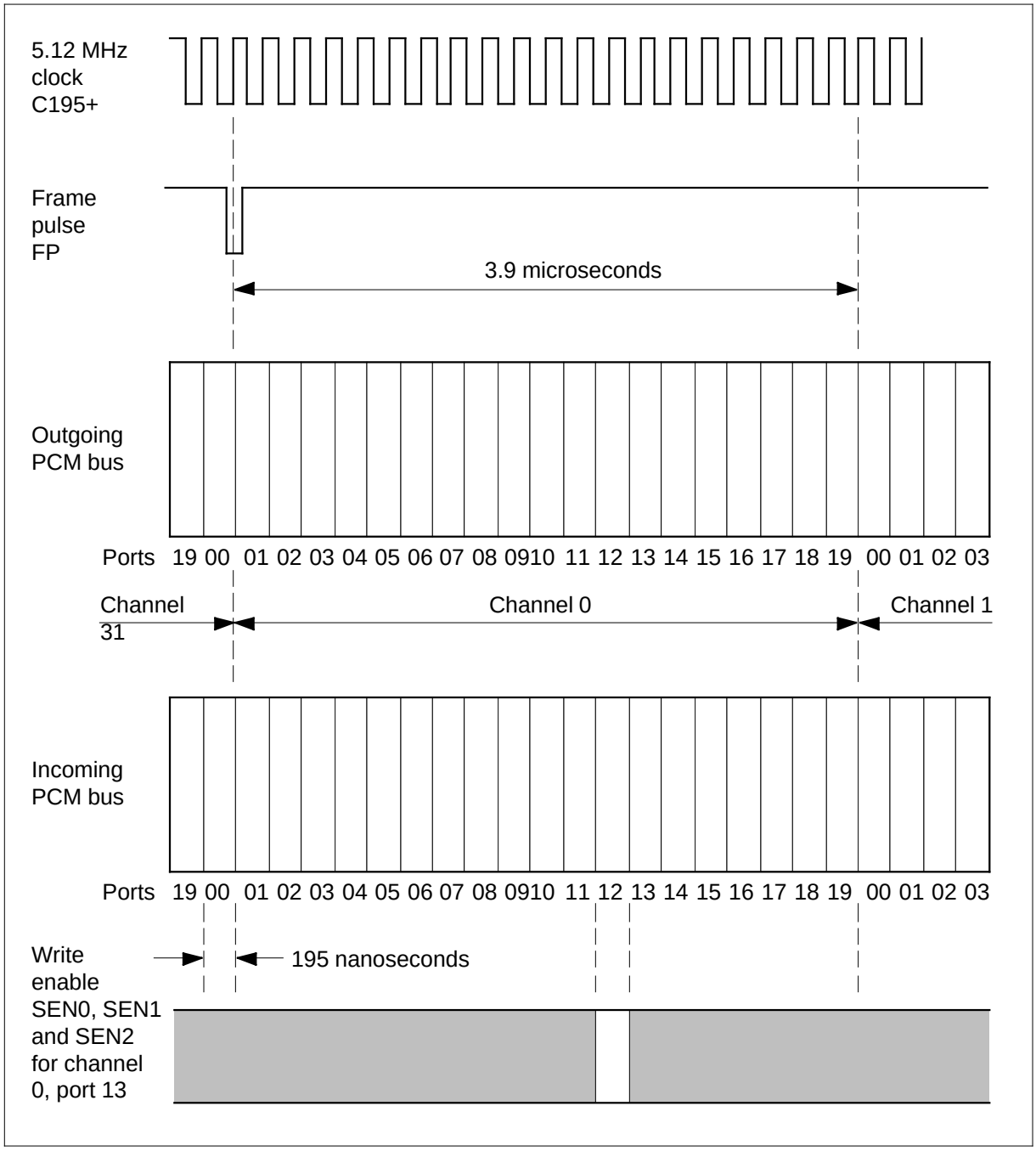
The two figures that follow show the timing for the speech-bus.

Timing of the channels on the speech-bus



NT6X78BA (continued)

Timing of the ports in a speech-bus channel



Technical data

The CMR card uses one 208-pin application specific integrated circuit (ASIC).

Power requirements

A calculated value for all of the power requirements for the CMR card is 1.0 A at +5V.

NT6X79AA

Product description

The NT6X79AA CPCE tone generator circuit (TGC) and the NT6X69AA common peripheral processor (CPP) message protocol circuit (MPC) can work together. These cards together produce a circuit equal to the NT6X69AB CPP message protocol and tone circuit.

Location

The card is in a spare slot in the following peripheral modules (PM):

- line group controller (LGC)
- line trunk controller (LTC)
- digital trunk controller (DTC)
- international digital trunk controller (IDTC)
- message switch buffer (MSB)
- remote cluster controller (RCC)

Functional description

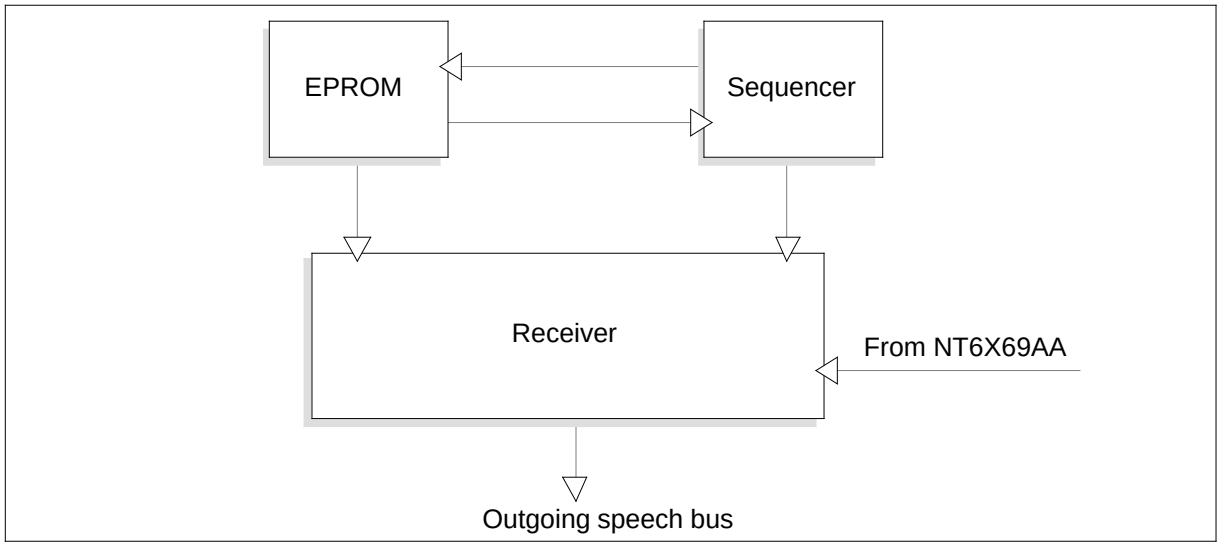
The NT6X79AA uses 125µs time frames and temporary memory storage. The NT6X79AA stores and releases tone samples to generate a specified tone.

Functional blocks

The NT6X79AA has the following functional blocks:

- erasable programmable read–only memory (EPROM)
- sequencer
- receiver

The NT6X79AA functional blocks



The EPROM

The EPROM has an 8 kbit capacity and stores samples of tones to transmit on the speech bus that the MPC controls. The circuit holds a maximum of 63 tones.

Sequencer

The sequencer controls the transfer of tone samples from the EPROM to the receiver. The sequencer determines the EPROM address of the tone sample. The sequencer sends a signal to the receiver to obtain the sample from that address.

The sequencer contains counters that divide one 125µs machine time frame into 64 machine cycles. To obtain a tone sample, the sequencer instructs the receiver to access a specified address in the EPROM during each cycle.

Receiver

The receiver uses two RAM circuits to retain tone samples from the EPROM for a limited time. The connection memory in the MPC allows the tone to transmit on the outgoing speech bus.

The circuit receives 64 tone samples during each 125µs time frame. At the end of each time frame the circuit switches one RAM from a read mode to a write mode. The circuit switches the other RAM from a write mode to a read mode.

NT6X79AA (end)

Technical data

Dimensions

The dimensions of the NT6X79AA card are as follows:

- height: 317.5 mm (12.5 in.)
- width: 254.0 mm (10.0 in.)

Power requirements

The power used by this card from the +5 V supply of the power converter is 8.5 W.

NT6X79AB

Product description

The NT6X79AB tone generator circuit (TGC) and the NT6X69AA CPP message protocol circuit (MPC) can work together. Together, these cards produce a circuit equal to the NT6X69AB CPP message protocol and tone circuit.

Location

The card is in a spare slot in the following peripheral modules (PM):

- line group controller (LGC)
- line trunk controller (LTC)
- digital trunk controller (DTC)
- international digital trunk controller (IDTC)
- message switch buffer (MSB)
- remote cluster controller (RCC)

Functional description

The NT6X79AB uses 125µs time frames and temporary memory storage. The NT6X79AB stores and releases tone samples to generate a specified tone.

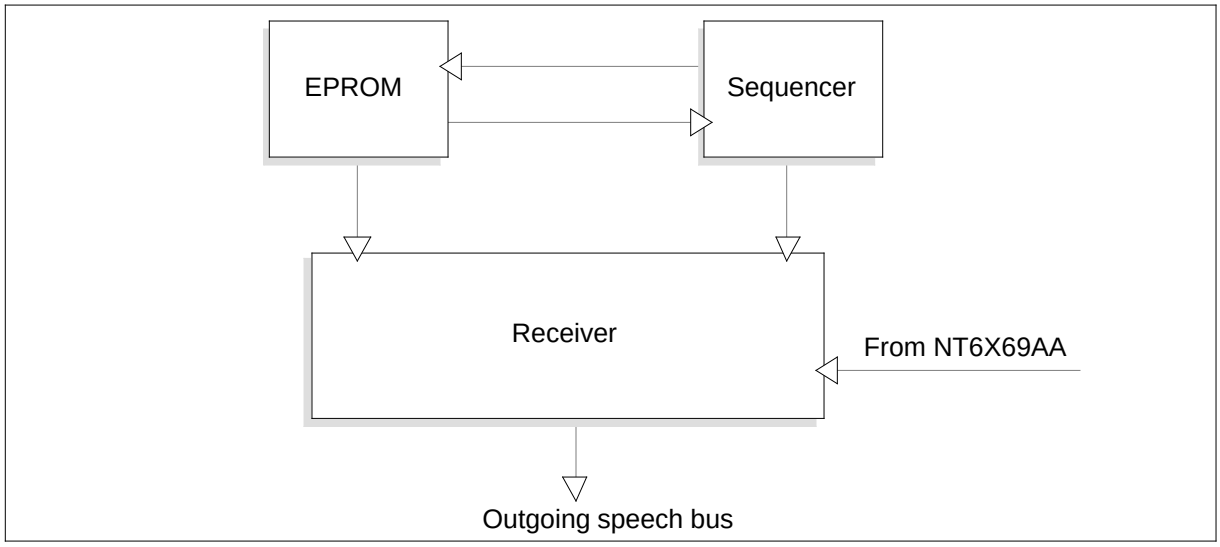
NT6X79AB (continued)

Functional blocks

The NT6X79AB has the following functional blocks:

- erasable programmable read–only memory (EPROM)
- sequencer
- receiver

The NT6X79AB functional blocks



The EPROM

The EPROM has an 8 kbit capacity and stores samples of tones to transmit on the speech bus under that the MPC controls. The circuit holds a maximum of 63 tones.

Sequencer

The sequencer controls the transfer of tone samples from the EPROM to the receiver. The sequencer determines the EPROM address of the tone sample. The sequencer sends a signal to the receiver to obtain the sample from that address.

The sequencer contains counters that divide one 125µs machine time frame in 64 machine cycles. To obtain a tone sample, the sequencer instructs the receiver to access a specified address in the EPROM during each cycle.

Receiver

The receiver uses two RAM circuits to retain tone samples from the EPROM for a limited time. The connection memory in the MPC allows the tone to transmit on the outgoing speech bus.

The circuit receives 64 tone samples during each 125µs time frame. At the end of each time frame the circuit switches one RAM from a read mode to a write mode. The circuit switches the other RAM from a write mode to a read mode.

Technical data

Dimensions

The dimensions of the NT6X79AB card are as follows:

- height: 317.5 mm (12.5 in.)
- width: 254.0 mm (10.0 in.)

Power requirements

The power use of the card is 8.5 W. The voltage of the LCM power converter is +5 V ±0.25 V.

NT6X80AA

Product description

The NT6X80AA subscriber carrier module (SCM) pad/ring card provides the following functions:

- attenuation
- ringing
- pulse code modulation (PCM) delay
- diagnostic testing

The card performs these functions on PCM speech the card receives from the NT6X72 formatter circuit pack. The card sends the PCM speech to the NT6X44 time switch.

Location

The card is part of the parallel speech bus circuits in the following SCM–100 peripherals:

- subscriber module rural (SMR)
- subscriber module SLC–96 (SMS)
- subscriber module urban (SMU)

Functional description

The NT6X80AA provides a controlled digital attenuation of the PCM speech for a channel. Frequency shift ratio (FSR) requires four sets of PCM ringing samples in the SMR. Superimposed ringing requires four dc control voltages. The card contains a delay circuit to delay PCM speech. The card uses the inject and catch registers for self–diagnostic tests with the signal processor (SP). These tests check sanity, status, and commands.

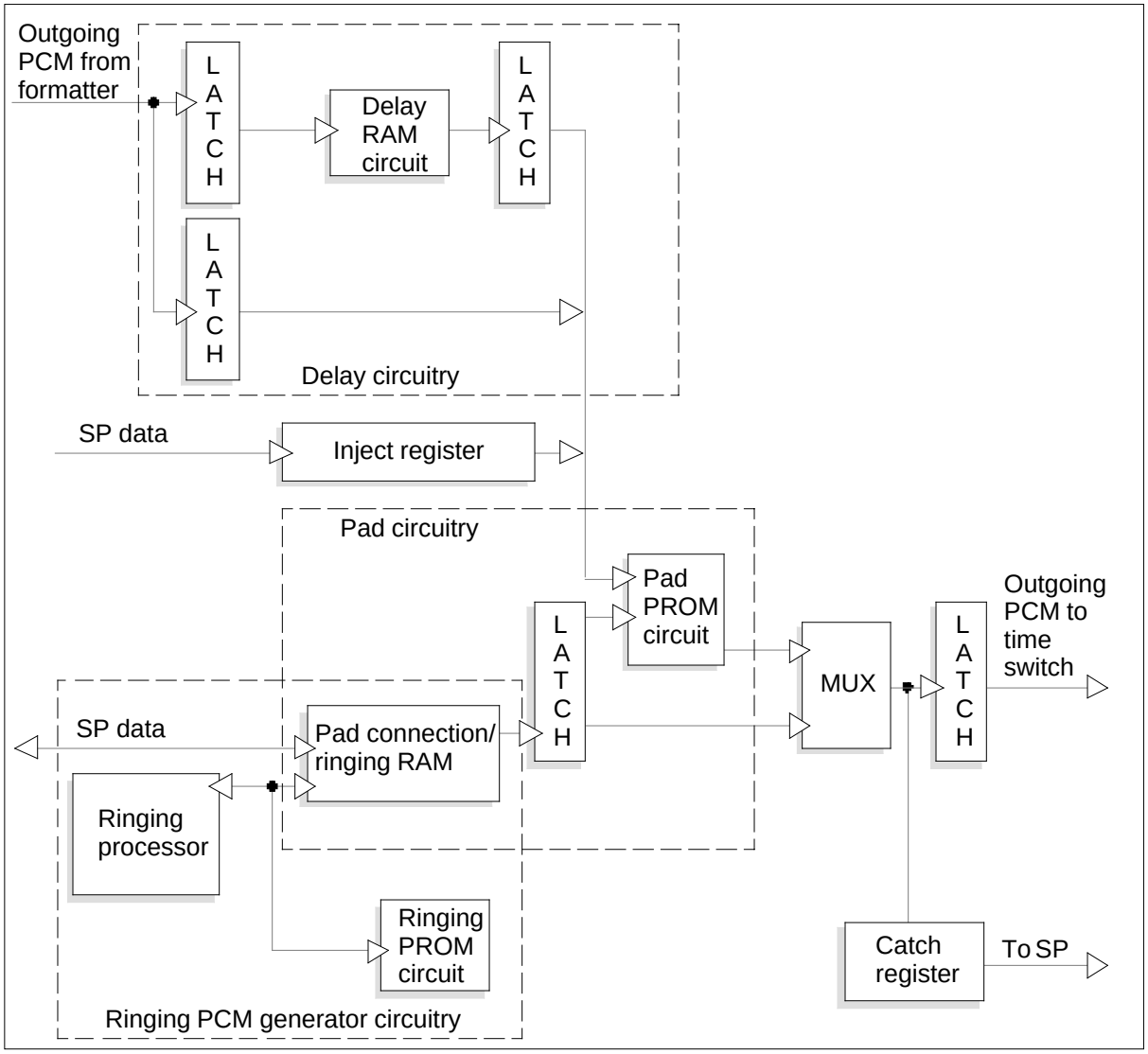
Functional blocks

The NT6X80AA has the following functional blocks:

- ringing processor
- pad connection/ringing random access memory (RAM)
- pad programmable read–only memory (PROM) circuit
- ringing PROM circuit
- multiplexer (MUX)
- delay RAM circuit
- inject register

- catch register
- five latch circuits

The NT6X80AA functional blocks



Ringing processor

The ringing processor is an 8 bit 8039 microprocessor. The microprocessor uses software that the ringing PROM holds to generate PCM ringing samples and communicate with the SP. The circuit uses commands from the SP for self–diagnostics on the pad connection/ringing RAM. The circuit performs a continuous checksum of data in the ringing PROM. The system sends the results of the tests to the SP.

NT6X80AA (continued)

Pad connection/ringing RAM

The pad connection/ringing RAM receives the required loss level from the SP and uses a memory location to store the loss. The circuit contains one memory location for each time slot on the parallel speech bus. The circuit sends the required loss data for each time slot through a latch circuit to the pad PROM.

Pad PROM circuit

The pad PROM circuit receives 8–bit PCM speech samples from the delay circuit. This circuit uses the value of the 3 bit loss level signal to attenuate this data. This loss signal is from the pad connection/ringing RAM. The circuit contains groups of 8–bit PCM samples with 0 to 7 dB loss in 1–dB increments. The circuit functions as a look–up table.

Ringing PROM memory circuit

The ringing PROM sends software commands and information to the ringing processor.

The MUX

The MUX receives 512 active and 128 service time slots from the outgoing parallel speech bus. The active time slots carry customer and PCM speech. The service time slots carry tones, ringing samples, and additional information. During active times, the MUX outputs attenuated PCM samples from the pad PROM. During service times, or dead times, the MUX selects the ringing samples from a latch circuit.

Both outputs transmit through a latch circuit to the NT6X44 time switch.

Delay RAM circuit

The delay RAM stores the outgoing PCM speech for 639 channel times (124.805µ) when a delay is necessary. If a delay is not necessary, a latch circuit buffers the PCM speech. The PCM speech transmits from the NT6X72 formatter circuit pack to the pad PROM.

Inject register

The inject register is a write–only register that overwrites PCM data from the NT6X72 formatter circuit pack to perform diagnostics. The register overwrites PCM data with a test pattern that the SP sends. The pad PROM attenuates the test pattern. The test pattern goes to the catch register for transmission to the SP.

Catch register

The catch register is a read–only register that receives the attenuated data from the MUX to perform diagnostic tests. The catch register sends the output to the SP for examination.

Latch circuits

The five latch circuits receive data from different circuits and buffer the data before transmission of data to the next circuit.

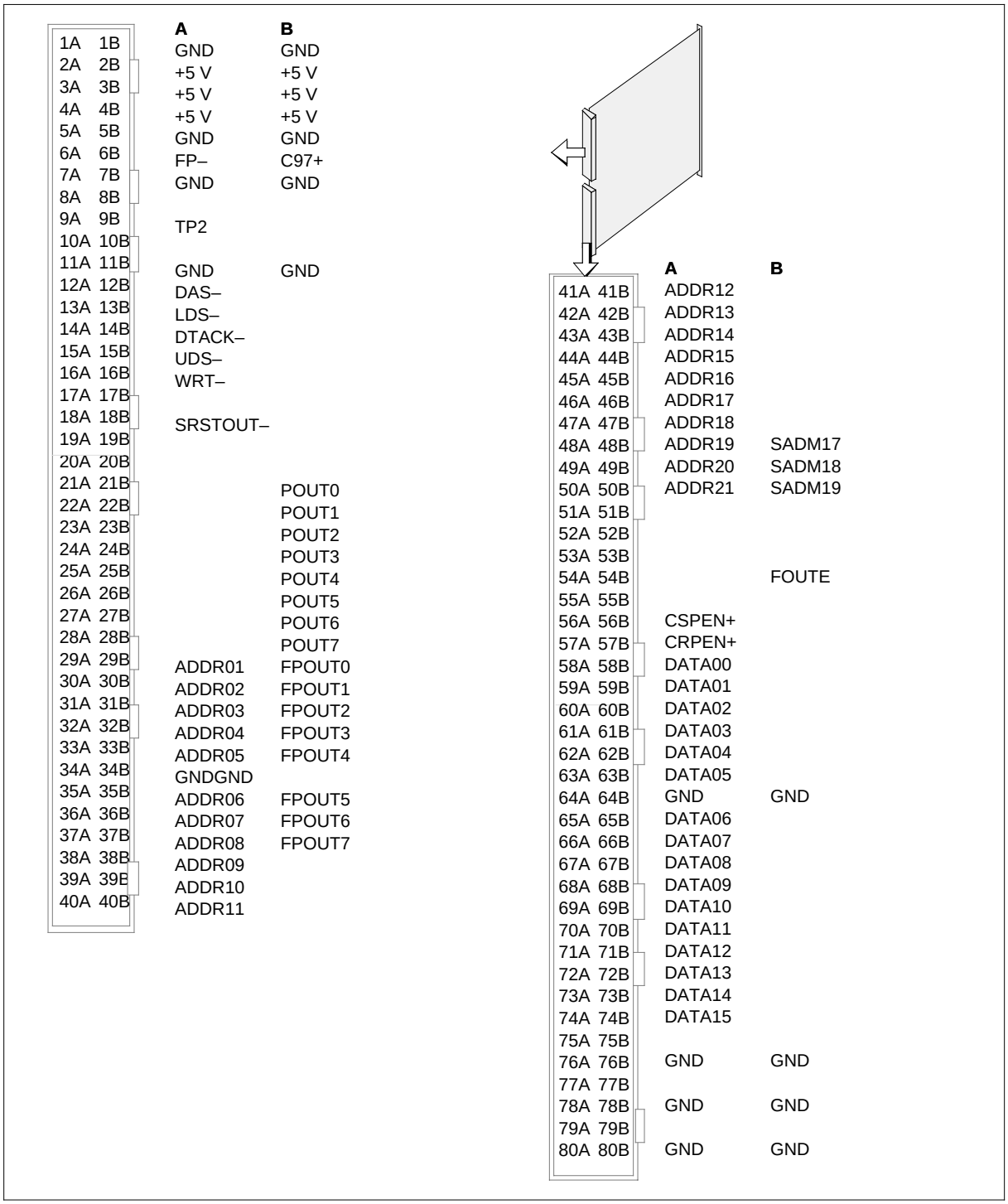
Signaling

Pin numbers

The pin number diagram for the NT6X80AA appears in the following table.

NT6X80AA (continued)

The NT6X80AA pin numbers



Technical data

The card uses μ–law PCM coding that negative TRUE logic implements. The ringing frequencies for the FSR appear in the following table.

Ringing frequencies for the FSR

Number	Frequence (Hz)	Nominal voltage (rms)	Peak voltage (V)
1	16.00	105	1.55
2	16.67	105	1.55
3	20.00	105	1.55
4	25.00	110	1.63
5	30.00	110	1.63
6	33.33	115	1.70
7	40.00	115	1.70
8	42.00	115	1.70
9	50.00	120	1.77
10	54.00	120	1.77
11	60.00	120	1.77
12	66.00	120	1.77
13	66.67	120	1.77

Note: The peak voltage is a maximum value of the sine wave by the coder-decoder (CODEC) of the QPP541 frequency selective remote line card of the SMR.

The dc control voltages for superimposed ringing appear in the following table. The reference voltage, that the QPP445A superimposed remote line card of the SMR uses, determines the selection of dc control voltages.

Dc control voltages for superimposed ringing (Sheet 1 of 2)

T or R voltage	The PCM of ringing generator	Voltage out of CODEC	The QPP445A reference voltage
+48 V ring party	4B	+0.32 V	0 < Vo < +0.61
-48 V ring party	CB	-0.32 V	-0.61 < Vo < 0

NT6X80AA (continued)

Dc control voltages for superimposed ringing (Sheet 2 of 2)

T or R voltage	The PCM of ringing generator	Voltage out of CODEC	The QPP445A reference voltage
+48 V tip party	6B	+1.30 V	Vo > +0.61
-48 V tip party	EB	-1.30 V	-0.61 > Vo

The command, board, and diagnostic status bytes appear in the following table.

Statusbyte (Sheet 1 of 2)

Type	Value	Description
Commands		
	00	Enable; nondelay
	08	Enable; nondelay, ring
	10	Run self–diagnostics
	20	Enable; delay
	28	Enable; delay, ring
	40	Disable; nondelay
	48	Disable; nondelay, ring
	60	Disable; delay
Board		
	10	Self–diagnostics in progress
	80	Enable; nondelay
	88	Enable; nondelay, ring
	A0	Enable; delay
	A8	Enable; delay, ring
	C0	Disable; nondelay
	C8	Disable; nondelay, ring
	E0	Disable; delay

Statusbyte (Sheet 2 of 2)

Type	Value	Description
Diagnostics		
	F0	Self–diagnostic passed
	F1	Bad program part of PROM
	F2	Bad ringing PCM part of PROM
	F3	Bad program and ringing PCM part of PROM
	F4	Bad RAM
	F5	Bad RAM and program part of PROM
	F6	Bad RAM and ringing PCM part of PROM
	F7	Bad RAM and program/ringing PCM part of PROM

Dimensions

The dimensions of the NT6X80AA are as follows:

- height: 317.5 mm (12.5 in.)
- depth: 254 mm (10.0 in.)
- width: 22.2 mm (0.875 in.)

Power requirements

The power requirements for the NT6X80AA are a voltage of +5V dc and current of 1.3 A.

NT6X81AA

Product description

The NT6X81AA subscriber carrier module (SCM) A-bit/B-word card connects the signal processor (SP) and time switch of the subscriber module rural (SMR). This connection allows A-bit and B-word data to pass between the SP and the remote concentrator terminal (RCT) in the DMS-1R family.

The card also uses the interface to automatically scan subscriber lines for an initial offhook status.

Location

The card is in the SMR shelf.

Functional description

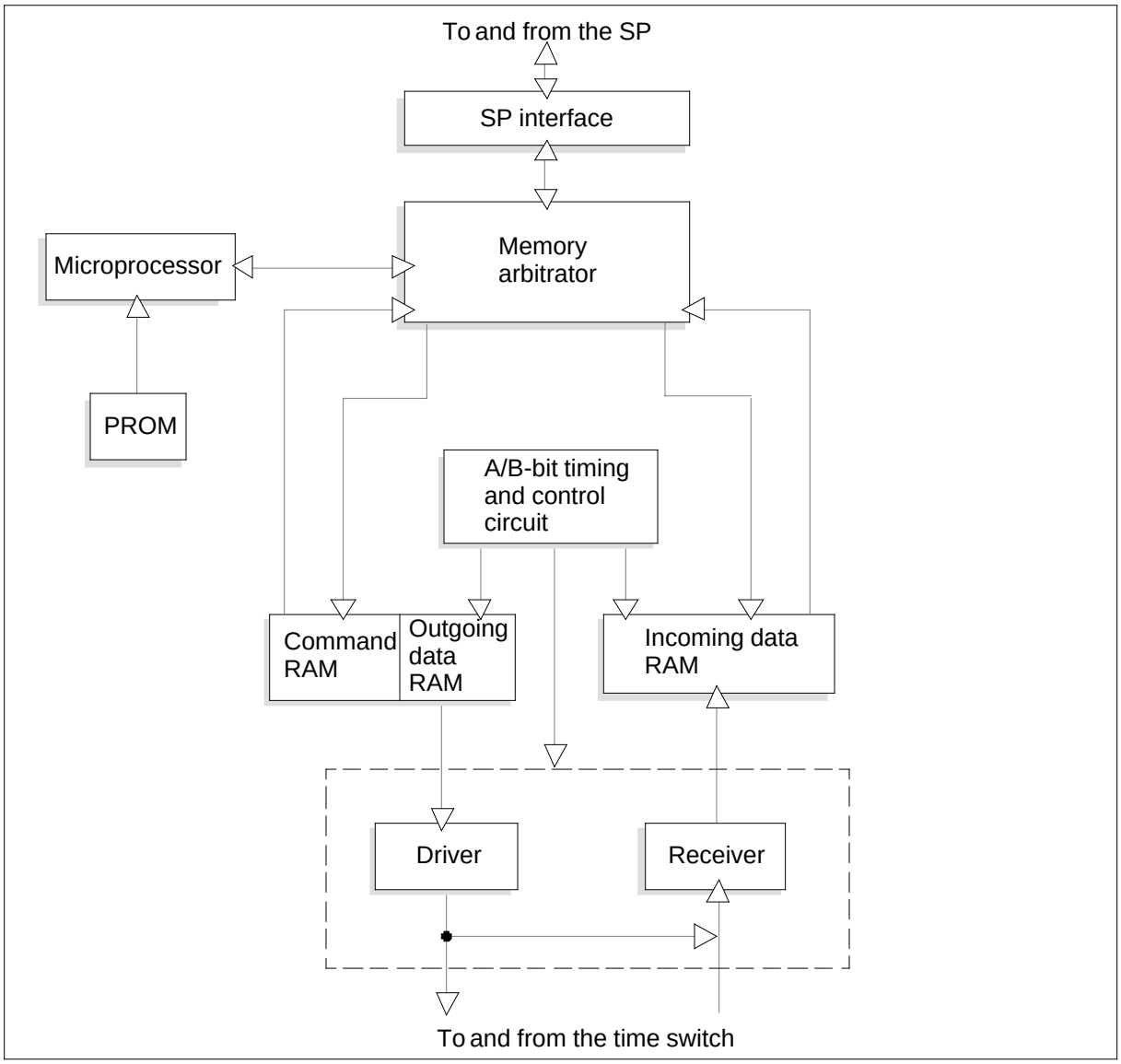
The NT6X81AA sends and receives A-bit and B-word messages between the SP and the time switch. The card performs encoding and decoding of B-word messages, autoscanning of subscriber lines, and self-diagnostic tests.

Functional blocks

The NT6X81AA has the following functional blocks:

- SP interface
- memory arbitrator
- microprocessor
- PROM
- A/B-bit timing and control circuit
- command RAM
- outgoing data RAM
- incoming data RAM
- driver
- receiver

NT6X81AA functional blocks



SP interface

The SP interface transfers data between the SP and the card. The circuit synchronizes the SP to the internal memory cycles of the card.

Memory arbitrator

The memory arbitrator chooses between the SP interface and the microprocessor to determine access to the RAMs of the card.

NT6X81AA (continued)

Microprocessor

The 8085 microprocessor encodes outgoing and decodes incoming B-words with the required protocol. This microprocessor also uses commands from the SP to automatically scan subscriber lines for initial offhook status.

PROM

The PROM contains the operating instructions for the microprocessor.

A/B-bit timing and control circuit

The A/B-bit timing and control circuit instructs the outgoing data RAM and the incoming data RAM to write the A-bit and B-word messages to the transmit and receive lines.

Command RAM

The command RAM functions as a buffer for messages that the system sends between the SP and the microprocessor. The command RAM and the outgoing data RAM are on the same chip.

Outgoing data RAM

The outgoing data RAM receives eight sequential A-bit data bits from the SP. The outgoing data RAM also sends the data bits through the driver to the time switch under control of the A/B-bit timing and control circuit. The outgoing RAM sends data bits in a sequence. The outgoing data starts with the most significant bit and ends with the least significant bit.

The circuit receives B-word messages from the SP. The circuit also uses encoded messages from the microprocessor to send the B-word messages through the driver to the time switch. The circuit sends these messages under control of the A/B-bit timing and control circuit. The outgoing data RAM and the command RAM are on the same chip.

Incoming data RAM

The incoming data RAM receives A-bit data. Under control of the A/B-bit timing and control circuit, the incoming data RAM records the digital state of the passing A-bits. This action allows the SP to read A-bit data.

The circuit receives and holds incoming B-words for the SP to read until the microprocessor decodes the words. The system receives B-words under control of the A/B-bit timing and control circuit.

Driver

The driver receives data from the outgoing data RAM and converts the parallel data to serial data for transmission to the time switch.

Receiver

The receiver accepts serial data that routes to the time switch from the RCT. The receiver converts the data to a parallel format.

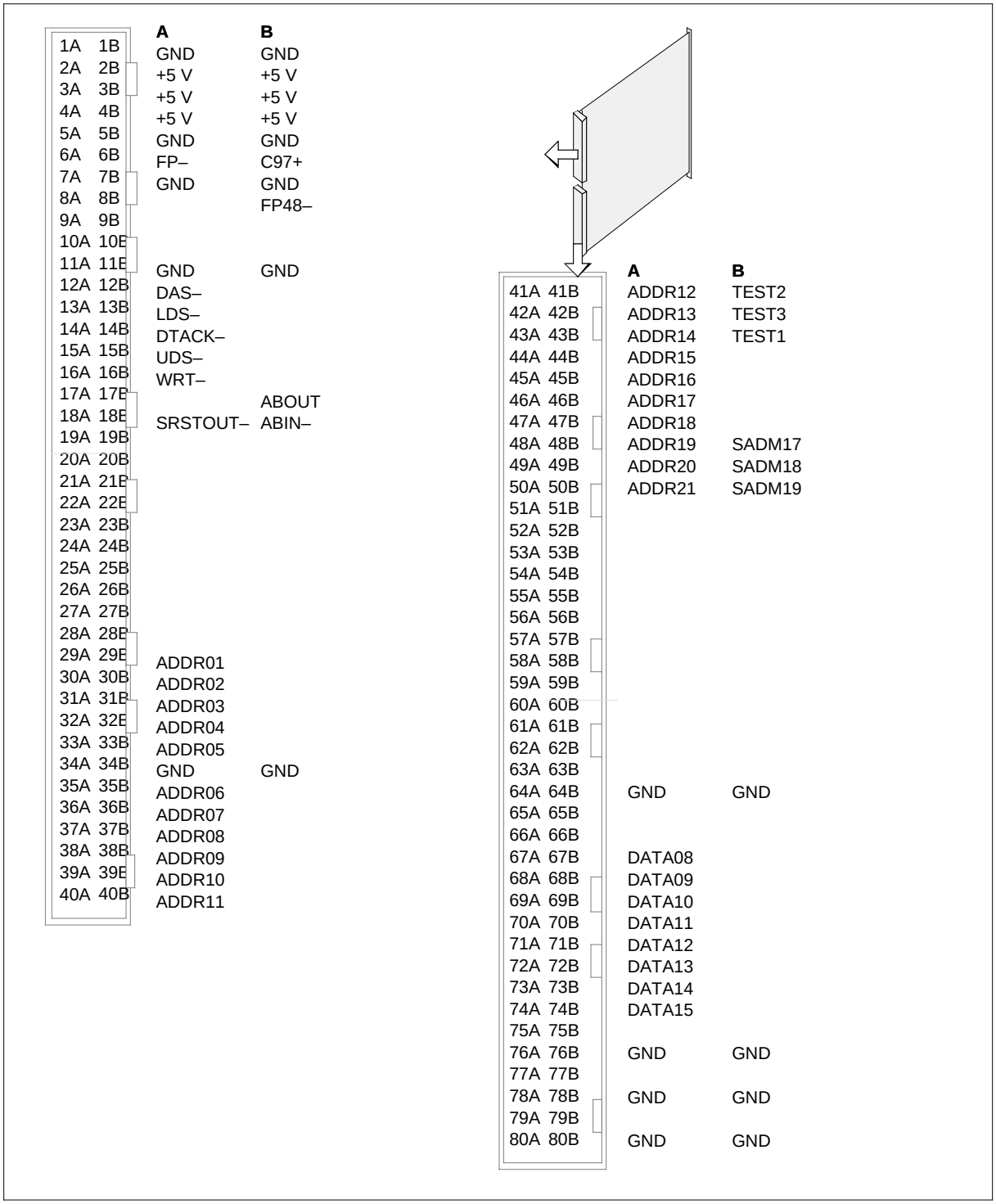
Signaling

Pin numbers

The pin numbers diagram for the NT6X81AA appears in the following figure.

NT6X81AA (continued)

NT6X81AA pin numbers



Technical data

The NT6X81AA has a mean time between failures (MTBF) of 193,189.2 hours (22 years). The NT6X1AA has a failure rate (FR) of $5.17627/10^6$ hours.

The card requires a 10.03 MHz master clock signal, a DS-1 frame pulse signal, and a master frame pulse signal. The time switch uses A/B output data (ABOUT) and A/B input data (ABIN) interface signals. The following table lists the microprocessor-to-SP interface signals.

Microprocessor interface to SP

Interface signal	Description
SADM17 - SADM9	Determines the board address of the card
ADDR01 - ADDR21	21-bit, unidirectional, tristate address bus
DATA08 - DATA15	8-bit, bidirectional, tristate data bus
Delayed address strobe (DAS)	Indicates a valid address
Read/write (R/W)	Defines the data bus transfer as an external read or write signal
Upper and lower data strobes (UDS, LDS)	Indicates valid data on the data bus
Data acknowledge (DTACK)	Indicates completion of data transfer. The card generates this signal.
SRSTOUT	Master reset

Physical dimensions

The physical dimensions of the NT6X81AA are as follows:

- height: 317.5 mm (12.5 in.)
- depth: 254 mm (10.0 in.)
- width: 22.2 mm (0.875 in.)

NT6X81AA (end)

Power requirements

The power requirements for the NT6X81AA appear in the following table.

Power requirements

Voltage	Current
+5V	2.77A
+5V + 10%	3.05A

NT6X85AA

Product description

The NT6X85AA DS-1 interface for SLC-96 card works in two modes: derived data link (DDL) and non-DDL. In the DDL mode, the card acts as the DS-1 interfacing circuit pack of the peripheral subscriber module SLC-96 (SMS). In the non-DDL mode, the system disables the DDL message capability of the card. In the non-DDL mode, the performance of the card is identical to the NT6X50AA DS-1 interface circuit pack.

In the DDL mode, the card supports two bidirectional DS-1 links to SLC-96 remote terminals. The card contains two links for both the incoming and outgoing circuits. These links connect to DS-1 links and work separately. These links perform the same functions.

Location

In the DDL mode, the card occupies one position in the SMS shelf. In the non-DDL mode, the card can be in the following modules as an NT6X50AA card:

- digital trunk controller
- line group controller
- line trunk controller
- subscriber module remote

Note: The NT6X85AA card is for SMS, SMU or SMSR use.

Functional description

The NT6X85AA uses conversion and control circuits to send and receive data between the SMS time switch (TMS) and two DS-1 links. The card uses synchronization circuits to compensate for the different clock frequency between the SLC-96 and the NT6X85AA.

Functional blocks

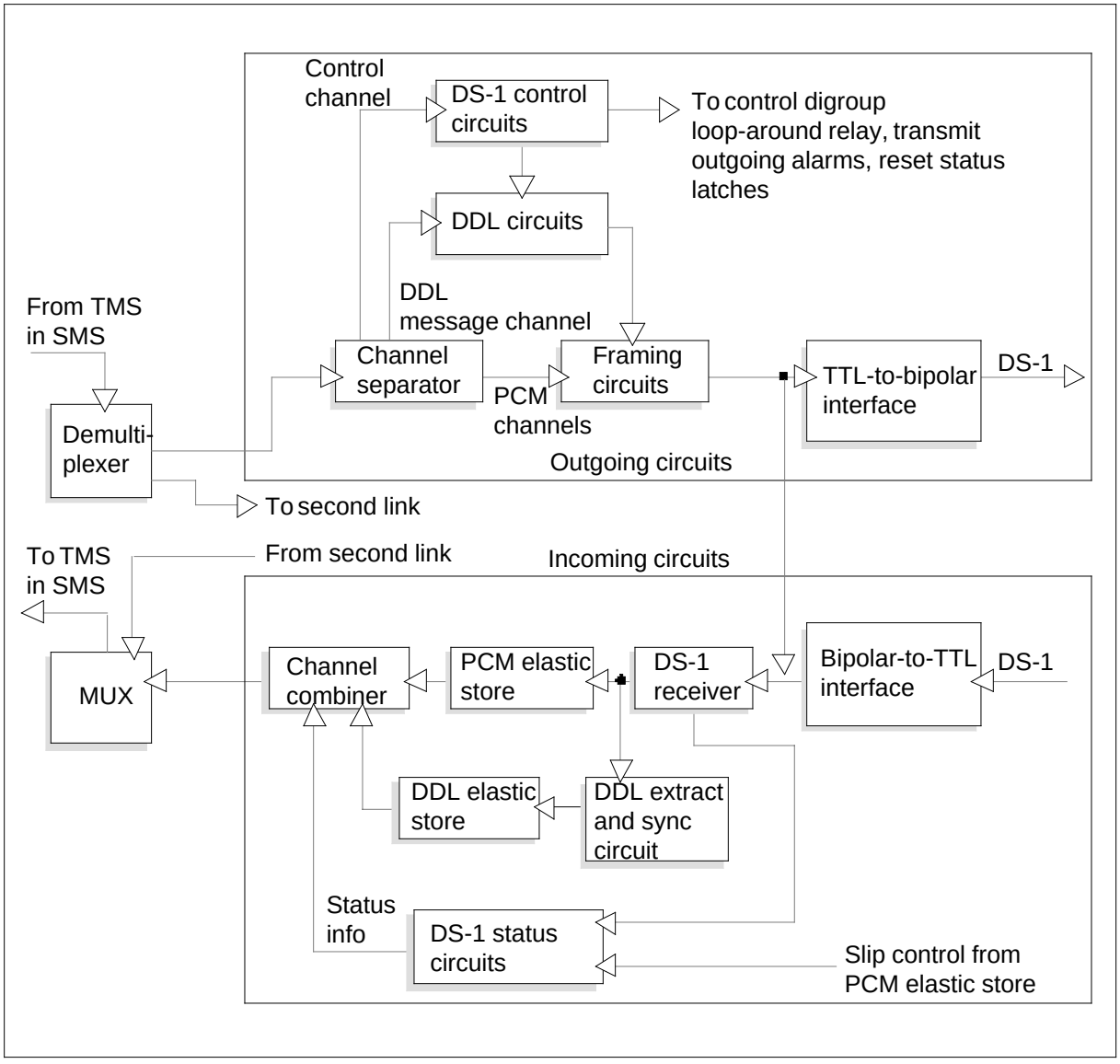
The NT6X85AA has the following functional blocks:

- demultiplexer
- channel separator
- DDL circuits
- DS-1 control circuits
- framing circuits
- transistor-transistor logic (TTL)-to-bipolar interface

NT6X85AA (continued)

- bipolar-to-TTL interface
- DS-1 receiver
- PCM elastic store
- channel combiner
- DDL extraction and synchronization circuit
- DDL elastic store
- DS-1 status circuits
- multiplexer (MUX)

NT6X85AA functional blocks



Demultiplexer

The demultiplexer receives data from the TMS over a 64-channel serial speech and message link. The circuit splits the data to two interleaved sets of 32 10-bit channels, one for each link. The demultiplexer works in a 5.12 Mbps (125 µs) frame.

NT6X85AA (continued)

Channel separator

The channel separator performs the following functions:

- receives a 32-channel frame
- sends 24 speech PCM channels to the framing circuits
- sends the DDL message channel to the DDL circuits
- sends the control channel to the DS-1 control circuits

DDL circuits

The DDL circuits latch and transfer the DDL message bit from the DDL message channel to an internal shift register. The framing circuits control the internal shift register. From the internal shift register, the system shifts the DDL message to the framing-bit time slot of the DS-1 frame.

DS-1 control circuits

The DS-1 control circuits receive the control channel from the channel separator and use the data to perform the following functions:

- transmit outgoing alarms
- reset status latches in the card
- control the digroup looparound relay for offline internal tests
- enable or disable the DDL circuits

Framing circuits

The framing circuits insert a framing bit in each outgoing DS-1 frame to format the 24 speech PCM channels. When the card operates in a non-DDL mode, the framing bits originate from the framing circuits alone. When the card operates in a DDL mode, the framing bits originate from the framing circuits and the NT6X45 SMS signal processor.

TTL-to-bipolar interface

The TTL-to-bipolar interface converts the TTL-level signals from the card to bipolar signals that DS-1 transmission require.

Bipolar-to-TTL interface

The bipolar-to-TTL interface converts the bipolar signals from the SLC-96 to TTL-level signals for the card to use.

DS-1 receiver

The DS-1 receiver accepts the TTL signal from the bipolar-to-TTL interface. The DS-1 synchronizes frames, extracts A-bits and B-bits, flags PCM data.

The receiver reports remote alarm, loss of frame alarm, and bipolar violation count information to the DS-1 status circuits.

PCM elastic store

The PCM elastic store is an elastic buffer. The PCM elastic store receives data from the DS-1 receiver and transmits the data to the channel combiner.

Channel combiner

The channel combiner receives data from the PCM elastic store, the DDL elastic store and the DS-1 status circuits. The channel combiner sends the information to the MUX for transmission to the TMS.

DDL extraction and synchronization circuit

The DDL extraction and synchronization circuit receives data from the DS-1 receiver and extracts the DDL data from the DS-1 framing bits.

DDL elastic store

The DDL elastic store is an elastic buffer that receives the extracted DDL data from the DDL extraction and synchronization circuit. The DDL elastic store sends the information to the channel combiner.

DS-1 status circuits

The DS-1 status circuits collect the information from the DS-1 receiver and the PCM elastic store. The DS-1 status circuits send the data to the channel combiner.

MUX

The MUX receives data from the channel combiner of each link. The MUX interleaves the data to a 64-channel format for transmission to the TMS.

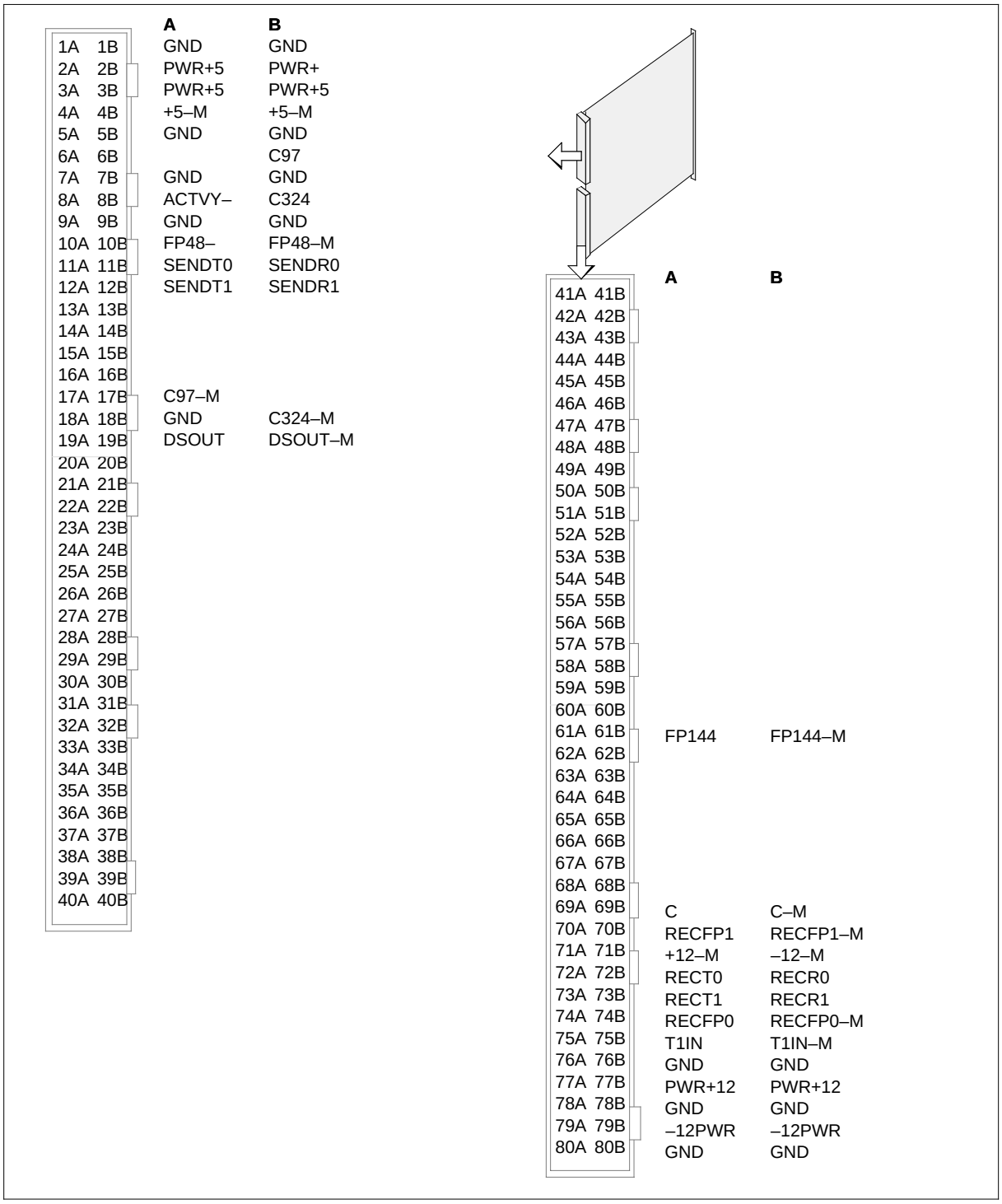
Signaling

Pin numbers

The pin numbers diagram for the NT6X85AA appears in the following figure.

NT6X85AA (continued)

NT6X85AA pin numbers



Technical data

The NT6X85AA has a mean time between failures (MTBF) of 126,230.4 h (14.4 years). The NT6X85AA has a failure rate of $7.90780/10^6$ h.

The card requires the following parts:

- a C97+ system clock signal
- a C324 master DS-1 clock signal
- an FP48-multiframe pulse
- an FP144 DDL frame pulse signal

The time switch interface has a 5.12 Mbps rate, 64 10-bit serial line time slots and bit interleave multiplexing for the data on the two DS-1 links. The DS-1 carrier interface characteristics appear in the following table.

DS-1 carrier interface characteristics

Characteristic	Value
Input data rate	1.544 Mbps ±200 bps
Output data rate	1.544 Mbps, phase locked to office clock
Structure	24 8-bit channels per frame
Code	Bipolar (50% duty cycle)
DS-1 transmitter	Output pulse height ±6 V ±.6 V; offset ±.3 V

The cable length between the DS-1 transmitter and the channel-bank repeaters ranges from 0 to 234 m. When the connection is to a DS-1 cross-connect frame, the cable length can range from 0 to 200 m. Miniature switches are provided to select one of three settings to effect cable equalization. The switch settings for S1 in offices without electromagnetic interference (EMI) protection appear in the following table.

Switch settings for S1 without EMI protection

	Switch settings							
Distance	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0 - 91 m (0 - 300 ft)	OFF	OFF	OFF	**ON**	OFF	OFF	OFF	OFF
92 - 137 m (301 - 452 ft)	OFF	**ON**	OFF	OFF	OFF	**ON**	OFF	**ON**
138 - 200 m (453 - 655 ft)	**ON**	OFF	OFF	OFF	**ON**	OFF	**ON**	OFF

NT6X85AA (continued)

The switch settings for S1 in offices with EMI protection appear in the following table.

Switch settings for S1 with EMI protection

	Switch settings							
Distance	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0 - 62 m (0 - 204 ft)	OFF	OFF	OFF	**ON**	OFF	OFF	OFF	OFF
63 - 156 m (205 - 514 ft)	OFF	**ON**	OFF	OFF	OFF	OFF	OFF	OFF
157 - 234 m (515 - 772 ft)	**ON**	OFF	OFF	OFF	**ON**	OFF	**ON**	OFF

The switch settings for S2 in offices without EMI protection appear in the following table.

Switch settings for S2 without EMI protection

	Switch settings							
Distance	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0 - 91 m (0 - 300 ft)	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF
92 - 137 m (301 - 452 ft)	OFF	**ON**	OFF	OFF	**ON**	OFF	OFF	**ON**
138 - 200 m (453 - 655 ft)	OFF	OFF	**ON**	OFF	OFF	**ON**	**ON**	OFF

The switch settings for S2 with EMI protection appear in the following table.

Switch settings for S2 with EMI protection

	Switch settings							
Distance	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0 - 62 m (0 - 204 ft)	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF
63 - 156 m (205 - 514 ft)	OFF	**ON**	OFF	OFF	OFF	OFF	OFF	OFF
157 - 234 m (515 - 772 ft)	OFF	OFF	**ON**	OFF	OFF	**ON**	**ON**	OFF

Dimensions

The dimensions of the NT6X85AA follow:

- height: 317.5 mm (12.5 in.)
- depth: 254 mm (10.0 in.)
- width: 22.2 mm (0.875 in.)

Power requirements

The power requirements for the NT6X85AA appear in the following table.

Power requirements

Voltage	Current
+5 V	1.67 A
+5 V + 10%	1.84 A
+ V	0.09 A
+12 V + 10%	0.10 A
-12 V	0.03 A
-12 V + 10%	0.03 A

NT6X85AB

Product description

The NT6X85AB DS-1 interface for SLC-96 card works in two modes: derived at a link (DDL) and non-DDL. In the DDL mode, the card functions as the DS-1 interfacing circuit pack of the peripheral subscriber module SLC-96 (SMS). In the non-DDL mode, the system disables the DDL message capability of the card. The performance of the card is identical to the NT6X50AA DS-1 interface circuit pack.

In the DDL mode, the card supports two bidirectional DS-1 links to SLC-96 remote terminals. The card contains two links for the incoming and outgoing circuits. The two links connect to DS-1 links and work separately, but perform the same functions.

Location

In the DDL mode, the card occupies one position in the SMS shelf. In the non-DDL mode, the card can be in the following modules as an NT6X50AA card:

- digital trunk controller
- line group controller
- line trunk controller
- subscriber module remote

Functional description

The NT6X85AB uses conversion and control circuits to send and receive data between the SMS time switch (TMS) and two DS-1 links. The card uses synchronization circuits to compensate for the different clock frequency between the SLC-96 and the NT6X85AB.

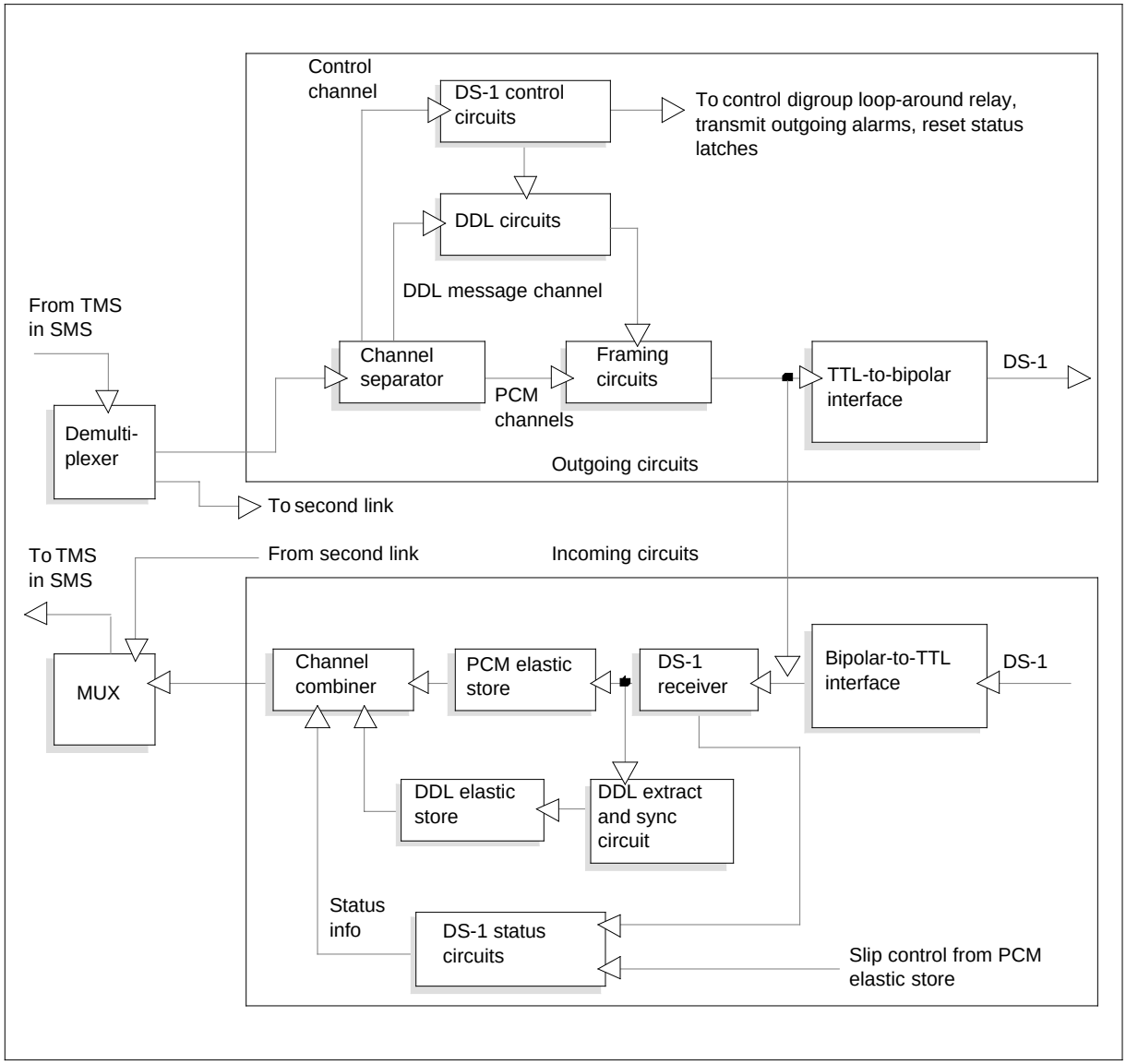
Functional blocks

The NT6X85AB has the following functional blocks:

- demultiplexer
- channel separator
- DDL circuits
- DS-1 control circuits
- framing circuits
- transistor-transistor logic (TTL)-to-bipolar interface
- bipolar-to-TTL interface
- DS-1 receiver

- PCM elastic store
- channel combiner
- DDL extraction and synchronization circuit
- DDL elastic store
- DS-1 status circuits
- multiplexer (MUX)

NT6X85AB functional blocks



NT6X85AB (continued)

Demultiplexer

The demultiplexer receives data from the TMS over a 64-channel serial speech and message link. The circuit splits the data to two interleaved sets of 32 10-bit channels, one for each link. The demultiplexer works in a 5.12 Mbps (125 µs) frame.

Channel separator

The channel separator receives a 32-channel frame and sends 24 speech PCM channels to the framing circuits. The channel separator sends the DDL message channel to the DDL circuits. The channel separator sends the control channel to the DS-1 control circuits.

DDL circuits

The DDL circuits latch and transfer the DDL message bit from the DDL message channel to an internal shift register. The framing circuits controls the internal shift register. The DDL message shifts to the framing-bit time slot of the DS-1 frame.

DS-1 control circuits

The DS-1 control circuits receive the control channel from the channel separator. The DS-1 control circuits use the data to transmit outgoing alarms. The circuits use the control channel to perform the following functions:

- reset status latches in the card
- control the digroup looparound relay for offline internal tests
- enable the DDL circuits
- disable the DDL circuits

Framing circuits

The framing circuits insert a framing bit in each outgoing DS-1 frame to format the 24 speech PCM channels. When the card operates in a non-DDL mode, the framing bits originate from the framing circuits. When the card operates in a DDL mode, the framing bits originate from the framing circuits and the NT6X45 SMS signal processor.

TTL-to-bipolar interface

The TTL-to-bipolar interface converts the TTL-level signals from the card to bipolar signals that DS-1 transmission requires.

Bipolar-to-TTL interface

The bipolar-to-TTL interface converts the bipolar signals from the SLC-96 to TTL-level signals for the card to use.

DS-1 receiver

The DS-1 receiver accepts the TTL signal from the bipolar-to-TTL interface. The DS-1 receiver synchronizes frames, extracts A-bits and B-bits, and flags PCM data.

The receiver reports remote alarm, loss of frame alarm and bipolar violation count information to the DS-1 status circuits.

PCM elastic store

The PCM elastic store is an elastic buffer. The PCM elastic store receives data from the DS-1 receiver and transmits the data to the channel combiner.

Channel combiner

The channel combiner receives data from the PCM elastic store, the DDL elastic store and the DS-1 status circuits. The channel combiner sends the information to the MUX for transmission to the TMS.

DDL extraction and synchronization circuit

The DDL extraction and synchronization circuit receives data from the DS-1 receiver. The DDL extraction and synchronization circuit extracts the DDL data from the DS-1 framing bits.

DDL elastic store

The DDL elastic store is an elastic buffer that receives the extracted DDL data from the DDL extraction and synchronization circuit. The DDL sends the information to the channel combiner.

DS-1 status circuits

The DS-1 status circuits collect the information from the DS-1 receiver and the PCM elastic store. The DS-1 status circuits sends the data to the channel combiner.

MUX

The MUX receives data from the channel combiner of each link. The MUX interleaves the data to a 64-channel format for transmission to the TMS.

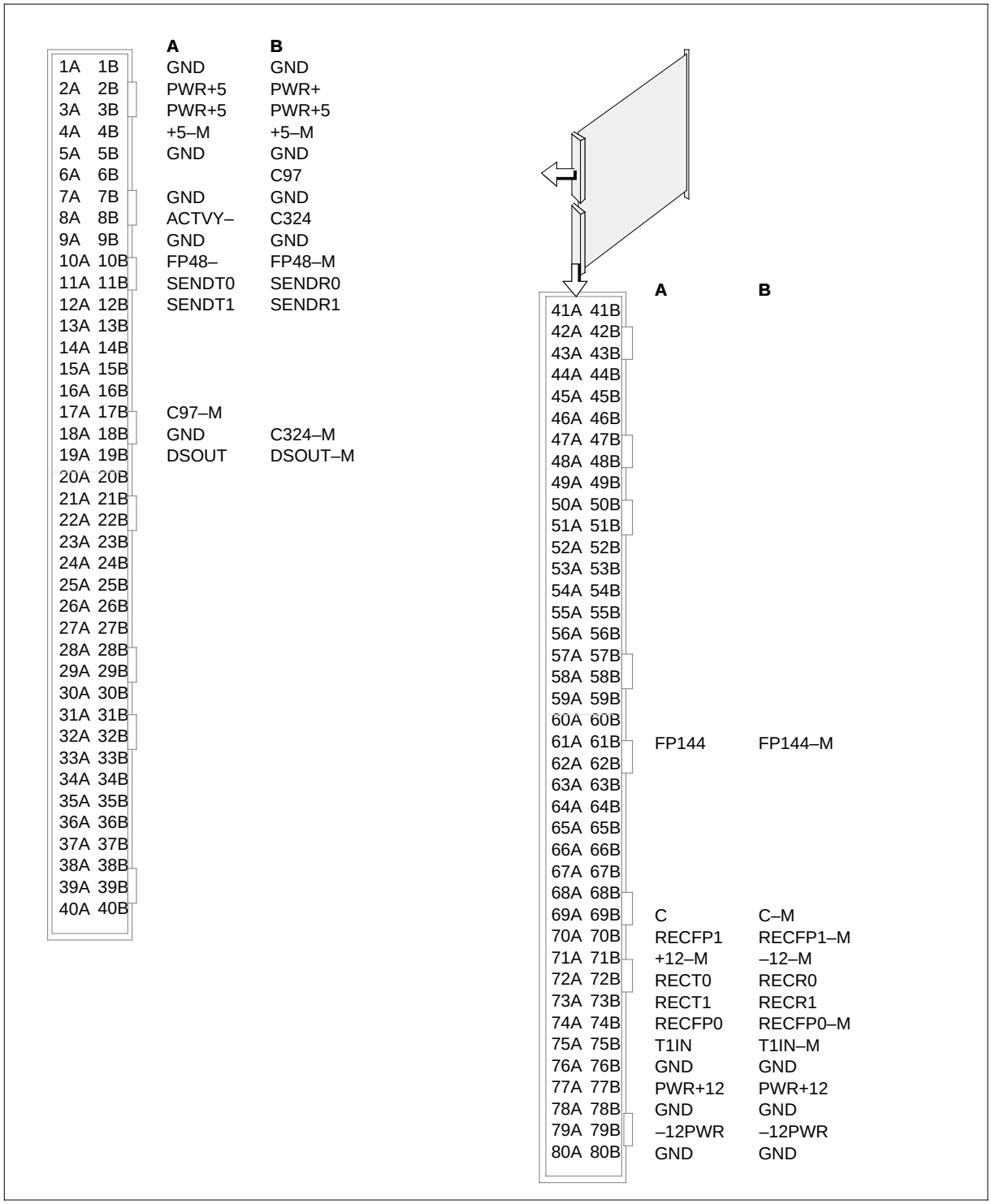
Signaling

Pin numbers

The pin numbers diagram for the NT6X85AB appears in the following figure.

NT6X85AB (continued)

NT6X85AB pin numbers



	A	B
1A 1B	GND	GND
2A 2B	PWR+5	PWR+
3A 3B	PWR+5	PWR+5
4A 4B	+5–M	+5–M
5A 5B	GND	GND
6A 6B		C97
7A 7B	GND	GND
8A 8B	ACTVY–	C324
9A 9B	GND	GND
10A 10B	FP48–	FP48–M
11A 11B	SENDT0	SENDR0
12A 12B	SENDT1	SENDR1
13A 13B		
14A 14B		
15A 15B		
16A 16B		
17A 17B	C97–M	
18A 18B	GND	C324–M
19A 19B	DSOUT	DSOUT–M
20A 20B		
21A 21B		
22A 22B		
23A 23B		
24A 24B		
25A 25B		
26A 26B		
27A 27B		
28A 28B		
29A 29B		
30A 30B		
31A 31B		
32A 32B		
33A 33B		
34A 34B		
35A 35B		
36A 36B		
37A 37B		
38A 38B		
39A 39B		
40A 40B		

	A	B
41A 41B		
42A 42B		
43A 43B		
44A 44B		
45A 45B		
46A 46B		
47A 47B		
48A 48B		
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B		
58A 58B		
59A 59B		
60A 60B		
61A 61B	FP144	FP144–M
62A 62B		
63A 63B		
64A 64B		
65A 65B		
66A 66B		
67A 67B		
68A 68B		
69A 69B	C	C–M
70A 70B	RECFP1	RECFP1–M
71A 71B	+12–M	–12–M
72A 72B	RECT0	RECR0
73A 73B	RECT1	RECR1
74A 74B	RECFP0	RECFP0–M
75A 75B	T1IN	T1IN–M
76A 76B	GND	GND
77A 77B	PWR+12	PWR+12
78A 78B	GND	GND
79A 79B	–12PWR	–12PWR
80A 80B	GND	GND

Technical data

The NT6X85AB has a mean time between failures (MTBF) of 13.49 years. The NT6X85AB has a failure rate of $8.46/10^6$h.

The card requires the following parts:

- a C97+ system clock signal
- a C324 master DS-1 clock signal
- an FP48-multiframe pulse
- an FP144 DDL frame pulse signal

The time switch interface has a 5.12 Mbps rate and 64 10-bit serial line time slots. The time switch interface also has bit interleave multiplexing for the data on the two DS-1 links. The DS-1 carrier interface characteristics appear in the following table.

DS-1 carrier interface characteristics

Characteristics	Value
Input data rate	1.544 Mbps ±200 bps
Output data rate	1.544 Mbps, phase locked to office clock
Structure	24 8-bit channels per frame
Code	Bipolar (50% duty cycle)
DS-1 receiver input signal	SCRIPT5 V to AA060 V
DS-1 transmitter	Output pulse height ±6 V ±.6 V; offset ±.3 V

The cable length between the DS-1 transmitter and the channel-bank repeaters can range from 0 to 234 m. When the connection is to a DS-1 cross-connect frame, the cable length can range from 0 to 200 m. Miniature switches are

NT6X85AB (end)

provided to select one of three settings to effect cable equalization. The switch settings for S320 and S620 switches appear in the following table.

Switch settings for S320 and S620

Distance	Switch settings							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0 - 91 m (0 - 300 ft)	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
92 - 137 m (301 - 452 ft)	OFF	OFF	ON	OFF	OFF	ON	OFF	ON
138 - 200 m (453 - 655 ft)	ON	OFF	OFF	OFF	ON	OFF	ON	OFF

Dimensions

The dimensions of the NT6X85AB are:

- height: 317.5 mm (12.5 in.)
- depth: 254 mm (10.0 in.)
- width: 22.2 mm (0.875 in.)

Power requirements

The power requirements for the appear in the following table.

Power requirements

Voltage	Current
+5 V	0.90 A
+5 V + 10%	0.99 A
+ 12 V	0.09 A
+12 V + 10%	0.10 A
-12 V	0.03 A
-12 V + 10%	0.03 A

NT6X86AA

Product description

The NT6X86AA A-bit message card is a part of the subscriber module SLC-96 (SMS). This module facilitates bidirectional A-bit and B-bit messaging and derived data link (DDL) messaging between the SMS and the subscriber line carrier (SLC-96).

Location

The card occupies one position on the SMS shelf.

Functional description

The NT6X86AA receives and transmits A-bit, B-bit, and DDL messages between the NT6X45AA signal processor (SP) and the time switch. The card uses selector circuits to select and convert the outgoing data from parallel to serial. The card also uses selector circuits to convert the incoming data from serial to parallel. The card provides looparound circuits for offline internal tests.

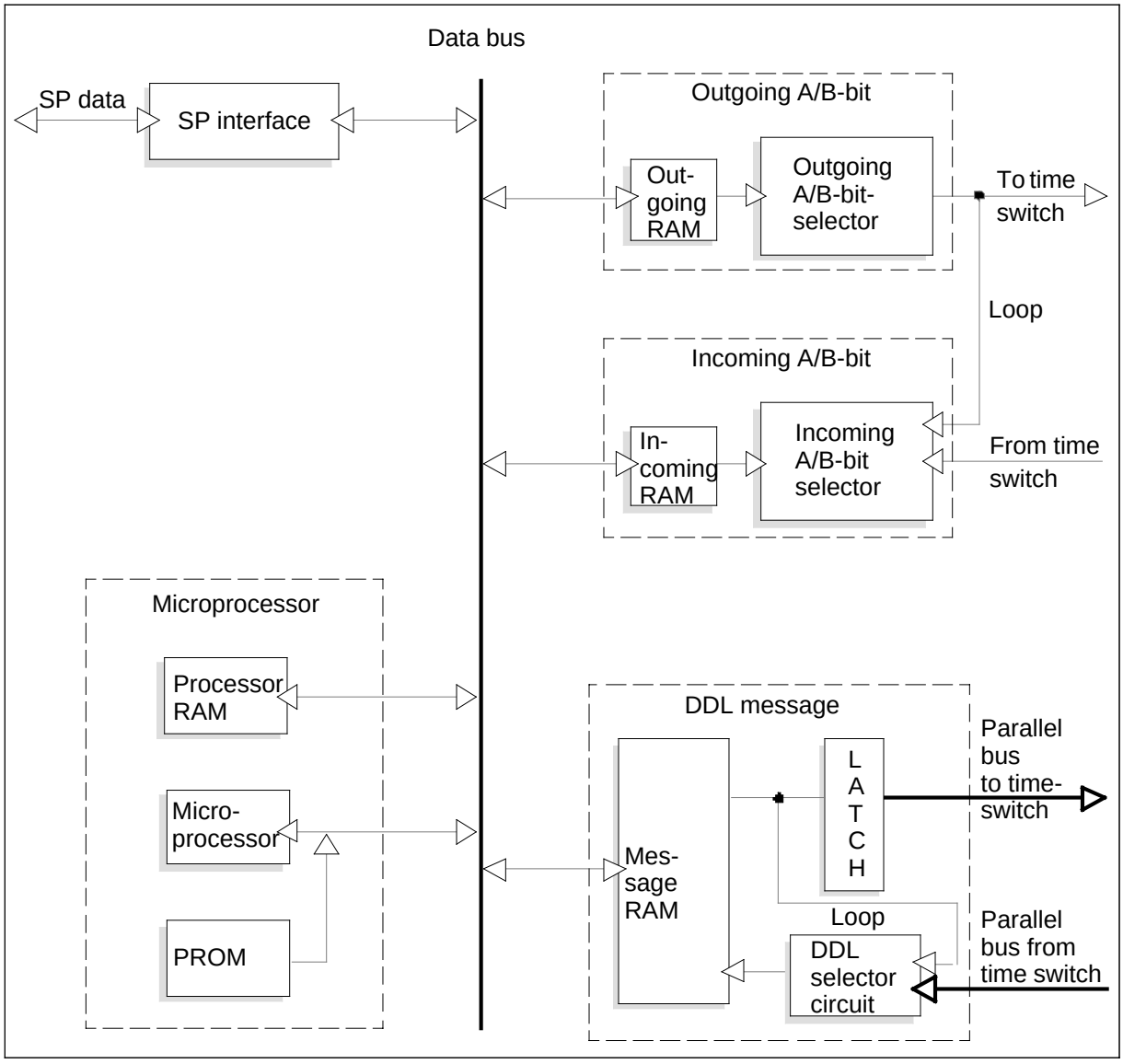
Functional blocks

The NT6X86AA has the following functional blocks:

- SP interface
- outgoing RAM
- outgoing A/B-bit selector
- incoming A/B-bit selector
- incoming RAM
- processor RAM
- microprocessor
- PROM
- message RAM
- DDL selector circuit
- latch circuit

NT6X86AA (continued)

NT6X86AA functional blocks



SP interface

The SP interface transfers A and B message bits, A-bit and B-bit data, and instructions between the card and the SP. The circuit synchronizes the SP with the internal memory cycles of the card. The circuit provides decode, arbitration and buffer functions to prevent memory conflicts.

Outgoing RAM

The outgoing RAM stores A-bit and B-bit values from the SP. The outgoing RAM sends the values to the outgoing A/B-bit selector.

Outgoing A/B-bit selector

The outgoing A/B-bit selector receives the parallel A-bit and B-bit values from the outgoing RAM. The outgoing A/B-bit selector converts the bits to serial data. The outgoing A/B-bit selector sends the values to the time switch. The selector sends the A-bit values during the first six frames of a DS-1 master frame. The selector sends the B-bit values during the last six frames.

Incoming A/B-bit selector

The incoming A/B-bit selector selects A-bits and B-bits from the A/B-bit loop or the incoming serial data link. The incoming A/B-bit selector converts the data to a format acceptable to the SP. The selector sends the data to the incoming RAM. The system updates the data bits one time every 12 frames (1.5 ms).

Incoming RAM

The incoming RAM receives A-bits and B-bits from the incoming A/B-bit selector. The incoming RAM stores the values until the SP reads the values.

Processor RAM

The processor RAM receives control and status information for the microprocessor. The RAM is accessible through the microprocessor and the SP.

Microprocessor

The microprocessor encodes outgoing DDL messages so that the messages conform to SLC-96 protocol. The microprocessor decodes incoming DDL messages for transmission to the SP.

PROM

The PROM, which connects to the microprocessor, contains the operating instructions for the microprocessor.

Message RAM

The message RAM stores outgoing and incoming DDL messages and operates as a buffer for the SP and the microprocessor.

DDL selector circuit

The DDL selector circuit selects DDL messages from the DDL looparound bus or the incoming parallel speech bus. The DDL selector circuit sends the messages to the message RAM for transmission to the SP.

NT6X86AA (continued)

Latch circuit

The latch circuit receives data from the message RAM. The latch circuit buffers the data before the circuit sends the data to the time switch through a parallel data bus.

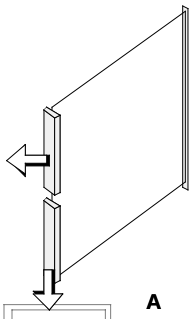
Signaling

Pin numbers

The pin number diagram for the NT6X86AA appears in the following figure.

NT6X86AA (continued)

NT6X86AA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	+5 V	+5 V
3A 3B	+5 V	+5 V
4A 4B	+5 V	+5 V
5A 5B	GND	GND
6A 6B	FP–	C97+
7A 7B	GND	GND
8A 8B		FP48–
9A 9B		
10A 10B		
11A 11B	GND	GND
12A 12B	AS–	TEST1
13A 13B	LDS–	TEST2
14A 14B	DTACK–	TEST3
15A 15B	UDS–	TEST4
16A 16B	WRT–	
17A 17B		ABOUT–
18A 18B	SRSTOUT–	ABIN–
19A 19B		
20A 20B		
21A 21B	PIN0	POUT0
22A 22B	PIN1	POUT1
23A 23B	PIN2	POUT2
24A 24B	PIN3	POUT3
25A 25B	PIN4	POUT4
26A 26B	PIN5	POUT5
27A 27B	PIN6	POUT6
28A 28B	PIN7	POUT7
29A 29B	ADDR01	
30A 30B	ADDR02	
31A 31B	ADDR03	
32A 32B	ADDR04	
33A 33B	ADDR05	
34A 34B	GND	GND
35A 35B	ADDR06	
36A 36B	ADDR07	
37A 37B	ADDR08	
38A 38B	ADDR09	
39A 39B	ADDR10	
40A 40B	ADDR11	

	A	B
41A 41B		
42A 42B	ADDR12	
43A 43B	ADDR13	
44A 44B	ADDR14	
45A 45B	ADDR15	
46A 46B	ADDR16	
47A 47B	ADDR17	
48A 48B	ADDR18	SAMD17
49A 49B	ADDR19	SADM18
50A 50B	ADDR20	SADM19
51A 51B	ADDR21	
52A 52B	SEN0	
53A 53B	SEN1	
54A 54B	SEN2	
55A 55B	FP144–	FP144–M
56A 56B		
57A 57B		
58A 58B	DATA00	
59A 59B	DATA01	
60A 60B	DATA02	
61A 61B	DATA03	
62A 62B	DATA04	
63A 63B	DATA05	
64A 64B	GND	GND
65A 65B	DATA06	
66A 66B	DATA07	
67A 67B	DATA08	
68A 68B	DATA09	
69A 69B	DATA10	
70A 70B	DATA11	
71A 71B	DATA12	
72A 72B	DATA13	
73A 73B	DATA14	
74A 74B	DATA15	
75A 75B		
76A 76B	GND	GND
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

NT6X86AA (continued)

Technical data

The NT6X86AA has a mean time between failures (MTBF) of 165,463.6 hours (18.9 years). The NT6X86AA has a failure rate of $6.04362/10^6$ hours.

The card requires the following items:

- a master clock signal
- a DS-1 frame pulse signal
- a master frame pulse signal
- a service enable signal

The time switch uses A/B output data (ABOUT) and A/B input data (ABIN) interface signals. A list of the microprocessor to SP interface signals appears in the following table.

Microprocessor to SP interface signals

Interface signal	Description
SADM17 - SADM19	Determines the board address of the card
ADDR01 -ADDR21	21-bit, unidirectional, tristate address bus
DATA08 -DATA15	8-bit, bidirectional, tristate data bus
Delayed address strobe (DAS)	Indicates a valid address
Read/write (R/W)	Defines the data bus transfer as an external read or write signal
Upper and lower data strobes (UDS, LDS)	Indicates valid data on the data bus
Data acknowledge (DTACK)	Indicates completion of data transfer; card generated
SRSTOUT	Master reset

Dimensions

The dimensions of the NT6X86AA follow:

- height: 317.5 mm (12.5 in.)
- depth: 254 mm (10.0 in.)
- width: 22.2 mm (0.875 in.)

Power requirements

The power requirements for the NT6X86AA are a voltage of +5V ± 10% and a current of 3.50 A.

NT6X87AB

Product description

The NT6X87AB data above voice line card (DAVLC) 500/2500 (4-slot) operates with a subscriber access multiplexer (SAM). The DAVLC and the SAM operate to provide circuit-switched data. This data is for customers that connect to a DMS-100 switching office or DMS-100 remote facilities.

The card allows the system to transmit voice and data service over a single pair of wires. The transmission of voice and data service occurs between the central office and the subscriber, at the same time.

Location

The card occupies four slots in a line concentrating module (LCM) line card drawer (LCD). The card requires four vertical slots, two slots in each of the two logical drawers.

Functional description

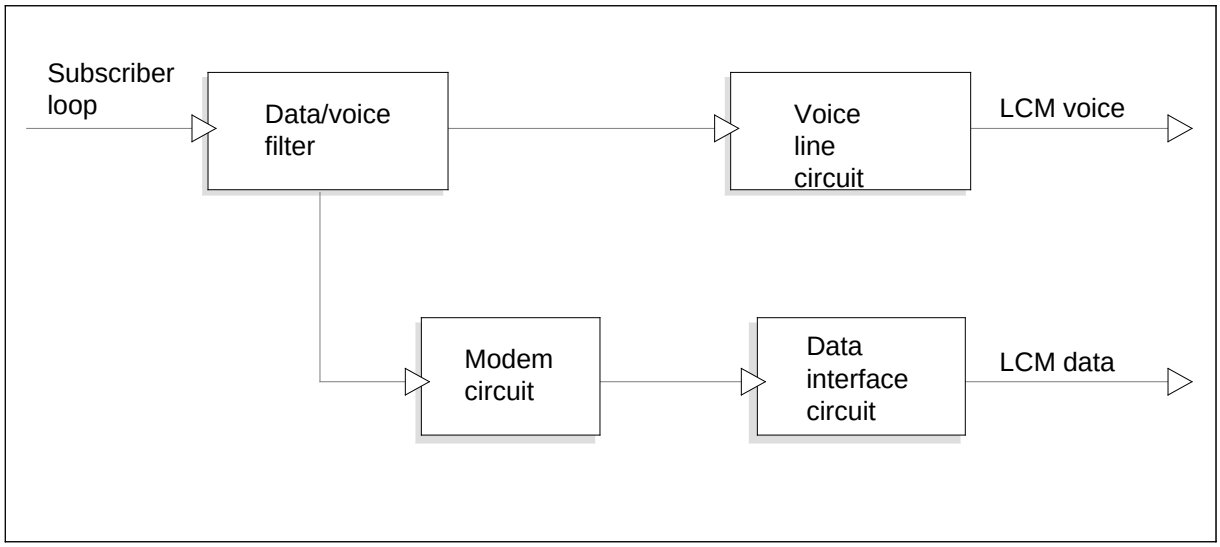
The NT6X87AB separates voice and data signals. The card provides analog-to-digital (A/D) and digital-to-analog (D/A) conversion and loop supervision to control voice calls. The card provides modulation and demodulation for carriers that send data over the subscriber loop. The card formats data to T-link protocol for transmission over a digital switched network.

Functional blocks

The NT6X87AB has the following functional blocks:

- data/voice filter
- voice line circuit
- modem circuit
- data interface circuit

NT6X87AB functional blocks



Data/voice filter

The data/voice filter separates the voice and data signals in the subscriber loop. The filter sends -3kHz voice signals to the voice interface circuit. The filter sends 20-kHz to 80-kHz data signals to the modem circuit.

Voice line circuit

The voice line circuit provides the following functions:

- A/D and D/A conversion of the voice signals
- loop supervision
- ringing connection
- loop testing
- battery feed

The circuit provides these functions to control voice calls. The output of the circuit connects to a 64-Kbps pulse code modulation (PCM) channel in the LCM.

Modem circuit

The modem circuit provides modulation and demodulation for the carriers that send data over the subscriber loop. The circuit sends data on a 76-Hz carrier frequency, and couples the high frequency signals in and out of the loop. The circuit amplifies and demodulates 28-kHz signals from the SAM, and detects the presence of a carrier on the subscriber loop.

NT6X87AB (continued)

Data interface circuit

The data interface circuit uses an internal microprocessor to format the data to T-link protocol for transmission over the digital switched network. The output of the circuit connects to a 64-Kbps PCM channel in the LCM.

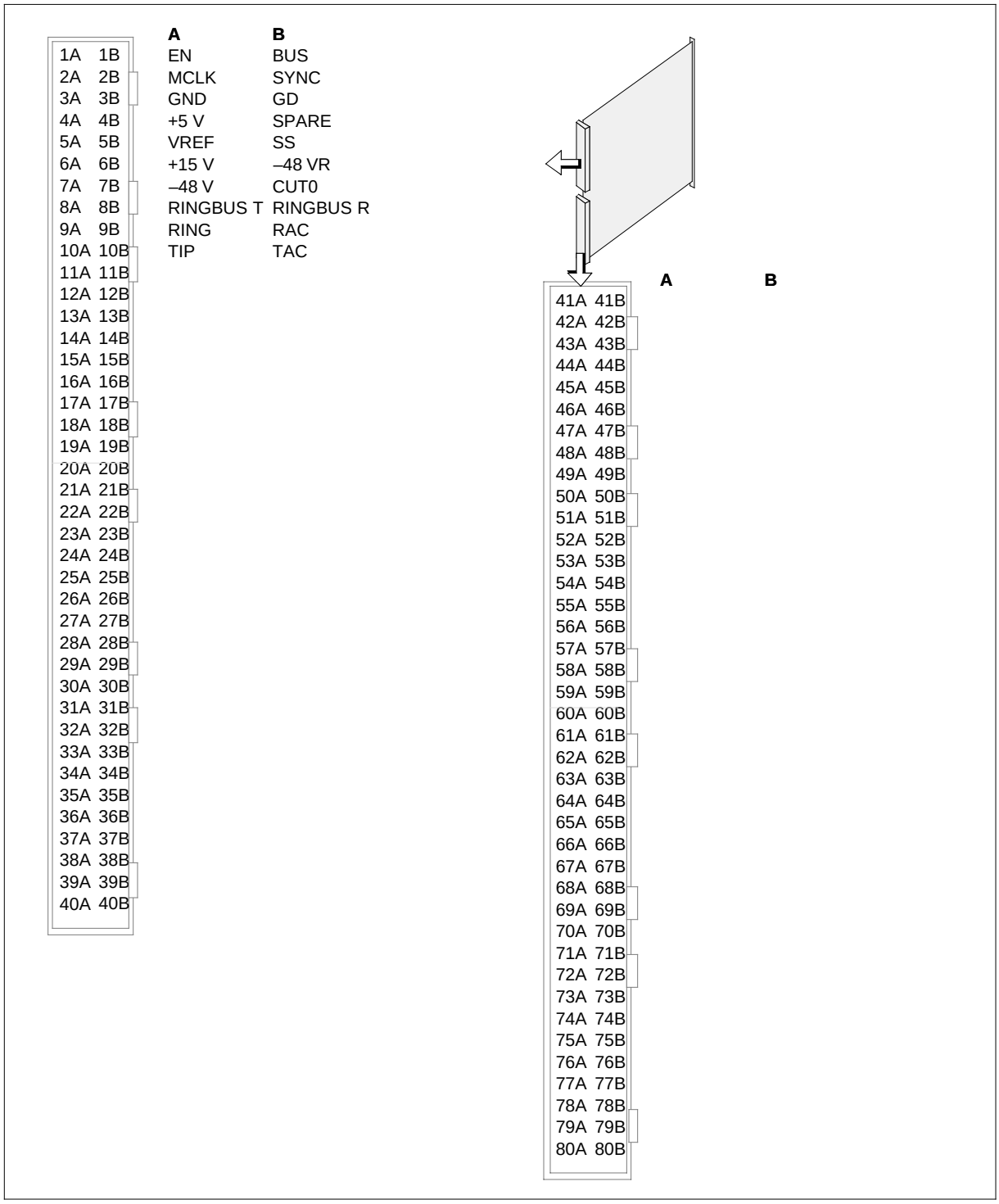
Signaling

Pin numbers

The pin number diagram for the NT6X87AB appears in the following figure.

NT6X87AB (continued)

NT6X87AB pin numbers



NT6X87AB (continued)

Technical data

A list of the transmission specifications for the DAVLC and SAM ends of the subscriber loop appears in the following table.

Transmission specifications

Characteristic	Value
Data rate	110, 150, 300, 600, 1200, 2400, 4800, and 9600 bps (+1% to -2%)
Operating mode	Full duplex
Operating format	Asynchronous; 7 bit plus parity or 8 bit without parity Mark, space, odd, or even parity 2 stop bits for 110 bit rate,1 stop bit for other rates
Modulation	Continuous phase, frequency shift keying
Line impedance	900Ω at 0.3 kHz to 3.3 kHz 135Ω at 20 kHz to 80 kHz
Frequencies	LC to SAM: 72-kHz space, 80-kHz mark SAM to LC: 24-kHz space, 32-kHz mark 4 kHz -15% deviation -2% center frequency accuracy
Transmit levels	LC to SAM: 76 kHz at 7 dBm maximum (no AGC) SAM to LC: 28 kHz at 10 dBm maximum (AGC) 15dB AGC SAM TX level reduction Maximum SAM TX level: -5 dBm with zero loop loss
Maximum loop loss	55 dB at 80 kHz 42 dB at 32 kHz
Minimum receive levels	-32 dBm at 32 kHz -48 dBm at 80 kHz
Carrier detect thresholds	-53 dBm at 80 kHz (at SAM) -36 dBm at 32 kHz (at LC)
Bit error rate	10^{-7} at 9.6 Kbps between SAM and DAVLC

Dimensions

The dimensions of the NT6X87AB follow:

- height: 19 mm (0.75 in.)
- depth: 300 mm (11.80 in.)
- width: 90 mm (3.54 in.)

Power requirements

The power requirements for the NT6X87AB appear in the following table.

Power requirements

	Voltage	Current
Data interface and modem	15 V	70 mA
Voice interface	15 V	23 mA

NT6X92AA

Product description

The NT6X92AA universal tone receiver card identifies and processes pulse code modulation (PCM) tones. These tones come from 32 voice channels on the parallel speech bus of the common peripheral controller (CPC) in DMS–100 equipment.

The card can detect a maximum of 128 frequencies of A–law or μ–law tones like the following:

- dual tone multi–frequency (DTMF)
- multi–frequency (MF)
- compelled multi–frequency (CMF)
- common channel interoffice signaling (CCIS)
- special information tone (SIT)

Location

The card occupies one position in the following CPC shelves:

- line group controller (LGC)
- line trunk controller (LTC)
- digital trunk controller (DTC)
- international digital trunk controller (IDTC)

Functional description

The NT6X92AA card receives PCM tone samples from the parallel speech bus, and analyzes the samples to identify the tones. The card translates the tones to digits for transmission to the NT6X46 signal processor (SP). The card provides error detection when the card cannot translate the tones to valid digits.

Functional blocks

The NT6X92AA has the following functional blocks:

- sequencer
- input buffer
- analyzer
- local processor
- signal processor interface

Sequencer

The sequencer schedules the read mode for PCM samples that the input buffer receives. The sequencer also schedules the write mode for tone samples that the input buffer sends to the analyzer.

Input buffer

The input buffer uses a 6–Kbyte RAM to store tone samples for each of the 32 channels on the speech bus. The buffer is in a read mode when the buffer sends data from the speech bus. The buffer is in a write mode when the buffer sends data to the analyzer.

Analyzer

The analyzer uses two microprocessors to identify and store a maximum of eight power levels from the switched channel. The analyzer notifies the local processor of the most dominant frequency or tone. The analyzer sends the results to the local processor every 375 ms.

Local processor

The local processor contains a microprocessor with an 8–Kbyte ROM and an 8–Kbyte RAM. The ROM and RAM receive tone combinations from the analyzer. The ROM and RAM determine if the tones are in A–law or μ–law format. The processor translates each tone to a valid digit, when possible. The processor performs error–detection tests when the translation is not possible. The system sends the valid digit or error code to the SP interface.

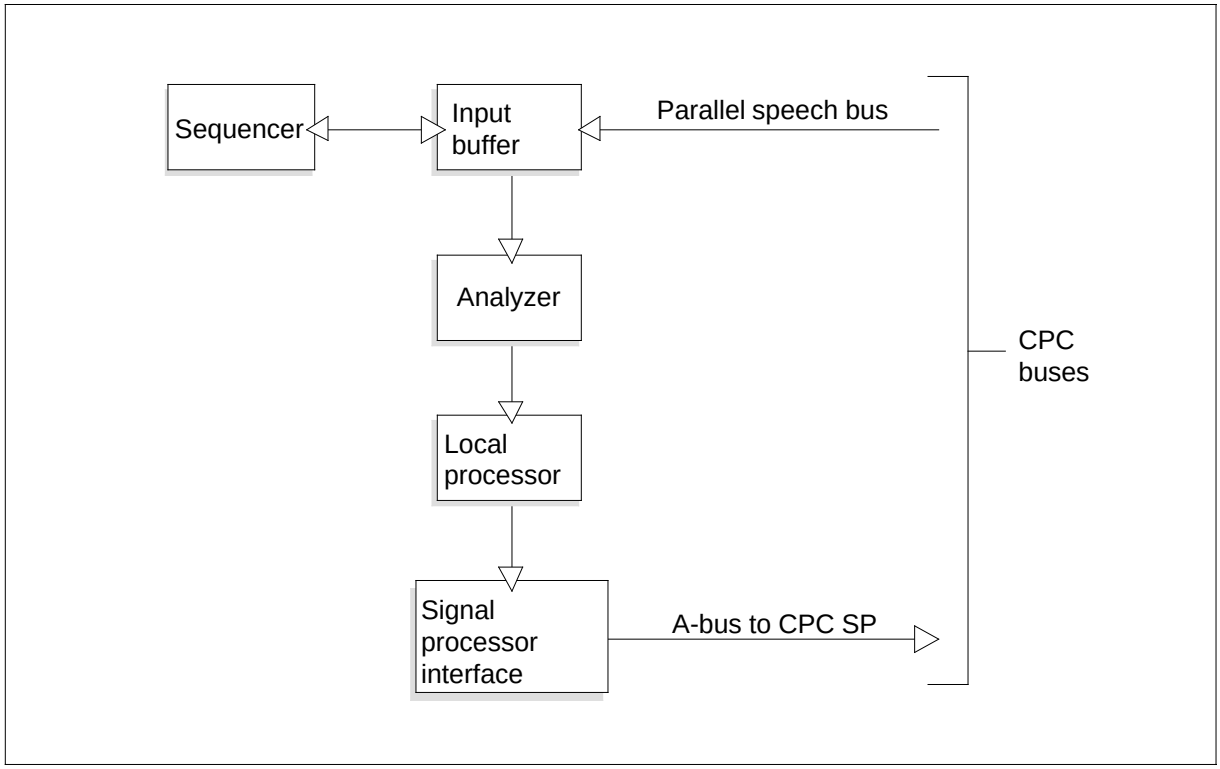
Signal processor interface

The SP interface transmits the valid digit to the NT6X46 SP and exchanges messages between the card and the CPC SP. The interface contains a 1–K RAM circuit for data exchange use. The local processor and the CPC SP access the interface. One processor is put on hold while the other processor accesses the interface.

The relationship between the functional blocks appears in the following figure.

NT6X92AA (end)

NT6X92AA functional blocks



Technical data

The NT6X92AA has a 4–kHz maximum input frequency that is possible to detect and a +3.75 dBm to -60dBm input power level range.

Dimensions

The dimensions of the NT6X92AA follow:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 20 mm (0.78 in.)

Power requirements

The power requirements for the NT6X92AA are a voltage of +5 V dc and a current of 3.5 A.

NT6X92BB

Product description

The NT6X92BB domestic universal tone receiver (UTR) is a 30–channel receiver. The UTR detects, processes and identifies valid dual–tone multifrequency (DTMF) and multifrequency (MF) tones. The UTR receives the DTMF and MF tones from the voice channels of the parallel speech bus of the common peripheral controller (CPC).

The firmware in the NT6X92BB is compatible backwards with the firmware in the NT6X92BA. The firmware in the NT6X92BB is not compatible with the firmware in the earlier version card, the NT6X92AA.

Location

A single extended multiprocessor system (XMS)–based peripheral module (XPM) shelf can contain one or two UTRs. The UTR can fit in slot 15, 16 or 17 of the following CPC shelves:

- the digital trunk controller (DTC)
- the line trunk controller (LTC)
- the line group controller (LGC)
- the remote switching center (RSC)

Functional description

The NT6X92BB receives DTMF and MF tone samples from 30 voice channels on the parallel speech bus. The NT6X92BB analyzes the samples to identify the tones. The NT6X92BB translates the tones into digits for transmission to the NT6X45 signal processor (SP). The card provides error detection if the NT6X92BB cannot translate into valid digits.

The UTR receives tone samples transmitted on the parallel speech bus. The input buffer stores the samples, and the samples pass through the correlator. The correlator filters the samples to detect tones of a DTMF or MF signaling set.

The signaling set that the UTR currently monitors on a particular channel determines which frequency bands are filtered. The local processor (LP) passes the signaling set information to the correlator. This occurs each time a UTR channel is assigned to perform a reception task.

After the UTR filters each frequency band, the power calculator calculates the power level of the filter output. The power level is stored in the sorter. The sorter reads the power level of the filters and arranges the results in descending power order for the LP.

NT6X92BB (continued)

The local processor analyzes the filter outputs and identifies the tones. When the LP identifies a valid tone, the digit results are returned to the SP through a common memory area. The SP uses the common memory to initialize the UTR, and to invoke diagnostics on the UTR. The SP also uses the common memory to instruct the UTR to perform reception tasks on specified channels.

Functional blocks

The NT6X92BB has the following functional blocks:

- the parallel speech bus interface
- the input tone sample buffer
- the correlator
- the power calculator
- the sorter
- local processor
- the signaling processor interface
- timing and control

The relationships of the functional blocks appears in the following figure.

Parallel speech bus interface

The NT6X44AA time switch card in the LTC or DTC detects and transmits pulse code modulation (PCM) tone samples on to the parallel speech bus (XPCM–bus). This event occurs under XPM software control. The card must be set to the appropriate port because the UTR collects data from only one of the two ports at a time. Ports 16 and 17 are reserved for this purpose. The SP sets the port during initialization. The XPCM–bus receives data once every channel time. A channel time contains 3.9 μs.

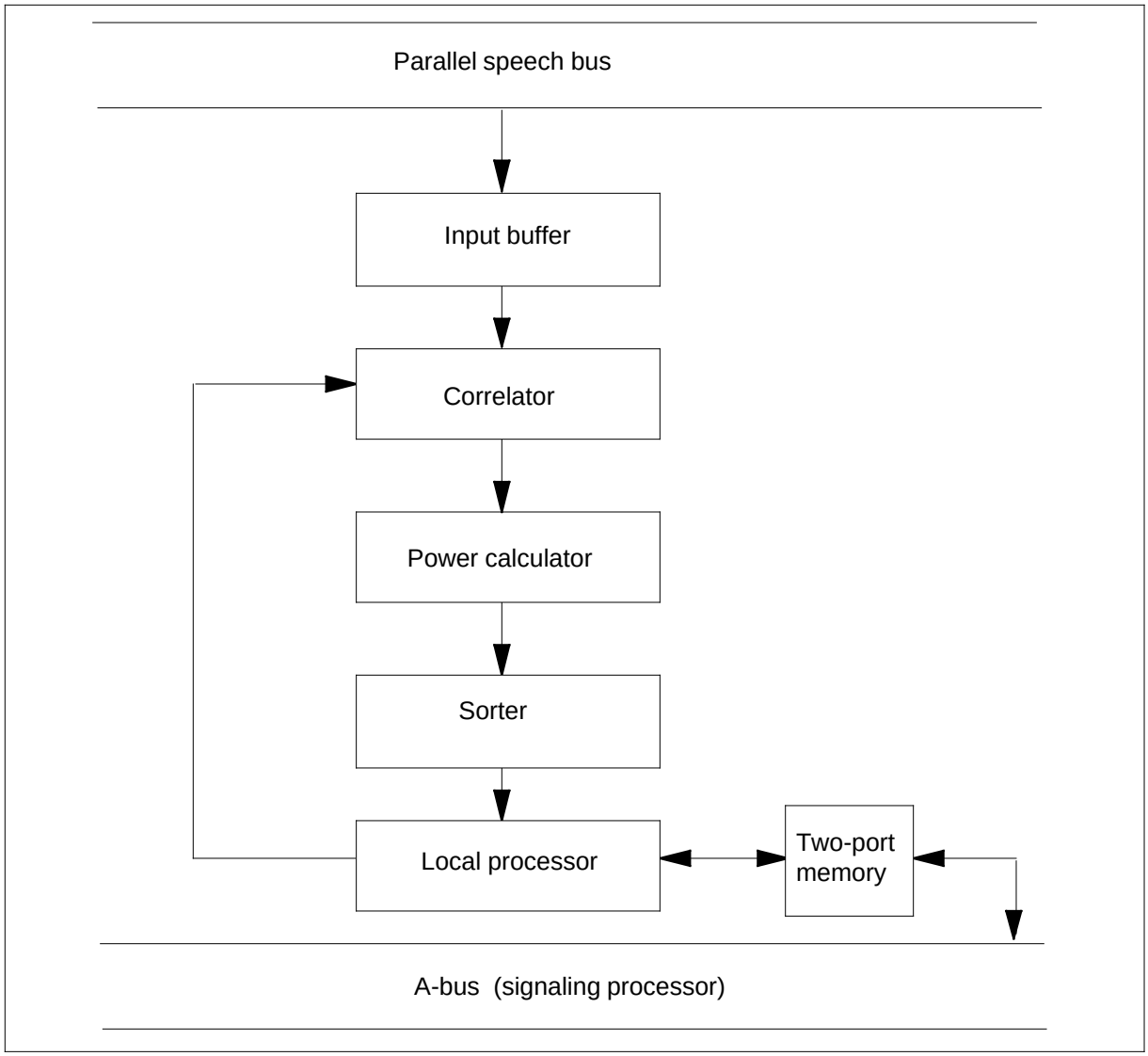
Channels 0 and 16 of the XPCM–bus contain signaling information. These channels are not used for tone reception.

Input tone sample buffer

The input tone sample buffer stores the tone samples that the parallel speech bus interface latches from the 30 channels. The input tone sample buffer also stores data for channels 0 and 16 for hardware simplicity. These two channels are not used for tone reception.

The buffer stores 192 samples for each channel. The buffer is organized as a ring so the buffer can always store the recent 192 samples. Hardware address counters read tone samples and pass the samples to the correlator.

NT6X92BB functional blocks



Correlator

The correlator filters the tone samples from the input buffer for selected frequencies. The correlator performs this action to detect the tones of DTMF or MF signaling sets. As the correlator filters, the correlator measures the following:

- the total power of the signal
- the speech power between 400 Hz and 480 Hz
- the signaling frequencies that the signaling set defines for that channel

NT6X92BB (continued)

Power calculator

The correlator transmits information about low signal power to the power calculator. The calculator determines the power level of each filter.

Sorter

The sorter performs the following functions:

- collects results from the power calculator output
- sorts the results in order of power amplitude
- adjusts the power level values if the automatic gain control (AGC) is set
- transmits the results to the local processor

Two channel times are necessary to process the results from one channel (375 µs for each channel). The first channel time collects the filter results from the power calculator and adjusts power levels, if required. Power levels can require adjustment because previous AGC changes occurred.

In the second channel time, the sorter routine chooses the filters with the three highest power levels. The sorter transmits the results from the following filters to the LP:

- the total power filter
- the lowband filter
- the three highest powered separate tone filter results

Local processor

The local processor operates at 6 MHz. The LP uses an 8–kbyte EPROM and an 8–kbyte RAM.

The local processor performs the following functions:

- exchanges messages with the signaling processor
- analyzes the filter results and identifies tones
- updates the code map RAM and filter RAM on command from the SP
- selects between A–law and µ–law PROMs
- selects the parallel speech bus port number

Signaling processor interface

The signaling processor interface contains address decode circuits, arbitration circuits, and a 1–K RAM. The interface allows communication between the NT6X45 signaling processor card and the LP in the NT6X92BB card. The LP communicates with the signaling processor on a common two–port RAM.

Arbitration circuits places one processor on hold if the other processor has access to the memory.

Timing and control

The timing and control block uses a PROM to provide timing signals for the correlator, the power calculator and the sorter.

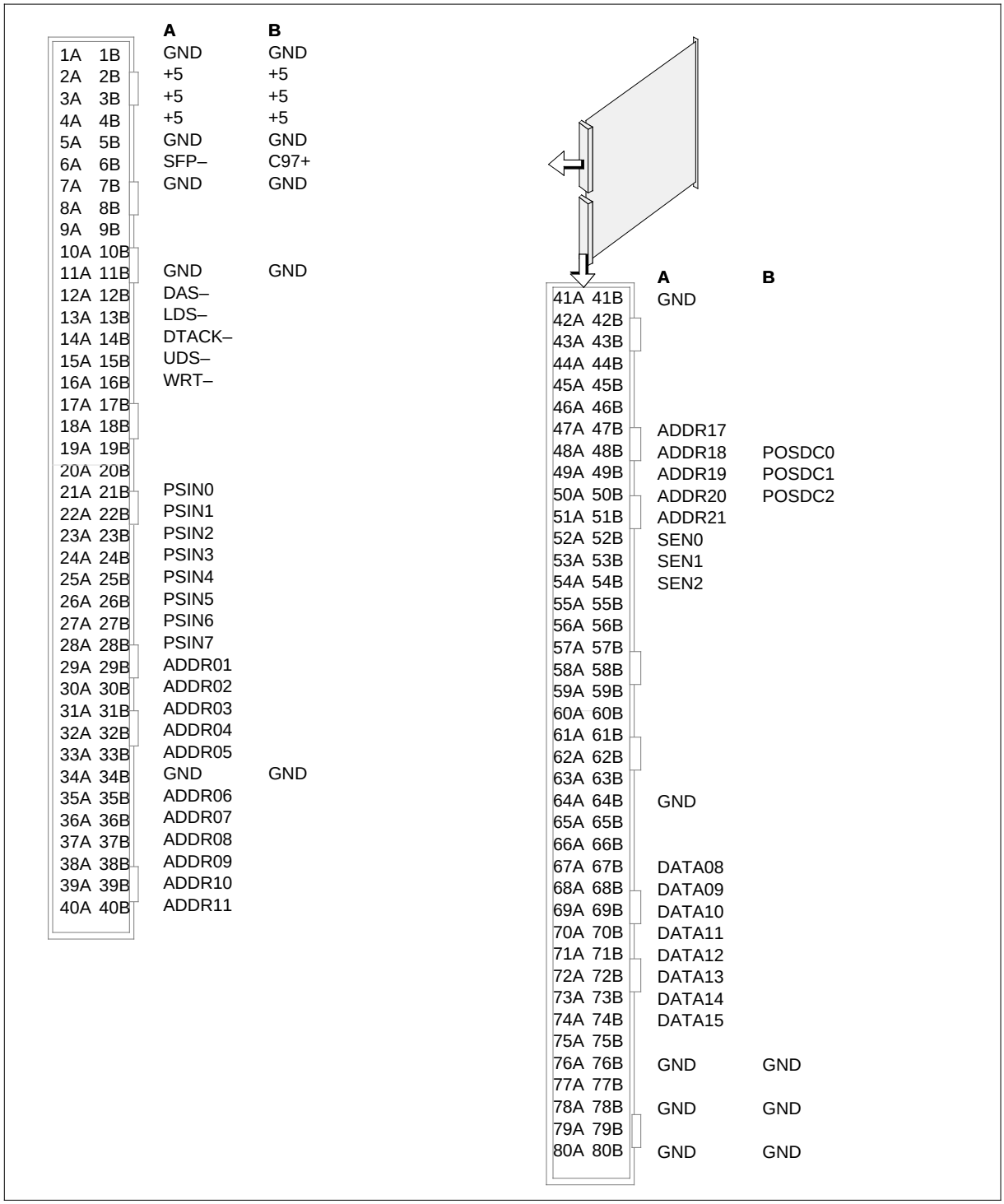
Signaling

Pin numbers

The pin numbers for the NT6X92BB appear in the following figure.

NT6X92BB (end)

NT6X92BB pin numbers



NT6X92BC

Product description

The NT6X92BC identifies and processes pulse code modulated (PCM) tones from 30 voice channels. The parallel speech bus of the common peripheral module (CPM) of the DMS–100 switch contains the 30 voice channels. The universal tone receiver can detect a maximum of 128 frequencies of A–law or u–law tones. These tones include the following:

- dual–tone multifrequency (DTMF)
- multifrequency compelled (MFC)
- common channel interoffice signaling (CCIS)
- special information tones

The XPM can be any part of the family of CPM systems which include the following:

- the line group controller (LGC)
- the line trunk controller (LTC)
- the digital trunk controller (DTC)
- the remote cluster controller (RCC)
- the integrated services digital network (ISDN)
- variants of the XPM (LGCI, LTCI, RSCI) and their international variations (ILGC, IDTC)

The NT6X92BC features lower power use and improved multifrequency tone reception. The NT6X92BC is based on application–specific integrated circuit (ASIC) technology. The NT6X92BC is fully backwards compatible to the NT6X92BB. The NT6X92BB is a non–ASIC version of this card.

Location

The NT6X92BC fits in slots 15, 16 or 17 of the common peripheral shelf.

Functional description

The NT6X92BC collects tone samples that the NT6X44 time switch switches the parallel speech bus. The input buffer stores the received samples of all 32 channels. The buffer reads the samples of each channel. The samples pass through the correlator. The correlator filters the samples to determine the tones of the signaling set. The signaling set that the NT6X92BC monitors on a particular channel determines the frequency bands filtered. The LP passes the signaling set information to the correlator. The LP passes this information each time a universal tone receiver channel is assigned to perform a reception task.

NT6X92BC (continued)

After each frequency is filtered, the power calculator calculates the power level of the filter output. The sorter stores the power level of the filter output. The sorter collects the power level of the filters and arranges the results in descending power order for the LP.

The LP analyzes the filter outputs and identifies the tone. When the LP identifies a valid tone, the digit results return to the processor. The digit results return to the processor on the CPM through a common buffer on the NT6X92BC. The signaling processor also uses the common buffer to perform the following tasks:

- to initialize the NT6X92BC
- to invoke diagnostics on the NT6X92BC
- to instruct the NT6X92BC to perform tone reception tasks on specified channels

Functional blocks

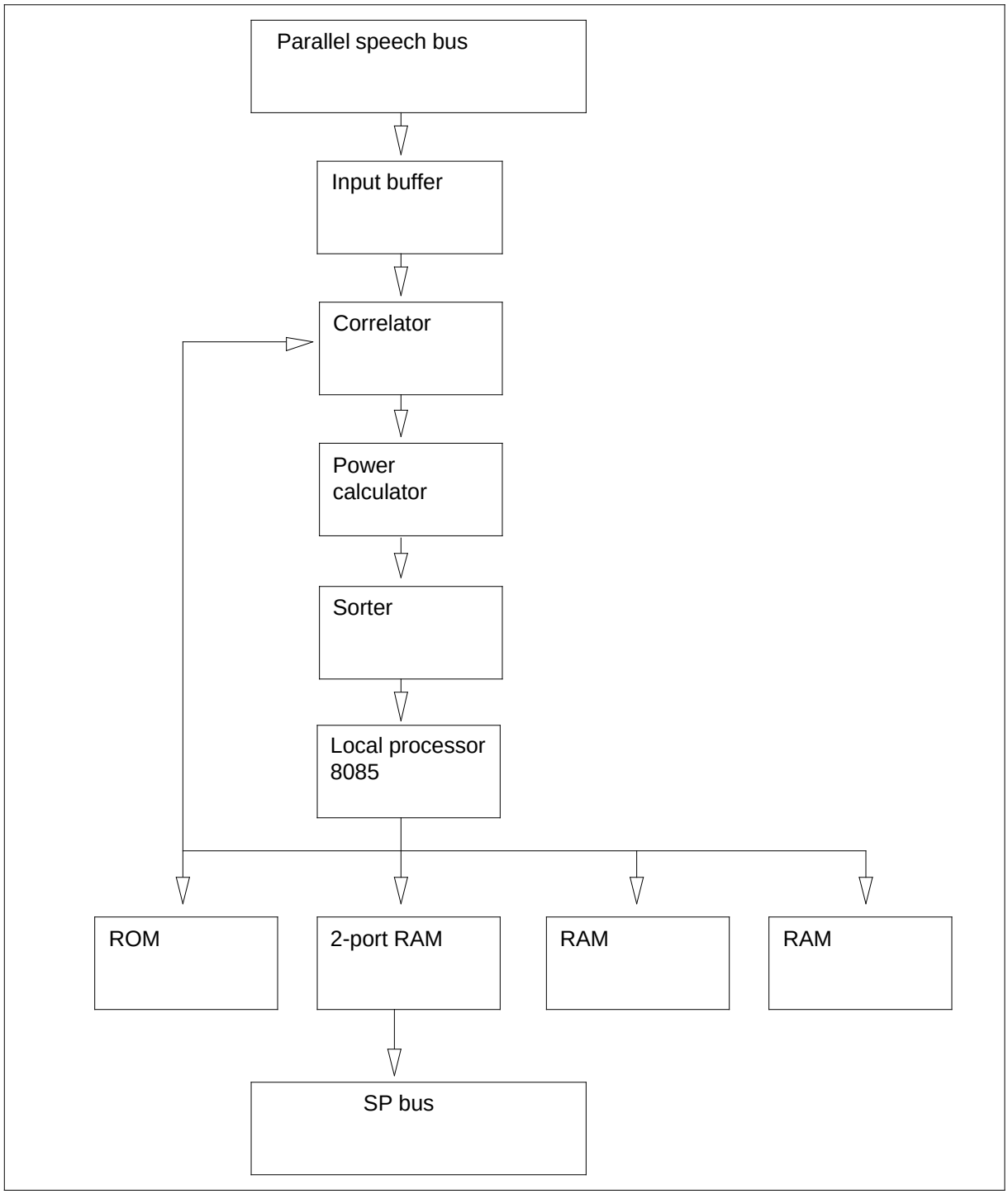
The NT6X92BC contains the following functional blocks:

- a parallel speech bus interface
- an input tone sample buffer
- a correlator
- a power calculator
- a sorter
- a local processor
- an SP interface
- timing and control

The relationship between the functional blocks appears in the following figure.

NT6X92BC (continued)

NT6X92BC functional blocks



NT6X92BC (continued)

Parallel speech bus interface

The parallel speech bus interface contains a parallel latch and the associated clock signal circuitry. The clock signal circuits generates the clock signal (TONECH) for this latch. Data is collected from port 16 or 17. The number of port the SP initializes for tone reception determines the port from which data is collected. The NT6X44 time switch transmits PCM tone samples to the parallel speech bus. Timing diagrams of TONECH generation to latch data on port 16 and port 17 appear in figures 3 and 4 on pages 7 and 8.

Input tone sample buffer

The input buffer is an external 8–kbyte by 8–bit random access memory (RAM) that stores tone samples. The input buffer stores tone samples that the parallel speech bus interface for 30 channels latches. Data is stored for channels 0 and 16. These channels are not used for tone reception. Each channel has 192 samples stored in the buffer. The sequencer schedules the input buffer for the write mode. The write mode occurs when tone samples are extracted from a channel on the speech bus. The sequencer schedules the input buffer for the read mode when the correlator receives tone samples.

Correlator

The correlator filters the tone samples from the input buffer for selected frequencies. The correlator multiplies the incoming signal by the sine and cosine components of a known reference frequency. The multiplication process translates the frequencies in the input tone that is close to the reference frequency to the DC range. The frequency–translated incoming signal is low–pass filtered. The result represents the power level of the incoming signal.

Power calculator

The filtered incoming signal transmits to the power calculator to determine the power level of the signal. If the total power over the voice band falls below –28 dBm, the AGC flag is set to amplify power measurements. The AGC flag is set to amplify measurements by 18 dBm.

Sorter

The sorter performs the following functions:

- collects results from the power calculator output
- sorts the results in order of power amplitude
- adjusts the power level values if the AGC flag is set
- passes the results to the local processor

Local processor

The local processor is internal to the ASIC and is based on the 8085 microprocessor. The LP has 1 kbyte static RAM internal to the ASIC. An EPROM external to the ASIC stores the program code for the processor.

The main functions of the local processor are as follows:

- performs messaging with the SP
- analyzes the filter results and identifies tones
- updates the code map RAM on command from the SP
- selects a–law or u–law conversion
- selects the parallel speech bus port number

Signaling processor interface

The signaling processor interface contains a 1 kbyte by 8 bit dual–port RAM internal to the ASIC. The local processor exchanges messages with the SP through the SP interface RAM. If one processor accesses the RAM, the other processor goes on hold. The processor remains on hold until the first processor finishes. This event occurs to avoid bus contention.

Timing and control

The input buffer read address signals S0–S7 and F0–F3 drive the timing and control block. The sample numbers appear as addresses to the timing logic.

The following signals are output:

- FTREND - signals when power result data for each filtering operation is valid
- SUMCLK - latches data from the output of the binary adders
- COSRES - latches the log cosine value
- SINRES - latches the log sine value
- ZERO - clears the sine and cosine accumulator registers
- AGCLT - latches MSB of total power filter results to use as the AGC flag

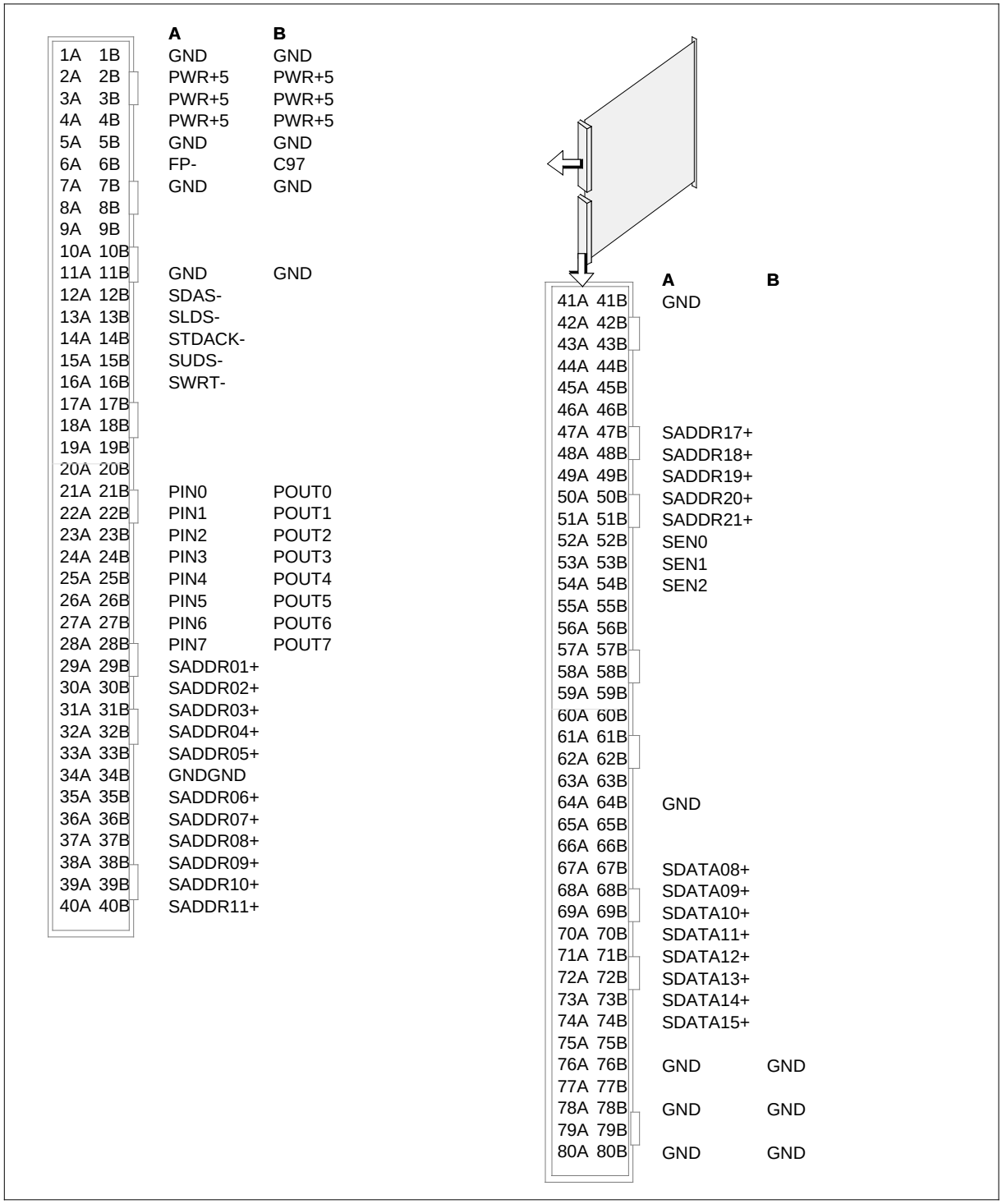
Signaling

Pin numbers

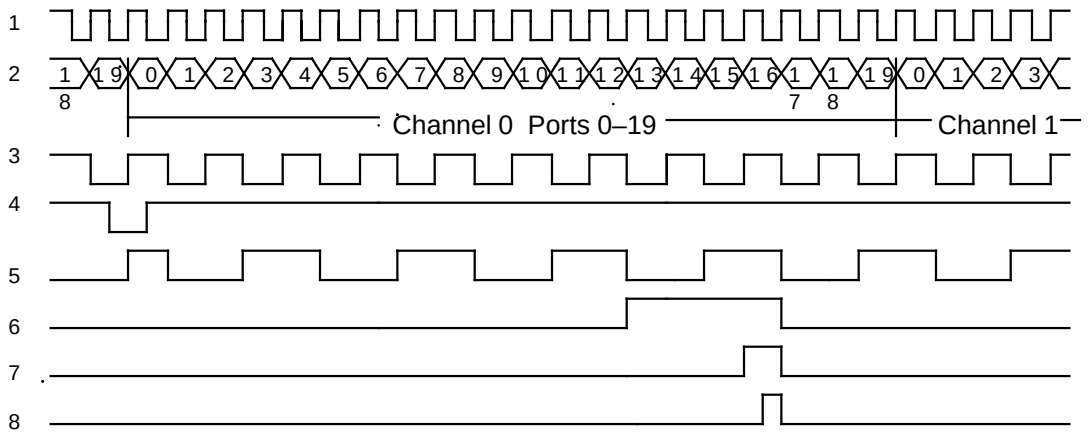
The pin numbers for the NT6X92BC appear in the following figure.

NT6X92BC (continued)

NT6X92BC pin numbers



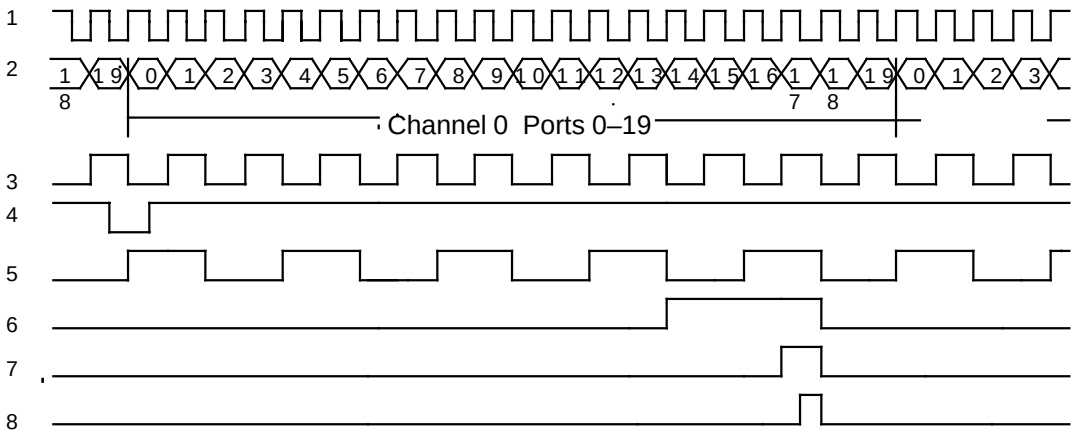
NT6X92BC input buffer clock timing for port 16



Legend
1. C195–
2. Speech bus timing
3. C390+ (internal)
4. FP–
5. P1 (internal)
6. P4 (internal)
7. CNT CARRY (internal)
8. TONECH

NT6X92BC (end)

NT6X92BC input buffer clock timing for port 17



Legend
1. C195-
2. Speech bus timing
3. C390+ (internal)
4. FP-
5. P1 (internal)
6. P4 (internal)
7. CNT CARRY (internal)
8. TONECH

Technical data

Environmental conditions

The universal tone receiver card performs under limited environmental controls. The environmental conditions appear in the following table.

Ambient conditions

Condition	Operating range	Short–term range
Temperature	10°C to 30°C (50°F to 86°F)	5°C to 49°C (41°F to 120.2°F)
Humidity	20% to 55%	20% to 80%

NT6X92CA

Product description

The NT6X92CA is based on the NT6X92AA tone receiver card. The NT6X92CA is introduced for the following reasons:

- to improve dual–tone multifrequency (DTMF) digit reception
- to eliminate digit skew problems in DTMF
- to add a Moroccan variant of the algorithm to detect a 1900–Hz check frequency and the 1700–Hz check frequency
- to alter default parameter tables for minimum power sensitivity to overcome digital filter power level detection offset

The NT6X92CA can detect many tones. These tones include the following:

- the DTMF tone
- the multifrequency (MF) tone
- the common channel interoffice signaling (CCIS) tone

If you program two on–board EPROM, the NT6X92CA can detect a maximum of 128 frequencies. The universal tone receiver (UTR) can handle both A–law and μ–law tones.

Location

One or more UTRs can reside in an international digital trunk controller (IDTC) or in an international line group controller (ILGC).

Functional description

The NT6X92CA is a 30–channel receiver. The facilities processor (FP) switches channel that requires tone detection to a minimum of one DS30A port. The port number depends on which spare slot the UTR occupies. The UTR tests all channels on the port. Channels 0 and 16 are reserved for messaging and cannot be used for tone detection. The NT6X44 time switch switches tone samples to the parallel speech bus (SB). The UTR collects the tone samples at the appropriate time slots. The UTR analyzes the samples and identifies the tones. The results are returned to the signaling processor (SP) through the use of dual–port memory. The samples of each channel are read from the buffer. The samples pass through the correlator ten times for ten filtering operations. The data in the code map RAM determines the type of filter. The power calculator calculates the power level of each filter output. The sorter stores the power level of each filter output. The sorter sorts the power level for each filter and arranges the results in descending order of power for the local processor. The local processor analyzes the filter outputs and

NT6X92CA (continued)

identifies the tones. Communication with the FP is made through dual–port memory on the UTR.

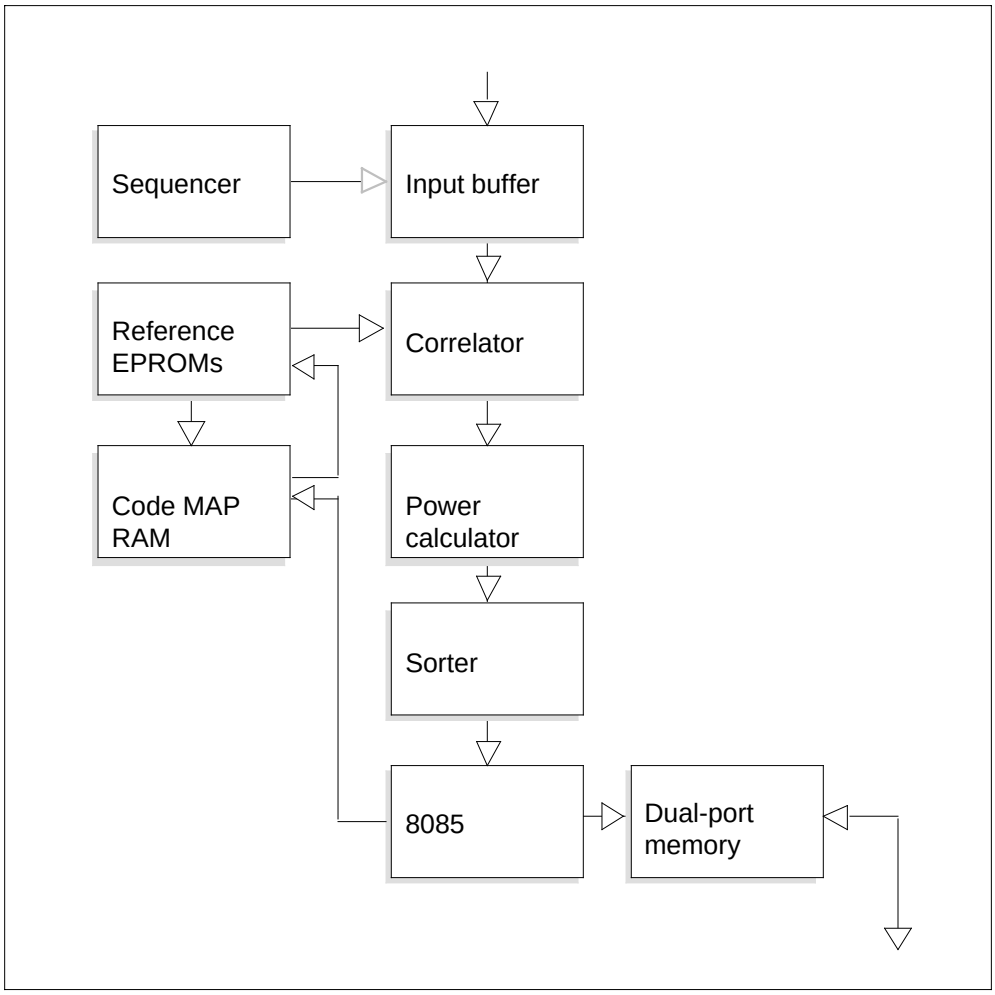
Functional blocks

The NT6X92CA consists of the following functional blocks:

- the parallel SB interface
- the input tone sample buffer
- the correlator
- the power calculator
- the sorter
- the local processor
- the SP interface

The functional relationship between these blocks appears in the following figure.

NT6X92CA functional blocks



Parallel SB interface

Pulse code modulation (PCM) tone samples that must be detected transmit to the parallel SB. The parallel SB bus is the transmit pulse code modulation (XPCM) bus. The time switch in the ILGC and the IDTC transmits the PCM tone samples. Ports 16 and 17 of the SB are reserved for this purpose. The UTR collects data from only one of the two ports. The card must be set for the appropriate port during initialization by the SP. Data is received once every channel time. Channels 0 and 16 of the XPCM bus contain signaling information, and are not used for tone reception.

Input tone sample buffer

The input buffer is organized as a ring buffer. The input buffer collects tone samples for all 30 channels. Channels 0 and 16 are tested for hardware

NT6X92CA (continued)

simplicity. For each channel, 192 samples are stored. All 192 samples are read ten times for the ten filtering operations. A write counter chain and a read counter chain generate the buffer addresses. The read counter chain contains five counters. The least important two counters are the sample number counter, and the filter number counter. The most important two counters are the channel number count.

Of the 192 samples, the least important nibble counts to B (hexadecimal). The next higher nibble counts to F. This allows the buffer address to divide in half by the most important address bit in the sample number counter. The exclusive–or (XOR) logic value adjusts the starting point of each processing window by half the buffer size. The XOR logic value consists of the most significant address line in the sample counter and the most significant bit of the channel counter. The adjustment poses some problems for the write counter chain. The read counter chain reads the input buffer twice before the write counter chain writes once. Normal counters cannot easily achieve the address sequence. An EPROM generates part of the required sequence. The EPROM operates as a state machine, which outputs a sample number according to the previous value. The EPROM stores a reset signal to synchronize the counter chains.

Correlator

The correlator filters tone samples from the input buffer at selected frequencies. The sorter sorts and stores the output of these filters. Each sample filters ten times. The first filter measures the total power of the signal. If total signal power is too low, an automatic gain control (AGC) flag amplifies the signal. A second filter measures speech power. The LP uses the speech power for a talk–off decision. The LP sets the eight filters that remain according to the signaling code used for that channel.

The correlator multiplies the incoming signal by the sine and cosine components of a reference frequency. A low–pass filter filters the outputs. The result represents the power level of the reference frequency present in the incoming signal. The use of PROM implements the multiplication and filtering operations. The multiplier PROMS receive incoming samples and local reference signals. Sign bits are treated separately and determine the sign of the product. The outputs that correspond are accumulated in two 16–bit sine and cosine registers. The AGC is applied here. The AGC flag functions as one of the address lines. There are two multiplier PROMs. The two multiplier PROMs are a μ–law PROM, and an A–law PROM. The processor selects one of these PROMs during initialization. The EPROMs can hold 128 frequencies. A code map RAM selects the 128 frequencies. The local processor updates the code map RAM in response to a command from the SP.

Power calculator

After the completion of each filtering operation, the sine and cosine registers read and pass through the power calculator. The registers read and pass through the power calculator to determine the power level. The power level requires two variables. The two variables are: log sine and log cosine. The two log numbers are latched and presented to an EPROM. The EPROM outputs the corresponding power level for the sorter.

Sorter

The sorter performs the following functions:

- collects results from the power calculator
- sorts the results in order of power amplitude
- adjusts power level values if AGC changed the values earlier
- sends results to the 8085 RAM area through direct memory access

The sorter contains two single–chip processors. These processors have identical firmware, but monitor alternate channels. One processor monitors even channels, the other monitors odd channels. Two channel times are required to process the results from one channel. The first channel time collects the filter results from the power calculator and adjusts power levels if required. The microprocessor uses the next channel time to sort the filters with the three highest power levels.

Local processor

The local processor performs the following functions:

- exchanges messages with the SP
- analyzes filter results and identifies tones
- updates the code map RAM
- selects A–law or μ–law PROMs
- selects the parallel SB port number

A power–up reset or a reset from the SP causes the processor to enter diagnostic mode. In this mode, the 8085 executes codes from EPROM. The diagnostic program scans the common RAM continuously for SP commands. The SP chooses one of the internal diagnostic routines by an issue of the appropriate code. At the termination of diagnostic mode, normal operating codes are copied to static RAM from EPROM. Codes copied to static RAM allows the 8085 to execute codes at full clock rate without wait states. The processor analyzes the sorted results according to a specified set of parameters. Tones or errors report to the SP through dual–port RAM.

NT6X92CA (end)

Signaling processor interface

The 8085 exchanges messages with the SP through the use of dual–port RAM. Ring type buffers controlled by pointers transfer the messages. If one processor has access to the memory, the other processor is put on hold to avoid contention. Both processors access the memory at full speed.

The UTR can be used in spare slots. The starting address for common memory depends on the slot that in use. The SP can reset the UTR by writing to locations in the base UTR.

NT6X92EA

Product description

The NT6X92EA global tone receiver (GTR) circuit pack identifies and processes pulse code modulation (PCM) tones from 32 voice channels on a parallel speech bus (SB). The SB is on the common peripheral module extended multiprocessor system (XMS)-based peripheral module (XPM).

The GTR is LATA Switching System Generic Requirements/International Telegraph and Telephone Consultative Committee (LSSGR/CCITT) compliant. All national and international applications where the NT6X92BB, NT6X92BC, and NT6X92CA are provisionable can use the GTR.

The GTR can detect tones from A-law or μ-law compressed PCM samples. The GTR can detect a maximum of 128 different tones.

Note: A signaling set contains a set of tones from the 0 Hz to 4000 Hz frequency range.

The GTR firmware now supports the following national and international signaling sets:

- dual-tone multifrequency (DTMF)
- multifrequency (MF)
- compelled multifrequency (CMF) forward
- compelled multifrequency (CMF) backward
- MF Socotel
- MF Socotel for Morocco
- special information tone (SIT) (not supported: code reserved for backward compatibility only)
- common channel interoffice signaling (CCIS) (not supported: code reserved for backward compatibility only)

Location

The GTR resides in the common peripheral shelf of the DMS-100. One or two GTRs can reside in each XPM unit.

The GTR uses slots 15, 16 or 17 of the common peripheral controller (CPC) shelf, that includes but is not limited to the following:

- the line group controller (LGC)
- the line trunk controller (LTC)

NT6X92EA (continued)

- the digital trunk controller (DTC)
- the remote cluster controller (RCC)
- integrated services digital network (ISDN) variants of the XPMs
  - — the LGCI
  - — the LTCI
  - — the remote switching center (RSCI)
- the international line group controller (ILGC)
- the international digital trunk controller (IDTC)

Functional description

The GTR detects tones that a subscriber telephone keypad or a central office sends. The GTR identifies and processes PCM tones from 32 voice channels on the parallel SB of the common peripheral module. The XPM, is a peripheral module of the DMS-100 digital switching system. The XPM can be from a group of XPM systems.

The GTR detects the occurrence of a valid set of tones in the PCM stream on a channel. The GTR decodes the tones in to the information that the tones represent. This information can be digits 1 through 9, 0, * and £ on a telephone keypad or a call progress tone sequence from a far end central office. When all digits are entered on a specified call, the GTR is removed from the voice path and prepared for another call. The GTR connects to the voice path when digits or signaling information is required. When a call is in the talking state, or when a telephone handset is on-hook, the GTR does not connect to that line.

The signaling processor (SP) switches any channel that requires tone detection to one of two DS-30A ports. The GTR stores tone samples from 32 channels on a port. National applications reserve channels 0 and 16 for messaging. A configurable set of parameters uses a digital signal processor (DSP) to process and analyze samples from each channel . The DSP reports valid digits and errors to the SP through a shared port memory.

The only function the dedicated hardware performs is to fetch PCM samples from the backplane PCM bus to the on-board buffers. Firmware executed by the local processor/digital signal processor (LP/DSP) on the GTR performs every other function. These other functions are as follows:

- filtering functions
- SP/LP communications

- DSP filtering
- digit detection

Functional blocks

NT6X92EA has the following functional blocks:

- the parallel SB interface
- the input tone sample buffer
- the flash firmware memory
- the main memory
- the DSP
- the SP interface
- the board timing and control glue logic

Parallel SB interface

The GTR hardware can be used in the spare slots in the LTC. The NT6X44 time switch in the LTC/DTC detects and transmits the PCM tone samples on the parallel SB. The parallel SB is the transmit pulse code modulation (XPCM) bus. The time switch performs this action under XPM software control. Ports 16 and 17 of the SB are currently reserved for this purpose. The GTR can collect data from two to four ports (ports 16/17 or ports 18/19). The GTR can collect data because of an anticipated China market requirement is present for more than 64 channels of tone reception for each XPM. To support more than 64 channels on an XPM, at least one GTR must be present and assigned to port 18/19. The other two cards are universal tone receiver (UTR) or GTR, and must be assigned to port 16 and 17. The GTR must be set to listen to the appropriate port during initialization by the SP. The GTR can detect digits on all 32 PCM channels at the same time.

Input tone sample buffer

Each port contains two PCM buffers. The two PCM buffers are 16 kbytes x 8 bytes. Only 9 kbytes x 8 bytes of this random access memory (RAM) are used. The two PCM buffers store PCM samples latched by the parallel SB interface for all 32 channels of each port. The buffers store 288 samples for each channel. The UTR design stored 192 PCM samples in a ring buffer to minimize RAM size. The RAM size is minimized because the reads and writes to the PCM buffers are in synchronization in the UTR. Discrete hardware performed the filtering. The GTR design stores 288 PCM samples to simplify the GTR processor addressing to the PCM samples.

The DSP reads 192 samples from the PCM buffer once for each channel processing time. The DSP uses the samples to perform the filtering and tone

NT6X92EA (continued)

detection for that channel. The 192 samples the processor for each channel received, accurately represent 24 ms of real time data (192 samples × 125 ms/sample). The 24 ms of data are processed on each of 32 channels in each 12-ms processing window. The following sentences account for 24 ms of data processed each 12 ms. The starting point for each processing window to read out the data for each channel must shift by 96 samples. This shift causes the data filtered during the current processing window to overlap the data processed during the previous processing window by 12 ms.

The GTR reads the samples for all 32 channels in a sequence. In order to maintain real time controls, the data in the PCM buffer for 32 channels process each 12 ms. The data in the PCM buffer is processed approximately 374.4 ms for each channel.

The real time control is derived when data for each channel is available on the XPM bus at each channel time.

A channel time consists of 3.9 ms. Note that the GTR captures data for both ports at each channel time. The GTR must process 192 samples for each of the 32 channels before the write circuit writes 96 samples to all 32 channels. If the GTR does not process 192 samples, the GTR misses data on the channel. The time allotted to each channel for processing digit information is as follows:

- 3.9 ms/sample-channel*32 channel*96 samples = 11.9808 ms and 11.9808 ms/32=˜374.4 ms

Flash firmware memory

The GTR contains one boot file. Earlier versions of the GTR contained several separate firmware streams. This boot file is stored in nonvolatile flash memory. The flash memory is one 128 kbytes × 8 bytes flash memory part.

The boot file contains the following:

- the A-law and μ-law expansion tables
- the reference frequency sine
- the cosine filter coefficients needed to perform the tone detection
- default signaling set parameters,
- digit tables and digit detection algorithms for the signaling sets

On power up or after a reset, the DSP reads the headers in the boot file in flash. The DSP translates the information in the boot file into the main memory as firmware.

This boot file can be downloaded from the SP through the SP/DSP dual port memory. The firmware download is available while the GTR is in the test loop entered after a power-up or reset. The correct software features must be present in the XPM to download new firmware to the GTR.

Main memory

The main memory contains 32 kbytes x 8 bytes fast static random access memory (SRAM) configured to act as a 32 kbytes x 32 bytes memory block. On power-up or after a reset, the firmware is copied in to this memory and the DSP performs the program completely from this memory. The main memory is accessible at three times rate of the flash to allow for fast program and data fetches. The main memory contains the following:

- program
- signaling set default parameters
- digit tables for all signaling sets
- different run-time call processing tables

The reference frequency filter coefficients are stored in the main memory.

DSP

The core of the GTR board is the TMS320C32, referred to as the LP DSP. The LP is a 50 MHz 32-bit floating point processor. The LP can perform single cycle, half the clock rate or 40 ns, multiply-accumulate instructions, parallel arithmetic-load/store instructions, and is designed for DSP applications. The main functions that the LP performs are as follows:

- performs boot load from flash main memory
- filters incoming PCM samples for signaling set reference frequencies
- analyzes the filter results for digits
- communicates with the SP
- maintains all processing tables, including updates from the SP
- selects A-law or μ-law conversion
- selects parallel SB ports

The LP performs the boot load of the boot file from the flash memory to the main memory. The bootload occurs during power up or after a board reset. The LP enters a diagnostic loop and performs out-of-service maintenance routines. The LP downloads firmware when the SP commands the download. The diagnostic program scans the SP/LP dual port memory continuously for SP

NT6X92EA (continued)

commands. The SP can choose one of the internal diagnostic routines by an issue of the appropriate code.

When the LP exits the test loop, the LP initializes and looks for a port (port 16/17 or 18/19). The initialized LP looks for a port to which the LP can listen. The LP determines when to decode A-law or μ-law PCM samples on the assigned port. After the LP receives this information, the LP starts to filter the channels for tones. The GTR uses the same correlation technique as the UTR to perform the tone filters. The GTR performs the tone filters with a modification to improve real time performance of the processor.

The GTR performs total power filters while the UTR sums the input PCM to estimate total power in the signal. Three band pass filters on the GTR, two for DTMF, and one for other signaling sets are present. The filters have a bandstop below the 500 Hz range to remove dial tone, power line noise and low frequency noise. The DTMF band-pass filters filter the row band and column band frequency power in the input signal. The row band frequencies range from 697 Hz to 941 Hz. The column band frequencies range from 1209 Hz to 1633 Hz. The band pass filter for all other signaling sets is a high pass filter.

Band pass filtering uses a large amount of real time. Analysis and optimization aided the creation of the final minimum tap band pass filters for the GTR. These filters are approximately 40 taps in length but with a radical twist. The band pass filtering runs on decimated input data to reduce the number of multiply-accumulates to approximate the power across 12-ms. The input PCM is decimated from 8 kHz sampled data to 4 kHz sampled data. This decimation reduces the number of samples required for a 12 ms window from 96 to 48 samples. This decimation is performed on data sampled at 8 kHz that was not band limited to 2 kHz before decimation. The result is that aliasing occurs on the 0 to 2 kHz band from the 2 kHz to 4 kHz band. Signaling sets defined in the standards up to this point are band limited below 4 kHz so the aliasing is not an issue. The highest signaling frequency is accurately 1900 Hz in MF Socotel. The aliasing is an advantage in DTMF talkoff rejection because speech and other noise (nonsignaling spectral energy) contains parts in the upper band. This energy becomes aliased into the row and column band pass filters. This energy helps in the rejection of false digits simulated by speech and other noise.

The LP first fetches 192 samples to perform the filtering operations on a channel. The LP fetches 192 samples from the PCM buffers into a RAM block on board the processor. The LP expands the μ-law/A-law 8-bit samples to linear values. After the LP expands the PCM data, the input data is decimated for band pass filtering. The LP perform the appropriate DTMF band pass filtering, or the high pass filtering for the other signaling sets.

The LP folds the data for tone filtering. The LP performs a total of eight tone filtering operations for each channel. The local processor selects these tones according to the defined frequencies for the signaling set used for that channel.

Each tone/reference frequency from a signaling set like MF or DTMF, associates with a filter number. The band pass filters also have respective filter numbers assigned. The LP receives a command from the SP to monitor a channel for a specified signaling set. The associated filter numbers for that signaling set are used to perform the filtering for that channel. The filter numbers are offsets to the coefficient table in the GTR firmware.

When the nine (10 in DTMF) filtering operations are complete, the eight tone filters that result are sorted to find the three highest power values. The eight tone filters make the reference frequencies for that signaling set. The current channel filter result table stores the three top reference frequencies and the band pass power results. The information in this table is used to detect digits in the input PCM stream for that channel. If a digit is detected and meets LSSGR/CCITT criteria, the digit is reported to the SP. The digit is reported to the SP through the SP/LP dual port memory.

This filtering process runs on all channels of every processing window of 12 ms. The GTR control register is an 8 bit word. This register controls A-law or μ-law selection and parallel speech bus port selection.

SP interface

The SP/LP interface is a 2-kbit x 8 dual port RAM. The LP exchanges messages with the SP by way of this RAM. The RAM is different from the UTR. This memory is true dual port with the least possible contention. Contention occurs only when the SP and the LP try to access the same memory location in the dual port RAM. If this condition occurs and the LP is first to the RAM, the LP gains access to the RAM. The LP can finish with enough time to allow the SP to gain access. If the SP is first, the SP gains access. The LP must wait until the SP is complete before the LP can access the RAM.

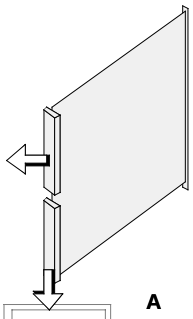
Signaling

Pin numbers

The pin numbers for NT6X92EA appear in the following figure.

NT6X92EA (continued)

NT6X92EA pin numbers



	A	B
1A 1B	GND	GND
2A 2B	PWR+5	PWR+5
3A 3B	PWR+5	PWR+5
4A 4B	PWR+5	PWR+5
5A 5B	GND	GND
6A 6B	FP-	C97+
7A 7B	GND	GND
8A 8B		
9A 9B		
10A 10B		
11A 11B	GND	GND
12A 12B	SDAS-	
13A 13B	SLDS-	
14A 14B	STDACK-	
15A 15B	SUDS-	
16A 16B	SWRT-	
17A 17B		
18A 18B		
19A 19B		
20A 20B		
21A 21B	PIN0	POUT0
22A 22B	PIN1	POUT1
23A 23B	PIN2	POUT2
24A 24B	PIN3	POUT3
25A 25B	PIN4	POUT4
26A 26B	PIN5	POUT5
27A 27B	PIN6	POUT6
28A 28B	PIN7	POUT7
29A 29B	SADDR01+	
30A 30B	SADDR02+	
31A 31B	SADDR03+	
32A 32B	SADDR04+	
33A 33B	SADDR05+	
34A 34B	GND	GND
35A 35B	SADDR06+	
36A 36B	SADDR07+	
37A 37B	SADDR08+	
38A 38B	SADDR09+	
39A 39B	SADDR10+	
40A 40B	SADDR11+	

	A	B
41A 41B	GND	
42A 42B		
43A 43B		
44A 44B		
45A 45B		
46A 46B		
47A 47B	SADDR17+	
48A 48B	SADDR18+	ADM17+
49A 49B	SADDR19+	ADM18+
50A 50B	SADDR20+	ADM19+
51A 51B	SADDR21+	
52A 52B	SEN0	
53A 53B	SEN1	
54A 54B	SEN2	
55A 55B		
56A 56B		
57A 57B		
58A 58B		
59A 59B		
60A 60B		
61A 61B		
62A 62B		
63A 63B		
64A 64B	GND	
65A 65B		
66A 66B		
67A 67B	SDATA08+	
68A 68B	SDATA09+	
69A 69B	SDATA10+	
70A 70B	SDATA11+	
71A 71B	SDATA12+	
72A 72B	SDATA13+	
73A 73B	SDATA14+	
74A 74B	SDATA15+	
75A 75B		
76A 76B	GND	GND
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

Technical data

Environmental conditions

The GTR card performs under limited environmental controls. The controls appear in the following table.

Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 °C to 30 °C (50 °F to 86 °F)	5 °C to 49 °C (41 °F to 120.2 °F)
Humidity	20% to 55%	20% to 80%

Power requirements

The GTR normal current use for the GTR is 1.2A.

NT6X93AA

Product description

The NT6X93AA meets impedance and loss plan requirements. This card provides a voice and signaling interface. This interface is between a two-wire analog subscriber line and one channel of the four-wire 32-channel 2.56-Mbps bit stream. The bit stream is from the DMS-100 Family of switches.

The NT6X93AA is a subscriber line interface that provides a plain ordinary telephone service (POTS) telephone interface. The card is for use with the following sets:

- sets compatible with an input impedance of 600 ohms in series with 2.16 μF
- sets compatible with a balance impedance of 600 ohms in parallel with the series group of 100 ohms and 50 nF

The NT6X93AA accepts both dual-tone multifrequency (DTMF) and dial pulse signaling.

The NT6X93AA has the following features:

- synthesized input and balance impedance
- software-programmable receive path loss
- loop range of 2 kohms (loop plus set)

Location

The NT6X93AA can occupy any line card slot in the following:

- line concentrating module
- enhanced line concentrating module
- small remote unit

Functional description

The NT6X93AA provides a voice and signaling interface. This interface is between a two-wire analog subscriber line and one channel of the four-wire 32-channel 2.56-Mbps bit stream of the DMS-100 Family of switches. The card provides for both analog and digital looparound for diagnostic purposes. The system provides access to the subscriber loop with or without the line card circuits connected for loop and line card testing. Software-controlled cutover is also provided.

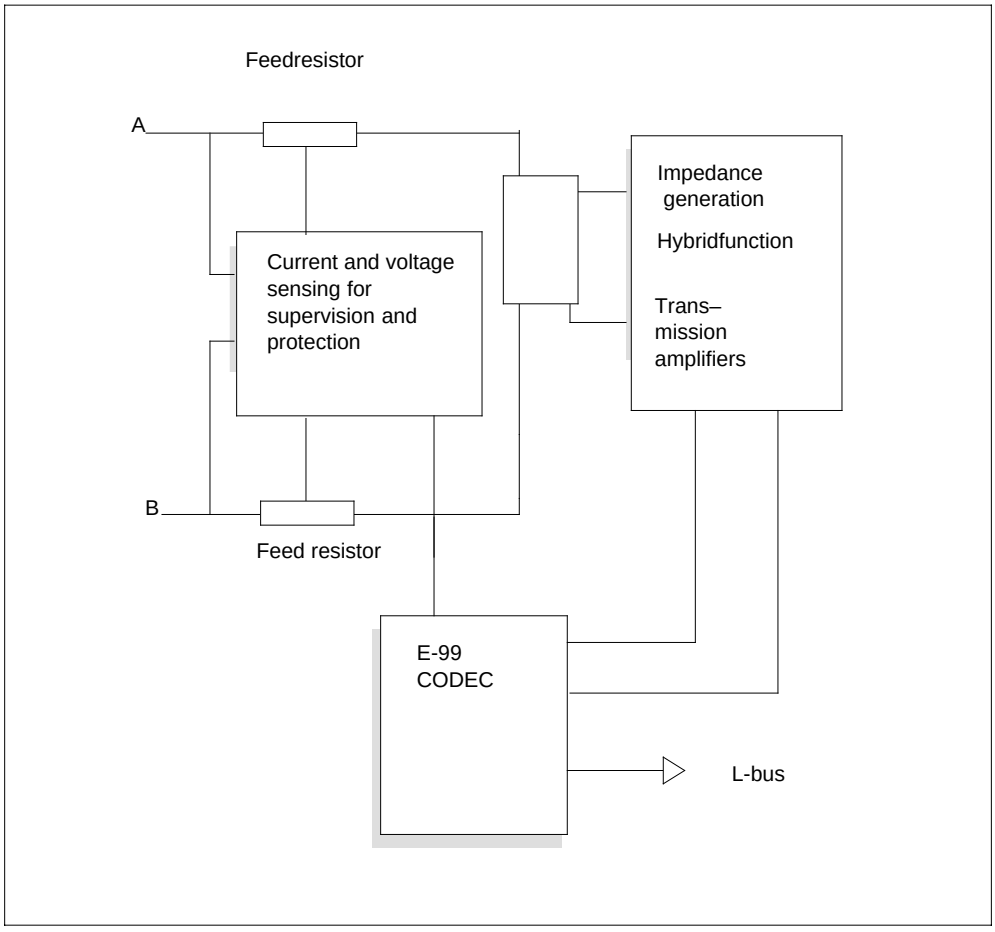
Current and voltage sensing for detecting on-hook or off-hook, ring trip, and flux balance is done on the primary side of the transformer. Transmission functions are in circuits on the secondary side of the transformer.

The speech path through the NT6X93AA goes from the A and B leads to the primary winding of the transformer. From the secondary winding of the transformer, the speech signal passes through an amplifier or filter stage. The speech signal enters the E-99 filter coder-decoder (CODEC) where the signal is encoded into pulse code modulation (PCM) before going on to the L-bus.

For a signal traveling in the analog-to-digital direction, the order is reversed. The E-99 filter CODEC receives PCM data from the L-bus and converts the data into an analog signal. The E-99 filter then applies the analog signal to the digital-to-analog amplifier or filter. Output from this amplifier is applied to the transformer, which drives the signal differentially onto the A and B leads.

The major functions of the NT6X93AA appear in the following figure.

NT6X93AA functional blocks



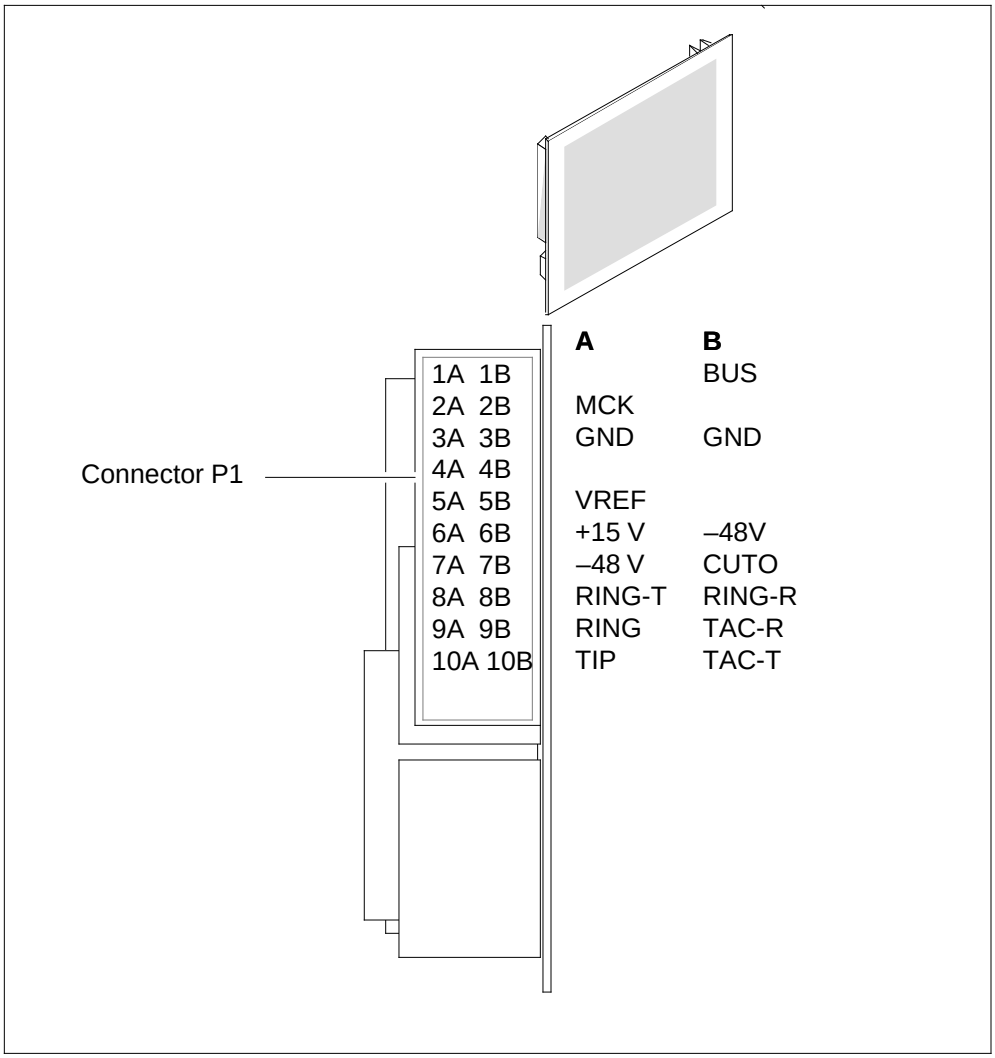
NT6X93AA (continued)

Signaling

Pin numbers

The pin numbers for the NT6X93AA appear in the following table.

NT6X93AA pin numbers



Technical data

Power requirements

The power requirements for the NT6X93AA appear in the following table.

Power requirements

Current draw	**+ 15 V**	**Current draw**	**– 52 V**	**Power dissipation**	
Idle	Active	Idle	Active	Idle	Active
16 mA	30 mA	0.4 mA	0.4 mA +1.2 –I-loop (See note)	0.264 W	2.68 W
Note: I-loop is assumed to be 60 mA					

NT6X93BA

Product description

The NT6X93BA was developed to meet impedance and loss plan requirements. This card provides a voice and signaling interface. This interface is between a two-wire analog subscriber line and one channel of the four-wire 32-channel 2.56-Mbps bit stream of the DMS-100 Family of switches.

The NT6X93BA is a subscriber line interface that provides a plain ordinary telephone service (POTS) telephone interface. The card is for use with the following sets that are compatible with:

- an input impedance of 300 ohms in series with the parallel group of 1000 ohms and 220 nF
- a balance impedance of 370 ohms in series with the parallel group of 620 ohms and 310 nF

The NT6X93BA accepts both dual-tone multifrequency (DTMF) and dial pulse signaling. The transmit path has a loss of 4 dB.

The NT6X93BA has the following features:

- synthesized input and balance impedance
- software-programmable receive path loss
- a loop range of 2 kohms (loop plus set)

Location

The NT6X93BA can occupy any line card slot in the following:

- line concentrating module
- enhanced line concentrating module
- small remote unit

Functional description

The NT6X93BA provides for both analog and digital looparound for diagnostic purposes. Access to the subscriber loop is provided with or without the line card circuits connected for loop and line card testing. Software-controlled cutover is also provided.

Current and voltage sensing for detecting on-hook or off-hook, ring trip, and flux balance is performed on the primary side of the transformer. Transmission functions are implemented in circuits on the secondary side of the transformer.

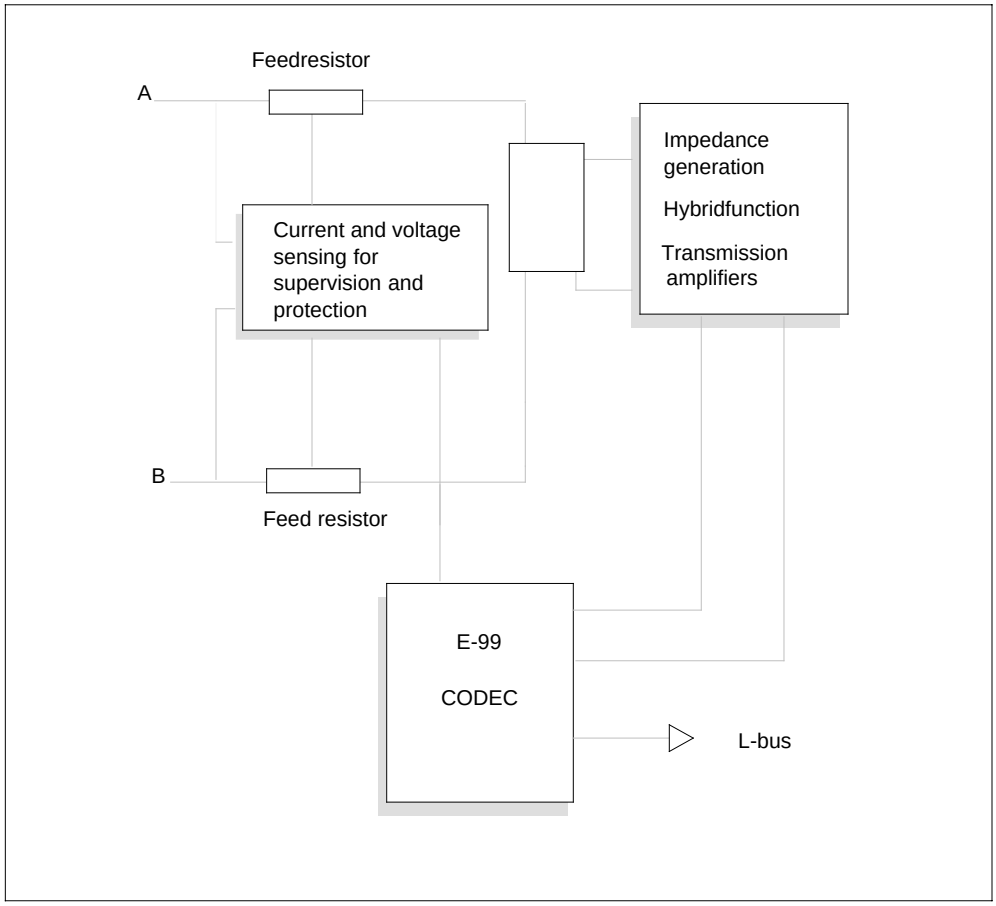
The speech path through the NT6X93BA goes from the A and B leads to the primary winding of the transformer. From the secondary winding of the

transformer, the speech signal passes through an amplifier or filter stage. The speech signal enters the E-99 filter coder-decoder (CODEC) where the system encodes the signal into pulse code modulation (PCM) before going on to the L-bus.

For a signal that travels in the analog-to-digital direction, the order is reversed. The E-99 filter CODEC receives PCM data from the L-bus and converts the data into an analog signal. The E-99 filter applies the analog signal to the digital-to-analog amplifier or filter. Output from this amplifier applies to the transformer, which drives the signal differentially on to the A and B leads.

The major functions of the NT6X93BA appear in the following figure.

NT6X93BA functional blocks



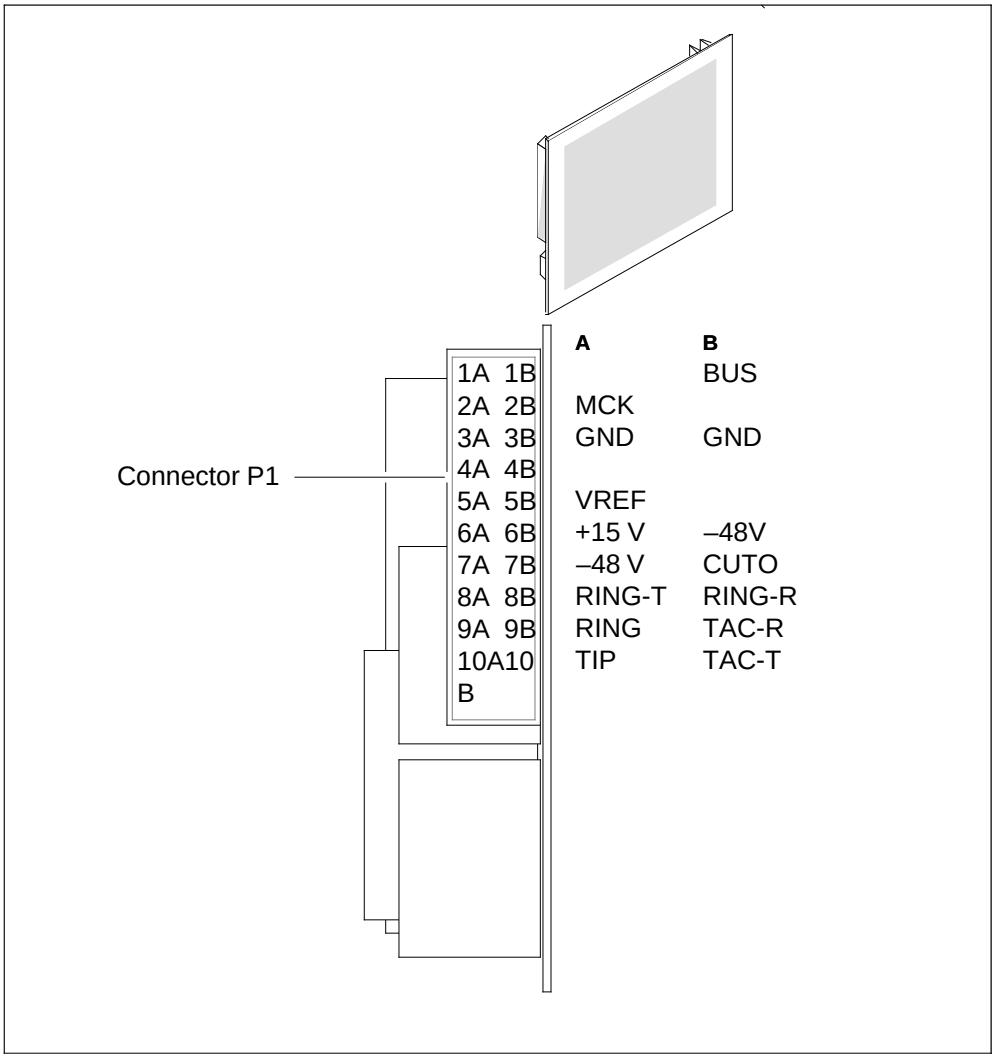
Signaling

Pin numbers

The pin numbers for the NT6X93BA appear in the following figure.

NT6X93BA (continued)

NT6X93BA pin numbers



Technical data

Power requirements

The power requirements for the NT6X93BA appear in the following table.

Power requirements

Current draw	+15 V	Current draw	–52 V	Power Dissipation	
Idle	Active	Idle	Active	Idle	Active
16 mA	30 mA	0.4 mA	0.4 mA +1.2 – I-loop (See note)	0.264 W	2.68 W
Note: I-loop is assumed to be 60 mA					

NT6X93CA

Product description

The NT6X93CA meets impedance and loss plan requirements. This card provides a voice and signaling interface. The interface occurs between a two-wire analog subscriber line and one channel of the four-wire 32-channel 2.56-Mbps bit stream. The bit stream is part of the DMS-100 Family of switches.

The NT6X93CA is a subscriber line interface that provides a plain ordinary telephone service (POTS) telephone interface. This card is for use with sets compatible with the following:

- an input impedance of 200 ohms in series with the parallel combination of 680 ohms and 100 mF
- a balance impedance of 160 ohms in series with a parallel combination of 780 ohms and 115 nF

The NT6X93CA accepts dual-tone multifrequency (DTMF) and dial pulse signaling.

The NT6X93CA has the following features:

- synthesized input and balance impedance
- software-programmable receive path loss
- loop range of 2 kohms (loop plus set)

Location

The NT6X93CA can occupy any line card slot in the line concentrating module (LCM), the enhanced LCM, or the small remote unit.

Functional description

The NT6X93CA allows analog and digital looparound for diagnostic purposes. The NT6X93CA provides access to the subscriber loop with or without the line card circuits that connect for loop and line card tests. The NT6X93CA also provides software-controlled cutover.

The primary side of the transformer senses current and voltage to detect on-hook or off-hook, ring trip and flux balance. Circuits on the secondary side of the transformer implement transmission functions.

The speech path through the NT6X93CA routes from the A and B leads to the primary winding of the transformer. From the secondary winding of the transformer, the speech signal passes through an amplifier or filter stage. After the amplifier or filter stage, the signal enters the E-99 filter coder-decoder

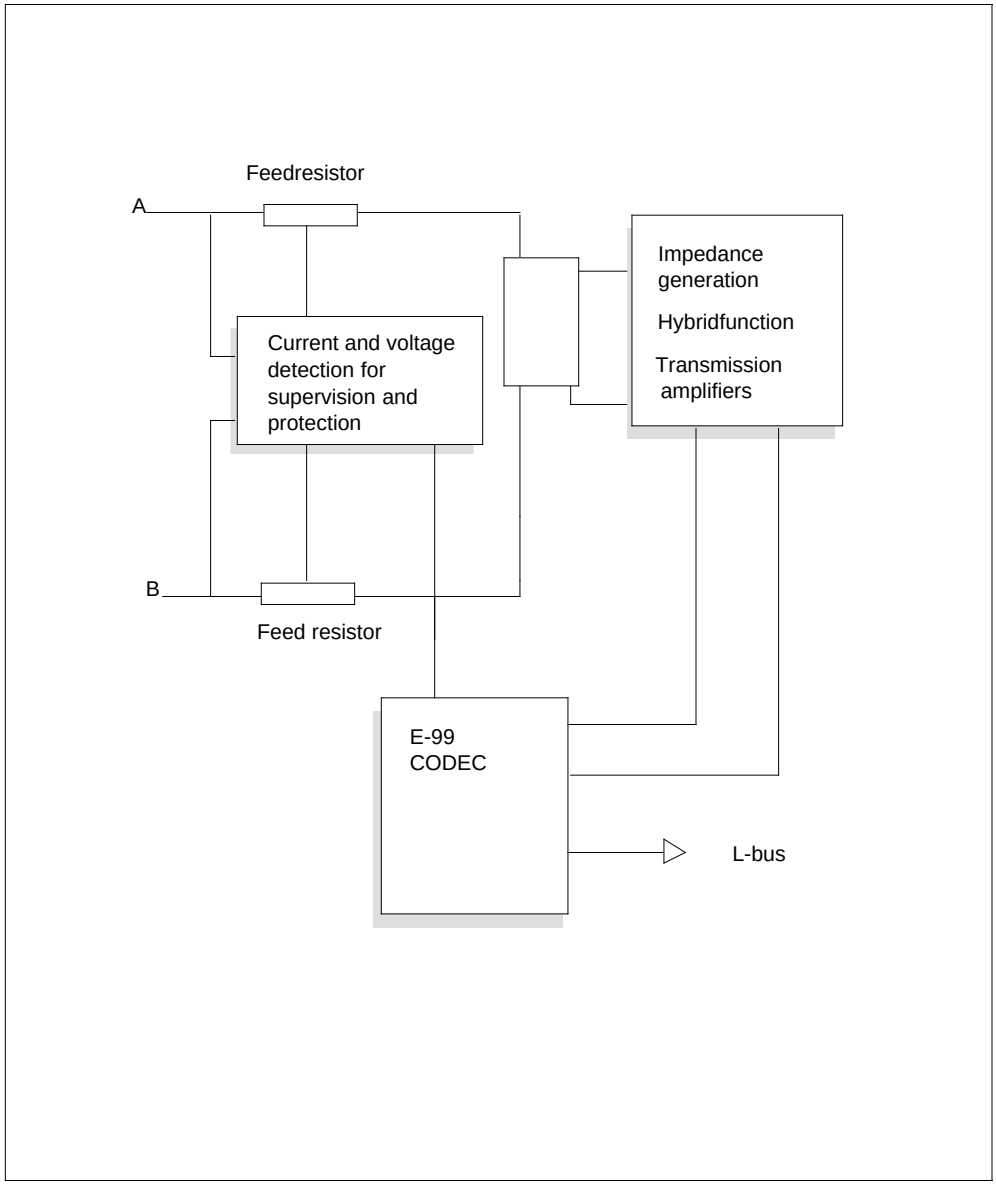
(CODEC). The CODEC codes the signal in pulse code modulation (PCM). After this event occurs, the signal goes on to the L-bus.

For a signal that travels from analog to digital, the order is reversed. The E-99 filter CODEC receives PCM data from the L-bus. The CODEC converts the data to an analog signal. The CODEC applies the signal to the digital-to-analog amplifier or filter. Output from this amplifier routes to the transformer. The transformer drives the signal differentially to the A and B leads.

The main functions of the NT6X93CA appear in the following diagram.

NT6X93CA (continued)

NT6X93CA functional blocks

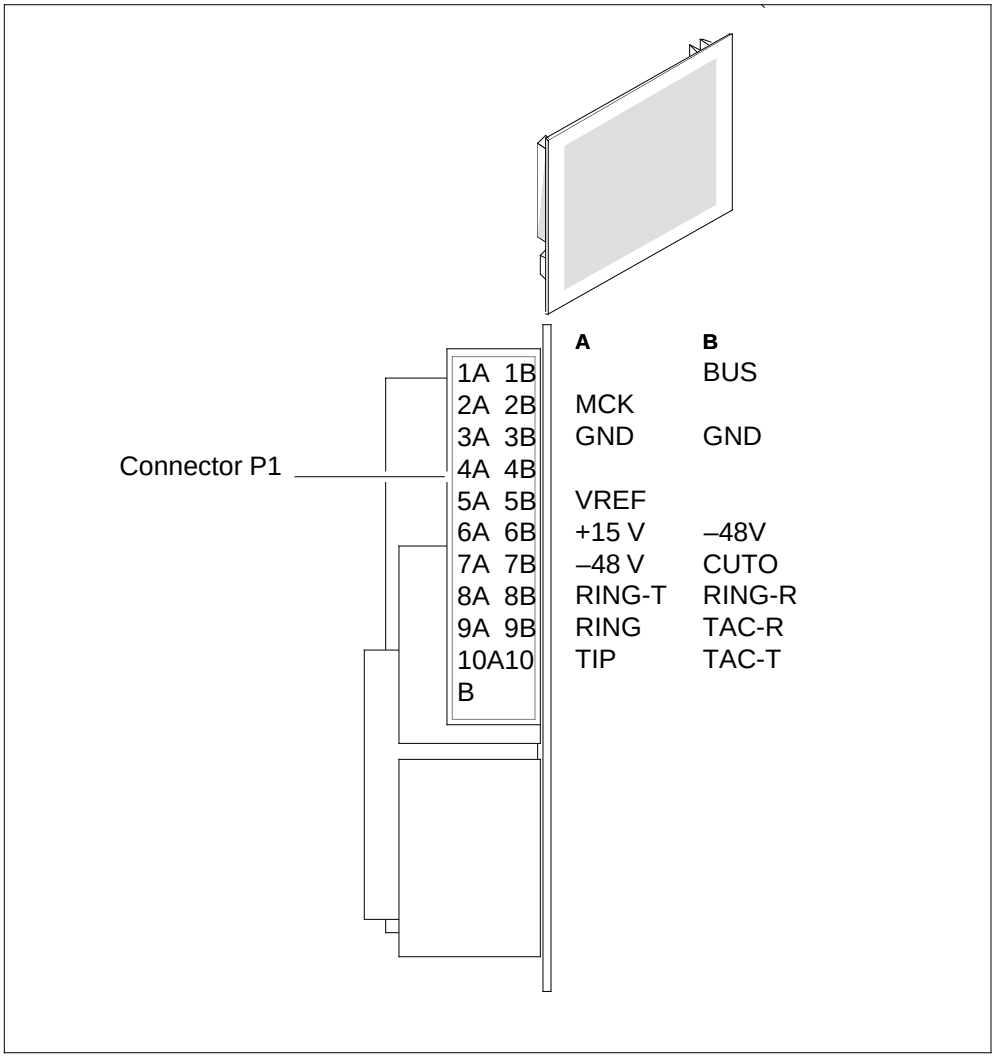


Signaling

Pin numbers

The pin numbers for the NT6X93CA appear in the following diagram.

NT6X93CA pin numbers



NT6X93CA (end)

Technical data

Power requirements

The power requirements for the NT6X93CA appear in the following table.

Power requirements

Current draw	**+ 15 V**	**Current draw**	**– 52 V**	**Power distribution**	
Idle	Active	Idle	Active	Idle	Active
16 mA	30 mA	0.4 mA	0.4 mA +1.2 ×I-loop (Refer to note)	0.264 W	2.68 W
Note: Assume the I-loop is 60 mA					

NT6X93DA

Product description

The NT6X93DA meets impedance and loss plan requirements. This card provides a voice and signaling interface between a two-wire analog subscriber line and one channel of the four-wire 32-channel 2.56-Mbps bit stream. This bit stream is part of the DMS-100 Family of switches

The NT6X93DA is a subscriber line interface that provides a plain ordinary telephone service (POTS) telephone interface. The card is for use with sets compatible with the following:

- an input impedance of 600 ohms in series with 216 nF
- a balance impedance of 210 ohms in series with the parallel combination of 880 ohms and 150 nF

The NT6X93DA accepts dual-tone multifrequency (DTMF) and dial pulse signaling.

The NT6X93DA has the following features:

- synthesized input and balance impedance
- software-programmable receive path loss
- loop range of 2 kohms (loop plus set)

Location

The NT6X93DA can occupy any line card slot in the line concentrating module (LCM), the enhanced LCM, or the small remote unit.

Functional description

The NT6X93DA allows analog and digital looparound for diagnostic purposes. The NT6X93DA provides access to the subscriber loop with or without the line card circuits that connect for loop and line card tests. The NT6X93DA also provides software-controlled cutover.

The primary side of the transformer senses current and voltage to detect on-hook or off-hook, ring trip and flux balance. Circuits in the secondary side of the transformer implements transmission functions.

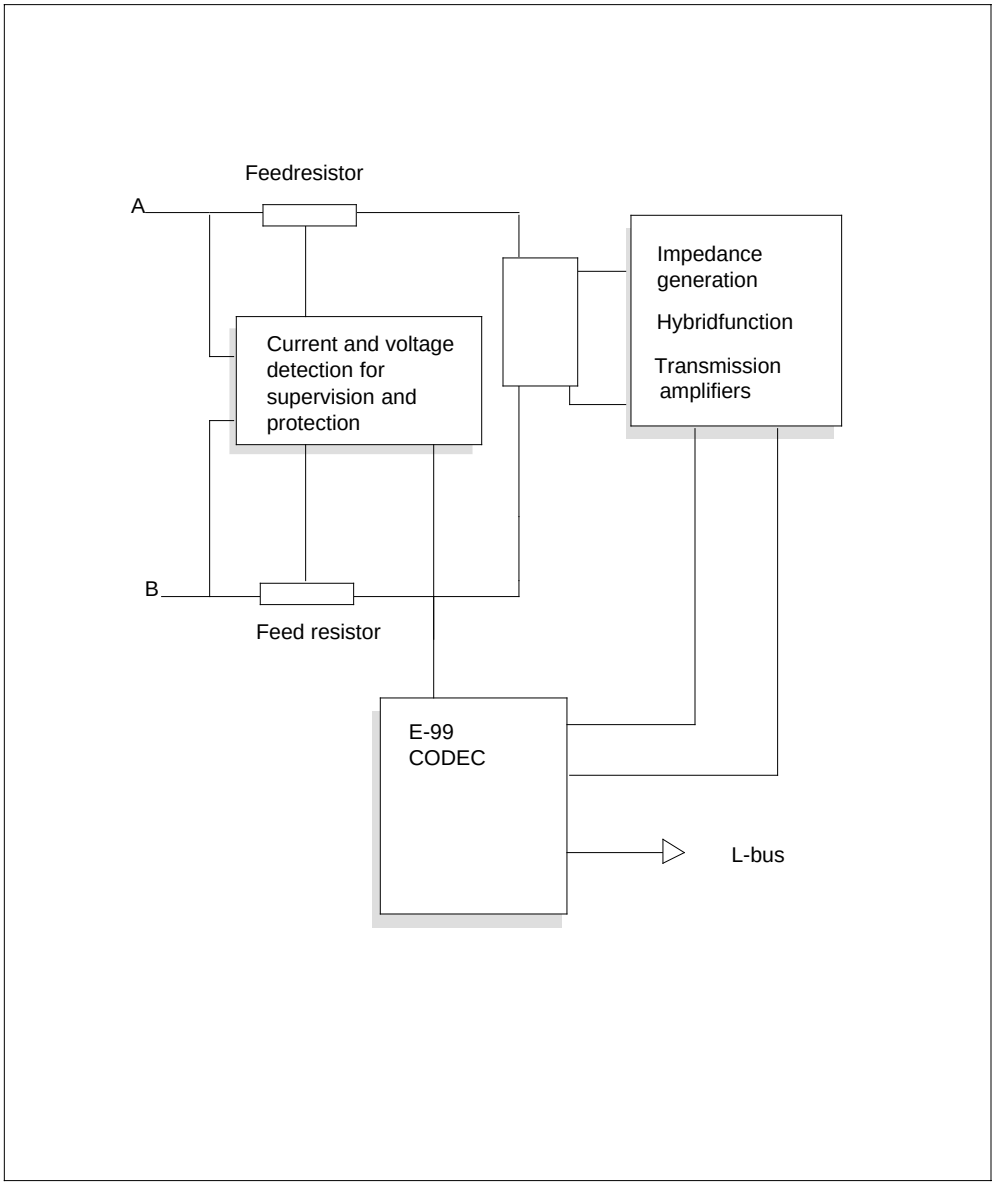
The speech path through the NT6X93DA routes from the A and B leads to the primary winding of the transformer. From the secondary winding of the transformer, the speech signal passes through an amplifier or filter stage. After the amplifier or filter stage, the signal enters the E-99 filter coder-decoder (CODEC). The CODEC codes the signal in pulse code modulation (PCM). After this event occurs, the signal goes on to the L-bus.

NT6X93DA (continued)

For a signal that travels from analog to digital, the order is reversed. The E-99 filter CODEC receives PCM data from the L-bus. The CODEC converts the data to an analog signal. The CODEC applies the signal to the digital-to-analog amplifier or filter. Output from this amplifier routes to the transformer. The transformer drives the signal differentially to the A and B leads.

The main functions of the NT6X93DA appear in the following diagram.

The NT6X93DA functional blocks

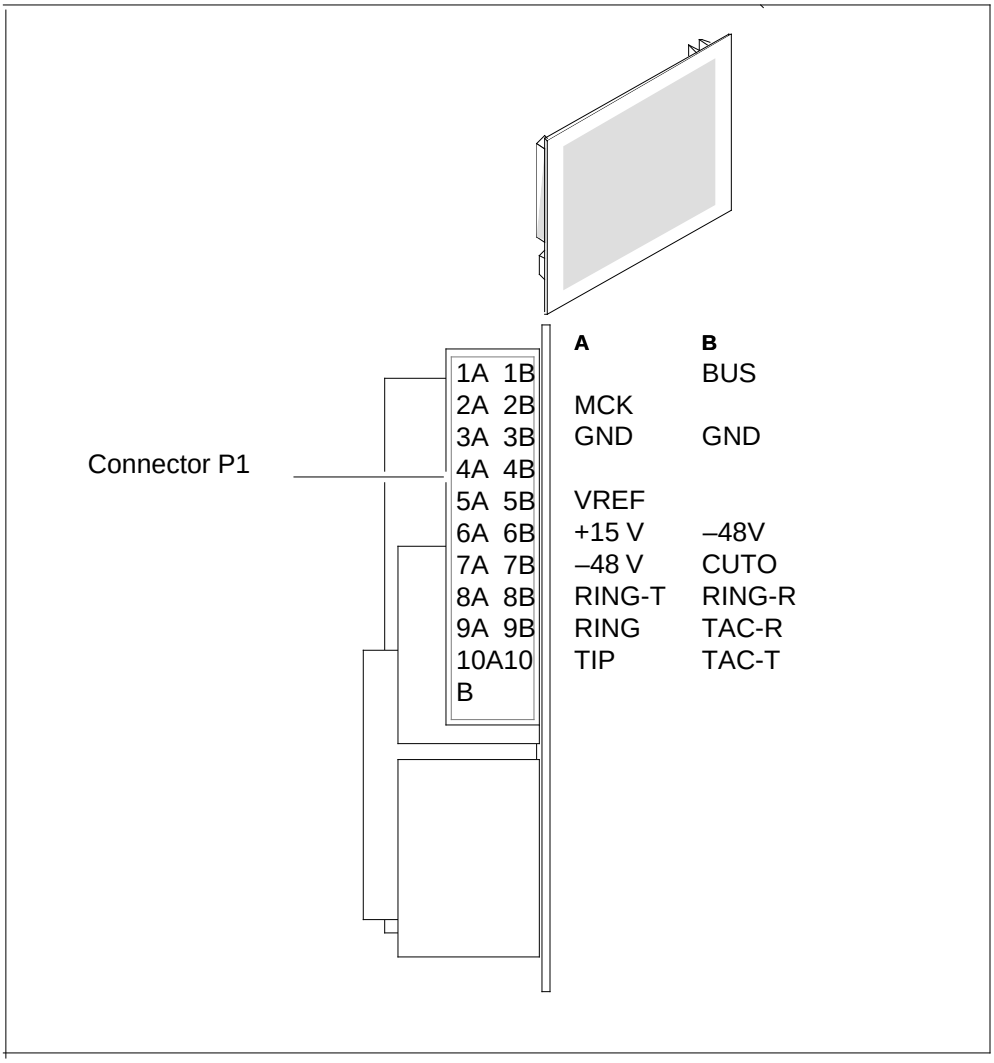


Signaling

Pin numbers

The pin numbers for the NT6X93DA appear in the following diagram.

The NT6X93DA pin numbers



NT6X93DA (end)

Technical data

Power requirements

The power requirements for the NT6X93DA appear in the following table.

Power requirements

Current draw	**+ 15 V**	**Current draw**	**– 52 V**	**Power distribution**	
Idle	Active	Idle	Active	Idle	Active
16 mA	30 mA	0.4 mA	0.4 mA +1.2 × I-loop (Refer to note)	0.264 W	2.68 W
Note: Assume the I-loop is 60 mA					

NT6X93EA

Product description

The NT6X93EA design is for the Australian intelligent network. The NT6X93EA meets impedance and loss plan requirements. This card provides a voice and signaling interface between a two-wire analog subscriber line and one channel of the four-wire 32-channel 2.56-Mbps bit stream. The bit stream is part of the DMS-100 Family of switches

The NT6X93EA is a subscriber line interface that provides a plain ordinary telephone service (POTS) telephone interface. The card is for use with sets compatible with an input and balance impedance of 220 ohms. The impedance must be in series with the parallel combination of 820 ohms and 120 nF. The NT6X93EA accepts dual-tone multifrequency (DTMF) and dial pulse (DP) signaling.

The NT6X93EA has the following features:

- synthesized input and balance impedance
- software-programmable receive path loss
- a loop range of 3.5 kohms (loop plus set)

Location

The NT6X93EA can occupy any line card slot in the line concentrating module (LCM), the enhanced LCM, or the small remote unit.

Functional description

The NT6X93EA card allows analog and digital looparound for diagnostic purposes. The card provides access to the subscriber loop with or without the line card circuits that connect for loop and line card tests. The card also provides software-controlled cutover.

The primary side of the transformer senses current and voltage to detect on-hook or off-hook, ring trip and flux balance. Circuits on the secondary side of the transformer implement transmission functions.

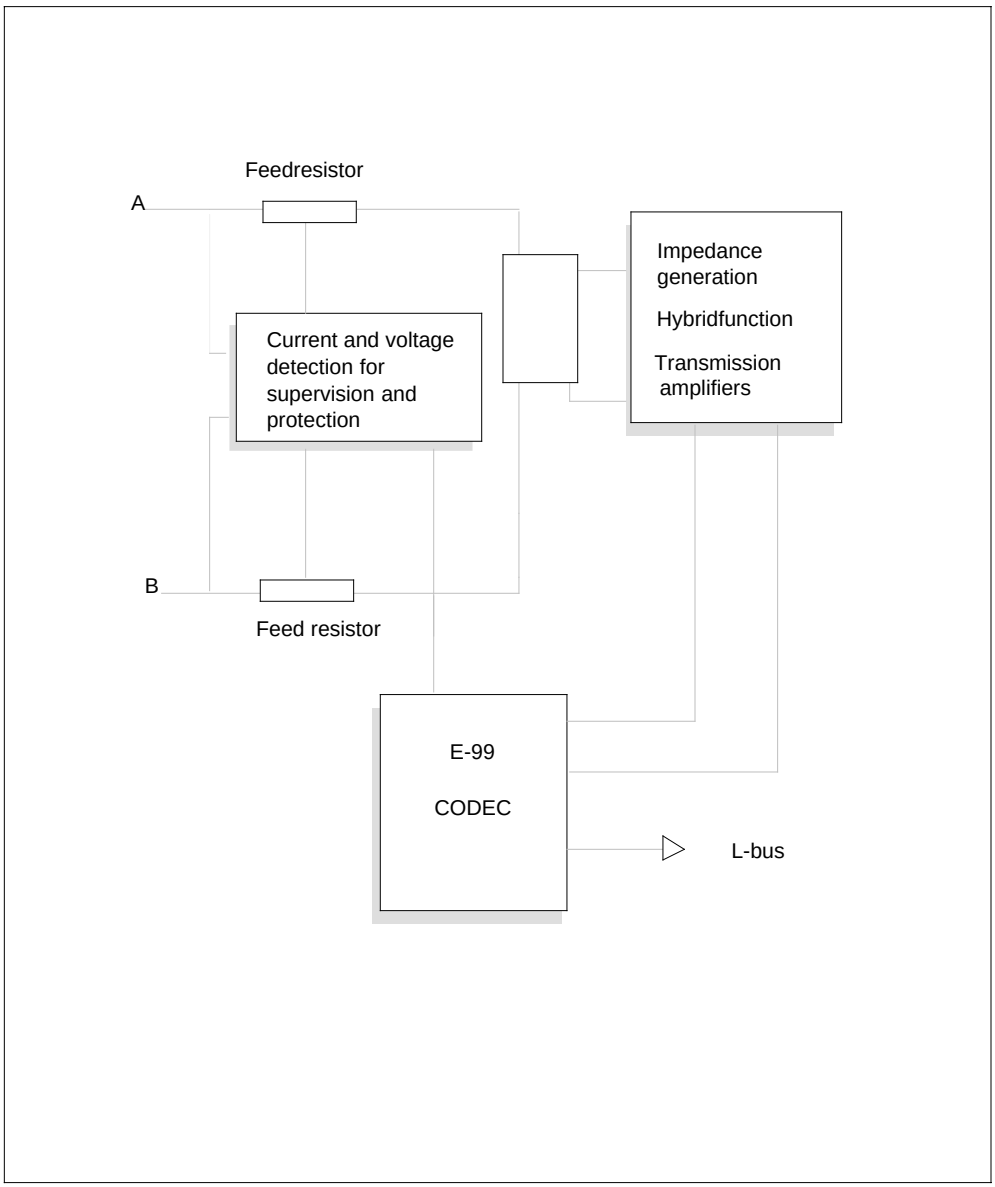
The speech path through the routes from the A and B leads. From the leads, the path routes through the feed resistors to the primary winding of the transformer. From the secondary winding of the transformer, the speech signal passes through an amplifier or filter stage. After the amplifier or filter stage, the signal enters the E-99 filter coder-decoder (CODEC). The CODEC codes the signal in pulse code modulation (PCM). After this event occurs, the signal goes on to the L-bus.

NT6X93EA (continued)

For a signal that travels from analog to digital, the order is reversed. The E-99 filter CODEC receives PCM data from the L-bus. The CODEC converts the data to an analog signal. The CODEC applies the signal to the digital-to-analog amplifier or filter. Output from this amplifier routes to the transformer. The transformer drives the signal differentially to the A and B leads.

The main functions of the NT6X93EA appear in the following diagram.

The NT6X93EA functional blocks

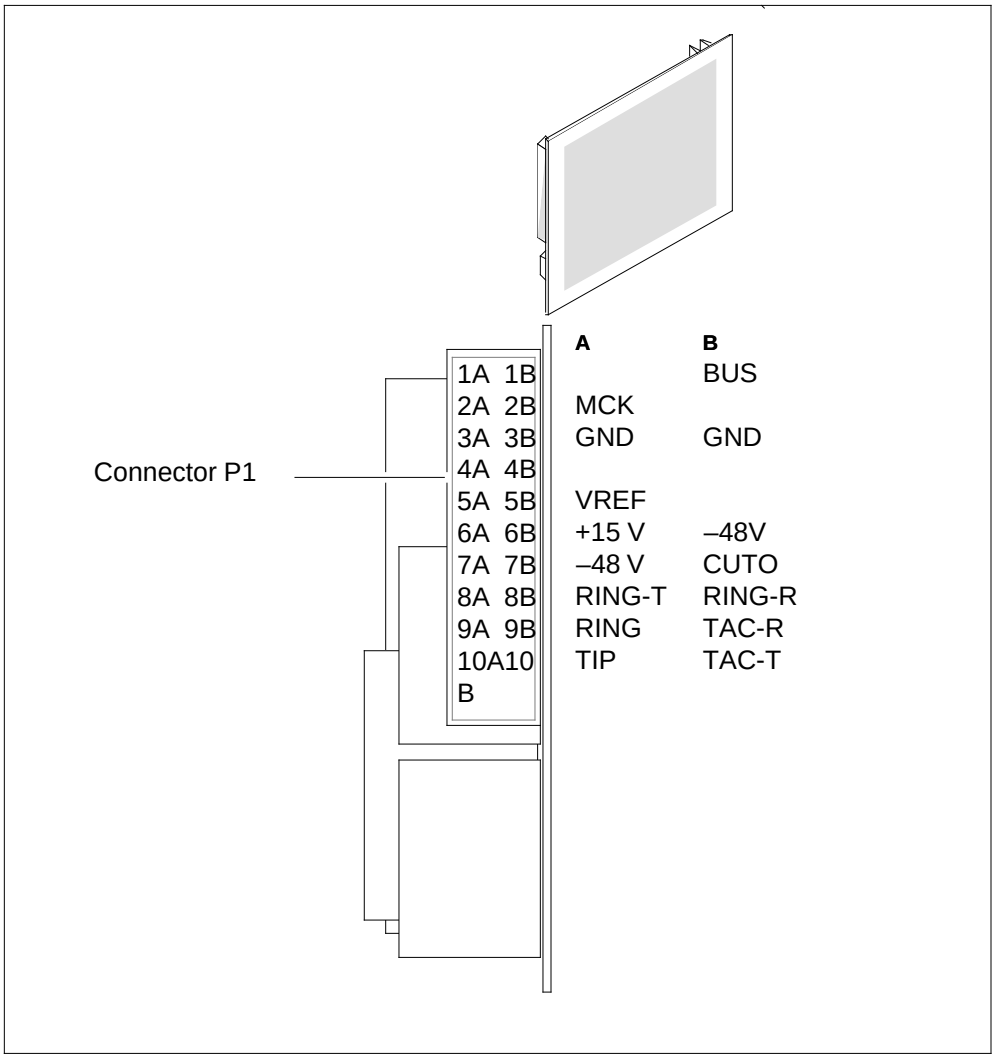


Signaling

Pin numbers

The pin numbers for the NT6X93EA appear in the following diagram.

The NT6X93EA pin numbers



NT6X93EA (end)

Technical data

Power requirements

The following table shows the power requirements for the NT6X93EA.

Power requirements

Current draw	**+ 15 V**	**Current draw**	**– 52 V**	**Power distribution**	
Idle	Active	Idle	Active	Idle	Active
16 mA	30 mA	0.4 mA	0.4 mA + 1.2 ×I-loop (Refer to note)	0.264 W	2.68 W
Note: Assume the I-loop is 60 mA.					

NT6X93FA

Product description

The extended range line card (ERLC) provides a voice and signaling interface. This interface occurs between a two-wire loop connected to the terminal equipment of a subscriber and one of the four-wire channels on the 32-channel speech bus. The 32-channel speech bus is part of the DMS-100.

The NT6X93FA is for applications where low subscriber concentration requires a longer loop length than the standard length.

Location

Each NT6X93FA occupies three slots next to each other in the international line drawer. Four slots are available in one vertical line.

Functional description

The NT6X93FA uses a dc-to-dc converter to increase the signaling range of the two-wire loop. The dc-to-dc converter increases the battery voltage from -48V to 86V when a subscriber goes offhook. The gain and equalization circuit increases the transmission range of the two-wire loop. The NT6X93FA handles analog and digital looparound for diagnostics purposes. This card provides cutover control, loop and card tests.

Functional blocks

The NT6X93FA has the following functional blocks:

- supervisory block
- transmission circuits
- coder/decoder (CODEC)
- voltage regulators
- relays

Supervisory block

The supervisory block performs the following functions:

- on/off hook detection
- flux balance
- ringing supervision

The supervisory block can detect on/off hook during ringing or silent intervals. The lead, A or B, on which the ringing is applied does not affect detection.

NT6X93FA (continued)

The flux balance function generates a flux balance current in the hybrid transformer. The flux balance current flows in the opposite direction to the loop current. This process cancels all flux that the talk battery creates.

The CODEC that detects the operation of the ringing relay and reports to the central processor (CP) provides ringing supervision.

Transmission circuits

The NT6X92FA has three transmission circuits, as follows:

- a circuit to meet the China input impedance three-element network
- a precision balance network circuit to achieve the required balance impedance for the transformer hybrid
- a gain and equalization circuit that increases the transmission range of the two-wire loop

The CODEC

The CODEC uses the bidirectional PCM bus to provide a link between software control and line card functions. The CODEC also provides pulse code modulation (PCM) links to other devices.

Voltage regulators

Three onboard voltage regulators (one +12V, and two +7.5V) reduce noise and crosstalk in the transmission circuits.

Relays

The CODEC activates a cutover relay and conserves power when an office is commissioned.

A test access relay provides access to the customer loop and the line card output during diagnostic tests.

When in operation, the ringing relay allows the application of ringing voltage to the loop.

Technical data

Power requirements

NT6X93FA Power requirements

Supply voltage	Supply current (Offhook)	Supply current (Onhook)
+ 12.7 V	50 µA	50 µA
+ 15.0 V	23.8 mA	35.7 mA
- 51.0 V	1.9 mA	91.0 mA

NT6X95AB

Product description

The NT6X95AB metering tone converter 12-kHz and 16-kHz card generates a sinusoidal tone. The sinusoidal tone is for the NT6X94AA international line card (LC) with metering use.

Location

The card occupies one position in an international line concentrating module (ILCM) line drawer (LD).

Functional description

The NT6X95AB performs the following functions:

- generates transistor-transistor logic (TTL) compatible square waves
- filters the square waves to produce tones
- adjusts the tones for transmission to the LD

The card contains monitors to indicate the presence of a tone and to make sure that the tone conforms to specifications.

Functional blocks

The NT6X95AB has the following functional blocks:

- line circuit chip
- crystal oscillator
- two square wave dividers
- two bandpass filters
- automatic gain control (AGC) circuit
- level adjustment circuit
- output buffer
- output monitor

Line circuit chip

The line circuit chip controls the transfer of data. The line circuit chip receives 10 bits of control data from the LD to control the transfer of data. The line circuit chip sends 10 bits of signaling data to the LD to control the transfer of data. The line circuit chip uses a bidirectional bus to send the signaling data to the LD.

The chip uses a 2.56-MHz TTL clock signal to control the timing of data transfers. The signaling data that the chips send indicates the following:

- tone presence
- correct function of the monitor circuit
- correct position of the LC in the LD

Crystal oscillator

The crystal oscillator generates a 1.53-MHz square wave. The square wave dividers divide the wave and the bandpass filters filter the wave. This event occurs to produce the tone.

Square wave dividers

The two square wave dividers receive the TTL-compatible square wave from the crystal oscillator. The two square wave dividers divide the tone. After this event occurs, the square wave dividers transmit the tone to the bandpass filters.

Bandpass filters

The two bandpass filters receive the divided square wave from the two square wave dividers. The bandpass filters filter the tone to produce a 12-kHz or a 16-kHz sine wave.

AGC circuit

The AGC circuit makes sure that a constant supply of output level is available to the LD. The circuit compares the filtered tone to a +12V reference voltage. The circuit amplifies a low input signal or attenuates a high input signal to provide a constant output level.

Level adjustment circuit

The level adjustment circuit adjusts the peak-to-peak level of the output tone.

Output buffer

The output buffer provides protection against short duration exposure to potentials that are not normal and output short circuits.

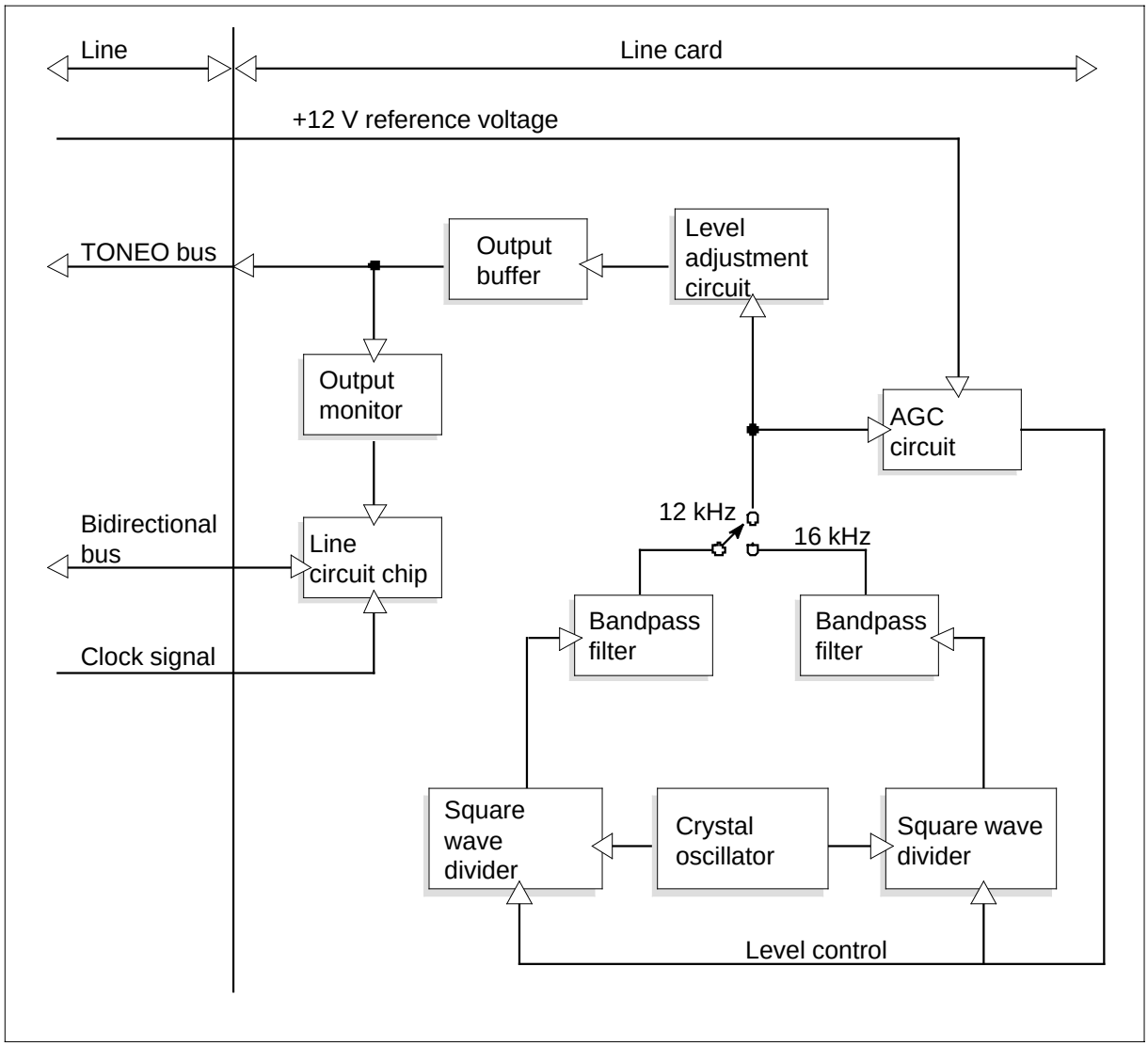
Output monitor

The output monitor receives a sample of the output signal. The output monitor rectifies and filters the signal to produce an equivalent dc voltage. The monitor notifies the system when the output voltage is not compatible with correct levels.

The relationship between the functional blocks appears in the following figure.

NT6X95AB (continued)

NT6X95AB functional blocks



Technical data

The signal specifications for the NT6X95AB appear in the following table.

Signal Specifications (Sheet 1 of 2)

Characteristic	Value
Output frequency	12.0 kHz or 16.0 kHz ±0.5%
Output dc offset	7.5 V dc ±0.5 V dc

Signal Specifications (Sheet 2 of 2)

Characteristic	Value
Total harmonic distortion	0.5%
Output level range	0 to 2.0 V peak to peak
Output monitor range	1.0 V ±0.2 V peak to peak
Output level stability	0.5%

Dimensions

The dimensions for the NT6X95AB follow:

- height: 76 mm (3.0 in.)
- width: 89 mm (3.5 in.)

Power requirements

The card consumes 120 mW of power. The card uses a +12.7V ±1% current as a reference current to convert a +15V ±0.5V current.

NT6X99AA

Product description

The NT6X99AA Datapath bit error rate tester (BERT) line card (2-slot) allows the system to generate bit error rate tests. The NT6X99AA allows the application of bit error rate tests to a Datapath data transmission link.

Location

The card plugs in to two adjacent line circuit card positions in the line drawer (LD) of a line concentrating module (LCM).

Functional description

The NT6X99AA receives control communications from the LCM. The NT6X99AA transmits BERT patterns to the LCM. The card checks the BERT patterns for errors and stores test results for use by the LCM. An activation signal allows the card to select an intelligent or a nonintelligent message format.

Functional blocks

The NT6X99AA has the following functional blocks:

- LCM interface
- power converter
- microreset circuit
- microprocessor
- 16-MHz crystal
- RAM circuit
- EPROM circuit

LCM interface

The LCM interface uses a 16-bit, parallel bidirectional bus to transmit and receive control data and performance statistics. The transmission and receipt of control data and performance statistics occurs between the LCM and the microprocessor. The circuit exchanges data about the transmission and reception of CCITT 511 BERT patterns with the microprocessor.

The interface uses a 1-kHz master frame pulse and a 2.56-MHz clock signal to synchronize card functions. The interface uses an activation signal to select intelligent or nonintelligent message formats.

When data transfers from the card to the LCM, the LCM interface contains registers that are *write-only* to the microprocessor. The LCM interface contains registers that are *read-only* from the bidirectional bus. When data transfers

from the LCM to the card, registers are *read-only* from the microprocessor. Registers are *write-only* to the bidirectional bus.

Power converter

The power converter receives a +15V power supply from the LD and converts the current to a regulated, filtered power supply. The power supply is for critical circuits in the card. The converter removes low and high frequency noise and tempers momentary changes in the supply current.

Microreset circuit

The microreset circuit resets the card with the use of one of two inputs. The two inputs are a +5V power supply output from the power converter or a microprocessor reset signal that the LCM sends.

When the +5V power supply rises during a power-up, the microreset circuit sends a reset signal to the LCM interface. The circuit sends a reset signal to the microprocessor when the LCM transmits a reset command through the LCM interface.

Microprocessor

The microprocessor communicates with the LCM interface to transmit and receive the following information:

- reset signals
- data rate mode settings
- starting or stopping of BERT patterns
- bulk rate transfers

The microprocessor uses 16-bit address buses to access the RAM and EPROM.

16-MHz crystal

The 16-MHz crystal generates an internal microprocessor clock signal to control the microprocessor instructions.

RAM circuit

The RAM circuit includes 8 Kbytes of memory. The 8 Kbytes or memory contain test results and data for microprocessor use.

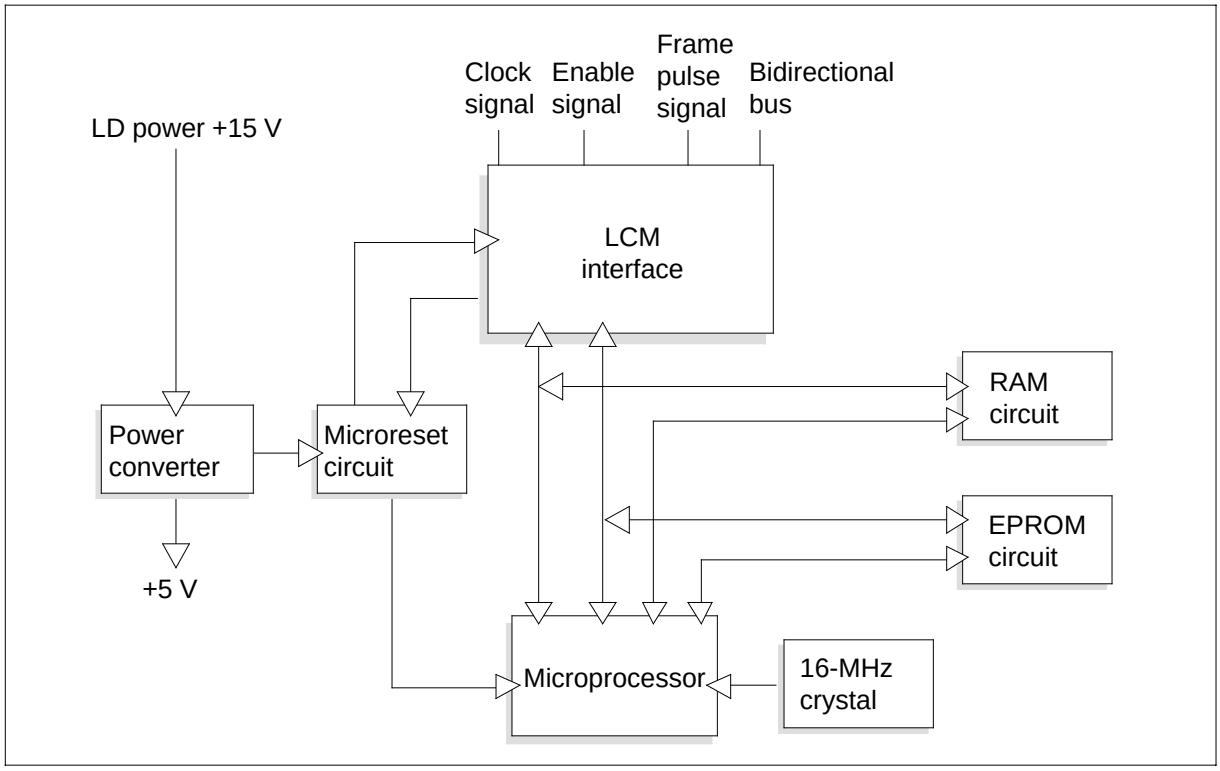
EPROM circuit

The EPROM circuit includes two 8-Kbyte blocks of memory. The memory blocks contain the 511-bit BERT pattern and program data for microprocessor use.

NT6X99AA (continued)

The relationship between the functional blocks appears in the following figure.

NT6X99AA functional blocks



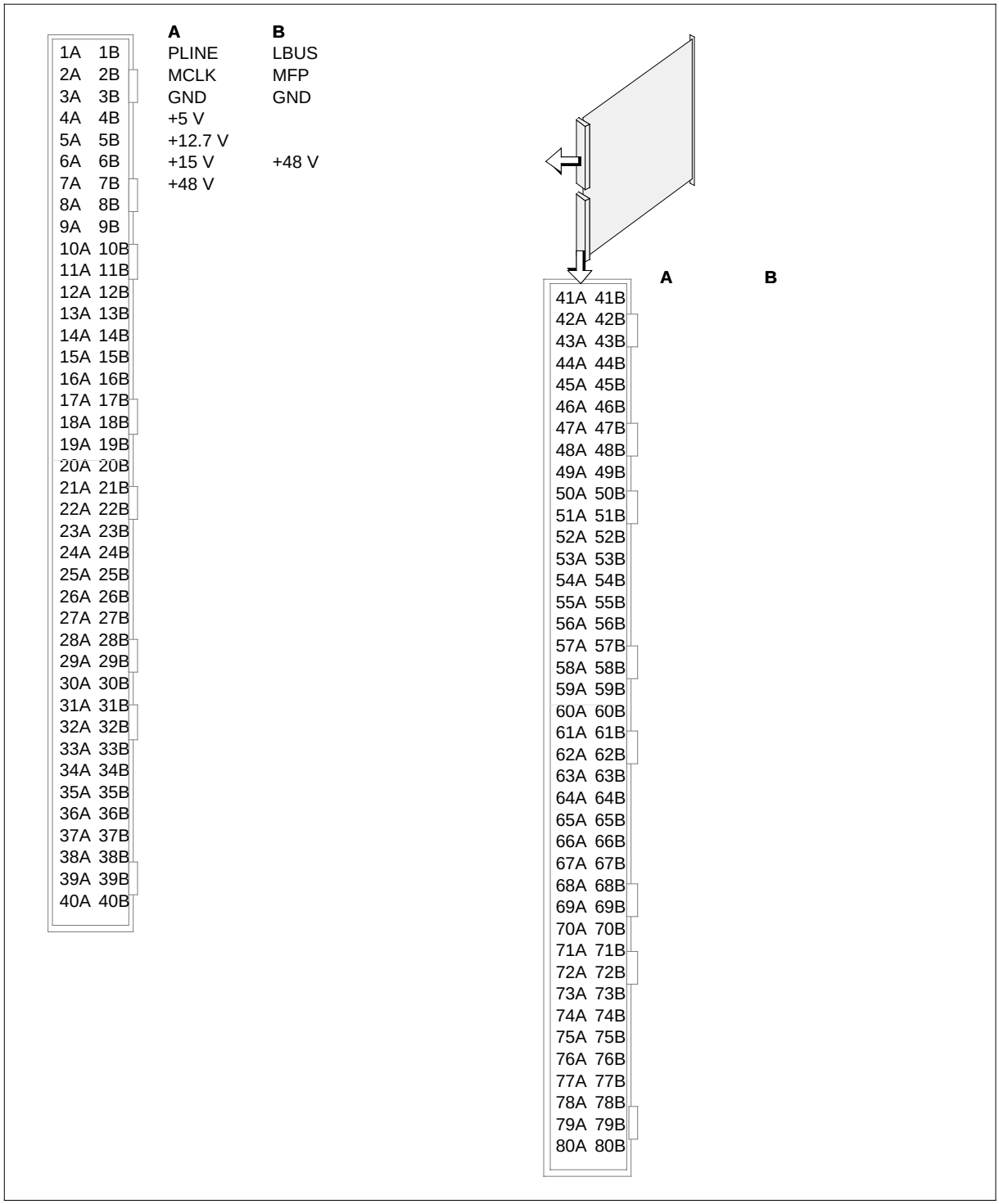
Signaling

Pin numbers

The pin number diagram for the NT6X99AA appears in the following figure.

NT6X99AA (continued)

NT6X99AA pin numbers



NT6X99AA (end)

Technical data

The NT6X99AA has a 1200- to 1400-bps synchronous data rate range. The NT6X99AA has a 50-bps to 19,200-bps asynchronous data rate range. The LCM interface characteristics appear in the following table.

LCM interface characteristics

Characteristic	Value
Clock signal	2.56 MHz
Master frame pulse signal	1.00 kHz
Enable signal format	0 - selects intelligent message format 1 - selects nonintelligent message format
Data transmission rate	64 Kbps
Data transmission structure	
Start	1.0 bit
Mode (0=PCM data; 1=signaling data)	1.0 bit
Data from LCM	8.0 bits
Delay for bidirectional bus reversal	0.5 bit
Data to LCM	8.0 bits
Supervision (buffer full)	1.0 bit
Supervision (data ready)	1.0 bit

Dimensions

The dimensions for the NT6X99AA follow:

- height: 152 mm (6.0 in.)
- depth: 89 mm (3.5 in.)
- width: 20 mm (0.8 in.)

Power requirements

The internal power converter sends the power requirements for the card. The power requirements for the NT6X99AA are a voltage of +5V and a maximum current of 45 mA.

2 NT7Xnnaa

NT7X03AA through NT7X90AA

NT7X03AA

Product description

The XPM Plus Power Manager circuit pack, NT7X03AA, prevents damaging power surges in the NT2X70 when it is powered down or fails. It eliminates a backfeed condition in the powershare circuitry of XPM+ shelves that contain eight (8) or more NT6X50AB pre-release BZ packs. The NT7X03AA eliminates the need for the 2X70 Forming Procedure noted in ER Warnings 960106 and 960088.

The NT7X03AA is a plug-in solution to break the backfeed condition. The NT7X03AA provides enough added +5V shelf current during the power down of an XPM+ shelf to allow proper operation of powershare curcuitry for the NT6X50AB pre-release BZ P-side link packs. The NT7X03AA performs this function by monitoring the state of the -12V rail from the local shelf converter.

Location

The NT7X03AA resides in slot 9 of the XPM shelf. and 17 of PDTCs and PLGCs as part of the upgrade to PDTC+ and PLGC+. This position uses the inherent overlap of FP/MP and MP/SP processor buses on the three processor backplanes. This position reduces the number of required interconnections. The FP and SP memory first occupied these slots, in that order.

Functional description

Two NT7X03AA cards are required to upgrade the PDTC and PLGC (three processor-based peripherals) to PDTC+ and PLGC+ (unified processor-based peripherals), in that order. An NTMX77AA Unified Processor Card and an NTMX71AA Bus Terminator Card are also required to complete the upgrade.

The XPM Plus Power Manager circuit pack provides sufficient +5V current draw that the NT6X50AB and other P-side interface packs powershare correctly after the unit's own shelf power converter (NT2X70) is turned off or has shut down. The NT7X03AA card monitors shelf power status by sensing the -12V rail that comes from the shelf's NT2X70 power converter. The NT7X03AA is in an inactive state while the NT2X70 supplies -12V to the shelf. It draws about 1 milliampere from the +5V and -12V rails. When the NT2X70 power converter stops supplying -12V to the shelf, because it is turned off or the converter fails, the NT7X03AA becomes active and switches a nominal 1.0 Ohm load across the +5V Own rail in the shelf. This extra current load of approximately 5 Amperes on the +5V Own rail provides enough current for the NT6X50AB power share circuitry to switch to the Mate unit's +5V source. This switching action of the NT6X50AB power share circuit removes any residual current flow to the shelf's +5V rail, it allows proper SwAct operation and it eliminates the need to charge the bulk output capacitance of the NT2X70 when the converter needs to be replaced. When the

-12V shelf supply is restored, as when the NT2X70 is replaced or reset, the NT7X03AA returns to the inactive state.

Technical data

The card is a two-layer printed circuit board standard DMS-100 card that measures 31.75 cm by 25.4 cm (12.5 in. by 10 in.). The NT7X03AA consists of 42 straps (tracks) that appear in the following table.

NT7X03AA straps (tracks) scheme (Sheet 1 of 2)

FP/SP Pin	MP Pin	Signal Name	FP/SP Pin	MP Pin	Signal Name
29A	29B	ADDR1	58A	58B	DAT0
30A	30B	ADDR2	59A	60B	DAT1
31A	31B	ADDR3	60A	61B	DAT2
32A	32B	ADDR5	61A	62B	DAT3
33A	33B	ADDR5	62A	63B	DAT4
35A	34B	ADDR6	63A	64B	DAT5
36A	35B	ADDR7	65A	65B	DAT6
37A	36B	ADDR8	66A	66B	DAT7
38A	37B	ADDR9	67A	67B	DAT8
39A	38B	ADDR10	68A	68B	DAT9
40A	39B	ADDR11	69A	69B	DAT10
42A	41B	ADDR12	70A	71B	DAT11
43A	42B	ADDR13	71A	72B	DAT12
44A	43B	ADDR14	72A	73B	DAT13
45A	44B	ADDR15	73A	74B	DAT14
46A	45B	ADDR16	74A	75B	DAT15
47A	46B	ADDR17	13A	11B	LDSN
48A	48B	ADDR18	15A	15B	UDSN
49A	49B	ADDR19	16A	16B	WRTN

NT7X03AA (end)

NT7X03AA straps (tracks) scheme (Sheet 2 of 2)

FP/SP Pin	MP Pin	Signal Name	FP/SP Pin	MP Pin	Signal Name
50A	50B	ADDR20	14A	14B	DTACKN
51A	51B	ADDR21	12A	10B	DASN

Power requirements for system level provisioning

Nominal Active power dissipation operates at 5.15 Vdc VCC = 25 W.

Nominal Standby power dissipation operates at 5.15 Vdc VCC = 5 mW.

Environmental conditions

The following table indicates local ambient temperature.

Local ambient temperature

Condition	Minimum	Maximum
Normal operating temperature range (C)	5	55
Short-term operating temperature range (C)	5	65
Storage temperature range (C)	-50	70

NT7X07AA

Product description

The NT7X07AA is the Internet protocol gateway (IPGW) card. The NT7X07AA provides the gateway functionality in the DMS-100 XMS-based peripheral module (XPM) implementation of an H.323-compliant voice over IP network application. The NT7X07AA provides a voice communications channel between public switched telephone network (PSTN) terminals and H.320 compliant terminals via a non-guaranteed quality of service (QOS) packet network. The NT7X07AA also provides high performance signal processing functionality on two T1 or E1 spans for subsequent use of the circuit pack in central office modem pool or fax relay applications.

Location

The NT7X07AA resides in the DS-1 P-side peripheral interface cards slots in an ISDN line trunk controller (LTCI) frame.

Functional description

The NT7X07AA supports the functions that follow:

- supports 60 concurrent, full-duplex voice channels between PSTN subscribers and H.323 packet network clients such as IP, frame relay, and asynchronous transfer mode (ATM)
- provides two 10/100 million bits per second (Mbit/s) unshielded twisted pair (UTP) interfaces that autosense 802.3 Ethernet
- provides two 25.6 Mbit/s UTP ATM interfaces
- provides two full-featured, long-haul/short-haul T1/E1 interfaces. The interfaces support channelized (24/32 channels) or unchannelized (ATM, ISDN PRI) configurations with complete software configuration of all options and formats
- supports 12 100 million instructions per second (MIPS), 16-bit, fixed-point digital signal processors (DSP) for signal processing operations
- supports a 266 MHz high-performance, embedded PowerPC-based processor for local control and protocol processing
- provides 64 megabytes (Mbyte) of error-correcting code (ECC)-protected memory for control processor operations
- supports two 64 kilobits per second (kbit/s) high-level data link control (HDLC) links for communications with XPM shelf processor
- supports NT6X50/NT6X27 emulation mode
- 48 V dc battery powered circuit pack with on-board point of use power supplies

NT7X07AA (continued)

The NT7X07AA is not backwards compatible with NT6X50 DS1 circuit packs and the NT6X27 E1 circuit packs. The NT7X07AA is primarily an H.323 gateway interface. The NT7X07AA provides equivalent voice functionality as the NT6X50 and NT6X27, but the NT7X07AA is not a facilities interface for telephone applications.

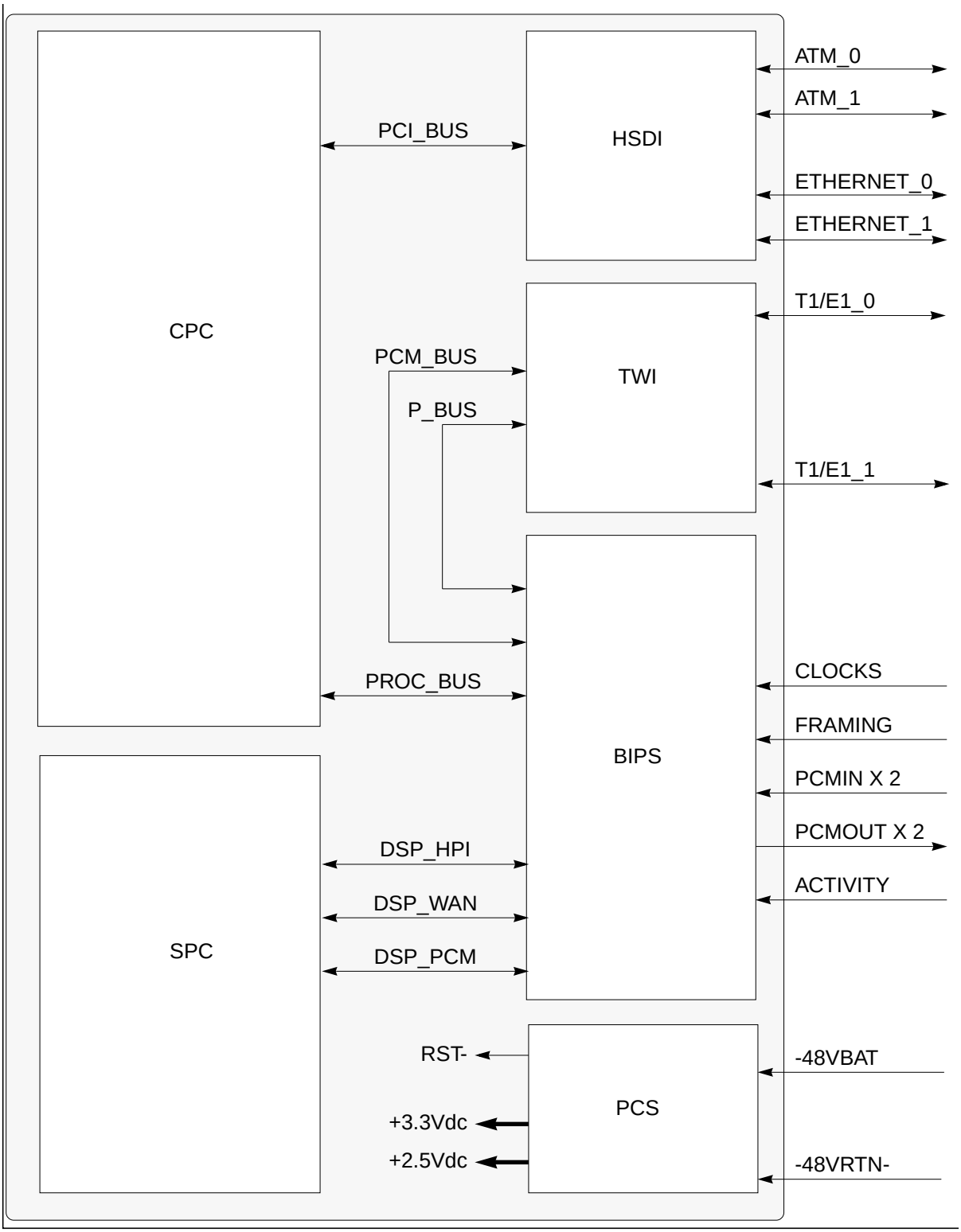
Functional blocks

NT7X07AA includes the functional blocks that follow:

- control processor complex (CPC)
- signal processing complex (SPC)
- telephony/WAN interface (TWI)
- high-speed datacom interface (HSDI)
- backplane interface and processor support (BIPS)
- power conversion system (PCS)

The figure that follows shows the relationship of the functional blocks.

NT7X07AA functional blocks



NT7X07AA (continued)

CPC

The CPC provides the central intelligence and local maintenance functions for the NT7X07AA. Some of these functions follow:

- HDLC-based message operations in the XPM shelf processor
- local area network (LAN) message operations, such as TCP/IP or ATM, with H.323 clients
- wide area network (WAN) message operations, such as ATM and point to point protocol (PPP) and with H.323 clients
- processor messaging operations with the local signal processing engines
- all card-based maintenance operations, either autonomously or by CM request

In a voice over IP application, the CPC uses the HSDI or TWI to perform all messaging between the NT7X07AA and external LAN or WAN clients.

The CPC includes the components that follow:

- Motorola 266 MHz MPC8240 Kahlua Integrated PowerPC processor
- 64 Mbytes of ECC-protected dynamic random access memory (DRAM)
- 2 Mbytes flash electrically erasable programmable read-only memory (EEPROM) as non-volatile memory
- 512 kilobytes (Kbyte) static random access memory (RAM) for log storage and scratchpad memory

SPC

The SPC consists of 12 DSPs and performs signal processing operations for the NT7X07AA. Some of these operations follow:

- transcoding functions between the toll-quality G.711 pulse code modulation (PCM) within the XPM/PSTN and the packetized PCM required by the H.323 clients
- dual tone multi-frequency (DTMF) detection and generation
- voice activity detection
- echo cancellation
- comfort noise generation
- packet loss management

Each DSP has a dedicated 1 megabit (Mbit) SRAM device that supports one wait-state memory access.

TWI

The TWI provides the NT7X07AA with two T1/E1 interfaces. These interfaces can serve as the facilities that follow:

- channelized PCM transmission facilities at 24 or 32 channels
- unchannelized WAN links that support ISDN PRI or ATM communications

Software control controls the selection between T1 and E1 link formats. TWI supports long-haul and short-haul formats.

The TWI permits the NT7X07AA to reside in remote locations without external LAN-to-WAN routing equipment for the T1/E1 WAN facility.

HSDI

The HSDI provides the interface between the NT7X07AA and the H.323 client. The CPC uses the HSDI to pass packetized PCM, control messaging, and signaling to the H.323 clients. The HSDI supports the interfaces that follow:

- two UTP ATM (25.6 Mbit/s) interfaces
- two redundant, auto-sensing 10/100 MBit/s UTP Ethernet interfaces for reliable connectivity to external LAN routing equipment

BIPS

The BIPS performs the functions that follow:

- recovers PCM and timing/framing information from the XPM backplane
- distributes PCM and timing/framing information to the DSPs on the NT7X07AA
- multiplexes the PCM data from the signal processors to redundant DS60 links for transmission to the XPM backplane
- supports the CPC with the processor functions that follow
  - — timers
  - — universal asynchronous receiver transmitter (UART)
  - — interrupt controller
  - — multichannel HDLC interface for the interprocessor communications between the CPC and the XPM shelf processor

NT7X07AA (continued)

PCS

The PCS uses a distributed power scheme to provide power to the components on the NT7X07AA. The PCS performs the functions that follow:

- converts the -48V backplane source to the +3.3V and +2.5V that the NT7X07AA components use
- provides inrush current limiting and overcurrent protection on the -48V supply
- supervisory and soft-start functions on the +3.3V and +2.5V supplies

Connectivity

This section describes the connectivity shown in the figure "NT7X07AA functional blocks" in this chapter.

PCI_BUS

The PCI_BUS is the peripheral component interconnect (PCI) bus. The PCI_BUS is a high-performance, processor-independent, local interconnect bus. The PCI_BUS supports a bus width of 32 bits and operates at 33 MHz. All communications between the CPC, 10/100 Mbit/s Ethernet, and ATM25 LAN interfaces occur over the PCI_BUS.

PROC_BUS

The PROC_BUS is a subset of the MPC8240 Kahlua memory bus. The PROC_BUS supports direct addressing of 16 Mbytes of data. The NT7X07AA uses the PROC_BUS to communicate with processor support peripherals system read-only memory (ROM).

P_BUS

The P_BUS is an 8-bit wide data bus that is a buffered extension of the PROC_BUS. The NT7X07AA uses the bus to configure the T1/E1 framer/transceiver devices in the TWI block.

DSP_HPI

The DSP_HPI is the DSP host port interface. The NT7X07AA uses the DSP_HPI to pass messages and packetized CPM between the CPC and DSPs in the SPC. The DSP_HPI is a buffered subset of the PROC_BUS.

DSP_PCM

The DSP_PCM bus has the features that follow:

- time-division multiplexed
- 8-bit width
- serial PCM data bus

The DSP_PCM carries G.711 data between the BIPS and the 12 DSPs in the SPC. Two electrically isolated buses present the serial data from the XPM backplane to the 12 DSPs in two groups of DSPs. The BIPS multiplexes the data to redundant DS60 links. The SPC packetizes the data on the DSP_PCM bus and forwards the data to the CPC for TCP/IP encapsulation and transmission.

DSP_WAN

The DSP_WAN bus has the features that follow:

- time-division multiplexed
- 8-bit width
- serial PCM data bus

The DSP_WAN carries G.711 data between the BIPS and the 12 DSPs in the SPC. Two electrically isolated buses present the serial data from the TWI to the 12 DSPs in two groups of DSPs. The BIPS multiplexes the data to two PCM links. The BIPS forwards the data to the PCM_BUS for transmission to the TWI.

PCM_BUS

The PCM_BUS has the features that follow:

- time-division multiplexed
- 8-bit width
- serial PCM data bus

The PCM_BUS carries G.711 data between the BIPS and the two T1/E1 framers/transceivers in the TWI. The BIPS performs the necessary re-timing and framing to interface DSP_WAN and PCM_BUS signals. Data on the PCM_BUS supports non-packet, real-time PCM and data applications, such as echo cancellation and NT6X50./NT6X27 applications. Data on the PCM_BUS does not support H.323 applications.

ETHERNET_0/ETHERNET_1

The ETHERNET_0/ETHERNET_1 interfaces provide redundant 10/100 Mbit/s of LAN connectivity to external Ethernet routing equipment. This connectivity supports the transfer of packetized voice between the NT7X07AA and LAN-based clients.

T1/E1_0/T1/E1_1

The T1/E1_0 and T1/E1_1 interfaces provide two external, industry-standard WAN or telephony interfaces for the NT7X07AA. These interfaces allow the

NT7X07AA (continued)

NT7X07AA to reside at a remote site with external LAN-to-WAN routing equipment. These links can carry the types of data that follow:

- traditional data
- channelized telephony PCM
- unchannelized data links, such as PRI or ATM

ATM_0/ATM_1

The ATM_01 and ATM_01 interfaces provide redundant, industry-standard ATM25 interfaces as an alternate datacom interface to the T1/E1 or Ethernet links. The ATM25 interface can carry the information that follow:

- packetized PCM
- G.711 PCM
- data

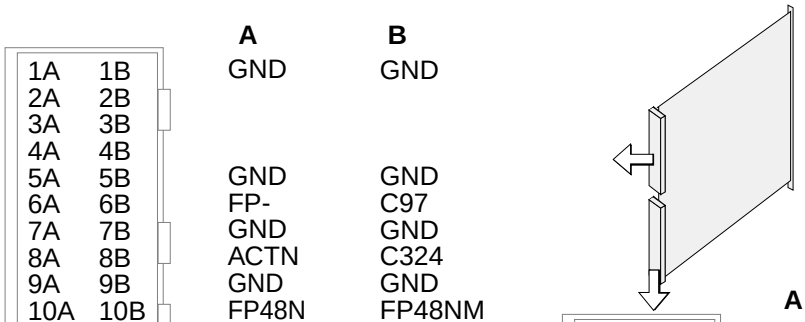
Signaling

This section describes the pin outs and timing of the messaging on the DS60 links.

Pin outs

The figure that follows shows the pin outs for NT7X07AA.

NT7X07AA pin outs



	A	B
1A 1B	GND	GND
2A 2B		
3A 3B		
4A 4B		
5A 5B	GND	GND
6A 6B	FP-	C97
7A 7B	GND	GND
8A 8B	ACTN	C324
9A 9B	GND	GND
10A 10B	FP48N	FP48NM
11A 11B	SENDT0	SENDR0
12A 12B	SENDT1	SENDR1
13A 13B		GND
14A 14A	GND	
15A 15B		GND
16A 16B		GND
17A 17B	C97M	FPM-
18A 18B	GND	C324M
19A 19B	DSOUT	DSOUTM
20A 20B	GND	
21A 21B	ETS-	ETSM-
22A 22B		
23A 23B	-48VBAT	-48VBAT
24A 24B		
25A 25B		
26A 26B	-48VBRTN	-48VBRTN
27A 27B		
28A 28B		
29A 29B		
30A 30B		
31A 31B		
32A 32B		
33A 33B		
34A 34B		
35A 35B		
36A 36B		
37A 37B		
38A 38B		
39A 39B		
40A 40B		

	A	B
41A 41B		
42A 42B		
43A 43B		
44A 44B	ATM0_TX+	ATM0_RX-
45A 45B		
46A 46B	ATM0_TX-	ATM0_RX+
47A 47B		
48A 48B	ATM1_TX+	ATM1_RX-
49A 49B		
50A 50B	ATM1_TX-	ATM1_RX+
51A 51B		
52A 52B	ETH0_TX+	ETH0_RX-
53A 53B		
54A 54B	ETH0_TX-	ETH0_RX+
55A 55B		
56A 56B	ETH1_TX+	ETH1_RX-
57A 57B		
58A 58B	ETH1_TX-	ETH1_RX+
59A 59B		
60A 60B		
61A 61B		
62A 62B		
63A 63B		
64A 64B		
65A 65B		
66A 66B		
67A 67B		
68A 68B		
69A 69B	C	CM
70A 70B		
71A 71B		
72A 72B	RECT0	RECR0
73A 73B	RECT1	RECR1
74A 74B	RECFP	RECFPM
75A 75B	T1IN	T1INM
76A 76B	GND	GND
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

NT7X07AA (continued)

The table that follows describes each pin out.

NT7X07AA pin out descriptions (Sheet 1 of 4)

Pin	Signal	Function	Description	Pin	Signal	Function	Description
1A	GND	Input	Shelf logic ground	1B	GND	Input	Shelf logic ground
5A	GND	Input	Shelf logic ground	5B	GND	Input	Shelf logic ground
6A	FP-	Input	Receive frame pulse from port 0 of own shelf	6B	c97	Input	10.24 MHz host clock from own shelf
7A	GND	Input	Shelf logic ground	7B	GND	Input	Shelf logic ground
8A	ACTN	Input	Shelf activity indicator	8B	C324	Input	3.088 MHz clock from own shelf
9A	GND	Input	Shelf logic ground	9B	GND	Input	Shelf logic ground
10A	FP48N	Input	48 frame host frame fuse from own shelf	10B	FP48NM	Input	48 frame host frame pulse from own shelf
11A	SENDT0	Output	Port 0 DS1/E1 bipolar data transmit tip	11B	SENDR0	Output	Port 0 DS1/E1 bipolar data transmit ring
12A	SENDT1	Output	Port 1DS1/E1 bipolar data transmit tip	12B	SENDR1	Output	Port 1DS1/E1 bipolar data transmit ring
				13B	GND	Input	Shelf logic ground
14A	GND	Input	Shelf logic ground				
				15B	GND	Input	Shelf logic ground
				16B	GND	Input	Shelf logic ground

NT7X07AA pin out descriptions (Sheet 2 of 4)

Pin	Signal	Function	Description	Pin	Signal	Function	Description
17A	C97M	Input	10.24 MHz host clock from mate shelf	17B	FPM-	Input	Receive frame pulse from port 0 of mate shelf
18A	GND	Input	Shelf logic ground	18B	C324M	Input	3.088 MHz clock from mate shelf
19A	DSOUT	Input	5.12 MHz multiplexed serial incoming data from own shelf	19B	DSOUTM	Input	5.12 MHz multiplexed serial incoming data from mate shelf
20A	GND	Input	Shelf logic ground				
21A	ETS-	Input	Enhanced timeswitch enable from own shelf	21B	ETSM-	Input	Enhanced timeswitch enable from mate shelf
23A	-48VBAT	Input	-48 volt battery	23B	-48VBAT	Input	-48 volt battery
26A	-48VBRTN	Input	-48 volt battery return	26a	48VBRTN	Input	-48 volt battery return
44A	ATM0_TX+	Output	25.6 Mbit/s ATM twisted pair transmit data+ (link 0)	44B	ATM0_RX+	Input	25.6 Mbit/s ATM twisted pair receive data- (link 0)
46A	ATM0_TX-	Output	25.6 Mbit/s ATM twisted pair transmit data -(link 0)	46B	ATM0_RX-	Input	25.6 Mbit/s ATM twisted pair receive data+ (link 0)
48A	ATM1_TX+	Output	25.6 Mbit/s ATM twisted pair transmit data+ (link 1)	48B	ATM1_RX+	Input	25.6 Mbit/s ATM twisted pair receive data- (link 1)
50A	ATM1_TX-	Output	25.6 Mbit/s ATM twisted pair transmit data- (link 1)	50B	ATM1_RX-	Input	25.6 Mbit/s ATM twisted pair receive data+ (link 1)

NT7X07AA (continued)

NT7X07AA pin out descriptions (Sheet 3 of 4)

Pin	Signal	Function	Description	Pin	Signal	Function	Description
52A	ETH0_TX+	Output	10/100 Mbit/s Ethernet twisted pair transmit data+ (link 0)	52B	ETH0_RX-	Input	10/100 Mbit/s Ethernet twisted pair receive data- (link 0)
54A	ETH0_TX-	Output	10/100 Mbit/s Ethernet twisted pair transmit data- (link 0)	54B	ETH0_RX+	Input	10/100 Mbit/s Ethernet twisted pair receive data+ (link 0)
56A	ETH1_TX+	Output	10/100 Mbit/s Ethernet twisted pair transmit data+ (link 1)	56B	ETH1_RX-	Input	10/100 Mbit/s Ethernet twisted pair receive data- (link 1)
58A	ETH1_TX-	Output	10/100 Mbit/s Ethernet Twisted Pair Transmit Data- (link 1)	58B	ETH1_RX+	Input	10/100 Mbit/s Ethernet twisted pair receive data+ (link 1)
69A	C	Input	Port enable from own shelf	69B	CM	Input	Port enable from mate shelf
72A	RECT0	Input	Port 0 DS1/E1 bipolar data receive tip	72B	RECR0	Input	Port 0 DS1/E1 bipolar data receive ring
73A	RECT1	Input	Port 1 DS1/E1 bipolar data receive tip	73B	RECR1	Input	Port 1 DS1/E1 bipolar data receive ring
74A	RECFP	Output	Recovered link frame pulse to own shelf	74B	RECFPM	Output	Recovered link frame pulse to mate shelf
75A	T1IN	Output	5.12 MHz multiplexed serial outgoing data to own shelf	75B	T1INM	Output	5.12 MHz multiplexed serial outgoing data to mate shelf

NT7X07AA pin out descriptions (Sheet 4 of 4)

Pin	Signal	Function	Description	Pin	Signal	Function	Description
76A	GND	Input	Shelf logic ground	76B	GND	Input	Shelf logic ground
78A	GND	Input	Shelf logic ground	78B	GND	Input	Shelf logic ground
80A	GND	Input	Shelf logic ground	80B	GND	Input	Shelf logic ground

Timing

The NT7X07AA uses DS0 channels in the serial DS60 PCM links to interface with the XPM. Each NT7X07AA terminates two DS60 links. The backplane ACT signal indicates the valid DS60 link for receiving data.

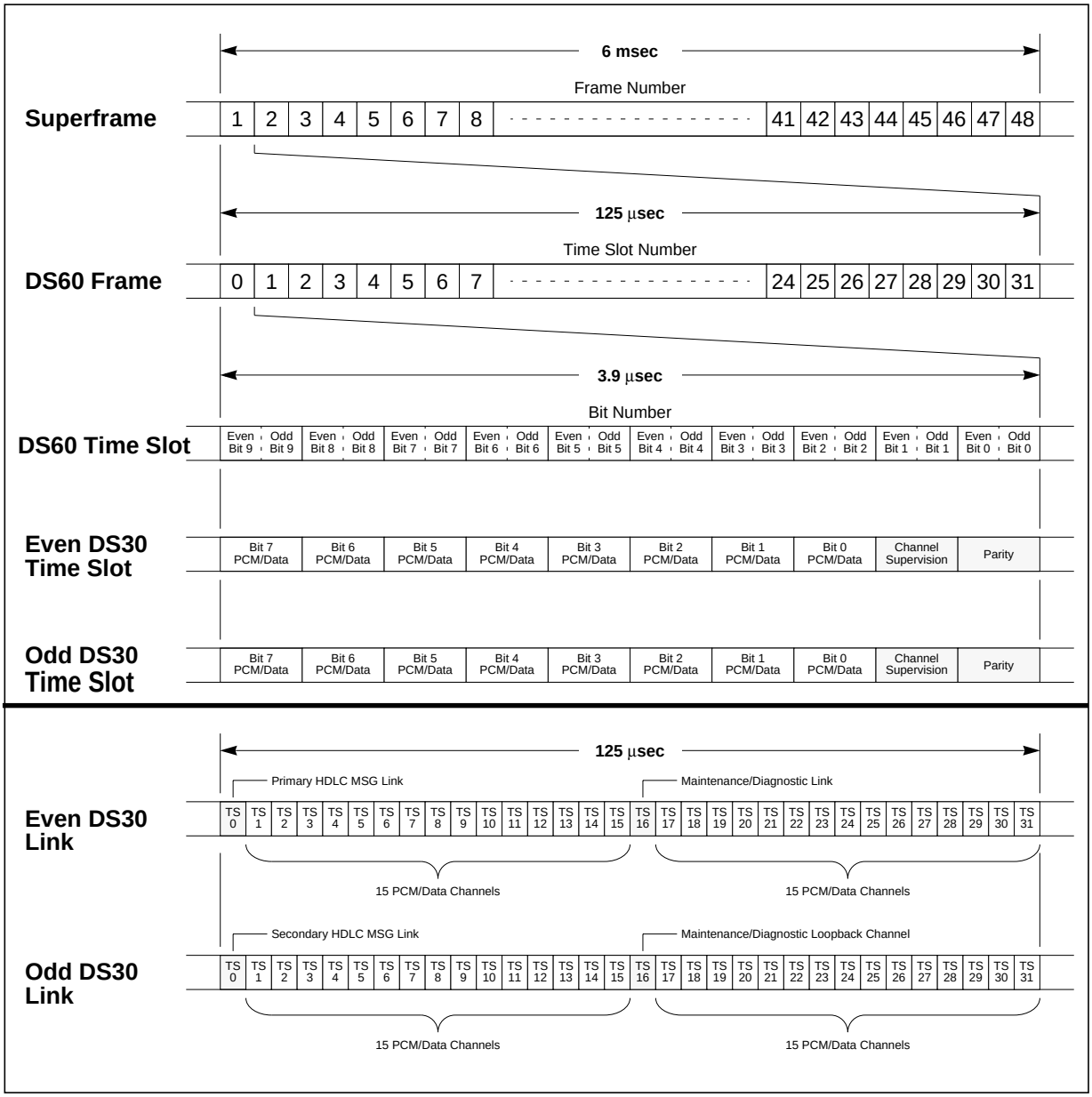
In the transmit direction, both DS60 links carry identical data in each timeslot. The NT7X07AA terminates 64 active channels. The information on the channels follows:

- Sixty channels carry PCM data.
- Two channels carry HDLC messages between the NT7X07AA and the XPM shelf processor.
- Two channels carry low-level control, maintenance, and diagnostic information.

Each DS60 link consists of two two multiplexed DS30 links. The figure that follows shows the timing format of the DS60/DS30 links for the NT7X07AA.

NT7X07AA (continued)

NT7X07AA timing on DS60/DS30 links



Technical data

This section provides technical data on the NT7X07AA.

Power requirements

A point-of-use power supply (PUPS) provides power to the components on the NT7X07AA. The PUPS converts the -48V backplane source to the +3.3V and +2.5V that the NT7X07AA components use.

The table that follows lists the power specifications and ratings for the NT7X07AA PUPS.

NT7X07AA PUPS power specifications and ratings

Parameter	min	typ	max	Units
Input supply voltage	36	48	75	Vdc
Input to output isolation voltage			1500	Vdc
Input isolation capacitance		2500		pF
Input isolation resistance	10			MW
Operating case temperature			100	^{o}C
Input current (V_{in} = 48 Vdc, I_{out} =10 Adc)		0.9	2.5	Adc
Inrush current			1.0	A^2s
Input reflected ripple (5 Hz to 20 MHz)		5		mA_{p-p}
Input ripple rejection (120 Hz)		60		dB
Output voltage (T_{in} = min - max, V_{in} = min - max, I_{out} = min - max)	3.2	3.3	3.4	Vdc
Output Current	0.5		10	Adc
Output regulation Line (V_{in} = 36 Vdc - 75 Vdc) Load (I_{out} = 0.5 Adc - 10 Adc) Temperature (T_c = -40 ^{o}C - 100 ^{o}C)		 0.01 0.05 15	 0.1 0.2 50	 % % mV
Output ripple and noise RMS Peak-to-peak (5 Hz to 20 MHz)				 mV_{rms} mV_{p-p}
Efficiency (V_{in} = 48 Vdc, I_{out} = 10 Adc)	78	81		%
Calculated MTBF		2,600,000		hr

NT7X26AE

Product description

The NT7X26AE dual network packaged core (DNPC) frame groups the functions of a central control complex (CCC) and network module (NM). The DNPC is a double bay unit that contains a pair of CCCs and two pairs of NMs.

The NT7X2701 NM shelves group network interface (NI) circuit cards with network crosspoint (XPT) circuit cards on the same shelf.

Each CCC contains a grouped CPU and memory shelf (CPM) and a grouped message/device controller (MDC) and memory shelf.

The NT7X26AE frame is the basic part in a DMS-100 packaged system.

Parts

The NT7X26AE consists of the following parts:

- NT3X90AA—Cooling/inverter unit
- NT7X2701—Network crosspoint (NC) interface shelf
- NT7X2801—MDC and memory shelf
- NT7X3102—CPU and memory shelf
- NT7X34AA—Frame supervisory panel (FSP)

Cooling/inverter unit

The NT3X90AA cooling unit uses ac-powered fans. As a result, the NT3X90AA cooling unit has two dc-ac converters. The NT0X42 power distribution center (PDC) A-bus through a 5A fuse feeds one inverter. The PDC B-bus through a 5A fuse feeds the other inverter.

The NT3X90AA cooling unit uses an NT3X9000 inverter.

Network crosspoint shelf

The NT7X26AE crosspoint interface shelf groups the functions of the NI with the network XPT on a single shelf. This shelf is different from network frames, like the NT5X13AA. In the NT5X13AA, the NI (NT5X16AA/AB) and XPT (NT5X15AA/AB) cards each occupy shelves. The NT7X2701 is a single backplane version of the NT5X13AA network without junctors.

The cards of the NT7X26AE have the same function as the cards of the NT5X13AA. These cards are in different slots in the shelves. The NT7X26AE cannot be expanded like the NT5X13AA.

The NT7X26AE has seven interface cards (numbered 0 to 6) with eight ports each. A total of 56 ports on each shelf are available. All ports are connected to peripheral side (P-side) links. The NT7X26AE has a serial-to-parallel formatter for the A-side and a parallel-to-serial formatter for the B-side.

The NT7X26AE does not have serial junctors because half of one network is hard-wired to half of the other. The NT7X26AE has two network configurations.

Message device controller and memory shelf

The MDC shelf groups the central message controller (CMC) and input/output controller (IOC) on the same equipment shelf.

The CMC provides an interface between the CPU and the network message controllers (NMC) of the switching network. The IOC controls the flow of data between the CPU and input/output (I/O) devices. The input/output devices include magnetic tape units, disk drive units, and visual display units.

The double bay frame provides duplicated MDCs. Duplicated MDCs can connect all CPU peripherals through the network frame/module and IOC as CMC0:00 and CMC1:00. The MDC can interface to a limited number of I/O devices when the MDC functions as an IOC.

The MDC can function as a normal CMC. The MDC can operate as an IOC. Because these functions overlap with card slot assignment, each function reduces the capacity of the other function.

Central processor unit and memory shelf

The CPU and program store (PS) memory occupy one shelf in the DNPC frame called the CPM. The CPM houses the DMS-100F NT40 CPU and PS (NT3X45EP and NT3X45EQ) circuit packs (CP).

The double bay DNPC frame provides duplicated CPMs that accommodate a maximum of 7.75 Mword of PS memory. A memory card is not required for spare memory. A spare row of memory devices on the controller serves as the hot spare.

The PS memory provides storage for the programs required for call processing, administration, maintenance, and the operating system.

Frame supervisory panel

The NT0X28AK FSP contains power control and alarm circuits. The power control and alarm circuits monitor the power supply to the DNPC from the power distribution center (PDC) in the digital switching system.

NT7X26AE (continued)

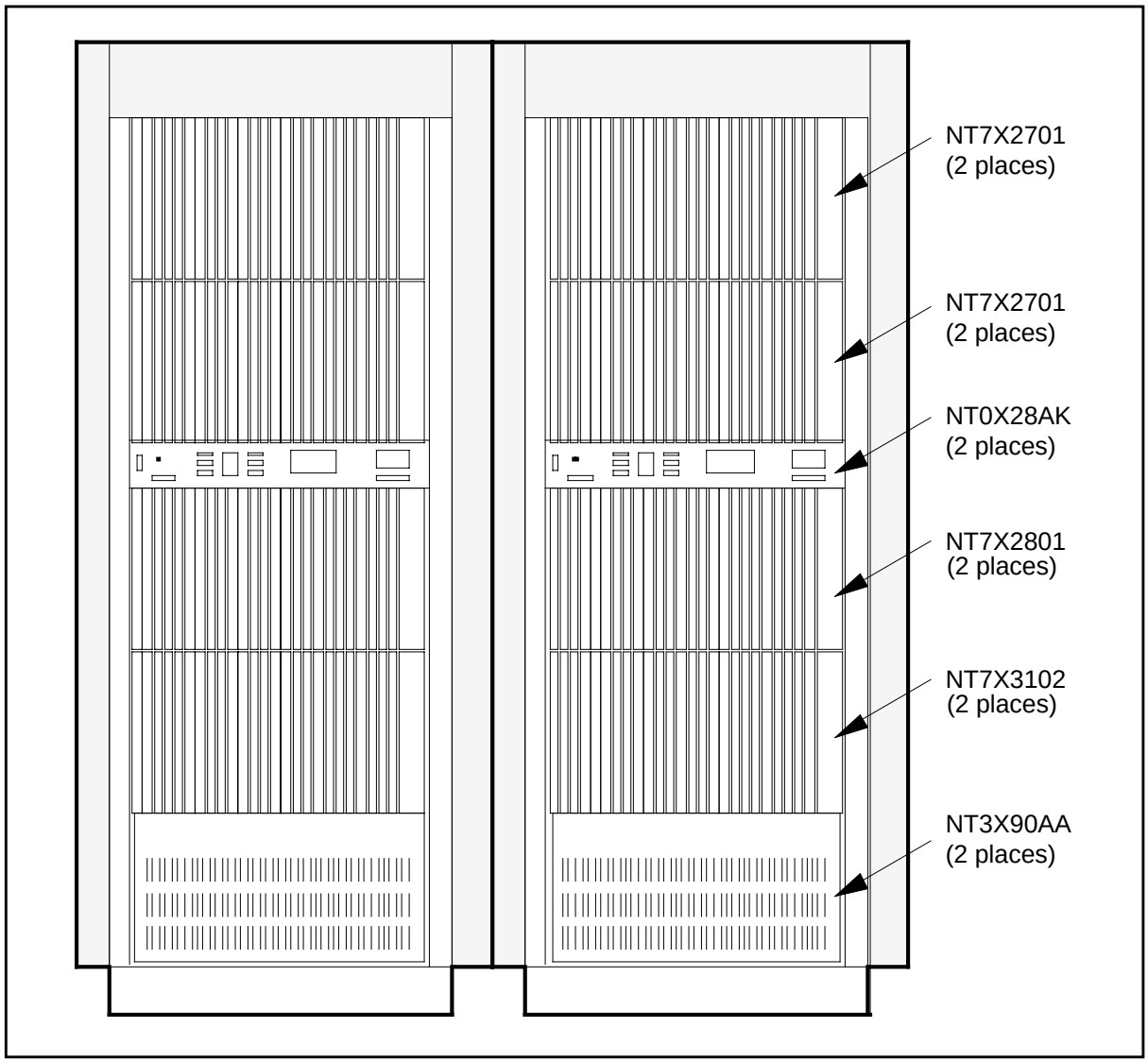
The NT0X28AK FSP conveys the needed potential from the office battery, -48V nominal, through four power feeds. The NT0X28AK FSP uses four circuit breakers to protect the power control and alarm circuits to the shelves in the DNPC. Several NT0X28 models use fuses to protect the power control. Several models require two or three power feeds.

The NT0X28AK has a feature called a mechanical interlock. This feature consists of a small sliding cover. The cover allows access to two of the circuit breakers at a time. For example, to CB1 and CB2 or to CB4 and CB5. If all four circuit breakers are ON at the start, you cannot trip circuit breakers in both groups.

Design

The design of the appears in the following figure.

NT7X26AE (end)



Note: This diagram is not drawn to scale.

NT7X38AB

Product description

The NT7X38AB packaged core line module (PCLM) frame provides line concentrating modules (LCM) for the packaged DMS-100 system. The NT7X38AB PCLM is like the NT6X03 line concentrating equipment (LCE) frame.

The LCMs are peripheral modules (PM) that interface the line trunk controller (LTC) or line group controller (LGC) and a maximum of 640 subscriber lines. The parts interface through the use of two to six DS30A links.

The NT7X38AB PCLM contains two LCMs. Each LCM consists of two NT7X3801 PCLM shelves and two associated NT6X30 ringing generators. The shelves and generators are in an NT6X35AA frame supervisory panel (FSP).

Parts

The NT7X38AB consists of the following parts:

- NT6X35AA—LCE FSP
- NT7X3801—PCLM shelf assembly
- NT7X3833—Line fan unit

LCE frame supervisory panel

The NT6X35AA FSP contains power control and alarm circuits. These circuits monitor the power supply from the power distribution center (PDC) in the digital switching system. The power supply continues on to the NT6X53 power converters in the PCLM shelves.

The NT6X35AA FSP conveys the required potential from the office battery, -48V nominal, through four power feeds. The NT6X35AA FSP uses four circuit breakers to protect the power control and alarm circuits to the shelves in the PCLM. This process occurs in contrast to several NT0X28 models that use fuses to protect the power control. This process is also in contrast to several models that require two or three power feeds.

The NT6X35AA FSP contains two ringing generators (RG). These generators operate separately. The FSP circuits power the generators. The LCM provides operational signals to and from the RGs.

PCLM shelf assembly

A NT7X3801 pair forms an LCM. Each NT7X3801 shelf consists of line subgroup (LSG) circuit cards, an LCM processor, a digroup control card (DCC), and a power converter.

The control complex of each NT7X3801 can take over control of PCLM shelves of the LCM. The control complex can perform this action if the mate control complex fails.

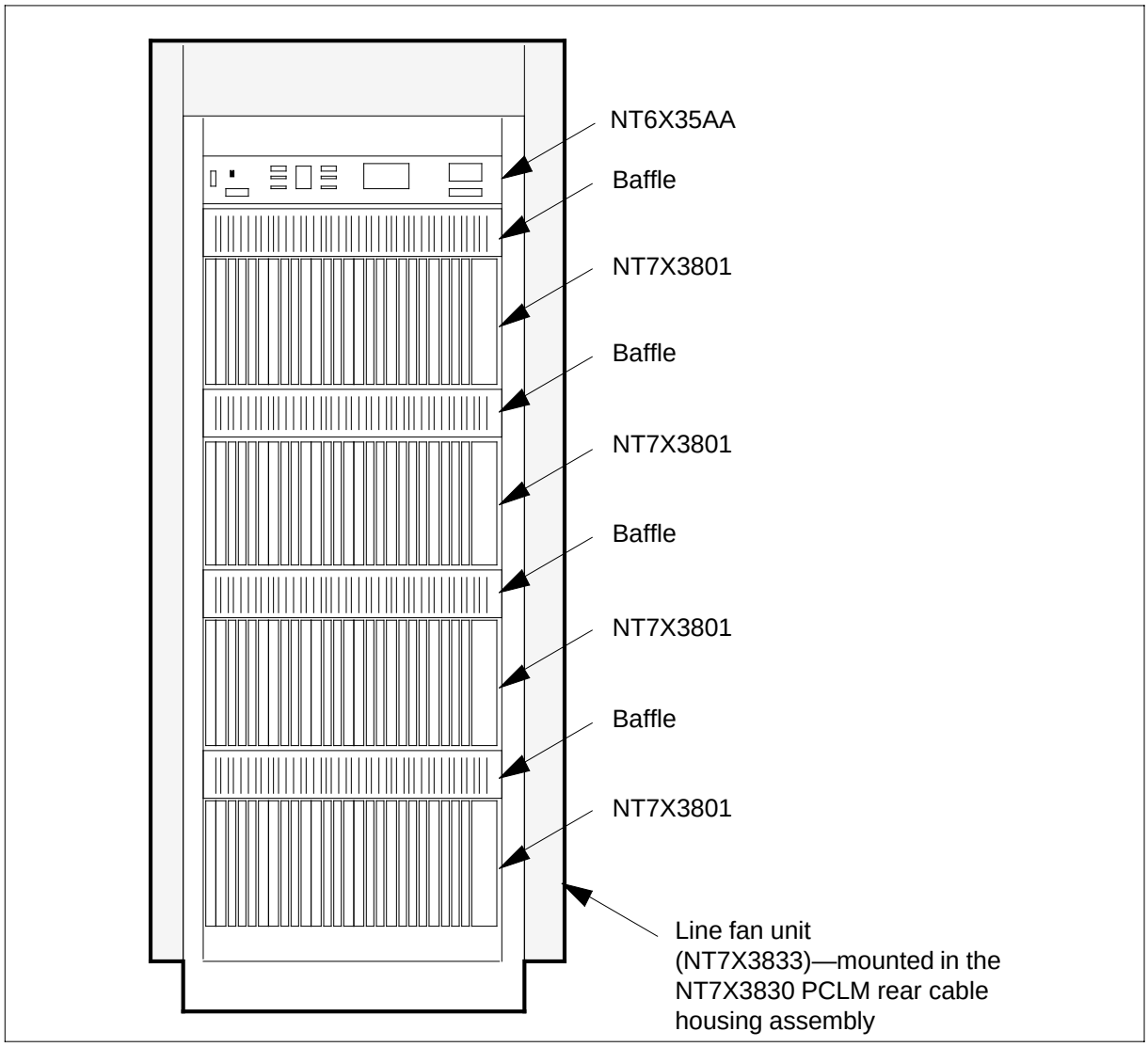
Line fan unit

The NT7X3833 line fan unit cools the NT7X38AB PCLM. The fan unit is part of the NT7X3830 PCLM rear cable housing assembly.

Design

The design of the NT7X38AB appears in the following figure.

NT7X38AB parts



NT7X53AA

Product description

The NT7X53AA remote interface and maintenance common fill is in each remote interface and maintenance (RIM) module. The RIM module is a group of a remote maintenance module (RMM) and a host interface equipment module. The RIM module supports maintenance and service circuits for remote integrated voice and data service. The RIM module also provides for the available capabilities of intra-calling and emergency stand-alone (ESA) operation.

Each RIM module is paired with a digital line module (DLM). Each RIM module is an interface. This interface is between the DLM at a remote site and the DS-1 links to a line group controller or line trunk controller at the host. The RIM module can be as far as 241 km (150 miles) from the DMS network.

A RIM module occupies one shelf in a Meridian cabinet digital remote frame, NTNX49AA. Each NTNX49AA frame houses one remote digital line module (RDLM). Each RDLM contains one or two pairs of RIM and DLM modules.

Parts

The NT7X53AA common fill contains the following parts:

- NT2X09AA—multioutput power converter card
- NT2X70AA—power converter (2) cards
- NT6X73AA—link control card (LCC) (2) cards
- NT6X74AB—RMM control card

Design

The parts appear in the following table. The figure that follows the table displays the position of the six cards in the RIM common fill.

NT7X53AA parts (Sheet 1 of 2)

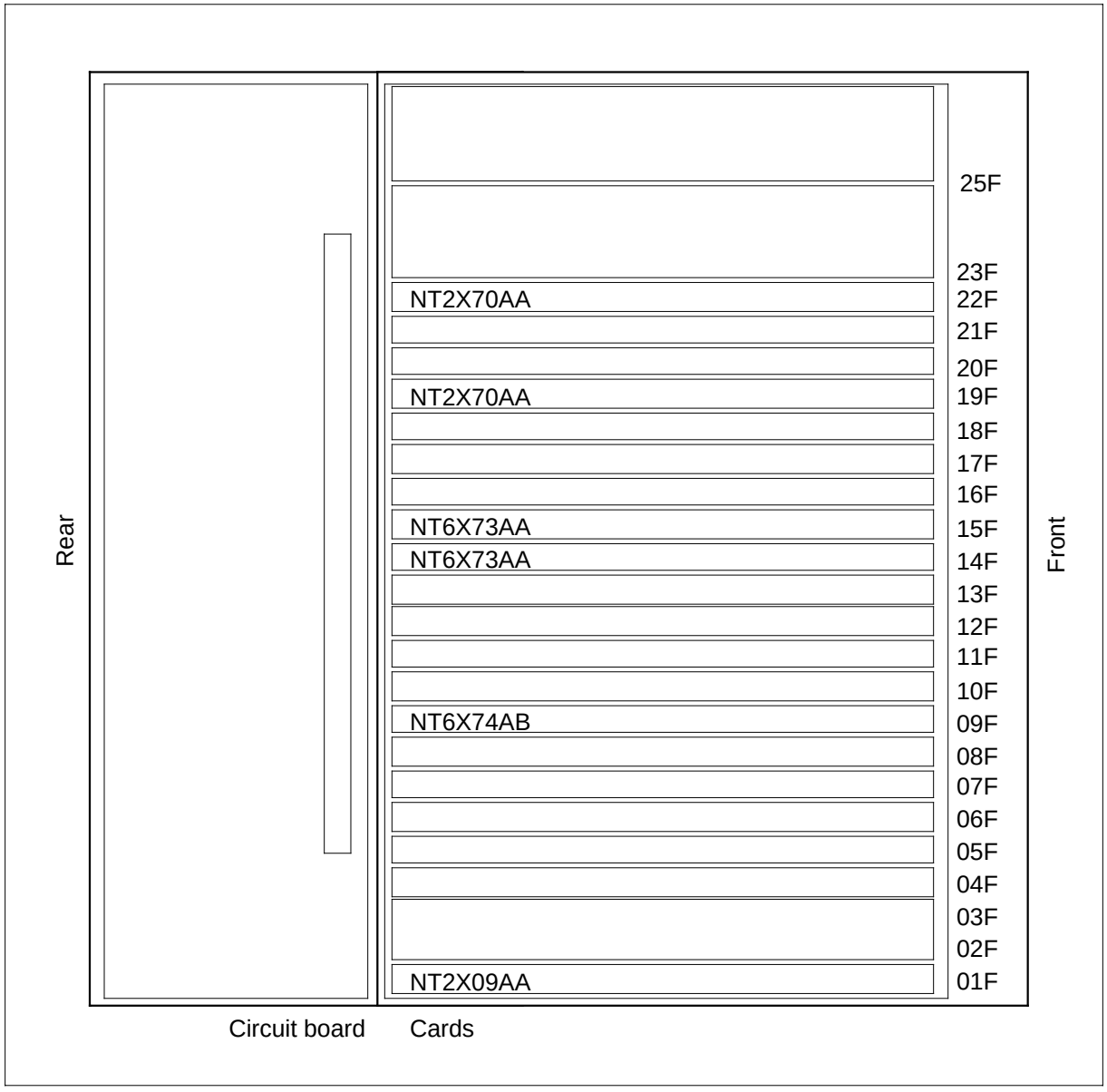
PEC	Slot	Description
NT2X09AA	1F	*Multioutput power converter card* The power converter card converts the dc voltage of -48V into the dc operating voltages (-5, -15, +5, +12, and +24V) that the circuits require in the RIM module. The card includes a low-voltage monitor circuit, overvoltage and overcurrent protection. The card also includes faceplate test jacks and a faceplate light-emitting diode (LED) status indicator.

NT7X53AA (end)

NT7X53AA parts (Sheet 2 of 2)

PEC	Slot	Description
NT2X70AA	19F, 22F	*Power converter card* The power converters provide the dc supplies of -5, -12, +12, and +15V needed by the circuits in the RIM module. The card includes a low-voltage monitor circuit, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate LED status indicator.

NT7X53AA parts



NT7X76BA

Product description

The wideband test access (WTA) panel is a cross–connect panel that provides metallic cross–connect capability. This capability is to test DMS wideband subscriber services. These services include ISDN, Datapath, and voice frequency DMS–100 subscriber services. Use the WTA panel to test the ISDN. Use the WTA panel to test Datapath service. The NT7X76BA WTA panel is for the dedicated line test unit/multiline test unit (LTU/MTU) function. You can connect a maximum of two dedicated LTU/MTUs to each NT7X76BA panel.

The WTA panel replaces the main distributing frame (MDF) with the metallic cross-connection of test circuits. These circuits include the LTU/MTU, metallic test access, and line equipment in DMS offices. The current MDF cabling cannot support tests of more current subscriber services transmission damage. This action occurs when you switch an excess of office cabling.

This panel mounts on the NT0X02AB miscellaneous equipment (MIS) frame. This panel allows the removal of cabling to the MDF. The removal results in much shorter wiring for subscriber services tests. If the MIS frame does not have WTA panels, you can mount other valid hardware units.

Parts

The NT7X76BA WTA panel is the NT7X75BA circuit board fastened in mounting brackets.

Multiple WTA panels are used. The correct number and configuration differs with office size. Offices larger than 75 000 lines require more than three WTA panels.

For offices with dedicated LTU/MTUs, the first row of WTA panels are type NT7X76BA. If connection to more dedicated LTU/MTUs is required, use type NT7X76BA panels for the second row of WTA panels. In other occurrences, use the NT7X76AA WTA panel.

For primary and extension offices that require new frames, mount the WTA panels on shelf positions 65, 51, 32, 18, and 04. First, mount the panels on the front. Second, mount the panels on the back of the MIS frame. To install the panels on current MIS frames, mount the WTA panels on an available position of the frame. The top shelf position is better. For ease of engineering cables, the WTA panels are assigned from the top position down on the MIS frame.

Correct position of frames around the MIS frame allows office wiring signal loss to be less than 1 dB. The NT3X09AA/BA cards and LTU/MTUs with

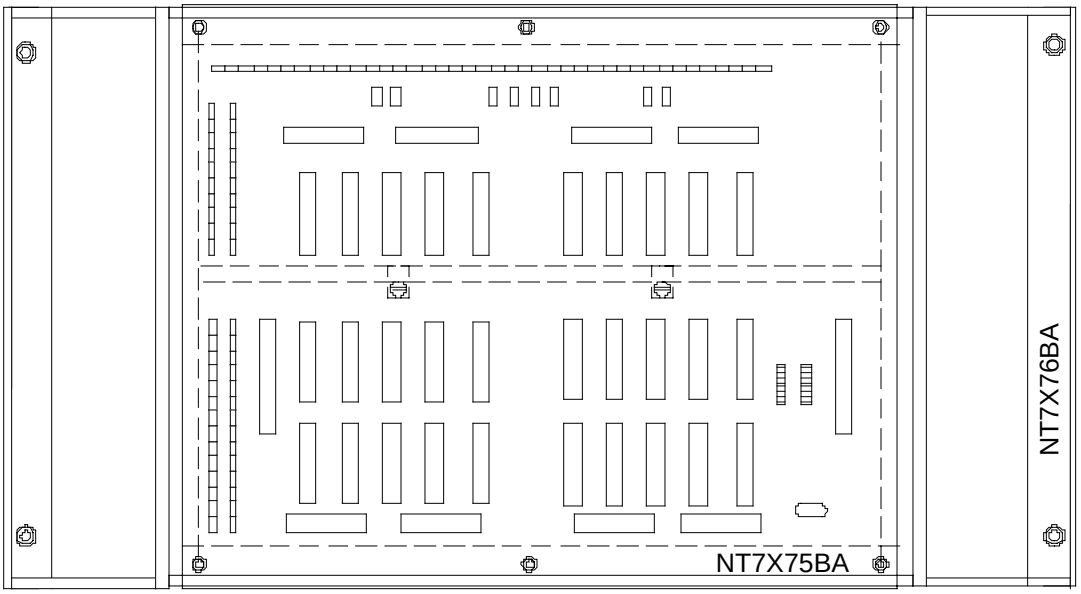
NT7X76BA (end)

maintenance trunk modules must be the least in number. The cards and LTU/MTUs must be in frames next to an MIS frame with WTA panels. Line concentrating equipment frames and ISDN line concentrating equipment frames must be around an MIS frame with WTA panels.

Design

A front view of the NT7X76BA WTA panel appears in the following figure.

NT7X76BA parts



Front view

NT7X80AA

Product description

The bus shorter card connects the FP bus, the MP bus, and the SP bus on three processor XPMs. The card consists of shorting tracks that connect the following:

- address buses ADDR0 to ADDR21
- data buses DAT0 to DAT15
- processor control signals LDS, UDS, WRT, DTACK, DAS

Location

Insert the NT7X80AA in slots 13 and 17 of PDTCs and PLGCs as part of the upgrade to PDTC+ and PLGC+. This position uses the inherent overlap of FP/MP and MP/SP processor buses on the three processor backplanes. This position reduces the number of required interconnections. The FP and SP memory first occupied these slots, in that order.

Functional description

Two NT7X80AA cards are required to upgrade the PDTC and PLGC (three processor-based peripherals) to PDTC+ and PLGC+ (unified processor-based peripherals), in that order. An NTMX77AA Unified Processor Card and an NTMX71AA Bus Terminator Card are also required to complete the upgrade.

Technical data

The card is a two-layer printed circuit board standard DMS-100 card that measures 31.75 cm by 25.4 cm (12.5 in. by 10 in.). The NT7X80AA consists of 42 straps (tracks) that appear in the following table.

NT7X80AA straps (tracks) scheme (Sheet 1 of 2)

FP/SP Pin	MP Pin	Signal Name	FP/SP Pin	MP Pin	Signal Name
29A	29B	ADDR1	58A	58B	DAT0
30A	30B	ADDR2	59A	60B	DAT1
31A	31B	ADDR3	60A	61B	DAT2
32A	32B	ADDR5	61A	62B	DAT3
33A	33B	ADDR5	62A	63B	DAT4
35A	34B	ADDR6	63A	64B	DAT5
36A	35B	ADDR7	65A	65B	DAT6

NT7X80AA (end)

NT7X80AA straps (tracks) scheme (Sheet 2 of 2)

FP/SP Pin	MP Pin	Signal Name	FP/SP Pin	MP Pin	Signal Name
37A	36B	ADDR8	66A	66B	DAT7
38A	37B	ADDR9	67A	67B	DAT8
39A	38B	ADDR10	68A	68B	DAT9
40A	39B	ADDR11	69A	69B	DAT10
42A	41B	ADDR12	70A	71B	DAT11
43A	42B	ADDR13	71A	72B	DAT12
44A	43B	ADDR14	72A	73B	DAT13
45A	44B	ADDR15	73A	74B	DAT14
46A	45B	ADDR16	74A	75B	DAT15
47A	46B	ADDR17	13A	11B	LDSN
48A	48B	ADDR18	15A	15B	UDSN
49A	49B	ADDR19	16A	16B	WRTN
50A	50B	ADDR20	14A	14B	DTACKN
51A	51B	ADDR21	12A	10B	DASN

Power requirements

Electronic devices on this card are not present.

NT7X90AA

Product description

The NT7X90AA frame supervisory panel (FSP), provides the power control circuits needed by the power converters and ringing generators (RG) located in individual shelves. The FSP includes frame-fail indicators and a fuse-fail alarm output.

The panel has five circuit breakers and eight fuses. It monitors the condition of the power converters and the RGs in the shelves. It also monitors the input voltage from the power distribution center (PDC).

Components

The NT7X90AA consists of the following components:

- Power distribution center
- NT7X92AA—(two) ringing generators

Power distribution center

The power distribution center distributes -48V dc to equipment used in the SRU60 frame. It detects power converter card and fuse failures. The FSP provides automatic recovery from low battery (ARLB), which prevents the five circuit breakers from tripping when the supply power is low. Therefore, operating company personnel do not have to manually reset the breakers on site.

There are eight fuses on the FSP connected to different areas of the SRU60 (refer to the table within this document).

Ringing generator

The FSP contains two ringing generators (NT7X92AA) which supply ringing voltages to POTS line cards.

Front panel controls and indicators

The front panel includes five circuit breakers (CB01-CB05), eight fuses (F01-F08), and the frame-fail LED. The circuit breakers can be operated manually or tripped by a problem in the associated power converter. The fuses have a mechanical indicator that is visible when a guard contact closes.

NT7X90AA (continued)

The circuit breakers and fuses are given in the following table, along with the associated functions and sizes.

CAUTION
Risk of service interruption and damage to equipment
Fuses F01, F04, and F05 must be removed before changing the following cards:

NTBX36 Bus Interface Card (BIC)

NTBX71 Point of Use Power Supply Card (PUPS)

Circuit breaker and fuse functions

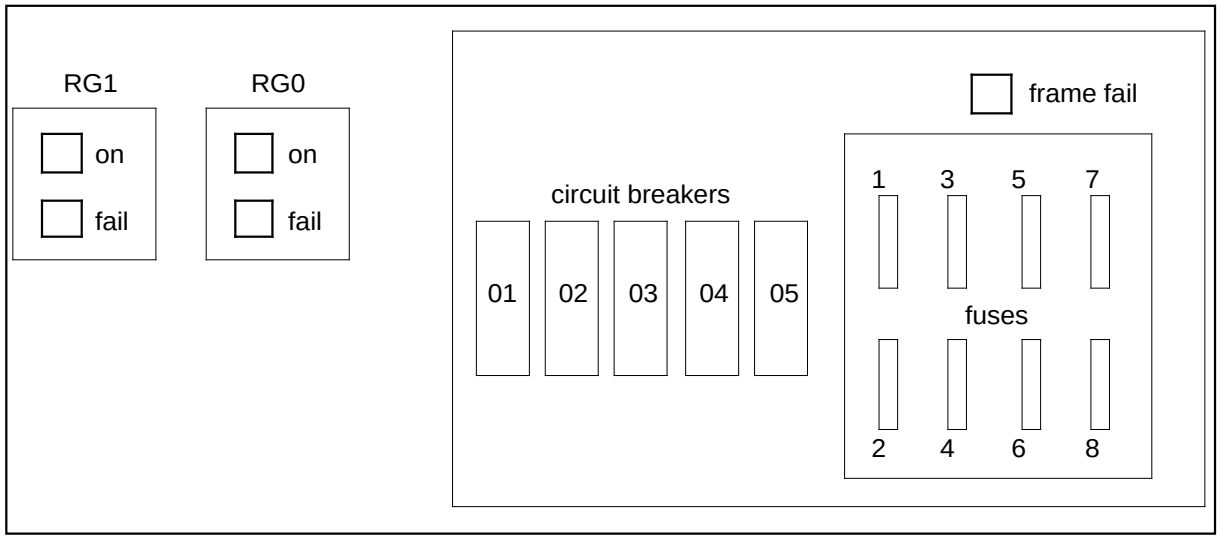
Designation	Function	Size
CB01	-48 V from PDC 0	20 A
CB02	-48 V from RG 0	10 A
CB03	-48 V from ABS	10 A
CB04	-48 V from PDC 1	20 A
CB05	–48 V from RG 1	10 A
F01	PUPS battery supply	1.3 A
F02	Ringing supply to line drawer	1.3 A
F03	Talk battery	1.3 A
F04	PUPS battery return	1.3 A
F05	15V to line cards	1.3 A
F06	Power-on lamps	1.3 A
F07	Frame fail	1.3 A
F08	Alarm control card	1.3 A

Note: See the warning at the beginning of the table.

Layout

The following figure shows the layout of the FSP.

NT7X90AA front view



Note: This illustration is not drawn to scale.

3 NT8Xnnaa

NT8X01AA through NT8X49AB

NT8X01AA

Production description

The NT8X01AA outside plant module (OPM) frame is a version of the remote line concentrating module (RLCM) frame (NT6X14AA). An environmentally controlled cabinet contains the OPM frame. The OPM frame is a self-contained switching center that supports a maximum of 640 analog lines. The NT8X01AA OPM frame includes the following:

- two-shelf line concentrating module (LCM)
- host interface equipment (HIE) shelf
- remote maintenance module (RMM) shelf
- frame supervisory panel (FSP) (NT6X25BB)
- two environmental control units (ECU)
- power equipment
- optional batteries for back-up power

The central side (C-side) of the OPM connects to a common peripheral controller (CPC) from two to six DS-1 links. The CPC can be a line group controller (LGC) or a line trunk controller (LTC). The CPC can be an LPG or a LTC at the host office or in a remote switching center (RSC). The CPC can instruct the OPM to link a subscriber line to one of the DS-1 channels. When the OPM links a subscriber line, incoming and outgoing calls can complete.

Optional fiber optic connections are available.

The OPM features a two-compartment cabinet. The main compartment contains main switching components. Main switching components include the LCM, the HIE shelf, and the RMM shelf. The main compartments also contains batteries and the environmental control equipment. The end-access compartment contains the protection, termination, and cross-connection equipment. This equipment is for voice frequency pairs and the DS-1 links to the host office or RSC.

Parts

The NT8X01AA contains the following parts:

- NT6X11AA-HIE shelf
- NT6X13AA-RMM
- NT6X25BB-FSP
- NT8X04AA-LCM

- NT8X05AA-Power control unit
- NT8X06AA-ECU

Host interface equipment shelf

The NT6X11AA host interface equipment shelf provides the interface between the DS30A links of the line concentrating array (LCA) and the DS-1 links of the CPC. The shelf provides the clock signal and ringing generators for the LCAs. The shelf provides the signals and generators for the messaging interface and data rate conversion. The interface and conversion is for the DS-1 line cards, the LCAs, and the RMM. The shelf also provides optional emergency stand-alone (ESA) call-processing functions if the communications links to the CPC fail. The ESA operation allows calls that originate and terminate on the same OPM to complete. The calls complete if the links to the host office are lost. The ESA operation supports the following:

- plain ordinary telephone service (POTS)
- local dialing plans for POTS and Meridian Digital Centrex (MDC)
- sequential hunt groups
- pulse and DTMF reception
- ringing types that the associated LCM supports
- ground and loop start lines
- revertive calling for non-business-set party lines
- 63 automatic lines
- a manual operator line

The ESA operation does not support following functions:

- attendant consoles
- vertical services
- local automatic message accounting (LAMA)
- centralized automatic message accounting (CAMA) billing
- recorded announcements
- coin-control functions
- maintenance and administration functions

The ESA operation supports some MDC services, like multiple centrex customer dialing plans. The ESA operation does not support most MDC services.

NT8X01AA (continued)

The shelf contains the following components:

- two or three NT6X50AA DS-1 interface circuit cards
- two NT6X73AA link control circuit cards (LCC-0 and LCC-1)
- two NT6X60AA ringing generators (RG-0 and RG-1) (NT6X60AA)
- two NT2X70AA power converters

If the ESA option is included, the shelf also contains the following:

- NT6X45AA ESA processor
- NT6X75AA ESA tone and clock card
- ESA memory card

Remote maintenance module

The NT6X13AA RMM shelf (NT6X13AA) is a modified version of the NT2X58 maintenance trunk module (MTM) shelf. The shelf provides maintenance and operational support for the OPM. The shelf supports the following components:

- metallic test access (MTA)
- incoming/outgoing test trunks
- line test units (LTUs)
- scan and signal distribution (SD) points
- Digitone receivers when the ESA option is included

The shelf contains the following components:

- an NT6X74AA control circuit card
- an NT2X59AA group coder-decoder (CODEC) and tone circuit card
- a pair of power converters (NT2X06AB and NT2X09AA)
- a maximum of 14 service circuit cards like the MTM. The specified application determines the types of cards used.

Some of the service cards used in the RMM are for MTA functions.

The RMM can reduce the amount of traffic on the DS-1 links. To reduce traffic, the RMM provides the LCM with access to test and service circuit cards at the remote site. The C-side interface of the RMM shelf connects to the two NT6X50AA DS-1 cards in the HIE shelf with DS30A links. The RMM connects the LCCs to make sure that the shelf remains operational. To remain operational, the shelf does not depend on which LCC is active. If the ESA

option is not included, a minimum of two OPMs at a remote site can share a single RMM. If the ESA option is included, each OPM must have a dedicated RMM. The RMM must include a Digitone receiver card.

The following procedures occur through the DS30A links to the LCM, and from the LCM to the host office:

- line circuit selection
- line circuit tests
- test result displays

Perform test procedures with the maintenance administration position (MAP) in accordance with the DMS-100 *Menu Commands Reference Manual*.

Frame supervisory panel

The NT6X25BB FSP provides the power control circuits that the power converters and ringing generators require. The power converters and ringing generators are in separate shelves. The FSP includes the following:

- frame-fail indicators
- fuse-fail alarm output
- front and rear alarm battery supply (ABS) test jacks
- four front-panel service jacks:
  - — two telephone pairs (TEL-A and TEL-B)
  - — two data pairs (DATA-A and DATA-B)
- two talk battery filters
- nine circuit breakers (CB1-CB9)
- eight fuses (F01-F08)
- three plug-in cards (CD1-CD3):
  - — an NT0X91AA alarm and converter drive circuit card
  - — an NT0X91AE converter drive protection circuit card
  - — an NT6X36AA alarm circuit card

The FSP monitors the condition of the power converters and ringing generators in the OPM shelves. The FSP monitors the input voltage. Two separate inputs are present: -48V (A) and -48V (B).

NT8X01AA (continued)

Line concentrating module

The NT8X04AA LCM provides the interface between the CPC and the analog lines. The module contains two single-shelf LCAs. These shelves are LCA-0 and LCA-1. The LCA-0 is on the bottom and LCA-1 is on the top. Each LCA includes a control complex. The control complex contains the NT6X51AB LCM processor and NT6X52AA digroup control cards. Each control complex can handle both LCAs in the following conditions:

- the control complex in the associated LCA fails
- a message link to the associated LCA fails
- the common peripheral controller forces an activity switch

Each LCA contains a maximum of five NT6X05AA LCM drawers. Each drawer contains an NT6X54AA bus interface card (BIC) and a maximum of 64 line circuit (LC) cards.

Each LCA includes a NT6X53AA power converter. The power converter provides the operating voltages for both of the LCAs in an LCM if the companion converter fails. The LCM incorporates loopback features in the digital path of each circuit card that can isolate single faults. Fuse and converter-failure alarm outputs are sent to the FSP.

Power control unit

The NT8X05AA power control unit contains ac power circuits and breakers for commercial power and emergency power. The power control unit includes two 25-A rectifiers that convert the ac input to -52V dc. When back-up batteries are in the OPM frame, the power control unit includes a battery charging unit (NT8X03AA). This unit controls battery charging and activates the back-up battery system if the ac power fails. The batteries are in strings in the rear of the OPM frame. Each string contains four 12V batteries.

Battery backup can maintain the operation of the OPM operating for maximum of 8 h.

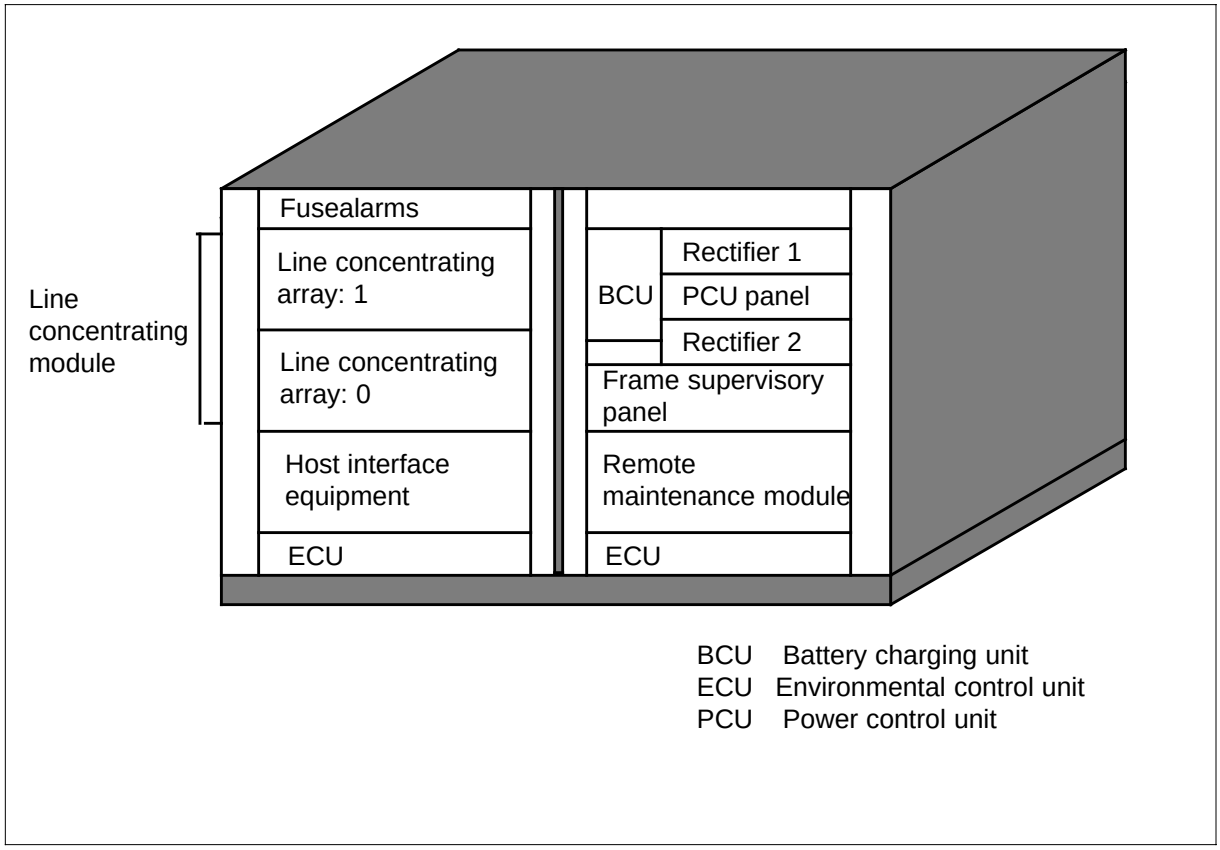
Environmental control units

The NT8X06AA environmental control units (ECUs) are at the bottom of each bay. The ECUs make sure that the environmental conditions in the main compartment remain in the operating range of the internal components. Environmental conditions include temperature and humidity. The ECUs contain the air inlets, air filters, fans, heaters, and air outlets required to maintain the correct operating conditions.

Design

The design of the OPM frame appears in the following figure.

OPM model 640-main compartment configuration



NT8X01BB

Product description

The NT8X01BB outside plant module (OPM) frame is a self-contained switching center that supports a maximum of 256 analog lines. The OPM includes the following parts:

- a single-shelf line concentrating module (LCM)
- an optional equipment shelf
- a host interface equipment (HIE) shelf
- a remote maintenance module (RMM) shelf
- a frame supervisory panel (FSP) (NT6X25BC)
- an optional equipment shelf
- two environmental control units (ECU)
- power equipment
- optional batteries for back-up power

The central side (C-side) of the OPM connects to a common peripheral controller (CPC) from two to six DS-1 links. The CPC can be a line group controller (LGC) or a line trunk controller (LTC). The LGC or LTC can be at the host office, or in a remote switching center (RSC). When the CPC instructs the OPM, the OPM links a subscriber line to a DS-1 channel. When the OPM links a subscriber line, incoming and outgoing calls can complete.

Optional fiber optic connections are available.

The optional equipment shelf can contain optional equipment packages. Housing optional equipment packages can increase the flexibility of the OPM.

The OPM features a two-compartment cabinet. The OPM contains the main compartment and the end-access compartment. The main compartment contains the main switching parts that follow.

- LCM
- HIE shelf
- optional equipment shelf
- RMM shelf
- batteries
- environmental control equipment

The end-access compartment contains the following:

- protection, termination and cross-connection equipment for voice frequency pairs
- DS-1 links to the host office or RSC

Parts

The NT8X01BB contains the following parts:

- NT6X11AA-HIE shelf
- NT6X13AA- RMM
- NT6X25BC-FSP
- NT8X04AA-LCM
- NT8X05AA-Power control unit
- NT8X06AA-Environmental control units
- Optional equipment shelf

Host interface equipment shelf

The NT6X11AA host interface equipment shelf provides an interface between the DS30A links of the LCM and the DS-1 links of the CPC. The shelf provides the clock signal and ringing generators for the LCM. The shelf provides messaging interface and data rate conversion for DS-1 line cards, the LCM and the RMM. The shelf provides optional emergency stand-alone (ESA) call-processing functions when the communications links to the CPC fail. The ESA operation allows calls that originate and terminate on the same OPM to complete. The ESA operation allows the calls to complete when the links to the host office are lost. The ESA operation supports the following services:

- plain ordinary telephone service (POTS)
- local dialing plans for POTS and Meridian Digital Centrex (MDC)
- sequential hunt groups
- pulse and DTMF reception
- ringing types that the associated LCM supports
- ground and loop start lines
- revertive calling for non-business-set party lines
- 63 automatic lines
- a manual operator line

NT8X01BB (continued)

The ESA operation does not support the following:

- attendant consoles
- vertical services
- local automatic message accounting (LAMA)
- centralized automatic message accounting (CAMA) billing
- recorded announcements
- coin-control functions
- maintenance functions
- administration functions

The ESA supports some MDC services, like multiple centrex customer dialing plans. The ESA does not support most MDC services.

The shelf contains the following:

- two or three NT6X50AA DS-1 interface circuit cards
- two NT6X73AA link control circuit cards (LCC-0 and LCC-1)
- two NT6X60AA ringing generators (RG-0 and RG-1) (NT6X60AA)
- two NT2X70AA power converters

When the ESA option is available, the shelf contains the following:

- NT6X45AA ESA processor
- NT6X75AA ESA tone and clock card
- ESA memory card

Remote maintenance module

The NT6X13AA RMM shelf is a modified version of the NT2X58 maintenance trunk module (MTM) shelf. The shelf provides maintenance and operational support for the OPM. The shelf supports the following functions:

- metallic test access (MTA)
- incoming/outgoing test trunks
- line test units (LTU)
- scan and signal distribution (SD) points
- when the ESA option is available, the shelf supports Digitone receivers

The shelf contains the following:

- an NT6X74AA control circuit card
- an NT2X59AA group coder-decoder (CODEC) and tone circuit card
- a pair of power converters (NT2X06AB and NT2X09AA)
- a maximum of 14 service circuit cards. The types of cards the system uses depends on the specific application. Some of the service cards in use in the RMM MTA are dedicated to MTA functions.

The RMM reduces the amount of traffic on the DS-1 links. The RMM gives the LCM access to test and service circuit cards at the remote site. The DS30 links connect the C-side interface of the RMM shelf to the two NT6X50AA DS-1 cards in the HIE shelf. When the RMM includes the ESA option, more than one OPM at a remote site can share an RMM. When the ESA option is available, each OPM must have a dedicated RMM. The RMM must include a Digitone receiver card.

The following test procedures are made through the DS30A links to the LCM, and from the LCM to the host office:

- select a line circuit
- test a line circuit
- display test results

Test procedures are performed with the MAP in accordance with the DMS-100 *Menu Commands Reference Manual*.

Frame supervisory panel

The NT6X25BC FSP provides the power control circuits that the power converters and ringing generators require. The power control circuits are in separate shelves. The FSP includes the following:

- frame-fail indicators
- fuse-fail alarm output
- front and rear alarm battery supply (ABS) test jacks
- four front-panel service jacks
  - — two telephone pairs (TEL-A and TEL-B)
  - — two data pairs (DATA-A and DATA-B)
- two talk battery filters
- nine circuit breakers (CB1-CB9)

NT8X01BB (continued)

- eight fuses (F01-F08)
- three plug-in cards (CD1-CD3)
  - — an NT0X91AA alarm and converter drive circuit card
  - — an NT0X91AE converter drive protection circuit card
  - — an NT6X36AA alarm circuit card

The FSP monitors the condition of the power converters and ringing generators in the OPM shelves, and monitors the input voltage. Two separate inputs are present: -48V (A) and -48V (B).

Line concentrating module

The NT8X04BA LCM provides the interface between the CPC and the analog lines. The single-shelf line module includes a control complex that contains the following:

- NT6X51AB LCM processor
- NT6X52AA digroup control cards
- four NT6X05AA LCM drawers

Each drawer contains an NT6X54AA bus interface card (BIC) and a maximum of 64 line circuit (LC) cards.

The LCM includes an NT6X53AA power converter that provides the voltages for the LCM circuits. The LCM incorporates loopback features in the digital path of each circuit card that can isolate single faults. Fuse and converter-failure alarm outputs are sent to the FSP.

Power control unit

The NT8X05AA power control unit contains ac power circuits and breakers for commercial power and emergency power. The power control unit includes two 25-A rectifiers that convert the ac input to -52V dc. When the OPM frame has back-up batteries, the power control unit also includes a battery charging unit (NT8X03AA). The battery charging unit controls battery charging and activates the back-up battery system when the ac power fails. The batteries are in strings to the rear of the OPM frame. Each string contains four 12-V batteries.

Battery backup can keep the OPM in operation for a maximum of 8 h.

Environmental control units

The NT8X06AA environmental control units are at the bottom of each bay. The ECUs contain the air inlets, air filters, fans, heaters and air outlets required for environmental control.

Optional equipment shelf

The optional equipment shelf expands the flexibility of the OPM frame. The optional equipment shelf can contain the following:

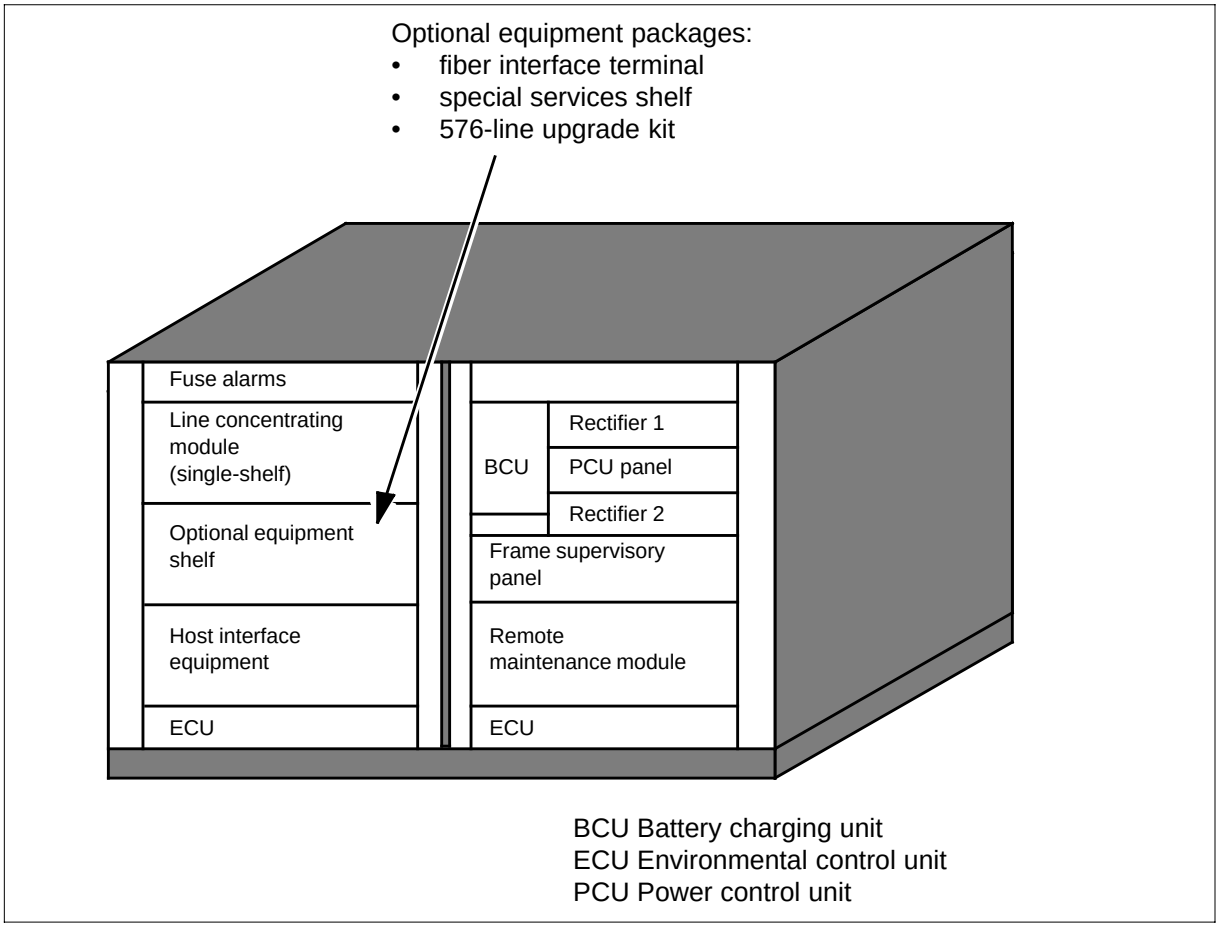
- a fiber optic terminal
- a special services shelf for applications like foreign exchange service and off-premises extensions
- a 576-line upgrade kit, which adds 320 lines to the 256 lines present and allows the OPM to meet expanding service needs

Design

The design of the OPM frame appears in the following figure

NT8X01BB (end)

OPM model 256-main compartment configuration



NT8X02AB

Product description

The NT8X02AB battery charging controller card controls and monitors power levels.

Location

The NT8X02AB fits in slots 01 and 03 in the NT8X03BC shelf, in the NT8X01AA, AB, AC, BA, BB and BC frames.

Functional description

The NT8X02AB provides the following functions:

- controls battery strings
- monitors outputs that relate to the string voltage and that relate to the discharge current
- monitors load resistors for test discharges
- monitors the power converter for subsequent charging

The NT8X02AB operates in the following sequence with each battery string, one at a time:

1. disconnects the battery string from the bus
2. holds the battery string on an open circuit
3. applies a test discharge to the battery string
4. charges the battery string
5. holds the battery string on an open circuit again
6. connects the battery string to the bus again

The -52.5V frame load bus powers the . The does not provide the primary power feed to that bus. The NT8X02AB does not control the primary power feed to that bus. The batteries or the rectifiers provide the power.

Functional blocks

The NT8X02AB has the following functional blocks:

- test discharge duration
- bus voltage tolerance
- short circuits and the power ON/OFF switch
- intended sequence of battery charging
- monitoring outputs

NT8X02AB (continued)

- incoming signals
- charge converter
- alarms and fusing

Test discharge duration

The NT8X02AB dissipates the heat that a test discharge produces. The discharge lasts 1 h, and occurs each week. When you increase the frequency of this activity, the life of the circuit card can shorten.

Bus voltage tolerance

The NT8X02AB monitors incoming charges. A charge command must be stopped or not issued when the frame load bus set point is more than the -52.5V, ± 1 % tolerance. The charge command is from the OPMPES MAP menu.

Short circuits and the power ON/OFF switch

The current-limiting circuits of the deal with a maximum of two shorted cells. The power ON/OFF switch is for safety when you insert the card into the backplane connector.

When a charge command combines with a short circuit, damage to occurs. Damage occurs when the switch is ON or OFF. Damage occurs in tens of seconds.

Intended sequence of battery charging

Incoming signals control the sequence of events involved in battery charging. The following is an example of an intended, or normal sequence.

- Each string is on the charge bus for 7 h, one time a week.
- After charging completes, the battery string is open circuited for a minimum of 4 h. The time lapse allows the voltage to decrease toward the voltage open circuit value. This event occurs before the string is back on the load bus.

One battery string goes through an open circuit, discharge and charge test each week.

Monitoring outputs

The NT8X02AB has five monitoring outputs. Four outputs, VPTS0 through VPTS3, provide voltages calculated from the battery strings designated 0 through 3. The fifth monitoring output, VPTTC, provides a voltage calculated from the test discharge current, with 1V that corresponds to 1A.

The NT8X02AB has five test points. The BATRND is battery return, and the other four test points, BATSTJ0 through BATSTJ3, are calculated from each associated battery string voltage.

The NT8X02AB has 12 signal input points, three for each of the battery strings. Each point drains less than 10 mA. The two states are rail voltage (-42 V to -56 V), and are open circuit or battery return.

Charge converter

The -52.5V bus powers the charge converter. The converter output voltage is normally more negative than the output voltage of the bus. The converter output voltage is approximately -57.5 V on no load, and toward the end of a normal charge. The normal initial output current is a maximum of 3A. The state of the battery string that the system charges is a factor. The charge converter cannot adjust output voltage more than a fraction positive to the -52.5V bus. The connecting circuits provisions for dealing with an overdischarged string, or with a string that has shorted cells.

Alarms and fusing

A Fail light-emitting diode (LED) on the front face of the lights during failure modes of the charge converter.

The faceplate contains six fuses:

- one on each of the four battery string circuits
- one on the output of the charge converter
- one on the power feed for the remaining circuits

The alarm contacts for the fuses connect so that any blown fuse activates the card alarm.

The four battery fuses protect the pack parts from damage when a part failure or short occurs on the battery string connections.

The other two fuses protect the card from damage when a part failure or an excessive current draw on the charge converter output occurs.

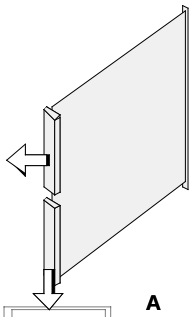
Signaling

Pin numbers

The pin numbers for the NT8X02AB appear in the following figure.

NT8X02AB (end)

The NT8X02AB pin numbers



	A	B
1A 1B	BatFeed	
2A 2B		
3A 3B	-52.5VBR	RFA0
4A 4B	RFA3	RFA0
5A 5B	VSTR3	VSTR3
6A 6B	52.5V	52.5V
7A 7B	52.5V	52.5V
8A 8B	52.5V	52.5V
9A 9B	52.5V	52.5V
10A 10B	52.5V	52.5V
11A 11B	52.5V	52.5V
12A 12B	52.5V	52.5V
13A 13B	52.5V	52.5V
14A 14B	52.5V	52.5V
15A 15B	52.5V	52.5V
16A 16B		
17A 17B		
18A 18B	BATSTR3	BATSTR3
19A 19B	BATSTR3	BATSTR3
20A 20B	BATSTR3	BATSTR3
21A 21B	BATSTR3	BATSTR3
22A 22B	BATSTR3	BATSTR3
23A 23B	BATSTR3	BATSTR3
24A 24B	CSWL3	CSWL3
25A 25B	CSWC3	CSWC3
26A 26B	CSWTL3	CSWTL3
27A 27B	BCFA	BCFA
28A 28B	VSTRA	VSTRA
29A 29B	BATSTR2	BATSTR2
30A 30B	BATSTR2	BATSTR2
31A 31B	BATSTR2	BATSTR2
32A 32B	BATSTR2	BATSTR2
33A 33B	BATSTR2	BATSTR2
34A 34B	-52.5VBR	-52.5VBR
35A 35B	-52.5VBR	-52.5VBR
36A 36B	-52.5VBR	-52.5VBR
37A 37B	-52.5VBR	-52.5VBR
38A 38B	-52.5VBR	-52.5VBR
39A 39B	-52.5VBR	-52.5VBR
40A 40B	-52.5VBR	-52.5VBR

	A	B
41A 41B	-52.5VBR	-52.5VBR
42A 42B	-52.5VBR	-52.5VBR
43A 43B	-52.5VBR	-52.5VBR
44A 44B	-52.5VBR	-52.5VBR
45A 45B		
46A 46B	CSWL2	CSWL2
47A 47B	CSWC2	CSWC2
48A 48B	CSWTL2	CSWTL2
49A 49B		
50A 50B		
51A 51B		
52A 52B		
53A 53B	VSTR1	VSTR1
54A 54B		
55A 55B	BATSTR1	BATSTR1
56A 56B	BATSTR1	BATSTR1
57A 57B	BATSTR1	BATSTR1
58A 58B	BATSTR1	BATSTR1
59A 59B	BATSTR1	BATSTR1
60A 60B		
61A 61B	CSWL1	CSWL1
62A 62B	CSWC1	CSWC1
63A 63B	CSWT1	CSWT1
64A 64B		
65A 65B	VSTR0	VSTR0
66A 66B		
67A 67B		
68A 68B		
69A 69B		
70A 70B		
71A 71B	BATSR0	BATSR0
72A 72B	BATSR0	BATSR0
73A 73B	BATSR0	BATSR0
74A 74B	BATSR0	BATSR0
75A 75B	BATSR0	BATSR0
76A 76B		
77A 77B		
78A 78B	CSWL0	CSWL0
79A 79B	CSWC0	CSWC0
80A 80B	CSWTL0	CSWTL0

NT8X04AA

Product description

The line concentrating module (LCM) is a two-shelf component in the NT8X01AA 640-line outside plant module (OPM) frame. The NT8X040AA functions as an interface between a common peripheral controller (CPC) and a maximum of 640 analog lines. The connections depend on the distance between the LCM and associated CPC. If the LCM is less than 15 m (50 ft) from the CPC, the NT8X040AA uses DS30A links. The NT8X040AA uses DS-1 links for distances to a maximum of 241 km (150 mi). An example of an LCM and the associated CPC is a line group controller or line trunk controller.

The LCM has two single-shelf line concentrating arrays (LCA). The LCAs are LCA-0 and LCA-1. The LCA-0 is on the bottom. The LCA-1 is on the top. Each LCA includes a control complex. The control complex contains the NT6X51AB LCM processor and NT6X52AA digroup control cards. The control complex can handle both LCAs if any of the following conditions occur:

- an LCM processor or digroup control card in the associated LCA fails
- a message link to the associated LCA fails
- the common peripheral controller forces an activity switch

Each LCA contains a maximum of five NT6X05AA LCM drawers. Each drawer contains an NT6X54AA bus interface card (BIC) and a maximum of 64 line circuit (LC) cards.

Each LCA has an NT6X53AA power converter. This power converter can provide the required operating voltages for the LCAs in an LCM. The power converter provides these voltages if the other converter of the LCM fails. The control complex has the same feature.

The LCM uses looparound features in the digital path of each circuit card to isolate single faults. Fuse and converter-failure alarm outputs also go to the frame supervisory panel (FSP).

Parts

Each LCA in an LCM contains the following parts:

- an NT6X05AA-LCM drawers
- an NT6X51AB-LCM processor card
- an NT6X52AA-digroup control card
- an NT6X53AA-power converter

NT8X04AA (continued)

Design

The design of the NT8X04AA appears in the following table.

NT8X04AA parts (Sheet 1 of 2)

Product engineering code (PEC)	Slot	Description
NT6X05AA	6F-20F	*Line drawer* The line drawer provides signaling and voice interfaces between 64 two-wire LC and the two LCA control complexes in an LCM. The drawer also controls the application of ringing signals to the LC cards. Each LCA has a maximum of five line drawers. Each line drawer contains an NT6X54AA BIC and a maximum of 64 line cards. The BIC is behind the front panel of the line drawer. The line cards occupy four rows behind the BIC. The NT6X05AA line drawer can have the following line cards: • NT6X17AA - standard line card type A • NT6X18AA- standard line card type B without +48 V • NT6X18AB - standard line card type B with +48 V • NT6X21AA - standard line card type C • NT6X23AA - power converter(+48 V) • NT6X71AA - standard line card type D
NT6X51AA	4F	*Line concentrating module processor* The LCM processor controls the activity of the LCA. The LCM processor functions as the interface between the DS30A links and the digroup controller. The LCM performs the following functions: • sanity checks • digit collection and messaging for a maximum of 640 lines • monitoring of power and ringing functions • recovery and generation of clock signals • the DMSX message protocol for the line group controller (LGC)

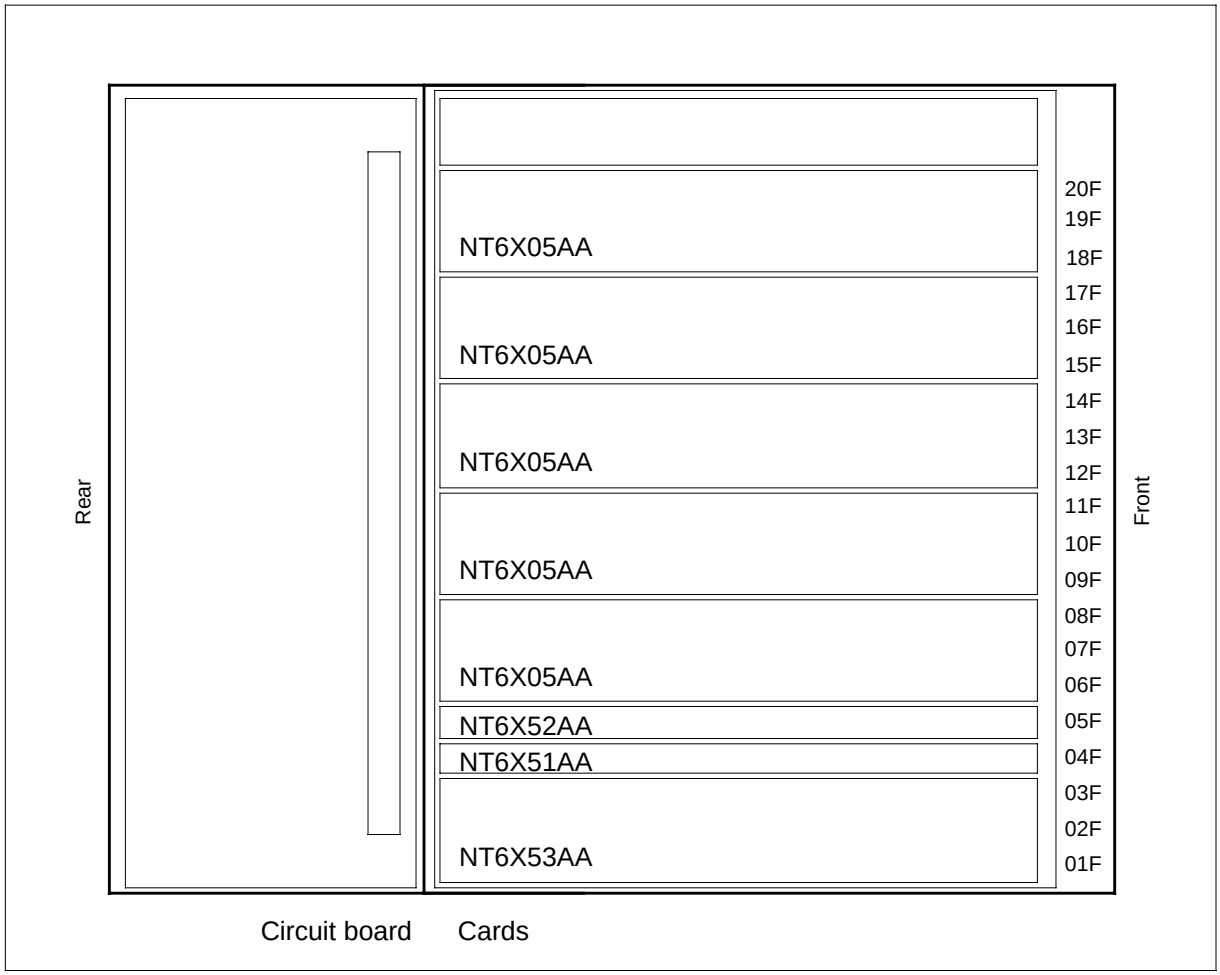
NT8X04AA parts (Sheet 2 of 2)

Product engineering code (PEC)	Slot	Description
NT6X52AA	5F	*Digroup controller* The digroup controller functions as an interface for a maximum of three DS30A links and a maximum of ten LCM drawers. The digroup controller supplies time switching for both external and internal channel assignments. The digroup controller provides the digital looparound paths for troubleshooting.
NT6X53AA	1F-3F	*Power converter* The power converter supplies the +5V and +15V dc that the LCA circuits require. The power converter includes relay circuits that apply the ringing, automatic number identification (ANI), and coin voltages to the LCs in the line drawer. The ringing generators in the FSP generate the coin voltages. Each power converter functions as a backup for the converter in the associated LCA.

The design of the NT8X04AA appears in the following figure.

NT8X04AA (end)

The NT8X04AA parts



NT8X04BA

Product description

The NT8X01BA line concentrating module (LCM) is a single-shelf component in the NT8X01BA 256-line outside plant module (OPM) frame. The NT8X04BA functions as an interface between a common peripheral controller (CPC) and a maximum of 256 analog lines. The connections between the LCM and associated CPC depend on the distance between the LCM and the CPC. The CPC can be a line group controller or line trunk controller. The NT8X04BA uses DS30A links if the LCM is less than 15 m (50 ft) from the CPC. The NT8X04BA uses DS-1 links for distances to a maximum of 241 km (150 mi). An example of the associated CPC is a line group controller or line trunk controller.

The LCM is a single-shelf unit that includes a control complex. The control complex contains the NT6X51AA LCM processor and NT6X52AA digroup control cards. The control complex contains a maximum of four LCM drawers (NT6X05AA). Each drawer contains an NT6X54AA bus interface card (BIC) and a maximum of 64 line circuit (LC) cards.

The shelf includes an NT6X53AA power converter that provides the required operating voltages for the LCM circuits. The shelf also uses loopback features in the digital path of each circuit card to isolate single faults. Fuse and converter-failure alarm outputs also go to the frame supervisory panel (FSP).

Parts

The LCM has the following parts:

- an NT6X05AA - LCM line drawers
- an NT6X51AB - LCM processor card
- an NT6X52AA - digroup control card
- an NT6X53AA - power converter

NT8X04BA (continued)

Design

The design of the NT8X04BA appears in the following table.

NT8X04BA parts (Sheet 1 of 2)

Product engineering code (PEC)	Slot	Description
NT6X05AA	6F-20F	*Line drawer* The line drawer provides signaling and voice interfaces between 64 two-wire LC and the two LCA control complexes in an LCM. The drawer controls the application of ringing signals to the LC cards. Each LCA has a maximum of five line drawers. Each line drawer contains an NT6X54AA BIC and a maximum of 64 line cards. The BIC is behind the front panel of the line drawer. The line cards occupy four rows behind the BIC. The NT6X05AA line drawer can have the following line cards: • NT6X17AA - standard line card type A • NT6X18AA - standard line card type B without +48 V • NT6X18AB - standard line card type B with +48 V • NT6X21AA - standard line card type C • NT6X23AA - power converter(+48 V) • NT6X71AA - standard line card type D
NT6X51AA	4F	*Line concentrating module processor* The LCM processor controls the activity of the LCA and functions as the interface between the DS30A links and the digroup controller. The LCM processor performs the following functions: • sanity checks • digits collection and messaging for a maximum of 640 lines • monitoring of power and ringing functions • recovery and generation of clock signals • the DMSX message protocol for the line group controller (LGC)

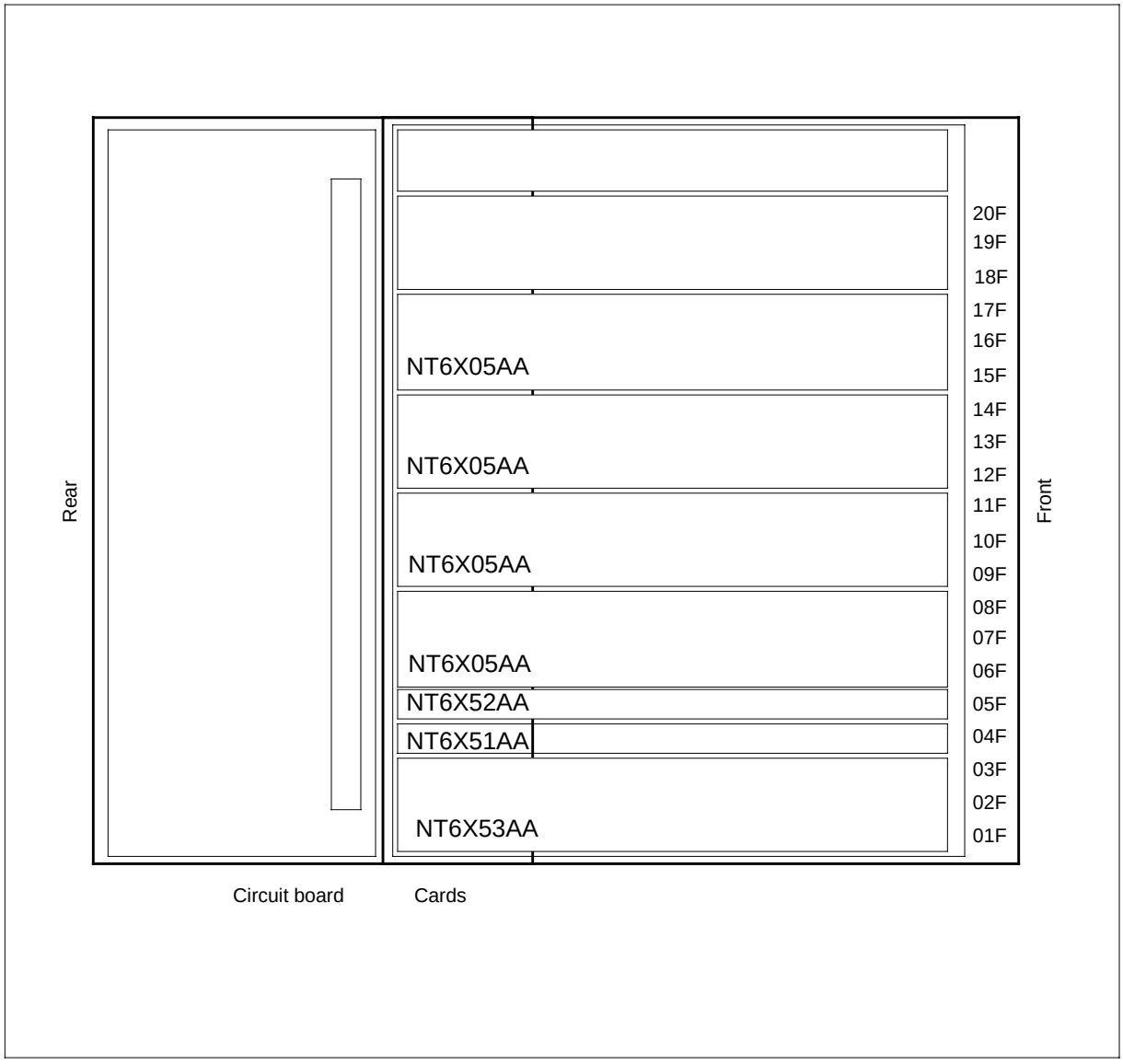
NT8X04BA parts (Sheet 2 of 2)

Product engineering code (PEC)	Slot	Description
NT6X52AA	5F	*Digroup controller* The digroup controller functions as an interface for a maximum of three DS30A links and a maximum of ten LCM drawers. The digroup controller supplies time switching for external and internal channel assignments and provides the digital looparound paths for troubleshooting.
NT6X53AA	1F-3F	*Power converter* The power converter supplies the +5V and +15V dc that the LCA circuits require. The power converter also includes relay circuits that apply the ringing, automatic number identification (ANI), and coin voltages to the LCs in the line drawer. The ringing generators in the FSP generate the coin voltages. Each power converter functions as a backup for the converter in the associated LCA.

The design of the NT8X04BA appears in the following figure.

NT8X04BA (end)

The NT8X04BA parts



NT8X05AA

Product description

The NT8X05AA power control unit is for commercial and emergency power in the following:

- international outside plant module (IOPM) frames
- outside plant module (OPM) frames

The power control unit contains ac power circuits and breakers for commercial and emergency power. The unit includes two 25-A rectifiers that convert the ac input to -52V dc. When the frames (OPM or IOPM) include backup batteries, the power control unit also includes a battery charging. The unit activates the backup battery system if the ac power fails. The batteries are in strings in the rear of the frame. Each string contains four 12-V batteries.

Battery backup can maintain the operation of the OPM for a maximum of 8 h.

Parts

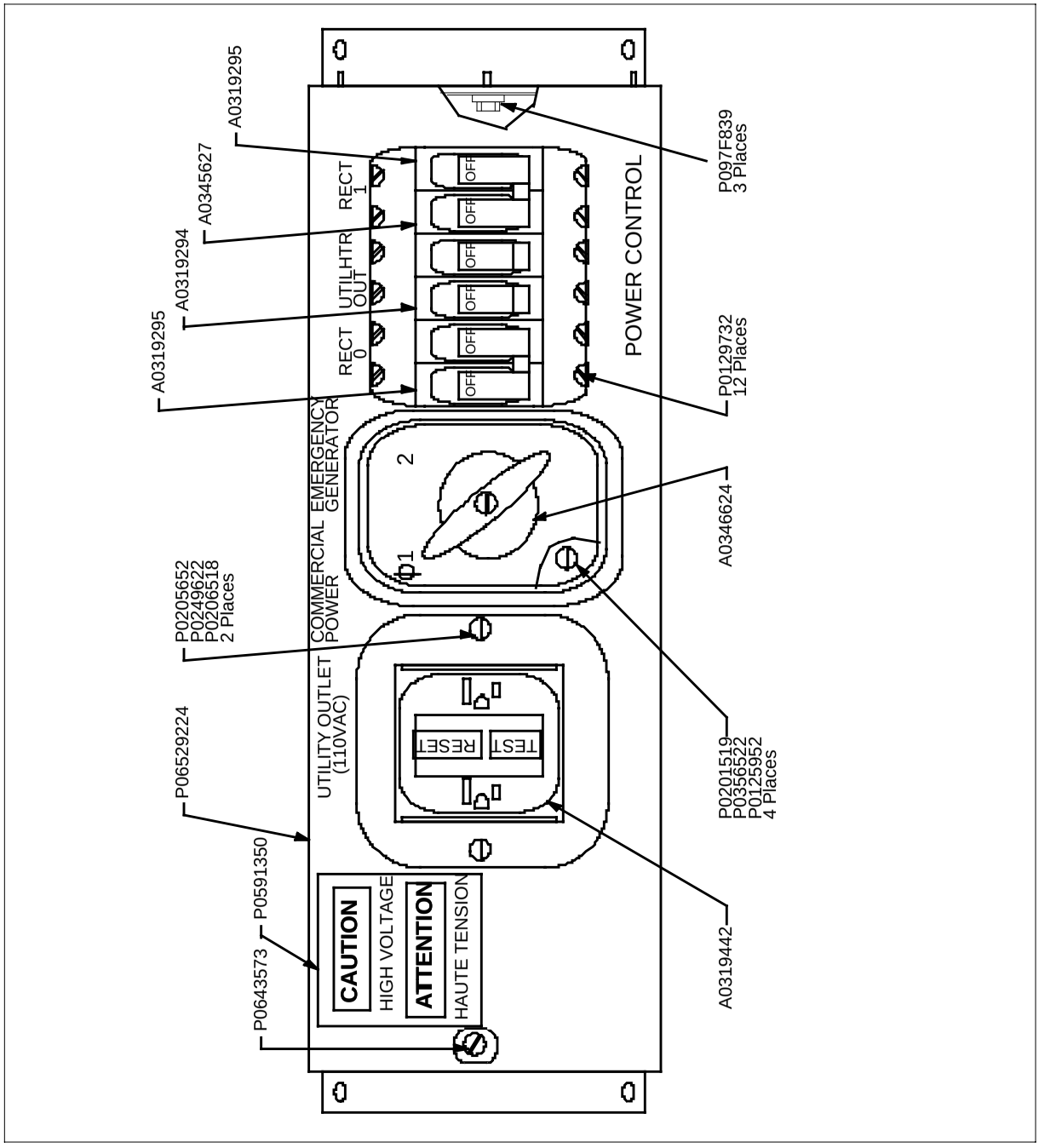
There are no attachments or parts for the power control unit.

Design

The design of the power control unit appears in the following figure.

NT8X05AA (end)

NT8X05AA Power control unit parts



NT8X06AB

Product description

The NT8X06AB environmental control unit (ECU) is part of the environmental control equipment. The outside plant module (OPM) frames or the international outside plant module (IOPM) frames use the ECU.

The frames also contain the following:

- booster fan unit (BFU)
- cabinet insulation
- incoming air filters and diffusers
- incoming air dampers
- thermostats and temperature sensors

The frames require two ECUs. One ECU is at the bottom of each bay in the frame.

The ECU makes sure that the environmental conditions in the main compartment remain in the operating range of the internal components. Environmental conditions include temperature and humidity. This unit contains air inlets, air filters, fans, heaters, and air outlets. The ECU requires these parts to maintain the correct conditions for operation.

Parts

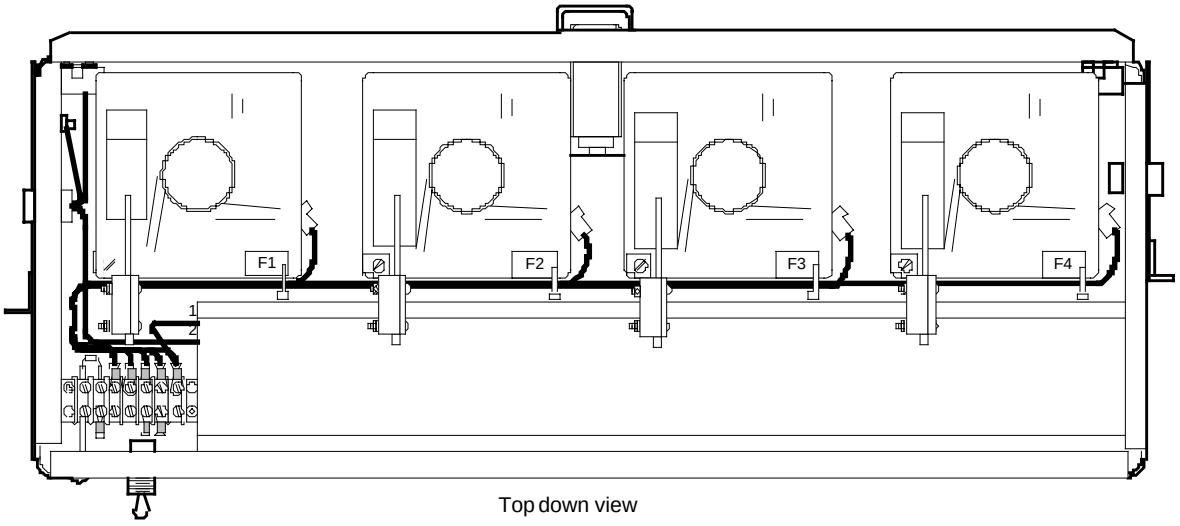
There are no important parts for NT8X06AB.

Design

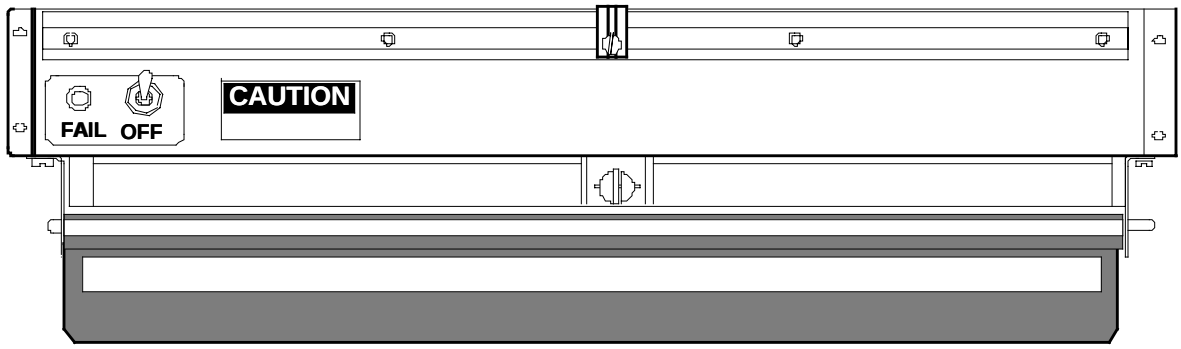
The design of NT8X06AB appears in the following figure.

NT8X06AB (end)

NT8X06AB parts



Top down view



Front view

NT8X06BA

Description

The NT8X06BA booster fan unit (BFU) is above line concentrating array (LCA) 1 in bay 0 of the NT8X06BA international outside plant module (IOPM) frame. The BFU and two environmental control units (ECU) are part of the environmental control equipment in the IOPM frame. This unit contains three circulation fans and a fan alarm card (FAC). The FAC activates an alarm if the fans fail.

Parts

The BFU contains three circulation fans and a FAC.

Circulation fans

The circulation fans provide an even distribution of cooling air. The fans also make sure that air flow is even and reduce possible short–circuit air flow.

Fan alarm card

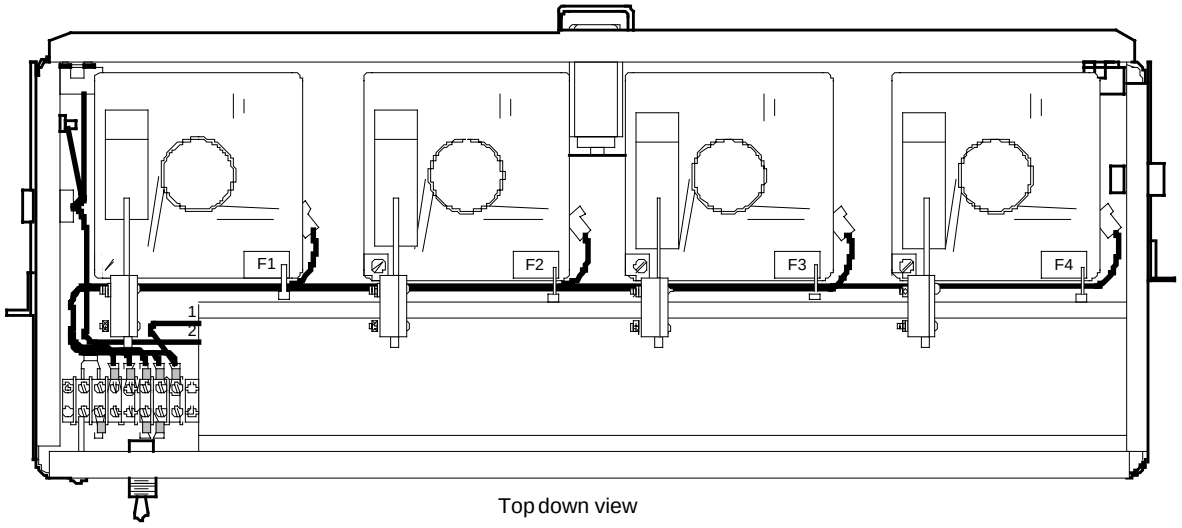
The FAC activates an alarm if the fans fail.

Design

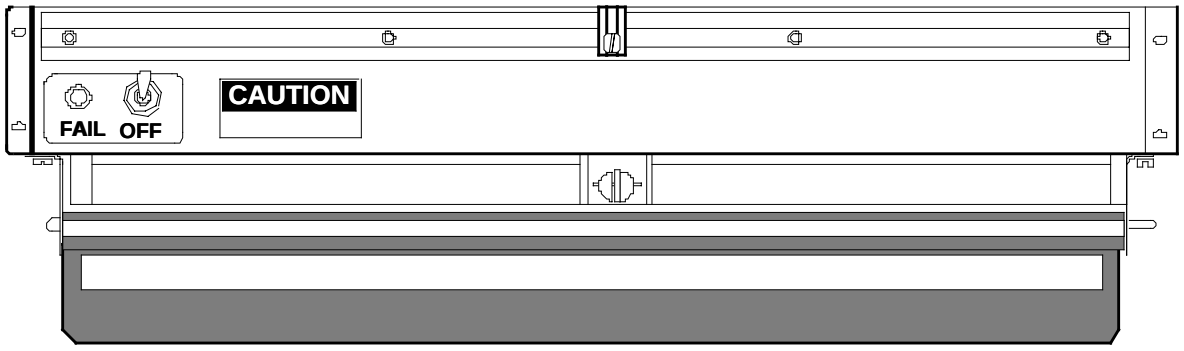
The design of the NT8X06BA appears in the following figure.

NT8X06BA (end)

NT8X06BA parts



Top down view



Front view

NT8X10AA

Product description

The NT8X10AA double-shelf network equipment (DSNE) frame is a single bay equipped with one or two networks. One network is available for each plane. The upper pair of shelves is Plane 00 and the lower pair is Plane 01.

The DSNE functions as an interface between the maintenance trunk module (MTM) shelves to the dual-plane combined core (DPCC).

Each network unit or module contains one clock circuit pack (CP) (NT3X76AC) and one network central processor CP (NT3X74BB).

The DSNE and a trunk module equipment (TME) frame form the office alarm system. The office alarm system is a part of the switching network.

Parts

The NT8X10AA has the following parts:

- an NT0X28AK-frame supervisory panel (FSP)
- an NT3X90AC-device controller (DC) fan cooling unit
- an NT8X11AB-double-shelf network assembly
- a P0575239-filler panel, present if only one network is set up

Frame supervisory panel

The NT0X28AK FSP contains power control and alarm circuits. These circuits monitor the power supply to the DSNE frame from the power distribution center (PDC) in the digital switching system.

The NT0X28AK FSP transmits the necessary potential from the office battery through four power feeds. The nominal voltage is -48 V. The NT0X28AK FSP uses four circuit breakers. The circuit breakers protect the power control and alarm circuits to the shelves in the DSNE frame. This model is different from other NT0X28 models. Some NT0X28 models use fuses to protect the power control, and some models require two or three power feeds.

The NT0X28AK has a mechanical interlock feature. This feature consists of a small cover that slides. This cover allows access to only two of the circuit breakers at a time. For example, the cover allows access to CB1 and CB2 or to CB4 and CB5. All four circuit breakers can be ON at the start. In this condition, the user cannot trip the breakers in both groups at the same time by accident.

NT8X10AA (continued)

Filler panel

The filler panel requires two shelf positions in the DSNE frame that are not used. Double-shelf network assemblies use these shelf positions when only one network is set up.

DC fan cooling unit

The NT3X90AC cooling unit contains five-fan assemblies that maintain a normal five-shelf cabinet. Two feeders in the PDC, each fused at 5 A, power the fans at 48V dc.

Two NT3X90AC units cool the NT3X45EW double bay frame. The units cool at a thermal stress equivalent (TSE) equal to the static bulk ambient temperature (50°C maximum). The heat distribution is to a maximum of 1200 W.

The NT3X90AC cooling unit uses a single-fan failure detection and signaling system. The multiple-fan design contains some redundancy. The redundancy allows for a single-fan failure without critical loss of cooling air.

Double-shelf network assembly

Two or four NT8X11AB double-shelf network assembly shelves are present in the NT8X10AA DSNE frame. Two shelves are available for each plane. These shelves perform the function of the NT8X10AA. The double-shelf network assemblies function as an interface between MTM shelves to the central control (CC).

Each NT8X11AB double-shelf network assembly shelf contains four types of circuit cards:

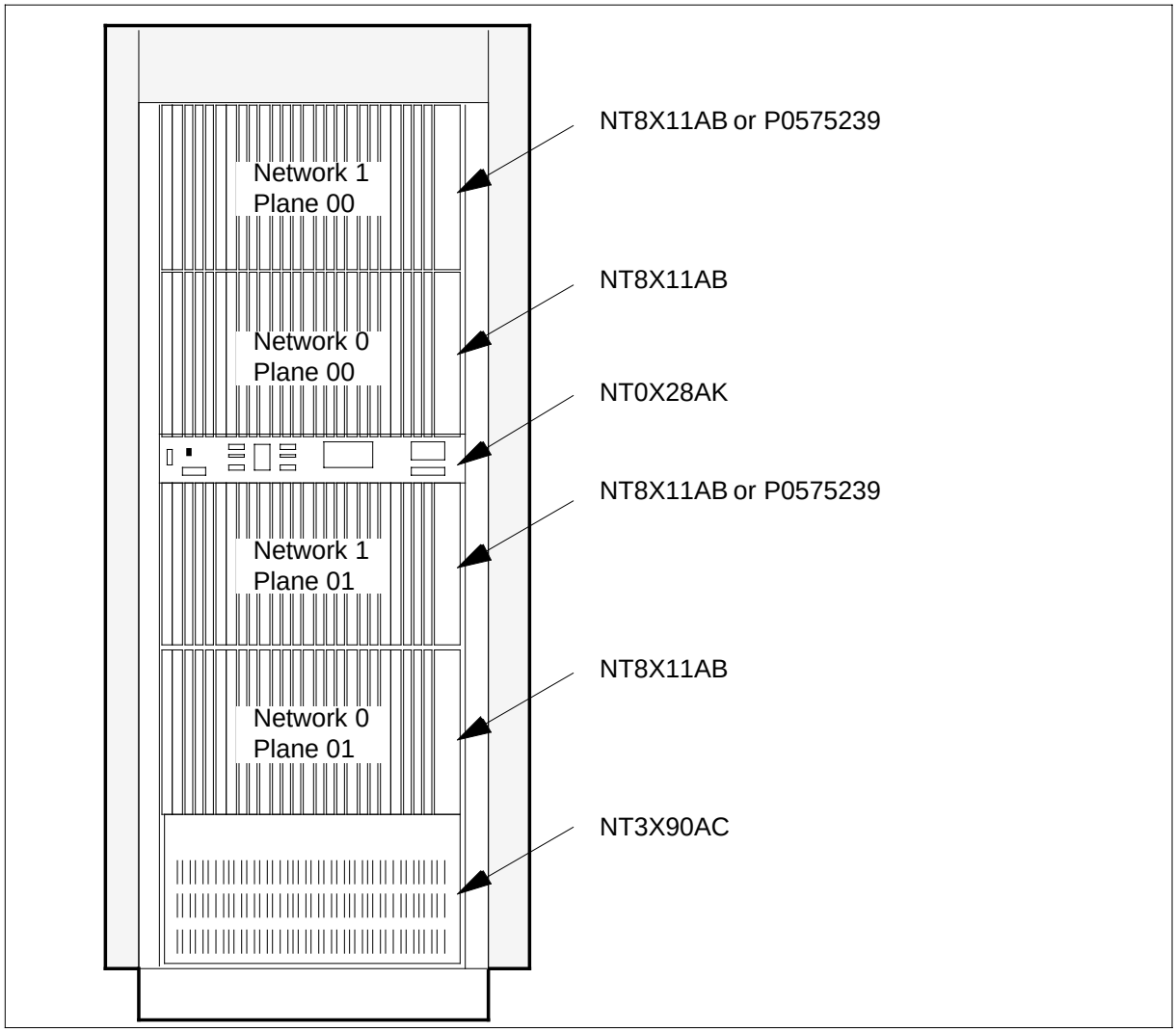
- the NT3X74BB-network control processor card
- the NT3X75BA-network peripheral side (P-side) message processor card
- the NT3X76AC-network clock CP
- the NT8X11AC-network common CPs

Design

The design of the NT8X10AA appears in the following figure.

NT8X10AA (end)

NT8X10AA parts



NT8X11AB

Description

As a network module (NM), the NT8X11AB NM establishes and maintains two-way, four-wire speech and signaling paths. The signaling paths are between the NT8X11AB NM and the peripheral modules (PM) for the duration of a call.

The NT8X11AB NM mounts with the card pair NM in an NT8X10AA double-shelf network equipment frame (DSNE). There is one NM for each plane. Two pairs can mount in a single DSNE, one pair for each network.

The NT8X11AB NM is different from other NMs: NT0X48, NT5X13, NT7X27 and NT7X40 for the following reasons:

- Parallel junctors occur in groups of 16 ports, and the backplane requires special cabling.
- Both serial-to-parallel and parallel-to-serial conversions occur in the NT8X12AA network port interface card.
- The NT8X11AB does not have interswitch link buses. Each of the two crosspoint cards get 2048 channels in the data memory (DM), and 1024 outgoing channels can be switched.
- The NT8X11AB handles time switching with a different method than other NMs. Normally, each side of an NM has pairs of digital crosspoint time switches (TS). The pair includes one incoming (IC) and one outgoing digital crosspoint TSs. The NT8X11AB NM has one TS pair.
- The NT8X11AB shelf uses parallel intra-junctors and serial inter-junctors. The peripheral side (P-side) and junctor side use the same port card.
- The NT8X11AB has four interface cards at 16 ports for each card. A total of 64 ports on each shelf is the result.

Parts

There are one or two pairs of NT8X11AB double-shelf network assembly shelves (modules) in the NT8X10AA DSNE frame. One pair is present for each network.

The NT8X11AB contains the following parts:

- NT0X50AA-Filler faceplate
- NT2X70AB-Power converter, ±5V
- NT3X74BA-Network control processor card
- NT3X75BA-Network P-side message processor card

- NT3X76BA-Network clock card
- NT8X12AA-Network interface (NI) card
- NT8X13AA-Crosspoint (XPT) card
- NT8X14AA-Test code cards

Design

Descriptions of the parts of the NT8X11AB shelf appear in the following table.

NT8X11AB (Sheet 1 of 5)

PEC	Slot	Description
NT0X50AA	18F, 20F, 22F, 24F	*Filler faceplate .875* The NT0X50AA fills circuit pack (CP) slots in the NT8X11AB shelf that are not in use.
NT2X70AB	25F	*Power converter, ±5 V* The NT2X70AB uses a -48V input from the office battery to provide a regulated electrical potential of ±5 V to the NT8X11AB shelf.
NT3X74BA	21F	*Network control processor card* The NT3X74BA NCP performs the following operations: • handles messages from the central message controller (CMC) or the computing module • performs central side (C-side) processor function controls the network switching • inserts or extracts test code (TC) in response to the central control (CC) or the computing module • provides the message buffer for the P-side processor when the PM communicates with the CC or the computing module

NT8X11AB (continued)

NT8X11AB (Sheet 2 of 5)

PEC	Slot	Description
NT3X75BA	19F	*Network P-side message processor card* The NT3X75BA handles message exchanges between an NM and the PM. The P-side of the processor connects across the four parallel buses. The four parallel buses are between the formatters and the XPT cards. The XPT cards are on the A-side and B-side of the peripheral faces. Messages from a PM are extracted at the output of the SP formatter. Messages to a PM are inserted at the input to the PS formatter. The processor can access the channel-zeroes that go to and come from the PM. This PEC can handle four message transactions that occur at the same time. Each parallel bus handles one message transaction. On the network side of the processor, the processor can access a message buffer on the NCP card. Messages that the processor receives from peripherals are deposited in this buffer. The NCP relays the messages to the CC or the computing module. The P-side processor scans this message buffer for outgoing messages. Outgoing messages are sent to the PM specified in the messages headers.
NT3X76BA	23F	*Network clock card* The NT3X76BA contains a circuit that generates a 10.24-MHz clock pulse and a frame pulse (125 ms). The clock circuit synchronizes with the frame pulse. The incoming data from the CMC or the computing module (CM) provides the frame pulse. The clock and frame pulses control timing in the NMs. The clock and frame pulses use interface cards to control timing to the PMs.
NT8X12AA	1F-4F, 14F-17F	*Network interface card* The NT8X12AA provides 16 bi-directional, 2.56-Mbps port interfaces for the DS30 design of NMs or PMs. The NT8X12AA provides the serial-to-parallel and parallel-to-serial formatter functions to interface with the NT8X13AA crosspoint card.

NT8X11AB (Sheet 3 of 5)

PEC	Slot	Description
		Each card has a W87 chip for the DS30 conversion and a W72 chip for the serial-to-parallel conversions. The W87 has a 32-bit elastic buffer that allows delay adjustment. The delay adjustment allows port card use on the peripheral and junctor sides. The W87 detects and decodes the clock, frame pulse and data from the biphase signal. The 16 serial data outputs from the W87s are multiplexed and input to the W72 chip. The W72 chip formats and shifts the serial data in parallel format. For the transmitting path, the the crosspoint card sends the 10-bit parallel data at 5.12MHz. The data is applied to the W72 chip. The W72 chip formats again and shifts the data in an 8-bit serial data stream. Each serial carries 64 pulse code modulation (PCM) channels at 5.12MHz. The W87 chip demultiplexes the serial transmitting data to 2.56 MHZ from 5.12MHz. The transmitted data that passes to the biphase encoder, which encodes framing information to a DS30 biphase format. A different line driver transmits the outputs of the biphase encoder in the W87. A transformer provides dc isolation and rejects common mode signals. The NT8X12 card of the NT8X11 network replaces the functions of the NT3X72, NT3X73 and NT3X86 cards of the NT5X13 network. Test code. The NT8X12AA card handles the insertion and removal of test code (TC) from the NT8X14AA TC card. The NT8X12AA card inserts TC on the port card in the speech channel after the outgoing circuit. When NT8X12AA card inserts TC, the speech bus disables for the involved port and channel. The NT8X12AA card removes the TC from a port card on the incoming side after insertion. The NT8X12AA removes the TC on the outgoing side before the W87 chips.

NT8X11AB (continued)

NT8X11AB (Sheet 4 of 5)

PEC	Slot	Description
	1F-4F, 14F-17F	*Network interface card* Incoming circuit. On each NT8X12AA card, two formatter chips (W72) convert 16 serial ports to parallel, or 16 parallel ports to serial. These circuits convert incoming DS30 data to PCM data. The circuits send the PCM data to an NT8X13AA crosspoint card. The circuits receive and realign incoming biphase data. Outgoing circuit. On each card, eight DS30 (W87) chips provide two bi-directional interfaces to DS30 links. The DS30 links connect NMs to PMs. These circuits convert outgoing PCM data from an NT8X13AA crosspoint card to the DS30 format. The circuits convert the data for transmission on DS30 links.
NT8X13AA	5F-8F, 10F-13F	*Crosspoint card* The NT8X13AA contains time switches (TS) for 2048 input channels and 1024 output channels. The switch from peripheral input channels to junctor output channels on the A-side requires one pair of cards. The switch from junctor input channels to peripheral output channels on the B-side requires a second pair of cards. The NT8X13AA card is identical for A-side and B-side functions. When the NT8X13AA card operates in a time-slot for an A-side function, the card outputs to the junctor cards. When the card operates in a time-slot for a B-side function, the card inputs from the junctor cards. When parallel junctors are in use, the signal goes from an A-side crosspoint card to a B-side crosspoint card. The NT8X13 card is different from the NT3X70 card of the NT5X13 network. The NT8X13 card is different because crosspoint cards do not block time switching. Input channels are switched to output channels without limits. The NT8X13 card is a single-stage TS. Each TS is a 2-way-commutated, 2-way matrix. The matrix switches one of the 2048 input channels to one of the 2048 output channels.

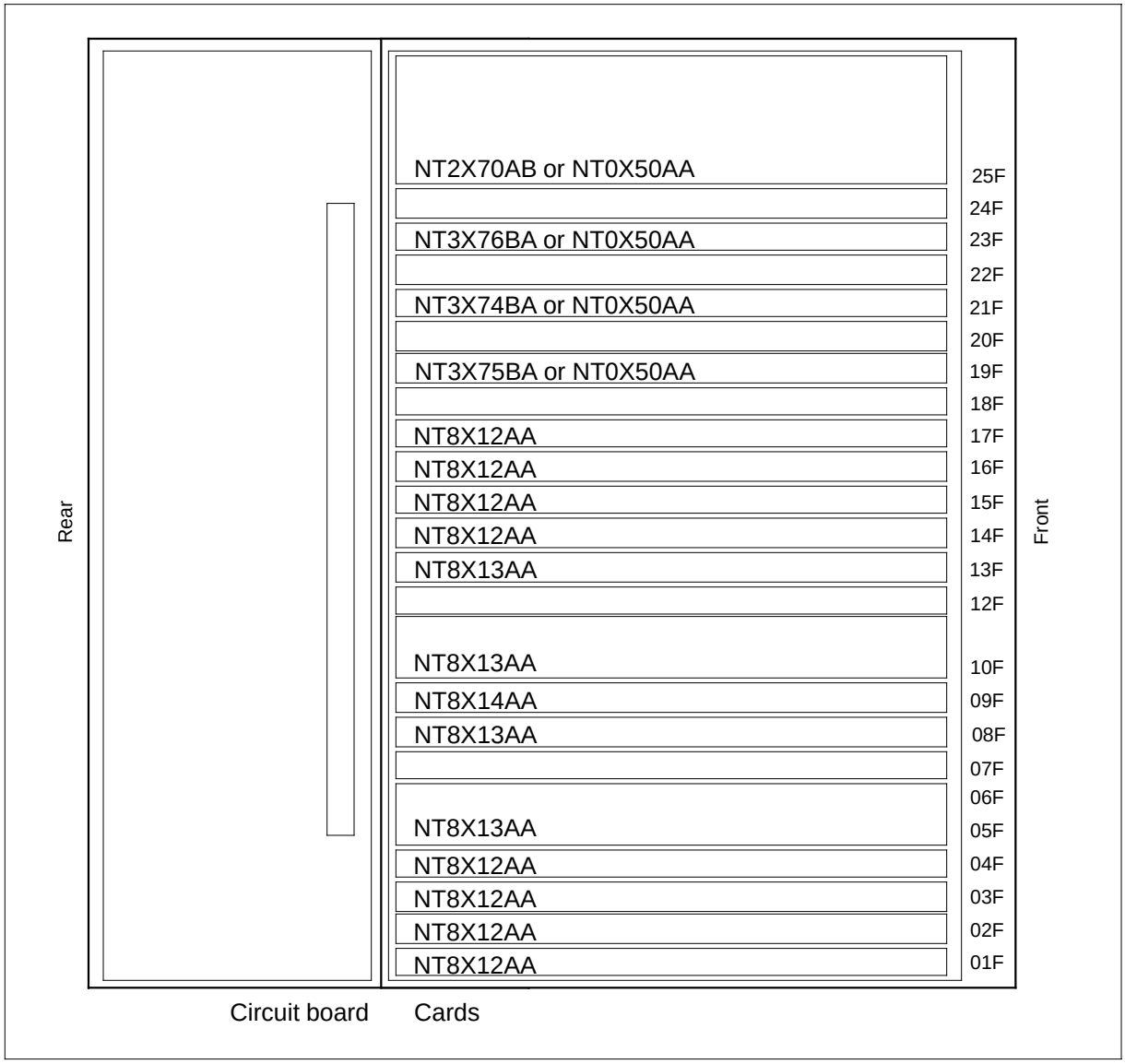
NT8X11AB (Sheet 5 of 5)

PEC	Slot	Description
		Each TS has two data memory (DM) chips that have one frame (125 ms) of PCM samples. The two input buses contain the PCM samples. The DM performs time switching. A speech sample is written in the DM at the time assigned to the interswitch link bus. The speech sample is written at an address a counter specifies. The counter repeatedly cycles through the 512 active addresses of the memory. A sample is read from the DM at an address that the connection memory (CM) in the TS supplies. A DM is 1 kbyte by 10 bits. The DM uses the same memory as the NT5X13. The memory of the NT5X13 is 55 ns, 1 kbyte times 4 SRAM chips. The NT5X13 builds the DM and CM. A CM controls a DM. The CM supplies the DM with the read addresses. The CM holds information that sets the switching pattern. The NCP writes the switching pattern in response to a control message from the CC or the computing module. The CM controls the space switching commutator on the interswitch links. The CM selects a digital pad that controls the level of the speech path. When this event occurs, the speech path follows the outgoing time switch.
NT8X14AA	9F	*Test code card* The NT8X14AA interfaces the NM with the NT3X74BA network control processor card (NCP). This interface occurs for the insertion and removal of TC and to test the digital pads. The CC or the computing module use the TC to check the continuity of a PCM path. When the TC card does not trace the expected test code, the NCP reads the location. The location is sent to the CC of the computing module. A card list of suspected defective card(s) appears at the MAP position.

The design NT8X11AB appears in the following figure.

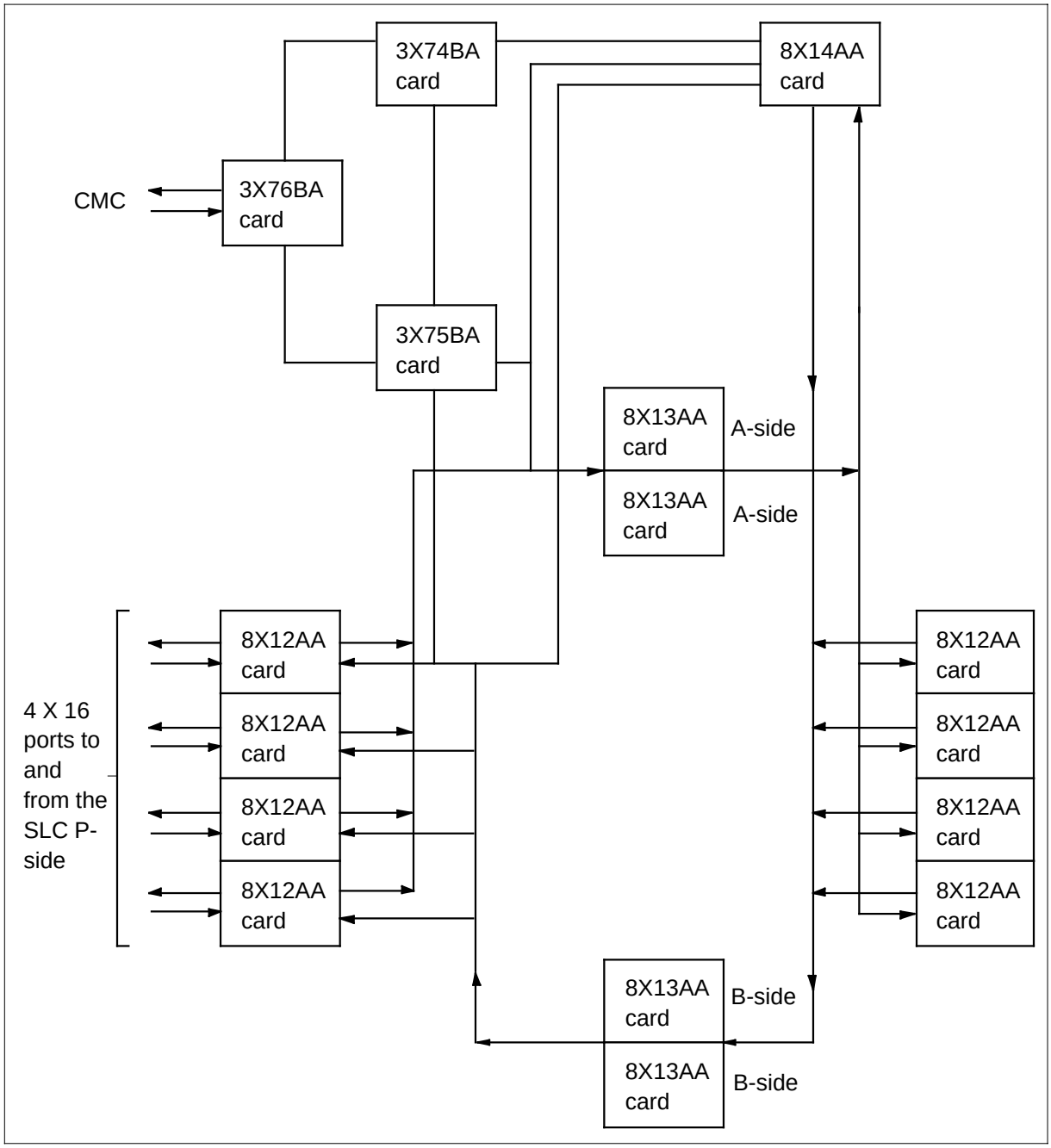
NT8X11AB (continued)

NT8X11AB design



The design of data transmit and receive paths in the NT8X11AB appears in the following figure.

NT8X11AB data transmit and receive paths



NT8X13AA

Product description

The NT8X13AA card provides switching for the NT8X10 dual-shelf network. Each card is a self-contained 2048 time slot (input) by 1024 time slot (output) non-blocking time switch. Any 2048 input time slot can switch to any 1024 output time slot without limits. The NT8X13 cards are in pairs to provide a complete 2048-by-2048 time switch. The dual-shelf network requires two pairs of cards:

- one pair for switching from peripheral inputs to junctor outputs
- one pair for switching from the junctor inputs to the output side

The NT8X13AA has four complementary metal-oxide semiconductor (CMOS) application-specific integrated circuits (ASIC). These circuits contain the following:

- data memory
- connection memory
- pulse code modulation (PCM) gain PROM
- switching logic

This arrangement makes the best use of connection memory than the NT8X13 card. The NT8X13 card requires two times more memory than the NT8X13AA.

Location

The NT8X13s that switch from the peripheral input channels to the junctor output channels are in shelf slots 10 and 12. The pair in slots 5 and 7 switch from the junctor input channels to the peripheral output channels.

Functional description

The main functions of the NT8X13AA follow:

- provision of a non-blocking 2048-by-1024 time switch
- switching from input to output ports on 10-bit parallel data
- read and write on the connection memory with the network control processor
- provision of programmable gain on outgoing switched PCM

Functional blocks

The NT8X13AA has two functional blocks:

- data memory (DM) ASIC J04
- connection memory (CM) ASIC J05

The NT8X13 card represents half of a two-board channel switch. The two boards receive the 10-bit input parallel ports, which are A, B, C and D. Each board has four ASICs that contain the memory and logic of the switch. There are two 10-bit parallel output ports per board. The top board drives outputs W and X, the bottom board drives Y and Z.

A J05 CM ASIC drives each output port on a board. One CM provides switching data for one output port. The clock generator and counter provide the timing in CM ASIC. The 10.24-MHz clock, NC97N and frame pulse NFPN provide timing on the board. The counter provides addresses for the CM. This counter and the CM contents provide addresses for the data memory J04 ASICs.

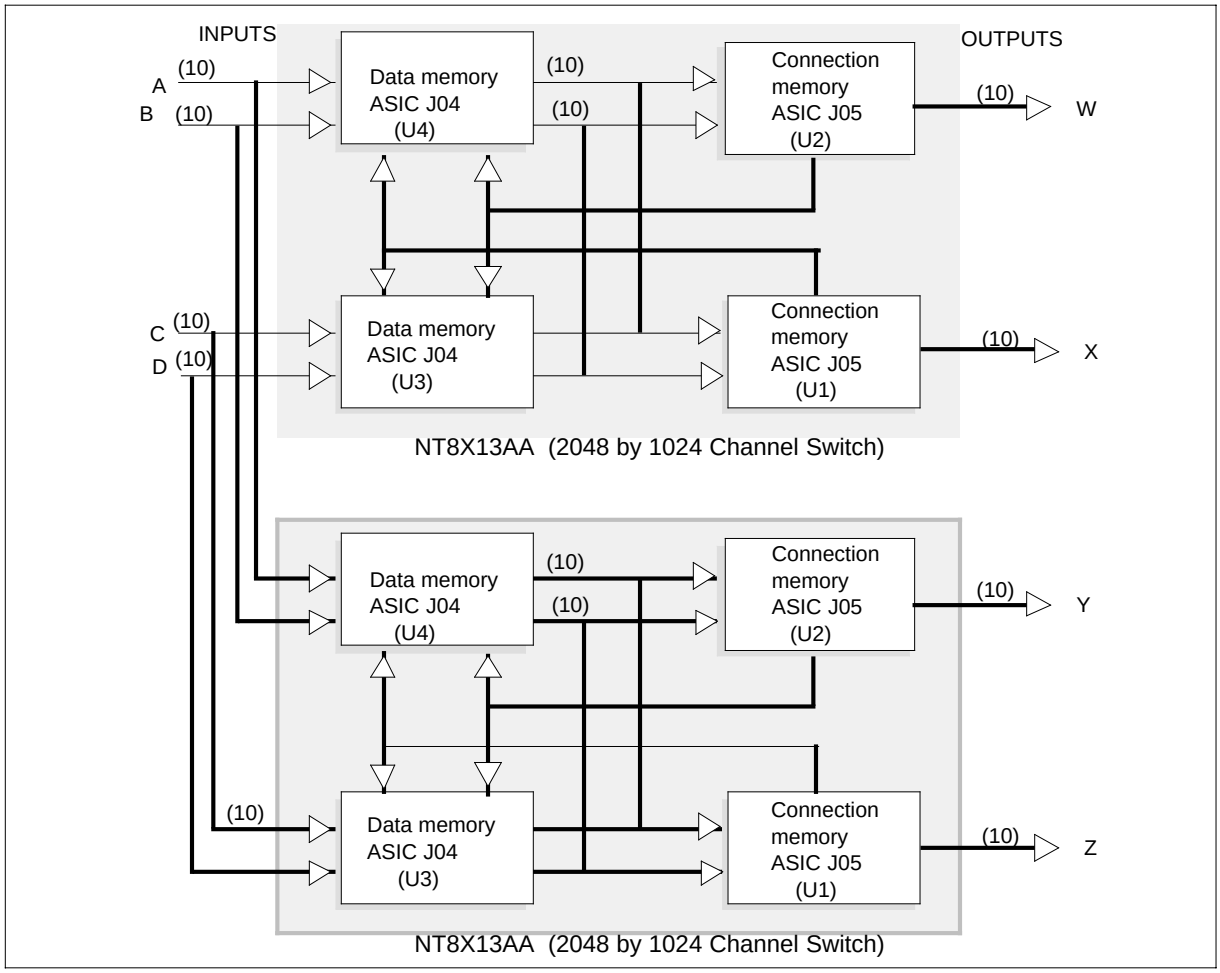
Each CM ASIC has a CPU interface which allows the network control processor (NCP) to control the contents of the CM. The CM of each J05 ASIC is in a different position in the NCP memory map. The CM data transference occurs on a bidirectional 8-bit data bus. To buffer the data between the NCP and the CM, latches that hold data are required. The data buses of both CM ASICs on a board are tied together. Address decoding in the CM ASICs prevents bus contention. The CM provides a digital pad circuit.

As data is written in the DMs, data is removed. The CM provides addressing for the DMs during read operations. The DM is time multiplexed between when the DM stores incoming data and reads data out according to the address the CM provides. Data that leaves the DM must go through two multiplexing stages.

The relationship between the functional blocks appears in the following figure.

NT8X13AA (continued)

NT8X13AA functional blocks



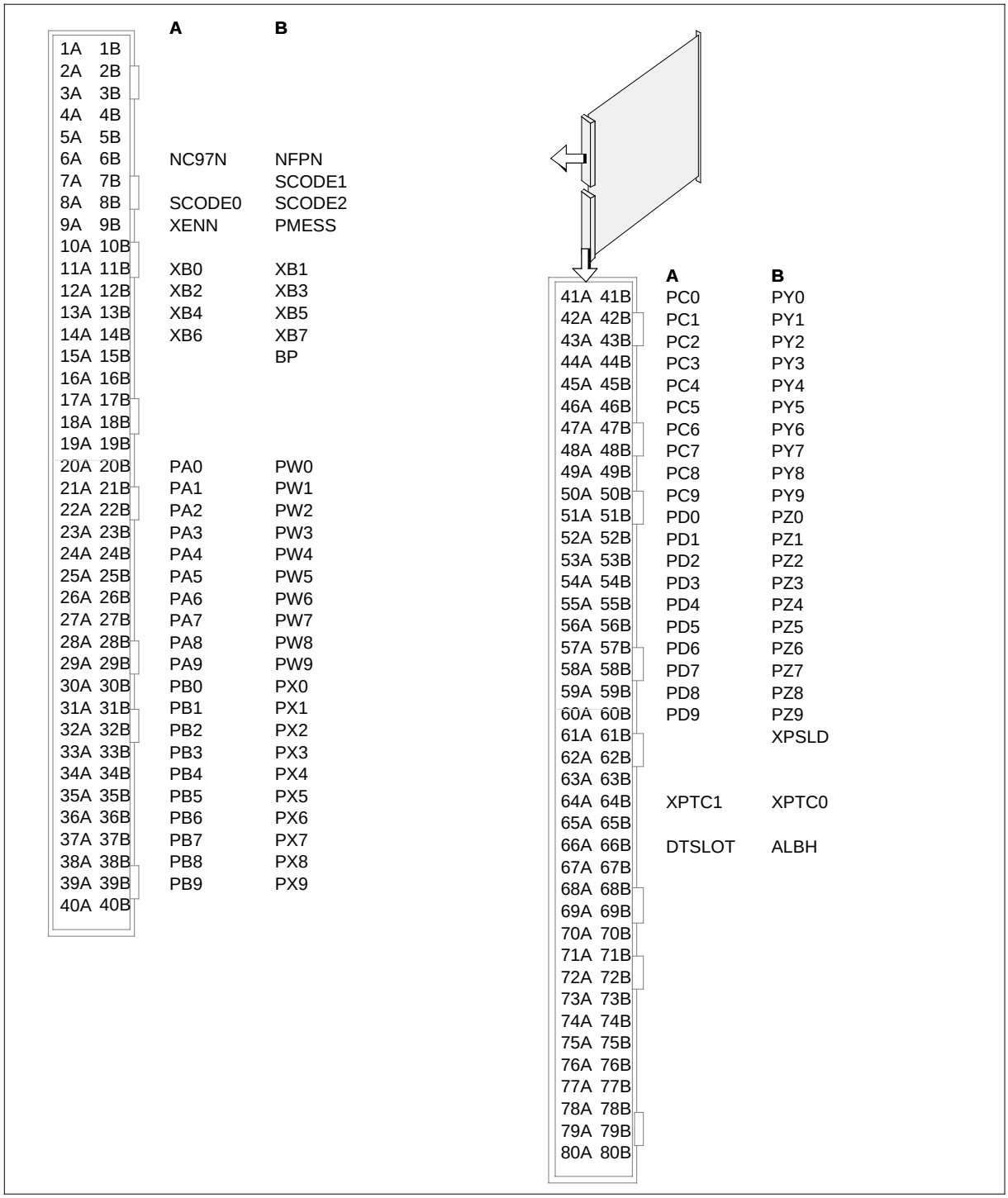
Signaling

Pin numbers

The pin numbers for NT8X13AA appear in the following figure.

NT8X13AA (continued)

NT8X13AA pin numbers

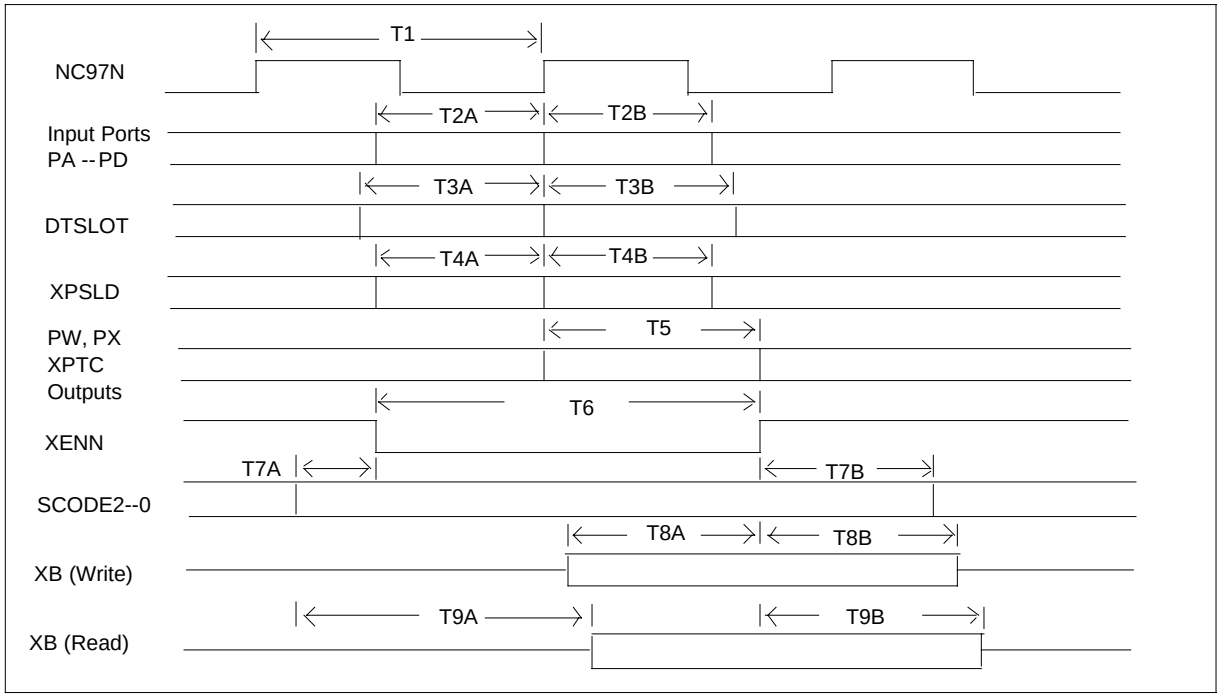


NT8X13AA (end)

Timing

The timing for the NT8X13AA appears in the following figure.

NT8X13AA timing



Technical data

Power requirements

The NT8X13AA draws 400mA of current for a power distribution of 2.0W at +5V.

NT8X18BA

Product description

The card is the central-side (C-side) interface that uses DS30A protocol of the subscriber carrier module-100S remote (SMSR). The NT8X18BA connects to the remote switching center (RSC).

The firmware for the is not backward compatible because the NT8X18BA has an important new design.

Location

The NT8X18BA fits in slot 22.

Functional description

The NT8X18BA serves as a network-side interface of the SMSR for pulse code modulation (PCM) data and messaging.

The NT8X18BA has the following features:

- a DS30A interface on the network side of the SMSR for PCM
- correct timing delays in the PCM path to match current link timing
- insertion and extraction of data from messaging channels
- data multiplexer from the link from a DS30 rate (2.56 Mbits/s) to a DS60 rate (5.12 Mbits/s)
- data demultiplexer that goes to the link from a DS60 rate to a DS30 rate
- link frame pulses from the link to the formatter for system synchronization
- the network looparound path and control circuits
- circular buffering for incoming and outgoing PCM

The NT8X18BA connects to the DS30A ports on the network side of the SMSR. In the SMSR system, the NT8X18BA connects to the formatter card and the message card. The DS30A ports use differential drivers and receivers to transmit and receive PCM at a 2.56 Mbits/s rate. The system receives frame pulses and clock pulses from the network side of the SMSR on the DS30A links. In the SMSR, the system transmits and receives PCM at a DS60 rate, to and from the formatter card. The system transmits messaging to and receives messaging from the message card at a DS60 rate.

Functional blocks

The NT8X18BA consists of the following functional blocks:

- the link-side interface
- the link-side PCM path

NT8X18BA (continued)

- the link-timing programmable read-only memory (PROM)
- the link-side incoming time slot counter
- the link-side outgoing time slot counter
- the shelf-side incoming time slot counter
- the shelf-side outgoing time slot counter
- the message timing PROM
- the shelf-side PCM path
- the outgoing message
- the incoming message
- the PCM demultiplexer
- the outgoing multiplexer
- the looparound circuit
- the formatter interface

The relationship between the functional blocks appears in the following table.

Link-side PCM path

The link-side PCM path is one of four PCM paths. Each path uses an N02 formatter device to perform two-way conversion of serial PCM between serial and parallel format. The paths include 8-bit and 10-bit latches. These latches align the PCM data for the N02 and for the dual-port RAM access.

Link timing PROM

The link timing PROM provides a receive frame pulse that is timed again. The link timing PROM provides the SYNC signal for the link-side N02 devices.

Link-side incoming time slot counter

The link-side incoming time slot counters in the NT8X18BA. The four time slot counters determine addresses for the parallel receive PCM (RPCM) data and transmit PCM (XPCM) data. Each of the counters load different values on a frame pulse. This action provides the correct delay for channel alignment at the outputs of the NT8X18BA.

Link-side outgoing time slot counter

The link-side outgoing time slot counter is one of four time slot counters in the NT8X18BA. The four time slot counters determine addresses for the parallel RPCM and XPCM data. Each of the counters load different values on a frame pulse. This action provides the correct delay for channel alignment at the outputs of the .

Shelf-side incoming time slot counter

The shelf-side incoming time slot counter is one of four time slot counters in the NT8X18BA. The four time slot counters determine addresses for the parallel RPCM and XPCM data. The shelf-side incoming time slot counter also drives the timing PROMs. Each of the counters load different values on a frame pulse. This action provides the correct delay for channel alignment at the outputs of the NT8X18BA.

Shelf-side outgoing time slot counter

The shelf-side outgoing time slot counter is one of four time slot counters in the NT8X18BA. The four time slot counters determine addresses for the parallel RPCM and XPCM data. Each of the counters load different values on a frame pulse. This action provides the correct delay for channel alignment at the outputs of the NT8X18BA.

Message timing PROM

The message timing PROM provides the signals for message channel insertion and removal. The message timing PROM provides the SYNC signals for the N02 devices in the shelf-side PCM path.

Shelf-side PCM path

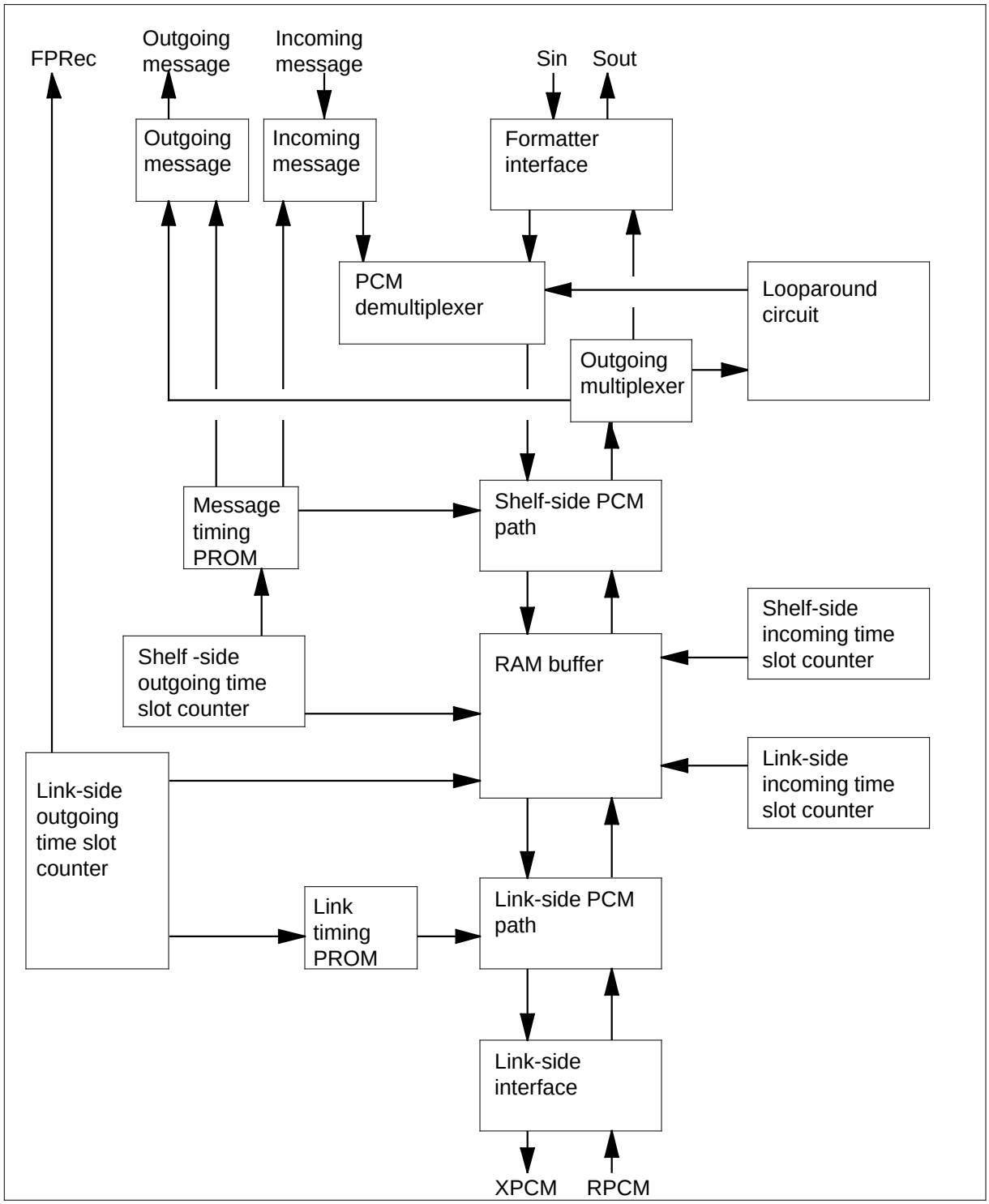
The shelf-side PCM path is one of four PCM paths. Each path uses an N02 formatter device to convert PCM from serial to parallel format, or from parallel to serial format. The paths include 8-bit and 10-bit latches. These latches align the PCM data for the N02 and for the dual-port RAM access.

Looparound circuit

The looparound circuit provides a looparound path back to the C-side. The system maintains loop control separately for each port and channel over a serial link. A register on the formatter card controls the loop circuit.

NT8X18BA (continued)

NT8X18BA functional blocks



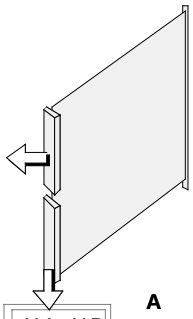
Signaling

Pin numbers

The pin numbers for the NT8X18BA appear in the following figure.

NT8X18BA (continued)

NT8X18BA pin numbers



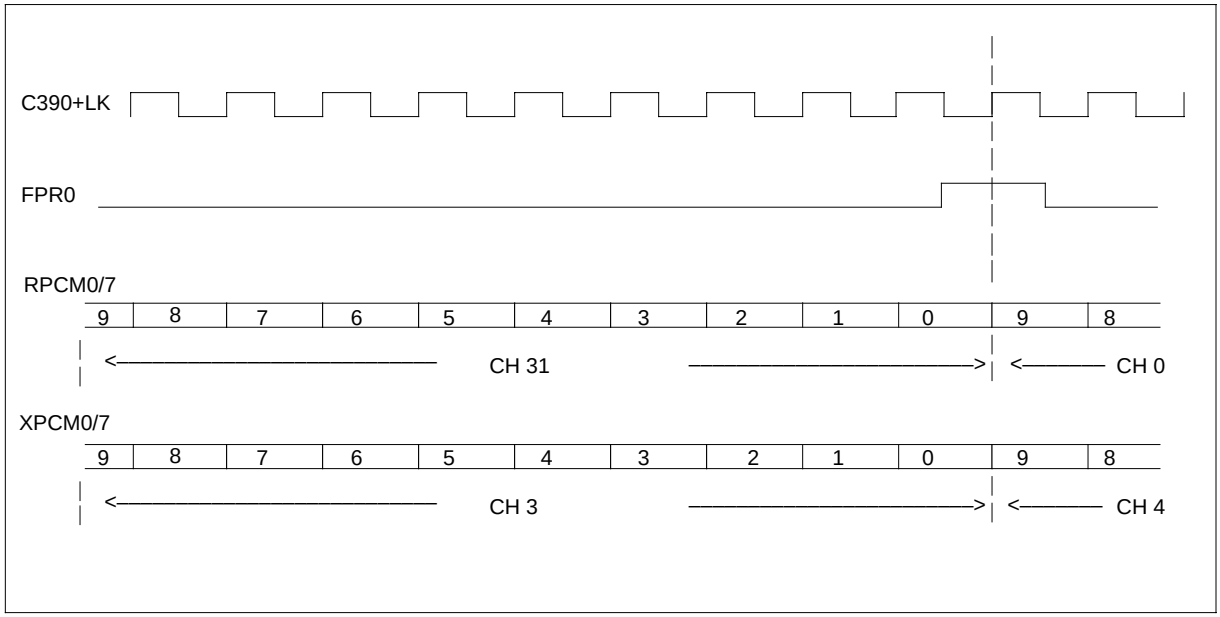
	A	B
1A 1B	GND	GND
2A 2B	+5V	+5V
3A 3B	+5V	+5V
4A 4B	+5V	+5V
5A 5B	GND	GND
6A 6B	FP–	C97+
7A 7B	GND	GND
8A 8B		
9A 9B	ACT	GND
10A 10B	C1950+	C1950–
11A 11B	FPR0+	FPR0–
12A 12B	RPCM0+	RPCM0–
13A 13B	RPCM1+	RPCM1–
14A 14B		
15A 15B		
16A 16B	RPCM2+	RPCM2–
17A 17B	RPCM3+	RPCM3–
18A 18B		
19A 19B	XPCM0+	XPCM0–
20A 20B	XPCM1+	XPCM1–
21A 21B		
22A 22B		
23A 23B	XPCM2+	XPCM2–
24A 24B	XPCM3+	XPCM3–
25A 25B		
26A 26B	GND	GND
27A 27B	SOUT0M	SOUT0
28A 28B	SOUT2M	SOUT2
29A 29B	SOUT4M	SOUT4
30A 30B	SOUT6M	SOUT6
31A 31B		
32A 32B		
33A 33B		
34A 34B		
35A 35B	GND	GND
36A 36B	FPT	C97+T
37A 37B	FP–M	C97+M
38A 38B	FPL–T	GND
39A 39B	FPL–M	CH0T
40A 40B	CH0TT	CH0TM

	A	B
41A 41B	GND	GND
42A 42B		
43A 43B	LPCNTM	LPCNT
44A 44B		
45A 45B	LPLTM	LPLT
46A 46B	GND	GND
47A 47B	SIN0M	SIN0
48A 48B	SIN2M	SIN2
49A 49B	SIN4M	SIN4
50A 50B	SIN6M	SIN6
51A 51B		
52A 52B		
53A 53B		
54A 54B		
55A 55B	FPL–	GND
56A 56B	RPCM4+	RPCM4–
57A 57B	RPCM5+	RPCM5–
58A 58B	RPCM6+	RPCM6–
59A 59B	RPCM7+	RPCM7–
60A 60B	XPCM4+	XPCM4–
61A 61B	XPCM5+	XPCM5–
62A 62B	XPCM6+	XPCM6–
63A 63B	XPCM7+	XPCM7–
64A 64B		
65A 65B		
66A 66B		
67A 67B		
68A 68B		
69A 69B		
70A 70B		
71A 71B		
72A 72B	GND	GND
73A 73B	FPRC2	FPRC0
74A 74B		
75A 75B	CH0S0	CH0R0
76A 76B	CH0S2	CH0R2
77A 77B		
78A 78B	GND	GND
79A 79B		
80A 80B	GND	GND

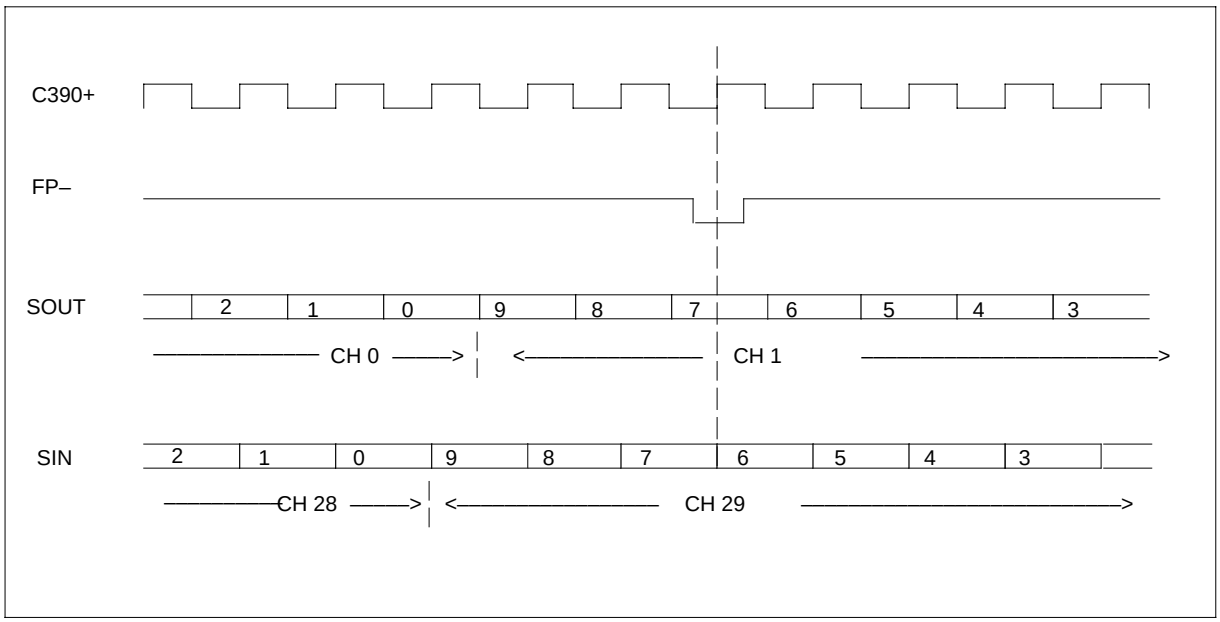
Timing

The timing for the NT8X18BA appears in the following figure.

NT8X18BA C-side timing

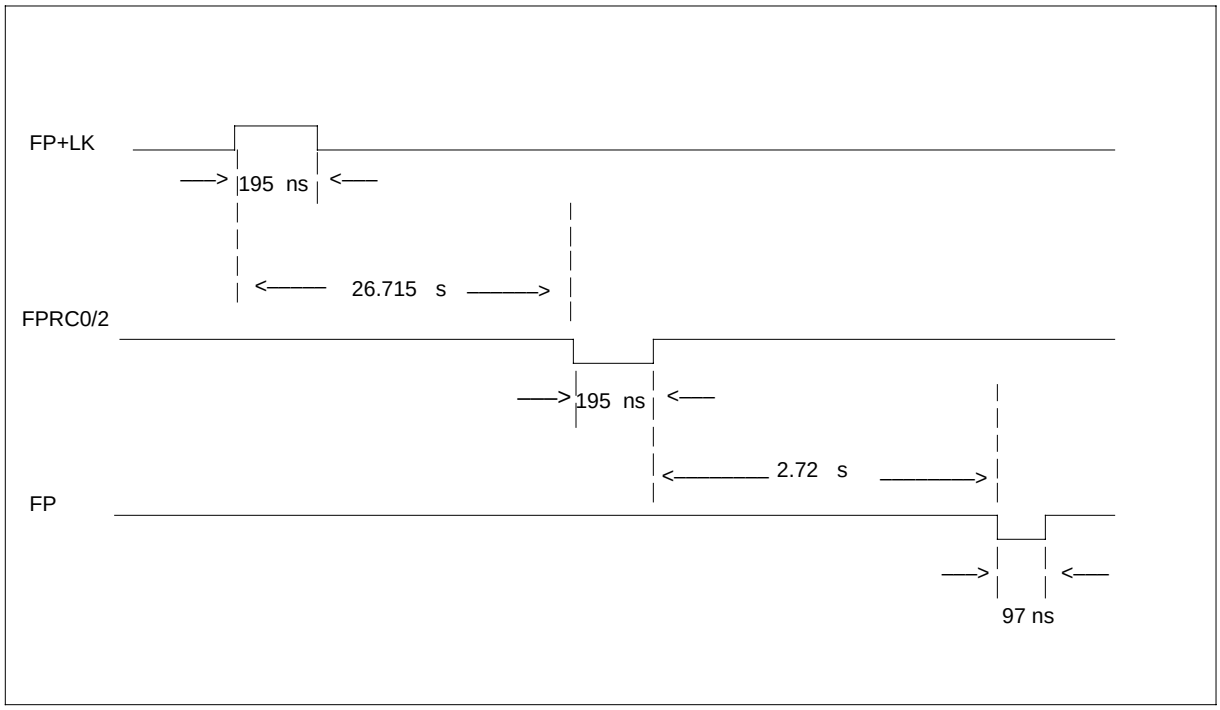


NT8X18BA formatter interface timing



NT8X18BA (end)

NT8X18BA timing relationship between frame pulses



Technical data

Power requirements

The nominal supply voltage for the NT8X18BA is +5V and the supply current is 1.8A.

NT8X40AA

Product description

The NT8X40AA international outside plant module (IOPM) is a complete switching center that supports a maximum of 640 analog lines. This module is a version of the NT6X14AA international remote line concentrating module (RLCM). An environmentally-controlled cabinet houses the module.

The NT8X40AA includes the following components:

- a two-shelf line concentrating module (LCM)
- host interface equipment (HIE) circuit pack fill
- a remote maintenance module (RMM) circuit pack fill
- a frame supervisory panel (FSP) (NT6X25BB)
- two environmental control units (ECU)
- power equipment and optional batteries for back-up power

The central side (C-side) of the IOPM connects to a common peripheral controller (CPC) by two to six DS-1 links. The CPC can be a line group controller (LGC) at the host office or in a remote switching center (RSC). The CPC can be a line trunk controller (LTC) at the host office or in a remote switching center (RSC). When the CPC instructs the IOPM, the IOPM links a subscriber line to a DS-1 channel. This link makes sure that incoming and outgoing calls can complete.

Optional fiber optic connections are also available.

The IOPM features a two-compartment cabinet. The main compartment contains the main switching components. The main switching components are as follows:

- LMM
- HIE common circuit pack fill
- RMM common circuit pack fill

The main compartment also contains batteries and the environmental control equipment. The end-access compartment contains the protection, termination, and cross-connection equipment for voice frequency pairs. The end-access compartment contains the DS-1 links to the host office or RSC.

NT8X40AA (continued)

Parts

The international OPM contains the following parts:

- NT6X04BB-International line control module
- NT6X11BB-International HIE common circuit pack fill
- NT6X13AA-International RMM
- NT6X25BB-FSP
- NT8X05AA-Power control unit
- NT8X06AA-ECU

International line concentrating module

The NT6X04BB international line concentrating module (ILCM) functions as an interface between the CPC and a maximum of 640 analog lines. The connections between the ILCM and the associated CPC depend on the physical distance between the two units. If the ILCM is in 15 m (50 ft) of the CPC, DS30A links are used. The DS-1 links are used for distances of a maximum of 241 km (150 mi).

The ILCM comprises two single-shelf line concentrating arrays (LCA): LCA-0 and LCA-1. The LCA-0 is on the bottom and LCA-1 is on the top. Each LCA in the ILCM includes a control complex. The control complex consists of an NT6X51AA LCM processor (NT6X51AA) and NT6X52AB digroup control cards. The control complex can control the two LCAs under the following conditions:

- the LCM processor or digroup control card in the associated LCA fails
- a message link to the associated LCA fails
- the LGC forces an activity switch

Each LCA also contains a maximum of five LCM drawers. Each drawer contains an NT6X54AB international bus interface card (BIC) and a maximum of 64 line circuit (LC) cards. The 64 line circuits divide in two 32-channel line subgroups (LSG). Each LCA includes an NT6X53AA power converter. The power converter can provide the operating voltages for the two LCAs if the companion converter fails. The circuit cards in the ILCM also incorporate digital-path looparound features that can isolate single faults. The system also sends fuse and converter-failure alarm outputs to the FSP.

International host interface equipment common circuit pack fill

The NT6X11BB international HIE common circuit pack fill functions as an interface. The NT6X11BB provides the interface between the DS30A links of

the LCAs and the CPC in the central office. The fill provides the following functions:

- clock signal and ringing generators for the LCAs
- messaging interface and data rate conversion for the following:
- PCM30 line cards
- LCA of the LCMs
- international RMM
- call-processing functions when the emergency stand-alone (ESA) option is included

These functions allow calls that originate and terminate on the same outside plant module (OPM) to complete. The calls can complete if the links to the host office are lost.

The fill contains the following parts:

- two or three NT6X27AB PCM30 interface circuit cards
- two NT6X73BA link control circuit cards (LCC-0 and LCC-1)
- two NT6X60AA RLCM ringing generators (RG-0 and RG-1)
- two NT2X70AE power converters

If the ESA option is included, the fill contains the following:

- NT6X45AF ESA processor
- NT6X75DA ESA tone and clock card
- NT6X47AB ESA memory card

International remote maintenance module

The NT6X13DA international RMM common circuit pack fill provides maintenance and operational support for remote offices. This circuit pack fill is a modified version of the NT2X58 maintenance trunk module (MTM) common circuit pack fill. The fill supports the following:

- metallic test access (MTA)
- incoming/outgoing test trunks
- line test units (LTU)
- scan and signal distribution (SD) points
- digitone receivers with the included ESA option

NT8X40AA (continued)

The international RMM common circuit pack fill contains the following:

- NT6X47AA control circuit card
- NT2X59AA group coder-decoder (CODEC)
- NT2X59AA tone circuit card
- NT2X06AB and NT6X09AA power converters
- a maximum of 14 service circuit cards. The types of cards depends on the needs of the office

Some of the service cards used in the international RMM are for MTA functions.

The international RMM common circuit pack fill reduces the amount of traffic on the DS-1 links. This circuit pack fill gives the NT6X04BB LCM access to test and service circuit cards at the remote site. The C-side interface of the international RMM common circuit pack fill connects to the following by DS30A links. The C-side interface connects to each of the two NT6X50AA line control cards in the host interface common circuit pack fill. The international RMM connects the two LCCs to make sure that the shelf remains operational. The activity of LCCs does not determine the connection. Selection and tests of a line circuit and display of test results occur through the DS30A links to the LCC. These activities also occur from the LCC to the host office. The test procedures occur with the maintenance administration position (MAP) and DMS-100 *Commands Reference Manual*.

Frame supervisory panel

The NT6X25BB FSP provides the power control circuits that the power converters and ringing generators require in separate shelves. The FSP includes the following:

- frame-fail indicators
- fuse-fail alarm output
- front and rear alarm battery supply (ABS) test jacks
- four front-panel service jacks that include two telephone pairs (TEL-A and TEL-B) and two data pairs (DATA-A and DATA-B)

The frame supervisory channel contains the following:

- has two talk battery filters
- nine circuit breakers (CB1-CB9)

- eight fuses (F01-F08)
- three plug-in cards (CD1-CD3) that consist of the following:
  - NT0X91AA alarm
  - NT0X91AA converter drive circuit pack
  - NT0X91AE converter drive protection circuit pack
  - NT6X36AA alarm circuit circuit pack

The frame supervisory channel monitors the condition of the power converters and ringing generators in the international OPM common circuit pack fills. The frame supervisory channel monitors the input voltage. Two separate inputs: -48V (A) and -48V (B) are available.

Power control unit

The NT8X05AA power control unit contains ac power circuits and breakers for commercial and emergency power. The power control unit includes two 25 A rectifiers that convert the ac input to -52V dc. When the international OPM frame includes the back-up batteries, the power control unit includes a battery charging unit (NT8X03AA). This unit controls battery charging and activates the back-up battery system if the ac power fails. The batteries are in strings in the rear of the OPM frame. Each string contains four 12 V batteries.

Battery backup can maintain the operation of the OPM for a maximum of 8 h.

Environmental control units

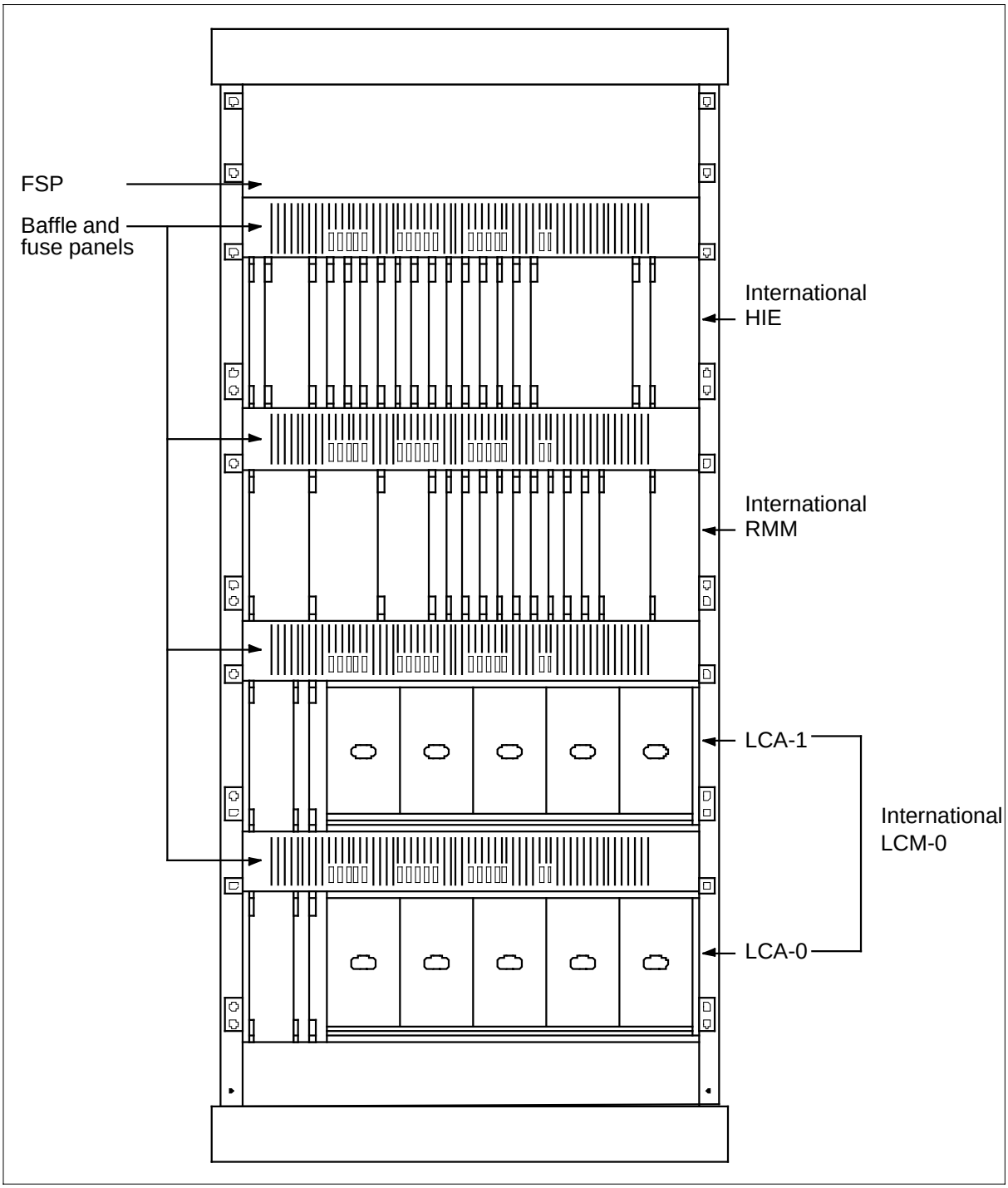
The NT8X06AA ECUs make sure that the environmental conditions in the main compartment remain in the operating range of the internal components. Some examples of environmental conditions are temperature and humidity. The ECUs are at the bottom of each bay. The ECUs contain the air inlets, air filters, fans, heaters and air outlets used to maintain best conditions for operation.

Design

The design of the international OPM appears in the following figure.

NT8X40AA (end)

NT8X40AA parts



Product description

The distributed processing peripheral complies with the Underwriters Laboratory (UL) specifications. This peripheral allows remote polling of automatic message accounting (AMA) data. The system collects and stores the AMA data on the distributed processing peripheral (DPP) internal disk drive units (DDU). The system forwards the data on request to a host collector.

The available disk drives for the are 5.25 in Winchester units. Three disk capacities are available: 140, 380 and 760 Mbyte.

The uses data compression firmware to increase data transmission speed to the host system. This process achieves a nominal compression ratio of 2.8 to 1. This ratio is equivalent to data that is not compressed polled at approximately 27,000 baud over dial-up phone lines. The host collector must be able to receive and expand compressed data. The system stores data at the DPP and host collector in non-compressed form.

The uses a modem interface for transmission of data to the host collector at a maximum speed of 56 Kbit/s. The 56-Kbit/s polling feature is standard with the NT6M72EA 760-Mbyte disk drive. This polling feature is an option for the NT6M72DA and NT6M72DA 380-Mbyte drives. This polling feature is not available for use with the NT6M72BA and NT6M72DE 140-Mbyte disk drives.

The system polls compressed data at a maximum rate of 9600 baud. The system uses an RS-232 interface from the AMA transmitter (AMAT) on the NT6M94BA to the modem. The modem is on a close shelf. A standard modem is the 049M037-011 circuit pack (CP) mounted on an NT5X08AC shelf.

The operates in a redundant configuration through the use of crossover circuits. The NT8X48AD operates in a redundant configuration to make sure operation continues in the event of a component failure.

The uses a UL-compliant chassis and is mounted in an input/output (I/O) controller frame like the NT0X43AD.

NT8X48AD (continued)

Parts

The NT8X48AD shelf consists of the following parts:

- Data Compression
  - — NT6M63CJ-the EPROM CP
  - — NT6M63CL-the EPROM CP
  - — NT6M94AA-the 56 Kbit/s interface CP
  - — NT6M94BA-the 56-Kcompression interface CP
- Disk Drive
  - — NT6M66AL-the Disk drive interface CP
  - — NT6M66AH-the Disk drive interface CP
  - — NT6M66BA-the SCSI disk drive interface CP
  - — NT6M66BC-the SCSI disk drive 140 interface CP
  - — NT6M72BA-the 140-Mbyte disk drive assembly (provisionable)
  - — NT6M72DE-the 140-Mbyte disk drive assembly (provisionable)
  - — NT6M72DA-the 380-Mbyte disk drive assembly (provisionable)

— NT6M72DD-the 380-Mbyte disk drive assembly (provisionable)

— NT6M72EA-the 760-Mbyte disk drive assembly (provisionable)

- DPP EMC
  - — NT8M05AB-the DPP EMC
    - – NTM609AB-the Error control jumper printed circuit board assembly (PCA)
    - – NT6M56AB-the Fan filter
    - – NT6M56AD-the Fan filter CP
    - – NT6M60BA-the Quad SIO PCA
    - – NT6M62BA-the CPU/DMA PCA
    - – NT6M64AA-the Extended memory
    - – NT6M65AA-the Error control II PCA
    - – NT6M68AA-the Bus terminator
    - – NT6M70AC-the Data stream interface (DSI) PCA
    - – NT6M71AB-the Power supply assembly
    - – NT6M84BA-the Power/alarm communication PCA
    - – NT6M85AA-the 4-channel communication PCA

Design

Descriptions of the parts that comprise the NT8X48AD appear in the following table.

NT8X48AD (Sheet 1 of 5)

PEC	Slot	Description
NTM609AB	B 05	*Error control II jumper circuit pack* The NT6M609AB contains a loop to feed data from the B processor bus to the NT6M65AA in the A chassis. The NT6M609AB contains a switch to bypass the NT6M65AA if the NT6M65AA needs replacement.
NT6M56AB	B 19	*Fan filter printed circuit board assembly* The NT6M56AB fan filter PCA is a low-pass filter that prevents the feedback of fan-generated noise on the line.

NT8X48AD (continued)

NT8X48AD (Sheet 2 of 5)

PEC	Slot	Description
NT6M56AD	A18, B18	*Fan filter circuit pack* The NT6M56AD suppresses fan noise from the -48V dc feed.
NT6M60BA	A06, B06	*Quad SIO circuit pack (4-MHz)* The NT6M60BA provides a port for maintenance terminal communications. The NT6M60BA provides a port for the polling of call record data-if the 56 K polling feature is not equipped. The NT6M60BA also provides two ports for the input/output controllers for serial communication with the DMS-100 maintenance and administration position (MAP). Each port maintains a separate, selectable baud rate for the transmit and receive functions. The receive clock can be set for internal or external.
NT6M62BA	A01, B01	*CPU/DMA circuit pack* The NT6M62BA uses an 8-bit microprocessor to control the data flow in the NT8X48AD. The two NT6M62BA CPUs can control the DPP. The two CPUs are electronically linked to allow one processor to assume control if the other processor fails. A disk crossover capability is also available so that one CPU can communicate with a disk drive. This crossover capability safeguards against the loss of data if a failure occurs in a processor. If the system fails, the standby processor takes control.
NT6M63CJ	A02, B02	*EPROM circuit pack (BCS29 and up)* The NT6M63CJ EPROM provides the firmware (programming) for the NT8X48AD, like the compression algorithm, for BCS29 and higher. The NT6M63CJ is for use with the 380 Mbyte and 760 Mbyte disk drives and the 56 K compression feature.

NT8X48AD (Sheet 3 of 5)

PEC	Slot	Description
NT6M63CL	A02, B02	*EPROM circuit pack (BCS21-28)* The NT6M63CL EPROM provides the firmware (programming) for the NT8X48AD, like the compression algorithm, for BCS21 to BCS28. The NT6M63CL is for use with the 56 K compression feature for BCS21-28 or non 56 K compression BCS29.
NT6M64AA	A03, B03	*Extended memory circuit pack* The NT6M64AA provides 128 Kbytes of dynamic RAM (DRAM) for processing elements of the NT8X48AD.
NT6M65AA	A 05	*Error control II circuit pack* The NT6M65AA constants checks the system to verify complete operation and immediately sense and react to a fault. At the system level, the NT6M65AA regulates the status lamps, alarms, and the processor A select (A SEL) line directing. Processor (A or B) is now in control of the DPP.
NT6M66AL	Provisionable A11, B11	*Disk drive interface circuit pack* The NT6M66AL disk interface CP links the processing unit and the disk controller PCB in the NT8X48AD.
NT6M66AH	Provisionable A11, B11	*Disk drive interface circuit pack* The NT6M66AH disk interface CP links the processing unit and the disk controller PCB in the NT8X48AD.
NT6M66BA	Provisionable A11, B11	*SCSI disk drive interface circuit pack* The NT6M66BA small computer systems interface (SCSI) disk interface CP links the processing unit and the disk controller PCB in the NT8X48AD.
NT6M66BC	Provisionable A11, B11	*SCSI disk drive 140 interface circuit pack* The NT6M66BC small computer standard interface (SCSI) disk interface CP links the processing unit and the disk controller PCB. The PCB is part of the NT6M72BA or DE 140-Mbyte disk drive unit (DDU) in the NT8X48AD.

NT8X48AD (continued)

NT8X48AD (Sheet 4 of 5)

PEC	Slot	Description
NT6M68AA	A14, B14	*Bus terminator printed circuit board assembly* The NT6M68AA bus terminator PCB assembly terminates the end of the system bus. The assembly is part of the NT8X48AD.
NT6M70AC	A12, B12, A13, B13	*Data stream interface II PCA* The NT6M70AC DSI II PCAs are smart circuit assemblies. Each assembly has a Z80 microprocessor, EPROM-resident software, and RAM. The NT6M70ACs are designed as active devices. Emulation of the magnetic tape drive (MTD) operations requires that the DPP maintain redundant communications with the DMS-100 mag tape ports. The DIS software receives and processes the commands that the DMS-100 normally sends to the MTD. The DIS software responds with the status and strobe signals that the MTDs normally send back to the DMS-100. The NT6M70AC provides the intelligence to handle the call record data from the DMS-100.
NT6M71AB	A20, B20	*Power supply assembly* The NT6M71AB power supply provides output voltages of -12V, +5V, +8.5V, and +12.0V. The NT6M71AB requires and input voltage between -42V and -60V.
NT6M72BA	Provisionable A21, B21	*140-Mbyte disk drive assembly* The NT6M72BA provides 140 Mbytes of disk space to the NT8X48AD.
NT6M72DE	Provisionable A21, B21	*140-Mbyte disk drive assembly* The NT6M72DE provides 140 Mbytes of disk space to the NT8X48AD.
NT6M72DA	Provisionable A21, B21	*380-Mbyte disk drive assembly* The NT6M72DA provides 380 Mbytes of disk space to the NT8X48AD.
NT6M72DD	Provisionable A21, B21	*380-Mbyte disk drive assembly* The NT6M72DD provides 380 Mbytes of disk space to the NT8X48AD.

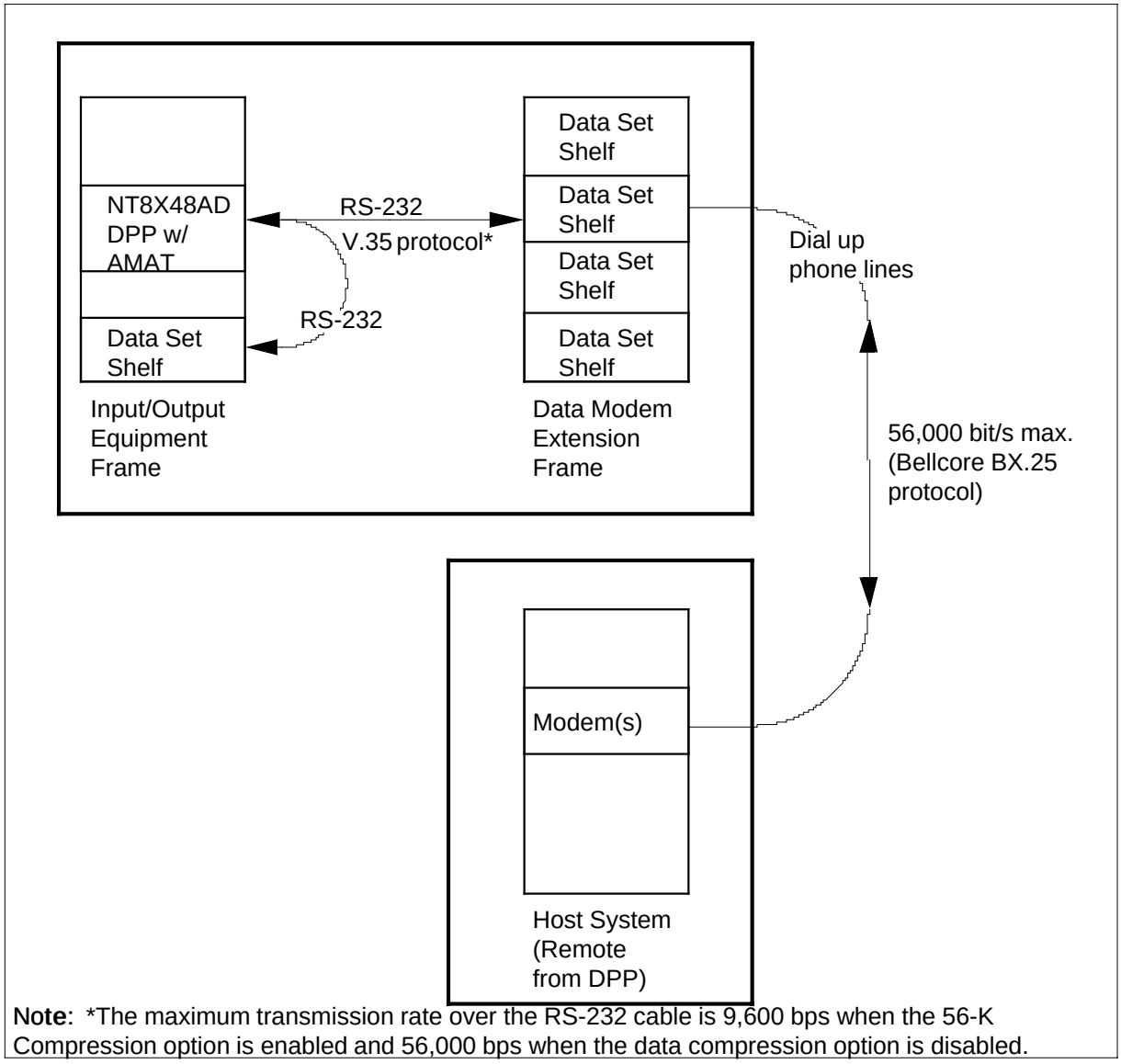
NT8X48AD (Sheet 5 of 5)

PEC	Slot	Description
NT6M72EA	Provisionable A21, B21	*760-Mbyte disk drive assembly* The NT6M72EA provides 760 Mbytes of disk space to the NT8X48AD.
NT6M84BA	A 16	*Power/alarm communication circuit pack* The NT6M84BA performs a multi-purpose function. The function is to provide the communication path between the NT6M60BA Quad SIO PCA and the different peripherals (maintenance terminal). *Note* : For a DPP system with 56K polling, the modem path is through the 56K Xovr. The NT6M84BA provides circuits to respond to switching signals from the NT6M65AA or keyboard-entered commands. The NT6M84BA also provides power detection, alarm generation and ac clock circuits.
NT6M85AA	A 17	*4-channel communication printed circuit board assembly* The NT6M85AA provides the physical interface between the serial communication channels of the DPP unit and external devices.
NT6M94AA	Provisionable A07, B07	*56 Kbit/s interface circuit pack* The NT6M94AA CP contains the AMAT.
NT6M94BA	Provisionable A07, B07	*56K/compression interface circuit pack* The NT6M94BA CP contains an AMAT that can take advantage of a data compression algorithm programmed to the NT6M63CJ EPROM.

The external data links for the NT8X48AD appear in the following figure.

NT8X48AD (continued)

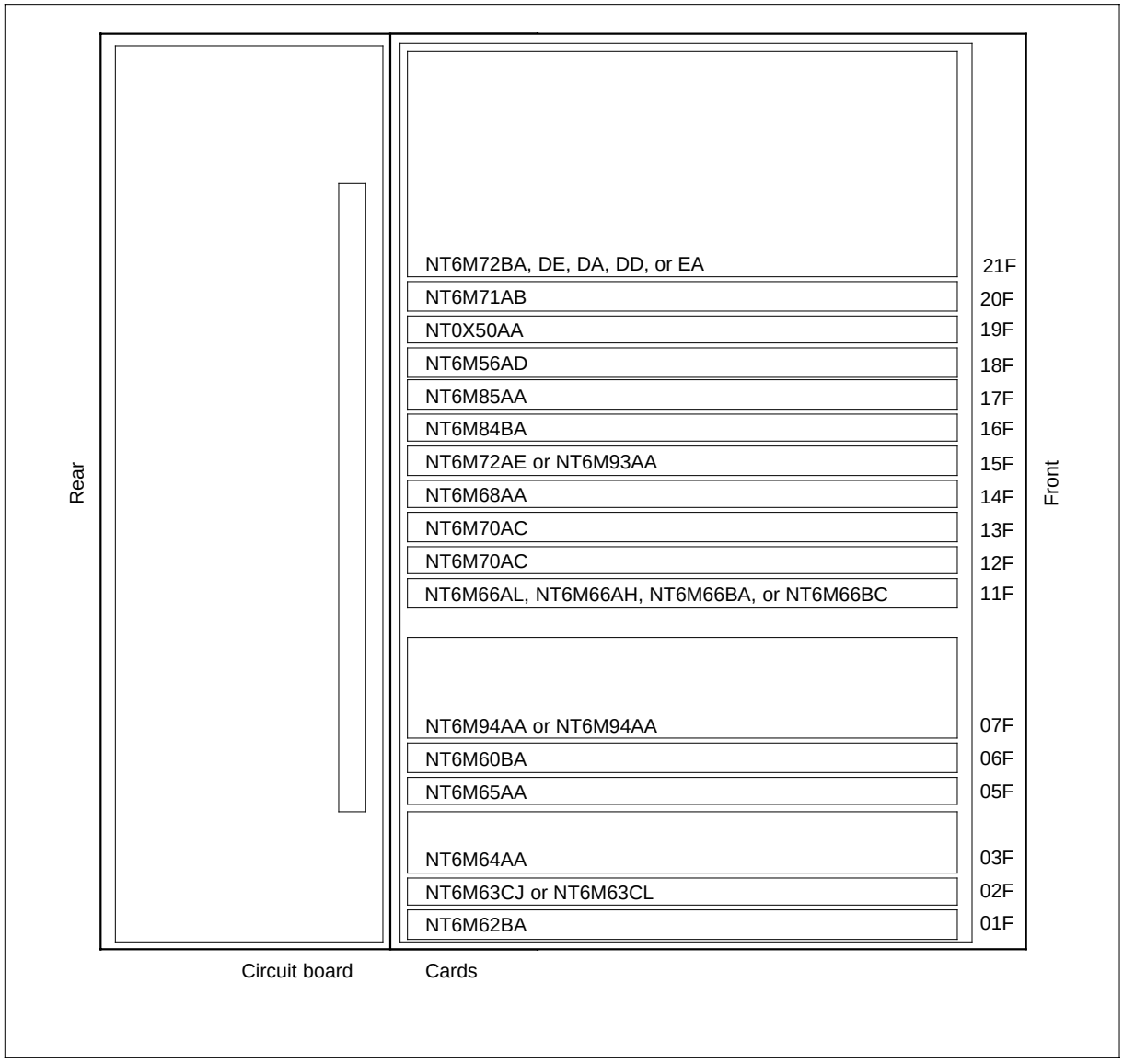
NT8X48AD external data links



Note: *The maximum transmission rate over the RS-232 cable is 9,600 bps when the 56-K Compression option is enabled and 56,000 bps when the data compression option is disabled.

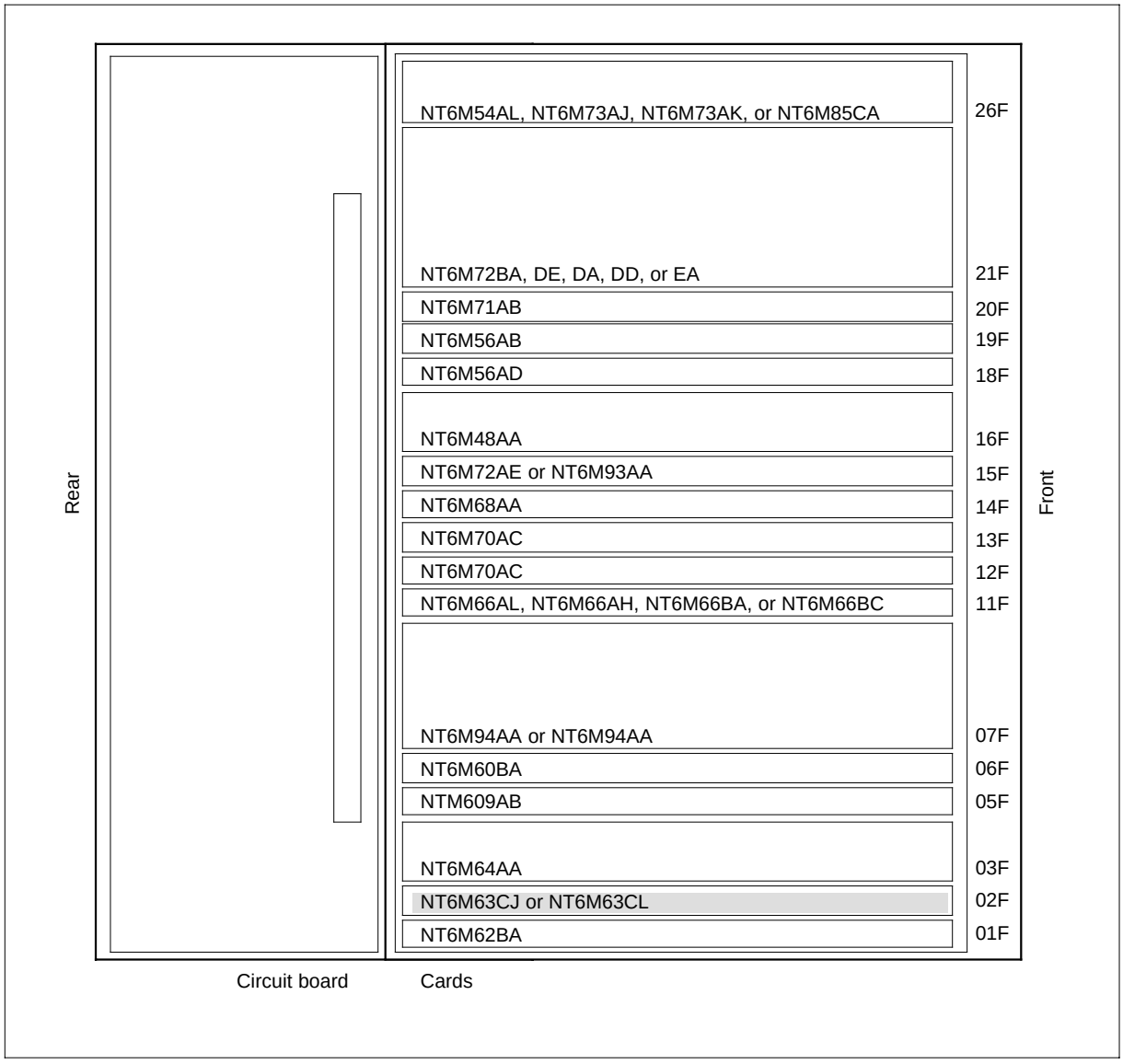
The A chassis and the B chassis of the NT8X48AD appear in the following figures.

NT8X48AD (A shelf design)



NT8X48AD (end)

NT8X48AD (B shelf design)



NT8X49AB

Product description

The digital set interface processor card (DSIP) is the control and maintenance manager for the following:

- DSIP
- parallel serial time switch (PSTS) card (NT8X46)
- digital sets in the SL-100

Location

The NT8X49AB resides in the digital line module (DLM) of the SL-100. The digital line module includes the following cards:

- PSTS card (NT8X46)
- line concentrating module (LCM) processor card (NT6X51)
- digroup control card (NT6X52)

Functional description

The NT8X49AB translates the control messages from the LCM processor card (NT6X51) to the format that the digital sets require. These control messages flow from the LCM processor to the digital set in the receive direction (RCON). These messages flow from the digital sets to the LCM processor in the transmit direction (TCON). The PSTS card (NT8X46) must be present for the NT8X49AB to operate.

Functional blocks

The NT8X49AB consists of the following functional blocks:

- microprocessor
- erasable programmable read-only memory (EPROM)
- random access memory (RAM)
- bus timeout logic
- address decode and control logic
- multifunctional peripheral (MFP)
- message extraction circuit
- RCON interface
- TCON interface

NT8X49AB (continued)

Microprocessor

The Motorola 68020 32-bit microprocessor operates at 12 MHz. A reset circuit in the microprocessor resets important hardware components on the NT8X49AB and the NT8X46. The microprocessor can execute a software reset. This action is like the action of the reset circuits except that the microprocessor does not reset the CPU.

EPROM

The four EPROMs in the NT8X49AB are configured as longword ports with one wait state inserted for each EPROM access. The EPROMs are 8 Kbytes by 8 bits in size.

RAM

The four static RAMs in the NT8X49AB are configured as longword ports with no wait states inserted between access times. The RAMs are 8 Kbytes by 8 bits in size.

Bus timeout logic

The bus timeout logic detects CPU data transfers that are not successful. With failed memory access, the bus timeout logic generates a bus error signal (BERR) after an exact period of time.

Address decode and control logic

The address decode and control logic generates chip selects and transfer acknowledge (DSACKS) signals for the NT8X49AB, NT8X46 and NT8X55. This block checks the alignment of the data ports.

MFP

The MFP block provides general input and output functions and timing functions for the NT8X49AB. The MFP is a Motorola 68901 8-bit peripheral that operates at a rate of 2.5 MHz and has 24 direct-address internal registers.

Message extraction circuit

The message extraction circuit receives signaling bits that the NT8X46 strips from ten 32-channel DS30X data streams. The message extraction circuit assimilates these 320 DS30X signaling bits at the same time. When this block receives a message, the block sends a signal to the MFP. The MFP interrupts the microprocessor.

RCON interface

The RCON interface consists of ten serial links from the LCM processor card (NT6X51). These links provide control and maintenance information to the NT8X49AB and the NT8X46. This interface converts serial data to parallel

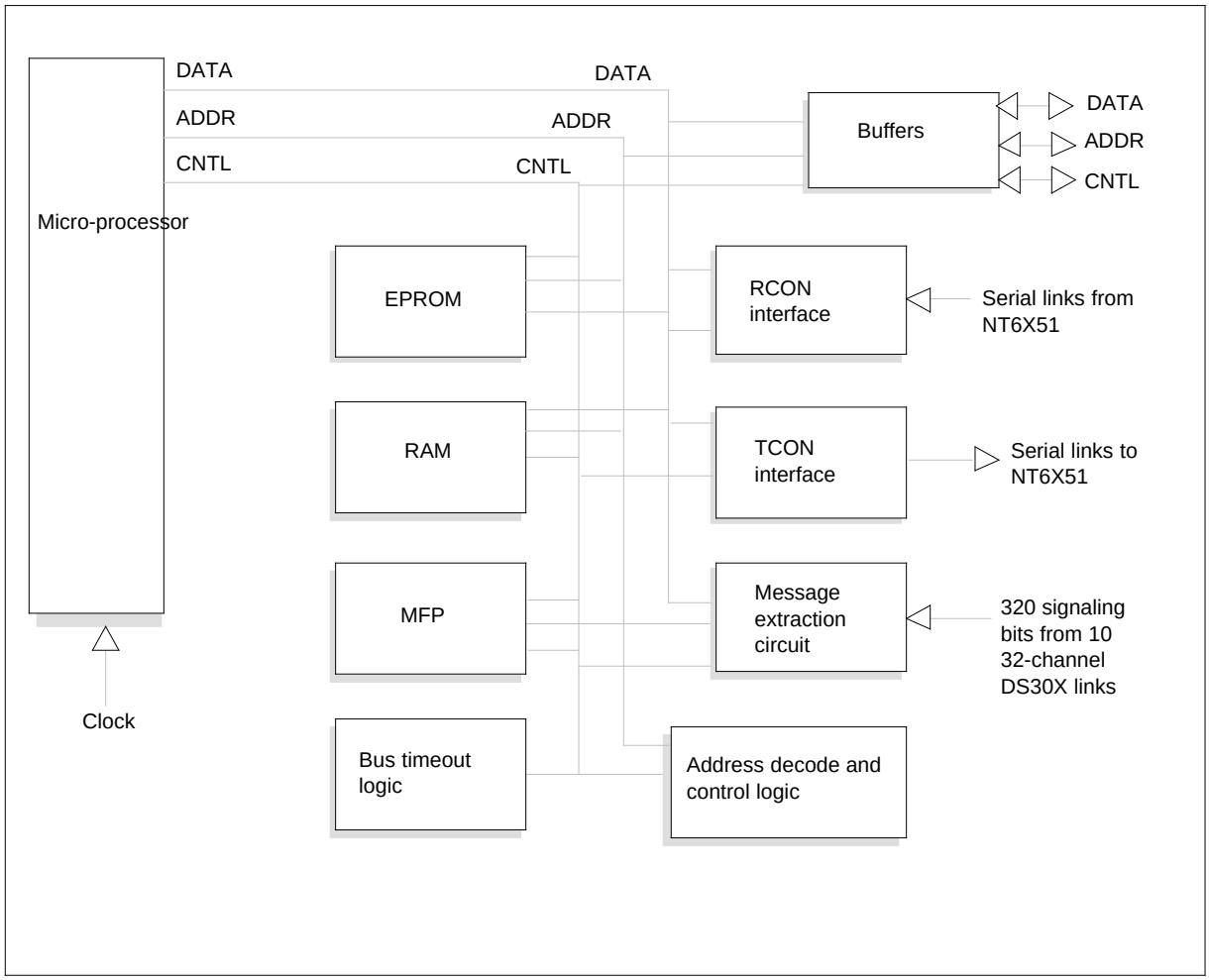
data. The interface also stores the data in a latch until the microprocessor on an interrupt reads the data.

TCON interface

The TCON interface consists of ten serial links to the LCM processor card (NT6X51). These links transmit control and maintenance information to the NT6X51 from NT8X49AB the and the NT8X46. The interface converts parallel data to serial. The interface stores the data in a first-in-first-out (FIFO) output, or in one of two latches until the microprocessor reads the data.

The relationship between the functional blocks appears in the following figure.

NT8X49AB functional block



4 NT9Xnnaa

NT9X01BA through NT9X74BA (continued in Volume 5)

NT9X01BA

Product description

The dual-plane combined core cabinet (DPCC) is a standard DMS SuperNode equipment cabinet. The DPCC contains the DMS-core and the DMS-bus. Copies of the DMS-core and the DMS-bus in two planes makes sure the system is reliable.

The DMS-core provides the central processing. The DMS-core has a computing module (CM) and a system load module (SLM). One shelf can hold two CMs. One shelf can hold two SLMs. Each CM is paired with an SLM. One pair is plane 0 and the other pair is plane 1. Refer to the diagram.

The DMS-bus is the messaging control component of the DMS-SuperNode switch. The DMS-bus contains message switches (MS). Each MS requires a shelf.

Parts

The NT9X01BA has the following parts:

- the NT9X03AA—frame supervisory panel (FSP)
- the NT9X04AE—MS
- the NT9X06AC—CM
- the NT9X07AB—SLM
- the A0323984—core cooling unit (CU)

Frame supervisory panel

The NT9X03AA FSP provides alarm, maintenance and different supervisory functions. The FSP is in the top shelf position in the NT9X01BA. Open the cabinet doors to access the front and rear of the NT9X03AA. A frame light is visible even with closed doors.

Power from the power distribution center frame comes into the FSP. The power distributes to different power supply modules in the cabinet, like the NT9X30AA and NT9X31AA power converters. Power control is in the power supply modules and is separate from the FSP.

Message switch

The NT9X04AE MS controls message flow to and from the CM and the input/output controllers (IOC) and network.

The pair of NT9X04AE MSs is a duplicated DMS-bus. The two MSs operate in a load-sharing mode.

Computing module

The NT9X06AC CM is the central processing unit (CPU) element of the SuperNode switch. The NT9X06AC uses a Motorola 68000-series microprocessor with integrated program and data store. The NT9X06AC can contain a maximum of 256 Mbytes of static random access memory (RAM) (S-RAM).

The duplicated SLMs and the duplicated CMs form the DMS-Core.

The DMS-core performs the following functions:

- controls administration and maintenance functions
- system startup and loading
- downloading and internal software distribution
- facilities management
- collection, storage and output of operational information
- compilation of alarm and statistical information

The seven functional subsystems in the CM are as follows:

- processor/memory
- transmission
- clock
- reset control
- bus termination
- bus extension
- power

The NT9X06AC CM has circuit packs (CP) on the front of the shelf with corresponding paddle boards in the rear. The CPs share a common bus with the paddle boards.

The two CMs operate by the same method at the same time. Each CM can continue to operate on a full message load alone. Message loss or service degradation does not occur.

An NT9X0601 shelf assembly holds the two NT9X06AC CMs.

System load module

The NT9X07AB SLM is a mass storage system to store office images. For redundancy, each cabinet provides two SLMs. Each CM processor has one

NT9X01BA (continued)

SLM. The port crossover bus provides both processors with access to each SLM.

Core cooling unit

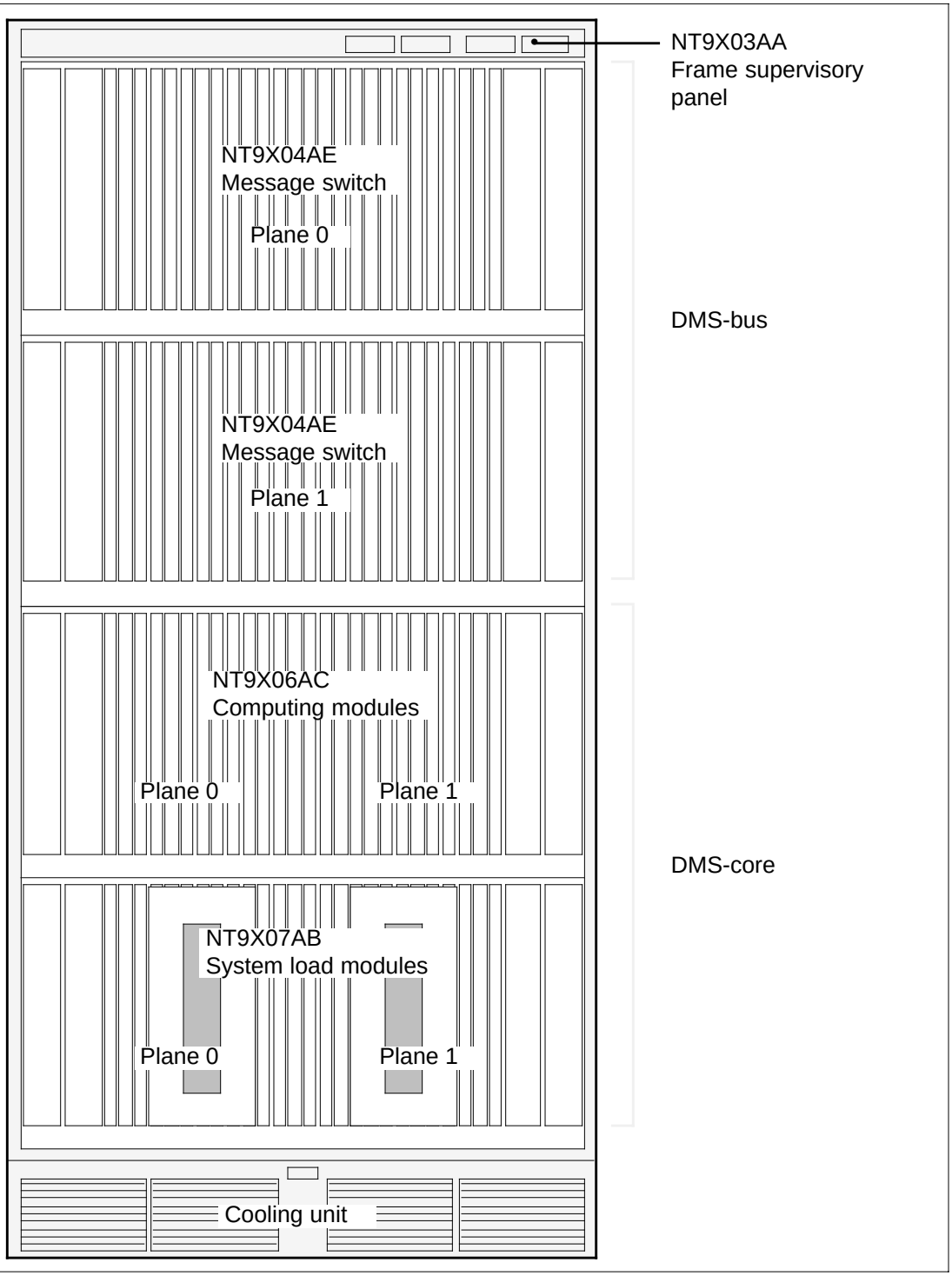
The CU provides mechanical ventilation for equipment that the DPCC cabinet contains.

Design

The design of the NT9X01BA appears in the following diagram.

NT9X01BA (end)

NT9X01BA parts



NT9X01DA

Product description

The NT9X01DA SuperNode cabinet contains a pair of enhanced network (ENET) shelves and a standard DMS-core. One ENET shelf is for plane 0 and one for plane 1. The DMS-core has a pair of computing modules (CM) and a pair of system load modules (SLM).

One shelf has two CMs. One shelf has two SLMs. Each CM is a pair with an SLM. One pair is plane 0 and the other pair is plane 1.

The ENET shelves provide high-speed interfaces between the DMS-core and peripherals. The ENET uses fiber optic connections to the DMS-core and fiber peripheral modules (PM).

Parts

The NT9X01DA has the following parts:

- the A0323984—core cooling unit (CU)
- the NT9X03AA—frame supervisory panel (FSP)
- the NT9X0801—simplex network shelf
- the NT9X0606—CM
- the NT9X0703—SLM

Core cooling unit

The A0323984 core CU provides mechanical ventilation for equipment in the SuperNode cabinet.

Frame supervisory panel

The NT9X03AA FSP provides alarm, maintenance and different supervisory functions. The FSP is in the top shelf position in the NT9X01AA. Open the cabinet doors to access the front and rear of the NT9X03AA. A frame light is visible even with closed doors.

Power from the power distribution center frame comes into the FSP. The power distributes to different power supply modules in the cabinet, like the NT9X30AA and NT9X31AA power converters. Power control is in the power supply modules and is separate from the FSP

Simplex network shelf

The NT9X0801 simplex network shelf concentrates and distributes messages to control message flow. The simplex network shelf allows parts to communicate directly with each other.

The pair of NT9X0801s is a duplicated ENET network interface. The duplication of shelves makes sure the system is reliable. The two ENET shelves operate by the same method at the same time. Each one can continue to operate on a full message load alone. Message loss or service degradation does not occur.

Computing module

The NT9X0606 CM is the CPU element of the SuperNode switch. The NT9X0606 uses a Motorola 68000-series microprocessor with integrated program and data store. The NT9X0606 can contain a maximum of 60 Mbytes of dynamic random access memory (RAM) (D-RAM).

The duplicated SLMs and the duplicated CMs form the DMS-core.

The DMS-core performs these functions:

- controls administration and maintenance functions
- system startup and loading
- downloading and internal software distribution
- management of the Common Channel Signaling 7 (CCS7) network
- facilities management
- collection, storage and output of operational information
- compilation of alarm and statistical information
- update of global title translation (GTT) and routing information

The seven functional subsystems in the CM are as follows:

- processor/memory
- transmission
- clock
- reset control
- bus termination
- bus extension
- power

The NT9X0606 CM has circuit packs (CP) on the front of the shelf with corresponding paddle boards in the rear. The CPs share a common bus with the paddle boards.

NT9X01DA (continued)

The two CMs operate by the same method at the same time. Each CM can continue to operate on a full message load alone. Message loss or service degradation does not occur.

An NT9X0601 shelf assembly holds the two NT9X0606 CMs.

System load module

The NT9X0703 SLM is the program store element of the DMS-core in the SuperNode switch. The SLM provides the bootstrapping and operational code for the CPU in the CM.

The two SLMs operate by the same method at the same time. Each SLM can continue to operate on a full message load alone. Message loss or service degradation does not occur.

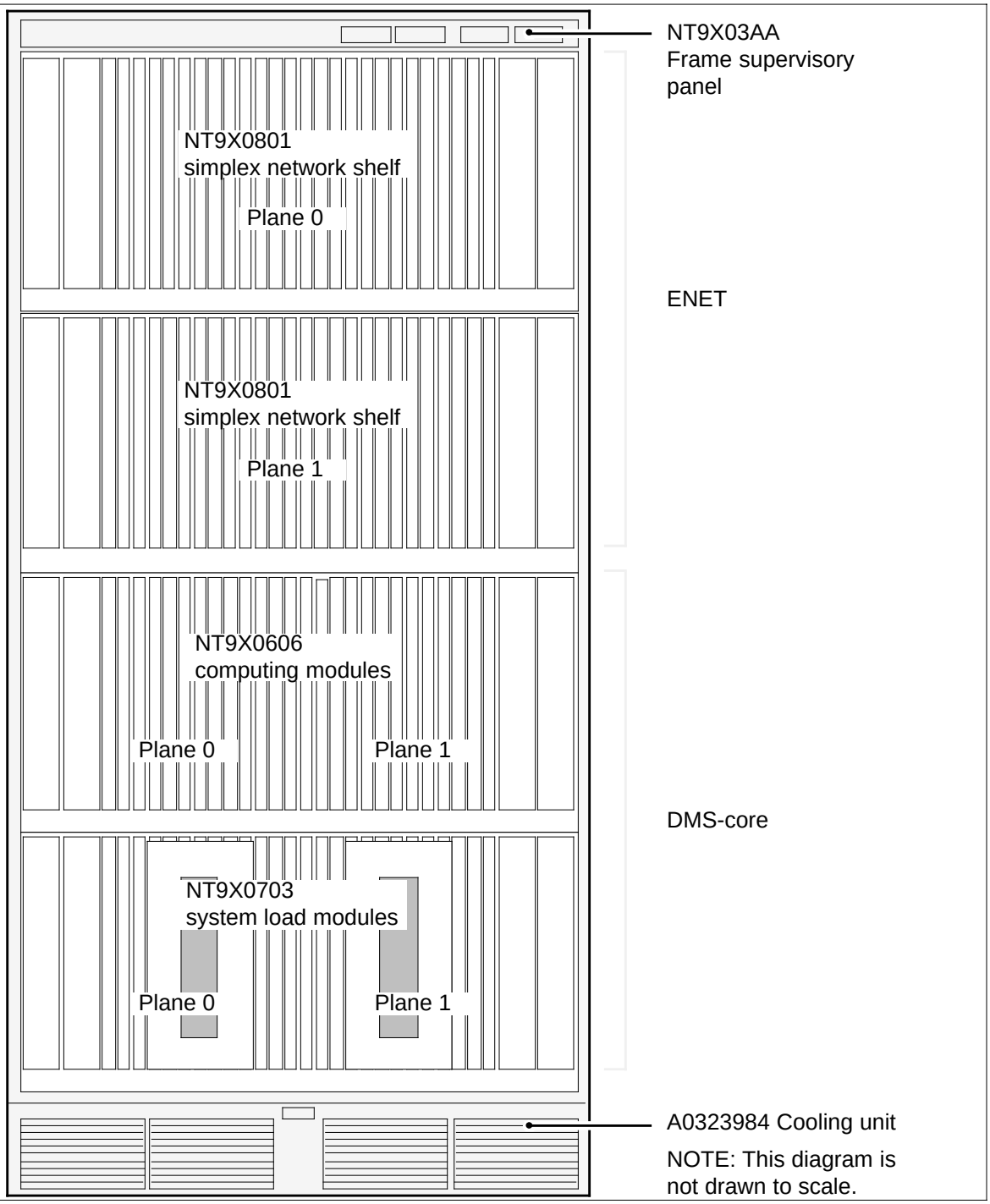
An NT9X0701 shelf assembly holds the two NT9X0703 SLMs.

Design

The design of the NT9X01DA appears in the following diagram.

NT9X01DA (end)

NT9X01DA parts



NT9X01JA

Description

The EMI dual-plane combined core cabinet (DPCC) is a standard DMS SuperNode equipment cabinet. The DPCC houses the DMS-core and the DMS-bus. Both the DMS-core and the DMS-bus are duplicated in two planes. This condition makes sure the system is reliable.

The NT9X01JA is an EMI-resistant version of the NT9X01BA DPCC.

The DMS-core provides the central processing. The DMS-core contains a computing module (CM) and a system load module (SLM). Two CMs are mounted on a single shelf and two of the SLMs are mounted on a single shelf. The system pairs each CM with an SLM. The system assigns the a pair to plane 0 and the other pair to plane 1.

The DMS-bus is the messaging control component of the DMS-SuperNode switch and contains a message switch (MS). Each MS requires a shelf.

Parts

The NT9X01JA cabinet contains the following parts:

- A0323984—Core cooling unit (CU)
- NT9X03AA—Frame supervisory panel (FSP)
- NT9X04AH—Message switch (MS)
- NT9X06AD—Computing module (CM)
- NT9X07AB—System load module (SLM)

Core cooling unit

The core CU provides mechanical ventilation for equipment. The equipment is in the DPCC cabinet.

Frame supervisory panel

The NT9X03AA FSP provides alarm, maintenance, and different supervisory functions. The FSP is in the top shelf position of the NT9X01JA. Open the cabinet doors to access the front and rear of the NT9X03AA. An associated frame light remains visible when the doors are closed.

The power distribution center frame sends power to the FSP. The FSP distributes power to different power supply modules within the cabinet. Examples of the modules includes the NT9X30AA and NT9X31AA power converters. All power control is in the power supply modules. The power control functions are independent of the FSP.

Message switch

The NT9X04AH MS controls message flow. This switching concentrates and distributes messages and allow the parts to communicate directly with each other.

The pair of NT9X04AH MSs comprise a duplicated DMS-bus. The duplicate shelves enhances system reliability. The two MSs operate together and use the same method to operate. Either MS can operate alone with a full message load without message loss or service degradation.

Computing module

The NT9X06AD CM is the CPU element of the SuperNode switch. The NT9X06AD uses a Motorola 68000-series microprocessor with integrated program and data store. The NT9X06AD can have a maximum of 60 Mbytes of RAM.

Along with the duplicated SLMs, the duplicated CMs form the DMS-core.

The DMS-core performs these functions:

- control of administration and maintenance functions
- system start up and loading
- downloading and internal software distribution
- management of the CCS7 network
- facilities management
- collection, storage and output of operational information
- compile alarm and statistical information
- update of global title translation (GTT) and routing information

There are seven operating subsystems in the CM. These subsystems are processor/memory, transmission, clock, reset control, bus termination, bus extension, and power.

The NT9X06AD CM is equipped with circuit packs (CP) on the front of the shelf with corresponding paddle boards in the rear. The CP shares a common bus with the paddle boards.

Both of the CMs use the same method to operate. Either CM can operate alone with a full message load without message loss or service degradation.

The two NT9X06AD CMs mount on a NT9X0601 shelf assembly.

NT9X01JA (continued)

System load module

The NT9X07AB SLM is the program store element of the DMS-core in the SuperNode switch. The SLM provides the bootstrap and operational code for the CPU in the CM.

The two SLMs use the same method to operate. Either SLM can operate alone with a full message load without message loss or service degradation.

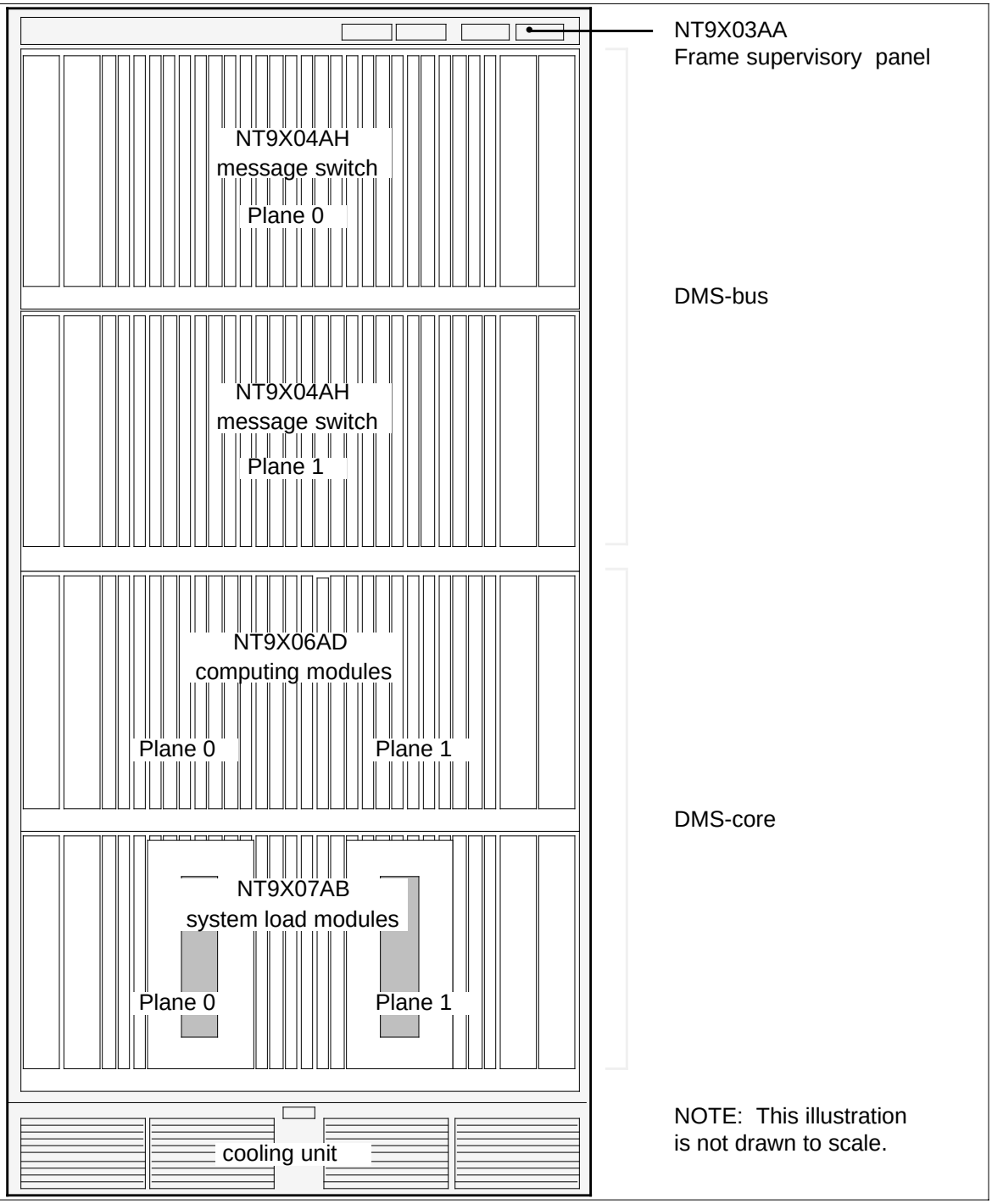
The two NT9X07AB SLMs mount on a NT9X0701 shelf assembly.

Design

The design of the NT9X01JA appears in the following figure.

NT9X01JA (end)

NT9X01JA parts



NT9X01JB

Description

The EMI dual-plane combined core cabinet (DPCC) is a standard DMS SuperNode equipment cabinet that houses the DMS-core and the DMS-bus. Both the DMS-core and the DMS-bus are duplicated in two planes to enhance system reliability.

The NT9X01JB is an EMI-resistant version of the NT9X01BA DPCC.

The DMS-core provides the central processing and contains a computing module (CM) and a system load module (SLM). Two CMs are mounted on a single shelf and both of the SLMs are mounted on a single shelf. Each CM has an SLM pair. The system assigns one of the pairs to plane 0 and the other pair to plane 1.

The DMS-bus is the messaging control component of the DMS SuperNode switch, composed of a message switch (MS). Each MS requires a shelf.

Parts

The NT9X01JB cabinet contains the following parts:

- A0323984—core cooling unit, -48 Vdc
- A0382102—core cooling unit, -60 Vdc
- NT9X03AA—SuperNode frame supervisory panel (FSP), -48 Vdc
- NT9X03BA—SuperNode frame supervisory panel, -60 Vdc
- NT9X04AL—message switch common fill
- NT9X06AF—computing module processor shelf fill
- NT9X07AC—system load module

Core cooling unit

The core cooling unit (CU) provides mechanical ventilation for equipment housed in the DPCC cabinet. Power requirements determine if the CU can handle dc voltages of -48V (A0323984) or -60V (A0382102).

SuperNode frame supervisory panel

The NT9X03AA, -48V dc or NT9X03BA, -60V dc SuperNode frame supervisory panel (FSP) provides alarm, maintenance and other supervisory functions. The FSP is in the top shelf position in the . Open the cabinet doors to access or view the front and rear faces of the NT9X03AA or NT9X03BA. A frame alarm light is in the cabinet. The NT9X01JB is visible when the cabinet doors are closed.

Power from the power distribution center frame comes into the FSP. Power distribution occurs to different power supply modules in the cabinet, like the NT9X30AA and NT9X31AA power converters. The power supply modules contain all power control. The power controls are independent of the FSP.

Message switch common fill

The NT9X04AL message switch common fill concentrates and distributes messages to control message flow. The NT9X04AL message switch common fill allows components to communicate directly with each other.

The NT9X04AL MS pair comprises a duplicated DMS-bus. The duplicate shelves enhance system reliability. The MS pair operates together and use the same method to operate. A single MS can operate a full message load without message loss or service degradation.

Computing module processor shelf fill

The NT9X06AF CM is the CPU element of the SuperNode switch. The NT9X06AF uses a 68020-, 68030-, or 88000 BRISC-series microprocessor along with integrated program and data store. The NT9X06AD can have a maximum of 240 Mbytes of RAM.

The duplicate SLMs and CMs form the DMS-core.

The DMS-core performs these functions:

- control of administration and maintenance functions
- system startup and loading
- downloading and internal software distribution
- management of the CCS7 network
- facilities management
- collection, storage, and output of operational information
- compile alarm and statistical information
- update of global title translation (GTT) and routing information

The seven subsystems in the CM are processor and memory, transmission, clock, reset control, bus termination, bus extension, and power.

The NT9X06AF CM has cards on the front of the shelf with associated paddle boards in the rear. The cards share a common bus with the paddle boards.

Both of the CMs use the same method to operate. Either CM can operate alone with a full message load without message loss or service degradation.

NT9X01JB (continued)

The two NT9X06AF CMs mount on an NT9X0605 shelf assembly.

System load module

The NT9X07AB SLM is the program store element of the DMS-core in the SuperNode switch. The SLM provides the bootstrap and operational code for the CPU in the CM.

The SLM is in a single unit that is easy to replace. The unit has a 133-mm (5.25 in.) hard disk drive, a 6 mm (.25 in.) streaming cartridge tape drive, and controller circuit pack. The SLM hard disk has a capacity of 600 Mbytes. The tape cartridge has a capacity of 150 Mbytes.

Both of the SLMs use the same method to operate. One SLM can operate alone with a full message load without message loss or service degradation.

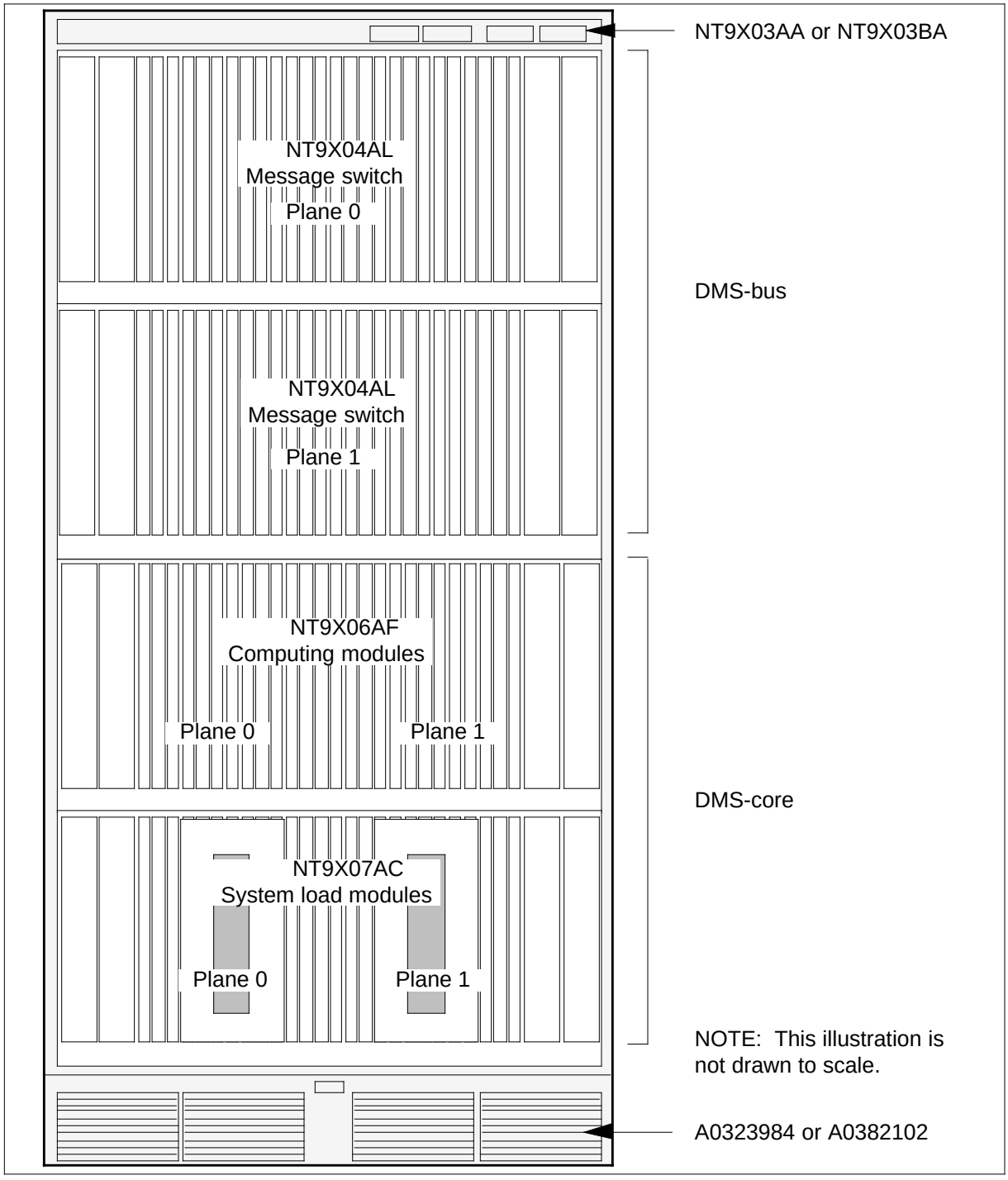
The two NT9X07AB SLMs mount on an NT9X0702 shelf assembly.

Design

The design of the NT9X01JB appears in the following figure.

NT9X01JB (end)

NT9X01JB parts



NT9X01MB

Product description

The SuperNode SE cabinet combines multiple functions in a single cabinet. These functions are combined computing module and system load module (CM/SLM), DMS-bus, link interface unit (LIU), and network functionality.

The cabinet merges the SuperNode functions of the following to a three-shelf control complex:

- CM
- SLM
- link peripheral processor (LPP)
- ENET
- DMS-bus

The cabinet performs the merge when the SuperNode SE cabinet is equipped with the 16 kbyte enhanced network (ENET) shelf. The merge reduces the amount of hardware required for small office applications.

The SuperNode SE cabinet handles address applications for end offices with 2000 to 12 000 lines. The SuperNode SE cabinet can expand to a maximum of 20 000 lines to include services like plain ordinary telephone service (POTS) and integrated services digital network (ISDN).

The SuperNode SE cabinet provides the following:

- completely duplicated and synchronized CM and SLM on one shelf
- duplex 16 kbyte ENET on one shelf with integrated LIU slots for two CCS7 links
- available LPP link interface shelf (LIS), which can provide an additional 12 LIUs
- duplicated, load-sharing message switches (DMS-bus) on a single shelf

The SuperNode SE cabinet supports the dual-shelf network and is compatible with current and future peripherals. The SuperNode SE cabinet ENET provides the ability to use fiber, copper, or a combination of the two interfaces to the peripheral modules.

Parts

The SuperNode SE cabinet contains the following parts:

- A0323984—cooling unit (CU)
- NT9X03AA—frame supervisory panel (FSP)
- NT9X0470—combined message switch
- NT9X0610—CM/SLM shelf
- NT9X7204—link interface shelf (LIS) (optional)
- LIU
- NT9X0810—16 kbyte ENET shelf (optional)

Frame supervisory panel

The NT9X03AA FSP provides alarm, maintenance and different supervisory functions. The FSP is in the top shelf position in the NT9X01BA. Open cabinet doors to access or view the front and rear faces of the NT9X03AA. A frame alarm light is in the cabinet. The light is visible with the cabinet doors closed.

Power from the power distribution center frame goes to the FSP. The FSP distributes the power to power supply modules, like the NT9X30AA and NT9X31AA power converters, in the cabinet. The power supply modules contain the power control. The power control is separate from the FSP.

Combined message switch

The SuperNode SE, with standard SuperNode circuit packs (CP) and paddle boards, reduces from two shelves to one for the message switch (MS) function. As a result, the port capacity is less than a standard SuperNode MS.

The SuperNode SE MS provides seven port cards on a side. One port card slot is for computer module intercommunications/ENET (CMIC/ENET) interfaces. Another port card is for input/output controller/intermessage switch link (IOC/IML) interfaces. Five provisionable port card slots on each SuperNode SE MS remain.

Backplane functionality for the MS shelf is new in the SuperNode SE cabinet. A direct link between an LIS and the MS is available.

CM/SLM shelf

The CM/SLM shelf combines the SuperNode type CMs and SLMs on a single shelf. The CMs work on this shelf in the same way as in the SuperNode. Under normal conditions, the duplicate CMs operate in synchronous match mode. In this mode, the controlling CPU is the Active and the mate is the Inactive.

NT9X01MB (continued)

The CMs use fiber CMIC links to connect to the MSs.

The SuperNode SE cabinet uses the same memory boards as the SuperNode-based switch. These boards provide for 24 Mbyte of memory on a board. The SuperNode SE cabinet provides the ability to provision a maximum of five memory packs on a side. For the specified 24 Mbyte memory circuit pack the ability amounts to 120 Mbyte. The 120 Mbyte includes an 8 Mbyte spare memory module,.

The SLMs provide the mass storage media for the SuperNode SE cabinet with a hard disk and streaming tape. The SuperNode SE cabinet uses the 5-slot SLM1A. The SLMA1 has a 340 Mbyte 89 mm (3.5 in.) hard disk drive and a 150-Mbyte tape unit.

Link interface shelf

This shelf is optional. In addition to the minimum two LIUs mounted on the 16 kbyte ENET shelf, the LIS can provide a maximum of 12 additional LIUs.

The SuperNode SE cabinet supports the same LIU ability as the NT9X70 SuperNode LPP. The SuperNode SE cabinet supports external fiber LISs in addition to the internal, copper-connected LIS. When an external fiber LIS is available, the number of CCS7 LIUs cannot exceed 24.

The SuperNode SE cabinet supports the provisioning of LPPs where required, to the ability of the SuperNode SE MS.

16 kbyte ENET shelf

The ENET shelf is optional. The network in use can be the current junctor network/dual shelf network (JNET/DSN) or the 16 kbyte SuperNode SE ENET. The JNET is in a separate frame or frames. A maximum of eight network modules (NM) normally can be provisioned. This number can increase to ten in module structure list (MSL) applications.

The SuperNode SE cabinet is compatible with each of the following JNET types: 0X- -, 5X- -, 7X- -, and 8X- -.

The SuperNode SE network (16 kbyte ENET) is a dual plane network. Each plane connects to the two MSs for control messaging. The rate of switching for this network is 64 kbit/s for each channel. Each network plane provides a maximum of 16 kbyte channels of non-blocking, constant delay switching. The SuperNode SE ENET is a junctorless, non-blocking network that provides full availability.

The 16 kbyte ENET provides the ability to support connections with rates greater than 64 kbit/s. The ENET switches groups of multiple channels of the

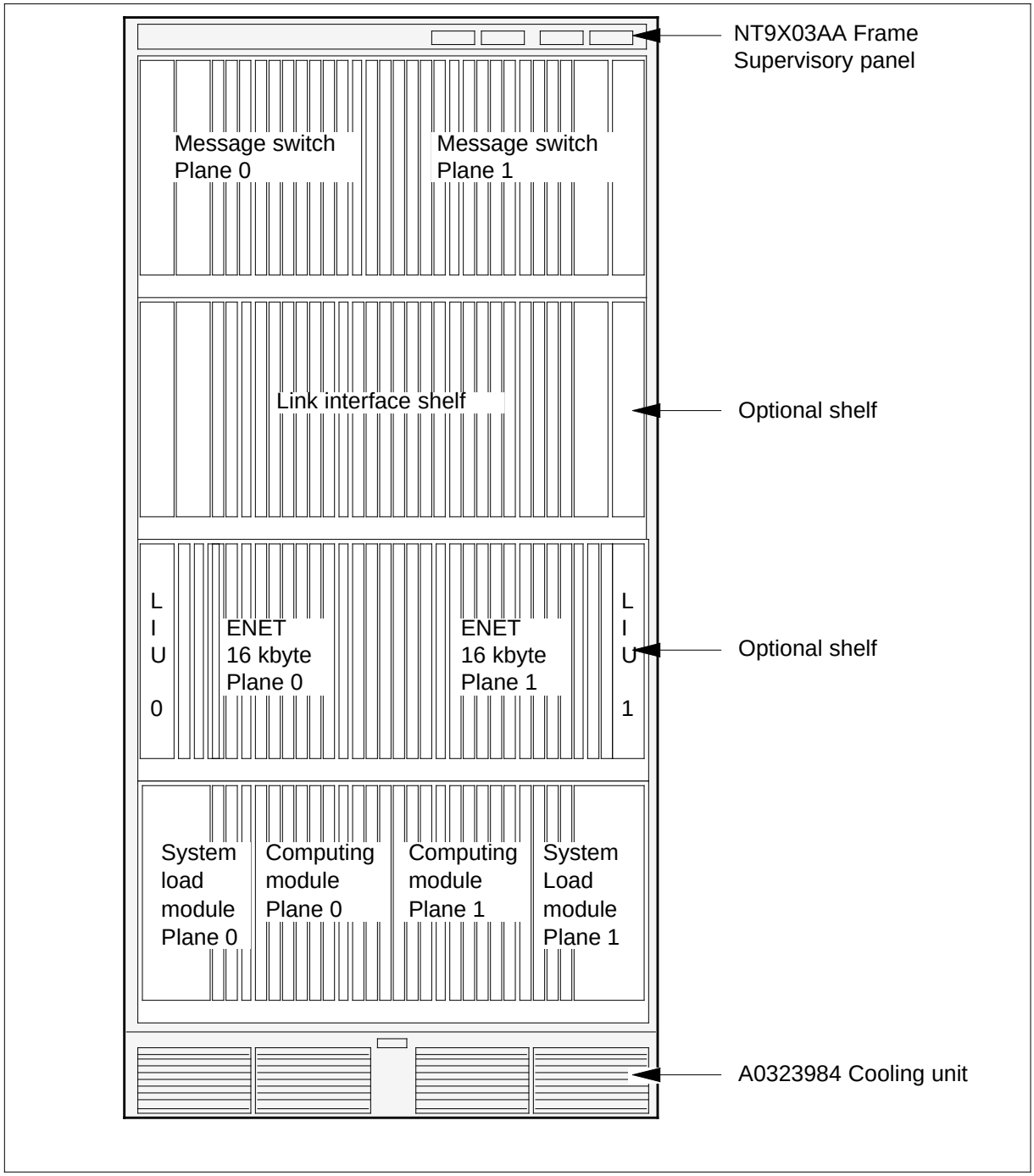
basic rate. The ENET performs switching when the ENET provides a constant switching delay for all channels across the network. This function is the same as the function that the SuperNode 128 kbyte ENET provides.

Design

The design of the NT9X01MB appears in the following figure.

NT9X01MB (end)

NT9X01MB parts



NT9X03AA

Product description

The NT9X03AA frame supervisory panel (FSP) performs alarm, maintenance and different supervisory functions. On a SuperNode cabinet, the FSP is in the top shelf position.

Power from the power distribution center comes to the FSP. The FSP distributes the power to power supply modules in the cabinet. The power supply modules contain the power control. The power control is separate from the FSP.

To access or view the front and rear faces of the NT9X03AA, open the cabinet doors. A frame alarm light is in the cabinet. The light is visible with the cabinet doors closed.

Parts

The NT9X03AA consists of an NT0X91AA alarm and converter drive and an NT6X36AF ARLB FSP alarm circuit pack (CP).

NT9X03AA (continued)

Design

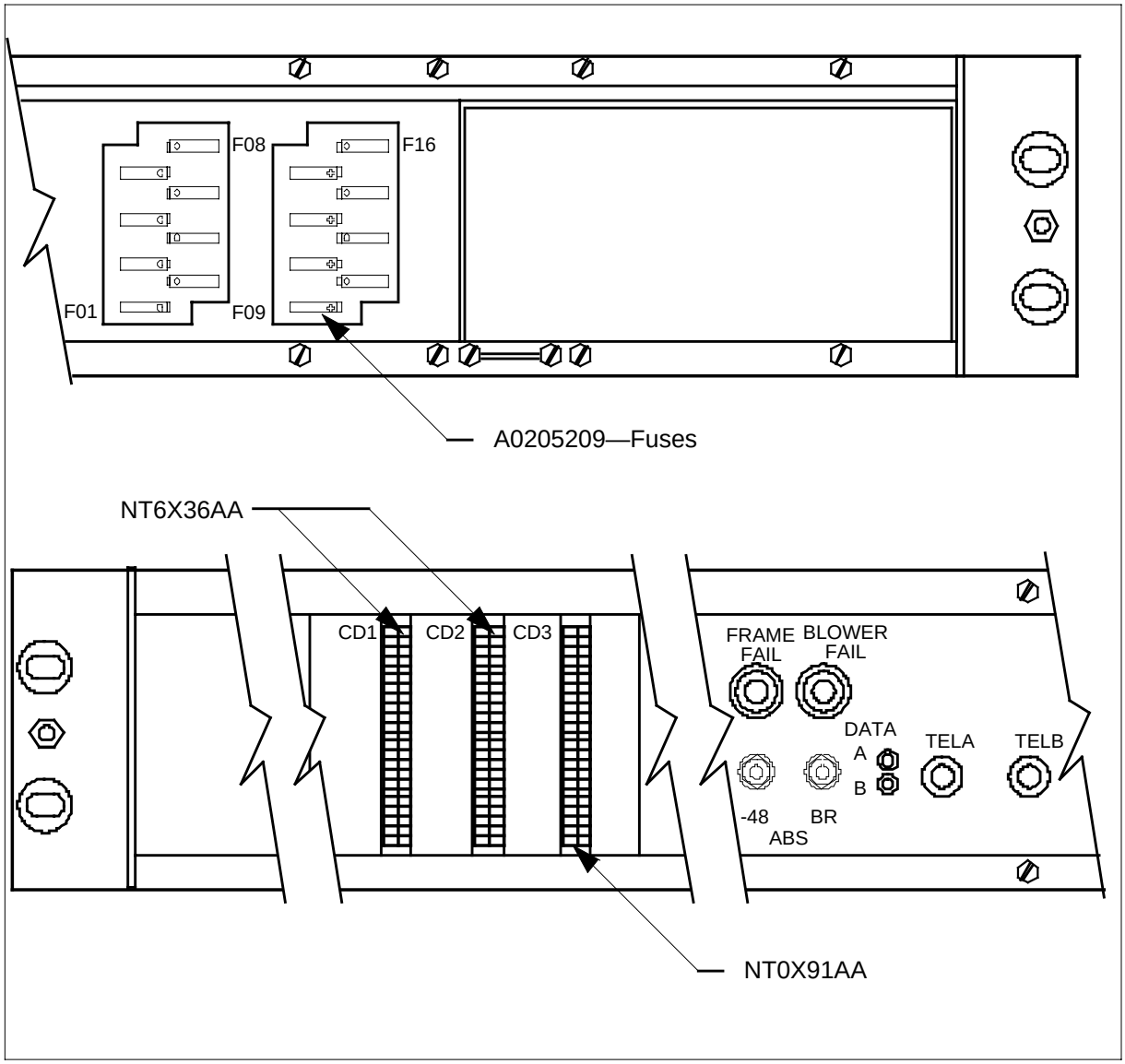
The parts of the NT9X03AA appear in the following table.

NT9X03AA parts

PEC	Slot	Description
NT0X91AA	n/a	*Alarm and converter drive circuit pack* The NT0X91AA regulates the output voltage to -48V dc. The NT0X91AA provides alarm output when the input voltage from the office battery deviates from requirements (-6V/+8V).
NT6X36AF	n/a	*ARLB FSP alarm circuit pack* The NT6X36AF monitors converters connected to the NT6X36AF. The NT6X36AF replaces the NT6X36AA CP, which provides the added ability of automatic recovery from low battery (ARLB). This ARLB function identifies the difference between converter failure and low office battery supply. Low battery conditions (less than 41.0V) disable the trip feature. The converters can shut down. The converters do not trip the circuit breakers. When the office battery supply regains power (above 45.0V), this condition enables the trip feature. The system can continue to monitor the converters.

The front and rear surfaces of the NT9X03AA appear in the following figure.

NT9X03AA front view



NT9X04AA

Product description

The message switch (MS) is the messaging component of SuperNode. The MS concentrates and distributes messages in the DMS-100 system. The MS provides larger message traffic capacity and larger message length than the central message controller.

The NT9X04AA also provides the central clock source for the DMS-100 office.

Like the computing module (CM), the MS duplicates. The two units operate in load-sharing mode.

The NT9X04AA has circuit packs (CP) on the front of the shelf and corresponding paddle cards on the rear. The CPs and paddle cards share a bus.

The NT9X04AA supports two types of link interfaces:

- the standard DS30 twisted-pair link to current network modules and input/output controllers (IOC)
- the DS512 fiber link to CMs and enhanced network (ENET)

The NT9X04AA accommodates two major internal buses:

- processing unit bus (P-bus), which communicates with the other components of the MS
- transaction bus (T-bus), on which messages transmit from port to port. This bus is synchronous and operates at 4.096 MHz

Parts

The NT9X04AA shelf contains the following parts:

- NT9X13DA—CPU 16-MHz circuit pack (CP)
- NT9X14AA—4 Mbyte memory CP
- NT9X15AA—Mapper CP
- NT9X17AA—MS 4-port CP
- NT9X17BA—MS 32-port CP
- NT9X17CA—MS 128-port CP
- NT9X19AA—Filler CP
- NT9X19BA—Filler paddle board (PB)
- NT9X20AA—DS512 PB

- NT9X23AA—DS30 4-port PB
- NT9X25AA—MS port extender PB
- NT9X26AB—Remote terminal interface (RTIF) PB
- NT9X30AA—Power converter, +5V CP
- NT9X31AA—Power converter, -5V CP
- NT9X32AA—MS load PB
- NT9X49CA—MS P-bus terminator CP
- NT9X52AA—T-bus access CP
- NT9X53AA—MS clock CP
- NT9X54AA—MS external clock interface PB

Design

The parts of the NT9X04AA appear in the following table.

NT9X04AA parts (Sheet 1 of 5)

PEC	Slot	Description
NT9X13DA	9F	*CPU card* The NT9X13DA is a 16 Mhz MC68020 CPU. The NT9X13DA offers memory access and write protection. The NT9X13DA uses a 4 kbyte data cache. The NT9X13DA uses a dual channel serial communications controller.
NT9X14AA	10F	*4 Mbyte memory card* The NT9X14AA consists of two memory modules. Each memory module has 2 Mbytes of dynamic RAM (DRAM). Each NT9X14AA memory module has error checking and correction. The NT9X14AA uses a 40 bit memory width. The 40 bit memory consists of 32 bits of data, 7 check bits, and 1 parity bit.

NT9X04AA (continued)

NT9X04AA parts (Sheet 2 of 5)

PEC	Slot	Description
NT9X15AA	11F	*Mapper circuit pack* The NT9X15AA is a specialized memory card that translates the software address to a physical address for routing. The CPU provides the software address. The NT9X15AA provides route state information. This route state information is route open or closed.
NT9X17AA	30F-31F Provisionable 12F-29F	*MS 4-port circuit pack (universal port card)* The NT9X17AA provides a data path for messaging between the MS and four external links. The NT9X17AA uses the T-bus to provide the data path.
NT9X17BA	Provisionable 12F-29F	*MS 32-port circuit pack* The NT9X17BA provides 32 logically separate ports. Each port corresponds to one separately addressable T-bus transceiver. Each port can handle one logical message path. Each NT9X17BA connects to a link interface paddle board through two 4.096 MHz 8 bit data buses. These two data buses are the shorting bus (S-bus).
NT9X17CA	Provisionable 12F-29F	*MS 128-port circuit pack* The NT9X17CA provides 128 logically separate ports. Each port corresponds to one separately addressable T-bus transceiver. Each port can handle one logical message path. Each NT9X17CA connects to a link interface paddle board through two 4.096-MHz 8-bit data buses. These two data buses are the S-bus.
NT9X19AA	12F-29F	*Filler circuit pack* The NT9X19AA fills in CP slots that are not used.

NT9X04AA parts (Sheet 3 of 5)

PEC	Slot	Description
NT9X19BA	11R-32R	*Filler paddle board* The NT9X19BA fills in PB slots that are not used.
NT9X20AA	30R-31R Provisionable 12R-27R	*DS512 paddle board* The NT9X20AA provides an interface between the 9X12 CPU port card and the fiber link to the CM. The NT9X20AA also performs 10 bit to 12 bit conversion.
NT9X23AA	Provisionable 12R-29R	*DS30 4-port paddle board* The NT9X23AA provides an interface between a parallel 4.096 MHz backplane data bus and the twisted-pair transmission cables associated with four DS30 links. The NT9X23AA performs the following secondary functions: • transmits out-of-band (OOB) data • receives OOB data • provisions a reference frame pulse extracted from the link The NT9X23AA is used with the NT9X17 MS 4-port card.
NT9X25AA	Provisionable 12R-27R	*MS port expander circuit board* The NT9X25AA connects the DS30 or DS512 links to port cards (NT9X17CA) on the MS shelf through the S-bus. The NT9X25AA connects the S-bus of slot N to the S-bus of slot N+1. An NT9X25BA card terminates the chain. The NT9X25AA is for use between an NT9X20BB and a NT9X25BA in the S-bus daisy chain. The NT9X25AA allows a maximum of four NT9X17CA circuit packs to share a single NT9X20BB DS512 MSEN PB.

NT9X04AA (continued)

NT9X04AA parts (Sheet 4 of 5)

PEC	Slot	Description
NT9X26AB	9R	*Remote terminal interface (RTIF) paddle board* The NT9X26AB monitors the incoming terminal and remote modem line for key words. The NT9X26AB provides a primitive person-machine interface when the CPU does not function. Used for maintenance.
NT9X30AA	4F, 36F	*Power converter, +5V circuit pack* The NT9X30AA provides an output of +5.2V ±2% at the minimum of 0A to the maximum of 20A to the CP on the NT9X04AA shelf.
NT9X31AA	1F, 33F	*Power converter, -5V circuit pack* The NT9X30AA provides an output of -5.2V ±2% at the minimum of 0A to the maximum of 20A to the CP on the NT9X04AA shelf.
NT9X32AA	7R, 10R, 12R-29R	*DMS bus load paddle board* The NT9X32AA guarantees a constant load distribution on the main clock and frame pulse signals that drive the shelf. This load distribution is separate from the number of cards or shelf type. The shelf type can be master of extension.
NT9X49CA	32F	*MS P-bus terminator circuit pack* The NT9X49CA provides termination for MS backplane tracks that the MS processor uses. The NT9X49CA provides a time-out on the MS T-bus.
NT9X52AA	7F	*T-bus access circuit pack* The NT9X52AA interfaces the P-bus with the T-bus. This interface allows the MS processor to receive and transmit messages on the T-bus.

NT9X04AA (continued)

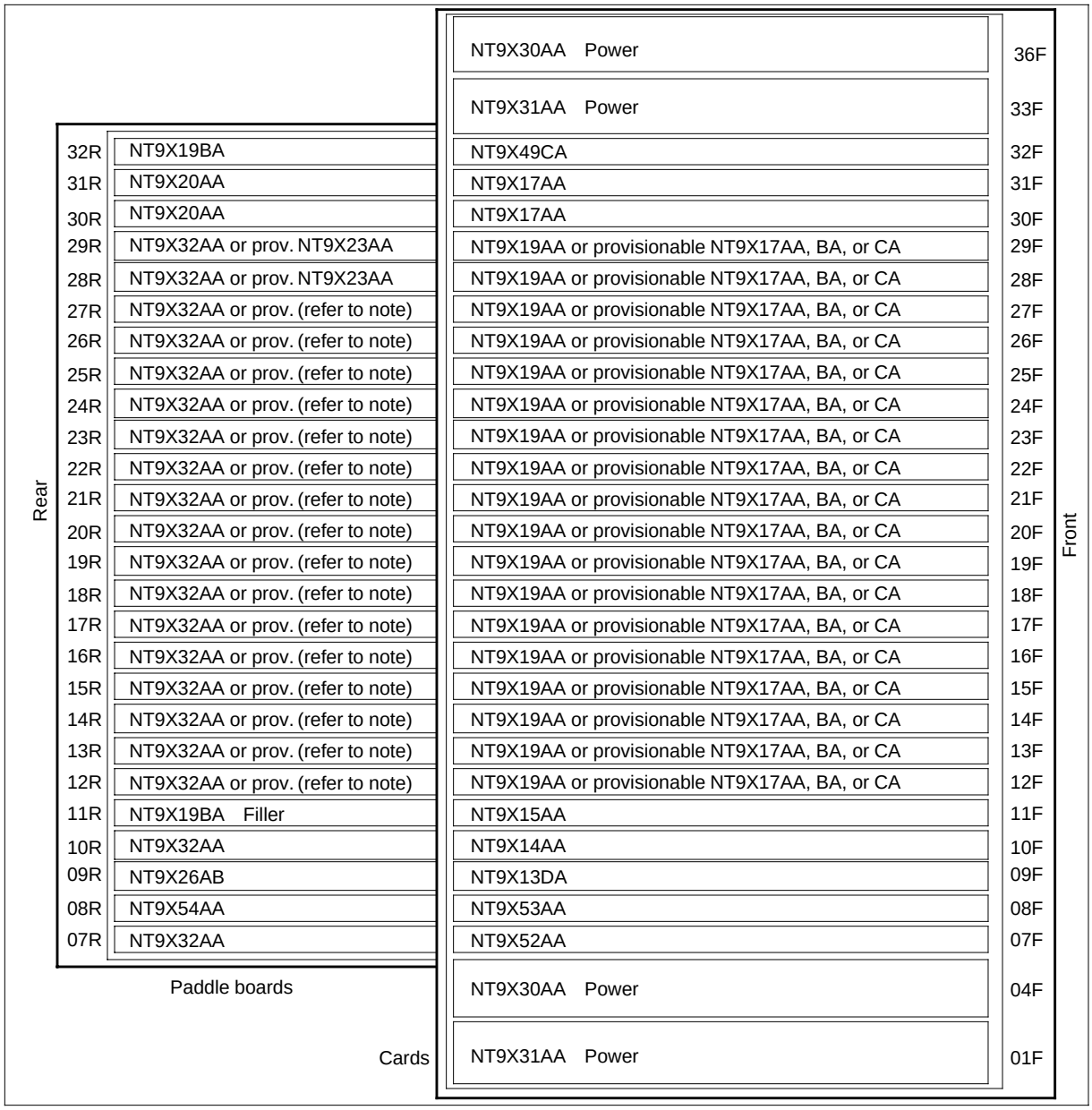
NT9X04AA parts (Sheet 5 of 5)

PEC	Slot	Description
NT9X53AA	8F	*MS clock circuit pack* The clock subsystem consists of the NT9X54AA and the NT9X53AA. This subsystem provides the clock source for the DMS-100 SuperNode system and the subsystem clock for the MS T-bus.
NT9X54AA	8R	*MS external clock interface paddle board* The NT9X54AA is the MS external clock interface PB that interfaces the NT9X53AA clock with the DMS-100 system. The clock subsystem consists of the NT9X53AA and this CP. This subsystem provides the clock source for the DMS-100 SuperNode system.

The design of the NT9X04AA appears in the following figure.

NT9X04AA (end)

NT9X04AA design



NT9X04AB

Product description

The message switch (MS) is the messaging component of SuperNode. The MS concentrates and distributes messages in the DMS-100 system. The NT9X04AB differs from the NT9X04AA. The AB shelf employs NT9X14BB 6 Mbyte memory cards with a handshake override feature. The AB shelf does not employ the NT9X14AA 4 Mbyte card.

The MS provides larger message traffic capacity and larger message length than the central message controller. The NT9X04AB provides the central clock source for the DMS-100 office.

Like the computing module (CM), the MS duplicates and the two units operate in load-sharing mode.

The NT9X04AB has circuit packs (CP) on the front of the shelf and with corresponding paddle boards (PB) on the rear. The CPs and PBs share a bus.

The NT9X04AB supports two types of link interfaces:

- the standard DS30 twisted-pair link to current network modules and input/output controllers
- the DS512 fiber link to CMs and enhanced network (ENET)

The NT9X04AB accommodates two major internal buses:

- processing unit bus (P-bus), which communicates with the other components of the MS
- transaction bus (T-bus), on which messages transmit from port to port. This bus is synchronous bus and operates at 4.096 MHz.

Parts

The NT9X04AB shelf contains the following parts:

- NT9X13DA—CPU 16 MHz CP
- NT9X14BB—6 Mbyte memory CP
- NT9X15AA—Mapper CP
- NT9X17AA—MS 4-port CP
- NT9X19AA—Filler CP
- NT9X19BA—Filler PB
- NT9X20AA—DS512 PB
- NT9X23AA—DS30 4-port PB

NT9X04AB (continued)

- NT9X25AA—MS port extender PB
- NT9X26AB—Remote terminal interface (RTIF) PB
- NT9X30AA—Power converter, +5V CP
- NT9X31AA—Power converter, -5V CP
- NT9X32AA—MS load PB
- NT9X49CA—MS P-bus terminator CP
- NT9X52AA—T-bus access CP
- NT9X53AA—MS clock CP
- NT9X54AA—MS external clock interface PB

Design

The parts for NT9X04AB appear in the following table.

NT9X04AB parts (Sheet 1 of 4)

PEC	Slot	Description
NT9X13DA	9F	*CPU card* The NT9X13DA is a 16 Mhz MC68020 CPU. The NT9X13DA offers memory access and write protection. The NT9X13DA uses a 4 kbyte data cache. The NT9X13DA uses a dual channel serial communications controller.
NT9X14BB	10F	*6 Mbyte memory card* The NT9X14BB consists of three memory modules. Each memory module has 2 Mbytes of dynamic RAM (DRAM). Each NT9X14BB memory module has error checking and correction. The NT9X14AA uses a 40 bit memory width. The 40 bit memory consists of 32 bits of data, 7 check bits, and 1 parity bit.
NT9X15AA	11F	*Mapper circuit pack* The NT9X15AA is a specialized memory card that translates the software address to a physical address for routing. The CPU provides the software address. The NT9X15AA provides route state information. The route state information is route open or closed.

NT9X04AB parts (Sheet 2 of 4)

PEC	Slot	Description
NT9X17AA	30F-31F Provisionable 12F-29F	*MS 4-port circuit pack (universal port card)* The NT9X17AA provides a data path for messaging between the MS and four external links. The NT9X17AA uses the T-bus to provide the data path.
NT9X19AA	12F-29F	*Filler circuit pack* The NT9X19AA fills CP slots that are not used.
NT9X19BA	11R-32R	*Filler paddle board* The NT9X19AA fills PB slots that are not used.
NT9X20AA	30R-31R Provisionable 12R-27R	*DS512 paddle board* The NT9X20AA provides an interface between the 9X12 CPU port card and the fiber link to the CM. The NT9X20AA performs 10 bit to 12 bit conversion.
NT9X23AA	Provisionable 12R-29R	*DS30 4-port paddle board* The NT9X23AA provides an interface between a parallel 4.096 MHz backplane data bus and the twisted-pair transmission cables associated with four DS30 links. The NT9X23AA performs the following secondary functions: • transmits out-of-band (OOB) data • receives OOB data • provisions of a reference frame pulse extracted from the link The NT9X23AA is used with the NT9X17 MS 4-port card.
NT9X25AA	Provisionable 12R-27R	*MS port expander circuit board* The NT9X25AA connects the DS30 or DS512 links to port cards (NT9X17CA) on the MS shelf through the secondary bus (S-bus). The NT9X25AA connects the S-bus of slot N to the S-bus of slot N+1. An NT9X25BA card terminates the chain. The NT9X25AA must be used between an NT9X20BB and a NT9X25BA in the S-bus daisy chain. The Nt9X25AA allows a maximum of four NT9X17CA circuit packs to share a single NT9X20BB DS512 MSEN PB.

NT9X04AB (continued)

NT9X04AB parts (Sheet 3 of 4)

PEC	Slot	Description
NT9X26AB	9R	*Remote terminal interface (RTIF) paddle board* The NT9X26AB monitors the incoming terminal and remote modem line for key words. The NT9X26AB provides a primitive person-machine interface when the CPU does not function. Used for maintenance.
NT9X30AA	4F, 36F	*Power converter, +5V circuit pack* The NT9X30AA provides an output of +5.2V ±2% at the minimum of 0A to the maximum of 20A to the CP on the NT9X04AB shelf.
NT9X31AA	1F, 33F	*Power converter, -5V circuit pack* The NT9X31AA provides an output of -5.2V ±2% at the minimum of 0A to the maximum of 20A to the CP on the NT9X04AB shelf.
NT9X32AA	7R, 10R,12R-29R	*DMS bus load paddle board* The NT9X32AA guarantees a constant load distribution on the main clock and frame pulse signals that drive the shelf. This load distribution is separate from the number of cards or shelf type. The shelf type is master or extension.
NT9X49CA	32F	*MS P-bus terminator circuit pack* The NT9X49CA provides termination for MS backplane tracks that the message switch processor uses. The NT9X49CA also provides a time-out on the MS T-bus.
NT9X52AA	7F	*T-bus access circuit pack* The NT9X52AA interfaces the P-bus with the T-bus. This interface allows the message switch processor to receive and transmit messages on the T-bus.

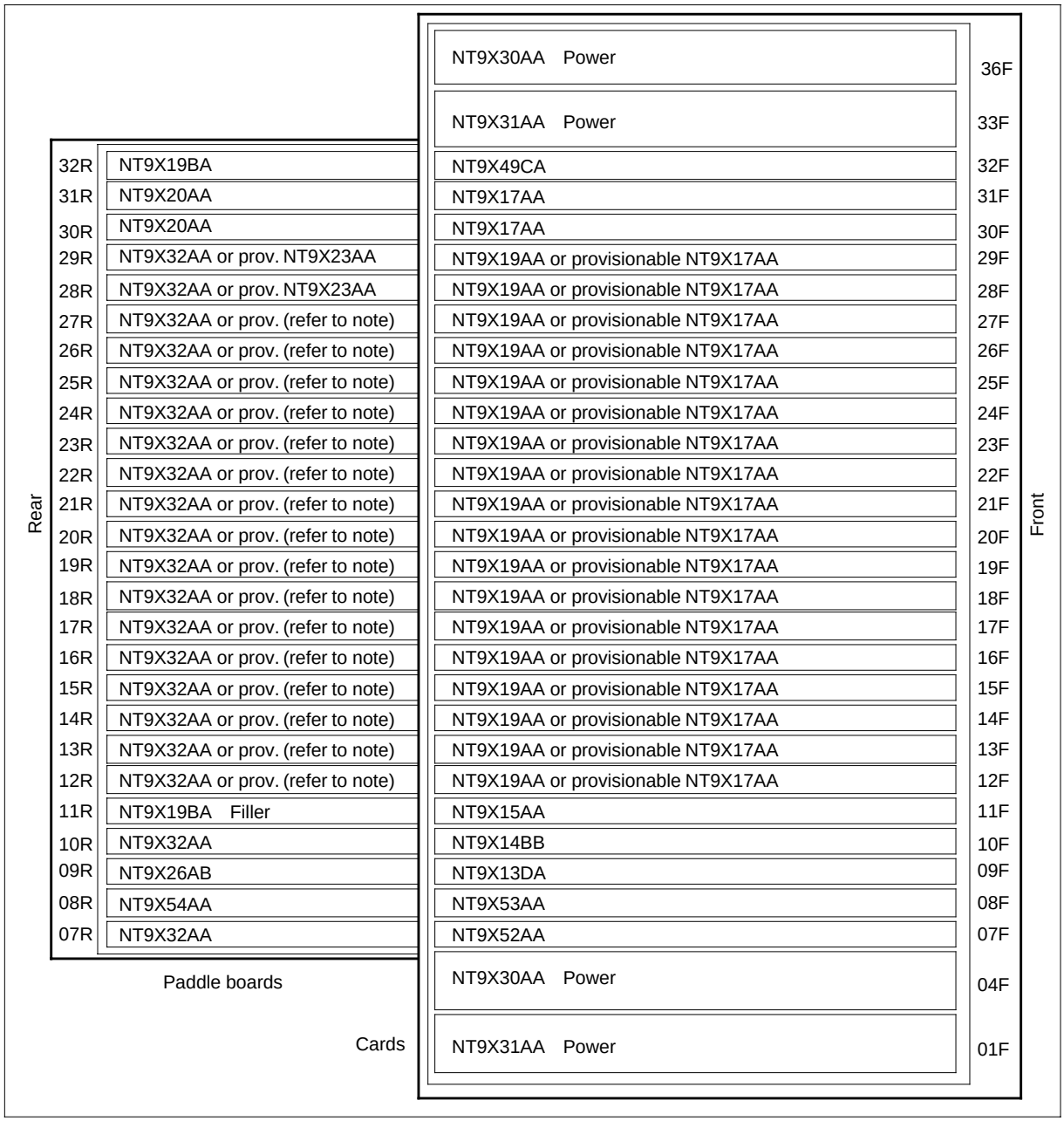
NT9X04AB parts (Sheet 4 of 4)

PEC	Slot	Description
NT9X53AA	8F	*MS clock circuit pack* The clock subsystem consists of the NT9X54AA and this CP (NT9X53AA). This subsystem provides the clock source for the DMS-100 SuperNode system and provides the subsystem clock for the MS T-bus.
NT9X54AA	8R	*MS external clock interface paddle board* The NT9X54AA is the MS external clock interface PB that interfaces the NT9X53AA clock with the DMS-100 system. The clock subsystem consists of the NT9X53AA and this CP (NT9X54AA). This subsystem provides the clock source for the DMS-100 SuperNode system.

The design of the NT9X04AB appears in the following figure.

NT9X04AB (end)

NT9X04AB design



NT9X04AE

Product description

The message switch (MS) is the messaging component of SuperNode. The MS concentrates and distributes messages in the DMS-100 system. The NT9X04AE differs from the NT9X04AB. The AE shelf employs NT9X14BB 6 Mbyte memory cards with a handshake override feature. The AE shelf does not employ the NT9X14AA 4 Mbyte cards.

The MS provides larger message traffic capacity and larger message length than the central message controller. The also provides the central clock source for the DMS-100 office.

Like the computing module (CM), the MS duplicates and the two units operate in load-sharing mode.

The NT9X04AE has circuit packs (CP) on the front of the shelf and corresponding paddle boards (PB) on the rear. The CP and PB share a bus.

The NT9X04AE supports two types of link interfaces:

- the standard DS30 twisted-pair link to current network modules and input/output controllers
- the DS512 fiber link to CMs and enhanced network (ENET)

The NT9X04AE accommodates two major internal buses:

- processing unit bus (P-bus), which communicates with the other components of the MS
- transaction bus (T-bus), on which messages transmit from port to port. This bus is synchronous and operates at 4.096 MHz.

Parts

The NT9X04AE shelf contains the following parts:

- NT9X13DA—CPU 16 MHz CP
- NT9X14BB—6 Mbyte memory with synchronous override CP
- NT9X15AA—Mapper CP
- NT9X17AA—MS 4-port CP
- NT9X19AA—Filler CP
- NT9X19BA—Filler PB
- NT9X20AA—DS512 PB
- NT9X23AA—DS30 4-port PB

NT9X04AE (continued)

- NT9X25AA—MS port extender PB
- NT9X26AB—Remote terminal interface (RTIF) PB
- NT9X30AA—Power converter, +5V CP
- NT9X31AA—Power converter, -5V CP
- NT9X32AA—MS load PB
- NT9X49CA—MS P-bus terminator CP
- NT9X52AA—T-bus access CP
- NT9X53AA—MS clock CP
- NT9X54AA—MS external clock interface PB

Design

The parts for NT9X04AE appear in the following table.

NT9X04AE parts (Sheet 1 of 4)

PEC	Slot	Description
NT9X13DA	9F	*CPU card* The NT9X13DA is a 16 Mhz MC68020 CPU. The NT9X13DA offers memory access and write protection. The NT9X13DA uses a 4 kbyte data cache. The NT9X13DA uses a dual channel serial communications controller.
NT9X14BB	10F	*6 Mbyte memory card* The NT9X14BB consists of three memory modules. Each memory module has 2 Mbyte of dynamic RAM (DRAM). Each NT9X14BB memory module has error checking and correction. The NT9X14AA uses a 40 bit memory width. The 40 bit memory consists of 32 bits of data, 7 check bits, and 1 parity bit.
NT9X15AA	11F	*Mapper circuit pack* The NT9X15AA is a specialized memory card that translates a software address to a physical address for routing. The CPU provides the software address. The NT9X15AA provides route state information. The route state information is route open or closed.

NT9X04AE parts (Sheet 2 of 4)

PEC	Slot	Description
NT9X17AA	30F-31F Provisionable; 12F-29F	*MS 4-port circuit pack (universal port card)* The NT9X17AA provides a data path for messaging between the MS and four external links. The NT9X17AA uses the T-bus to provide the data path.
NT9X19AA	12F-29F	*Filler circuit pack* The NT9X19AA fills CP slots that are not used.
NT9X19BA	11R-32R	*Filler paddle board* The NT9X19BA fills PB slots that are not used.
NT9X20AA	30R-31R Provisionable: 12R-27R	*DS512 paddle board* The NT9X20AA provides an interface between the 9X12 CPU port card and the fiber link to the CM. The NT9X20AA performs 10 bit to 12 bit conversion.
NT9X23AA	Provisionable 12R-29R	*DS30 4-port paddle board* The NT9X23AA provides an interface between a parallel 4.096 MHz backplane data bus and the twisted-pair transmission cables associated with four DS30 links. The NT9X23AA performs the following secondary functions: • transmits out-of-band (OOB) data • receives OOB data • provisions a reference frame pulse extracted from the link The NT9X23AA is used with the NT9X17 message switch 4-port card.
NT9X25AA	Provisionable: 12R-27R	*MS port expander circuit board* The NT9X25AA connects the DS30 or DS512 links to port cards (NT9X17CA) on the MS shelf through the secondary bus (S-bus). The NT9X25AA connects the S-bus of slot N to the S-bus of slot N+1. An NT9X25BA card terminates the chain. The NT9X25AA must be used between an NT9X20BB and a NT9X25BA in the S-bus daisy chain. The NT9X25AA allows a maximum of four NT9X17CA CPs to share a single NT9X20BB DS512 MSEN PB.

NT9X04AE (continued)

NT9X04AE parts (Sheet 3 of 4)

PEC	Slot	Description
NT9X26AB	9R	*Remote terminal interface (RTIF) paddle board* The NT9X26AB monitors the incoming terminal and remote modem line for key words. The NT9X26AB provides a primitive person-machine interface when the CPU does not function. Used for maintenance.
NT9X30AA	4F, 36F	*Power converter, +5V circuit pack* The NT9X30AA provides an output of +5.2V ±2% at the minimum of 0A to the minimum of 20A to the circuit packs on the NT9X04AB shelf.
NT9X31AA	1F, 33F	*Power converter, -5V circuit pack* The NT9X31AA provides an output of -5.2V ±2% at the minimum of 0A to the maximum of 20A to the CPs on the NT9X04AB shelf.
NT9X32AA	7R, 10R, 12R-29R	*DMS bus load paddle board* The NT9X32AA guarantees a constant load distribution on the main clock and frame pulse signals that drive the shelf. The load distribution is separate from the number of cards or shelf type. The shelf type is master or extension.
NT9X49CA	32F	*MS P-bus terminator circuit pack* The NT9X49CA provides termination for MS backplane tracks that the message switch processor uses. The NT9X49CA also provides a time-out on the MS T-bus.
NT9X52AA	7F	*T-bus access circuit pack* The NT9X52AA interfaces the P-bus with the T-bus. This interface allows the message switch processor to receive and transmit messages on the T-bus.

NT9X04AE (continued)

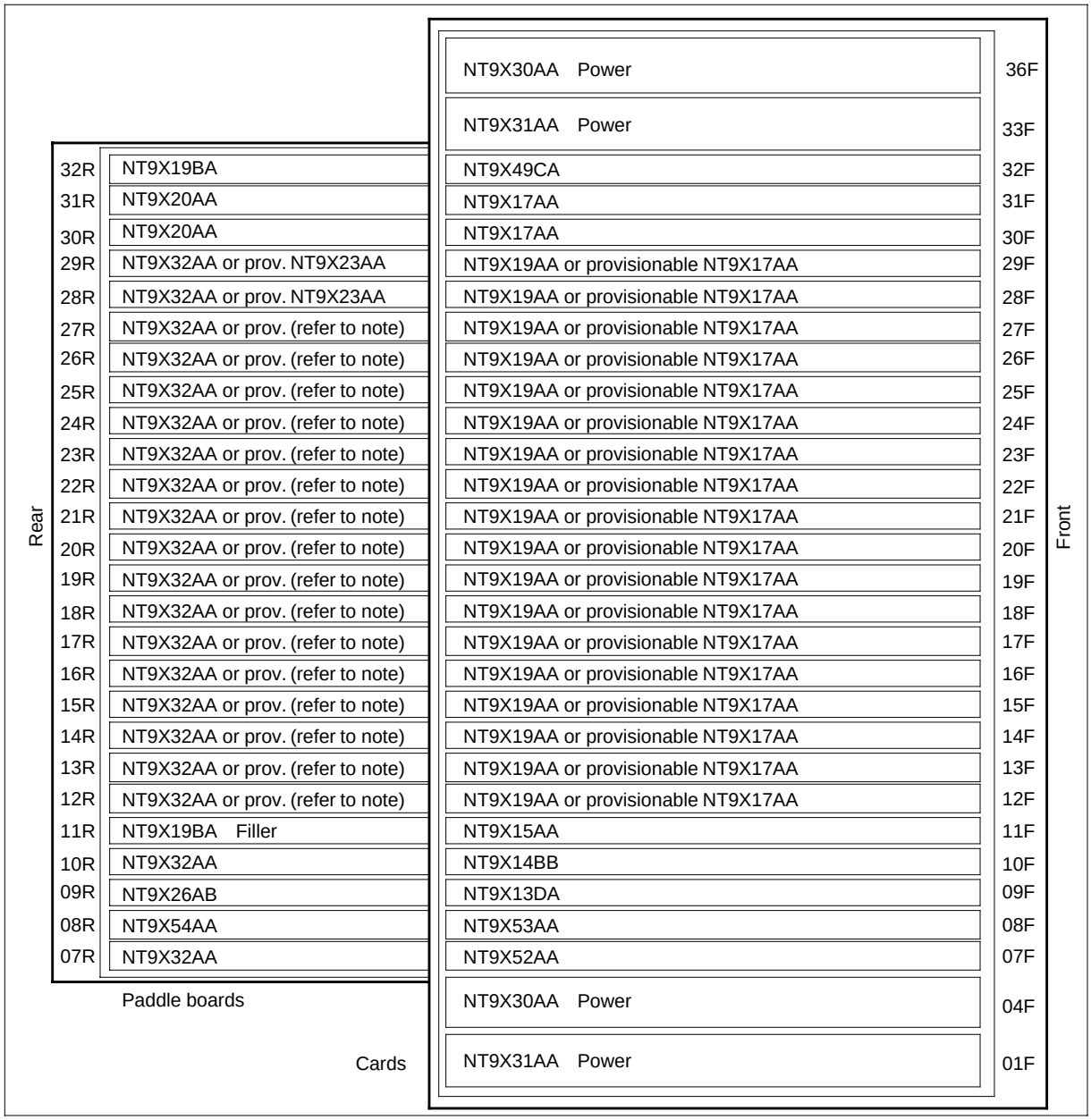
NT9X04AE parts (Sheet 4 of 4)

PEC	Slot	Description
NT9X53AA	8F	MS clock circuit pack The clock subsystem consists of the NT9X54AA and the NT9X53AA. This subsystem provides the clock source for the DMS-100 SuperNode system and provides the subsystem clock for the MS T-bus.
NT9X54AA	8R	MS external clock interface paddle board The NT9X54AA is the MS external clock interface paddle board that interfaces the NT9X53AA clock with the DMS-100 system. The clock subsystem consists of the NT9X53AA and the NT9X54AA. The subsystem provides the clock source for the DMS-100 SuperNode system.

The design of the NT9X04AE appears in the following figure.

NT9X04AE (end)

NT9X04AE design



NT9X04AH

Product description

The message switch (MS) is the messaging component of SuperNode. The NT9X04AH MS concentrates and distributes messages in the DMS-100 system.

The MS provides larger message traffic capacity and larger message length in comparison to the central message controller. The also provides the central clock source for the DMS-100 office.

Like the computing module (CM), the MS duplicates and the two units operate in load-sharing mode.

The NT9X04AH has circuit packs (CP) on the front of the shelf and corresponding paddle boards (PB) on the rear. The CPs and PBs share a common bus.

The NT9X04AH supports two types of link interfaces:

- the standard DS30 twisted-pair link to current network modules and input/output controllers (IOC)
- the DS512 fiber link to CMs and enhanced network (ENET)

The NT9X04AH accommodates two major internal buses:

- processing unit bus (P-bus), which communicates with the other components of the MS
- transaction bus (T-bus), on which messages transmit from port to port. This bus is synchronous and operates at 4.096 MHz.

Parts

The NT9X04AH shelf contains the following parts:

- NT9X13DB—CPU 16 MHz CP
- NT9X14BB—6 Mbyte memory CP
- NT9X15AA—Mapper CP
- NT9X17AA—MS 4-port CP
- NT9X17DA—MS 64-port CP
- NT9X19AA—Filler CP
- NT9X19BA—Filler PB
- NT9X20AA—DS512 PB

NT9X04AH (continued)

- NT9X23BA—DS30 4-port PB
- NT9X25BA—MS port extender PB
- NT9X26AB—Remote terminal interface (RTIF) PB
- NT9X30AA—Power converter, +5V CP
- NT9X31AA—Power converter, -5V CP
- NT9X32AA—MS load PB
- NT9X49CA—MS P-bus terminator CP
- NT9X52AA—T-bus access CP
- NT9X53AA—MS clock CP
- NT9X53AB—DMS-SuperNode clock card
- NT9X54AA—MS external clock interface PB

Design

The parts for the NT9X04AH shelf appear in the following table.

NT9X04AH parts (Sheet 1 of 6)

PEC	Slot	Description
NT9X13DB	9F	*CPU card* The NT9X13DB is a 32 bit, 20 MHz MC68020 CPU. The NT9X13DB offers memory access and write protection. The NT9X13DB uses a 4 kbyte data cache. The NT9X13DB uses a dual channel serial communications controller.
NT9X14BB	10F	*6 Mbyte memory card* The NT9X14BB consists of three memory modules. Each module has 2 Mbyte of dynamic RAM (DRAM). Each NT9X14BB memory module has error checking and correction. The NT9X14AA uses a 40 bit memory width. The 40 bit memory consists of 32 bits of data, 7 check bits, and 1 parity bit.

NT9X04AH (continued)

NT9X04AH parts (Sheet 2 of 6)

PEC	Slot	Description
NT9X15AA	11F	*Mapper circuit pack* The NT9X15AA is a specialized memory card that translates a software address to a physical address for routing. The CPU provides the software address. The NT9X15AA provides route state information. The route state information is route open or closed.
NT9X17AA	30F-31F Provisionable: 12F-29F	*MS 4-port circuit pack (universal port card)* The NT9X17AA provides a data path for messaging between the MS and four external links. The NT9X17AA uses the T-bus to provides the data path.
NT9X17DA	Provisionable: 12-29F	*DMS-bus 64-port circuit pack* The NT9X17DA provides 64 logically separate ports. Each port corresponds to one separately addressable T-bus transceiver and can handle one logical message path. The NT9X17DA connects to link interface PBs through two 4.096 MHz 8 bit data buses. The two data buses are the shorting bus (S-bus).
NT9X19AA	12F-29F	*Filler circuit pack* The NT9X19AA fills CP slots that are not used.
NT9X19BA	11R	*Filler paddle board* The NT9X19BA fills PB slots that are not used.
NT9X20AA	30R-31R	*DS512 paddle board* The NT9X20AA provides an interface between the 9X12 CPU port card and the fiber link to the CM. The NT9X20AA performs 10 bit to 12 bit conversion.

NT9X04AH (continued)

NT9X04AH parts (Sheet 3 of 6)

PEC	Slot	Description
NT9X20BB	Provisionable: 12R-29R	*DS512 MSEN paddle board* The NT9X20BB is a DMS-bus fiber interface PB used for messaging links between DMS-bus and the enhanced network (ENET). The NT9X20BB interface on the backplane side is an S-bus, that runs at a maximum average rate of 4.088 Mwords each second. The S-bus has two sections: in-band and out-of-band (OOB). The in-band section refers to the 8 bits that carry the messaging information to or from the link handlers. The link handlers reside on port cards. The 2 bits that remain are called OOB and carry system reset information. The NT9X20BB has a bidirectional P-bus. The P-bus provides access to different read and write registers on the card. These registers are used for initialization, maintenance activities, and system reset requirements.
NT9X23AA	Provisionable: 12R-29R	*DS30 4-port paddle board* The NT9X23AA provides an interface between a parallel 4.096 MHz backplane data bus and the twisted-pair transmission cables associated with four DS30 links. The NT9X23AA performs the following secondary functions: • transmits OOB data • receives OOB data • provisions a reference frame pulse extracted from the link The NT9X23AA is used with the NT9X17 message switch 4-port card.

NT9X04AH parts (Sheet 4 of 6)

PEC	Slot	Description
NT9X23BA	Provisionable: 12R-29R	*DS30 4-port paddle board (signal transfer point)* The NT9X23BA provides an interface between a parallel 4.096 MHz backplane data bus and the twisted-pair transmission cables associated with four DS30 links. The NT9X23BA performs the following secondary functions: • transmits OOB data • receives OOB data • provisions a reference frame pulse extracted from the link The NT9X23BA is used with the NT9X17 message switch 4-port card.
NT9X25AA	Provisionable: 12R-29R	*MS port expander circuit board* The NT9X25AA connects the DS30 or DS512 links to port cards (NT9X17CA) on the MS shelf through the S-bus. The NT9X25AA connects the S-bus of slot N to the S-bus of slot N+1. An NT9X25BA card terminates the chain. The NT9X25AA must be used between an NT9X20BB and a NT9X25BA in the S-bus daisy chain. The NT9X25AA allows a maximum of four NT9X17CA CPs to share a single NT9X20BB DS512 MSEN PB.
NT9X26AA or AB	8R-9R	*Remote terminal interface (RTIF) paddle board* The NT9X26AA (or AB) monitors the incoming terminal and remote modem line for key words. The NT9X26AA provides a primitive person-machine interface when the CPU does not function. Used for maintenance.
NT9X30AA	4F, 36F	*Power converter, +5V circuit pack* The NT9X30AA provides an output of +5.2V ±2% at the minimum of 0A to the maximum of 20A for the CPs on the NT9X04AH shelf.
NT9X31AA	1F, 33F	*Power converter, -5V circuit pack* The NT9X30AA provides an output of -5.2V ±2% at the minimum of 0A to the maximum of 20A for the CPs on the NT9X04AH shelf.

NT9X04AH (continued)

NT9X04AH parts (Sheet 5 of 6)

PEC	Slot	Description
NT9X32AA	7R, 10R, 12R-29R	*DMS bus load paddle board* The NT9X32AA guarantees a constant load distribution on the main clock and frame pulse signals that drive the shelf. The load distribution is separate from the card group or shelf type. The shelf type is master or extension.
NT9X49CA	Provisionable: 32F	*MS P-bus terminator circuit pack* The NT9X49CA provides termination for MS backplane tracks that the message switch processor uses. The NT9X49CA also provides a time-out on the MS T-bus.
NT9X49CB	Provisionable: 32F	*DMS-bus tracer circuit pack* The NT9X49CB provides a logic analyzer tracing T-bus messages, that the MS processor can configure. The NT9X49CB performs same functions as the NT9X49CA.
NT9X52AA	7F	*T-bus access circuit pack* The NT9X42AA interfaces the P-bus with the T-bus. This interface allows the message switch processor to receive and transmit messages on the T-bus.
NT9X53AA	Provisionable: 8F	*MS clock circuit pack* The clock subsystem consists of the NT9X54AA and the NT9X53AA. This subsystem provides the clock source for the DMS-100 SuperNode system and the subsystem clock for the MS T-bus.

NT9X04AH (continued)

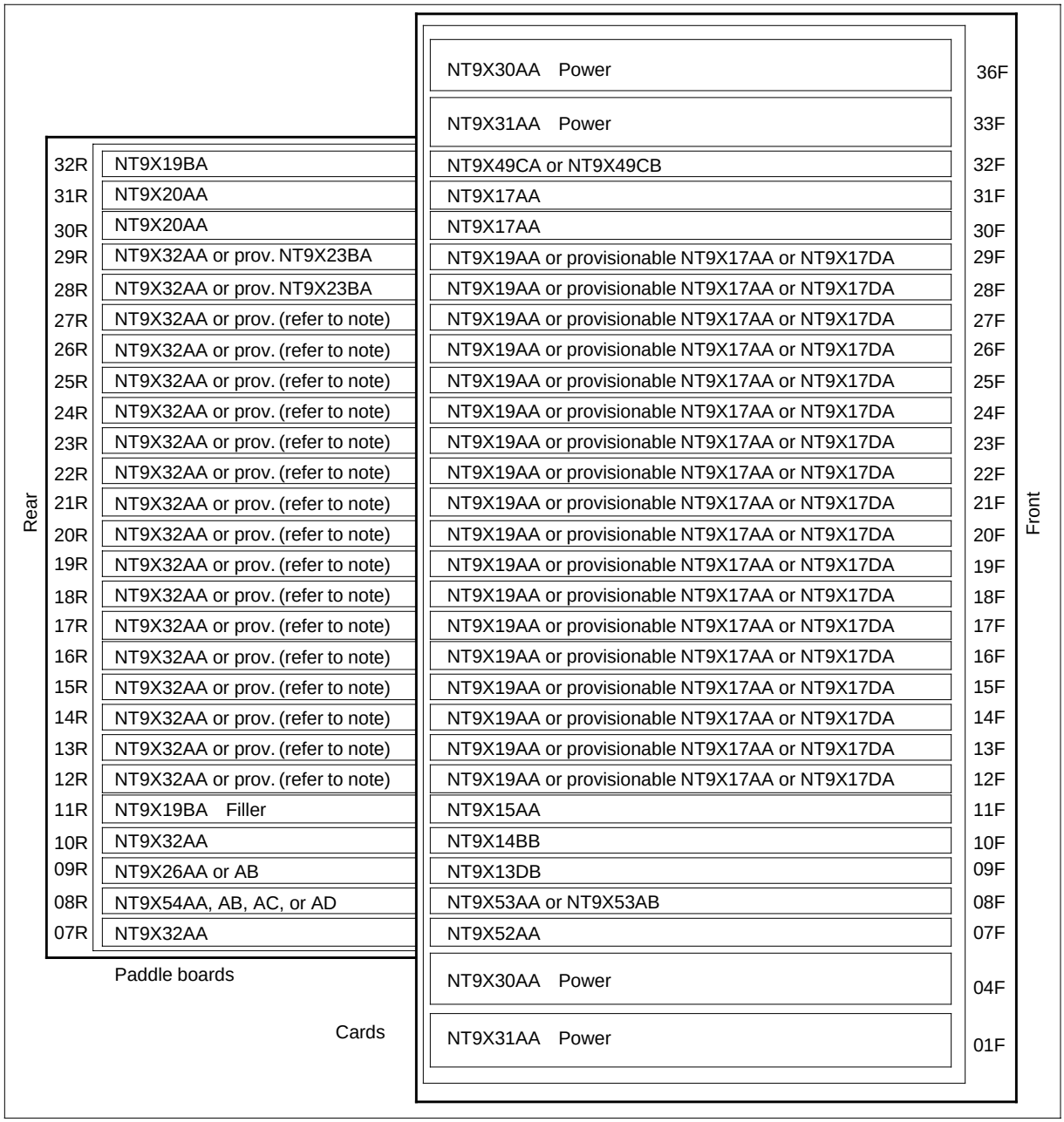
NT9X04AH parts (Sheet 6 of 6)

PEC	Slot	Description
NT9X53AB	Provisionable: 8F	*DMS-SuperNode clock circuit pack* The NT9X53AB generates accurate timing signals from two digital phased locked loops (DPLL). The DPLLs use Stratum 3 oscillators. With a remote clock, one of the DPLLs can use a Stratum 2 or 2.5 oscillator. The DPLLs generate clock signals and 8 kHz frame pulse signals. The NT9X53Ab can lock onto a highly accurate external clock source, like a Stratum 1 (caesium) oscillator.
NT9X54AA, AB, AC, or AD	Provisionable: 8R	*MS external clock interface paddle board* The NT9X54 is the MS external clock interface PB that interfaces the NT9X53 clock with the DMS-100 system. The clock subsystem consists of the NT9X53AB and the NT9X54. This subsystem provides the clock source for the DMS-100 SuperNode system.

The design of the NT9X04AH appears in the following figure.

NT9X04AH (end)

NT9X04AH design



NT9X05AB

Product description

The NT9X05AB enhanced network (ENET) cabinet is the standard DMS SuperNode cabinet. The NT9X05AB cabinet can contain one or two pairs of NT9X08 ENET shelves. Shelves are divided between plane 0 and plane 1.

The following figure describes a standard ENET configuration. One fully equipped cabinet acts as plane 0. Another fully equipped cabinet acts as plane 1. One ENET shelf pair can provide a maximum of 15 speech link interface cards for each plane.

The number of ENET shelves required depends on the quantity and types of peripheral modules (PM) the shelves interface with. The number of PMs determine the required number of speech link interface cards.

The ENET shelves provide high-speed interfaces between the DMS-core and peripherals. The ENET uses fiber optic connections to the DMS-core and fiber peripheral modules.

Empty shelf positions are provisioned with cage filler panels to satisfy the forced-air cooling requirements of the cabinet. For the same reason, card filler plates occupy shelf slots that are not in use.

Parts

The ENET simplex cabinet contains the following parts:

- A0323984—Core cooling unit (CU)
- NT9X03AA—Frame supervisory panel (FSP)
- NT9X0801—ENET shelf

Core cooling unit

The A0323984 core CU provides mechanical ventilation for equipment that the SuperNode cabinet houses.

Frame supervisory panel

The NT9X03AA frame supervisory panel (FSP) provides alarm, maintenance and supervisory functions. The FSP is in the top shelf position in the NT9X01AA. To access the front and rear of the NT9X03AA, open the cabinet doors. A frame light is visible when the door is closed.

Power from the power distribution center frame comes to the FSP. The FSP distributes the power to power supply modules in the cabinet, like the NT9X30AA and NT9X31AA power converters. The power supply modules contain the power control. The power control is separate from the FSP.

NT9X05AB (continued)

ENET shelf

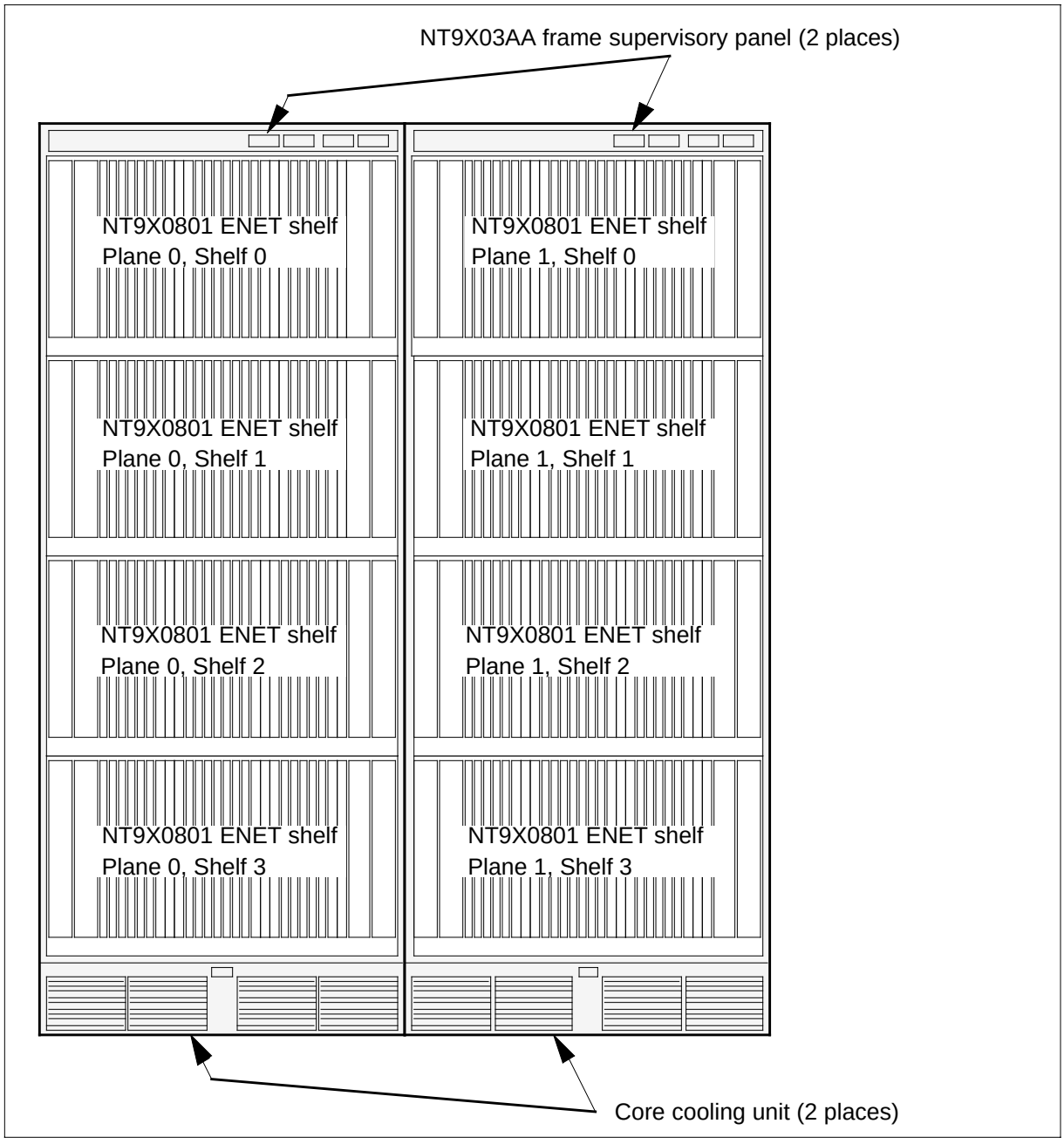
To control message flow, the NT9X0801 ENET shelf concentrates and distributes messages. The shelf allows components to communicate directly with each other.

The pairs of NT9X0801s comprise a duplicate ENET network interface between the DMS-core and the high-speed peripherals of the system. The duplication of the shelves guarantee the reliability of the system. The two ENET shelves operate at the same time and in the same way. The ENET can continue to operate alone on a full message load without message loss or service degradation.

Design

The design of the NT9X05AB cabinet appears in the following figure.

NT9X05AB parts



NT9X05AC

Product description

The NT9X05AC Enhanced Network (ENET) cabinet is the standard DMS SuperNode cabinet. The NT9X05AC cabinet can contain one or two pairs of NT9X08 ENET shelves. Shelves are divided between plane 0 and plane 1.

The following figure describes a standard ENET configuration. One fully equipped cabinet acts as plane 0. Another fully equipped cabinet acts as plane 1. One ENET shelf pair can provide a maximum of 15 speech link interface cards for each plane.

The number of ENET shelves required depends on the quantity and types of peripheral modules (PM) the shelves link to. The number of PMs determines the required number of speech link interface cards.

The ENET shelves provide high-speed interfaces between the DMS-core and peripherals. The ENET uses fiber optic connections to the DMS-core and fiber peripheral modules.

Empty shelf positions are provisioned with cage filler panels for the forced-air cooling requirements of the cabinet. For the same reason, card filler plates occupy shelf slots that are not in use.

Parts

The ENET simplex cabinet contains the following parts:

- A0323984—core cooling unit
- NT0X24BD—blank shelf assembly
- NT9X01FB—filler faceplate
- NT9X03AA—SuperNode frame supervisory panel
- NT9X0801—ENET shelf

Core cooling unit

The A0323984 core cooling unit (CU) provides mechanical ventilation for equipment that the SuperNode cabinet houses.

Blank shelf assembly

Blank shelf assembly filler panels (NT0X24BD) occupy empty shelves in positions 00, 13, and 26 for forced-air cooling requirements.

Filler faceplate

One NT9X01FB filler faceplate occupies each shelf assembly when the shelf does not have a card.

SuperNode frame supervisory panel

The NT9X03AA FSP provides alarm, maintenance and supervisory functions. The FSP is in the top shelf position in the NT9X01AA. To access or view the front and rear faces of the NT9X03AA, open the cabinet doors. A frame alarm light is in the cabinet. The light is visible with the cabinet doors closed.

Power from the power distribution center frame comes in the FSP. The FSP distributes the power to power supply modules in the cabinet. Power supply modules include the NT9X30AA and NT9X31AA power converters. The power supply modules contain the power control. The power control is separate from the FSP.

ENET shelf

The NT9X0801 ENET shelf controls message flow. To control message flow, the shelf concentrates and distributes messages. The shelf allows components to communicate directly with each other.

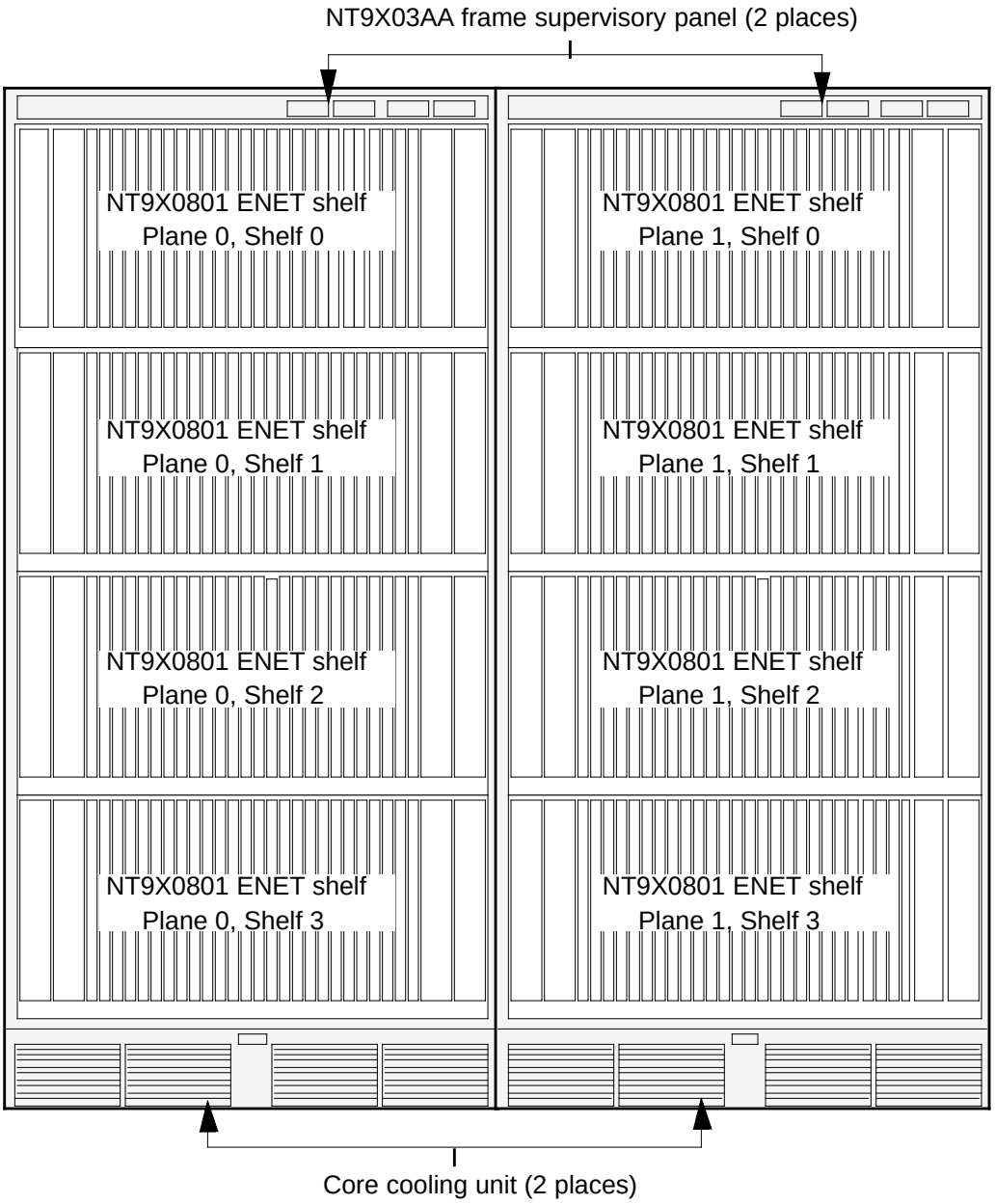
The pairs of NT9X0801s comprise a duplicate ENET network interface between the DMS-core and the high-speed peripherals of the system. The duplication of shelves guarantees reliability of the system. The two ENET shelves operate at the same time and in the same way. The ENET can operate alone on a full message load without message loss or service degradation.

Design

The design of the NT9X05AC cabinet appears in the following figure.

NT9X05AC (end)

NT9X05AC parts



Note: This diagram is not drawn to scale.

NT9X05AD

Description

The NT9X05AD single cabinet Enhanced Network (ENET) is the standard DMS SuperNode cabinet. The NT9X05AD cabinet can contain one or two pairs of NT9X08 ENET shelves. Shelves are divided between plane 0 and plane 1.

The following figure describes a standard ENET configuration. One fully equipped cabinet acts as plane 0. Another fully equipped cabinet acts as plane 1. One ENET shelf pair can provide a maximum of 15 speech link interface cards for each plane.

The number of ENET shelves required depends on the quantity and types of peripheral modules (PM) the shelves link to. The number of PMs determines the number of speech link interface cards required.

The ENET shelves provide high-speed interfaces between the DMS-core and peripherals. The ENET uses fiber optic connections to the DMS-core and fiber peripheral modules.

Empty shelf positions are provisioned with cage filler panels for the forced-air cooling requirements of the cabinet. For the same reason, shelf slots that are not in use are filled with card filler plates.

Parts

The NT9X05AD ENET simplex cabinet contains the following parts:

- A0377580—core cooling unit, -48V dc
- NT0X24BD—blank shelf assembly
- NT9X01FB—filler faceplate
- NT9X03AA—SuperNode frame supervisory panel
- NT9X0801—ENET shelf

Core cooling unit

The A0377580 core cooling unit (CU) provides mechanical ventilation for equipment that the single cabinet ENET houses.

Blank shelf assembly

The NT0X24BD blank shelf fills in shelf positions 00 and 26 when the positions are not in use.

NT9X05AD (continued)

Filler faceplate

The NT9X01FB filler faceplate occupies an empty NT0X24BD shelf for the forced-air cooling requirements of the cabinet.

SuperNode frame supervisory panel

The NT9X03AA SuperNode frame supervisory panel (FSP) provides alarm, maintenance and several supervisory functions. The FSP is in the top shelf position in the NT9X05CA. To access or view the front and rear faces of the NT9X03AA, open the cabinet doors. A frame alarm light in the cabinet is visible with the doors closed.

Power from the power distribution center frame comes in the FSP. The FSP distributes the power to power supply modules in the cabinet, like the NT9X30AA and NT9X31AA power converters. The power supply modules contain power control. The power control is separate from the FSP.

ENET shelf

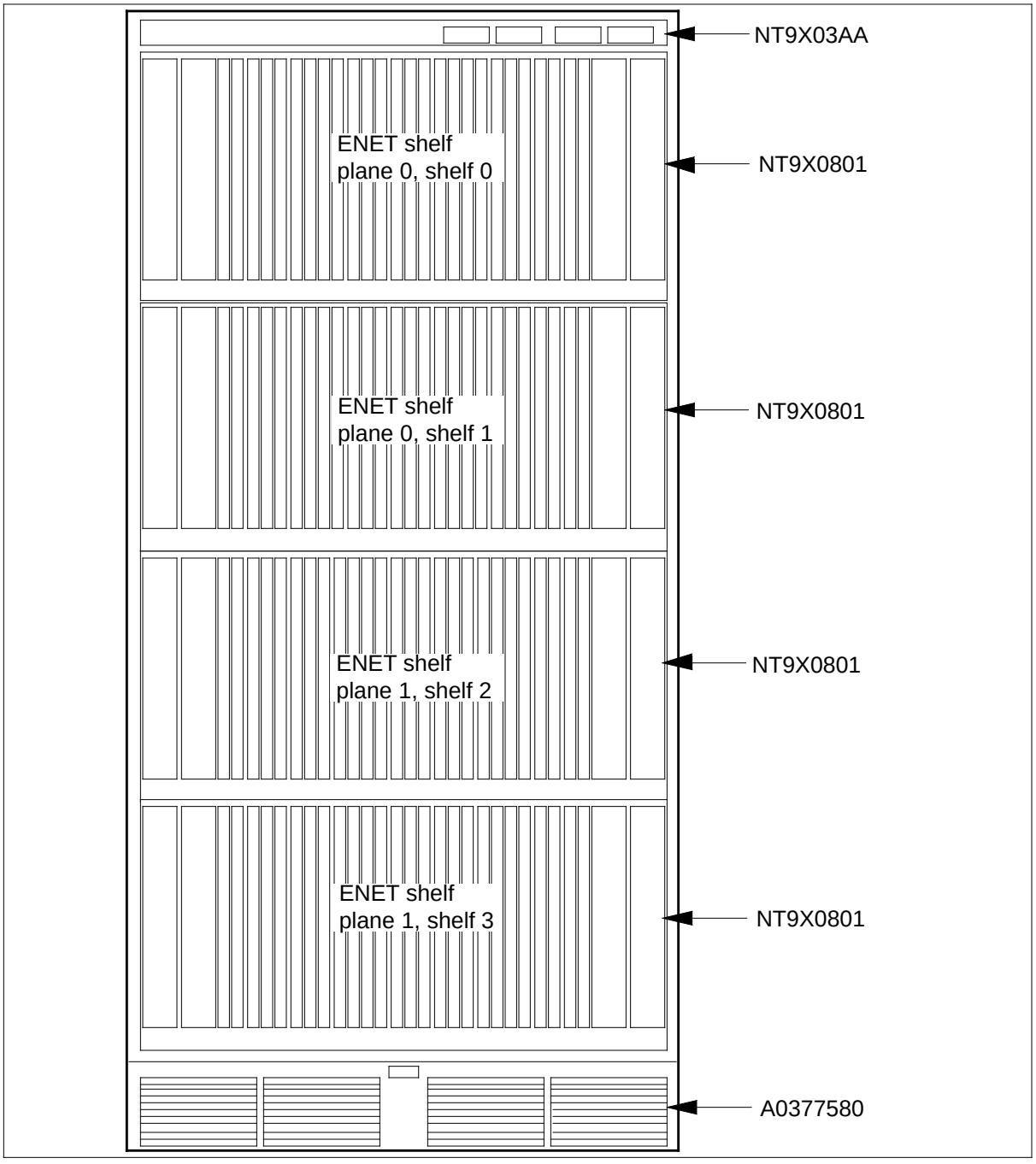
The NT9X0801 ENET shelf controls message flow. To control message flow, the shelf concentrates and distributes messages. The shelf allows components to communicate directly with each other.

The pairs of NT9X0801s comprise a duplicate ENET network interface between the DMS-core and the high-speed peripherals of the system. The duplication of shelves guarantees the reliability of the system. The two ENET shelves operate at the same time and in the same way. The ENET can operate alone on a full message load without message loss or service degradation.

Design

The design of the NT9X05AD cabinet appears in the following figure.

NT9X05AD parts



Note: This diagram is not drawn to scale.

NT9X06AA

Description

The computing module (CM) consists of a pair of CPUs with associated memory. The CPUs operate in a synchronous matched mode on two separate planes. One plane is active. The active plane maintains control of the system when the other plane is on standby.

The CMs provide the CPUs for the DMS SuperNode switching system. A Motorola MC68020 microprocessor controls each CPU. To guarantee system accuracy between the active and inactive shelves, a mate exchange bus connects the CPUs. This connection allows the processors on each shelf to compare computations.

Parts

The NT9X06AA shelf contains the following parts:

- NT9X12AA—CPU port circuit pack (CP)
- NT9X13BA—CPU processor CP
- NT9X14AA—4 Mbyte memory CP
- NT9X14BA—6 Mbyte memory CP
- NT9X19AA—Filler CP
- NT9X19BA—Filler paddle board (PB)
- NT9X20AA—DS512 PB
- NT9X21AA—CM bus terminator PB
- NT9X22CA—CM subsystem clock PB
- NT9X26AA—Remote terminal interface (RTIF) PB
- NT9X27AA—CM bus extension PB
- NT9X30AA—Power converter, +5V CP
- NT9X31AA—Power converter, -5V CP

Design

Descriptions of the NT9X06AA parts appear in the following table.

NT9X06AA parts (Sheet 1 of 2)

PEC	Slot	Description
NT9X12AA	17F-18F, 21F-22F	*CPU port card* The NT9X12AA provides a communication port between the CM CPU and the MS at 40.96 Mbit/s. The NT9X12AA provides 32 bit communication with the CPU. The NT9X12AA provides a 32 bit mate crossover bus to mate CPU port card.
NT9X12AA	17F-18F, 21F-22F	*Cpu port card* The NT9X12AA provides a communication port between the CM CPU and the MS at 40.96 Mbit/s. The NT9X12AA provides 32 bit communication with the CPU. The NT9X12AA provides a 32 bit mate crossover bus to mate CPU port card.
NT9X13BA	19F-20F	*Cpu card* The NT9X13BA is a 20 MHz MC68020 CPU. The NT9X13BA offers memory access and write protection. The NT9X13BA uses a 4 kbyte data cache. The NT9X13BA also uses a dual channel serial communications controller (SCC).
NT9X14AA	23F-32F	*4 Mbyte memory card* Each NT9X14AA consists of two memory modules. Each module has 2 Mbytes of dynamic RAM (DRAM). Each memory NT9X14AA has error checking and correction. The NT9X14AA uses a 40 bit memory width. The 40 bit memory consists of 32 bits of data, 7 check bits, and 1 parity bit.
NT9X14BA	7F-16F	*6 Mbyte memory card* Each NT9X14BA consists of three memory modules. Each module has 2 Mbytes of DRAM. Each memory NT9X14BA has error checking and correction. The NT9X14BA uses a 40 bit memory width. The 40 bit memory consists of 32 bits of data, 7 check bits, and 1 parity bit.

NT9X06AA (continued)

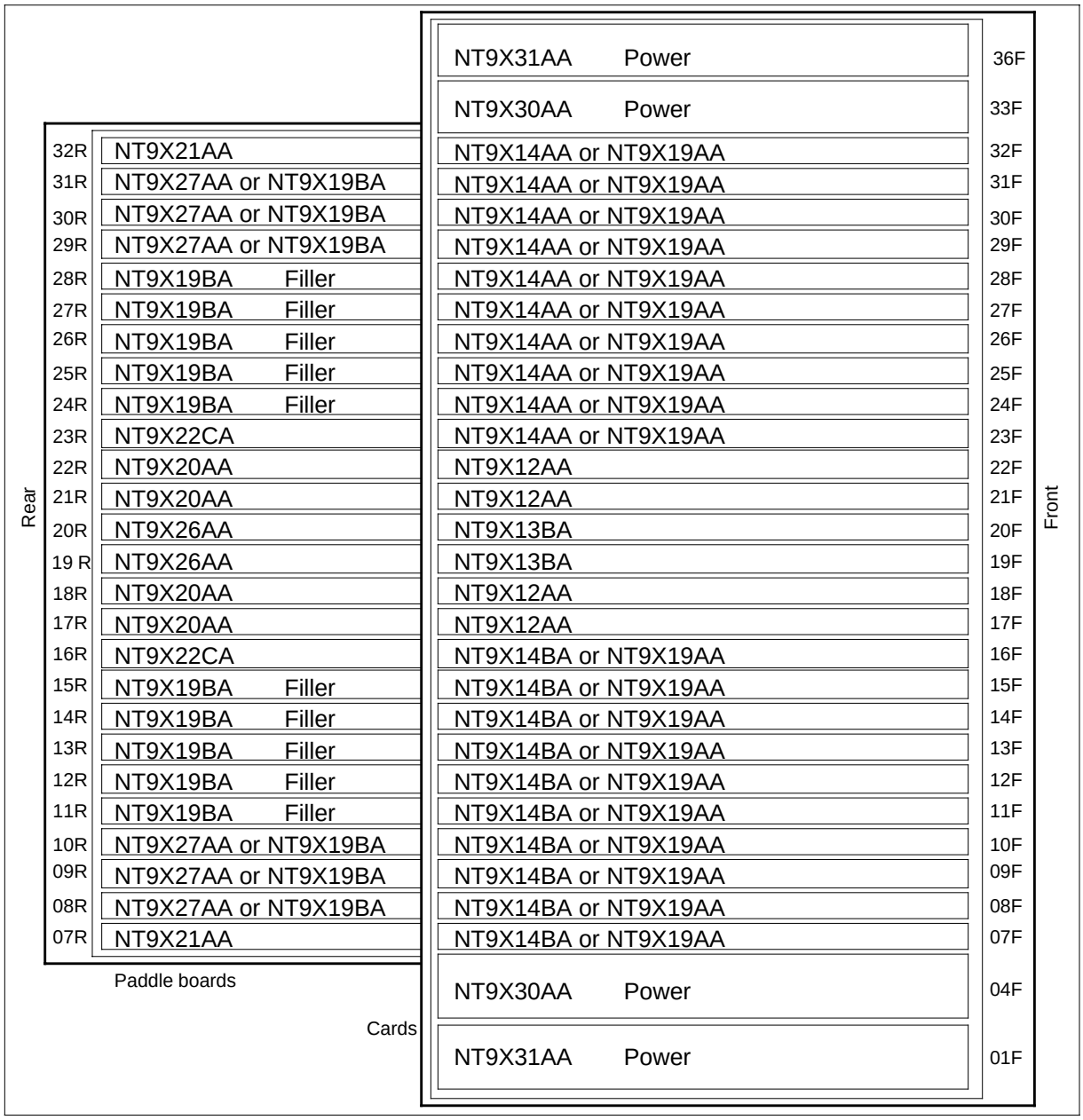
NT9X06AA parts (Sheet 2 of 2)

PEC	Slot	Description
NT9X19AA	7F-16F, 23F-32F	*Filler circuit pack* The NT9X19AA fills in slots that are not used. Memory cards can occupy these slots.
NT9X19BA	8R-15R, 24R-31R	*Filler circuit pad* The NT9X19BA fills slots that are not used. These slots be used for processor shelf bus extender cards (NT9X27AA).
NT9X20AA	17R-18, 21R-22R	*DS512 paddleboard* The NT9X20AA provides an interface between the 9X12 CPU port card and the fiber link to the MS. The NT9X20AA offers 10 bit to 12 bit conversion.
NT9X21AA	7R, 32R	*CM bus terminator paddle board* The NT9X21AA provides termination for the system bus in the CM and extension shelf.
NT9X22CA	16R, 23R	*CM subsystem clock paddle board* The NT9X22CA inputs a 8 kHz frame pulse. The NT9X22CA outputs a 16.38 MHz synchronous clock and a 8 kHz frame pulse. These signals are phase and frequency synchronized to the input frame pulse.
NT9X26AA	19R-20R	*Remote terminal interface (RTIF)* The NT9X26AA monitors the incoming terminal and remote modem line for key words. The NT9X26AA provides a primitive person-machine interface when the CPU does not function.
NT9X27AA	8R, 31R	*CM processor shelf bus extender* The NT9X27AA is an extender for the processor bus (P-bus) from the CM processor shelf to the CM extension shelf
NT9X30AA	4F, 36F	*Power converter, +5V* The NT9X30AA provides an output of +5.2V ±2% at the minimum of 0A to the maximum of 20A to the CPs on the NT9X06AA shelf.
NT9X31AA	1F, 33F	*Power converter, -5V* The NT9X30AA provides an output of -5.2V ±2% at the minimum of 0A to the maximum of 20A to the CPs on the NT9X06AA shelf.

NT9X06AA (end)

The design of the NT9X06AA appears in the following figure.

NT9X06AA design



NT9X06AB

Description

The computing module (CM) consists of a pair of CPUs with associated memory. The CPUs operate in a synchronous matched mode on two separate planes. One plane is active. The active plane maintains control of the system when the other plane is on standby.

The CMs provide the CPUs for the DMS SuperNode switching system. A Motorola MC68020 microprocessor controls each CPU. To guarantee system accuracy between the active and inactive shelves, a mate exchange bus connects the CPUs. This connection allows the processors on each shelf to compare computations.

Parts

The NT9X06AB shelf contains the following parts:

- NT9X12AA—CPU port circuit pack (CP)
- NT9X13BA—CPU processor CP
- NT9X14AA—4 Mbyte memory CP
- NT9X14BA—6 Mbyte memory CP
- NT9X19AA—Filler CP
- NT9X19BA—Filler paddle board (PB)
- NT9X20AA—DS512 PB
- NT9X21AA—CM bus terminator PB
- NT9X22CA—CM subsystem clock PB
- NT9X26AA—Remote terminal interface (RTIF) PB
- NT9X27AA—CM bus extension PB
- NT9X30AA—Power converter, +5V CP
- NT9X31AA—Power converter, -5V CP

Design

Descriptions of the NT9X06AB parts appear in the following table.

NT9X06AB parts (Sheet 1 of 2)

PEC	Slot	Description
NT9X12AA	17F-18F, 21F-22F	*CPU port card* The NT9X12AA provides a communication port between the CM CPU and the MS at 40.96 Mbit/s. The NT9X12AA provides 32 bit communication with the CPU. The NT9X12AA provides a 32 bit mate crossover bus to the mate CPU port card.
NT9X13BA	19F-20F	*CPU card* The NT9X13BA is a 20 MHz MC68020 CPU. The NT9X13BA offers memory access and write protection. The NT9X13BA uses a 4 kbyte data cache. The NT9X13BA also uses a dual channel serial communications controller (SCC).
NT9X14AA	23F-32F	*4 Mbyte memory card* Each NT9X14AA consists of two memory modules. Each memory module has 2 Mbyte of dynamic RAM. Each memory NT9X14AA has error checking and correction. The NT9X14AA uses a 40 bit memory width. The 40 bit memory consists of 32 bits of data, 7 check bits, and 1 parity bit.
NT9X14BA	7F-16F	*6 Mbyte memory card* Each NT9X14BA consists of three memory modules. Each module has 2 Mbyte of dynamic RAM. Each memory NT9X14BA has error checking and correction. The NT9X14BA uses a 40-bit memory width. The 40 bit memory consists of 32 bits of data, 7 check bits, and 1 parity bit.
NT9X19AA	7F-16F, 23F-32F	*Filler circuit pack* The NT9X19AA fills slots that are not used. Memory cards can occupy these slots.
NT9X19BA	8R-15R, 24R-31R	*Filler circuit pack* The NT9X19BA fills slots that are not used. Processor shelf bus extender cards (NT9X27AA) can occupy these slots.

NT9X06AB (continued)

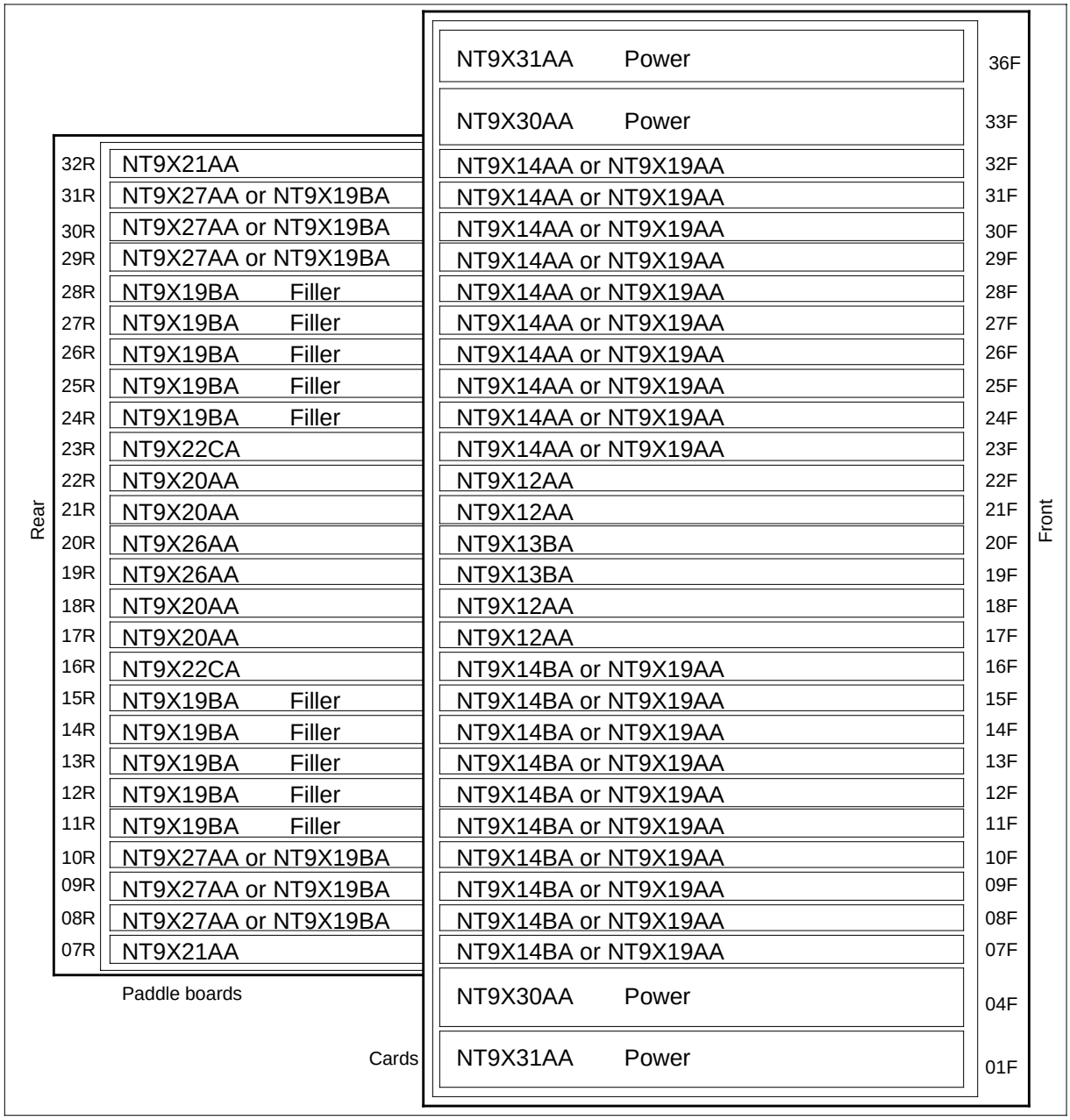
NT9X06AB parts (Sheet 2 of 2)

PEC	Slot	Description
NT9X20AA	17R-18R, 21R-22R	*DS512 paddle board* The NT9X20AA provides an interface between the 9X12 CPU port card and the fiber link to the MS. The NT9X20AA provides 10 bit to 12 bit conversion.
NT9X21AA	7R, 32R	*CM bus terminator paddle board* The NT9X21AA provides termination for the system bus in the CM and extension shelf.
NT9X22CA	16R, 23R	*CM subsystem clock paddle board* The NT9X22CA inputs a 8 kHz frame pulse. The NT9X22CA outputs a 16.38 MHz synchronous clock and a 8 kHz frame pulse. These signals phase and frequency synchronized to the input frame pulse.
NT9X26AA	19R-20R	*Remote terminal interface (RTIF)* The NT9X26AA monitors the incoming terminal and remote modem line for key words. The NT9X26AA provides a primitive person-machine interface when the CPU does not function.
NT9X27AA	8R, 31R	*CM processor shelf bus extender* The NT9X27AA is an extender for the Processor bus (P-bus) from the CM processor shelf to the CM extension shelf.
NT9X30AA	4F, 36F	*Power converter, +5V* The NT9X30AA provides an output of +5.2V ±2% at the minimum of 0A to the maximum of 20A to the CPs on the NT9X06AB shelf.
NT9X31AA	1F, 33F	*Power converter, -5V* The NT9X31AA provides an output of -5.2V ±2% at the minimum of 0A to the maximum of 20A to the CPs on the NT9X06AB shelf.

The design of the NT9X06AB appears in the following figure.

NT9X06AB (end)

NT9X06AB design



NT9X06AC

Description

The computing module (CM) consists of a pair of CPUs with associated memory. The CPUs operate in a synchronous matched mode on two separate planes. One plane is active. The active plane maintains control of the system when the other plane is on standby.

The CMs provide the CPUs for the DMS SuperNode switching system. A Motorola MC68020 microprocessor controls each CPU. To guarantee system accuracy between the active and inactive shelves, a mate exchange bus connects the CPUs. This connection allows the processors on each shelf to compare computations.

Parts

The NT9X06AC shelf consists of the following parts:

- NT9X12AA—CPU port circuit pack (CP)
- NT9X13BA—CPU (static RAM) CP
- NT9X14AA—4 Mbyte memory CP
- NT9X14BA—6 Mbyte memory CP
- NT9X19AA—Filler CP
- NT9X19BA—Filler paddle board (PB)
- NT9X20AA—DS512 PB
- NT9X21AA—CM bus terminator PB
- NT9X22CA—CM subsystem clock PB
- NT9X26AA—Remote terminal interface (RTIF) PB
- NT9X27AA—CM bus extension PB
- NT9X30AA—Power converter, +5V CP
- NT9X31AA—Power converter, -5V CP

Design

Descriptions of the NT9X06AC parts appear in the following table.

NT9X06AC parts (Sheet 1 of 2)

PEC	Slot	Description Heading
NT9X12AA	17F-18F, 21F-22F	*CPU port card* The NT9X12AA provides a communication port between the CM CPU and the MS at 40.96 Mbit/s. The NT9X12AA provides 32 bit communication with CPU. The NT9X12AA provides a 32 bit mate crossover bus to mate CPU port card.
NT9X13BA	19F-20F	*CPU card* The NT9X13BA is a 20 MHz MC68020 CPU. The NT9X13BA offers memory access and write protection. The NT9X13BA uses a 4 kbyte data cache. The NT9X13BA also uses a dual channel serial communications controller (SCC).
NT9X14AA	23F-32F	*4 Mbyte memory card* Each NT9X14AA consists of two memory modules. Each module has 2 Mbyte of dynamic RAM. Each memory NT9X14AA has error checking and correction. The NT9X14AA uses a 40-bit memory width. The 40 bit memory consists of 32 bits of data, 7 check bits, and 1 parity bit.
NT9X14BA	7F 16F	*6 Mbyte memory card* Each NT9X14BA consists of three memory modules. Each module has 2 Mbyte of dynamic RAM. Each memory NT9X14BA has error checking and correction. The NT9X14BA uses a 40 bit memory width. The 40 bit memory consists of 32 bits of data, 7 check bits, and 1 parity bit.
NT9X19AA	7F 16F, 23F 32F	*Filler circuit pack* The NT9X19AA fills slots that are not used. Memory cards can occupy these slots.
NT9X19BA	8R 15R, 24R 31R	*Filler circuit pack* The NT9X19BA fills slots that are not used. Processor shelf bus extender cards (NT9X27AA) can occupy these slots.

NT9X06AC (continued)

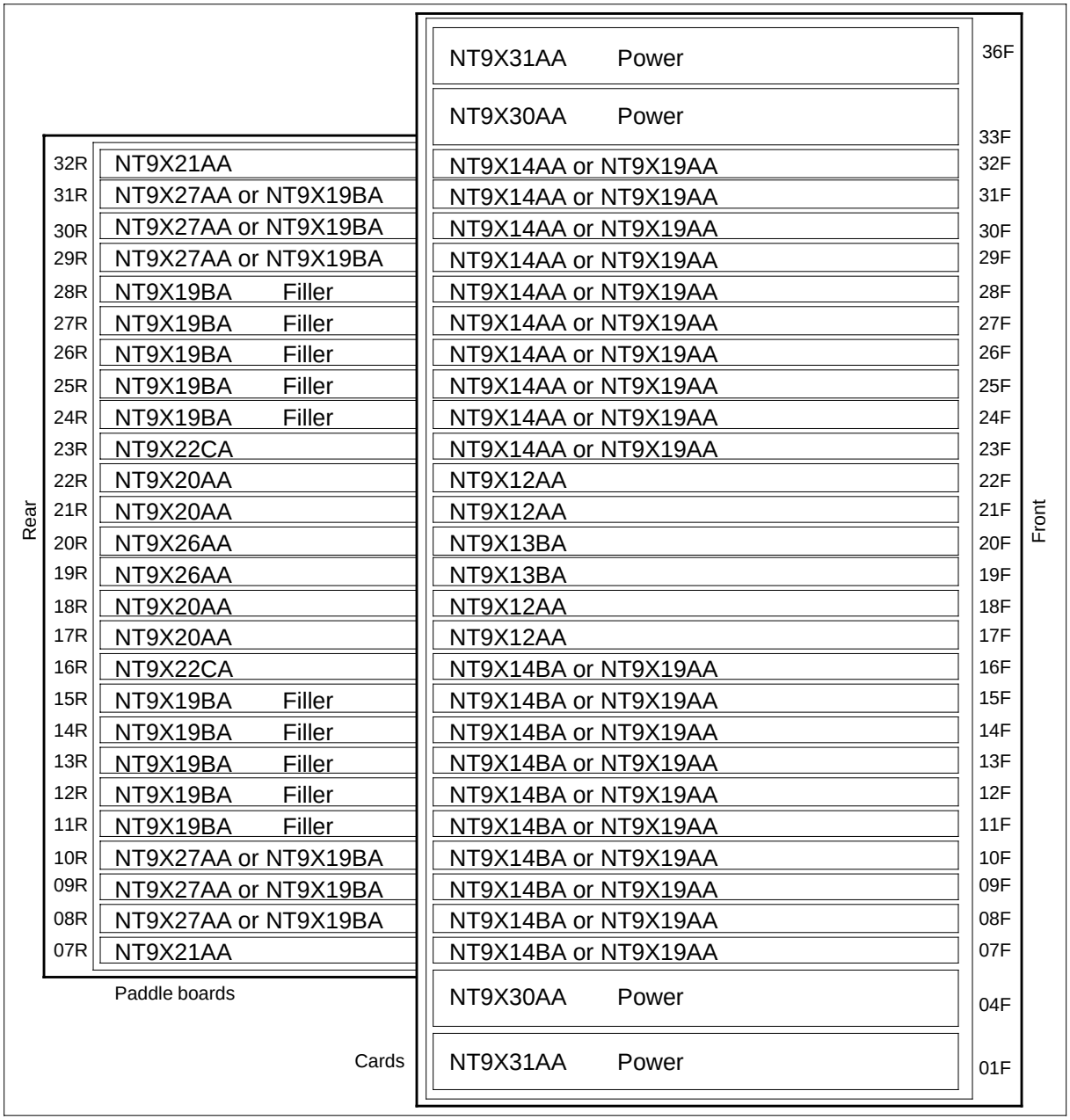
NT9X06AC parts (Sheet 2 of 2)

PEC	Slot	Description Heading
NT9X20AA	17R 18R, 21R 22R	*DS512 paddle board* The NT9X20AA provides an interface between the 9X12 CPU port card and the fiber link to the MS. The NT9X20AA performs 10 bit to 12 bit conversion.
NT9X21AA	7R, 32R	*CM bus terminator paddle board* The NT9X21AA provides termination for the system bus in the CM and extension shelf.
NT9X22CA	16R, 23R	*CM subsystem clock paddle board* The NT9X22CA inputs an 8 kHz frame pulse. The NT9X22CA outputs a 16.38 MHz synchronous clock and an 8 kHz frame pulse. These signals are phase and frequency synchronized to the input frame pulse.
NT9X26AA	19R-20R	*Remote terminal interface (RTIF)* The NT9X26AA monitors the incoming terminal and remote modem line for key words. The NT9X26AA provides a primitive person-machine interface when the CPU does not function.
NT9X27AA	8R, 31R	*CM processor shelf bus extender* The NT9X27AA is an extender for the processor bus (P-bus) from the CM processor shelf to the CM extension shelf.
NT9X30AA	4F, 36F	*Power converter, +5V* The NT9X30AA provides an output of +5.2V ±2% at the minimum of 0A to the maximum of 20A to the CPs on the NT9X06AC shelf.
NT9X31AA	1F, 33F	*Power converter, -5V* The NT9X30AA provides an output of -5.2V ±2% at the minimum of 0A to the maximum of 20A to the CPs on the NT9X06AC shelf.

The design of the NT9X06AC appears in the following figure.

NT9X06AC (end)

NT9X06AC design



NT9X06AD

Description

The computing module (CM) consists of a pair of CPUs with associated memory. The CPUs operate in a synchronous matched mode on two separate planes. One plane is active. The active plane maintains control of the system when the other plane is on standby.

The CMs provide the CPUs for the DMS SuperNode switching system. A Motorola MC68000-series microprocessor controls each CPU. To guarantee system accuracy between the active and inactive shelves, a mate exchange bus connects the CPUs. This connection allows the processors on each shelf to compare computations.

Parts

The NT9X06AD shelf contains the following parts:

- NT9X12AB—CPU port circuit pack (CP)
- NT9X13BC—CPU (static RAM) CP
- NT9X14DB—24 Mbyte memory CP
- NT9X19AA—Filler CP
- NT9X19BA—Filler paddle board (PB)
- NT9X20AA—DS512 PB
- NT9X21AA—CM bus terminator PB
- NT9X22CA—CM subsystem clock PB
- NT9X26AB—Remote terminal interface (RTIF) PB
- NT9X27AA—CM bus extension PB
- NT9X30AA—Power converter, +5V CP
- NT9X31AA—Power converter, -5V CP

Design

Descriptions of the NT9X06AD parts appear in the following table.

NT9X06AD parts (Sheet 1 of 2)

PEC	Slot	Description
NT9X12AB	17F-18F, 21F-22F	*CPU port card* The NT9X21AB provides a communication port between the CM CPU and the MS at 40.96 Mbit/s. The NT9X12AB provides 32 bit communication with CPU. The NT9X12AB provides a 32 bit mate crossover bus to mate CPU port card.
NT9X13BC	19F-20F	*CPU card* The NT9X13BC is a 20 MHz MC68020 CPU. The NT9X13BA offers memory access and write protection. The NT9X13BC uses a 4 kbyte data cache. The NT9X13BC also uses a dual channel serial communications controller (SCC).
NT9X14DB	12F-16F, 23F-27F	*24 Mbyte memory card* Each NT9X14DB consists of three memory modules. Each module has 8 Mbytes of dynamic RAM. Each memory NT9X14DB has error checking and correction. The NT9X14DB uses a 40 bit memory width. The 40 bit memory consists of 32 bits of data, 7 check bits, and 1 parity bit. The NT9X14DB provides handshake override capability. The NT9X14DB is not A-bus compatible.
NT9X19AA	7F-16F, 23F-32F	*Filler circuit pack* The NT9X19AA fills CP slots that are not used.
NT9X19BA	8R-15R, 24R-31R	Filler circuit pack The NT9X19BA fills PB slots that are not used.
NT9X20AA	17R-18R, 21R-22R	*DS512 paddle board* The NT9X20AA provides an interface between the 9X12 CPU port card and the fiber link to the MS. The NT9X20AA performs 10 bit to 12 bit conversion.

NT9X06AD (continued)

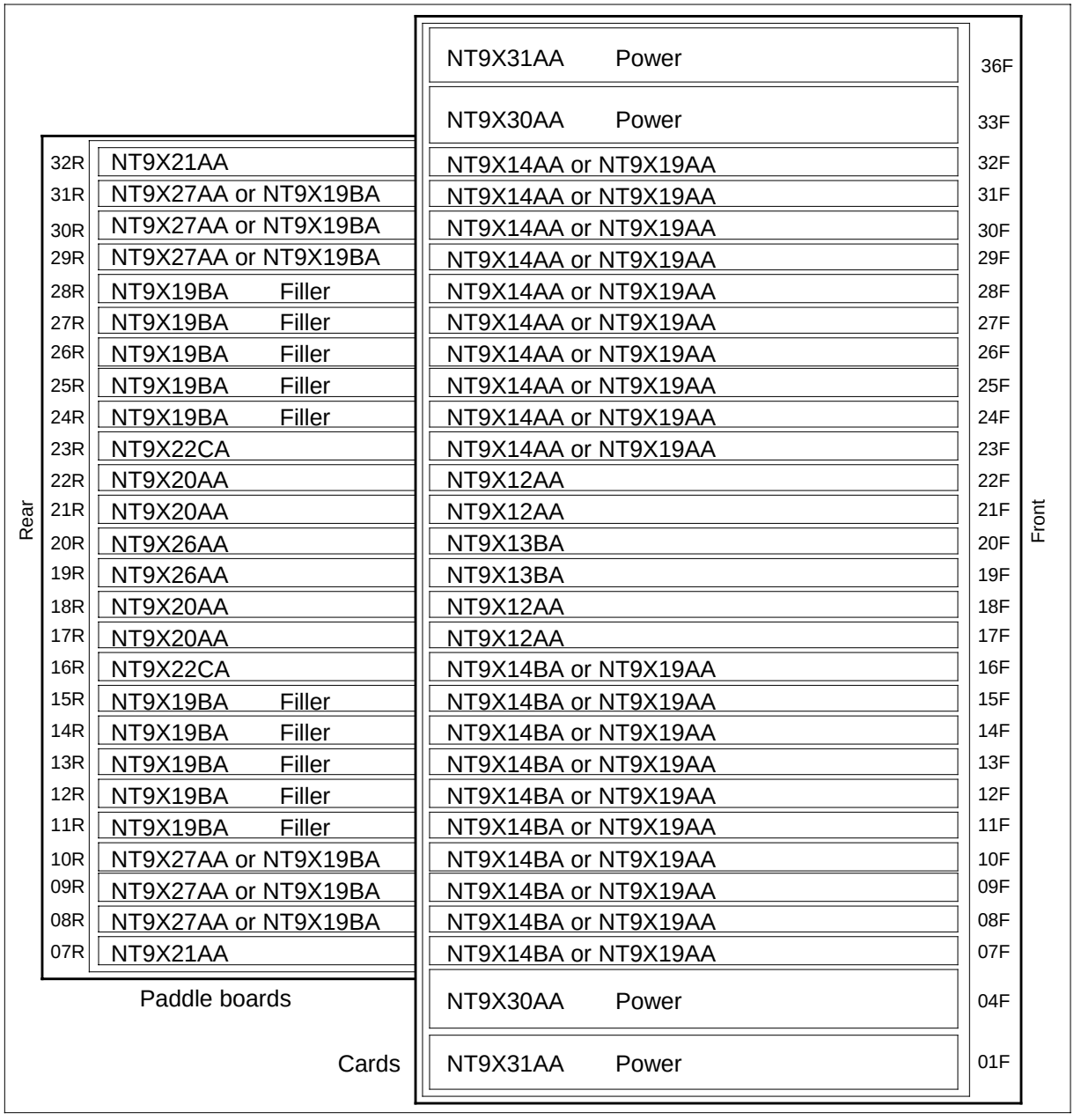
NT9X06AD parts (Sheet 2 of 2)

PEC	Slot	Description
NT9X21AA	7R, 32R	*CM bus terminator paddle board* The NT9X21AA provides termination for the system bus in the CM and extension shelf.
NT9X22CA	16R, 23R	*CM subsystem clock paddle board* The NT9X22CA inputs an 8 kHz frame pulse. The NT9X22CA outputs a 16.38 MHz synchronous clock and an 8 kHz frame pulse. These signals are phase and frequency synchronized to the input frame pulse.
NT9X26AB	19R-20R	*Remote terminal interface (RTIF)* The NT9X26AB monitors the incoming terminal and remote modem line for key words. The NT9X26AB provides a primitive person-machine interface when the CPU does not function.
NT9X27AA	8R, 31R	*CM processor shelf bus extender* The NT9X27AA is an extender for the Processor bus (P-bus) from the CM processor shelf to the CM extension shelf.
NT9X30AA	4F, 36F	*Power converter, +5V* The NT9X30AA provides an output of +5.2V ±2% at the minimum of 0A to the maximum of 20A to the CPs on the NT9X06AD shelf.
NT9X31AA	1F, 33F	*Power converter, -5V* The NT9X31AA provides an output of -5.2V ±2% at the minimum of 0A to the maximum of 20A to the CPs on the NT9X06AD shelf.

The design of the NT9X06AD appears in the following figure.

NT9X06AD (end)

NT9X06AD design



NT9X06AF

Description

The computing module (CM) consists of a pair of CPUs with associated memory. The CPUs operate in a synchronous matched mode on two separate planes. One plane is active. The active plane maintains control of the system when the other plane is on standby.

The CMs provide the CPUs for the DMS SuperNode switching system. A Motorola MC68000-series microprocessor controls each CPU. To guarantee system accuracy between the active and inactive shelves, a mate exchange bus connects the CPUs. This connection allows the processors on each shelf to compare computations.

Parts

The NT9X06AF circuit pack fill contains the following parts:

- NT9X20AA—DS512 paddle board (PB)
- NT9X21AA—CM bus terminator PB
- NT9X22CA—CM subsystem clock PB

Design

Descriptions of the NT9X06AF parts appear in the following table.

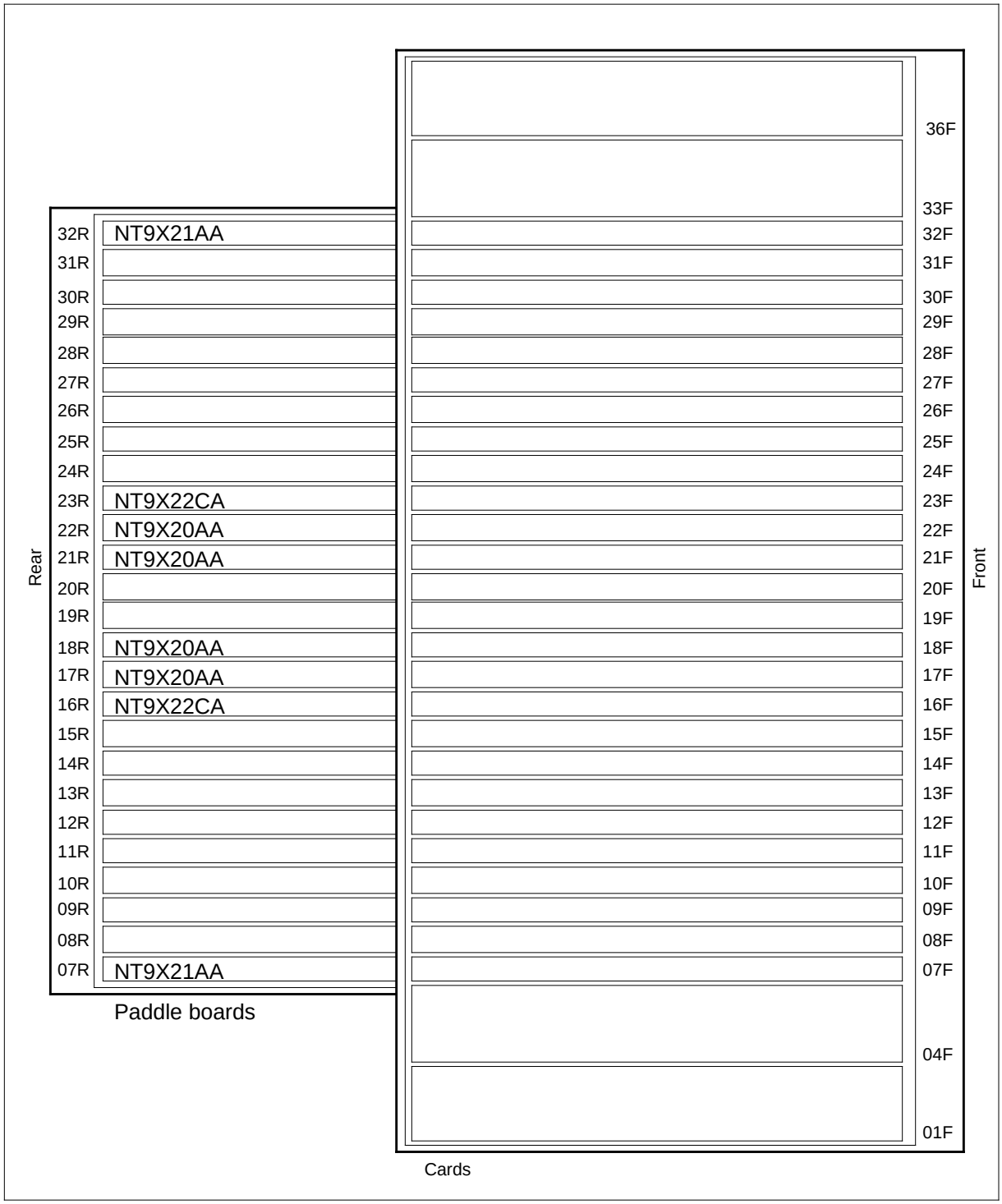
NT9X06AF parts

PEC	Slot	Description
NT9X20AA	17R-18R, 21R-22R	*DS512 paddle board* The NT9X20AA provides an interface between the 9X12 CPU port card and the fiber link to the MS. The NT9X20AA performs 10 bit to 12 bit conversion.
NT9X21AA	7R, 32R	*CM bus terminator paddle board* The NT9X21AA provides termination for the system bus in both the CM and extension shelf.
NT9X22CA	16R, 23R	*CM subsystem clock paddle board* The NT9X22CA inputs an 8 kHz frame pulse. The NT9X22CA outputs a 16.38 MHz synchronous clock and an 8 kHz frame pulse. These signals are phase and frequency synchronized to the input frame pulse.

The design of the appears in the following figure.

NT9X06AF (end)

NT9X06AF design



NT9X07CA

Description

The system load module (SLM) is a combination of a tape/disk storage unit and an array of circuit packs (CP). The tape/disk storage unit and CP provide the bootstrap device for the SuperNode. A DS30 link separates the SLM bootstrap device from the input/output (I/O) system. The DS30 connects the bootstrap device directly to a dedicated transmission port on the computing module (CM) extension shelf. The DS30 provides increased reliability and reduces load time with this action

The NT9X07CA frame provides one redundant SLM for each of the two CM processors. The port crossover bus provides both processors with access to the two SLMs.

The SLM performs the following functions:

- bootstraps the CM from disk or tape
- allows offline transfers between tape and disk in both directions
- provides a medium to which the CM can dump a core image
- provides a loadmate for the inactive CM

The SLM has a 140 Mbyte, 5.25 in. Winchester disk drive unit (DDU). The SLM has a 75 Mbyte, 0.25 in. high-speed streaming tape cartridge tape drive.

Parts

The NT9X07CA shelf has the following parts:

- the NT9X12AB—CPU port CP
- the NT9X19AA—Filler CP
- the NT9X19BA—Filler paddle board (PB)
- the NT9X21AA—CM bus terminator PB
- the NT9X22CA—CM subsystem clock PB
- the NT9X27BA—CM bus extension PB
- the NT9X30AA—Power converter, +5 V CP
- the NT9X44AA—System load module
- the NT9X46AA—Parallel port interface PB
- the NT9X47AA—Power converter, +12 V CP

Design

Descriptions for the parts of the NT9X07CA appear in the following table.

NT9X07CA parts (Sheet 1 of 2)

PEC	Slot	Description
NT9X12AB	18F, 21F	*CPU port card* The NT9X12AB provides a communication port between the CM CPU and the MS at 40.96 Mbit/s. The NT9X12AB provides a 32-bit communication link to the CPU. The NT9X12AB uses a 32-bit mate crossover bus to the mate CPU port card.
NT9X19AA	7F, 16F-17F, 20F, 22F-32F	*Filler circuit pack* The NT9X19AA fills in empty CP slots.
NT9X19BA	9R-15R, 17R, 20R, 25R-31R	*Filler circuit pack* The NT9X19BA fills in empty PB slots.
NT9X21AA	19R, 22R	*CM bus terminator paddle board* The NT9X21AA provides termination for the system bus in the CM and extension shelf.
NT9X22CA	16R, 23R	*CM subsystem clock paddle board* The NT9X22CA inputs an 8-kHz frame pulse and outputs a 16.38-MHz synchronous clock and an 8-kHz frame pulse. The clock and output frame pulse are phase and frequency synchronized to the input frame pulse.
NT9X27BA	7R, 32R	*CM processor shelf bus extender* The NT9X27BA is an extender for the processor bus (P-bus) from the CM processor shelf to the CM extension shelf.
NT9X30AA	4F, 36F	*Power converter, +5 V circuit pack* The NT9X30AA provides an output of +5.2V ±2% at a minimum of 0A to a maximum of 20A to the SLM.

NT9X07CA (continued)

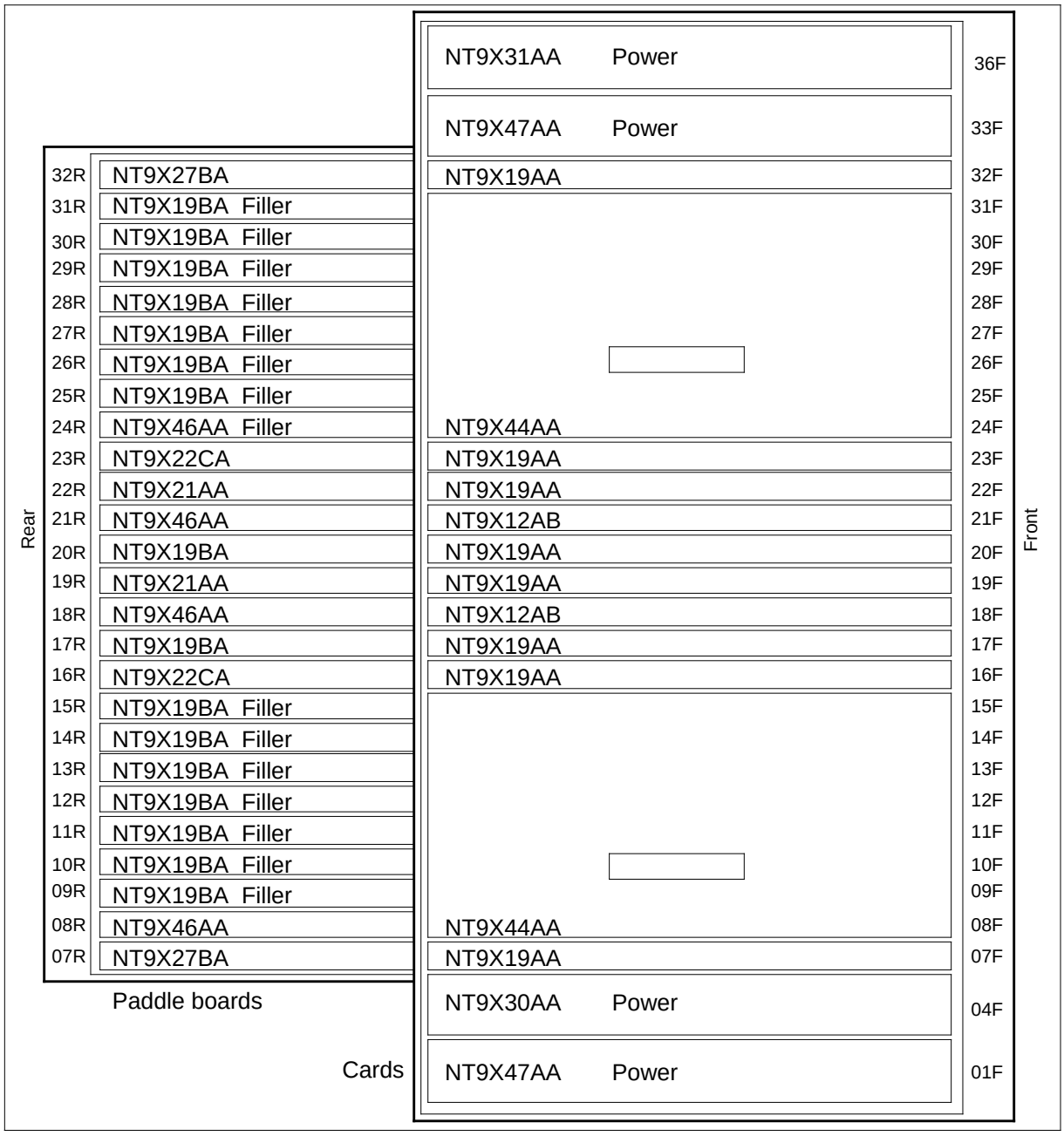
NT9X07CA parts (Sheet 2 of 2)

PEC	Slot	Description
NT9X44AA	8R, 24R	*System load module* The NT9X44AA contains the following: • a Winchester DDU • a cartridge tape drive unit • a small computer systems interface (SCSI) controller board • a disk/tape controller board (NT9X4402)
NT9X46AA	8R, 18R, 21R, 24R	*Parallel port interface paddle board* The NT9X46AA provides the interface for signals from the CPU port card to the SLM.
NT9X47AA	1F, 33F	*Power converter, +12V circuit pack* The NT9X47AA provides an output of +12V ±2% at a minimum of 0.5 A to a maximum of 20A to the CP on the NT9X07CA shelf.

The design of the NT9X07CA appears in the following figure.

NT9X07CA (end)

NT9X07CA design



NT9X10AA

Description

The NT9X10AA provides a stepped performance increase over the NT9X13 group of processors. Operating company personnel can replace this processor card with the NT9X13 DMS-core processor card. Operating company personnel cannot replace this card in a remote terminal interface (RTIF) board.

Functional description

Functional blocks

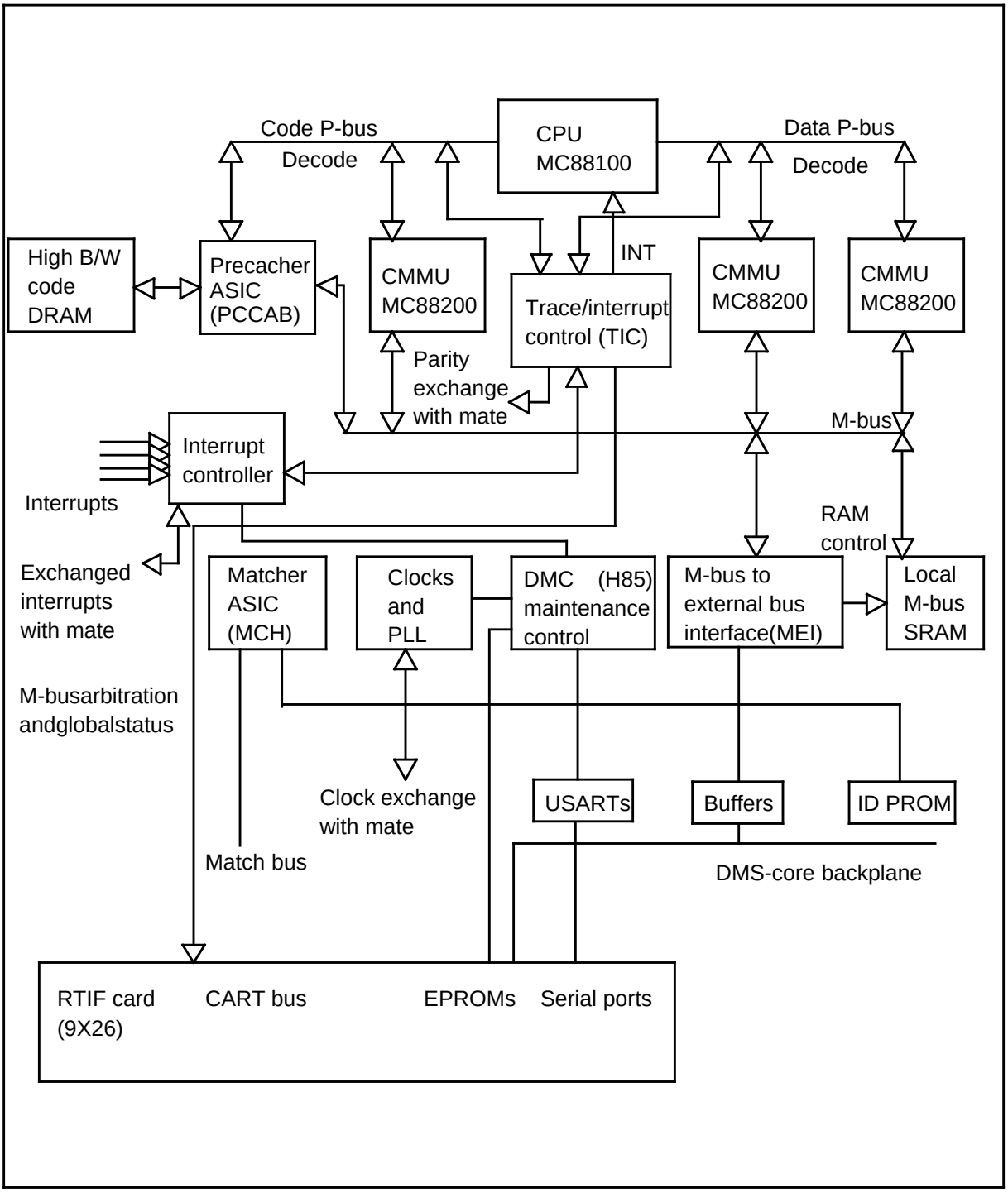
The NT9X10AA has the following functional blocks:

- the 88100 reduced instruction set computer (RISC) processor
- the 88200 cache and memory management units
- the precacher application-specific integrated circuit (ASIC) with circular content addressable buffer (PCCAB)
- the high-bandwidth code dynamic RAM (DRAM)
- the memory bus (M-bus) to external bus interface ASIC
- the local M-bus static RAM (LMS)
- the trace/interrupt controller (TIC) ASIC
- the Bell-Northern Research RISC (BRISC) interrupt controller
- the DMS-core maintenance ASIC
- the matcher ASIC
- the erasable programmable read-only memory (EPROM)
- the element identification (ID) PROM
- the element decode
- the clock control
- the M-bus arbitration and global status
- the P-bus decoding
- the interrupt windowing

The relationship between the functional blocks appears in the following figure.

NT9X10AA (continued)

NT9X10AA functional blocks



NT9X10AA (continued)

88100 reduced instruction set computer processor

The MC88100 is a RISC processor with the following features:

- 51 instructions, some with several modes
- a true Harvard architecture, which includes separate processor buses (P-buses). The P-buses are for fetching code (code P-bus) and data (data P-bus)
- the 33-MHz target clock rate
- talks on the P-bus to other P-bus devices that are normally caches, like the 88200 cache and memory management units (CMMU)
- pipelines all code and data requests to a depth of three
- an integer unit which executes all integer, bit-field and control register operations
- a register that scoreboards in the processor, which permits synchronization of execution in hardware

88200 cache and memory management units

The 88200 CMMUs are 16-kbyte caches each, in addition to the memory management capabilities. Two 88200 CMMUs are present on the data side and one 88200 CMMU is present on the code P-bus. The CMMU has the following features:

- 16-kbyte cache, four-way set associative cache
- zero wait state cache access by the CPU
- write-through and copyback cache miss modes
- cache operations defined by area (4 gigabyte), segment (4 Mbyte) and page (4 kbyte) granularity
- separate user and supervisor logical address spaces of 4 gigabytes each
- supervisor access protection and write protection for user and supervisor access
- multiprocessor investigation and cache accuracy capabilities (not in use)
- memory management unit (MMU) section has two address translation caches

Precacher ASIC with circular content addressable buffer

The precacher ASIC with circular content addressable buffer (PCCAB) is an intelligent instruction precacher for the MC88100 processor. The PCCAB attempts to hide memory latency when the PCCAB prerequests instructions from high-bandwidth memory. The PCCAB memory requests for instructions before the CPU requests these instructions. This action makes sure that each

instruction is available when accurate request occurs. The PCCAM controls multiple banks of page-mode DRAM memory. This control achieves the minimum required memory bandwidth of one instruction for each clock cycle.

High-bandwidth code dynamic RAM

The code DRAM is configured as two separate controlled banks of page-mode DRAMs. The two separate banks of the code DRAM permit twice the read/write access bandwidth of a single bank. The DRAM parts operate in page mode, and stagger accesses to the banks by one clock cycle. This DRAM activity normally allows the system to read one instruction word from memory each clock cycle.

Memory bus to external bus interface ASIC

The M-bus to the external bus interface (MEI) bridges the DMS-core environment and the 88-K RISC CPU and CMMUs. The MEI provides the following services:

- M-bus interface
- interface between the DMS maintenance controller (DMC) ASIC, the matcher (MCH) ASIC, the P-bus, and the M-bus
- continuous size adjustments of external bus
- burst memory card support
- conversion of M-bus burst accesses to sequential external bus accesses
- continuous system memory definition adjustment as non-existent system maintenance on a 256-Mbyte segment base for the following:
  - — P-bus
  - — memory controller ASIC bus
  - — hi-performance bus
  - — DMS-core base
  - — local M-bus SRAM (LMS)
- parity checks for M-bus and external bus
- local M-bus static RAM (SRAM) control of from 1 to 8 Mbyte of memory. This control addresses translation table entries and supports access protection override.
- support of different copy modes: simplex copy, LMS update, external bus update and duplex copy

NT9X10AA (continued)

- maintenance features like parity checks, duplex handshake control, response time-out detection, mismatch override, sanity freeze control, and incompatible access type detection
- over 32 error and system state registers

Local M-bus static RAM

The MEI controls one Mbyte of SRAM, which resides directly on the M-bus. The local M-bus static RAM is configured as a longword device that supports byte-wide and burst operations. The SRAM array contains data and stores a parity bit for each byte. Initialize the memory array before you activate the M-bus parity.

Trace/interrupt controller ASIC

The TIC ASIC is compatible with the Motorola MC88100 microprocessor in the DMS-core. The TIC ASIC monitors both the code and data address bus. The TIC ASIC monitors the data bus of the data port and six bits of the code data bus.

The TIC ASIC monitors these buses to provide the following functions:

- debugging support
- trace execution for maintenance purposes
- the ability to exchange a parity bit with the TIC ASIC mate TIC when the TIC ASIC runs in synchronization. This action occurs for match purposes.

BRISC interrupt controller

The BRISC interrupt controller design is an attempt to assist software to handle interrupts quickly and with low overhead. Approximately 7000 interrupts occur each second in a switch that runs. The TIC ASIC contains the final interrupt controller stage to facilitate the quick handling of interrupts. The interrupt controller performs most of the interrupts with XILINX in the 1W1 stage, and as an ASIC for 0D1 activity.

DMS-core maintenance ASIC

The BRISC design uses the DMS-core maintenance ASIC (DMC-H85) from the NT9X13GA design. The DMC-H85 provides the following features:

- interval and sanity timer
- serial maintenance port
- matcher interface
- activity control
- reset control

- state indication register
- clock source failure monitor and clock selection logic

Matcher application-specific integrated circuit

The main functions of the matcher are:

- to match external bus backplane cycles in duplex mode
- to exchange data between planes while in simplex mode (through MCR) or in duplex mode (through the mate exchange bus)

EPROM

The BRISC paddleboard contains the EPROM, which includes all executable CPU firmware. The EPROM is on the BRISC paddle board as a P-bus slave. The MEI provides an address decode signal to the RTIF.

Element identification PROM

The NT9X10AA IDPROM is like other DMS-core cards. The MEI and the programmable array logic (PAL) perform the decode for the PROM. A PAL implements a state machine to control the P-bus response.

Element decode

The PAL logic that decodes the element block for the IDPROM decodes element block 7. The PAL logic forwards this decode to the RTIF. Element 7 corresponds to the IDPROM address for the RTIF.

Clock control

The BRISC board CPU and CMMUs operate at 33 MHz. The tight clock skew and duty cycle requirements of these devices are met with the use of a phase-lock loop (PLL). The Motorola 915PLL chip provides the PLL technology. The PLL locks to a 16-MHz clock exchanged between the two planes. The PLL regenerates a 16-MHz and several 33-MHz clocks.

M-bus arbitration and global status

This block is the central M-bus arbiter. One PAL implements the arbitration logic. The arbitration logic gives priority to the data CMMUs. The bus requests of all CMMUs can be programmed to operate in fairness arbitration or priority arbitration mode. In the fairness protocol, all CMMUs assert bus request when other M-bus master do not have a pending request for mastership. In the priority mode, the CMMU ignores the requests of other masters to assert bus request. In both events, the bus arbitration PAL assigns higher priority to the data CMMUs.

NT9X10AA (continued)

Processor bus decoding

The PAL logic decodes P-bus addresses. The P-bus addresses select PCCAB and code CMMU or data CMMU A and data CMMU B.

Interrupt windowing

Level 1, 2, and 3 can be windowed with CPU branch instruction requests. This feature sets a bit in the TIC and generates windowable Windowing results in windowable interrupts to the processor. This event occurs only when valid branch instruction requests occur.

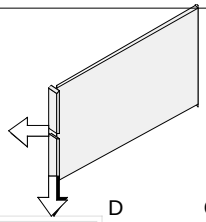
Signaling

Pin numbers

The pin numbers for the NT9X10AA appear in the following figure.

NT9X10AA (continued)

NT9X10AA pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2	OM22P	OM17P	OM00P	GND
3	IM23P	IM18P	IM01P	GND
4	OM23P	OM18P	OM01P	GND
5	IM24P	IM19P	IM02P	GND
6	OM24P	OM19P	OM02P	GND
7	IM25P	IM20P	IM03P	GND
8	OM25P	OM20P	OM03P	GND
9	IM26P	IM21P	IM04P	GND
10	OM26P	OM21P	OM04P	GND
11	IM27P	PBOP	IM05P	GND
12	OM27P	PBIP	OM05P	GND
13		DSON	IM06P	TXDA
14	MASTER-	DSIN	OM06	CARTD28
15	CPUN+	IJAMIN	IM07P	CARTD29
16	OOB-IN	GRD	OM07P	RTSA
17	PERINT6-	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-	OM08P	RXDA
19	BUSREQ-	PERINT2-	IM09P	
20	DS-	PERINT3-	OM09P	DTR-REQA
21	OOB-IN1	PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-	OM10P	TXDB
23	RSTOUT-	BUSLOCK-	IM11P	CARTD30
24	PERINT1-	PERINT0-	OM11P	CARTD31
25	BEN1-	BEN0-	IM12P	RTSB
26	BEN3-	BEN2-	OM12P	DCDB
27	GRD	DAS-	IM13P	RXDB
28	WRT-	GRD	OM13P	
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-	OM14P	FP97
31	PRTYEN-	MEMERR-	IM15P	C97
32	FAS-	GRD	OM15P	SH0
33	DAS32-	CPUCLK+	IM16P	SH1
34	DATA00	EDAS-	OM16P	FP61-
35	DATA01	ADDR01	TYPE1	C61
36	DATA02	ADDR02	HW0	-5V
37	DATA03	ADDR03	HW1	-5V
38	DATA04	ADDR04	HW2	-5V
39	DATA05	ADDR05	HW3	-5V
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07	CMLINE	GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09	PBRST+	GND
44	DATA10	ADDR10	PBRST-	5V
45	DATA11	ADDR11	PERR-	5V

	D	C	B	A
46	DATA12	ADDR12	DISABSAN	-5V
47	DATA13	ADDR13	GRD	5V
48	DATA14	ADDR14	FACKN	5V
49	DATA15	ADDR15	ENOMN	5V
50	DATA16	ADDR16	DCDVM	5V
51	DATA17	ADDR17	DCDMM	5V
52	DATA18	ADDR18	DCDV	5V
53	DATA19	ADDR19	DCDM	5V
54	DATA20	ADDR20	OJAMIN	5V
55	DATA21	ADDR21	GRD	5V
56	DATA22	ADDR22	GRD	TYPE0
57	DATA23	ADDR23	ISHFTD	OSHFTD
58	DATA24	ADDR24	ISTRD	OSTRD
59	DATA25	ADDR25	ISTWR	OSTWR
60	DATA26	ADDR26	ISPARE	OSPARE
61	DATA27	ADDR27	GRD	GRD
62	DATA28	ADDR28	CARTD10	CARTCK
63	DATA29	ADDR29	CARTD11	CARTINTN
64	DATA30	ADDR30	CARTD12	CARTD00
65	DATA31	ADDR31	CARTD13	GRD
66	ETYPE0	FC0+	CARTD14	GRD
67	ETYPE1	FC1+	CARTD15	CARTD01
68	ETYPE2	FC2+	CARTD16	CARTD02
69	ETYPE3	CARTD27	CARTD17	CARTD03
70	ETYPE4	PSPARE1	CARTD18	GRD
71	RSTIN	IM28P	CARTD19	GRD
72	RSTON	OM28P	CARTD20	CARTD04
73	CLPIN	IM29P	CARTD21	CARTD05
74	CLKOP	OM29P	CARTD22	CARTD06
75	IMCRN	IM30P	CARTD23	GRD
76	OMCRN	OM30P	CARTD24	CARTD07
77	IMCWN	IM31P	CARTD25	CARTD08
78	OMCWN	OM31P	CARTD26	CARTD09
79	IMMN	SYNC16-	DTR-REQB	GND
80	OMMN	SYNC16-	CTS	GND
81	ACTIN	MSCCN		GND
82	ACTON	OSCCN	RTIFINTN	GND
83	OFFIN	IPR0N	RTIFRAMN	GND
84	OFFON	OPR0N	FWPROMN	GND
85	IFRCN	IPR1N	NMIN	GND
86	OFRCN	OPR1N	CKFLN	GND
87	IFRLN	IPR2N	CKACTN	GND
88	OFRLN	OPR2N	JAMIN	GND
89	IFRDP	IPR3N	IDPROMN	GND
90	OFRDP	OPR3N	RISCN	GND

NT9X10AA (continued)

Technical data

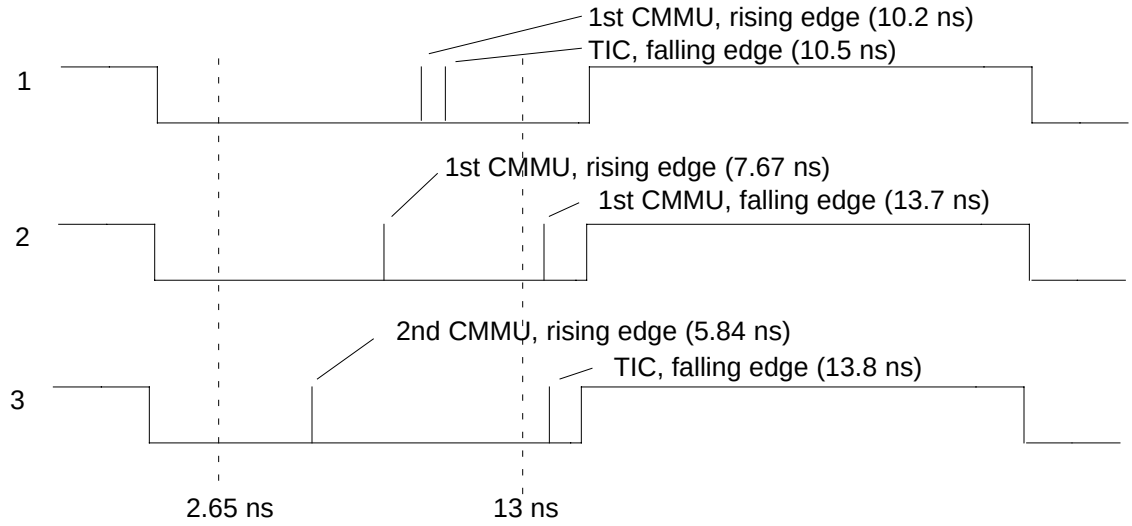
Power requirements

The voltage required is 5V ±0.25V.

Timing

The following figures show the timing diagrams for the NT9X10AA.

NT9X10AA P-bus timing margins

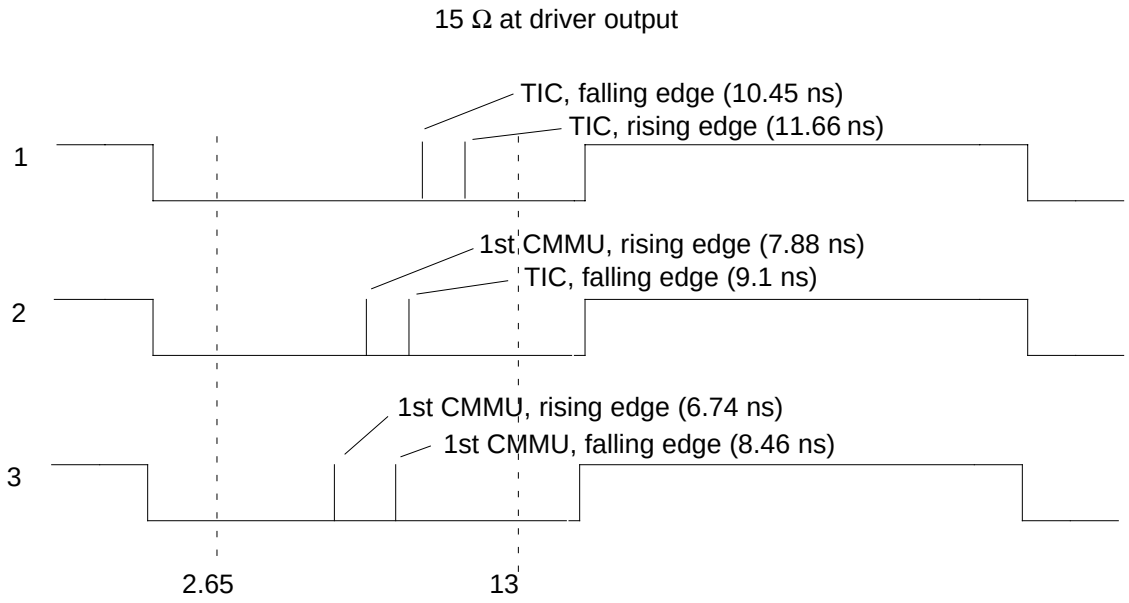


Legend

1 Best: Vdd = 4.75 V, T = 85C, CMOS dimensions larger than mean
2 Nominal: Vdd = 5 V, T = 25C, CMOS dimensions are at mean
3 Worst: Vdd = 5.25 V, T = 0C, CMOS dimensions smaller than mean

The vertical lines refer to the longest observed settling times and the locations where they occur for the P-bus simulation. The signal is valid 2 ns prior to the clock rising edge and is not available prior to 2.65 ns after the clock falling edge.

NT9X10AA P-bus timing margins with 15 W terminations



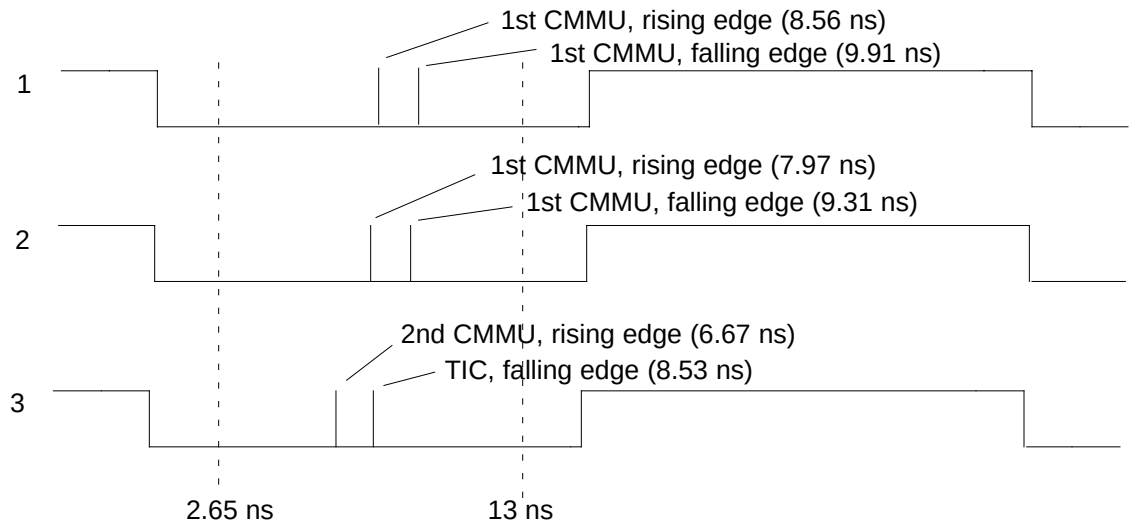
Legend

1 Best: Vdd = 4.75 V, T = 85C, CMOS dimensions larger than mean
2 Nominal: Vdd = 5 V, T = 25C, CMOS dimensions are at mean
3 Worst: Vdd = 5.25 V, T = 0C, CMOS dimensions smaller than mean

The vertical lines refer to the longest observed settling times and the locations where they occur for the P-bus simulation. The signal is valid 2 ns prior to the clock rising edge and is not available prior to 2.65 ns after the clock falling edge.

NT9X10AA (continued)

NT9X10AA P-bus timing margins using M-bus drivers

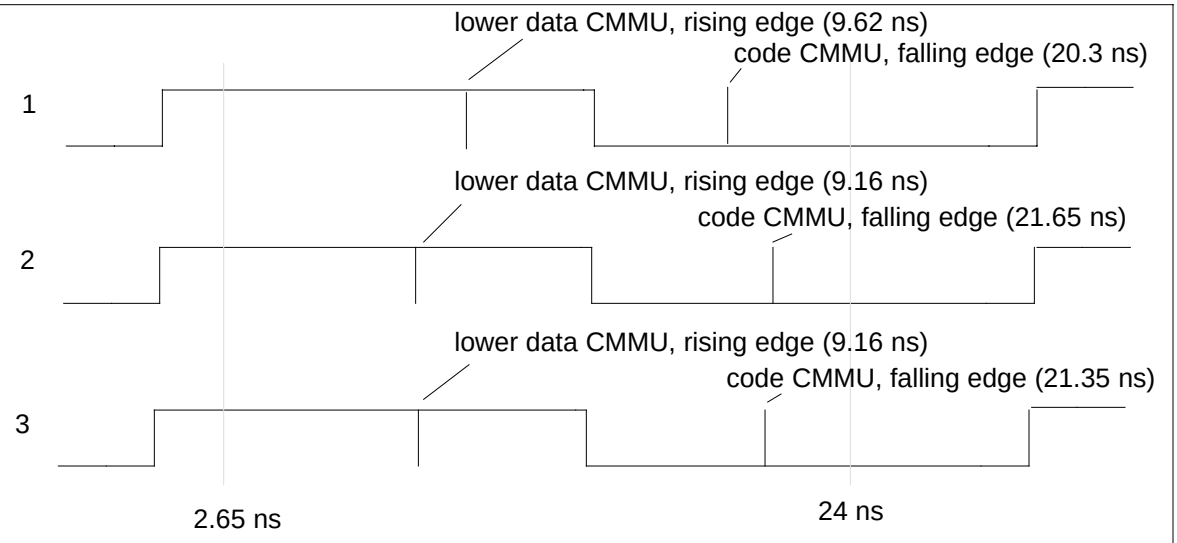


Legend

1 Best: Vdd = 4.75 V, T = 85C, CMOS dimensions larger than mean
2. Nominal: Vdd = 5 V, T = 25C, CMOS dimensions are at mean
3. Worst: Vdd = 5.25 V, T = 0C, CMOS dimensions smaller than mean

The vertical lines refer to the longest observed settling times and the locations where the lines occur for the P-bus simulation. The signal is valid 2 ns prior to the clock rising edge and is not available prior to 2.65 ns after the clock falling edge.

NT9X10AA M-bus timing margins



Legend

1 Best: Vdd = 4.75 V, T = 85C, CMOS dimensions larger than mean
2. Nominal: Vdd = 5 V, T = 25C, CMOS dimensions are at mean
3. Worst: Vdd = 5.25 V, T = 0C, CMOS dimensions smaller than mean

The vertical lines refer to the longest observed settling times and the locations where the lines occur for the M-bus simulation. The signal is valid 6 ns prior to the clock rising edge and is not available prior to 2.65 ns after the previous clock rising edge.

NT9X10DA

Product description

The NT9X10DA Series 70/EM66 BNR reduced instruction set computer (BRISC) CPU card provides increased performance over the NT9X10AA CPU. It also maintains Series 70 performance for large software loads. The NT9X10DA card is identical to the Series 70/EM BRISC CPU card (NT9X10CA), except that it runs at 66.3552 MHz. The NT9X10DA CPU card can replace the Series 50/60/70 BRISC CPU and the NT9X13 cards. The NT9X10DA card also requires the replacement of the RTIF cards with the NT9X26GA card.

The NT9X10DA processor card, the NT9X26GA RTIF card, and the optional NT9X14FA memory card are designed to be used together. The NT9X10DA CPU card functions only with the NT9X26GA RTIF paddle board and the optional NT9X14FA extended memory card.

Functional description

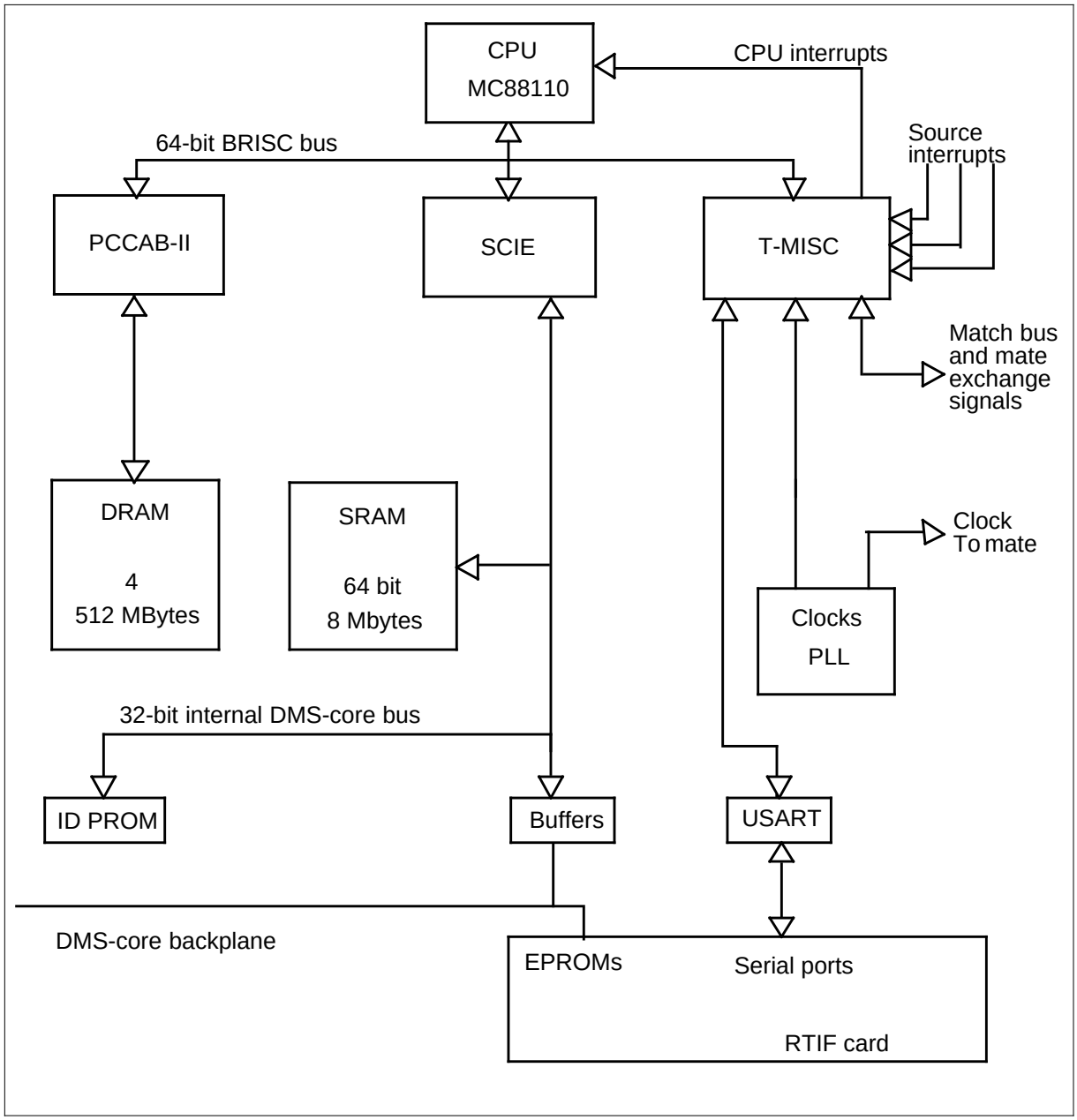
Functional blocks

The NT9X10DA card consists of the following functional blocks:

- 88110 reduced instruction set computer (RISC) processor
- 64-bit BRISC bus
- pre-cacher application-specific integrated circuit (ASIC) with a type-II circular content addressable buffer (PCCAB-II)
- high-bandwidth code dynamic random access memory (DRAM)
- static RAM (SRAM) controller and interface to ECORE bus ASIC (SCIE)
- tracer, matcher, interrupt, synchronization controller (T-MISC)
- erasable programmable read-only memory (EPROM)
- element identification programmable read only memory (ID PROM)
- clock control
- BRISC bus control
- interrupt windowing
- series test access port master (STAPM)

The following figure shows the relationship between the functional blocks.

NT9X10DA functional blocks



88110 reduced instruction set computer processor

The MC88110 is a RISC processor with the following features:

- 66 instructions, some with several modes
- 66.3552MHz target clock rate
- 2 separate 8-Kbyte internal caches, one for code, one for data.

NT9X10DA (continued)

- internal Harvard architecture in which separate processor buses (PBUS) provide fetching of code (code PBUS) and data (data PBUS)
- only 1 combined PBUS with a datapath width of 64bits
- the 88110 is a Superscaler processor. It has multiple execution units, and can launch up to two instructions per clock.

BRISC bus

The BRISC bus allows communication between the 88110 processor, the PCCAB-II, the T-MISC, and the SCIE.

The BRISC bus supports the following features:

- double-word, word, half-word, and byte non-burst transactions
- (4-beat) burst code and data transactions
- critical word first on all burst transactions
- parity checking on all 64 data bits, on a byte basis
- update mode handshaking

Pre-cacher ASIC and high-bandwidth code DRAM (PCCAB-II)

The PCCAB-II provides instruction prefetching and caching.

The features of the PCCAB-II are as follows:

- BRISC-bus interface
  - — compatible with the 88110 processor bus protocol
  - — critical-word-first operation on burst access
- cache memory
  - — 32-line content-addressable cache memory
  - — 1 wait-state operation for the first 64-bit transfer, and 0 wait-states for subsequent transfers
  - — dual-ported cache for compare and write access in the same cycle
- instruction access
  - — straight program path prefetching of instructions
- data access
  - — data write buffer for 1 wait-state response for the initial beat in burst access, and 0 wait-states for subsequent beats
  - — supports read-modify-write for byte, half-word, or half-beat writes

- DRAM interface
  - — 64-bit-wide data paths
  - — control for interleaved memory banks with 2 subbanks
  - — sustainable burst bandwidth of up to 64 bits per clock
  - — ECC protection on DRAM array
- user features
- 32-bit hit-and-miss counters allow operating personnel to gather statistics about PCCAB performance

SRAM controller and interface to Ecore bus ASIC (SCIE)

The SCIE performs two functions on the Series 70/EM66 CPU card:

- it interfaces between the BRISC bus and the DMS SuperNode backplane memory bus (MEMBUS)
- it controls the local processor bus SRAM

The features of the SCIE are as follows:

- 20 MHz DMS backplane operation
- DMS PBUS accesses
- DMS MEMBUS accesses
- DMS burst MEMBUS accesses
- backplane parity generation, checking, and error detection
- response time-out detection
- access compatibility detection
- exception handling for each supported bus
- support for alternate MEMBUS master arbitration
- BRISC bus interface
- write buffer allows 2,0,0,0 wait state writes, and it forgets BRISC bus burst writes
- longer response time-out value
- 16-entry content addressable memory (CAM) based address range decoding
- byte smearing for all accesses that are not 64-bit accesses
- bus parity generation
- bus parity error detection

NT9X10DA (continued)

- support of 8 Mbytes through 64 Mbytes of 64-bit-wide SRAM using 1 Mbit by 4 bit, or 4 Mbit by 4 bit SRAMs
- ECC protection of SRAM
- test access to ECC RAMs
- ECC protection on addresses for increased duplex fault isolation

Tracer, matcher, interrupt, synchronization controller (T-MISC)

The T-MISC is the ASIC for the Series 70/EM66 processor card, which incorporates the functions of the following ASICs found on the SR50 processor card:

- G62 matcher
- H85B DMS maintenance controller (DMC)
- J38 trace/interrupt controller (TIC)
- J50B BIC

The features of the T-MISC are as follows:

- duplex operation matching of the BRISC bus address, data, and processor PSTAT signals between planes
- read update mode used for getting processors into synchronized operation
- update list memory
- mate communication register (MCR) support for communication between processors during upgrades
- enhanced MCR provides higher-speed MCR operation
- universal asynchronous receiver/transmitter (UART), or serial communication controller (SCC) control for communication with the remote terminal interface (RTIF) terminal
- sanity timer and super-sanity timer
- activity control
- clock switch control
- interrupt controller
- reset controller
- SOS timer
- synchronization and on-line control
- mate fault indication register (FIR) communication
- tracer

EPROMs

Like the SR50 processor, the EPROMs that contain the 88110 executable CPU firmware are located on the RTIF board.

Element identification PROM (ID PROM)

The SCIE and the STAPM incorporate the NT9X10DA ID PROM circuits. The SCIE decodes the shelf and hardware address for the NT9X10DA card and requests ID PROM information from the STAPM.

Clock control

The 88110 BRISC CPU and the BNR ASICs operate at 66.3552 MHz. These devices use phase-lock loop (PLL) technology to meet tight clock skew and duty cycle requirements. The 88110 BRISC CPU and the BNR ASICs use the Motorola MPC974 clock PLL chip. The PLL locks to a 22.1184-MHz clock exchanged between both planes and regenerates 20-MHz and 66.3552-MHz outputs.

BRISC bus control

Each ASIC handles all address decoding and all acknowledge generation on the 66.3552-MHz BRISC bus. The three ASICs have a common BRISC bus control block.

Interrupt windowing

Interrupt windowing is enabled by setting a bit in the 88110 processor control register. Interrupt levels 1 to 3 are handled inside the 88110 processor. When the decoding of valid branch instructions occurs, the processor generates the interrupt.

Series test access port master (STAPM)

The STAPM acts as the test or scan mode of operation (JTAG) bus master. The STAPM controls the 5-pin JTAG IEEE1149.1 bus that is routed between the 88110 and the BNR ASICs. The STAPM runs all built-in self test (BIST) and scan tests under software control.

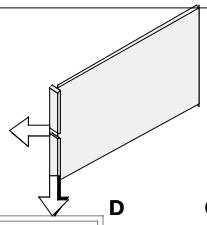
Signaling

Pin outs

The following figure shows the pin outs for the NT9X10DA.

NT9X10DA (continued)

NT9X10DA pin outs



	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2	OM22P	OM17P	OM00P	GND
3	IM23P	IM18P	IM01P	GND
4	OM23P	OM18P	OM01P	GND
5	IM24P	IM19P	IM02P	GND
6	OM24P	OM19P	OM02P	GND
7	IM25P	IM20P	IM03P	GND
8	OM25P	OM20P	OM03P	GND
9	IM26P	IM21P	IM04P	GND
10	OM26P	OM21P	OM04P	GND
11	IM27P	MPWROUT	IM05P	GND
12	OM27P	MPWRIN	OM05P	GND
13		DSON	IM06P	TXDA
14	MASTER-	DSIN	OM06	
15	CPUN+	IJAMIN	M07P	
16	OOB-IN0	GRD	OM07P	RTSA
17	PRNT6-	BUSGRI-	IM08P	DCDA
18	PRNT7-	BUSGRO-	OM08P	RXDA
19	BUSREQ-	PRNT2-	IM09P	JGTXD
20	DS-	PRNT3-	OM09P	DTR-RA
21	OOB-IN1	PRNT4-	IM10P	CTSA
22	BUSBSY-	PRNT5-	OM10P	TXDB
23	RSTOUT-	BUSLOCK-	IM11P	
24	PRNT1-	PRNT0-	OM11P	JGRXD
25	BEN1-	BEN0-	IM12P	RTSB
26	BEN3-	BEN2-	OM12P	DCDB
27	GRD	BRSTAS-	IM13P	RXDB
28	WRT-	GRD	OM13P	JGRTS
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-	OM14P	FP97
31	PRTYEN-	MEMERR-	IM15P	C97
32	FAS-	GRD	OM15P	SH0
33	DAS32-	CPUCLK+	IM16P	SH1
34	DATA00	BRSTAK-	OM16P	FP61-
35	DATA01	ADDR01	TYPE1	C61
36	DATA02	ADDR02	HW0	-5V
37	DATA03	ADDR03	HW1	-5V
38	DATA04	ADDR04	HW2	-5V
39	DATA05	ADDR05	HW3	-5V
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07	CMLINE	GND
42	DATA08	ADDR08	CMSC	GND
43	DATA09	ADDR09	PBRST+	GND
44	DATA10	ADDR10	PBRST-	5V
45	DATA11	ADDR11	PERR-	5V

	D	C	B	A
46	DATA12	ADDR12	DISABSAN	5V
47	DATA13	ADDR13	GRD	5V
48	DATA14	ADDR14	FACKN-	5V
49	DATA15	ADDR15	ENOMN	5V
50	DATA16	ADDR16	DCDVM	5V
51	DATA17	ADDR17	DCDMM	5V
52	DATA18	ADDR18	DCDV	5V
53	DATA19	ADDR19	DCDM	5V
54	DATA20	ADDR20	OJAMIN	5V
55	DATA21	ADDR21	GRD	5V
56	DATA22	ADDR22	GRD	TYPE0
57	DATA23	ADDR23	ISHFTD	OSHFTD
58	DATA24	ADDR24	ISTRD	OSTRD
59	DATA25	ADDR25	ISTWR	OSTWR
60	DATA26	ADDR26	ISPARE	OSPARE
61	DATA27	ADDR27	GRD	GRD
62	DATA28	ADDR28	JGCTS	JGTCK
63	DATA29	ADDR29	L+5V	JGTRST
64	DATA30	ADDR30	L+5V	JGTMS
65	DATA31	ADDR31	L+5V	GRD
66	ETYPE0	FC0+	L+5V	GRD
67	ETYPE1	FC1+	L+5V	JGTDI
68	ETYPE2	FC2+	L+5V	JGTDO
69	ETYPE3	RTIFROMN	L+5V	
70	ETYPE4	PSPARE1	L+5V	GRD
71	RSTIN	IM28P	L+5V	GRD
72	RSTON	OM28P	L+5V	
73	SPRIN	IM29P	L+5V	
74	SPROUT	OM29P	L+5V	
75	IMCRN	IM30P	L+5V	GRD
76	OMCRN	OM30P	L+5V	
77	IMCWN	IM31P	L+5V	
78	OMCWN	OM31P		
79	IMMN	IFIRN	DTR-REQB	GND
80	OMMN	OFIRN	CTSB	GND
81	ACTIN	MSCCN	CLKVLDN	GND
82	ACTON	OSCCN	RTIFINTN	GND
83	OFFIN	IPSM0P	RTIFRAMN	GND
84	OFFON	OPSM0P	FWPROMN	GND
85	ACTIP	IPSM1P	NMIN	GND
86	ACTOP	OPSM1P	CKFLN	GND
87	SPRIN	IPSM2P	CKACTN	GND
88	SPROUT	OPSM2P	JAMIN	GND
89	CLKOP	IMINTP	IDPROMN	GND
90	CLPIN	OMINTP	RISCN	GND

CMSC = CMSYNC
DTR-RA = DTR-REQA
JG = JTAG
PRNT = PERINT
SPRIN = SPARE XOVR IN
SPROUT= SPARE XVR OUT

Technical data

Power requirements

The voltage required is 5 V ±0.25 V.

NT9X12AB

Product description

The NT9X12AB CPU port card is part of the processor complex of the DMS-100E system. The main function of the port card is to provide a high-bandwidth communications link between the CPU and the message switch. The transport medium can be a DS512 fiber optic link with a 40.96 Mbit/s capacity. The transport medium can be a DS30 transmission link with a 2.084 Mbit/s capacity. The card supports four link protocols.

A standard configuration contains four port cards for each system. Each half of the processor has two port cards in the card slots next to each processor.

Functional description

Functional blocks

The NT9X12AB has the following functional blocks:

- 68020 A32 bus interface
- mate crossover A32 bus interface
- parity generation
- time-of-day register
- gate array interface for the Bus Access Circuit (BAC) and LH gate arrays
- bus access circuit (BAC gate array)
- link handler circuit (LH gate array)
- transmit first-in first-out (FIFO) RAM
- 2 kbytes of RAM (receive buffer)
- paddle board interface
- control and status registers
- split-mode header register

68020 A32 bus interface

The 68020 A32 bus provides 32 bits of data, 32 bits of address, interrupt and bus access control lines. The CPU card NT9X13AA is the master of a bus transaction. The master must wait for acknowledgement from the before the master completes the transaction. The processor data store acknowledge controls the transactions.

Mate crossover A32 bus interface

When the CM processors are in a duplex mode, the active processor has read and write access to all port cards equipped. When the CM processors are in the duplex mode, the inactive processor has read-only access.

Parity generation

Parity generation occurs across the address and data bus during read and write transactions. The parity operation on a bus transaction depends on the port card that asserts PARITY ENB. The port card asserts PARITY ENB to inform the processor to verify parity on this bus transaction.

Time-of-day register

The CPU port card supports a 48-bit timer synchronized to the 125-µs transmit frame pulse. The 48-bit timer is a real time clock. The timer provides wraparound on the counter chain of a minimum of 1000 years.

Gate array interface

To provide access to the BAC and link handler gate arrays, the correct address and data leads are buffered to the gate arrays. The chip selects are also buffered. The chip selects correspond to the element block address range plus a read/write lead. The gate arrays respond with acknowledge that drives the A32 bus DSACK lines.

Bus access circuit

The BAC provides memory control for data input/output to the appropriate memories. The bus access circuit has three sections:

- link to buffer—writes extracted data received from the link handler into the buffer memory. The link provides read access of the buffer to the bus interface of the port card.
- bus to FIFO to link—writes the data for transmission in to the FIFO memory. The bus reads the data from the FIFO. The protocol interface between BAC and link handler controls the FIFO.
- microprocessor interface—configures the different operational modes of the BAC. The interface provides status information.

Link handler circuit

The link handler is a CMOS semi-custom gate array. The link handler is a part of a chip set that controls the message flow in DMS-100E. The link handler

NT9X12AB (continued)

acts as a protocol converter for the DS30, DMS-X, DMS-Y and framer byte oriented protocols. The link handler has four functional blocks:

- transmit—works with control block to send state codes and messages from the FIFO. These messages are in a correct format.
- receive—works with control block to extract state codes and messages. The control blocks and state codes are sent to the buffer memory.
- microprocessor—configures the operational mode of the link handler. Provides status information.
- control—works with transmit to send state codes and messages from the FIFO. The state codes and messages are in a correct format. Works with receive to extract block state codes and messages that are sent to the buffer memory.

Transmit first-in first-out RAM

The transmit FIFO RAM of 16 kbytes stores the messages for transmission. The data written in to the FIFO from the bus are done on long work, 32-bit boundaries. The BAC controls the data written into the FIFO. The data read from the FIFO to the link handler are done on 8-bit byte boundaries. The BAC controls the read of the data from the FIFO.

Receive buffer RAM

The receive buffer RAM stores a single message received from a message switch. The data written into the buffer RAM from the link handler are done on 8-bit byte boundaries. The BAC controls this process. Data read from the buffer RAM to bus interface is done on 32-bit longword boundaries. The BAC controls this process.

Paddle board interface

You can use the paddle board interface between the card and paddle board with the NT9X20AA or the NT9X23AA. The NT9X20AA is a DS512 paddle board. The NT9X23AA is DS30 four-port paddle board.

Control and status registers

Control and status registers in the card monitor the board.

Split-mode header register

The split mode header register modifies the destination address of a data message to be written to the FIFO on a simplex CPU. Only the active CPU can write on the register. The card must be in the inactive CPU plane. Split mode refers to a mode with both planes equipped and operational. These planes are not synchronized.

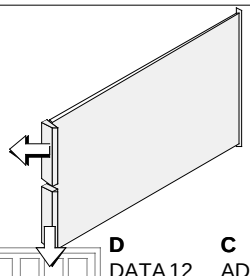
Signaling

Pin numbers

The pin numbers for the NT9X12AB appear in the following figure.

NT9X12AB (continued)

NT9X12AB pin numbers



	D	C	B	A
1				GND
2				GND
3				GND
4				GND
5				GND
6				GND
7				GND
8				GND
9				GND
10				GND
11		INT4-		GND
12				GND
13				I/O 1
14				I/O 2
15			CLK01	I/O 3
16	RCBD0	RCBTD1	CLK02	I/O 4
17	PERINT6-	BUSGRI-	CLK03	I/O 5
18	PERINT7-	BUSGRO-	CLK04	I/O 6
19	BUSREQ-	PERINT2-	CLK05	I/O 7
20	RCBTD0	PERINT3-	CLK06	I/O 8
21	RCBRD1	PERINT4-	CLK07	I/O 9
22	BUSBSY-	PERINT5-	CLK08	I/O 10
23	RSTOUT-	BUSLOCK-		I/O 11
24	PERINT1-	PERINT0-		I/O 12
25	BEN1-	BEN0-		I/O 13
26	BEN3-	BEN2-		I/O 14
27	LDS-	DAS-		I/O 15
28	WRT-	UDS-		I/O 16
29	EDTACK-	DTACK-		HW4
30	PARITY+	SSR-	FRMSP	FP97-
31	PRTYEN-	MEMERR-	TOSP-	C97
32	FAS-	S/E-	CMACT	SH0
33	DAS32-	CPUCLK+	CMLINE	
34	SH1			
35	DATA 00	EDAS-	CMSYN	FP61-
36	DATA 01	ADDR 01	TYPE 1	C61
37	DATA 02	ADDR 02	HW0	-5V
38	DATA 03	ADDR 03	HW1	-5V
39	DATA 04	ADDR 04	HW2	-5V
40	DATA 05	ADDR 05	HW3	-5V
41	DATA 06	ADDR 06	TOMRES	GND
42	DATA 07	ADDR 07	FRMRES-	GND
43	DATA 08	ADDR 08	TOMHERE-	GND
44	DATA 09	ADDR 09	FRMHERE-	GND
45	DATA 10	ADDR 10	TOMWRT-	+5V
	DATA 11	ADDR 11	FRMWRT-	+5V

	D	C	B	A
46	DATA 12	ADDR 12	TOMAS-	+5V
47	DATA 13	ADDR 13	FRMAS-	+5V
48	DATA 14	ADDR 14	TOMACK-	+5V
49	DATA 15	ADDR 15	FRMACK-	+5V
50	DATA 16	ADDR 16	TOMBSDEC-	+5V
51	DATA 17	ADDR 17	FRMBSDEC-	+5V
52	DATA 18	ADDR 18	TOSPARE	+5V
53	DATA 19	ADDR 19	FRMSPARE	+5V
54	DATA 20	ADDR 20	MADDR 00	+5V
55	DATA 21	ADDR 21	MADDR 01	+5V
56	DATA 22	ADDR 22	LNKFP-	TYPE0
57	DATA 23	ADDR 23	TXFP 1	TXFP0
58	DATA 24	ADDR 24	RXFP 1	RXFP0
59	DATA 25	ADDR 25	STDB 0	STDA0
60	DATA 26	ADDR 26	STDB 1	STDA1
61	DATA 27	ADDR 27	STDB 2	STDA2
62	DATA 28	ADDR 28	STDB 3	STDA3
63	DATA 29	ADDR 29	STDB 4	STDA4
64	DATA 30	ADDR 30	STDB 5	STDA5
65	DATA 31	ADDR 31	STDB 6	STDA6
66	MDATA 07	MADDR 02	STDB 7	STDA7
67	MDATA 08	MADDR 03	STDB 8	STDA8
68	MDATA 09	MADDR 04	STDB 9	STDA9
69	MDATA 10	MADDR 05	SRDB 0	SRDA0
70	MDATA 11	MADDR 06	SRDB 1	SRDA1
71	MDATA 12	MADDR 07	SRDB 2	SRDA2
72	MDATA 13	MADDR 08	SRDB 3	SRDA3
73	MDATA 14	MADDR 09	SRDB 4	SRDA4
74	MDATA 15	MADDR 10	SRDB 5	SRDA5
75	MDATA 16	MADDR 11	SRDB 6	SRDA6
76	MDATA 17	MADDR 12	SRDB 7	SRDA7
77	MDATA 18	MADDR 13	SRDB 8	SRDA8
78	MDATA 19	MADDR 14	SRDB 9	SRDA9
79	MDATA 20	MADDR 15	I/O 17	GND
80	MDATA 21	MADDR 16	I/O 18	GND
81	MDATA 22	MADDR 17	I/O 19	GND
82	MDATA 23	MADDR 18	I/O 20	GND
83	MDATA 24	MADDR 19	I/O 21	GND
84	MDATA 25	MDATA 00	I/O 22	GND
85	MDATA 26	MDATA 01	I/O 23	GND
86	MDATA 27	MDATA 02	I/O 24	GND
87	MDATA 28	MDATA 03	I/O 25	GND
88	MDATA 29	MDATA 04	I/O 26	GND
89	MDATA 30	MDATA 05	I/O 27	GND
90	MDATA 31	MDATA 06	I/O 28	GND

Technical data

Power requirements

The NT9X12AB requires 5V ±5%, and 5A maximum, nominal 3.5A.

NT9X12AC

Product description

The NT9X12AC supercedes the NT9X12AB CPU port card. The NT9X12AC card adds parity and fault isolation capabilities to the transmit and receive buffers on the card.

Location

A standard configuration has four port cards for each computing module (CM). Each half of the processor has two port cards in the card slots immediately next to to each processor. The system load module (SLM) has two additional port cards.

Functional description

The primary function of the NT9X12AC is to provide a high-bandwidth communications link between the CPU and message switch. This card provides a load route from the SLM to the CM. The card supports four link protocols.

Functional blocks

The NT9X12AC has the following functional blocks:

- messaging
- split mode register (SMR)
- command and status registers
- time-of-day clock
- paddle board interface
- element identification (ID) PROM
- reset circuit
- 9X22 diagnostics
- interrupt
- parity
- bus interface

Messaging

The messaging block provides protocol conversion, buffering and flow control of incoming and outgoing messages. The messaging block interfaces with the asynchronous data bus on the bus side. The messaging block interfaces with the shorting bus (S-bus) on the link side. Parity protection is provided over the message path.

Split mode register

When the system is in split mode, the SMR modifies the destination addresses of data messages. The messages are to be written in the first-in first-out RAM (FIFO) on the inactive CPU. Only the active CPU can write to the SMR. Split mode is a mode where the two planes operate separately. The main function of the split mode is for BCS upgrades.

Command and status registers

Command and status registers monitor the board.

Time-of-day clock

The time-of-day clock is a 48-bit timer synchronized to the 125 µs transmit frame pulse. The time of day clock is a real-time clock. Applications that require an accurate timing element use the time-of-day clock as a reference.

Paddle board interface

The paddle board interface communicates the signals required for P-bus transactions to the paddle board. The paddle board interface supports the NT9X20AA and the NT9X46AA. The NT9X20AA is a DS512 interface paddle board. The NT9X46AA is a parallel port interface paddle board.

Element identification PROM

The ID PROM contains the product engineering code (PEC), release, vintage information and checksum.

Reset circuit

After a power-up or software reset, the reset circuit initializes the hardware. The reset circuit places the card in 12AB or 12AC mode.

9X22 diagnostics

The 9X22 diagnostics provides a diagnostic interface to the 9X22 clock card.

Interrupt

The interrupt function provides distribution and control of port card error interrupts level 4. The interrupt function transmits and receives message interrupts level 1.

Parity

Parity generation performs across the address and data bus during read and write transactions. The port card activates the bus parity bit. The processor verifies that the bus parity bit is valid. The parity operation on a bus transaction occurs when the port card asserts PARITY ENB. The PARITY ENB is a signal that tells the processor to verify parity on this bus transaction.

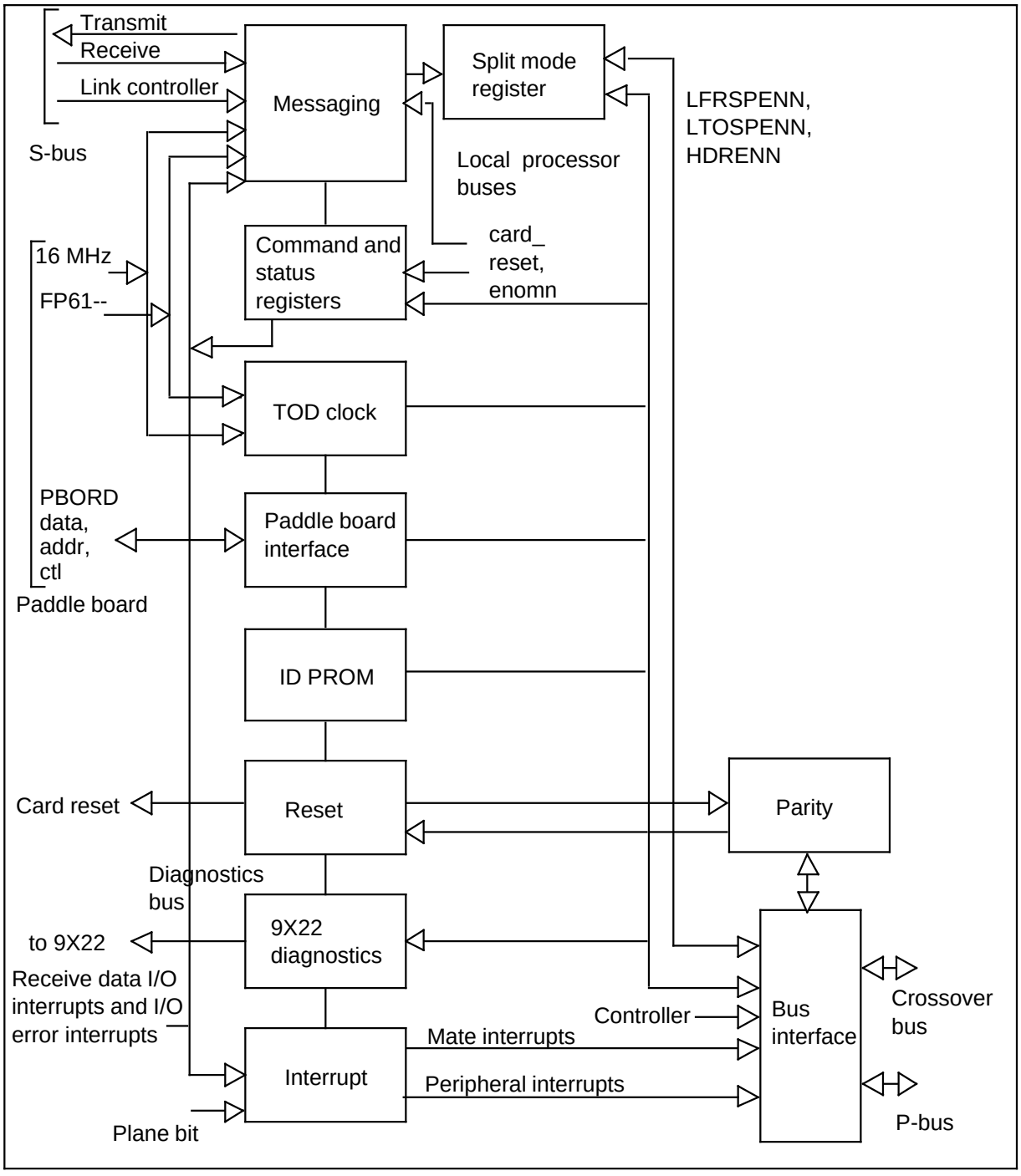
NT9X12AC (continued)

Bus interface

The bus interface provides an interface for the processor bus (P-bus), the crossover bus and the local processor buses. The bus interface provides address decoding.

The relationship between the functional blocks appears in the following figure.

NT9X12AC functional blocks



NT9X12AC (continued)

Signaling

Pin numbers

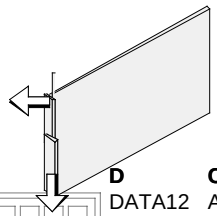
The pin numbers for the NT9X12AC appear in the following figure.

Technical data

Power requirements

The NT9X12AC requires 5V ±5% and 5A maximum. The nominal current is 4A.

NT9X12AC pin numbers



	D	C	B	A
1				GND
2				GND
3				GND
4				GND
5				GND
6				GND
7				GND
8				GND
9				GND
10				GND
11		INT4--		GND
12				GND
13				PENB--
14				PWRT--
15	PLN0--		CLK*1	PDTACK--
16			CLK*2	C244
17	PEINT6--		CLK*3	PADR0
18	PEINT7--		CLK*4	PADR1
19		PEINT2--	CLK*5	PADR2
20		PEINT3--	CLK*6	PADR3
21		PEINT4--	CLK*7	DREN--
22		PEINT5--	CLK*8	PADR4
23			TMTINT--	PADR5
24	PEINT1--	PEINT0--	FMTINT--	
25	BEN1--	BEN0--	TMRINT--	
26	BEN3--	BEN2--	FMRINT--	
27	GND		TSPLEN--	
28	WRT--	GND	FSPLEN--	
29	HDTACK	LDTACK--	ENOMN--	HW4
30	PARITY+		FRMSP--	FP97--
31	PRTYEN--		TOSP--	C97
32		GND	CMACT--	SH0
33	DAS32--			SH1
34	DATA00		CMSYNC--	FP61--
35	DATA01			C61
36	DATA02	ADDR02P	HW0	
37	DATA03	ADDR03P	HW1	
38	DATA04	ADDR04P	HW2	
39	DATA05	ADDR05P	HW3	
40	DATA06	ADDR06P	TOMRES--	GND
41	DATA07	ADDR07P	FRMRES--	GND
42	DATA08	ADDR08P	TOMPWR--	GND
43	DATA09	ADDR09P	FHERE--	GND
44	DATA10	ADDR10P	TOMWRT--	+5V
45	DATA11	ADDR11P	FRMWRT--	+5V

	D	C	B	A
46	DATA12	ADDR12P	TOMAS--	+5V
47	DATA13	ADDR13P	FRMAS--	+5V
48	DATA14	ADDR14P	TOMACK--	+5V
49	DATA15	ADDR15P	FRMACK--	+5V
50	DATA16	ADDR16P	TBSDEC--	+5V
51	DATA17	ADDR17P	FBSDEC--	+5V
52	DATA18	ADDR18P	TMIOINT	+5V
53	DATA19	ADDR19P	FMIOINT	+5V
54	DATA20	ADDR20P	MADDR00	+5V
55	DATA21	ADDR21P	MADDR01	+5V
56	DATA22	ADDR22P		
57	DATA23	ADDR23P		PLTVL
58	DATA24	ADDR24P		PLRVL
59	DATA25	ADDR25P		STDA0
60	DATA26	ADDR26P		STDA1
61	DATA27	ADDR27P		STDA2
62	DATA28	ADDR28P		STDA3
63	DATA29	ADDR29P		STDA4
64	DATA30	ADDR30P		STDA5
65	DATA31	ADDR31P		STDA6
66	MDAT07	MADDR02P		STDA7
67	MDAT08	MADDR03P		
68	MDAT09	MADDR04P		
69	MDAT10	MADDR05P	SRDA0	
70	MDAT11	MADDR06P	SRDA1	
71	MDAT12	MADDR07P	SRDA2	
72	MDAT13	MADDR08P	SRDA3	
73	MDAT14	MADDR09P	SRDA4	
74	MDAT15	MADDR10P	SRDA5	
75	MDAT16	MADDR11P	SRDA6	
76	MDAT17	MADDR12P	SRDA7	
77	MDAT18	MADDR13P		
78	MDAT19	MADDR14P		
79	MDAT20	MADDR15P	PDATA0	GND
80	MDAT21	MADDR16P	PDATA1	GND
81	MDAT22	MADDR17P	PDATA2	GND
82	MDAT23	MADDR18P	PDATA3	GND
83	MDAT24	MADDR19P	PDATA4	GND
84	MDAT25	MDAT00	PDATA5	GND
85	MDAT26	MDAT01	PDATA6	GND
86	MDAT27	MDAT02	PDATA7	GND
87	MDAT28	MDAT03	PDATA8	GND
88	MDAT29	MDAT04	PDATA9	GND
89	MDAT30	MDAT05	PDATA10	GND
90	MDAT31	MDAT06	PDATA11	GND

Legend

PADR = PADDR

NT9X12AD

Product description

The NT9X12AD replaces the NT9X12AB and NT9X12AC central processing port (CPU) port cards. The NT9X12AD adds parity and fault isolation capabilities to the transmit and receive buffers on the card.

Location

A standard configuration has four port cards for each computing module (CM). Each half of the processor has two port cards in the card slots next to each processor. The system load module (SLM) has two additional port cards.

Functional description

The primary function of the NT9X12AD is to provide a high-bandwidth communications link between the CPU and message switch. This card also provides a load route from the SLM to the CM. The card supports four link protocols.

Functional blocks

NT9X12AD includes the functional blocks that follow:

- messaging
- split mode register (SMR)
- command and status registers
- time-of-day clock
- paddle board interface
- element identification (ID) PROM
- reset circuit
- 9X22 diagnostics
- interrupt
- parity
- bus interface

Messaging

The messaging block provides protocol conversion, buffering and flow control of incoming and outgoing messages. The messaging block interfaces with the asynchronous dat bus on the bus side.. The messaging block interfaces with the shorting bus (S-bus) on the link side. Parity protection is provided over the message path.

Split mode register

When the system is in split mode, the SMR modifies the destination addresses of data messages. The messages are to be written in the first-in first-out RAM (FIFO) on the inactive CPU. Only the active CPU can write to the SMR. Split mode is a mode where two planes operate separately. The main function of the split mode is for software upgrades.

Command and status registers

Command and status registers monitor the card.

Time-of-day clock

The time-of-day clock is a 48-bit timer synchronized to the 125 µs transmit frame pulse. the time-of-day clock is a real-time clock. Applications that require an accurate timing element use the time-of-day clock as a reference.

Paddle board interface

The paddle board interface communicates the signals required for P-bus transactions to the paddle board. The paddle board interface supports NT9X20AA and the NT9X46AA. The NT9X20AA is a DS-512 interface paddle board. The NT9X46AA is a parallel port interface paddle board.

Element identification PROM

The ID PROM contains the product engineering code (PEC), release, version information, and checksum.

Reset circuit

After a power-up or software reset, the reset circuit initializes the hardware. The reset circuit places the card in 12AB or 12AC mode.

9X22 diagnostics

The 9X22 diagnostics provides a diagnostic interface to the 9X22 clock card.

Interrupt

The interrupt function provides distribution and control of port card error interrupts level 4. The interrupt function transmits and receives message interrupts level 1.

Parity

Parity generation performs across the address and data bus during read and write transactions. The port card activates the bus parity bit. The processor checks that the bus parity bit is valid. The parity operation on a bus transaction occurs when the port card maintains PARITY ENB. The PARITY ENB is a signal that tells the processor to check parity on this bus transaction.

NT9X12AD (continued)

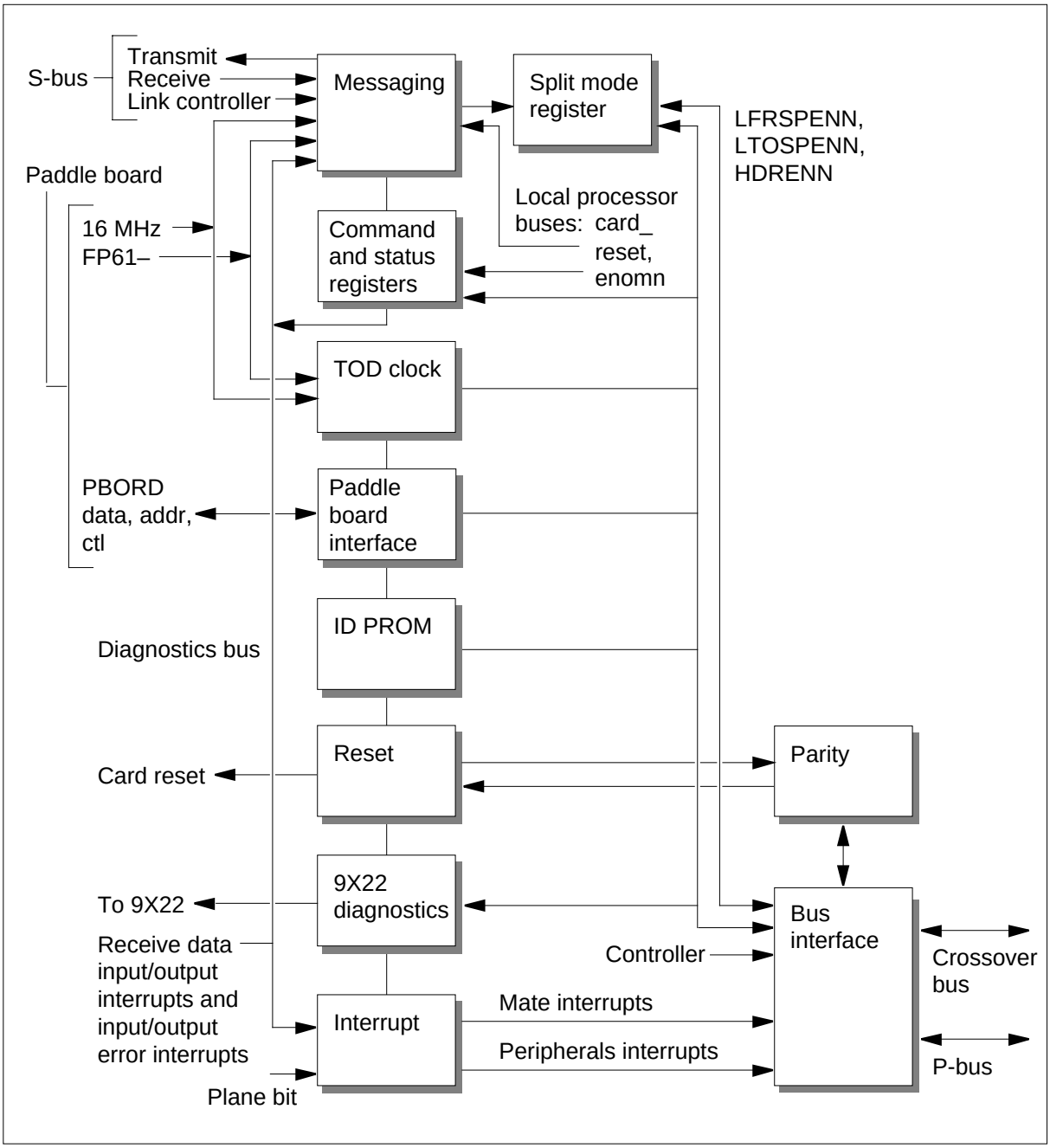
The figure that follows shows the relationship of the functional blocks.

Bus interface

The bus interface provides an interface for the processor bus (P-bus), the crossover bus, and the local processor buses. The bus interface provides address decoding.

The relationship between functional blocks appears in the figure that follows:

NT9X12AD functional blocks



NT9X12AD (continued)

Signaling

Pin outs

The table that follows shows the pin outs for NT9X12AD.

NT9X12AD pin outs (Sheet 1 of 4)

Pin	Row D	Row C	Row B	Row A
1				GND
2				GND
3				GND
4				GND
5				GND
6				GND
7				GND
8				GND
9				GND
10				GND
11		INT4-		GND
12				GND
13				PENB-
14				PWRT-
15	PLN0-		CLK*1	PDTACK-
16			CLK*2	C244
17	PEINT6-		CLK*3	PADDR0
18	PEINT7-		CLK*4	PADDR1
19		PEINT2-	CLK*5	PADDR2
20		PEINT3-	CLK*6	PADDR3
21		PEINT4-	CLK*7	DREN-
22		PEINT5-	CLK*8	PADDR4

NT9X12AD pin outs (Sheet 2 of 4)

Pin	Row D	Row C	Row B	Row A
23			TMTINT-	PADDR5
24	PEINT1	PEINT0-	FMTINT-	
25	BEN1-	BEN0-	TMRINT-	
26	BEN3-	BEN2-	FMRINT-	
27	GND		TSPLEN-	
28	WRT-	GND	FSPLEN-	
29	HDTACK	LDTACK-	ENOMN-	HW4
30	PARITY+		FRMSP-	FP97-
31	PRTYEN-		TOSP-	C97
32		GND	CMACT-	SH0
33	DAS32-			SH1
34	DATA00		CMSYNC-	FP61-
35	DATA01			C61
36	DATA02	ADDR02P	HW0	
37	DATA03	ADDR03P	HW1	
38	DATA04	ADDR04P	HW2	
39	DATA05	ADDR05P	HW3	
40	DATA06	ADDR06P	TOMRES-	GND
41	DATA07	ADDR07P	FRMRES-	GND
42	DATA08	ADDR08P	TOMPWR-	GND
43	DATA09	ADDR09P	FHERE-	GND
44	DATA10	ADDR10P	TOMWRT-	+5V
45	DATA11	ADDR11P	FRMWRT-	+5V
46	DATA12	ADDR12P	TOMAS-	+5V

NT9X12AD (continued)

NT9X12AD pin outs (Sheet 3 of 4)

Pin	Row D	Row C	Row B	Row A
47	DATA13	ADDR13P	FRMAS-	+5V
48	DATA14	ADDR14P	TOMACK-	+5V
49	DATA15	ADDR15P	FRMACK-	+5V
50	DATA16	ADDR16P	TBSDEC-	+5V
51	DATA17	ADDR17P	FBSDEC-	+5V
52	DATA18	ADDR18P	TMIOINT	+5V
53	DATA19	ADDR19P	FMIOINT	+5V
54	DATA20	ADDR20P	MADDR00	+5V
55	DATA21	ADDR21P	MADDR01	+5V
56	DATA22	ADDR22P		
57	DATA23	ADDR23P		PLTVL
58	DATA24	ADDR24P		PLRVL
59	DATA25	ADDR25P		STDA0
60	DATA26	ADDR26P		STDA1
61	DATA27	ADDR27P		STDA2
62	DATA28	ADDR28P		STDA3
63	DATA29	ADDR29P		STDA4
64	DATA30	ADDR30P		STDA5
65	DATA31	ADDR31P		STDA6
66	MDAT07	MADDR02P		STDA7
67	MDAT08	MADDR03P		
68	MDAT09	MADDR04P		
69	MDAT10	MADDR05P	SRDA0	
70	MDAT11	MADDR06P	SRDA1	

NT9X12AD pin outs (Sheet 4 of 4)

Pin	Row D	Row C	Row B	Row A
71	MDAT12	MADDR07P	SRDA2	
72	MDAT13	MADDR08P	SRDA3	
73	MDAT14	MADDR09P	SRDA4	
74	MDAT15	MADDR10P	SRDA5	
75	MDAT16	MADDR11P	SRDA6	
76	MDAT17	MADDR12P	SRDA7	
77	MDAT18	MADDR13P		
78	MDAT19	MADDR14P		
79	MDAT20	MADDR15P	PDATA0	GND
80	MDAT21	MADDR16P	PDATA1	GND
81	MDAT22	MADDR17P	PDATA2	GND
82	MDAT23	MADDR18P	PDATA3	GND
83	MDAT24	MADDR19P	PDATA4	GND
84	MDAT25	MDAT00	PDATA5	GND
85	MDAT26	MDAT01	PDATA6	GND
86	MDAT27	MDAT02	PDATA7	GND
87	MDAT28	MDAT03	PDATA8	GND
88	MDAT29	MDAT04	PDATA9	GND
89	MDAT30	MDAT05	PDATA10	GND
90	MDAT31	MDAT06	PDATA11	GND

Technical data

Power requirements

The NT9X12AD requires 5V ±5% and 5A maximum. The nominal current is 4A.

NT9X13BB

Product description

The NT9X13BB DMS SuperNode processor card is a high-performance microcomputer board based on the Motorola MC68020 32-bit microprocessor. Applications like the DMS SuperNode use the processor card.

The NT9X13BB has the following features:

- a 20 MHz MC68020 CPU
- memory access protection, write protect
- a 4 kbyte data cache
- dual-channel serial communications controller (SCC)
- socket for optional paged memory management unit (SCC)
- a 256 kbyte static RAM (SRAM) with parity
- processor bus (P-bus) compatibility
- a 128 kbytes of EPROM
- element identification (ID) PROM
- synchronous and matching modes
- timers
- interrupts
- status and control registers
- fault indication registers (FIR)

Functional description

Functional blocks

The NT9X13BB has the following functional blocks:

- MC68020 CPU
- memory controller (MEM) and memory array
- memory access unit (MAU)
- maintenance, timing, and control (MTC)
- matcher (MCH)

MC68020 CPU

The 20 MHz MC68020 CPU is the main processing machine of the . The MC68020 CUP provides significant performance enhancement over the earlier MC6800 CPUs.

Memory controller

The memory controller can correct single data errors. The memory controller can detect double or multiple errors.

Memory access unit

This functional block performs the following functions:

- controls a data cache
- provides address space access protection in 64 kbyte blocks
- starts a parity protection design on bus accesses and the data cache
- supplies the necessary control signals for P-bus specification for the extended multiprocessor system (XMS)
- supplies the necessary control signals for memory bus specification for the SuperNode CM/MEM

Maintenance, timing, and control (MTC)

The MTC interfaces with the 68020 CPU. The MTC provides the CPU with basic signals like clock, reset and chip selects to the associated EPROM and other peripherals. The MTC incorporates an interval timer and a sanity timer. The interval timer can operate in a number of modes. Interrupts from the different sources are latched, encoded and passed to the processor at a fixed priority. The MTP provides the interface to the SCC for reset terminal interface (RTIF) communications. In duplex operation, the MTC provides clock detection and selection. The MTC provides a serial FIR to obtain information about the mate system clock and control signals. This serial FIR allows the CPU that initiates the request to obtain information from an inoperative mate.

Matcher

The MCH performs the following functions:

- compares address and data on MC68020 CPU bus cycles against the address and data of the mate. This comparison detects mismatch error.
- multiplexes bus cycles address and data to the outgoing match bus to allow the mate MCH to perform the same match check.
- passes the incoming match bus from mate to the data bus when the MTC requests the start of the update mode of operation. The update mode is a computing module that updates the memory data of the mate on read cycles.
- maintains a hardware lock on the address hold register. After the MCH detects a fault, the recovery diagnostic software unlocks the register.
- provides a 32-bit maintenance control register to which the data bus can write. The mate CPU reads from the register. A signal the CPU supplies to

NT9X13BB (continued)

lace the mate communication register (MCR) on the operational measurements (OM) bus controls when the CPU reads.

Signaling

Pin numbers

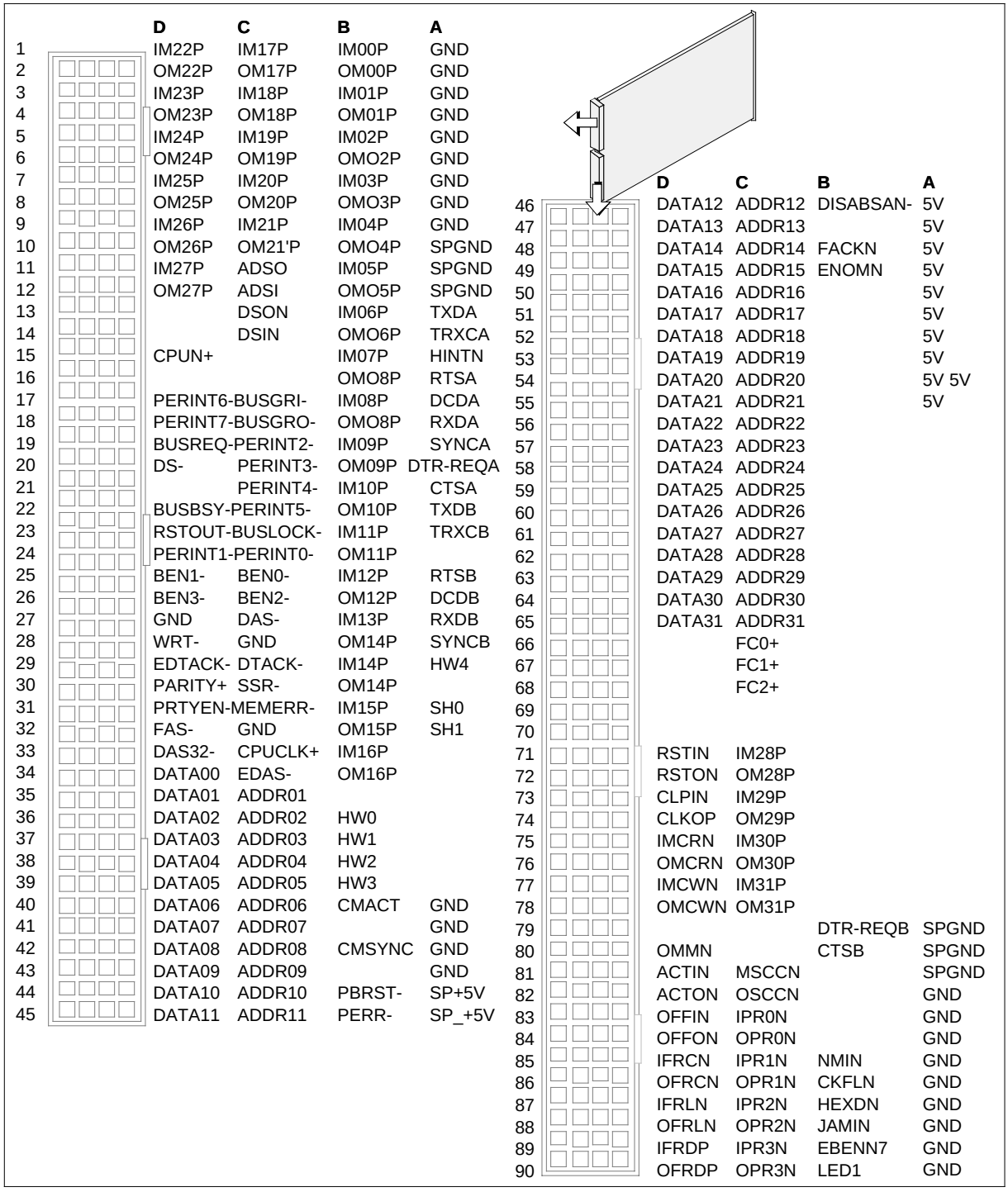
The pin numbers for NT9X13BB appear in the following figure.

Technical data

Power requirements

The NT9X13BB requires +5V ±5%.

NT9X13BB pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2	OM22P	OM17P	OM00P	GND
3	IM23P	IM18P	IM01P	GND
4	OM23P	OM18P	OM01P	GND
5	IM24P	IM19P	IM02P	GND
6	OM24P	OM19P	OMO2P	GND
7	IM25P	IM20P	IM03P	GND
8	OM25P	OM20P	OMO3P	GND
9	IM26P	IM21P	IM04P	GND
10	OM26P	OM21'P	OMO4P	SPGND
11	IM27P	ADSO	IM05P	SPGND
12	OM27P	ADSI	OMO5P	SPGND
13		DSON	IM06P	TXDA
14		DSIN	OMO6P	TRXCA
15	CPUN+		IM07P	HINTN
16			OMO8P	RTSA
17	PERINT6-	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-	OMO8P	RXDA
19	BUSREQ-	PERINT2-	IM09P	SYNCA
20	DS-	PERINT3-	OM09P	DTR-REQA
21		PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-	OM10P	TXDB
23	RSTOUT-	BUSLOCK-	IM11P	TRXCB
24	PERINT1-	PERINT0-	OM11P	
25	BEN1-	BEN0-	IM12P	RTSB
26	BEN3-	BEN2-	OM12P	DCDB
27	GND	DAS-	IM13P	RXDB
28	WRT-	GND	OM14P	SYNCB
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-	OM14P	
31	PRTYEN-	MEMERR-	IM15P	SH0
32	FAS-	GND	OM15P	SH1
33	DAS32-	CPUCLK+	IM16P	
34	DATA00	EDAS-	OM16P	
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10	PBRST-	SP+5V
45	DATA11	ADDR11	PERR-	SP_+5V

	D	C	B	A
46	DATA12	ADDR12	DISABSAN-	5V
47	DATA13	ADDR13		5V
48	DATA14	ADDR14	FACKN	5V
49	DATA15	ADDR15	ENOMN	5V
50	DATA16	ADDR16		5V
51	DATA17	ADDR17		5V
52	DATA18	ADDR18		5V
53	DATA19	ADDR19		5V
54	DATA20	ADDR20		5V 5V
55	DATA21	ADDR21		5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66		FC0+		
67		FC1+		
68		FC2+		
69				
70				
71	RSTIN	IM28P		
72	RSTON	OM28P		
73	CLPIN	IM29P		
74	CLKOP	OM29P		
75	IMCRN	IM30P		
76	OMCRN	OM30P		
77	IMCWN	IM31P		
78	OMCWN	OM31P		
79			DTR-REQB	SPGND
80	OMMN		CTSB	SPGND
81	ACTIN	MSCCN		SPGND
82	ACTON	OSCCN		GND
83	OFFIN	IPR0N		GND
84	OFFON	OPR0N		GND
85	IFRCN	IPR1N	NMIN	GND
86	OFRCN	OPR1N	CKFLN	GND
87	IFRLN	IPR2N	HEXDN	GND
88	OFRLN	OPR2N	JAMIN	GND
89	IFRDP	IPR3N	EBENN7	GND
90	OFRDP	OPR3N	LED1	GND

NT9X13BC

Product description

The NT9X13BC DMS SuperNode processor card is a high-performance microcomputer board based on the Motorola MC68020 32-bit microprocessor. The processor card is like the NT9X13BA. The processor card uses the E87 version of the 68020 instead of A70. The processor card uses the H42 version of the memory access unit. Applications like the DMS SuperNode use the .

The NT9X13BC has the following features:

- a 20 MHz MC68020 CPU
- memory access protection, write protect
- a 4 kbyte data cache
- dual-channel serial communications controller (SCC)
- socket for optional paged memory management unit (PMMU)
- a 256 kbyte static RAM (SRAM) with parity
- processor bus (P-bus) compatibility
- one hundred and twenty eight (128) kbyte of EPROM
- element identification (ID) PROM
- synchronous and matching modes
- timers
- interrupts
- status and control registers
- fault indication registers (FIR)

Functional description

Functional blocks

NT9X13BC has the following functional blocks:

- MC68020 CPU
- memory access unit (MAU)
- memory controller (MEM) and memory array
- maintenance, timing and control (MTC)
- matcher (MCH)

MC68020 CPU

The 20 MHz MC68020 CPU is the main processing machine of the NT9X13BC. The CPU provides improved performance over the earlier MC6800 CPUs.

Memory access unit

This functional block performs the following functions:

- controls a data cache
- provides address space access protection in 64 kbyte blocks
- starts a parity protection design on bus accesses and the data cache
- supplies the necessary control signals for the extended multiprocessor system (XMS) P-bus specification
- supplies the necessary control signals for the SuperNode CM/MEM memory bus specification

Memory controller

The MEM can correct any single data errors and detect any double or multiple errors.

Maintenance, timing, and control

The MTC interfaces with the 68020 CPU. The MTC provides the CPU with basic signals like clock, reset and chip selects to the associated EPROM and other peripherals. The MTC incorporates an interval timer and a sanity timer. The interval timer can operate in a number of modes. Interrupts from the different sources are latched, encoded and passed to the processor at a correct priority. The MTP provides the interface to the SCC for remote terminal interface (RTIF) communications. In duplex operation, the MTC provides clock detection and selection. The MTC provides a serial FIR to obtain information about the mate system clock and control signals. The serial FIR allows the CPU that initiates the request to get information from an inoperative mate.

Matcher

The MCH performs the following functions:

- compares address and data on MC68020 CPU bus cycles against the address and data of the mate CPU. This action detects mismatch error.
- multiplexes bus cycles address and data to the outgoing match bus to allow the mate MCH to perform the same match check.
- passes the incoming match bus from mate to the data bus the MTC requests to start the update mode of operation. A computing module updates the memory data of the mate CPU on read cycles.

NT9X13BC (continued)

- maintains a hardware lock on the address hold register. After the MCH detects a fault, recovery diagnostic software unlocks the register.
- provides a 32-bit maintenance control register to which the data bus can write. The mate CPU can read from the register. A signal that the CPU supplies to lace the mate communication register (MCR) on the operational measurements (OM) bus controls when the CPU reads.

Signaling

Pin numbers

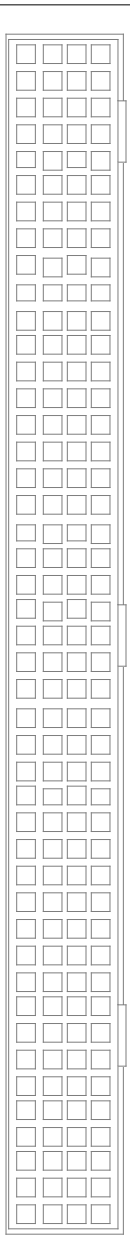
The pin numbers for NT9X13BC appear in the following figure.

Technical data

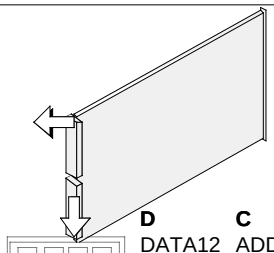
Power requirements

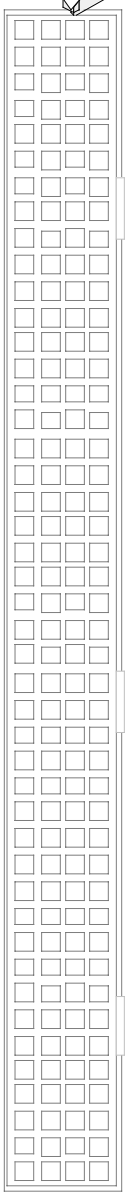
The NT9X13BC requires +5V, ±5%.

NT9X13BC pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2	OM22P	OM17P	OM00P	GND
3	IM23P	IM18P	IM01P	GND
4	OM23P	OM18P	OM01P	GND
5	IM24P	IM19P	IM02P	GND
6	OM24P	OM19P	OMO2P	GND
7	IM25P	IM20P	IM03P	GND
8	OM25P	OM20P	OMO3P	GND
9	IM26P	IM21P	IM04P	GND
10	OM26P	OM21'P	OMO4P	SPGND
11	IM27P	ADSO	IM05P	SPGND
12	OM27P	ADSI	OMO5P	SPGND
13		DSON	IM06P	TXDA
14		DSIN	OMO6P	TRXCA
15	CPUN+		IM07P	HINTN
16		GND	OMO8P	RTSA
17	PERINT6-	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-	OMO8P	RXDA
19	BUSREQ-	PERINT2-	IM09P	SYNCA
20	DS-	PERINT3-	OM09P	DTR-REQA
21		PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-	OM10P	TXDB
23	RSTOUT-	BUSLOCK-	IM11P	TRXCB
24	PERINT1-	PERINT0-	OM11P	
25	BEN1-	BEN0-	IM12P	RTSB
26	BEN3-	BEN2-	OM12P	DCDB
27	GND	DAS-	IM13P	RXDB
28	WRT-	GND	OM14P	SYNCB
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-	OM14P	
31	PRTYEN-	MEMERR-	IM15P	SH0
32	FAS-	GND	OM15P	SH1
33	DAS32-	CPUCLK+	IM16P	
34	DATA00	EDAS-	OM16P	
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10	PBRST-	SP+5V
45	DATA11	ADDR11	PERR-	SP_+5V





	D	C	B	A
46	DATA12	ADDR12	DISABSAN-	5V
47	DATA13	ADDR13	GND	5V
48	DATA14	ADDR14	FACKN	5V
49	DATA15	ADDR15	ENOMN	5V
50	DATA16	ADDR16		5V
51	DATA17	ADDR17		5V
52	DATA18	ADDR18		5V
53	DATA19	ADDR19		5V
54	DATA20	ADDR20		5V
55	DATA21	ADDR21	GND	5V
56	DATA22	ADDR22	GND	
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27	GND	GND
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		GND
66		FC0+		GND
67		FC1+		
68		FC2+		
69				
70				GND
71	RSTIN	IM28P		GND
72	RSTON	OM28P		
73	CLPIN	IM29P		
74	CLKOP	OM29P		
75	IMCRN	IM30P		GND
76	OMCRN	OM30P		
77	IMCWN	IM31P		
78	OMCWN	OM31P		
79			DTR-REQB	SPGND
80	OMMN		CTSB	SPGND
81	ACTIN	MSCCN		SPGND
82	ACTON	OSCCN		GND
83	OFFIN	IPR0N		GND
84	OFFON	OPR0N		GND
85	IFRCN	IPR1N	NMIN	GND
86	OFRCN	OPR1N	CKFLN	GND
87	IFRLN	IPR2N	HEXDN	GND
88	OFRLN	OPR2N	JAMIN	GND
89	IFRDP	IPR3N	EBENN7	GND
90	OFRDP	OPR3N	LED1	GND

NT9X13CA

Description

The NT9X13CA CPU circuit card is a high-performance microcomputer board based on the Motorola MC68020 32-bit microprocessor. The main application of the microcomputer board is in signaling transfer point (STP) and enhanced network (ENET). The microcomputer board has potential for other applications based on SuperNode hardware.

Compatibility

The NT9X13CA is like the 32-bit environment of the extended multiprocessor system (XMS) processor bus (P-bus) specification for asynchronous operations. The NT9X13CA is like the SuperNode CM/MEM bus specification for high-speed synchronous memory operations.

Functional description

Feature list

The NT9X13CA uses a Motorola 20 MHz MC68020 CPU as the main processing machine of the NT9X13CA.

The memory access unit (MAU) on the NT9X13CA provides the following types of memory access protection:

- write protect
- user write protect
- execute only (program store read access) memory access protection
- non-executable (data access only) memory access protection
- read protect

The NT9X13CA provides 4 Mbytes of on-board dynamic RAM (DRAM) with error-correction code (ECC). The ECC provides error detection of multiple bit errors. The ECC provides error correction of single bit errors.

The 128 kbytes of EPROM provide firmware for boot and initialization of the NT9X13CA.

The NT9X13CA contains element identification PROMs. These PROMs contain product engineering code (PEC) and vintage information to start system configuration.

An on-board two-channel serial communications controller (SCC) provides baud-rate programmable asynchronous or synchronous modes of operation. This procedure allows interface to character-oriented peripherals and synchronous data link control (SDLC). A terminal is an example of a

character-oriented peripheral. This procedure allows SDLC loop mode and high-level data link control (HDLC) communications controllers.

Several timer facilities are available. The timer facilities provide an operating system scheduler, bus response time-out and sanity timer functions.

Several hardware and software controlled interrupt facilities are available. These facilities provide debugging,hardware error detection, timer interval and peripheral communication.

Functional blocks

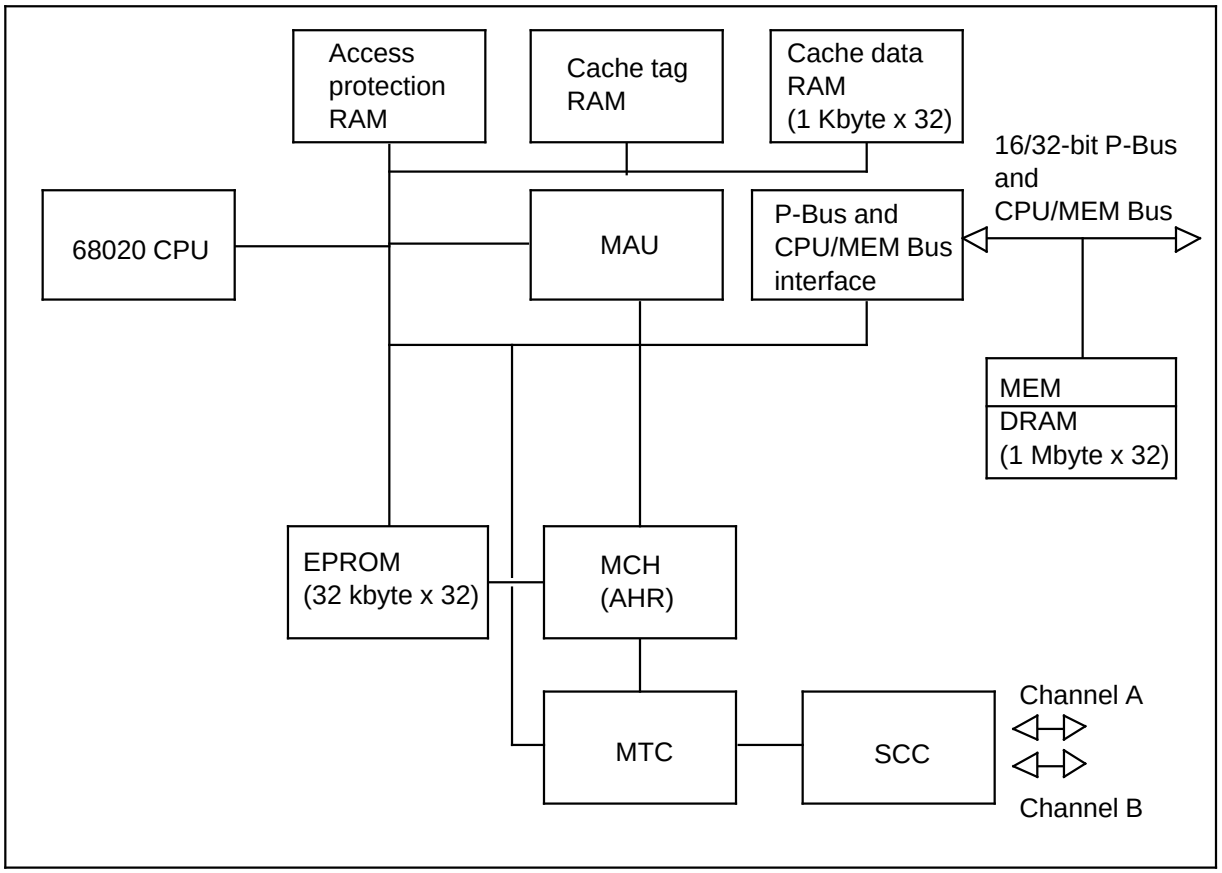
The NT9X13CA contains the following functional blocks:

- MC68020 CPU
- memory controller (MEM) and memory array
- maintenance, timing, and control (MTC)
- matcher (MCH)
- Zilog Z8530 SCC
- memory access unit (MAU)

The relationship between the functional blocks appears in the following figure.

NT9X13CA (continued)

NT9X13CA functional blocks



MC68020 central processing unit

The MC68020 CPU is a microprocessor that runs at 20MHz. The microprocessor contains a high-speed 4 kbyte data cache for access to often used data. The data cache is direct mapped and was in use in the past. The cache does not predict. The cache is not block oriented.

Memory controller

The memory controller is the heart of the memory module. The memory controller operates in a 32-bit environment to correct any single data errors. The memory controller detects double or multiple errors.

Maintenance, timing, and control

The MTC is a collection of functions that normally relate to maintenance. The MTC interfaces with the 68020 CPU. The MTC provides the basic signals like clock, reset and chip selects to the associated EPROM and other peripherals. The MTC includes an interval timer. The internal timer can operate in a number of modes, like the operating system clock. A sanity timer monitors the

running software. Interrupts from the different sources are latched, encoded and passed to the processor at a correct priority. The 68020 CPU can read, write and clear the maintenance circuits latch system fault conditions. The MTC provides the interface to the SCC for reset terminal interface (RTIF) communications.

Matcher

On the NT9X13CA, the MCH provides an address hold register function during error conditions. When the MCH detects an error, the MCH freezes the address of the last cycle. The cycle began before the error in a register. The errors are memory ECC, bus parity, or mismatch. This register is the address hold register (AHR). The AHR retains the address of the mismatched bus cycle until the MTC releases the hold signal.

Zilog Z8530 serial communications controller

The Zilog Z8530 is a non-multiplexed bus serial communications controller (SCC). The Zilog has the following capabilities:

- two separate full-duplex channels
- separate programmable baud-rate generators in each channel for synchronous/iso-synchronous data rates
- asynchronous capabilities
- 5, 6, 7, or 8 bits for each character
- 1, 1.5, or 2 stop bits
- odd or even parity
- X1, X16, X32, or X64 clock modes
- break generation and detection
- parity, overrun and framing error detection
- byte-oriented synchronous capabilities
- SDLC/HDLC capabilities
- digital phase-locked loop (DPLL) for clock recovery
- crystal oscillator

Memory access unit

The MAU is one set of four gate arrays for the SuperNode processor card. The MAU controls a data cache. The MAU provides address space access protection in 64 kbyte blocks. The MAU starts a parity protection design on bus access and the data cache. The MAU supplies the necessary control signals

NT9X13CA (continued)

for the XMS P-bus specification and the SuperNode CM/MEM memory bus specification.

Signaling

Pin numbers

The pin numbers for the NT9X13CA appear in the following figure.

Technical data

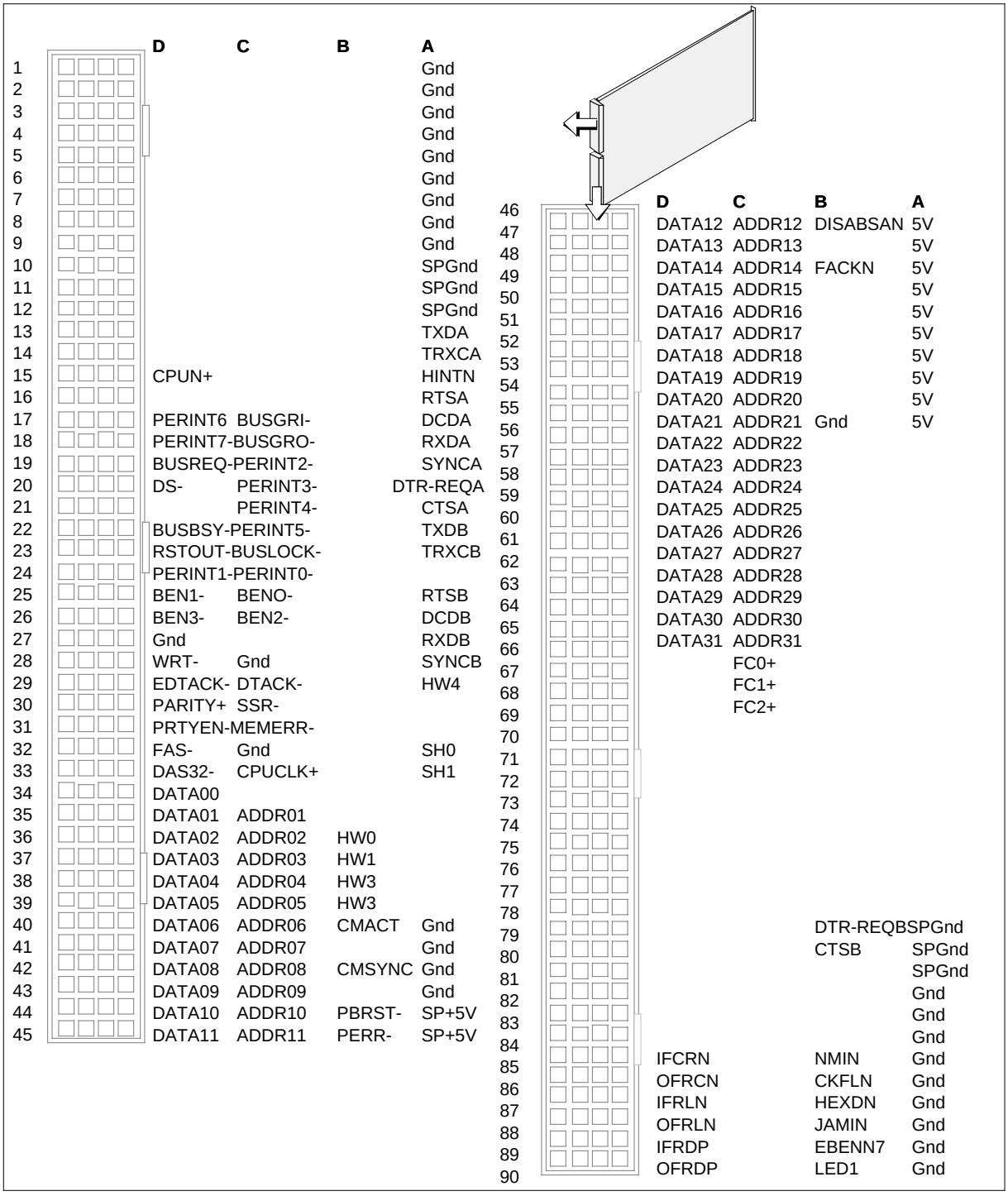
Power requirements

The power requirements for the appear in the following table.

NT9X13CA power requirement

Voltage	Current Normal	Maximum
+5 V	6.8 A	10.0 A

NT9X13CA pin numbers



	D	C	B	A
1				Gnd
2				Gnd
3				Gnd
4				Gnd
5				Gnd
6				Gnd
7				Gnd
8				Gnd
9				Gnd
10				SPGnd
11				SPGnd
12				SPGnd
13				TXDA
14				TRXCA
15	CPUN+			HINTN
16				RTSA
17	PERINT6	BUSGRI-		DCDA
18	PERINT7-	BUSGRO-		RXDA
19	BUSREQ-	PERINT2-		SYNCA
20	DS-	PERINT3-		DTR-REQA
21		PERINT4-		CTSA
22	BUSBSY-	PERINT5-		TXDB
23	RSTOUT-	BUSLOCK-		TRXCB
24	PERINT1-	PERINT0-		
25	BEN1-	BENO-		RTSB
26	BEN3-	BEN2-		DCDB
27	Gnd			RXDB
28	WRT-	Gnd		SYNCB
29	EDTACK-	DTACK-		HW4
30	PARITY+	SSR-		
31	PRTYEN-	MEMERR-		
32	FAS-	Gnd		SH0
33	DAS32-	CPUCLK+		SH1
34	DATA00			
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW3	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	Gnd
41	DATA07	ADDR07		Gnd
42	DATA08	ADDR08	CMSYNC	Gnd
43	DATA09	ADDR09		Gnd
44	DATA10	ADDR10	PBRST-	SP+5V
45	DATA11	ADDR11	PERR-	SP+5V

	D	C	B	A
46	DATA12	ADDR12	DISABSAN	5V
47	DATA13	ADDR13		5V
48	DATA14	ADDR14	FACKN	5V
49	DATA15	ADDR15		5V
50	DATA16	ADDR16		5V
51	DATA17	ADDR17		5V
52	DATA18	ADDR18		5V
53	DATA19	ADDR19		5V
54	DATA20	ADDR20		5V
55	DATA21	ADDR21	Gnd	5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66		FC0+		
67		FC1+		
68		FC2+		
69				
70				
71				
72				
73				
74				
75				
76				
77				
78				
79			DTR-REQB	SPGnd
80			CTSB	SPGnd
81				SPGnd
82				Gnd
83				Gnd
84				Gnd
85	IFCRN		NMIN	Gnd
86	OFRCN		CKFLN	Gnd
87	IFRLN		HEXDN	Gnd
88	OFRLN		JAMIN	Gnd
89	IFRDP		EBENN7	Gnd
90	OFRDP		LED1	Gnd

NT9X13DA

Product description

The NT9X13DA CPU 20 MHz card is a high-performance microcomputer board based on the Motorola MC68020 32-bit microprocessor. The microprocessor board provides general purpose applications and special purpose applications like the DMS SuperNode. The first application of the microprocessor is in the message switch of the DMS SuperNode.

The NT9X13DA has the following features:

- 20 MHz MC68020 CPU
- memory access protection, write protect
- 4 kbyte data cache
- dual-channel serial communications controller (SCC)
- socket for optional paged memory management unit (PMMU)
- 1 Mbyte dynamic RAM (DRAM) with error-correction code (ECC)
- processor bus (P-bus) compatibility
- 128 kbyte of EPROM
- element identification (ID) PROM
- synchronous and matching modes
- timers
- interrupts
- status and control registers
- fault indication registers (FIR)

This card is not available any longer. The NT9X13DB replaces the NT9X13DA. The NT9X13DB provides a bus access parity protection design not available on the .

Functional description

Functional blocks

The NT9X13DA contains the following functional blocks:

- MC68020 CPU
- memory access unit (MAU)
- memory controller (MEM) and memory array

- maintenance, timing, and control (MTC)
- matcher (MCH)

MC68020 CPU

The 20 MHz MC68020 CPU is the main processing engine of the NT9X13DA.

Memory access unit

This functional block controls a data cache and provides address space access protection in 64 kbyte blocks. This functional block supplies the necessary control signals for the extended multiprocessor system (XMS) P-bus specification. The signals are also for the SuperNode CM/MEM memory bus specification.

Memory controller

The memory controller can correct any single data errors and detect double or multiple errors.

Maintenance, timing, and control

The MTC interfaces with the MC68020 CPU. The MTC provides the CPU with basic signals. The basic signals the MTC provides include clock, reset, and chip selects to the associated EPROM and other peripherals. The MTC provides interval timer for a number of modes, and a sanity timer. Interrupts from the different sources are latched, encoded, and passed to the processor at a valid priority. The MTP provides the interface to the SCC for reset terminal interface (RTIF) communications. In duplex operation, the MTC provides clock detection and selection. The MTC also provides a serial FIR to obtain information about the mate system clock and control signals. The serial FIR allows the CPU that requests to get information from a mate that is not operational.

Matcher

The MCH performs the following functions:

- compares address and data on MC68020 CPU bus cycles. Compares the address and data against the address and data of the mate of the CPU to detect mismatch errors.
- multiplexes address and data of bus cycles to the outgoing match bus. This multiplex allows the mate MCH to perform the same match check.
- passes the incoming match bus from the mate to the data bus. Passes the match bus when the MT requests the start of the update mode of operation. A computing module updates the memory data of the mate of the computing module on read cycles.

NT9X13DA (continued)

- maintains a hardware lock on the address hold register and unlocks by recovery-diagnostic software after fault detection.
- provides a 32-bit maintenance control register. The data bus writes to the register. The mate CPU can read from the register under control of a signal the CPU supplies. The CPU supplies the signal to lace the mate communication register (MCR) on the operational measurements (OM) bus.

Signaling

Pin numbers

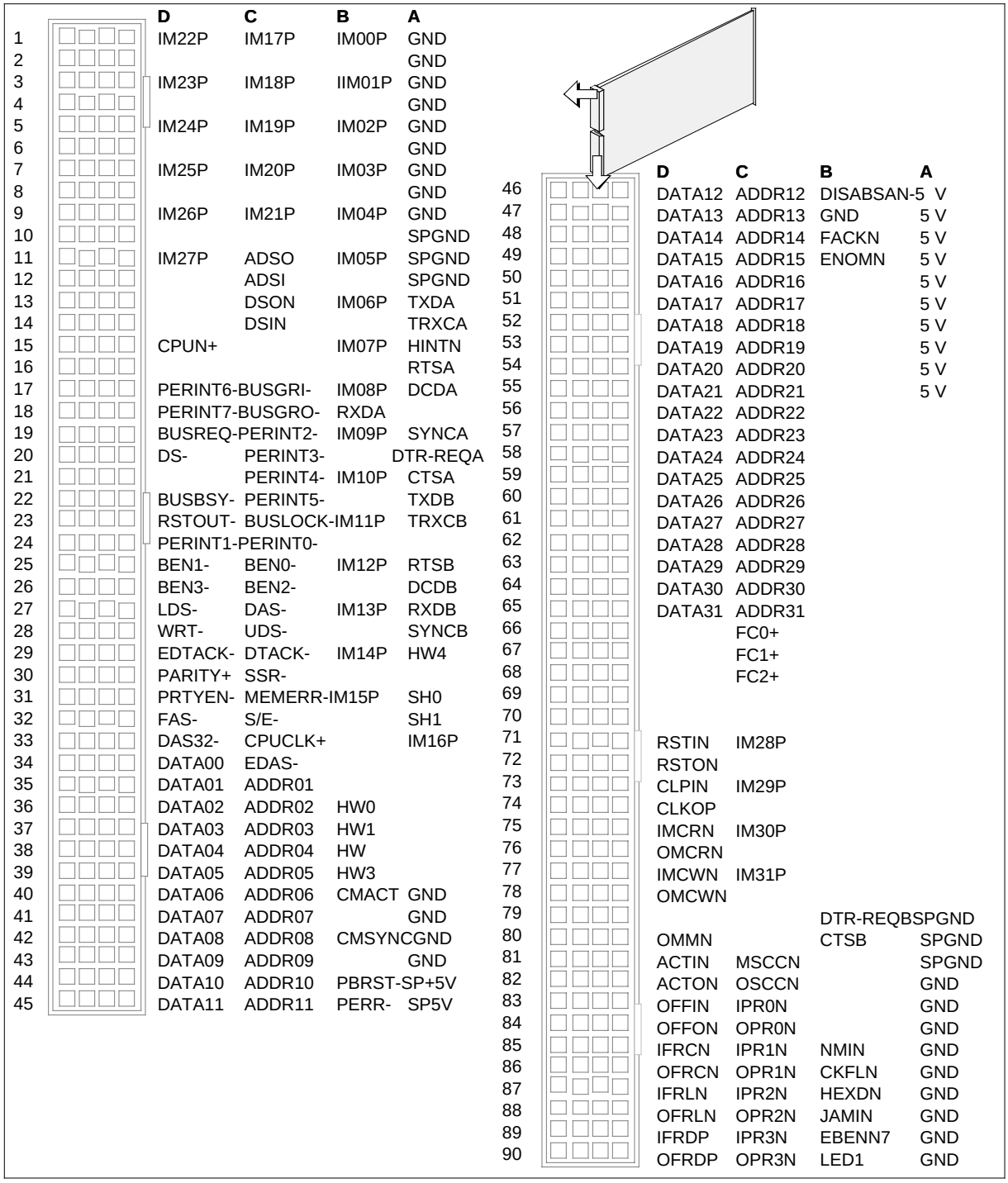
The pin numbers for NT9X13DA appear in the following figure.

Technical data

Power requirements

The NT9X13DA requires +5V ±5%.

NT9X13DA pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2				GND
3	IM23P	IM18P	IIM01P	GND
4				GND
5	IM24P	IM19P	IM02P	GND
6				GND
7	IM25P	IM20P	IM03P	GND
8				GND
9	IM26P	IM21P	IM04P	GND
10				SPGND
11	IM27P	ADSO	IM05P	SPGND
12		ADSI		SPGND
13		DSON	IM06P	TXDA
14		DSIN		TRXCA
15	CPUN+		IM07P	HINTN
16				RTSA
17	PERINT6-	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-	RXDA	
19	BUSREQ-	PERINT2-	IM09P	SYNCA
20	DS-	PERINT3-		DTR-REQA
21		PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-		TXDB
23	RSTOUT-	BUSLOCK-	IM11P	TRXCB
24	PERINT1-	PERINT0-		
25	BEN1-	BEN0-	IM12P	RTSB
26	BEN3-	BEN2-		DCDB
27	LDS-	DAS-	IM13P	RXDB
28	WRT-	UDS-		SYNCB
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-		
31	PRTYEN-	MEMERR-	IM15P	SH0
32	FAS-	S/E-		SH1
33	DAS32-	CPUCLK+		IM16P
34	DATA00	EDAS-		
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10	PBRST-	SP+5V
45	DATA11	ADDR11	PERR-	SP5V

	D	C	B	A
46	DATA12	ADDR12	DISABSAN-	5 V
47	DATA13	ADDR13	GND	5 V
48	DATA14	ADDR14	FACKN	5 V
49	DATA15	ADDR15	ENOMN	5 V
50	DATA16	ADDR16		5 V
51	DATA17	ADDR17		5 V
52	DATA18	ADDR18		5 V
53	DATA19	ADDR19		5 V
54	DATA20	ADDR20		5 V
55	DATA21	ADDR21		5 V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66		FC0+		
67		FC1+		
68		FC2+		
69				
70				
71	RSTIN	IM28P		
72	RSTON			
73	CLPIN	IM29P		
74	CLKOP			
75	IMCRN	IM30P		
76	OMCRN			
77	IMCWN	IM31P		
78	OMCWN			
79			DTR-REQB	SPGND
80	OMMN		CTSB	SPGND
81	ACTIN	MSCCN		SPGND
82	ACTON	OSCCN		GND
83	OFFIN	IPR0N		GND
84	OFFON	OPR0N		GND
85	IFRCN	IPR1N	NMIN	GND
86	OFRCN	OPR1N	CKFLN	GND
87	IFRLN	IPR2N	HEXDN	GND
88	OFRLN	OPR2N	JAMIN	GND
89	IFRDP	IPR3N	EBENN7	GND
90	OFRDP	OPR3N	LED1	GND

NT9X13DB

Product description

The NT9X13DB CPU 20 MHz card is a high-performance microcomputer board based on the Motorola MC68020 32-bit microprocessor. The microprocessor provides general purpose applications and special purpose applications like the DMS SuperNode. The initial application of the microprocessor is in the message switch of the DMS SuperNode.

The NT9X13DB has the following features:

- 20 MHz MC68020 CPU
- memory access protection, write protect
- 4 kbyte data cache
- dual-channel serial communications controller (SCC)
- socket for optional paged memory management unit (PMMU)
- 1 Mbyte dynamic RAM (DRAM) with error-correction code (ECC)
- processor bus (P-bus) compatibility
- 128 kbyte of EPROM
- element identification (ID) PROM
- synchronous and matching modes
- timers
- interrupts
- status and control registers
- fault indication registers (FIR)

Functional description

Functional blocks

The NT9X13DB consists of the following functional blocks:

- MC68020 CPU
- memory access unit (MAU)
- memory controller (MEM) and memory array
- maintenance, timing, and control (MTC)
- matcher (MCH)

MC68020 CPU

The 20 MHz MC68020 CPU is the main processing engine of the NT9X13DB. The CPU provides improved performance over the earlier MC6800 CPUs.

Memory access unit

This functional block controls a data cache, provides address space access protection in 64 kbyte blocks. The block starts a parity protection scheme on bus accesses and the data cache. The block supplies the control signals for the extended multiprocessor system (XMS) P-bus specification and the SuperNode CM/MEM memory bus specification.

Memory controller

The memory controller can correct any single data errors and detect any double or multiple errors.

Maintenance, timing, and control

The MTC interfaces with the 68020 CPU. The MTC provides the CPU with basic signals like clock, reset, and chip selects to the associated EPROM and other peripherals. The MTC includes an interval timer that can be in a number of modes, and a sanity timer. Interrupts from the different sources are latched, encoded, and passed to the processor at a valid priority. The MTP provides the interface to the SCC for reset terminal interface (RTIF) communications. In duplex operation, the MTC provides clock detection and selection. The MTC provides a serial FIR to obtain information about the mate system clock and control signals. The serial FIR allows the CPU that requests to get information from an mate that is not operational.

Matcher

The MCH performs the following functions:

- compares address and data on MC68020 CPU bus cycles. Compares the address and data against the address and data of the mate of the CPU. This procedure provides mismatch error detection.
- multiplexes bus cycles address and data to the outgoing match bus. This multiplex allows the mate MCH to perform the same match check.
- passes the incoming match bus from mate to the data bus. Passes the match bus when the MTC requests the start of the update mode of operation. A computing module updates the mate of the CM memory data on read cycles.
- maintains a hardware lock on the address hold register and unlocks by recovery/diagnostic software after fault detection
- provides a 32-bit maintenance control register. The data bus writes to the register. The mate CPU can read from the register under control of a signal

NT9X13DB (continued)

the CPU. The CPU supplies the signal to lace the mate communication register (MCR) on the operational measurements (OM) bus.

Signaling

Pin numbers

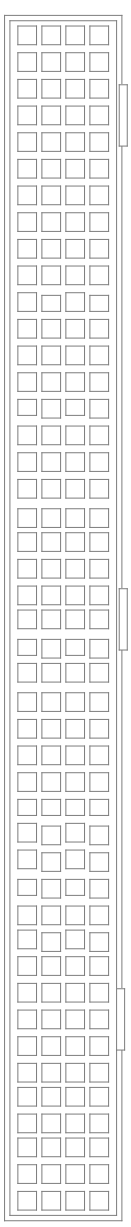
The pin numbers for NT9X13DB appears in the following figure.

Technical data

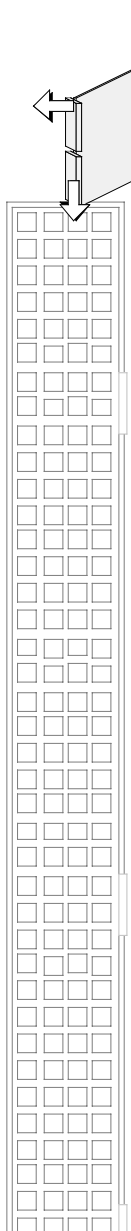
Power requirements

The NT9X13DB requires +5V, ±5%.

NT9X13DB pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2				GND
3	IM23P	IM18P	IIM01P	GND
4				GND
5	IM24P	IM19P	IM02P	GND
6				GND
7	IM25P	IM20P	IM03P	GND
8				GND
9	IM26P	IM21P	IM04P	GND
10				SPGND
11	IM27P	ADSO	IM05P	SPGND
12		ADSI		SPGND
13		DSON	IM06P	TXDA
14		DSIN		TRXCA
15	CPUN+		IM07P	HINTN
16				RTSA
17	PERINT6-	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-		RXDA
19	BUSREQ-	PERINT2-	IM09P	SYNCA
20	DS-	PERINT3-		DTR-REQA
21		PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-		TXDB
23	RSTOUT-	BUSLOCK-	IM11P	TRXCB
24	PERINT1-	PERINT0-		
25	BEN1-	BEN0-	IM12P	RTSB
26	BEN3-	BEN2-		DCDB
27	LDS-	DAS-	IM13P	RXDB
28	WRT-	UDS-		SYNCB
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-		
31	PRTYEN-	MEMERR-	IM15P	SH0
32	FAS-	S/E-		SH1
33	DAS32-	CPUCLK+		IM16P
34	DATA00	EDAS-		
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10	PBRST-	SP+5V
45	DATA11	ADDR11	PERR-	SP_+5V



	D	C	B	A
46	DATA12	ADDR12	DISABSAN-	5V
47	DATA13	ADDR13	GND	5V
48	DATA14	ADDR14	FACKN	5V
49	DATA15	ADDR15	ENOMN	5V
50	DATA16	ADDR16		5V
51	DATA17	ADDR17		5V
52	DATA18	ADDR18		5V
53	DATA19	ADDR19		5V
54	DATA20	ADDR20		5V
55	DATA21	ADDR21		5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66		FC0+		
67		FC1+		
68		FC2+		
69				
70				
71	RSTIN	IM28P		
72	RSTON			
73	CLPIN	IM29P		
74	CLKOP			
75	IMCRN	IM30P		
76	OMCRN			
77	IMCWN	IM31P		
78	OMCWN			
79			DTR-REQB	SPGND
80	OMMN		CTSB	SPGND
81	ACTIN	MSCCN		SPGND
82	ACTON	OSCCN		GND
83	OFFIN	IPR0N		GND
84	OFFON	OPR0N		GND
85	IFRCN	IPR1N	NMIN	GND
86	OFRCN	OPR1N	CKFLN	GND
87	IFRLN	IPR2N	HEXDN	GND
88	OFRLN	OPR2N	JAMIN	GND
89	IFRDP	IPR3N	EBENN7	GND
90	OFRDP	OPR3N	LED1	GND

NT9X13DC

Product description

The NT9X13DC DMS SuperNode processor card is a high-performance microcomputer board based on the Motorola MC68020 32-bit microprocessor. The microcomputer board is for general purpose applications and special purpose applications like the DMS SuperNode. The card uses all 4 Mbytes of available memory.

The NT9X13DC has the following features:

- 20 MHz MC68020 CPU
- memory access protection, write protect
- 4 kbyte data cache
- dual-channel serial communications controller (SCC)
- 4 Mbyte dynamic RAM (DRAM) with error correction code (ECC)
- processor bus (P-bus) compatibility
- 128 kbyte of EPROM
- element identification (ID) PROM
- timers
- interrupts
- status and control registers
- fault indication registers (FIR)

Functional description

Functional blocks

The NT9X13DC consists of the following functional blocks:

- MC68020 CPU
- memory access unit (MAU)
- memory controller (MEM) and memory array
- maintenance, timing, and control (MTC)
- matcher (MCH)

MC68020 CPU

The 20 MHz MC68020 CPU is the main processing engine of the NT9X13DC. The CPU provides improved performance over the earlier MC6800 CPUs.

Memory access unit

This functional block controls a data cache and provides address space access protection in 64 kbyte blocks. The block starts a parity protection scheme on bus accesses and the data cache. The block supplies the necessary control signals for the extended multiprocessor system (XMS) P-bus specification and the SuperNode CM/MEM memory bus specification.

Memory controller

The memory controller can correct any single data errors and detect double or multiple errors.

Maintenance, timing, and control

The MTC interfaces with the MC68020 CPU. The MTC provides the CPU with basic signals like clock, reset, and chip selects to the associated EPROM and other peripherals. The MTC includes an interval timer that can be used in a number of modes, and a sanity timer. Interrupts from the different sources are latched, encoded, and passed to the processor at a valid priority. The MTP provides the interface to the SCC for reset terminal interface (RTIF) communications. In duplex operation, the MTC provides clock detection and selection. The MTC also provides a serial FIR to obtain information about the mate system clock and control signals. The serial FIR allows the CPU that requests to get information from a mate that is not operational.

Matcher

The MCH performs the following functions:

- compares address and data on MC68020 CPU bus cycles. Compares the address and data against the address and data of the mate of the CPU to detect mismatch errors.
- multiplexes bus cycles address and data to the outgoing match bus. The multiplex allows the mate MCH to perform the same match check.
- passes the incoming match bus from the mate to the data bus when. Passes the match bus the MT requests at the start of the update mode of operation. A computing module updates the memory data of the mate of the computing module on read cycles.
- maintains a hardware lock on the address hold register and unlocks by recovery diagnostic software after fault detection
- provides a 32-bit maintenance control register. The data bus can write to the register. The mate CPU can read from the register under control of a signal the CPU supplies. The CPU supplies the signal to lace the mate communication register (MCR) on the operational measurements (OM) bus.

NT9X13DC (continued)

Signaling

Pin numbers

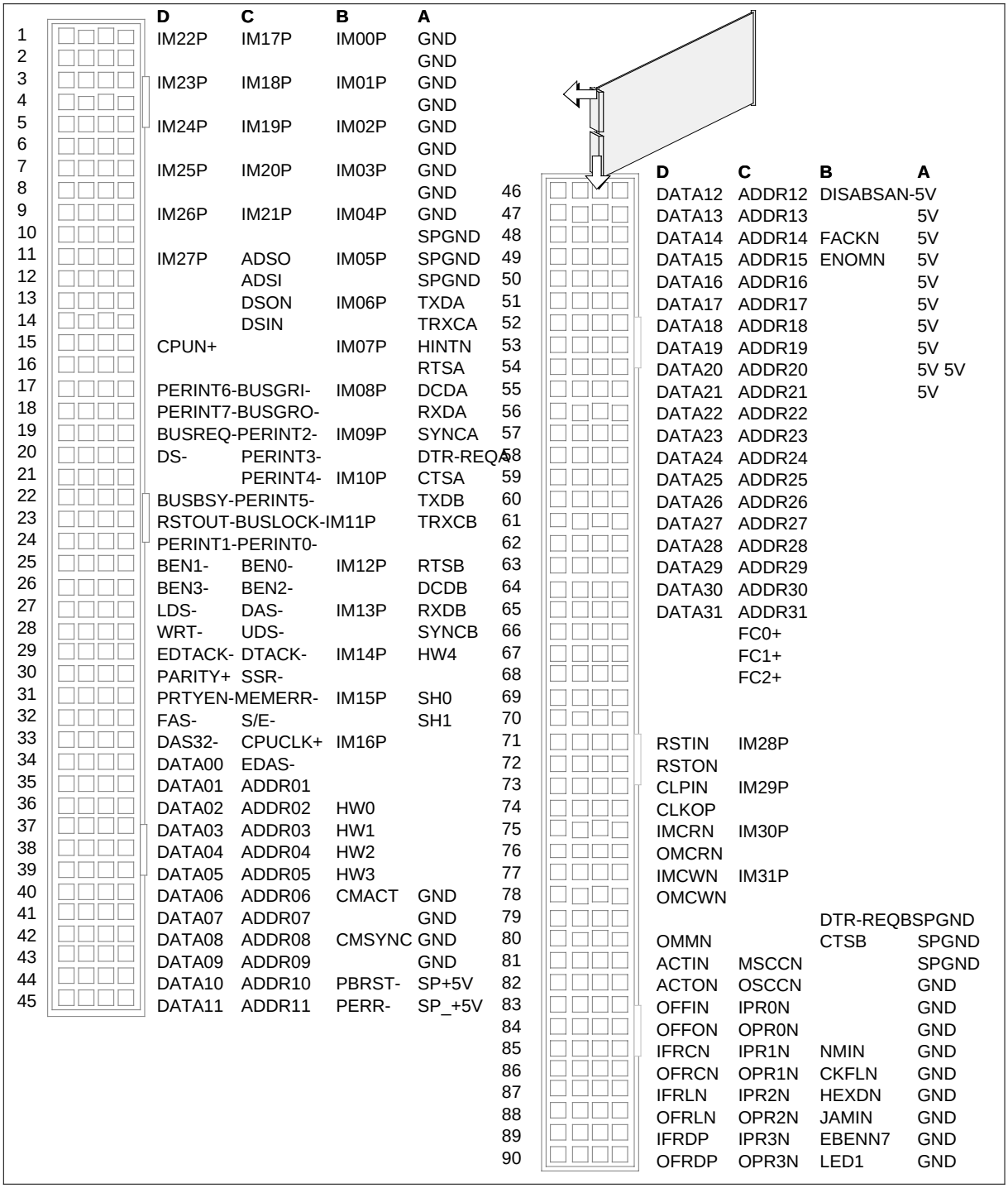
The pin numbers for NT9X13DC appear in the following figure.

Technical data

Power requirements

The NT9X13DC requires +5V, ±5%.

NT9X13DC pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2				GND
3	IM23P	IM18P	IM01P	GND
4				GND
5	IM24P	IM19P	IM02P	GND
6				GND
7	IM25P	IM20P	IM03P	GND
8				GND
9	IM26P	IM21P	IM04P	GND
10				SPGND
11	IM27P	ADSO	IM05P	SPGND
12		ADSI		SPGND
13		DSON	IM06P	TXDA
14		DSIN		TRXCA
15	CPUN+		IM07P	HINTN
16				RTSA
17	PERINT6-	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-		RXDA
19	BUSREQ-	PERINT2-	IM09P	SYNCA
20	DS-	PERINT3-		DTR-REQA
21		PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-		TXDB
23	RSTOUT-	BUSLOCK-	IM11P	TRXCB
24	PERINT1-	PERINT0-		
25	BEN1-	BEN0-	IM12P	RTSB
26	BEN3-	BEN2-		DCDB
27	LDS-	DAS-	IM13P	RXDB
28	WRT-	UDS-		SYNCB
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-		
31	PRTYEN-	MEMERR-	IM15P	SH0
32	FAS-	S/E-		SH1
33	DAS32-	CPUCLK+	IM16P	
34	DATA00	EDAS-		
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10	PBRST-	SP+5V
45	DATA11	ADDR11	PERR-	SP_+5V

	D	C	B	A
46	DATA12	ADDR12	DISABSAN-	5V
47	DATA13	ADDR13		5V
48	DATA14	ADDR14	FACKN	5V
49	DATA15	ADDR15	ENOMN	5V
50	DATA16	ADDR16		5V
51	DATA17	ADDR17		5V
52	DATA18	ADDR18		5V
53	DATA19	ADDR19		5V
54	DATA20	ADDR20		5V 5V
55	DATA21	ADDR21		5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66		FC0+		
67		FC1+		
68		FC2+		
69				
70				
71	RSTIN	IM28P		
72	RSTON			
73	CLPIN	IM29P		
74	CLKOP			
75	IMCRN	IM30P		
76	OMCRN			
77	IMCWN	IM31P		
78	OMCWN			
79			DTR-REQB	SPGND
80	OMMN		CTSB	SPGND
81	ACTIN	MSCCN		SPGND
82	ACTON	OSCCN		GND
83	OFFIN	IPR0N		GND
84	OFFON	OPR0N		GND
85	IFRCN	IPR1N	NMIN	GND
86	OFRCN	OPR1N	CKFLN	GND
87	IFRLN	IPR2N	HEXDN	GND
88	OFRLN	OPR2N	JAMIN	GND
89	IFRDP	IPR3N	EBENN7	GND
90	OFRDP	OPR3N	LED1	GND

NT9X13DD

Product description

The NT9X13DD is a DMS SuperNode processor card that performs specified applications. The card performs these applications in the junctor network (JNET), enhanced network (ENET), single shelf link peripheral processor (SS LPP), and link interface module (LIM).

The NT9X13DD has the following features:

- 20 MHz MC68020 CPU
- memory access protection, write protect
- 16 kbyte data cache
- dual channel serial communications controller (SCC)
- 16 Mbyte DRAM with ECC
- P-bus compatibility
- 256 kbyte of EPROM
- element identification (ID) PROM
- timers
- interrupts
- status and control registers
- fault indication registers (FIR)

The NT9X13DD is backwards compatible with DMS SuperNode series 10 and up.

Location

The NT9X13DD is in these slots for the following applications:

- in slot 9 for DMS SuperNode
- in slots 17, 22 for DMS SuperNode SE
- in slots 10, 20 for ENET
- in slots 17, 22 for the SS LPP for DMS SuperNode SE

Functional description

The NT9X13DD is a high performance microcomputer board based on the Motorola MC68020 32-bit microprocessor.

Functional blocks

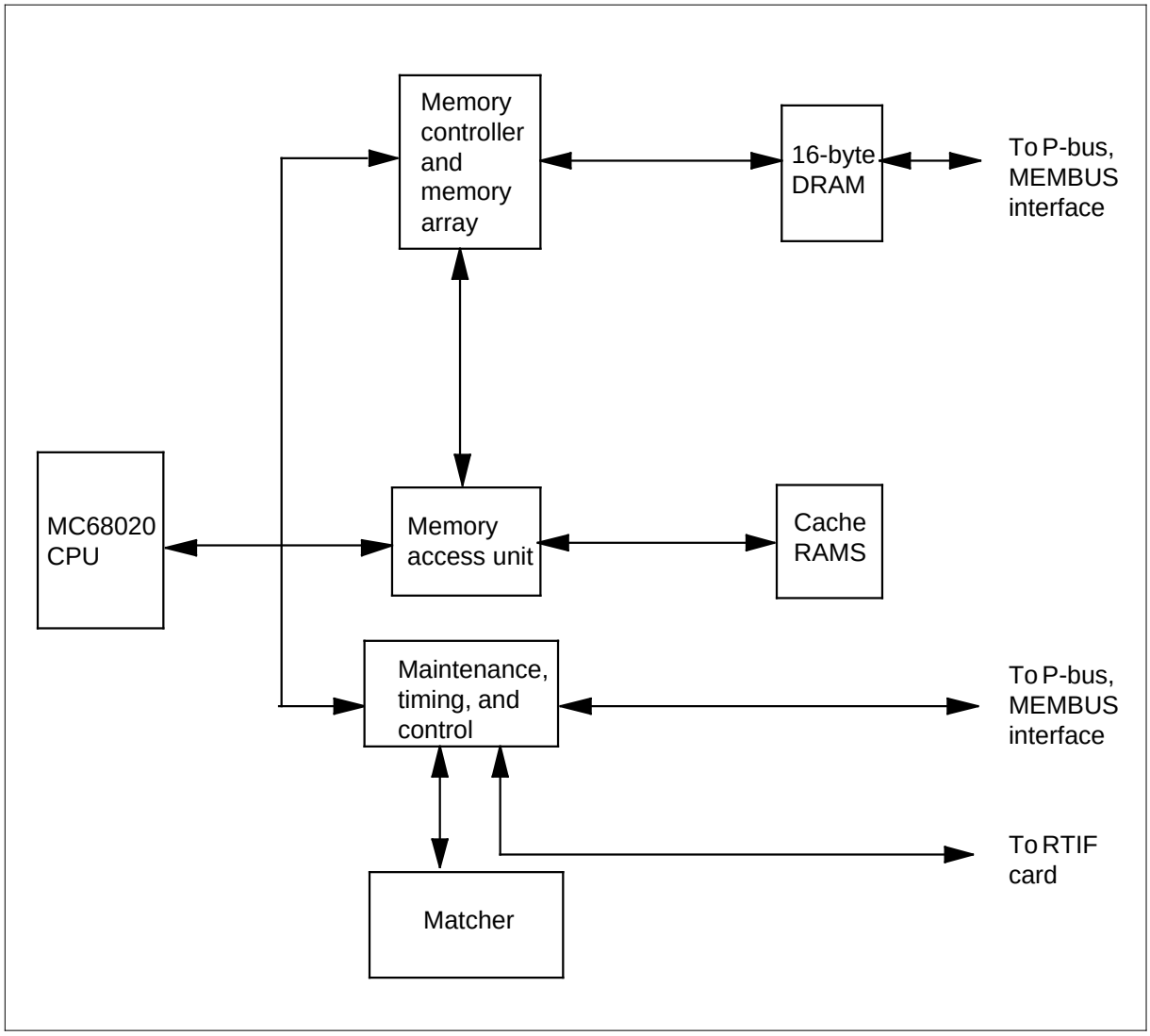
The NT9X13DD has the following functional blocks:

- MC68020 CPU
- memory access unit (MAU)
- memory controller (MEM) and memory array
- maintenance, timing, and control (MTC)
- matcher (MCH)

The relationship between the functional blocks appear in the following figure.

NT9X13DD (continued)

NT9X13DD functional blocks



68020 central processing unit

The Motorola 20 MHz MC68020 CPU is the first 32-bit external bus implementation of the MC68000 family of Motorola microprocessors. The CPU provides improved performance over earlier versions. The following resources are available:

- sixteen 32-bit general purpose address and data registers
- two 32-bit supervisor stack points
- a 32-bit program counter
- five special purpose control registers

- 4 Gbyte direct address range
- 18 addressing modes
- memory mapped I/O
- high performance on chip 256 kbyte instruction cache
- 32-bit upgraded and current instructions
- operations on seven data types

To improve performance and function, the CPU also has the following hardware features:

- multiple micro-engines for a very efficient concurrent pipeline operation
- high performance 32-bit barrel shifter in ALU
- dynamic bus sizing
- coprocessor interface

Memory access unit (MAU)

The MAU controls a data cache and provides address space access protection in 64 kbyte blocks. The MAU starts a parity protection scheme on bus accesses and the data cache. The MAU supplies the necessary control signals for the extended multiprocessor system (XMS) P-bus specification and the SuperNode CM/MEM memory bus specification.

Memory controller (MEM) and memory array

The memory module uses a 4 Mbit DRAM in a 16 Mbyte memory bank. The memory controller operates in the 32-bit environment, corrects any single data errors, and detects double or multiple errors.

Maintenance, timing, and control (MTC)

The MTC interfaces with the CPU. The MTC provides the CPU with basic signals. The signals include clock, reset, and chip selects to the associated EPROM and other peripheral modules. The MTC includes an interval timer that can be in a number of modes, and a sanity timer. Interrupts from different sources are latched, encoded and passed to the processor at a fixed priority. Maintenance circuits latch system fault detections so that the CPU can read, write or clear the detections.

The MTP provides the interface to the SCC for reset terminal interface (RTIF) communications. In duplex operation, the MTC provides clock detection and selection. The MTC also provides a serial FIR to obtain information about the mate system clock and control signals. This action allows the CPU that requests to get information from a mate that is not operational.

NT9X13DD (continued)

Matcher (MCH)

Matcher performs the following functions:

- maintains a hardware lock on the address hold register and unlocks by recovery-diagnostic software after fault detection
- provides a 32-bit maintenance control register in which the data bus can write. The mate CPU can read this register with a signal the CPU supplies. The signal laces the mate communication register (MCR) on the operational measurements (OM) bus.

Signaling

Pin numbers

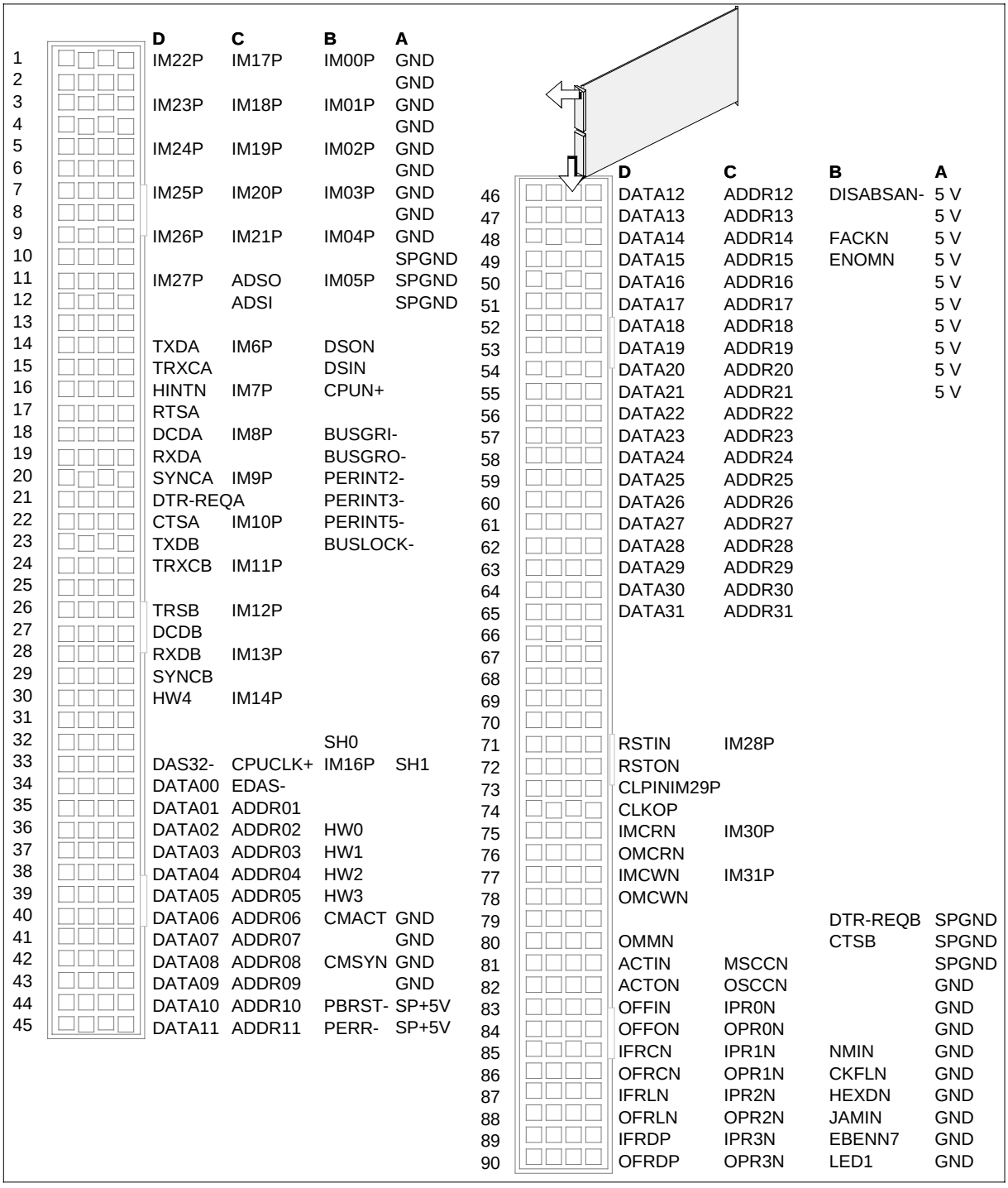
The pin numbers for the NT9X13DD appear in the following figure.

Technical data

Power requirements

The NT9X13DD requires +5V, + or - 5%.

NT9X13DD pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2				GND
3	IM23P	IM18P	IM01P	GND
4				GND
5	IM24P	IM19P	IM02P	GND
6				GND
7	IM25P	IM20P	IM03P	GND
8				GND
9	IM26P	IM21P	IM04P	GND
10				SPGND
11	IM27P	ADSO	IM05P	SPGND
12		ADSI		SPGND
13				
14	TXDA	IM6P	DSON	
15	TRXCA		DSIN	
16	HINTN	IM7P	CPUN+	
17	RTSA			
18	DCDA	IM8P	BUSGRI-	
19	RXDA		BUSGRO-	
20	SYNCA	IM9P	PERINT2-	
21	DTR-REQA		PERINT3-	
22	CTSA	IM10P	PERINT5-	
23	TXDB		BUSLOCK-	
24	TRXCB	IM11P		
25				
26	TRSB	IM12P		
27	DCDB			
28	RXDB	IM13P		
29	SYNCB			
30	HW4	IM14P		
31				
32			SH0	
33	DAS32-	CPUCLK+	IM16P	SH1
34	DATA00	EDAS-		
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYN	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10	PBRST-	SP+5V
45	DATA11	ADDR11	PERR-	SP+5V

	D	C	B	A
46	DATA12	ADDR12	DISABSAN-	5 V
47	DATA13	ADDR13		5 V
48	DATA14	ADDR14	FACKN	5 V
49	DATA15	ADDR15	ENOMN	5 V
50	DATA16	ADDR16		5 V
51	DATA17	ADDR17		5 V
52	DATA18	ADDR18		5 V
53	DATA19	ADDR19		5 V
54	DATA20	ADDR20		5 V
55	DATA21	ADDR21		5 V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70				
71	RSTIN	IM28P		
72	RSTON			
73	CLPINIM29P			
74	CLKOP			
75	IMCRN	IM30P		
76	OMCRN			
77	IMCWN	IM31P		
78	OMCWN			
79			DTR-REQB	SPGND
80	OMMN		CTSB	SPGND
81	ACTIN	MSCCN		SPGND
82	ACTON	OSCCN		GND
83	OFFIN	IPR0N		GND
84	OFFON	OPR0N		GND
85	IFRCN	IPR1N	NMIN	GND
86	OFRCN	OPR1N	CKFLN	GND
87	IFRLN	IPR2N	HEXDN	GND
88	OFRLN	OPR2N	JAMIN	GND
89	IFRDP	IPR3N	EBENN7	GND
90	OFRDP	OPR3N	LED1	GND

NT9X13DE

Product description

The NT9X13DE card is a high-performance microcomputer board based on the Motorola MC68020 32-bit microprocessor.

The NT9X13DE card has the following features:

- 16-MHz MC68020 central processing unit (CPU)
- memory access protection
- 16-kbyte data cache
- dual-channel serial communications controller (SCC)
- 16-Mbyte dynamic RAM (DRAM) with error-correction code (ECC)
- processor bus (P-bus) compatibility
- 256 kbyte of erasable programmable read-only memory (EPROM)
- element identification (ID) PROM
- timers
- interrupts
- status and control registers
- fault indication registers

Location

The NT9X13DE card is located in the link interface module (LIM) shelf in the enhanced link peripheral processor (ELPP) cabinet.

Functional description

The NT9X13DE card performs the same functions as the NT9X13DD (CPU 16-MHz card), but the firmware of the DE version is changed to accommodate the fiber-optic initialization of the ELPP cabinet. The redesigned firmware makes the NT9X13DE card compatible with the NT9X62BB paddle board, which provides an interface to the fiber-optic links in the ELPP cabinet.

Functional blocks

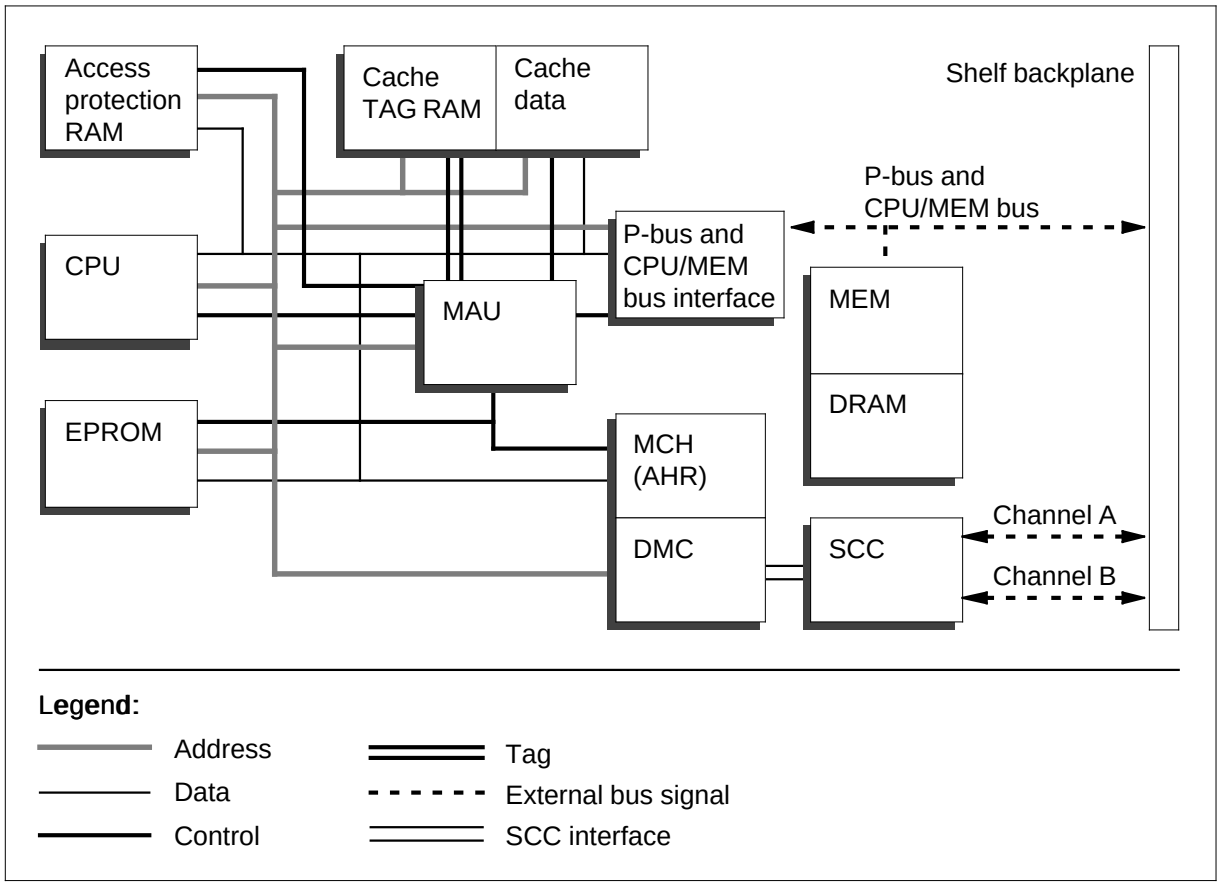
NT9X13DE has the following functional blocks:

- MC68020 CPU
- memory access unit (MAU)
- memory (MEM) controller and memory array
- DMS maintenance controller (DMC)

- matcher (MCH)
- dual-channel SCC

The following figure shows the relationship of the functional blocks.

NT9X13DE functional blocks



MC68020 central processing unit

The Motorola 32-bit 16-MHz MC68020 CPU is the main processing engine of the NT9X13DE card. The processor provides the following resources:

- sixteen 32-bit general-purpose address and data registers
- two 32-bit supervisor stack pointers
- 32-bit program counter
- five special-purpose control registers
- 4-Gbyte direct address range
- eighteen addressing modes

NT9X13DE (continued)

- memory mapped input/output (I/O)
- high-performance on-chip 256-byte instruction cache
- 32-bit upgraded and new instructions
- operations on seven data types

Memory access unit

The MAU controls and allows direct access to the data cache. It also provides access protection over processor address space and parity generation and checking for the data cache and selected backplane access. The MAU supplies control signals for the extended multiprocessor system (XMS) P-bus specifications and the memory bus specifications.

Memory controller and memory array

The memory module uses a 4-Mbit DRAM. The memory controller, which is the main component of the memory module, operates in the 32-bit environment. It corrects any single data errors and detects any double or multiple errors.

DMS maintenance controller

The DMC performs maintenance functions. The DMC interfaces directly with the CPU, providing it with basic signals like clock, reset, and chip selects to the associated EPROM and other peripheral modules. The DMC incorporates an interval and sanity timer. Interrupts from the different sources are latched, encoded, and passed to the processor at a fixed priority. The DMC also interfaces with the SCC for the reset terminal interface (RTIF) communications.

Matcher

The matcher (MCH) provides an address hold register (AHR) function during error conditions. When the DMC detects an error, the MCH holds in the AHR the address of the last bus cycle that started before the error. The AHR retains the address of the bus cycle until the DMC releases the hold signal.

Dual-channel SCC

The Zilog Z8530 is a non-multiplexed bus SCC. It is a dual-channel device: channel A receives signals and channel B transmits signals. Channels A and B are independent of each other. SCC provides baud-rate programmable asynchronous or synchronous modes of operations.

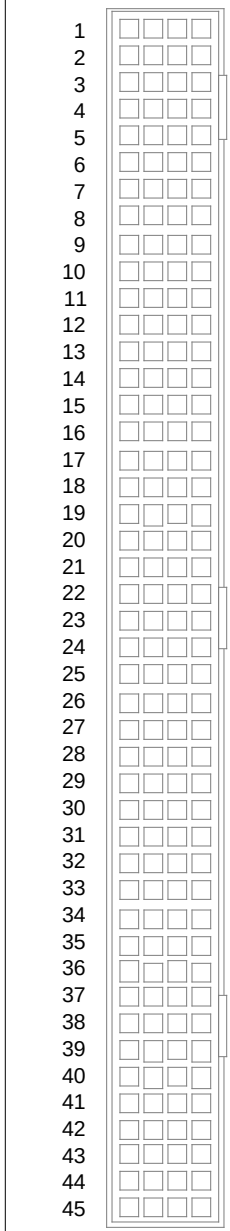
Signaling

Pin outs

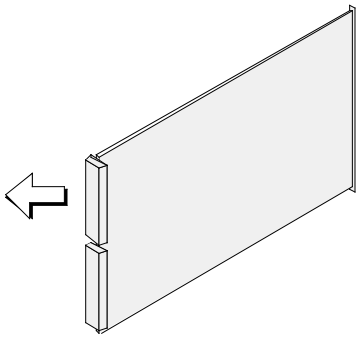
The following figure shows the pin outs for NT9X13DE.

NT9X13DE (continued)

NT9X13DE pin outs (part 1 of 2)

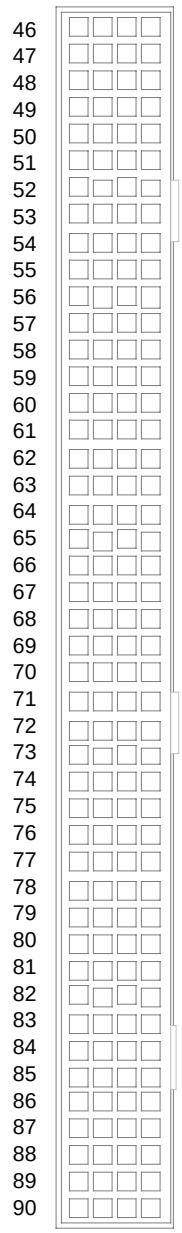


	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2				GND
3	IM23P	IM18P	IM01P	GND
4				GND
5	IM24P	IM19P	IM02P	GND
6				GND
7	IM25P	IM20P	IM03P	GND
8				GND
9	IM26P	IM21P	IM04P	GND
10				SPGND
11	IM27P	ADSO	IM05P	SPGND
12		ADSI		SPGND
13		DSON	IM06P	TXDA
14		DSIN		TRXCA
15	CPUN+		IM07P	HINTN
16				RTSA
17	PERINT6-	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-		RXDA
19	BUSREQ-	PERINT2-	IM09P	SYNCA
20	DS-	PERINT3-		DTR-REQA
21		PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-		TXDB
23	RSTOUT-	BUSLOCK-	IM11P	TRXCB
24	PERINT1-	PERINT0-		
25	BEN1-	BEN0-	IM12P	RTSB
26	BEN3-	BEN2-		DCDB
27	LDS-	DAS-	IM13P	RXDB
28	WRT-	UDS-		SYNCB
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-		
31	PRTYEN-	MEMERR-	IM15P	
32	FAS-	S/E-		SH0
33	DAS32-	CPUCLK+	IM16P	SH1
34	DATA00	EDAS-		
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10	PBRST-	SP+5 V
45	DATA11	ADDR11	PERR-	SP+5 V



NT9X13DE (continued)

NT9X13DE pin outs (part 2 of 2)



	D	C	B	A
46	DATA12	ADDR12	DISABSAN-	5 V
47	DATA13	ADDR13		5 V
48	DATA14	ADDR14	FACKN	5 V
49	DATA15	ADDR15	ENOMN	5 V
50	DATA16	ADDR16		5 V
51	DATA17	ADDR17		5 V
52	DATA18	ADDR18		5 V
53	DATA19	ADDR19		5 V
54	DATA20	ADDR20		5 V
55	DATA21	ADDR21		5 V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66		FC0+		
67		FC1+		
68		FC2+		
69				
70				
71	RSTIN	IM28P		
72	RSTON			
73	CLPIN	IM29P		
74	CLKOP			
75	IMCRN	IM30P		
76	OMCRN			
77	IMCWN	IM31P		
78	OMCWN			
79			DTR-REQB	SPGND
80	OMMN		CTSB	SPGND
81	ACTIN	MSCCN		SPGND
82	ACTON	OSCCN		GND
83	OFFIN	IPR0N		GND
84	OFFON	OPR0N		GND
85	IFRCN	IPR1N	NMIN	GND
86	OFRCN	OPR1N	CKFLN	GND
87	IFRLN	IPR2N	HEXDN	GND
88	OFRLN	OPR2N	JAMIN	GND
89	IFRDP	IPR3N	EBENN7	GND
90	OFRDP	OPR3N	LED1	GND

Technical data

The NT9X13DE requires the following environmental conditions:

- +5°C to +50°C temperature
- 10% to 95% humidity

Power requirements

The following table lists the power requirements for NT9X13DE card.

NT9X13DE power requirements

Parameter	Minimum	Nominal	Maximum
Supply voltage	4.75 V	5.0 V	5.25 V
Supply current (fuse 1)		0.5 A	
Supply current (fuse 2)		3.7 A	

NT9X13FA

Product description

The NT9X13FA DMS SuperNode processor card is a high-performance microcomputer board based on the Motorola MC68020 32-bit microprocessor. The microprocessor board is for specified purpose application in the enhanced network (ENET).

The NT9X13FA has the following features:

- 20 MHz MC68020 CPU
- memory access protection, write protect
- 16 kbyte data cache
- dual-channel serial communications controller (SCC)
- 4 Mbytes dynamic RAM (DRAM) with error correction code (ECC)
- processor bus (P-bus) compatibility
- 128 kbytes of EPROM
- element identification (ID) PROM
- timers
- interrupts
- status and control registers
- fault indication registers (FIR)

Functional description

Functional blocks

The NT9X13FA contains the following functional blocks:

- MC68020 CPU
- memory access unit (MAU)
- memory controller (MEM) and memory array
- maintenance, timing, and control (MTC)
- matcher (MCH)

MC68020 CPU

The 20 MHz MC68020 CPU is the main processing engine of the NT9X13FA. The CPU provides improved performance over the earlier MC6800 CPUs.

Memory access unit

This functional block controls a data cache, provides address space access protection in 64 kbyte blocks. The block starts a parity protection scheme on bus accesses and the data cache. The block supplies the necessary control signals. The signals are for the extended multiprocessor system (XMS) P-bus specification and the SuperNode CM/MEM memory bus specification.

Memory controller

The memory controller can correct any single data errors and detect double or multiple errors.

Maintenance, timing, and control

The MTC interfaces with the 38020 CPU. The MTC provides the CPU with basic signals like clock, reset, and chip selects to the associated EPROM and other peripherals. The MTC includes an interval timer for a number of modes, and a sanity timer. Interrupts from the different sources are latched, encoded and passed to the processor at a fixed priority. The MTP provides the interface to the SCC for reset terminal interface (RTIF) communications. In duplex operation, the MTC provides clock detection and selection. The MTC also provides a serial FIR to obtain information about the mate system clock and control signals. The MTC allows the CPU that requests information from a mate that is not operational.

Matcher

The MCH performs the following functions:

- compares address and data on MC68020 CPU bus cycles against the address and data of CPU mate to provide mismatch error detection
- multiplexes bus cycles address and data to the outgoing match bus to allow the mate MCH to perform the same match check
- passes the incoming match bus from mate to the data bus when the MTC requests the start of the update mode of operation. A computing module (CM) updates the mate of the CM memory data on read cycles.
- maintains a hardware lock on the address hold register and unlocks by recovery diagnostic software after fault detection
- provides a 32-bit maintenance control register that the data bus can write and the mate CPU can read from. This register is under control of a signal the CPU supplies to lace the mate communication register (MCR) on the operational measurements (OM) bus.

Signaling

Pin numbers

The NT9X13FA pin numbers for appear in the following figure.

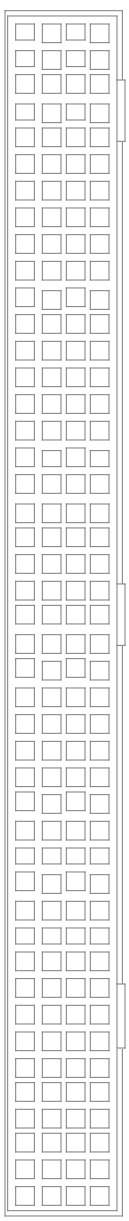
NT9X13FA (continued)

Technical data

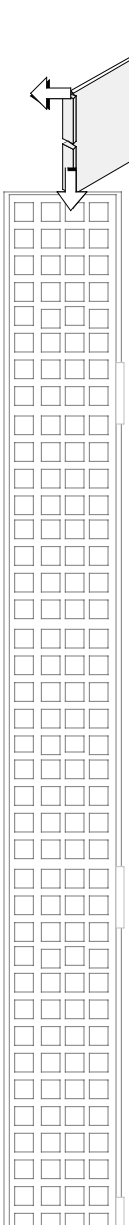
Power requirements

The NT9X13FA requires +5V, ±5%.

NT9X13FA pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2				GND
3	IM23P	IM18P	IM01P	GND
4				GND
5	IM24P	IM19P	IM02P	GND
6				GND
7	IM25P	IM20P	IM03P	GND
8				GND
9	IM26P	IM21P	IM04P	GND
10				SPGND
11	IM27P	ADSO	IM05P	SPGND
12		ADSI		SPGND
13		DSON	IM06P	TXDA
14		DSIN		TRXCA
15	CPUN+	IM07P	HINTN	
16				RTSA
17	PERINT6-	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-		RXDA
19	BUSREQ-	PERINT2-	IM09P	SYNCA
20	DS-	PERINT3-		DTR-REQA
21		PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-		TXDB
23	RSTOUT-	BUSLOCK-	IM11P	TRXCB
24	PERINT1-	PERINT0-		
25	BEN1-	BEN0-	IM12P	RTSB
26	BEN3-	BEN2-		DCDB
27	LDS-	DAS-	IM13P	RXDB
28	WRT-	UDS-		SYNCB
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-		
31	PRTYEN-	MEMERR-	IM15P	SH0
32	FAS-	S/E-		SH1
33	DAS32-	CPUCLK+	IM16P	
34	DATA00	EDAS-		
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10	PBRST-	SP+5V
45	DATA11	ADDR11	PERR-	SP_+5V



	D	C	B	A
46	DATA12	ADDR12	DISABSAN-	5V
47	DATA13	ADDR13		5V
48	DATA14	ADDR14	FACKN	5V
49	DATA15	ADDR15	ENOMN	5V
50	DATA16	ADDR16		5V
51	DATA17	ADDR17		5V
52	DATA18	ADDR18		5V
53	DATA19	ADDR19		5V
54	DATA20	ADDR20		5V 5V
55	DATA21	ADDR21		5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66		FC0+		
67		FC1+		
68		FC2+		
69				
70				
71	RSTIN	IM28P		
72	RSTON			
73	CLPIN	IM29P		
74	CLKOP			
75	IMCRN	IM30P		
76	OMCRN			
77	IMCWN	IM31P		
78	OMCWN			
79			DTR-REQ	BSPGND
80	OMMN		CTSB	SPGND
81	ACTIN	MSCCN		SPGND
82	ACTON	OSCCN		GND
83	OFFIN	IPR0N		GND
84	OFFON	OPR0N		GND
85	IFRCN	IPR1N	NMIN	GND
86	OFRCN	OPR1N	CKFLN	GND
87	IFRLN	IPR2N	HEXDN	GND
88	OFRLN	OPR2N	JAMIN	GND
89	IFRDP	IPR3N	EBENN7	GND
90	OFRDP	OPR3N	LED1	GND

NT9X13GA

Product description

The NT9X13GA high-performance module (HPM)-based CPU card provides a real-time performance gain. The gain occurs when the card supports software compatibility. The processor card allows a direct card-for-card replacement with the NT9X13 DMS-core processor card.

Compatibility

Use NT9X13GA the card with other CPU cards that can operate in the split-mode functions. These functions support a warm switch of activity (SWACT).

Use NT9X13GA the only with software loads of BCS29 and up.

The NT9X13GA is compatible with all other connection memory (CM) hardware. This compatibility means that a CM upgrade for the required real-time improvements requires the CPU card. The CPU card does not operate with other CPU cards except another .

Functional description

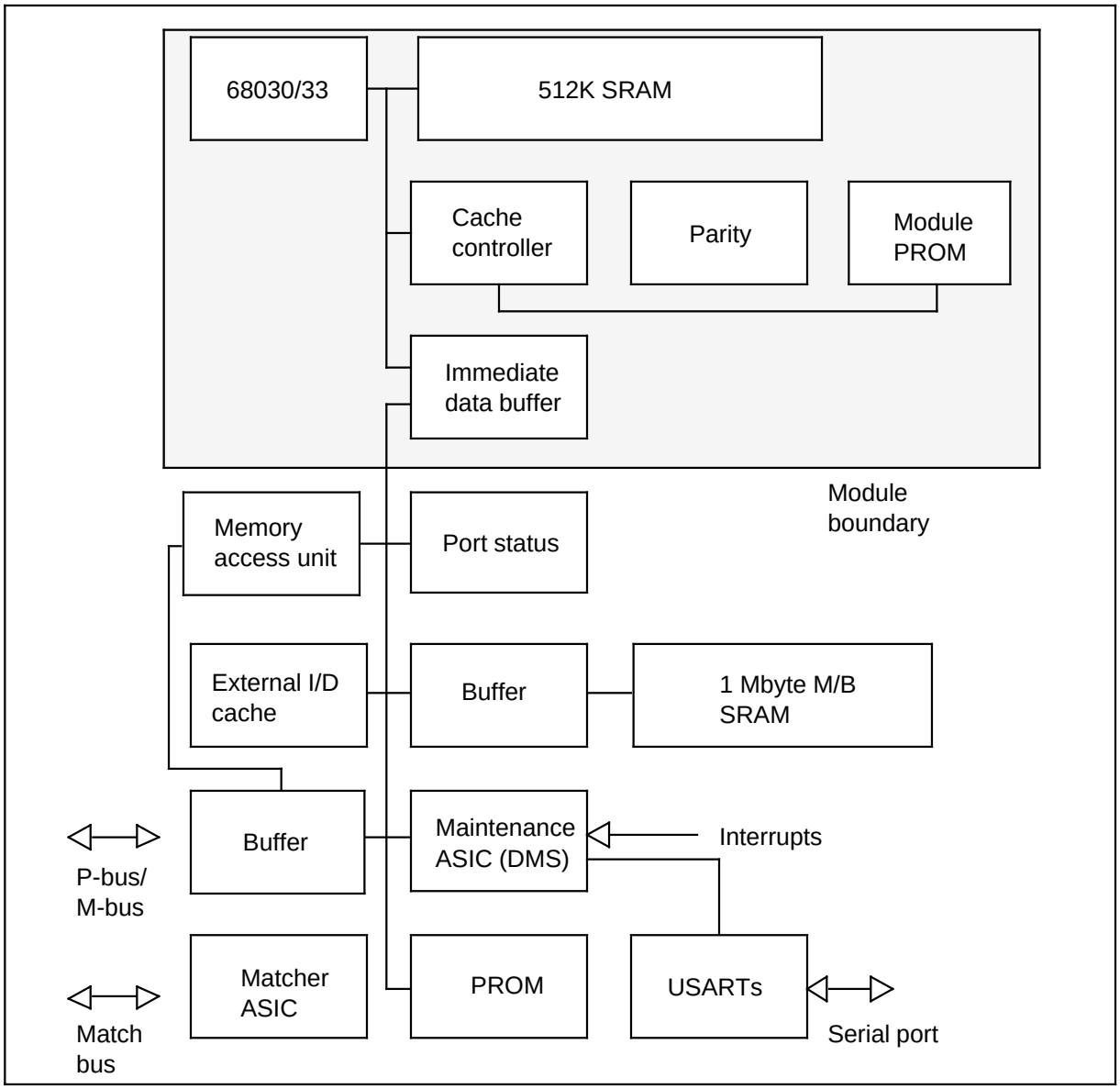
Functional blocks

The NT9X13GA contains the following functional blocks:

- HPM
- motherboard control
- maintenance controller
- clock control
- memory access unit (MAU)
- system bus interface
- duplex support
- Z8530 serial communications controller (SCC)
- element identification (ID) PROM

The relationship of these parts appears in the following figure.

NT9X13GA functional blocks



High-performance module

The HPM contains a 68030 processor, a cache controller, a module/motherboard interface, and motherboard memory.

NT9X13GA (continued)

Motherboard control

The motherboard control contains 17 programmable array logic (PAL) devices, P1 to P17 as follows:

- board address strobe (BPAS) (P1)
- motherboard static RAM (SRAM) control (P2)
- motherboard SRAM parity (P3)
- maintenance tape center (MTC) decode (P4)
- control register (P5)
- motherboard SRAM sequencer (P6)
- STA (P7)
- module interface (P8)
- element address decode (P9)
- (P10)
- clock (P11)
- address decode (P12)
- (P13)
- function code translation (P14)
- access protection (P15)
- (P16)
- initial program load (IPL) synchronization (P17)

Maintenance controller

The maintenance controller is near the H04 maintenance gate array on the NT9X13 series of CPUs. The maintenance controller is the DMS maintenance controller (DMC H85/H85).

The main functions of this chip are as follows:

- interrupt encoder and interrupt mismatch monitor
- interval and sanity timer
- serial maintenance port
- universal sychronous/asychronous receiver/transmitter (USART) interface
- EPROM interface
- matcher interface

- activity control
- reset control circuits
- status indication registers
- address and data parity circuits
- clock source failure monitor

Clock control

The clock control performs the following functions:

- synchronizes the 16 MHz clocks on both planes to make sure the clocks are in phase
- selects between the control clock and the mate clock to drive the processor card
- holds the 33 MHz clock in the high state when a controlled clock switch occurs
- minimizes the skew between the specified clocks on both planes and makes sure the 68030 clock requirements are met

Memory access unit

The MAU supports the following features:

- high-performance memory communication through a private synchronous memory bus (M-bus) interface protocol
- a standard purpose memory and peripheral interface through the processor bus (P-bus) specification
- bus parity checking
- CM handshaking support for duplex applications
- external caching
- address space access protection of the lower 256 Mbyte address range (in 64 kbyte blocks)

System bus interface

The system bus interface operates at 33 MHz. The limit on the interface is normally for the CPU modules, the clocks, and the local motherboard memory array.

The higher performance synchronous M-Bus and the general purpose P-bus interface are supported on the CPU card. The card also supports the current single-bit parity.

NT9X13GA (continued)

Duplex support

The NT9X13GA CPU card supports the current lock-step matching plans used with the DMS-core computing module.

Zilog Z8530 serial communications controller

The Zilog Z8530 is a non-multiplexed bus SCC with the following capabilities:

- two separate full-duplex channels
- separate programmable baud rate generators in each channel for synchronous/iso-synchronous data rates

The Zilog Z8530 also has the following asynchronous capabilities:

- 5, 6, 7, or 8 bits for each character
- 1, 1.5, or 2 stop bits
- odd or even parity
- X1, X16, X32, or X64 clock modes
- break generation and detection
- parity, overrun, and framing error detection

Identification PROM

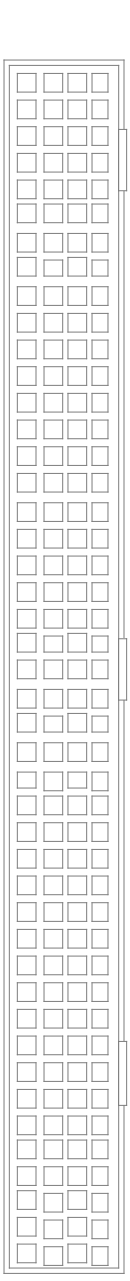
The NT9X13GA supports the DMS-core requirement of the ID PROM. This PROM contains the product engineering code (PEC) code and vintage information to aid in system configuration. The CPU card is the smart entity on the DMS-core bus. The motherboard design limits the access of the PROM to occur from the PROM. The motherboard design does not allow access from the backplane.

Pin numbers

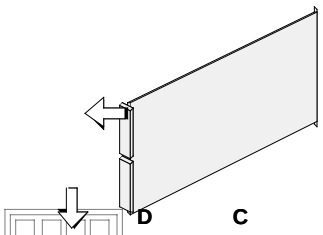
The pin numbers for the NT9X13GA appear in the following figure

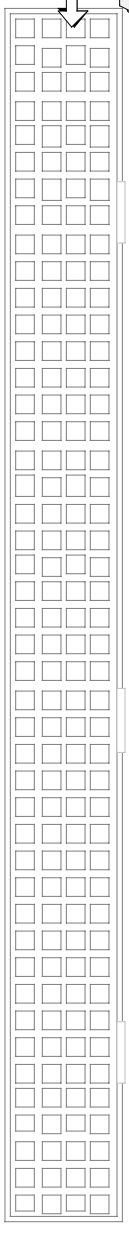
NT9X13GA (continued)

NT9X13GA pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	Gnd
2	OM22P	OM17P	OM00P	Gnd
3	IM23P	IM18P	IM01P	Gnd
4	OM23P	OM18P	OM01P	Gnd
5	IM24P	IM19P	IM02P	Gnd
6	OM24P	OM19P	OM02P	Gnd
7	IM25P	IM20P	IM03P	Gnd
8	OM25P	OM20P	OM03P	Gnd
9	IM26P	IM21P	IM04P	Gnd
10	OM26P	OM21P	OM04P	Gnd
11	IM27P	SYNC16–	IM05P	Gnd
12	OM27P	SYNC16–	OM05P	Gnd
13		DSON	IM06P	TXDA
14		DSIN	OM06P	TRXCA
15	CPUN+	IM07P	HINTN	
16		Gnd	OM08P	RTSA
17	PERINT6	BUSGRI–	IM08P	DCDA
18	PERINT7–	BUSGRO–	OM08P	RXDA
19	BUSREQ–	PERINT2–	IM09P	SYNCA
20	DS–	PERINT3–	OM09P	DTR–REQA
21		PERINT4–	IM10P	CTSA
22	BUSBSY–	PERINT5–	OM10P	TXDB
23	RSTOUT–	BUSLOCK–	IM11P	TRXCB
24	PERINT1–	PERINT0–	OM11P	
25	BEN1–	BENO–	IM12P	RTSB
26	BEN3–	BEN2–	OM12P	DCDB
27	Gnd	DAS–	IM13P	RXDB
28	WRT–	Gnd	OM14P	SYNCB
29	EDTACK–	DTACK–	IM14P	HW4
30	PARITY+	SSR–	OM14P	
31	PRTYEN–	MEMERR–	IM15P	
32	FAS–	Gnd	OM15P	SH0
33	DAS32–	CPUCLK+	IM16P	SH1
34	DATA00	EDAS–	OM16P	
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW3	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	Gnd
41	DATA07	ADDR07		Gnd
42	DATA08	ADDR08	CMSYNC	Gnd
43	DATA09	ADDR09		Gnd
44	DATA10	ADDR10	PBRST–	+5V
45	DATA11	ADDR11	PERR–	+5V





	D	C	B	A
46	DATA12	ADDR12	DISABSAN	5V
47	DATA13	ADDR13	Gnd	5V
48	DATA14	ADDR14	FACKN	5V
49	DATA15	ADDR15	ENOMN	5V
50	DATA16	ADDR16		5V
51	DATA17	ADDR17		5V
52	DATA18	ADDR18		5V
53	DATA19	ADDR19		5V
54	DATA20	ADDR20		5V
55	DATA21	ADDR21	Gnd	5V
56	DATA22	ADDR22	Gnd	
57	DATA23	ADDR23	Gnd	
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27	Gnd	Gnd
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		Gnd
66		FC0+		Gnd
67		FC1+		
68		FC2+		
69				
70				Gnd
71	RSTIN	IM28P		Gnd
72	RSTON	OM28P		
73	CLPIN	IM29P		
74	CLKOP	OM29P		
75	IMCRN	IM30P		Gnd
76	OMCRN	OM30P		
77	IMCWN	IM31P		
78	OMCWN	OM31P		
79			DTR–REQB	Gnd
80	OMMN		CTSB	Gnd
81	ACTIN	MSCCN		Gnd
82	ACTON	OSCCN		Gnd
83	OFFIN	IPR0N		Gnd
84	OFFON	OPR0N		Gnd
85	IFCRN	IPR1N	NMIN	Gnd
86	OFRCN	OPR1N	CKFLN	Gnd
87	IFRLN	IPR2N	HEXDN	Gnd
88	OFRLN	OPR2N	JAMIN	Gnd
89	IFRDP	IPR3N	EBENN7	Gnd
90	OFRDP	OPR3N	LED1	Gnd

NT9X13GA (end)

Technical data

The power requirements for the NT9X13GA appear in this section.

Power requirements

The power requirements for the NT9X13GA appear in the following table.

NT9X13GA power requirements

NT9X13GA parts	+5V supply current (MA)
40-MHz CPU module	2200
motherboard ASICs	120
serial controller	72
local SRAM	1060
EPROM	20
external cache	450
PALs	2160
discrete logic	510
MSI buffers	1570
passive networks	500
Total	8.57 A

NT9X13HA

Product description

The NT9X13HA 40 MHz 68030 high-performance module (HPM)-based processor card provides a real-time performance gain. The gain occurs when the card supports software compatibility. The processor card allows a direct card-for-card replacement with the current NT9X13 DMS-core processor card.

Compatibility

The NT9X13HA is compatible with other CPU cards that can operate in the split-mode functions. These functions support a warm switch of activity (SWACT).

Use NT9X13HA the with software loads of BCS29 and up.

The NT9X13HA is compatible with all other connection memory (CM) hardware. A CM upgrade for the required real-time improvements involves the CPU card. The CPU card does not operate with any CPU card except another

Functional description

Functional blocks

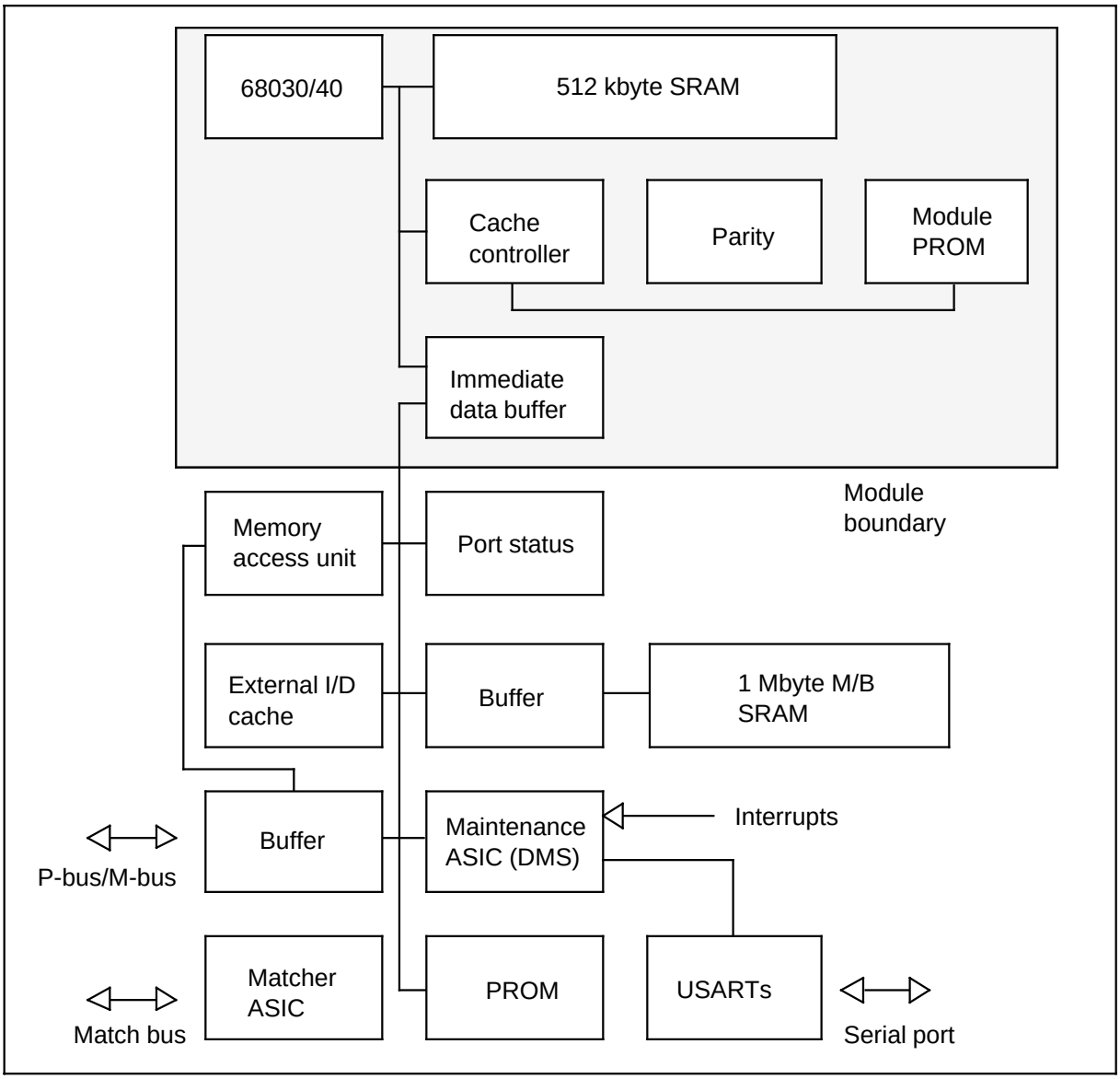
The NT9X13HA contains the following functional blocks:

- high-performance module (HPM)
- motherboard control
- maintenance controller
- clock control
- memory access unit (MAU)
- system bus interface
- duplex support
- element identification (ID) PROM
- Z8530 serial communications controller (SCC)

The functional relationship of these parts appears in the following figure.

NT9X13HA (continued)

NT9X13HA functional blocks



High-performance module

The HPM consists of a 68030 processor, a cache controller, a module/motherboard interface, and motherboard memory.

Motherboard control

The motherboard control contains 17 programmable array logic (PAL) devices, P1 to P17.

- board address strobe (BPAS) (P1)
- motherboard static RAM (SRAM) control (P2)
- motherboard SRAM parity (P3)
- maintenance tape center (MTC) decode (P4)
- control register (P5)
- motherboard SRAM sequencer (P6)
- STA (P7)
- module interface (P8)
- element address decode (P9)
- (P10)
- clock (P11)
- address decode (P12)
- (P13)
- function code translation (P14)
- access protection (P15)
- (P16)
- initial program load (IPL) synchronization (P17)

Maintenance controller

The maintenance controller is from the H04 maintenance gate array on the NT9X13 series of CPUs. The maintenance controller is the DMS maintenance controller (DMC H85/H85).

The main functions of the chip are as follows:

- interrupt encoder and interrupt mismatch monitor
- interval and sanity timer
- serial maintenance port
- universal synchronous-asynchronous receiver-transmitter (USART) interface
- EPROM interface
- matcher interface

NT9X13HA (continued)

- activity control
- reset control circuits
- status indication registers
- address and data parity circuits
- clock source failure monitor

Clock control

The clock control performs the following functions:

- synchronizes the 16 MHz clocks on both planes to make sure the clocks are in phase
- selects between the control clock and the mate clock to drive the processor card
- holds the 40 MHz clock in the high state when a controlled clock switch occurs
- minimizes the skew between the selected clocks on both planes and makes sure the 68030 clock requirements are met

Memory access unit

The MAU supports the following features:

- high performance memory communication through a private synchronous memory bus (M-bus) interface protocol
- a standard purpose memory and peripheral interface through the processor bus (P-bus) bus specification
- bus parity checks
- CM handshaking support for duplex applications
- external caches
- address space access protection of the lower 256 Mbyte address range (in 64 kbyte blocks)

System bus interface

The system bus interface operates at 40 MHz. The limit on the interface is for the CPU modules, the clocks, and the local motherboard memory array.

The higher performance synchronous M-bus and the general purpose P-bus interface are supported on the CPU card. The card also supports the current single-bit parity.

Duplex support

The NT9X13 HPM CPU card supports the current lock-step that matches plans with the DMS-core computing module.

Identification PROM

The NT9X13HA supports the DMS-core requirement of the ID PROM. This PROM contains the product engineering code (PEC) code and vintage information to aid in system configuration. The CPU card is the smart entity on the DMS-core bus. The motherboard design limits access of the PROM to occur from the PROM. The motherboard design limits do not occur from the backplane.

Zilog Z8530 serial communications controller

The Zilog Z8530 is a bus SCC that is not multiplexed. The SCC has the following capabilities:

- two separate full-duplex channels
- separate programmable baud-rate generators in each channel for synchronous/isosynchronous data rates

The Zilog Z8530 also has the following asynchronous capabilities:

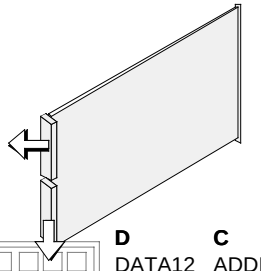
- 5, 6, 7, or 8 bits per character
- 1, 1.5, or 2 stop bits
- odd or even parity
- X1, X16, X32, or X64 clock modes
- break generation and detection
- parity, overrun, and framing error detection

Pin numbers

The pin numbers for the NT9X13HA appear in the following figure.

NT9X13HA (continued)

NT9X13HA pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	Gnd
2	OM22P	OM17P	OM00P	Gnd
3	IM23P	IM18P	IM01P	Gnd
4	OM23P	OM18P	OM01P	Gnd
5	IM24P	IM19P	IM02P	Gnd
6	OM24P	OM19P	OM02P	Gnd
7	IM25P	IM20P	IM03P	Gnd
8	OM25P	OM20P	OM03P	Gnd
9	IM26P	IM21P	IM04P	Gnd
10	OM26P	OM21P	OM04P	Gnd
11	IM27P	SYNC16–	IM05P	Gnd
12	OM27P	SYNC16–	OM05P	Gnd
13		DSON	IM06P	TXDA
14		DSIN	OM06P	TRXCA
15	CPUN+		IM07P	HINTN
16		Gnd	OM08P	RTSA
17	PERINT6	BUSGRI–	IM08P	DCDA
18	PERINT7–	BUSGRO–	OM08P	RXDA
19	BUSREQ–	PERINT2–	IM09P	SYNCA
20	DS–	PERINT3–	OM09P	DTR–REQA
21		PERINT4–	IM10P	CTSA
22	BUSBSY–	PERINT5–	OM10P	TXDB
23	RSTOUT–	BUSLOCK–	IM11P	TRXCB
24	PERINT1–	PERINT0–	OM11P	
25	BEN1–	BENO–	IM12P	RTSB
26	BEN3–	BEN2–	OM12P	DCDB
27	Gnd	DAS–	IM13P	RXDB
28	WRT–	Gnd	OM14P	SYNCB
29	EDTACK–	DTACK–	IM14P	HW4
30	PARITY+	SSR–	OM14P	
31	PRTYEN–	MEMERR–	IM15P	
32	FAS–	Gnd	OM15P	SH0
33	DAS32–	CPUCLK+	IM16P	SH1
34	DATA00	EDAS–	OM16P	
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW3	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	Gnd
41	DATA07	ADDR07		Gnd
42	DATA08	ADDR08	CMSYNC	Gnd
43	DATA09	ADDR09		Gnd
44	DATA10	ADDR10	PBRST–	+5V
45	DATA11	ADDR11	PERR–	+5V

	D	C	B	A
46	DATA12	ADDR12	DISABSAN	5V
47	DATA13	ADDR13	Gnd	5V
48	DATA14	ADDR14	FACKN	5V
49	DATA15	ADDR15	ENOMN	5V
50	DATA16	ADDR16		5V
51	DATA17	ADDR17		5V
52	DATA18	ADDR18		5V
53	DATA19	ADDR19		5V
54	DATA20	ADDR20		5V
55	DATA21	ADDR21	Gnd	5V
56	DATA22	ADDR22	Gnd	
57	DATA23	ADDR23	Gnd	
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27	Gnd	Gnd
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		Gnd
66		FC0+		Gnd
67		FC1+		
68		FC2+		
69				
70				Gnd
71	RSTIN	IM28P		Gnd
72	RSTON	OM28P		
73	CLPIN	IM29P		
74	CLKOP	OM29P		
75	IMCRN	IM30P		Gnd
76	OMCRN	OM30P		
77	IMCWN	IM31P		
78	OMCWN	OM31P		
79			DTR–REQB	Gnd
80	OMMN		CTSB	Gnd
81	ACTIN	MSCCN		Gnd
82	ACTON	OSCCN		Gnd
83	OFFIN	IPR0N		Gnd
84	OFFON	OPR0N		Gnd
85	IFCRN	IPR1N	NMIN	Gnd
86	OFRCN	OPR1N	CKFLN	Gnd
87	IFRLN	IPR2N	HEXDN	Gnd
88	OFRLN	OPR2N	JAMIN	Gnd
89	IFRDP	IPR3N	EBENN7	Gnd
90	OFRDP	OPR3N	LED1	Gnd

Technical data

The power requirements for the NT9X13HA appear in this section.

Power requirements

The power requirements for the NT9X13HA appear in the following table.

NT9X13HA power requirements

NT9X13HA parts	+5V supply current (mA)
40-MHz CPU module	2200
motherboard ASICs	120
serial controller	72
local SRAM	1060
EPROM	20
external cache	450
PALs	2160
discrete logic	510
MSI buffers	1570
passive networks	500
total	8.57 A

NT9X13HB

Product description

The NT9X13HB CPU (68030) 40-MHz processor card provides a real-time performance gain while the processor card supports software compatibility. The processor card allows a direct card-for-card replacement with the current NT9X13 DMS-core processor card.

Compatibility

The NT9X13HB must be in use with software loads of BCS30 and higher.

The NT9X13HB is compatible with all other connection memory (CM) hardware. The upgrade of the CM for the required real-time enhancements involves only the CPU card. The CPU card does not operate in synchronization with any other CPU card except another .

Functional description

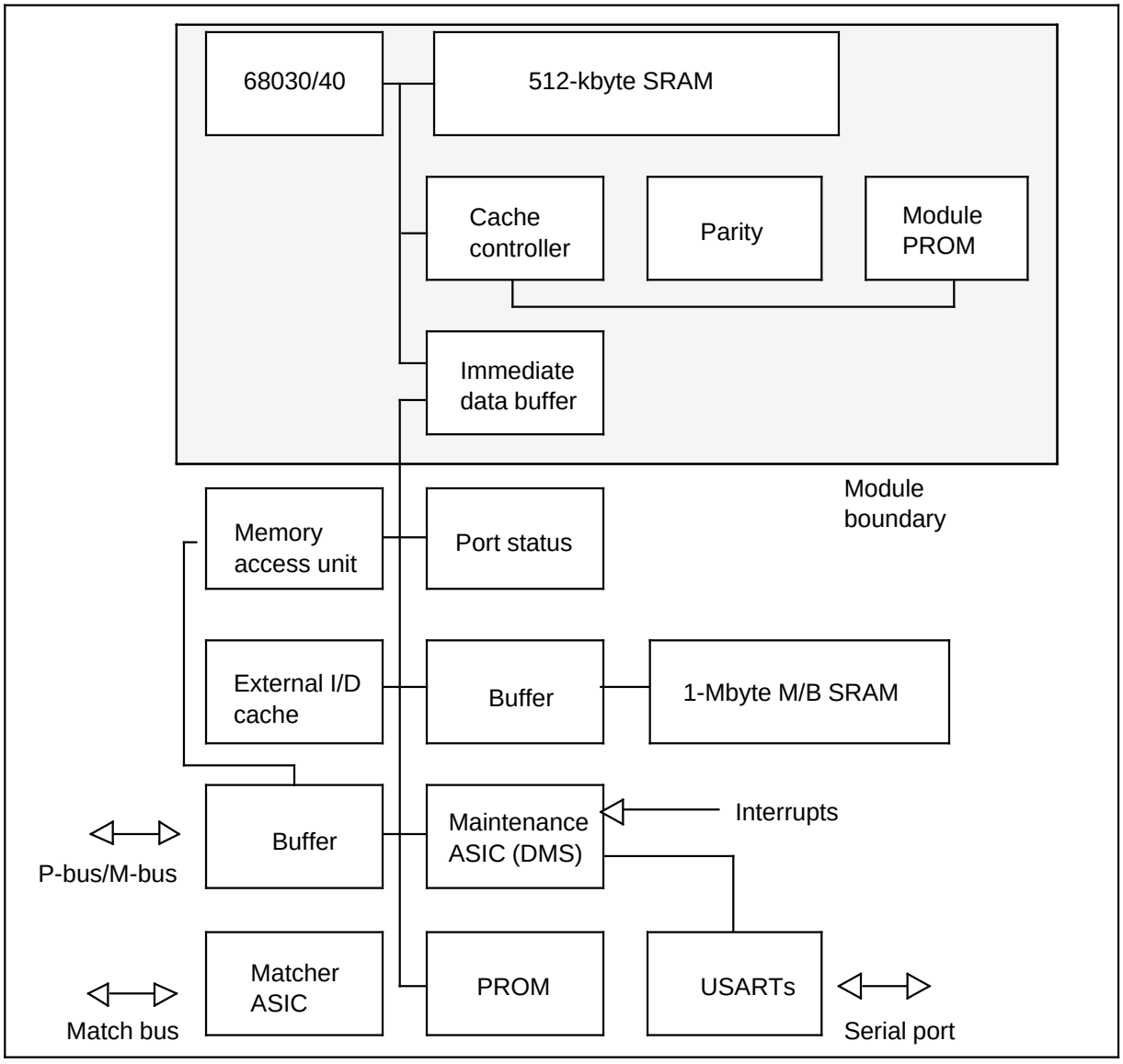
Functional blocks

The NT9X13HB contains the following functional blocks:

- high-performance module (HPM)
- motherboard control
- maintenance controller
- clock control
- memory access unit (MAU)
- system bus interface
- duplex support
- element identification (ID) PROM
- Z8530 serial communications controller (SCC)

The relationship between the functional blocks appears in the following figure.

NT9X13HB functional blocks



High-performance module

The HPM contains the following:

- 68030 processor
- cache controller
- module-motherboard interface
- motherboard memory

NT9X13HB (continued)

Motherboard control

The motherboard control has 17 programmable array logic (PAL) devices, P1 to P17:

- board address strobe (BPAS) (P1)
- motherboard static RAM (SRAM) control (P2)
- motherboard SRAM parity (P3)
- maintenance tape center (MTC) decode (P4)
- control register (P5)
- motherboard SRAM sequencer (P6)
- STA (P7)
- module interface (P8)
- element address decode (P9)
- (P10)
- clock (P11)
- address decode (P12)
- (P13)
- function code translation (P14)
- access protection (P15)
- (P16)
- initial program load (IPL) synchronization (P17)

Maintenance controller

The maintenance controller has DMS maintenance controller label, derived from the H04 maintenance gate array. The H04 maintenance gate array is in use on the NT9X13 series of CPUs.

The main functions of this chip are as follows:

- interrupt encoder and interrupt mismatch monitor
- interval and sanity timer
- serial maintenance port
- universal synchronous-asynchronous receiver-transmitter (USART) interface
- EPROM interface
- matcher interface

- activity control
- reset control circuits
- status indication registers
- address and data parity circuits
- clock source failure monitor

Clock control

The clock control performs the following functions:

- synchronizes the 20-MHz clocks on both planes so that they are in phase
- selects between the clock control and the mate clock to drive the processor card
- holds the 40-MHz clock in the high state when a controlled clock switch occurs
- minimizes the skew between the selected clocks on both planes and satisfies the 68030 clock requirements

Memory access unit

The MAU supports the following features:

- high-performance memory communication through a private synchronous memory bus (M-bus) interface protocol
- general purpose memory and peripheral interface through the processor bus (P-bus) bus specification
- bus parity checking
- CM handshaking support for duplex applications
- external caching
- address space access protection of the lower 256-Mbyte address range (in 64-kbyte blocks)

System bus interface

The system bus interface operates at 40 MHz. The system bus interface applies mainly to the CPU modules, the clocks, and the local motherboard memory array.

Both the higher performance synchronous M-bus and the general purpose P-bus interface are supported on the CPU card. The interface supports the current single-bit parity.

NT9X13HB (continued)

Duplex support

The NT9X13 HPM CPU card supports the current lock-step that matches plans with the DMS-core computing module.

Identification PROM

The NT9X13HB supports the DMS-core requirement of the ID PROM. This PROM contains the product engineering code (PEC) and vintage information to aid in system configuration. The CPU card is the intelligent entity on the DMS-core bus. The motherboard design restricts the access of the PROM to occur from the PROM. This restriction does not allow access from the backplane.

Zilog Z8530 SCC

The Zilog Z8530 is a nonmultiplexer bus SCC. The Zilog Z8530 has the following capabilities:

- two independent full-duplex channels
- independent programmable baud rate generators in each channel for synchronous/iso-synchronous data rates

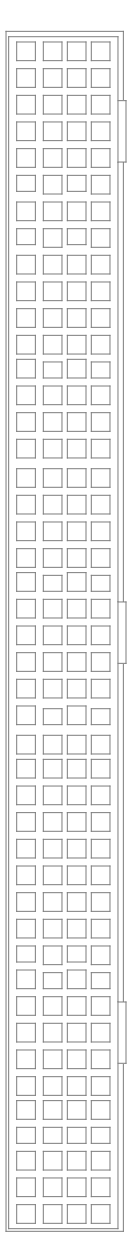
The Zilog Z8530 has the following asynchronous capabilities:

- 5, 6, 7, or 8 bits for each character
- 1, 1.5, or 2 stop bits
- odd or even parity
- X1, X16, X32, or X64 clock modes
- break generation and detection
- parity, overrun, and framing error detection

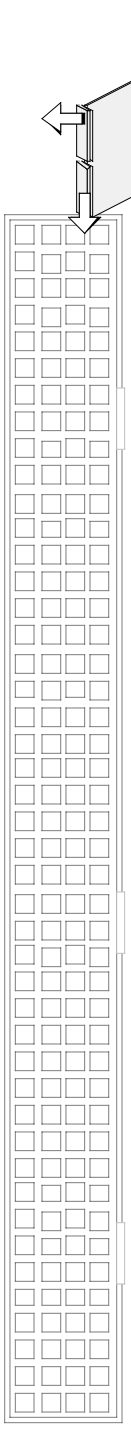
Pin numbers

The pin numbers for the NT9X13HB appear in the following table.

NT9X13HB pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	Gnd
2	OM22P	OM17P	OM00P	Gnd
3	IM23P	IM18P	IM01P	Gnd
4	OM23P	OM18P	OM01P	Gnd
5	IM24P	IM19P	IM02P	Gnd
6	OM24P	OM19P	OM02P	Gnd
7	IM25P	IM20P	IM03P	Gnd
8	OM25P	OM20P	OM03P	Gnd
9	IM26P	IM21P	IM04P	Gnd
10	OM26P	OM21P	OM04P	Gnd
11	IM27P	SYNC16-	IM05P	Gnd
12	OM27P	SYNC16-	OM05P	Gnd
13		DSON	IM06P	TXDA
14		DSIN	OM06P	TRXCA
15	CPUN+		IM07P	HINTN
16		Gnd	OM08P	RTSA
17	PERINT6	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-	OM08P	RXDA
19	BUSREQ-	PERINT2-	IM09P	SYNCA
20	DS-	PERINT3-	OM09P	DTR-REQA
21		PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-	OM10P	TXDB
23	RSTOUT-	BUSLOCK-	IM11P	TRXCB
24	PERINT1-	PERINT0-	OM11P	
25	BEN1-	BENO-	IM12P	RTSB
26	BEN3-	BEN2-	OM12P	DCDB
27	Gnd	DAS-	IM13P	RXDB
28	WRT-	Gnd	OM14P	SYNCB
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-	OM14P	
31	PRTYEN-	MEMERR-	IM15P	
32	FAS-	Gnd	OM15P	SH0
33	DAS32-	CPUCLK+	IM16P	SH1
34	DATA00	EDAS-	OM16P	
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW3	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	Gnd
41	DATA07	ADDR07		Gnd
42	DATA08	ADDR08	CMSYNC	Gnd
43	DATA09	ADDR09		Gnd
44	DATA10	ADDR10	PBRST-	+5V
45	DATA11	ADDR11	PERR-	+5V



	D	C	B	A
46	DATA12	ADDR12	DISABSAN	5 V
47	DATA13	ADDR13	Gnd	5 V
48	DATA14	ADDR14	FACKN	5 V
49	DATA15	ADDR15	ENOMN	5 V
50	DATA16	ADDR16		5 V
51	DATA17	ADDR17		5 V
52	DATA18	ADDR18		5 V
53	DATA19	ADDR19		5 V
54	DATA20	ADDR20		5 V
55	DATA21	ADDR21	Gnd	5 V
56	DATA22	ADDR22	Gnd	
57	DATA23	ADDR23	Gnd	
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27	Gnd	Gnd
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		Gnd
66		FC0+		Gnd
67		FC1+		
68		FC2+		
69				
70				Gnd
71	RSTIN	IM28P		Gnd
72	RSTON	OM28P		
73	CLPIN	IM29P		
74	CLKOP	OM29P		
75	IMCRN	IM30P		Gnd
76	OMCRN	OM30P		
77	IMCWN	IM31P		
78	OMCWN	OM31P		
79			DTR-REQB	Gnd
80	OMMN		CTSB	Gnd
81	ACTIN	MSCCN		Gnd
82	ACTON	OSCCN		Gnd
83	OFFIN	IPR0N		Gnd
84	OFFON	OPR0N		Gnd
85	IFCRN	IPR1N	NMIN	Gnd
86	OFRCN	OPR1N	CKFLN	Gnd
87	IFRLN	IPR2N	HEXDN	Gnd
88	OFRLN	OPR2N	JAMIN	Gnd
89	IFRDP	IPR3N	EBENN7	Gnd
90	OFRDP	OPR3N	LED1	Gnd

NT9X13HB (end)

Technical data

Electrical requirements

The power requirements for the NT9X13HB appear in the following table.

NT9X13HB power requirements

NT9X13HB part	+5V supply current (mA)
40-MHz CPU module	2200
motherboard ASICs	120
serial controller	72
local static RAM	1060
EPROM	20
external cache	450
PALs	2160
discrete logic	510
MSI buffers	1570
passive networks	500
total	8.57 A

Product description

The NT9X13KA DMS SuperNode processor card is a high-performance microcomputer card based on the Motorola MC68020 32-bit microprocessor. The special purpose application in the enhanced network (ENET) requires the NT9X13KA.

The NT9X13KA has the following features:

- 20-MHz MC68020 CPU
- memory access protection
- 16-kbyte data cache
- dual-channel serial communications controller (SCC)
- 16-Mbyte dynamic RAM (DRAM) with error correction code (ECC)
- processor bus (P-bus) compatibility
- 256 kbytes of EPROM
- element identification (ID) PROM
- timers
- interrupts
- status and control registers
- fault indication registers (FIR)

Functional description

Functional blocks

The NT9X13KA contains the following functional blocks:

- MC68020 CPU
- memory address unit (MAU)
- error correction and burst memory controller (EBM)
- DMS maintenance controller (DMC)
- matcher (MCH)
- SCC

MC68020 CPU

The 20-MHz MC68020 CPU is the main processing machine of the NT9X13KA. The MC68020 CPU provides performance enhancement over the previous MC68000 CPUs.

NT9X13KA (continued)

Memory access unit

The MAU performs the following functions:

- controls a data cache
- provides address space access protection in 64-kbyte blocks
- implements a parity protection design on bus accesses and the data cache
- supplies the necessary control signals for the extended multiprocessor system (XMS) P-bus specification and the SuperNode CPU/MEM bus specification

Error correction and burst memory controller

The EBM corrects single-bit data errors and detects double-bit or multiple-bit errors.

DMS maintenance controller

The DMC interfaces directly with the 68020 CPU to provide the processor with basic signals. These basic signals include clock, reset, and chip selects to the associated EPROM and other peripherals. The DMC incorporates a programmable interval timer and a sanity timer. Interrupts from the different sources latch, encode, and pass to the processor at a fixed priority. The DMC provides the interface to the SCC for remote terminal interface (RTIF) communications. The MTC provides clock detection and selection. The MTC provides a serial FIR to obtain information about the mate system clock and control signals. The requesting CPU obtains information from an inoperative mate.

Matcher

The MCH provides an address hold register function during error conditions.

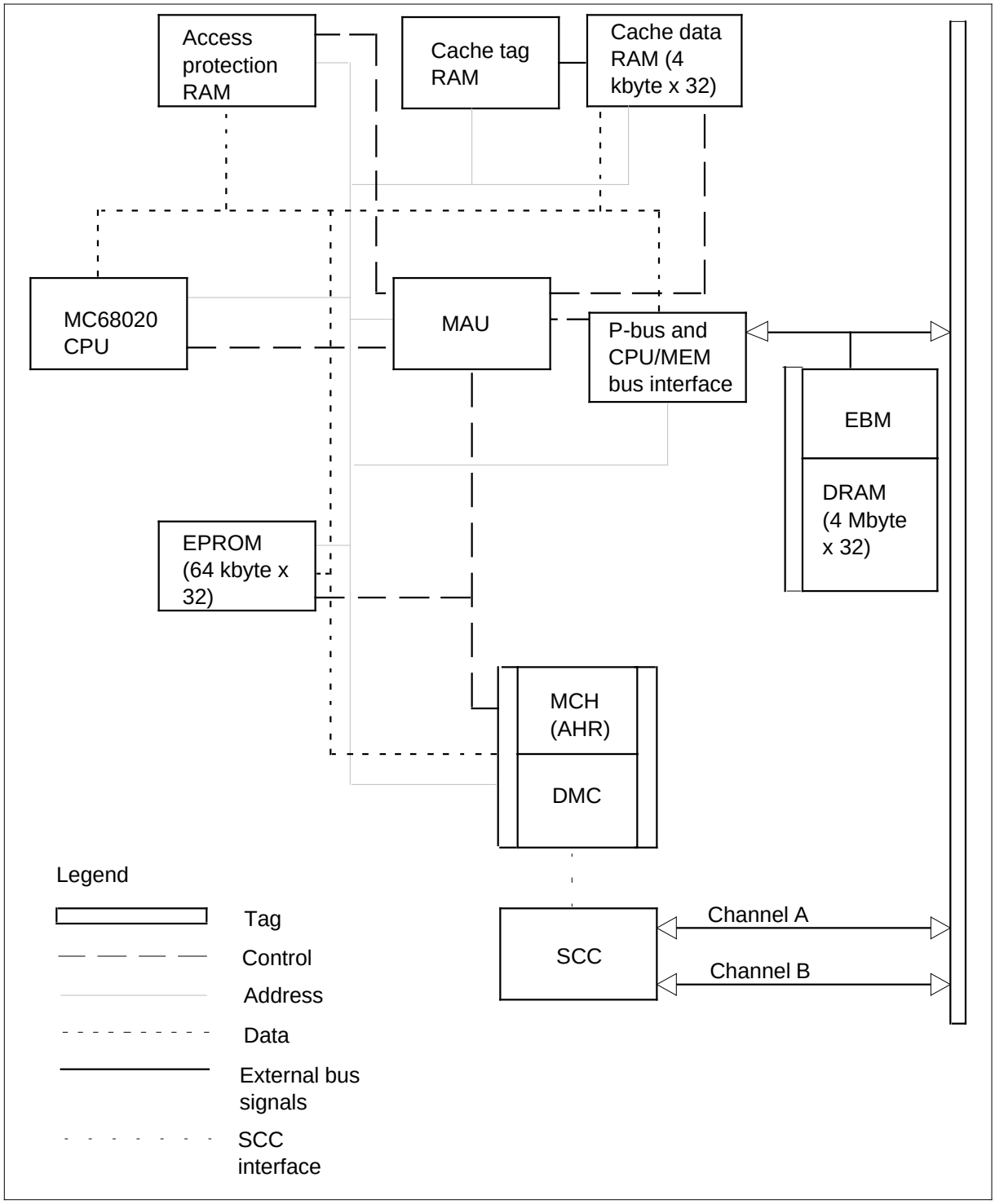
Serial communications controller

The Zilog Z8530 is a non-mutliplexed bus SCC with the following features:

- two independent full-duplex channels
- independent programmable baud-rate generators in each channel for synchronous/iso-synchronous data rates
- asynchronous capabilities
- byte-oriented synchronous capabilities
- synchronous data link control (SDLC) and high-level data link control (HDLC) capabilities

The operating relationship between the blocks appears in the following figure.

NT9X13KA functional blocks



NT9X13KA (continued)

Signaling

Pin numbers

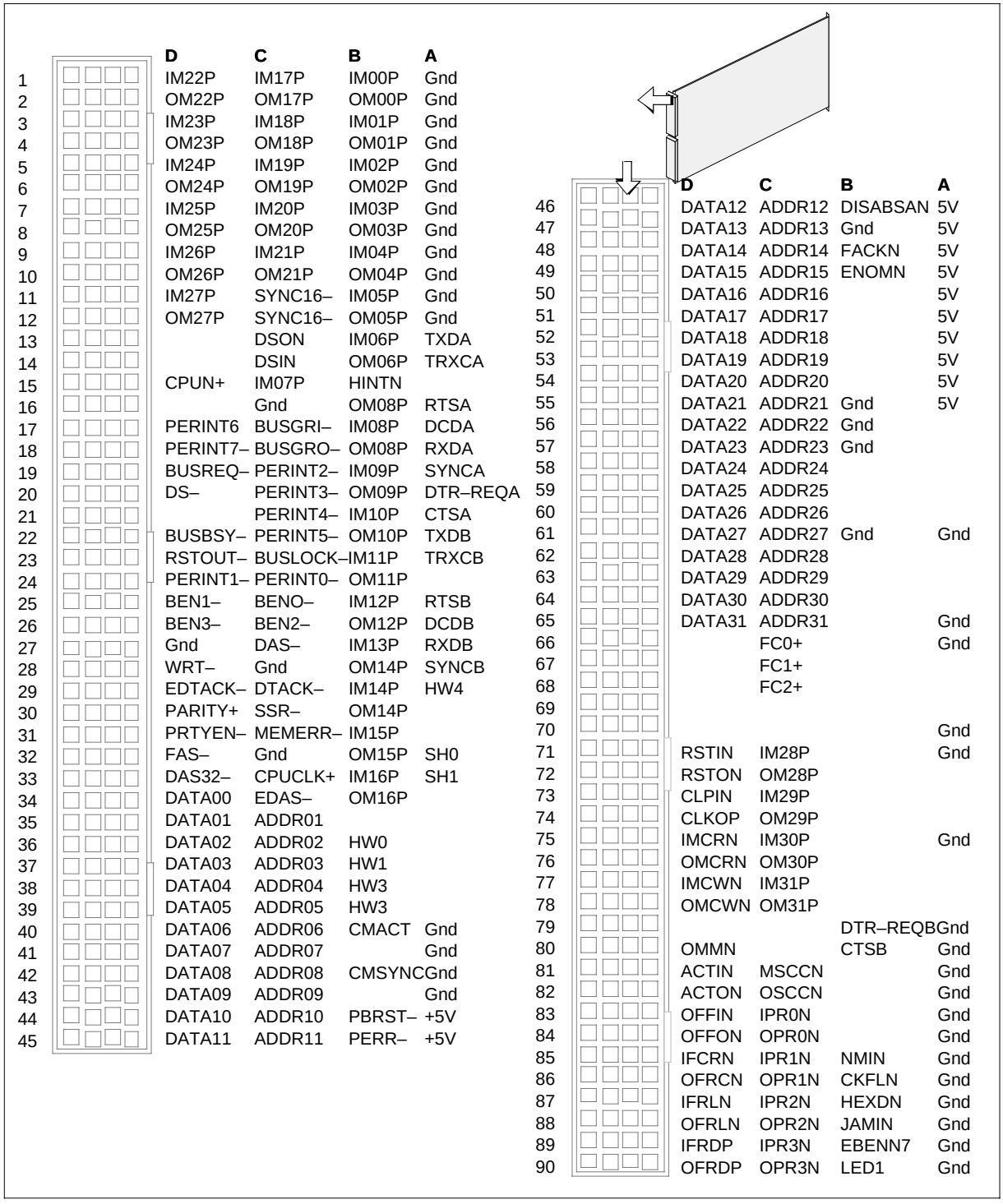
The pin numbers for the NT9X13KA appear in the following figure.

Technical data

Power requirements

The NT9X13KA requires +5 V ±5%.

NT9X13KA pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	Gnd
2	OM22P	OM17P	OM00P	Gnd
3	IM23P	IM18P	IM01P	Gnd
4	OM23P	OM18P	OM01P	Gnd
5	IM24P	IM19P	IM02P	Gnd
6	OM24P	OM19P	OM02P	Gnd
7	IM25P	IM20P	IM03P	Gnd
8	OM25P	OM20P	OM03P	Gnd
9	IM26P	IM21P	IM04P	Gnd
10	OM26P	OM21P	OM04P	Gnd
11	IM27P	SYNC16–	IM05P	Gnd
12	OM27P	SYNC16–	OM05P	Gnd
13		DSON	IM06P	TXDA
14		DSIN	OM06P	TRXCA
15	CPUN+	IM07P	HINTN	
16		Gnd	OM08P	RTSA
17	PERINT6	BUSGRI–	IM08P	DCDA
18	PERINT7–	BUSGRO–	OM08P	RXDA
19	BUSREQ–	PERINT2–	IM09P	SYNCA
20	DS–	PERINT3–	OM09P	DTR–REQA
21		PERINT4–	IM10P	CTSA
22	BUSBSY–	PERINT5–	OM10P	TXDB
23	RSTOUT–	BUSLOCK–	IM11P	TRXCB
24	PERINT1–	PERINT0–	OM11P	
25	BEN1–	BENO–	IM12P	RTSB
26	BEN3–	BEN2–	OM12P	DCDB
27	Gnd	DAS–	IM13P	RXDB
28	WRT–	Gnd	OM14P	SYNCB
29	EDTACK–	DTACK–	IM14P	HW4
30	PARITY+	SSR–	OM14P	
31	PRTYEN–	MEMERR–	IM15P	
32	FAS–	Gnd	OM15P	SH0
33	DAS32–	CPUCLK+	IM16P	SH1
34	DATA00	EDAS–	OM16P	
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW3	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	Gnd
41	DATA07	ADDR07		Gnd
42	DATA08	ADDR08	CMSYNC	Gnd
43	DATA09	ADDR09		Gnd
44	DATA10	ADDR10	PBRST–	+5V
45	DATA11	ADDR11	PERR–	+5V

	D	C	B	A
46	DATA12	ADDR12	DISABSAN	5V
47	DATA13	ADDR13	Gnd	5V
48	DATA14	ADDR14	FACKN	5V
49	DATA15	ADDR15	ENOMN	5V
50	DATA16	ADDR16		5V
51	DATA17	ADDR17		5V
52	DATA18	ADDR18		5V
53	DATA19	ADDR19		5V
54	DATA20	ADDR20		5V
55	DATA21	ADDR21	Gnd	5V
56	DATA22	ADDR22	Gnd	
57	DATA23	ADDR23	Gnd	
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27	Gnd	Gnd
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		Gnd
66		FC0+		Gnd
67		FC1+		
68		FC2+		
69				
70				Gnd
71	RSTIN	IM28P		Gnd
72	RSTON	OM28P		
73	CLPIN	IM29P		
74	CLKOP	OM29P		
75	IMCRN	IM30P		Gnd
76	OMCRN	OM30P		
77	IMCWN	IM31P		
78	OMCWN	OM31P		
79			DTR–REQB	Gnd
80	OMMN		CTSB	Gnd
81	ACTIN	MSCCN		Gnd
82	ACTON	OSCCN		Gnd
83	OFFIN	IPR0N		Gnd
84	OFFON	OPR0N		Gnd
85	IFCRN	IPR1N	NMIN	Gnd
86	OFRCN	OPR1N	CKFLN	Gnd
87	IFRLN	IPR2N	HEXDN	Gnd
88	OFRLN	OPR2N	JAMIN	Gnd
89	IFRDP	IPR3N	EBENN7	Gnd
90	OFRDP	OPR3N	LED1	Gnd

NT9X13LA

Product description

The NT9X13LA provides the processing capability for the application processor (AP) or the file processor (FP). The 68030 CPU on the card provides the capability to run foreign (not switch) operating systems.

Compatibility

The NT9X13LA can use only software loads of BCS33 and higher.

The CPU card does not operate in synchronization with any CPU card except another .

Functional description

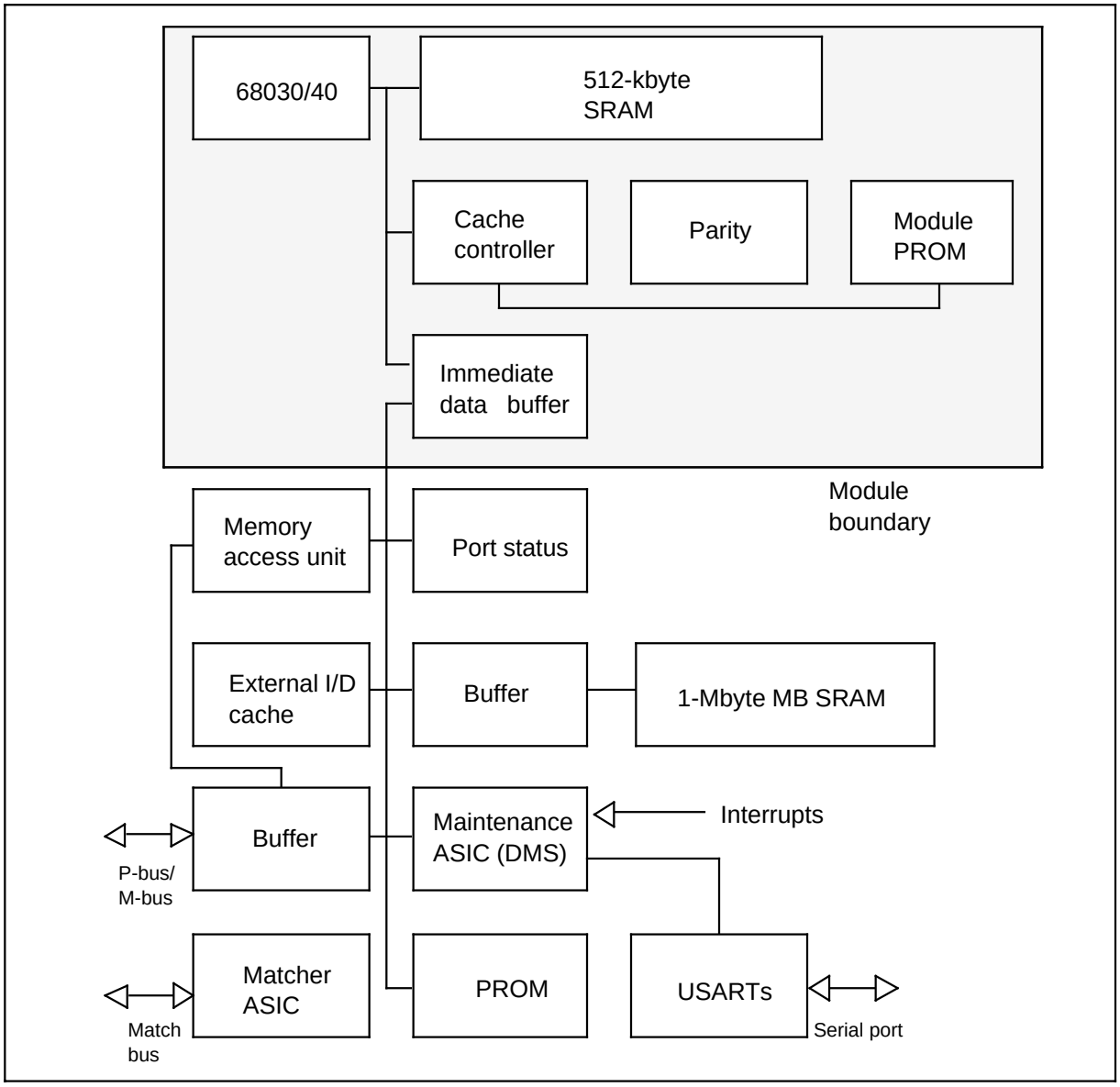
Functional blocks

The NT9X13LA contains the following functional blocks:

- high-performance module (HPM)
- motherboard (MB) control
- maintenance controller
- clock control
- memory access unit (MAU)
- system bus interface
- duplex support
- Z8530 serial communications controller (SCC)
- identification (ID) PROM

The relationship between the functional blocks appears in the following table.

NT9X13LA functional blocks



High-performance module

The HPM contains the following items:

- 68030 processor
- cache controller
- module-to-MB interface
- MB memory

NT9X13LA (continued)

Motherboard control

The MB control has 17 programmable array logic (PAL) devices, P1 to P17:

- board address strobe (BPAS) (P1)
- MB static RAM (SRAM) control (P2)
- MB SRAM parity (P3)
- maintenance, timing, and control (MTC) decode (P4)
- control register (P5)
- MB SRAM sequencer (P6)
- STA (P7)
- module interface (P8)
- element address decode (P9)
- P10
- clock (P11)
- address decode (P12)
- P13
- function code translation (P14)
- access protection (P15)
- P16
- initial program load (IPL) synchronization (P17)

Maintenance controller

The DMS maintenance controller is derived closely from the H04 maintenance gate array in the NT9X13 series of CPUs.

The main functions of the maintenance controller are:

- interrupt encoder and interrupt mismatch monitor
- interval and sanity timer
- serial maintenance port
- universal synchronous/asynchronous receiver/transmitter (USART) interface
- EPROM interface
- matcher interface
- activity control

- reset control circuits
- status indication registers
- address and data parity circuits
- clock source failure monitor

Clock control

The clock control performs the following functions:

- synchronizes the 20-MHz clocks on both planes so that the clocks are in phase
- selects the control clock or the mate clock to drive the processor card
- holds the 40-MHz clock in the high state when a controlled clock switch occurs
- minimizes the skew between the selected clocks on both planes and satisfies the 68030 clock requirements

Memory access unit

The MAU supports the following features:

- high-performance memory communication through a private synchronous memory bus (M-bus) interface protocol
- a general purpose memory and peripheral interface through the processor bus (P-bus) specification
- bus parity checking
- mate CM handshaking support for duplex applications
- external caching
- address space access protection of the lower 256-Mbyte address range (in 64-kbyte blocks)

System bus interface

The system bus interface operates at 40 MHz. The system bus interface applies to the CPU modules, the clocks, and the local MB memory array.

The CPU card supports the higher performance synchronous M-bus interface and the general purpose P-bus interface. The interface supports the current single-0 bit parity.

NT9X13LA (continued)

Duplex support

The NT9X13 HPM CPU card supports the current lock-step matching (duplex) mode. This current mode is identical to the mode in the DMS-core computing module.

Zilog Z8530 serial communications controller

The Zilog Z8530 is a non-multiplexed bus serial communications controller (SCC). The Zilog Z8530 has the following capabilities:

- two independent full-duplex channels
- independent programmable baud-rate generators in each channel for synchronous and iso-synchronous data rates

The Zilog Z8530 has the following asynchronous capabilities:

- 5, 6, 7, or 8 bits for each character
- 1, 1.5, or 2 stop bits
- odd or even parity
- X1, X16, X32, or X64 clock modes
- break generation and detection
- parity, overrun, and framing error detection

Identification PROM

The supports the DMS-core requirement of the ID PROM. The ID PROM contains the PEC and vintage information to aid in system configuration. The CPU card is the only intelligent entity on the AP bus and on the FP bus. The MB design allows the ID PROM to access from the IDPROM and not from the backplane.

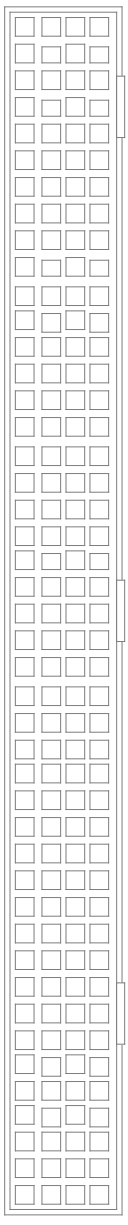
Signaling

Pin numbers

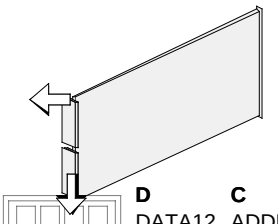
The pin numbers for the NT9X13LA appear in the following figure.

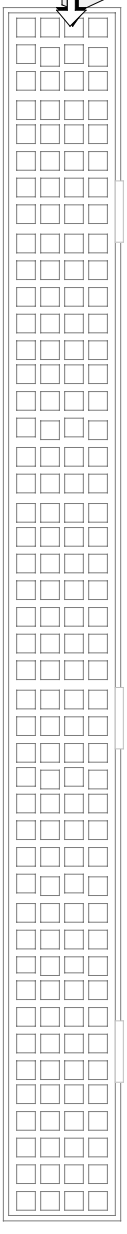
NT9X13LA (continued)

NT9X13LA pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	Gnd
2	OM22P	OM17P	OM00P	Gnd
3	IM23P	IM18P	IM01P	Gnd
4	OM23P	OM18P	OM01P	Gnd
5	IM24P	IM19P	IM02P	Gnd
6	OM24P	OM19P	OM02P	Gnd
7	IM25P	IM20P	IM03P	Gnd
8	OM25P	OM20P	OM03P	Gnd
9	IM26P	IM21P	IM04P	Gnd
10	OM26P	OM21P	OM04P	Gnd
11	IM27P	SYNC16-	IM05P	Gnd
12	OM27P	SYNC16-	OM05P	Gnd
13		DSON	IM06P	TXDA
14		DSIN	OM06P	TRXCA
15	CPUN+		IM07P	HINTN
16		Gnd	OM08P	RTSA
17	PERINT6	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-	OM08P	RXDA
19	BUSREQ-	PERINT2-	IM09P	SYNCA
20	DS-	PERINT3-	OM09P	DTR-REQA
21		PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-	OM10P	TXDB
23	RSTOUT-	BUSLOCK-	IM11P	TRXCB
24	PERINT1-	PERINT0-	OM11P	
25	BEN1-	BENO-	IM12P	RTSB
26	BEN3-	BEN2-	OM12P	DCDB
27	Gnd	DAS-	IM13P	RXDB
28	WRT-	Gnd	OM14P	SYNCB
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-	OM14P	
31	PRTYEN-	MEMERR-	IM15P	
32	FAS-	Gnd	OM15P	SH0
33	DAS32-	CPUCLK+	IM16P	SH1
34	DATA00	EDAS-	OM16P	
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW3	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	Gnd
41	DATA07	ADDR07		Gnd
42	DATA08	ADDR08	CMSYNC	Gnd
43	DATA09	ADDR09		Gnd
44	DATA10	ADDR10	PBRST-	+5V
45	DATA11	ADDR11	PERR-	+5V





	D	C	B	A
46	DATA12	ADDR12	DISABSAN	5V
47	DATA13	ADDR13	Gnd	5V
48	DATA14	ADDR14	FACKN	5V
49	DATA15	ADDR15	ENOMN	5V
50	DATA16	ADDR16		5V
51	DATA17	ADDR17		5V
52	DATA18	ADDR18		5V
53	DATA19	ADDR19		5V
54	DATA20	ADDR20		5V
55	DATA21	ADDR21	Gnd	5V
56	DATA22	ADDR22	Gnd	
57	DATA23	ADDR23	Gnd	
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27	Gnd	Gnd
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		Gnd
66		FC0+		Gnd
67		FC1+		
68		FC2+		
69				
70				Gnd
71	RSTIN	IM28P		Gnd
72	RSTON	OM28P		
73	CLPIN	IM29P		
74	CLKOP	OM29P		
75	IMCRN	IM30P		Gnd
76	OMCRN	OM30P		
77	IMCWN	IM31P		
78	OMCWN	OM31P		
79			DTR-REQB	Gnd
80	OMMN		CTSB	Gnd
81	ACTIN	MSCCN		Gnd
82	ACTON	OSCCN		Gnd
83	OFFIN	IPR0N		Gnd
84	OFFON	OPR0N		Gnd
85	IFCRN	IPR1N	NMIN	Gnd
86	OFRCN	OPR1N	CKFLN	Gnd
87	IFRLN	IPR2N	HEXDN	Gnd
88	OFRLN	OPR2N	JAMIN	Gnd
89	IFRDP	IPR3N	EBENN7	Gnd
90	OFRDP	OPR3N	LED1	Gnd

NT9X13LA (end)

Technical data

Power requirements

The power requirements for the appear NT9X13LA in the following table.

NT9X13LA power requirements

NT9X13LA part	+5V supply current (mA)
40-MHz CPU module	2200
MB ASICs	120
serial controller	72
local SRAM	1060
EPROM	20
external cache	450
PALs	2160
discrete logic	510
MSI buffers	1570
passive networks	500
total	8.57 A

NT9X13MA

Product description

The NT9X13MA SuperNode SE core computing module (CM) card is a high-performance microcomputer board based on a 68020 32-bit microprocessor. The is a recycled board based on the NT9X13BC.

The NT9X13MA is like the NT9X13BA, but the NT9X13MA uses the E87 version of the 68020 microprocessor. The NT9X13MA does not use the A70 and the H42 version of the memory access unit (MAU). The DMS SuperNode SE application uses the NT9X13MA.

The NT9X13MA replaces the H04 maintenance, timing, and control (MTC) maintenance gate array with the H85 DMC DMS maintenance controller gate array. The has 1-Gbyte access protection, while the NT9X13BC has only 256-Mbyte access protection.

The NT9X13MA has the following features:

- 20-MHz 68020 CPU
- 1-Gbyte memory access protection and write protection
- 4-kbyte data cache
- dual-channel serial communications controller (SCC)
- 256-kbyte static RAM (SRAM) with parity
- processor bus (P-bus) compatibility
- 128-kbyte EPROM
- element identification PROM (ID PROM)
- synchronous and matching modes
- timers
- interrupts
- status and control registers
- fault indication registers

Location

The NT9X13MA circuit pack fits in slots 19 and 20 on a SuperNode SE CM shelf.

NT9X13MA (continued)

Functional description

Functional blocks

The NT9X13MA has the following functional blocks:

- 68020 CPU
- MAU
- memory controller (MEM) and memory array
- MTC
- matcher (MCH)

The relationship in the functional blocks appears in the following figure.

68020 CPU

The 20-MHz 68020 CPU provides a large amount of performance enhancement over the previous 680XX CPUs. The 68020 CPU has the following:

- 32-bit registers
- data paths
- 32-bit addresses
- strong instruction set
- versatile addressing modes

The 68020 is compatible with earlier versions in the 68000 series, and has the following components:

- new addressing modes to support high-level languages
- an in-chip instruction cache
- a flexible coprocessor interface with full IEEE floating-point support (the 68881)

Memory access unit

The MAU block has the following functions:

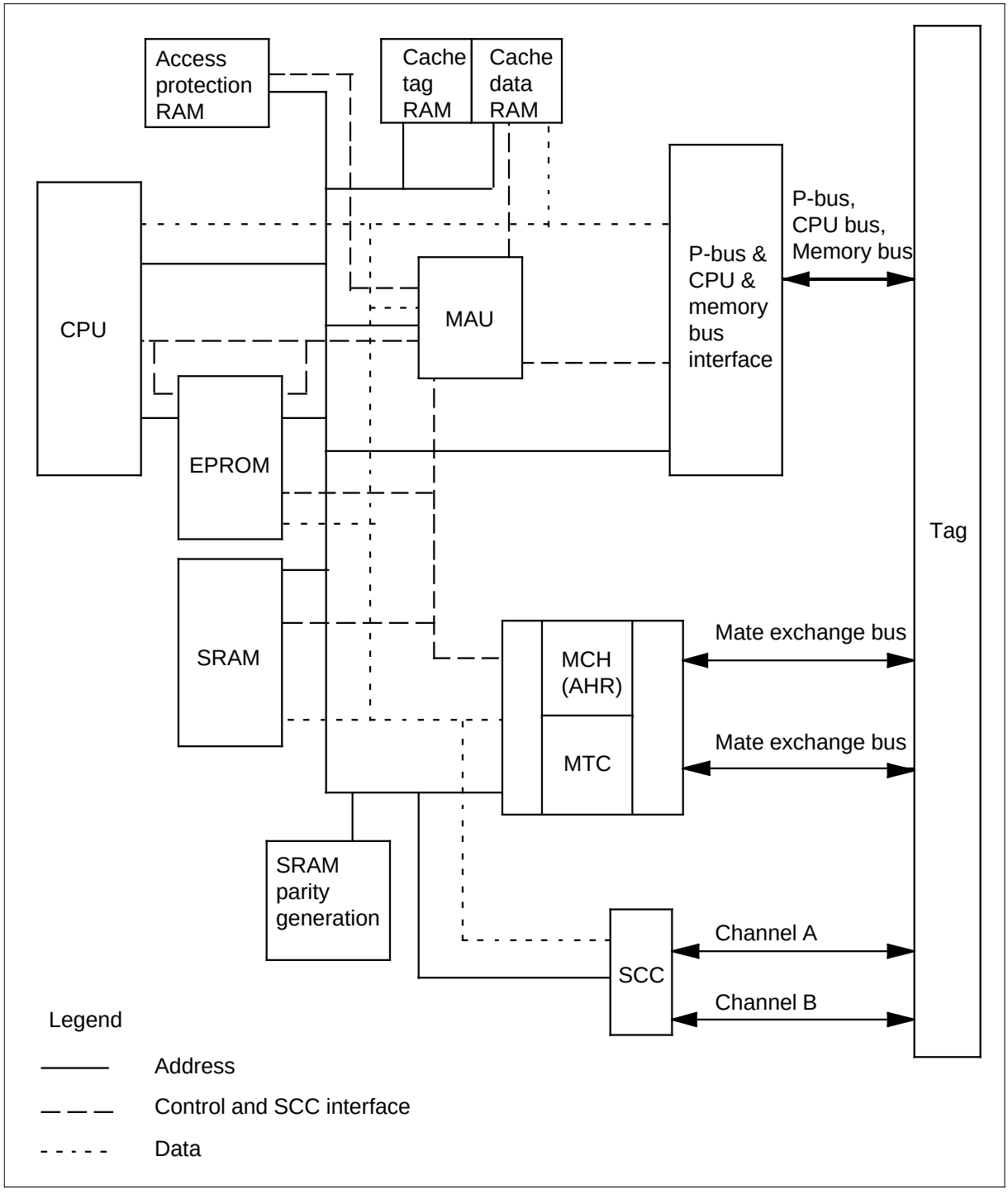
- controls a data cache
- provides address space access protection in 64-kbyte blocks
- implements a parity protection design on bus accesses and the data cache
- supplies the necessary control signals for the extended multiprocessor system (XMS) P-bus specification and the enhanced CORE (ECORE) CM/MEM memory bus specification

Memory controller and memory array

The memory controller can correct single-bit data errors and detect double-bit errors.

NT9X13MA (continued)

NT9X13MA functional blocks



Maintenance, timing, and control

The MTC connects to the 68020 CPU. The MTC provides the CPU with clock and reset signals, and chip selects to the associated EPROM and other peripherals. The MTC incorporates a sanity timer and an interval timer. A fixed priority allows interrupts from different sources to latch, encode, and pass to the processor. The MTC provides the interface to the SCC for remote terminal interface (RTIF) communications. In duplex operation, the MTC provides clock detection and selection. The MTC provides a serial fault indication register (FIR) to obtain information about the mate system clock and control signals. The requesting CPU can retrieve information from an inoperative mate.

Matcher

The MCH performs the following functions:

- compares addresses and data on the 68020 CPU bus cycles against the address of the mate CPU and data to provide mismatch error detection
- multiplexes bus cycle addresses and data to the outgoing match bus to allow the mate MCH to perform the same match check
- passes the incoming match bus from the mate MCH to the data bus
- maintains a hardware lock on the address hold register and releases the lock after the fault is acknowledged
- provides a 32-bit maintenance control register that the data bus can write to and the mate CPU can read from

Signaling

Pin numbers

The pin numbers for the NT9X13MA appear in the following figure.

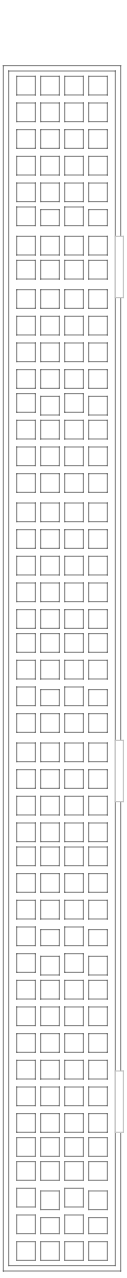
Technical data

Power requirements

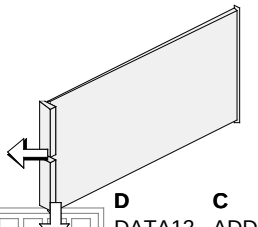
The requires +5 V, ±5 %.

NT9X13MA (end)

NT9X13MA pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2	OM22P	OM17P	OM00P	GND
3	IM23P	IM18P	IM01P	GND
4	OM23P	OM18P	OM01P	GND
5	IM24P	IM19P	IM02P	GND
6	OM24P	OM19P	OM02P	GND
7	IM25P	IM20P	IM03P	GND
8	OM25P	OM20P	OM03P	GND
9	IM26P	IM21P	IM04P	GND
10	OM26P	OM21P	OM04P	SPGND
11	IM27P	ADSO	IM05P	SPGND
12	OM27P	ADSI	OM05P	SPGND
13		DSON	IM06P	TXDA
14		DSIN	OM06P	TRXCA
15	CPUN+		IM07P	HINTN
16		GND	OM08P	RTSA
17	PERINT6-	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-	OM08P	RXDA
19	BUSREQ-	PERINT2-	IM09P	SYNCA
20	DS-	PERINT3-	OM09P	DTR-REQA
21		PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-	OM10P	TXDB
23	RSTOUT-	BUSLOCK-	IM11P	TRXCB
24	PERINT1-	PERINT0-	OM11P	
25	BEN1-	BEN0-	IM12P	RTSB
26	BEN3-	BEN2-	OM12P	DCDB
27	GND	DAS-	IM13P	RXDB
28	WRT-	GND	OM13P	SYNCB
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-	OM14P	
31	PRTYEN-	MEMERR-	IM15P	SH0
32	FAS-	GND	OM15P	SH1
33	DAS32-	CPUCLK+	IM16P	
34	DATA00	EDAS-	OM16P	
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10	PBRST-	SP+5V
45	DATA11	ADDR11	PERR-	SP+5V



	D	C	B	A
46	DATA12	ADDR12	DISABSAN-	+5V
47	DATA13	ADDR13	GND	+5V
48	DATA14	ADDR14	FACKN	+5V
49	DATA15	ADDR15	ENOMN	+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21	GND	+5V
56	DATA22	ADDR22	GND	
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27	GND	GND
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		GND
66		FC0+		GND
67		FC1+		
68		FC2+		
69				
70				GND
71	RSTIN	IM28P		GND
72	RSTON	OM28P		
73	CLPIN	IM29P		
74	CLKOP	OM29P		
75	IMCRN	IM30P		GND
76	OMCRN	OM30P		
77	IMCWN	IM31P		
78	OMCWN	OM31P		
79			DTR-REQB	SPGND
80	OMMN		CTSB	SPGND
81	ACTIN	MSCCN		SPGND
82	ACTON	OSCCN		GND
83	OFFIN	IPR0N		GND
84	OFFON	OPR0N		GND
85	IFRCN	IPR1N	NMIN	GND
86	OFRCN	OPR1N	CKFLN	GND
87	IFRLN	IPR2N	HEXDN	GND
88	OFRLN	OPR2N	JAMIN	GND
89	IFRDP	IPR3N	EBENN7	GND
90	OFRDP	OPR3N	LED1	GND

NT9X13MB

Product description

The NT9X13MB SuperNode SE core computing module (CM) card is a high-performance microcomputer board. The NT913MB card is based on a 68020 32-bit microprocessor. The is a recycled board based on the NT9X13BC.

The NT9X13MB is like the NT9X13BA. The NT9X13MB uses the E87 version of the 68020 microprocessor instead of the A70. The NT9X13MB also uses the H42 version of the memory access unit (MAU). Applications like DMS SuperNode SE use the card.

The NT9X13MB replaces the H04 maintenance, timing and control (MTC) maintenance gate array with the H85 DMC DMS maintenance controller gate array. The also includes 1-Gbyte access protection. The NT9X13BC includes only 256-Mbyte access protection. The larger capacity of 1 Gbyte allows the to support the NT9X14EA 96-Mbyte memory board.

The NT9X13MB includes the following features:

- a 20-MHz 68020 central processing unit (CPU)
- a 1-Gbyte memory access protection and write protection
- a 4-kbyte data cache
- two-channel serial communications controller (SCC)
- a 256-kbyte static random access memory (RAM) (S-RAM) with parity
- processor bus (P-bus) compatibility
- a 128-kbyte erasable programmable read-only memory (EPROM)
- element identification PROM (ID PROM)
- synchronous and matching modes
- timers
- interrupts
- status and control registers
- fault indication registers

Location

The NT9X13MB circuit pack fits in slots 19 and 20 on a SuperNode SE CM shelf.

NT9X13MB (continued)

Functional description

Functional blocks

The NT9X13MB includes the following functional blocks:

- a 68020 CPU
- memory access unit (MAU)
- an MTC
- matcher (MCH)

The relationship between the functional blocks appears in the following diagram.

The 68020 CPU

The 20-MHz 68020 CPU enhances performance of the previous 680XX CPUs. The 68020 CPU includes the following:

- the 32-bit registers and data paths
- the 32-bit addresses
- a strong instruction set
- flexible addressing modes
- new addressing modes to support high-level languages
- an in-chip instruction cache
- a flexible co-processor interface with full IEEE floating-point support, the 68881

The 68020 CPU is compatible with earlier versions in the 68000 series.

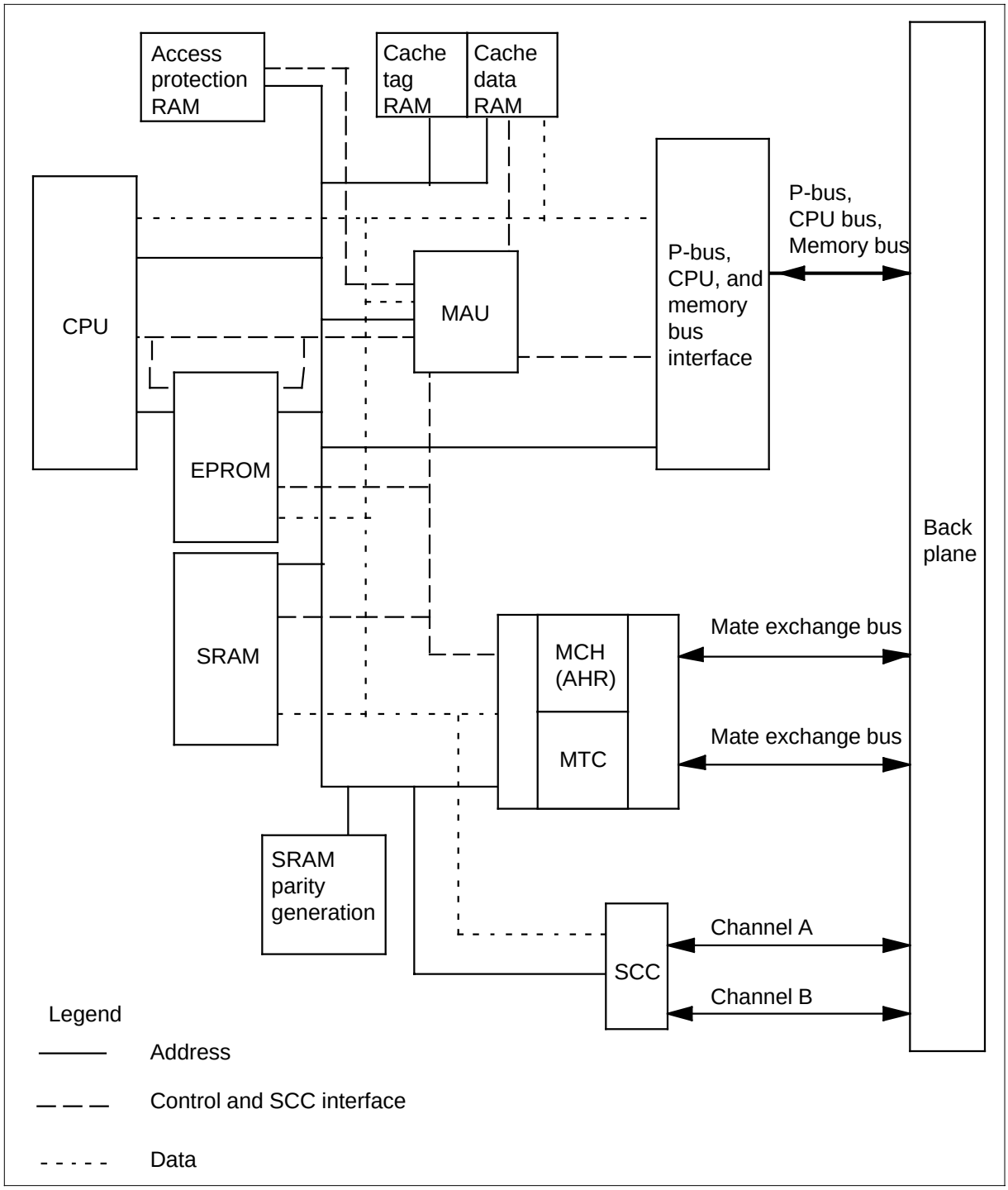
Memory access unit

The memory access unit (MAU) block has the following functions:

- control of a data cache
- protection of address space access in 64-kbyte blocks
- implementation of parity protection design on bus accesses and the data cache
- the necessary control signals for the P-bus specification of the extended multiprocessor system (XMS)

the necessary control signals for the enhanced CORE (ECORE) CM/MEM memory bus specification

The NT9X13MB functional blocks



NT9X13MB (continued)

Maintenance, timing and control

The MTC connects to the 68020 CPU. The MTU provides the CPU with the following:

- clock signals
- reset signals
- chip selects to the associated EPROM and other peripherals

The MTC includes a sanity timer and an interval timer. The system latches, codes, and passes interrupts from different sources to the processor by a fixed priority.

The MTC provides the following:

- the interface to the SCC for remote terminal interface (RTIF) communications
- clock detection and selection during duplex operation
- a serial fault indication register (FIR)

The FIR allows the MTC to obtain information about the mate system clock and control signals. The information allows a CPU to retrieve information from a CPU mate that does not operate.

Matcher

The matcher (MCH) performs the following functions:

- comparison of addresses and data between the bus cycles of the 68020 CPU and the CPU mate to detect mismatch errors
- multiplexing of addresses of bus cycles and data to the match bus that is outgoing. This process allows the mate MCH to perform the same match check
- pass of incoming match bus from the mate MCH to the data bus
- maintenance of hardware lock on the address hold register and release of lock after the fault acknowledgement
- a 32-bit maintenance control register to which the data bus can write and from which the mate CPU can read

Signaling

Pin numbers

The pin numbers for the NT9X13MB appear in the following figure.

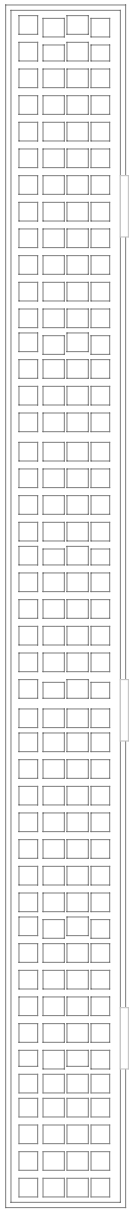
Technical data

Power requirements

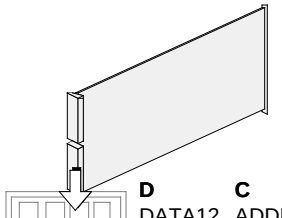
The NT9X13MB requires +5V ±5%.

NT9X13MB (end)

The NT9X13MB pin numbers



	D	C	B	A
1	IM22P	IM17P	IM00P	GND
2	OM22P	OM17P	OM00P	GND
3	IM23P	IM18P	IM01P	GND
4	OM23P	OM18P	OM01P	GND
5	IM24P	IM19P	IM02P	GND
6	OM24P	OM19P	OM02P	GND
7	IM25P	IM20P	IM03P	GND
8	OM25P	OM20P	OM03P	GND
9	IM26P	IM21P	IM04P	GND
10	OM26P	OM21P	OM04P	SPGND
11	IM27P	ADSO	IM05P	SPGND
12	OM27P	ADSI	OM05P	SPGND
13		DSON	IM06P	TXDA
14		DSIN	OM06P	TRXCA
15	CPUN+		IM07P	HINTN
16		GND	OM08P	RTSA
17	PERINT6-	BUSGRI-	IM08P	DCDA
18	PERINT7-	BUSGRO-	OM08P	RXDA
19	BUSREQ-	PERINT2-	IM09P	SYNCA
20	DS-	PERINT3-	OM09P	DTR-REQA
21		PERINT4-	IM10P	CTSA
22	BUSBSY-	PERINT5-	OM10P	TXDB
23	RSTOUT-	BUSLOCK-	IM11P	TRXCB
24	PERINT1-	PERINT0-	OM11P	
25	BEN1-	BEN0-	IM12P	RTSB
26	BEN3-	BEN2-	OM12P	DCDB
27	GND	DAS-	IM13P	RXDB
28	WRT-	GND	OM13P	SYNCB
29	EDTACK-	DTACK-	IM14P	HW4
30	PARITY+	SSR-	OM14P	
31	PRTYEN-	MEMERR-	IM15P	SH0
32	FAS-	GND	OM15P	SH1
33	DAS32-	CPUCLK+	IM16P	
34	DATA00	EDAS-	OM16P	
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10	PBRST-	SP+5V
45	DATA11	ADDR11	PERR-	SP+5V



	D	C	B	A
46	DATA12	ADDR12	DISABSAN-	+5V
47	DATA13	ADDR13	GND	+5V
48	DATA14	ADDR14	FACKN	+5V
49	DATA15	ADDR15	ENOMN	+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21	GND	+5V
56	DATA22	ADDR22	GND	
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27	GND	GND
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		GND
66		FC0+		GND
67		FC1+		
68		FC2+		
69				
70				GND
71	RSTIN	IM28P		GND
72	RSTON	OM28P		
73	CLPIN	IM29P		
74	CLKOP	OM29P		
75	IMCRN	IM30P		GND
76	OMCRN	OM30P		
77	IMCWN	IM31P		
78	OMCWN	OM31P		
79			DTR-REQB	SPGND
80	OMMN		CTSB	SPGND
81	ACTIN	MSCCN		SPGND
82	ACTON	OSCCN		GND
83	OFFIN	IPR0N		GND
84	OFFON	OPR0N		GND
85	IFRCN	IPR1N	NMIN	GND
86	OFRCN	OPR1N	CKFLN	GND
87	IFRLN	IPR2N	HEXDN	GND
88	OFRLN	OPR2N	JAMIN	GND
89	IFRDP	IPR3N	EBENN7	GND
90	OFRDP	OPR3N	LED1	GND

NT9X14AA

Product description

The NT9X14AA card is a 4-Mbyte memory board with error checking and correction (ECC). The DMS-100E uses the NT9X14AA card. This card can divide into two separate 2-Mbyte memory modules. The arrangement of each memory module is a 2×40 array of 256×1 dynamic random access memory (RAM) (DRAM). Each memory modules subdivides into banks of 1×40 DRAMs. The 40-bit memory width has 32 data bits, 7 check bits and 1 parity bit. The supports all types of memory access.

Functional description

Functional blocks

The NT9X14AA card contains the following functional blocks:

- element address decoding
- main memory address decoding
- timing and control
- address bus (A-bus) interface
- parity
- error logging
- memory page mode
- diagnostic modes

Element address decoding

During system initialization, the element block enables identify elements of NT9X14AA. The element block decode circuits provide enables for the motherboard identification (ID) PROM and the control registers.

The decoding design allows 16 elements for each slot and 64 bytes for each element. The EBENN signals to select elements on the NT9X14 motherboard. The element block enables decode the NT9X14 motherboard as element 0. The element block enables designate the memory modules as elements 1 and 2.

Main memory address decoding

Module select and page mode address comparators provide address decoding. When a module selection occurs, NT9X14 generates the signal SSRN. The SSRN signal is a buffered version of the output of the module select comparator. The SSRN provides synchronized operation between the memory controller and the memory access unit.

NT9X14AA (continued)

Timing and control

The NT9X14AA supports 32 bit and 16-bit system memory cycles.

All timing is based on the 256×1 DRAM with 120-ns maximum access time. In a synchronized bus environment, optimal system performance enhances the entire processor. In an asynchronous bus environment, the system directs valid data to the bus according to the peripheral bus specification.

The A-bus interface

The NT9X14AA works with 32-bit devices and 16-bit devices. During access to the main memory address space, the NT9X14 motherboard always sends 32-bit responses.

The new peripheral bus specification supports a 4-Gbyte address range. When the memory controller receives the 32-bit address strobe, NT9X14 starts a 32-bit memory cycle. The 32-bit address strobe indicates that the address bus is correct over the 4-Gbyte range. The current 16-bit processor and peripherals use the 16-bit address strobes. The 16-bit address strobes map to the top 16 Mbytes of the 4-Gbyte range. In 16-bit mode, EAENN is not applied and address bits are masked to logical 1.

Parity

After the generation of the bus parity bit, the bit transmits to the bus master for parity error checking. After the selection of a module, NT9X14 sends the signal PRENN to the bus master. Information about parity errors is not latched. An optional address parity DRAM is present for additional protection against addressing errors. During write cycles, the address parity bit calculates over 32 address bits. The address parity DRAM contains the address parity bit during write cycles. During the read cycles, the address parity bit reads from DRAM and feeds to the bus parity logic. The parity calculation includes the address parity bit after the bus parity logic receives the bit.

Error logging

For maintenance purposes, the memory controller latches information about memory errors in the status registers of the controller. This action identifies the types of memory data errors. Signal MERRN is an interrupt line. Signal MERRN is asserted when the following conditions occur:

- a data error in check-only mode
- a multiple data error in error correction code (ECC) mode

The processor must access a status register to reset this signal.

Memory page mode

The block allows for consecutive memory accesses at multiple locations in the same page. These memory accesses increase speed without an increase in power use. The block strobes a row address into DRAM. This action maintains a low RASN signal during all consecutive memory cycles that have the row address in common. The current dynamic memories allow the RASN signal to remain low for a maximum of 10 µs. *The NT9X14 motherboard includes a page mode timeout preset register. The register is loaded during system initialization.*

Diagnostic modes

The memory controller supports two diagnostic modes. The two diagnostic modes can occur during manufacturing test and normal system diagnostic routines. Diagnostic 1 mode allows tests of the check bits memory through the system data bus. Diagnostic 2 mode allows tests of the ECC part of the memory controller.

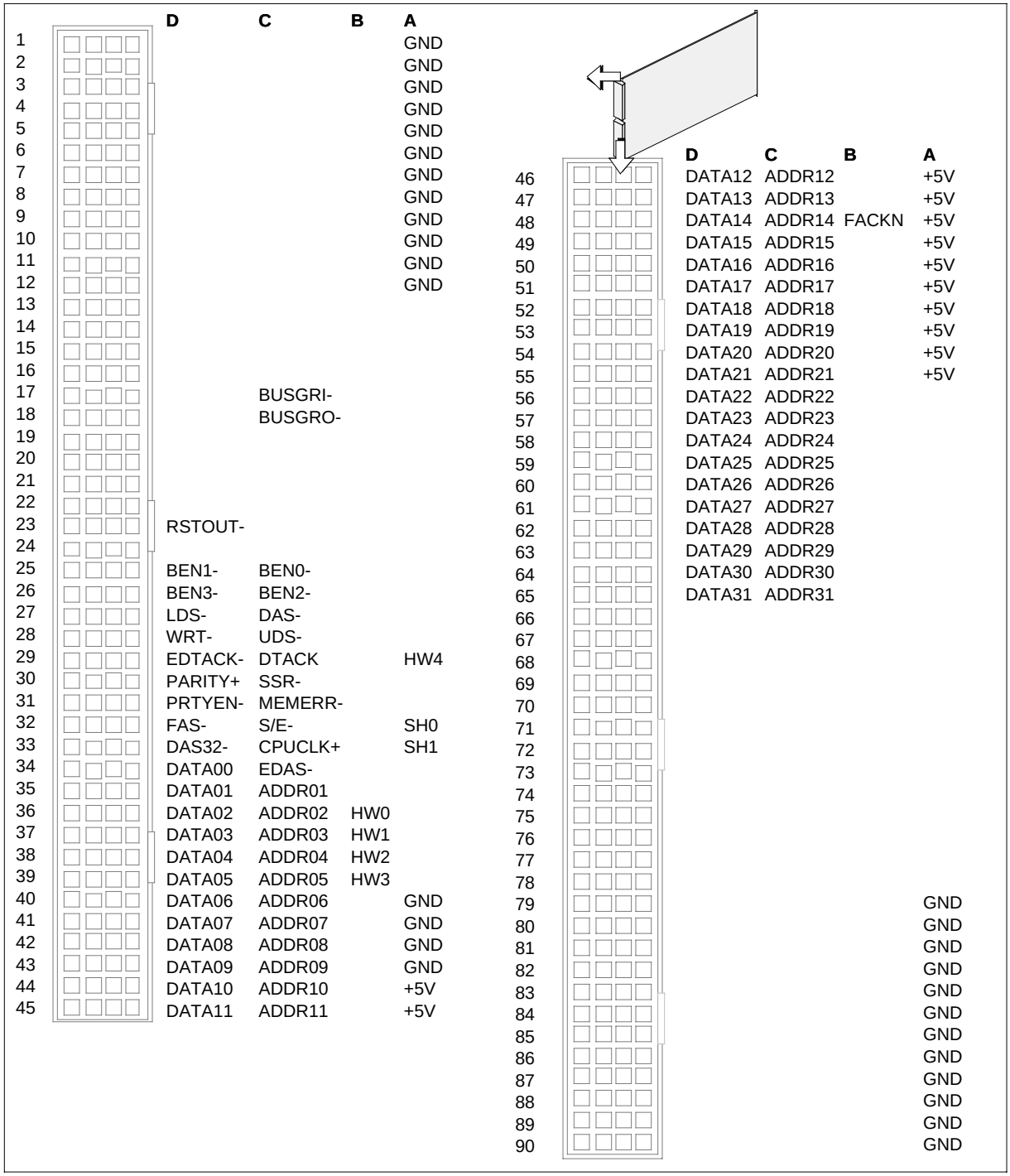
Signaling

Pin numbers

The pin numbers for appear NT9X14AA in the following figure.

NT9X14AA (end)

NT9X14AA pin numbers



	D	C	B	A
1				GND
2				GND
3				GND
4				GND
5				GND
6				GND
7				GND
8				GND
9				GND
10				GND
11				GND
12				GND
13				
14				
15				
16				
17		BUSGRI-		
18		BUSGRO-		
19				
20				
21				
22				
23	RSTOUT-			
24				
25	BEN1-	BEN0-		
26	BEN3-	BEN2-		
27	LDS-	DAS-		
28	WRT-	UDS-		
29	EDTACK-	DTACK		HW4
30	PARITY+	SSR-		
31	PRTYEN-	MEMERR-		
32	FAS-	S/E-		SH0
33	DAS32-	CPUCLK+		SH1
34	DATA00	EDAS-		
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06		GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08		GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10		+5V
45	DATA11	ADDR11		+5V

	D	C	B	A
46	DATA12	ADDR12		+5V
47	DATA13	ADDR13		+5V
48	DATA14	ADDR14	FACKN	+5V
49	DATA15	ADDR15		+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21		+5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70				
71				
72				
73				
74				
75				
76				
77				
78				
79				GND
80				GND
81				GND
82				GND
83				GND
84				GND
85				GND
86				GND
87				GND
88				GND
89				GND
90				GND

NT9X14BB

Product description

The NT9X14BB card is a 6-Mbyte memory board with error checking and correction (ECC). The DMS-100E uses the NT9X14BB. The card can divide into three separate 2-Mbyte memory modules. The arrangement of each memory module is a 2×40 array of 256×1 dynamic random access memory (RAM) (DRAM). The three memory modules subdivide into banks of 1×40 DRAMs. The 40-bit memory width has 32 data bits, 7 check bits, and one parity bit. The NT9X14BB supports all types of memory access. The synchronous memory bus accesses the memory. The asynchronous peripheral bus reads the (ID) PROM and accesses the status registers. This memory board is not compatible with the address-bus (A-bus).

Functional description

Functional blocks

The NT9X14BB has the following functional blocks:

- element address decoding
- main memory address decoding
- timing and control
- an A-bus interface
- parity
- error logging
- memory page mode
- diagnostic modes

Element address decoding

During system initialization, the element block enables identify elements of NT9X14BB. The element block decode circuits provide enables for the motherboard ID PROM and the control registers.

The decoding design allows 16 elements for each slot and 64 bytes for each element. The EBENN signals to select elements on the NT9X14BB. The element block enables decode the NT9X14BB ID PROM as element 0. The element block enables designate the memory modules as elements 1, 2 and 3.

Main memory address decoding

Module select and page mode address comparators in the memory controllers provide address decoding. When a module selection occurs, generates the signal SSR-. The output of the module select comparator in the memory

NT9X14BB (continued)

controller produces the signal. Signal SSR- is for synchronized operation between card and the processor board NT9X13.

Timing and control

Card NT9X14BB supports all memory cycles described in the memory bus specification and peripheral bus specification. This board provides more ground pins because the board does not support the A-bus specification.

All timing is based on 256×1 DRAM with 120 ns maximum access time. All 0D2 NT9X14BB and some OD1NT9X14BBs have 100-ns DRAMs to decrease the access time. These packs must initialize to 120 ns in base+1C register of the memory controllers on the pack. A new issue of the ID PROM identifies these packs.

Parity

After the generation of the bus parity bit, the bit transmits to the bus master for parity error checking. After the selection of a module, NT9X14BB sends the signal PREN- to the bus master. Information about parity errors is not latched. The NT9X14BB parity logic only sends parity after parity from the memory controller settles. An optional address parity DRAM is present for additional protection against addressing errors. During write cycles, the address parity bit calculates over 32 address bits. The address parity DRAM contains the address parity bit during write cycles. During the read cycles, the address parity bit reads from DRAM and feeds to the bus parity logic. The parity calculation includes the address parity bit after the bus parity logic receives the bit.

Error logging

For maintenance purposes, the memory controller latches information about memory errors. The memory controller latches information in the status registers of the controller to identify the types of memory data errors. Signal MERR- is an interrupt line. Signal MERR- is asserted for a data error in check-only mode or multiple data error in ECC mode. The processor has to access a status register to reset this signal.

Memory page mode

The block allows for consecutive memory accesses at multiple locations in the same page. These memory accesses increase speed without an increase in power use. The block strobes a row address into DRAM. This action maintains a low RASN signal during all consecutive memory cycles that have the row address in common. The current dynamic memories allow the RASN signal to remain low for a maximum of 10 µs. *Card NT9X14BB includes a page mode preset register and a page mode counter.*

Refresh control

The memory controller H22 and H44 also provide a mechanism to preset the refresh counters. The mechanism writes to a control register to preset the refresh counters. This action distributes the memory refreshes in the system so that memories do not refresh at the same time. The handshake override operation of the DMS-100E computing module requires synchronization of the refresh counters that correspond on both sides.

Diagnostic modes

The memory controller supports two diagnostic modes. These modes can occur during manufacturing test routines and normal system diagnostic routines. Diagnostic 1 mode allows tests of the check bit memory through the system data bus. Diagnostic 2 mode allows tests of the ECC part of the memory controller.

Signaling

Pin numbers

The pin numbers for card NT9X14AA appear in the following figure.

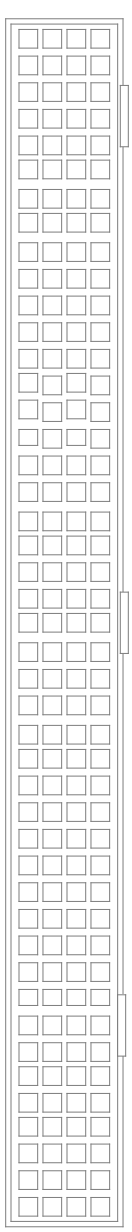
Technical data

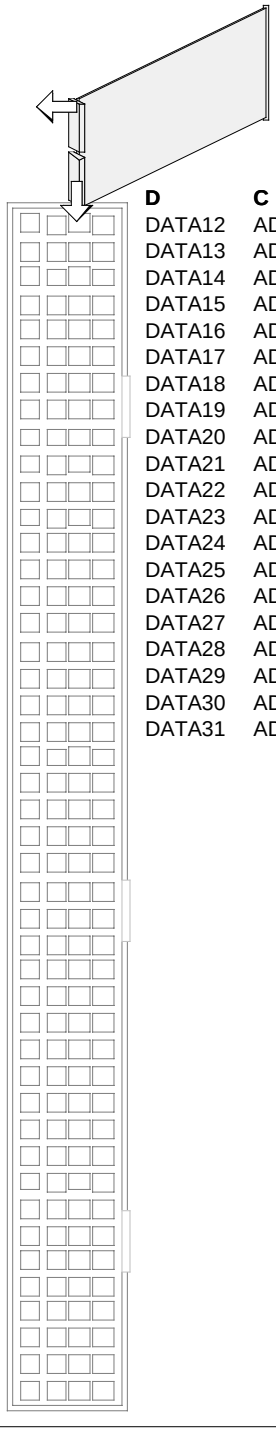
Power requirements

Card NT9X14BB requires a +5V current supply. The database transceivers on connect to a special power SP+5. The data bus ground is separate from the logic ground that the rest of the board uses. The separation minimizes the noise on the main logic ground. High-to-low transitions of the data bus cause the noise.

NT9X14BB (end)

The NT9X14BB pin numbers





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1				GND
2				GND
3				GND
4				GND
5				GND
6				GND
7				GND
8				GND
9				GND
10				SPGND
11				SPGND
12				SPGND
13				
14				
15				
16				
17		BUSGRI-		
18		BUSGRO-		
19				
20				
21				
22				
23	RSTOUT-			
24				
25	BEN1-	BEN0-		
26	BEN3-	BEN2-		
27	LDS-	DAS-		
28	WRT-	UDS-		
29	EDTACK-	DTACK-		HW4
30	PARITY+	SSR-		
31	PREN-	MEMERR-		
32	FAS-	S/E-		SH0
33	DAS32-	CPUCLK+		SH1
34	DATA00	EDAS-		
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06		GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08		GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10		SP+5V
45	DATA11	ADDR11		SP+5V

	D	C	B	A
46	DATA12	ADDR12		+5V
47	DATA13	ADDR13		+5V
48	DATA14	ADDR14	FACK-	+5V
49	DATA15	ADDR15		+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21		+5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
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64	DATA30	ADDR30		
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79				SPGND
80				SPGND
81				SPGND
82				GND
83				GND
84				GND
85				GND
86				GND
87				GND
88				GND
89				GND
90				GND

NT9X14DB

Product description

The NT9X14DB card is a 24-Mbyte memory board equipped with error checking and correction (ECC). The DMS SuperNode uses card NT9X14DB. The card divides into three separate 8-Mbyte memory modules. The arrangement of each memory module is a 2×40 array of 256×1 dynamic random access memory (DRAM). The three modules subdivide into banks of 1×40 DRAMs. The 40-bit memory width has 32 data bits, 7 check bits, and one parity bit. The NT9X14DB supports all types of memory access. The synchronous memory bus accesses the memory. The asynchronous peripheral bus reads the (ID) PROM and accesses the status registers. This board is not compatible with the address bus (A-bus).

Functional description

Functional blocks

Card NT9X14DB has the following functional blocks:

- element address decoding
- main memory address decoding
- timing and control
- parity
- error logging
- memory static column mode
- refresh control
- diagnostic modes

Element address decoding

During system initialization, the element block enables identify elements of NT9X14DB. The element block decode circuits provide enables for the motherboard ID PROM and the control registers.

The decoding design allows 16 elements for each slot and 64 bytes for each element. The EBENN signals to select elements on the NT9X14DB. The element block enables decode the ID PROM as element 0. The element block enables designate the memory modules as elements 1, 2 and 3.

Main memory address decoding

Module select and page mode address comparators in the memory controllers provide address decoding. When a module selection occurs, NT9X14DB generates the signal SSR-. The output of the module select comparator in the

NT9X14DB (continued)

memory controller produces the signal. Signal SSR- is for synchronized operation between card NT9X14DB and the processor board NT9X13.

Timing and control

The NT9X14DB supports all memory cycles described in the memory bus specification and peripheral bus specification. This board does not support the A-bus specification.

The 1M×1 static column DRAMs with 100-ns access time determines all timing.

Parity

After the generation of the bus parity bit, the bit transmits to the bus master for parity error checking. After the selection of a module, NT9X14DB sends the signal PREN- to the bus master. Information about parity errors is not latched. The parity logic only sends parity to the back plane when parity from the memory controller settles. An optional address parity DRAM is present for additional protection against addressing errors. During write cycles, the address parity bit calculates over 32 address bits. The address parity DRAM contains the address parity bit during write cycles. During the read cycles, the address parity bit reads from DRAM and feeds to the bus parity logic. The parity calculation includes the address parity bit after the bus parity logic receives the bit.

Error logging

For maintenance purposes, the memory controller latches information about memory errors in the status registers of the memory controller. This action identifies the types of memory data errors. Signal MERR- is an interrupt line. Signal MERR- appears for a data error in check-only mode or multiple data error in ECC mode. The processor must access a status register to reset this signal.

Memory static column mode

The block allows for consecutive memory accesses at multiple locations in the same page. These memory accesses increase speed without an increase in power use. The block strobes a row address into DRAM. This action maintains low RASN and CASN signals during all consecutive memory cycles that have the row address in common. The current dynamic memories allow the RASN and CASN signals to remain low for a maximum of 10 µs.

When DMS SuperNode computing modules (CM) use NT9X14DB,the static column mode counters must synchronize for handshake override operation. The handshake override operation occurs when a wait loop with a minimum of 10 µs loses static RAM on NT9X13. The wait loop loses static RAM while the

CPUs are in synchronization. This process makes sure that static column mode counters expire on both sides.

Refresh control

The memory controller H44 provides a mechanism to preset the refresh counters. The mechanism writes to a control register to preset the refresh counters. This action distributes the memory refreshes in the system so that all memories do not refresh at the same time. The handshake override operation also requires the synchronization of the refresh counters that correspond on both sides.

Diagnostic modes

The memory controller supports two diagnostic modes. These modes can occur during manufacturing test routines and normal system diagnostic routines. Diagnostic 1 mode allows tests of the check bit memory through the system data bus. Diagnostic 2 mode allows tests of the ECC part of the memory controller.

Signaling

Pin numbers

The pin numbers for card NT9X14DB appear in the following figure.

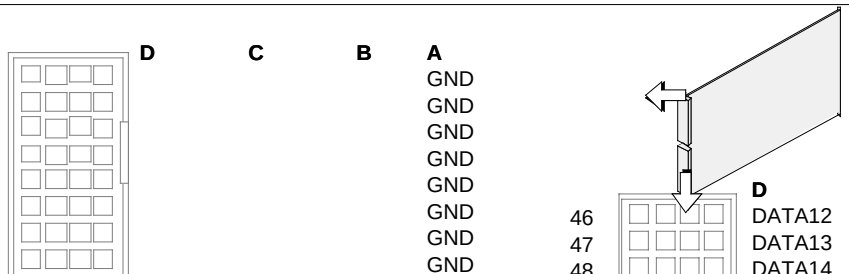
Technical data

Power requirements

Card NT9X14DBrequires a +5V current supply. The database transceivers on NT9X14DB connect to a special power SP+5 and a special ground. These power and group signals are separate from the regular power and ground signals. The separation minimizes the noise on the regular logic ground. High-to-low transitions of the data bus cause the noise.

NT9X14DB (end)

NT9X14DB pin numbers



	D	C	B	A
1				GND
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25	BEN1-	BEN0-		
26	BEN3-	BEN2-		
27	LDS-	DAS-		
28	WRT-	UDS-		
29	EDTACK-	DTACK-		HW4
30	PARITY+	SSR-		
31	PREN-	MEMERR-		
32	FAS-	S/E-		SH0
33	DAS32-	CPUCLK+		SH1
34	DATA00	EDAS-		
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06		GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08		GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10		SP+5V
45	DATA11	ADDR11		SP+5V

	D	C	B	A
46	DATA12	ADDR12		+5V
47	DATA13	ADDR13		+5V
48	DATA14	ADDR14	FACK-	+5V
49	DATA15	ADDR15		+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21		+5V
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89				GND
90				GND

NT9X14EA

Product description

The NT9X14EA is a 96 Mbyte memory card. The NT9X14EA circuit card provides storage for the NT9X13MB central processing unit (CPU) of the DMS SuperNode and the DMS SuperNode SE. The NT9X14EA circuit card supports error checking and correction (ECC) and parity. The NT9X14EA circuit card has three identical, independent memory modules. Each module has two banks of 40 4 Mbyte by 1 bit dynamic random-access memories (DRAM). Each bank contains 32 DRAMs for data, 7 DRAMs for the error checking and correction bits, and 1 DRAM for parity.

The NT9X14EA has the following functions:

- contains three independent 32 Mbyte memory modules
- allows memory modules to be mapped on any 2 Mbyte boundary in synchronous memory bus (MEMBUS) address space
- retains complete memory contents when a module moves to a different base address
- supports MEMBUS accesses. Supports high speed, multi-longword burst accesses
- stores a series of long words in alternate memory banks for interleaved burst accesses
- supports page mode for faster accesses when the row addresses of a series of accesses are the same
- provides software with refresh synchronization control. This function allows memory accesses in handshake override mode with NT9X13 and NT9X10 processors. The function allows software control over refresh staggering on the backplane.
- supports error detection and correction
- corrects all possible single bit errors
- detects all possible single bit and double bit errors
- detects errors when any combination of bits in the same nibble is in error.

Note: A nibble is a group of four bits on a four bit boundary.

The NT9X14EA circuit card is compatible with backplane frequencies from 16 MHz to 20 MHz. This compatibility allows the NT9X14EA circuit card to be compatible with current NTX910 and NT9X13 processors. The NT9X14EA circuit card is compatible with backplanes for previous versions of the NT9X14EA series memory cards. The NT9X14EA circuit card uses the

NT9X14EA (continued)

same backplane connections, peripheral bus and memory bus protocols as in earlier versions.

The current memory controller application specific integrated circuit (ASIC) has a different register set. The current memory controller ASIC requires upgraded firmware and software.

Location

The NT9X14EA memory circuit cards reside in the slots

- 11-16 and slots 23-28 of the computing module (CM) shelf in the DMS SuperNode

  Note: Memory slots not used, slots 7-10 and 29-32, must contain filler circuit cards for the DMS SuperNode.

- 12-16 and slots 23-27 of the CM/system load module (SLM) shelf in the DMS SuperNode SE

Functional description

The NT9X14EA circuit card expands memory capacity from 240 Mbytes to 960 Mbytes. The three independent 32 Mbyte memory module blocks of the card expand the memory capacity. Write access to one block of memory does not affect access to the other two blocks of memory. The blocks of memory are on the same card.

Functional blocks

Functional blocks of the NT9X14EA circuit card are:

- the address buffer, latch
- data buffers
- clock conditioning
- the control signal input
- the control signal output
- the ID PROM
- memory modules

Each memory module has the following functional blocks:

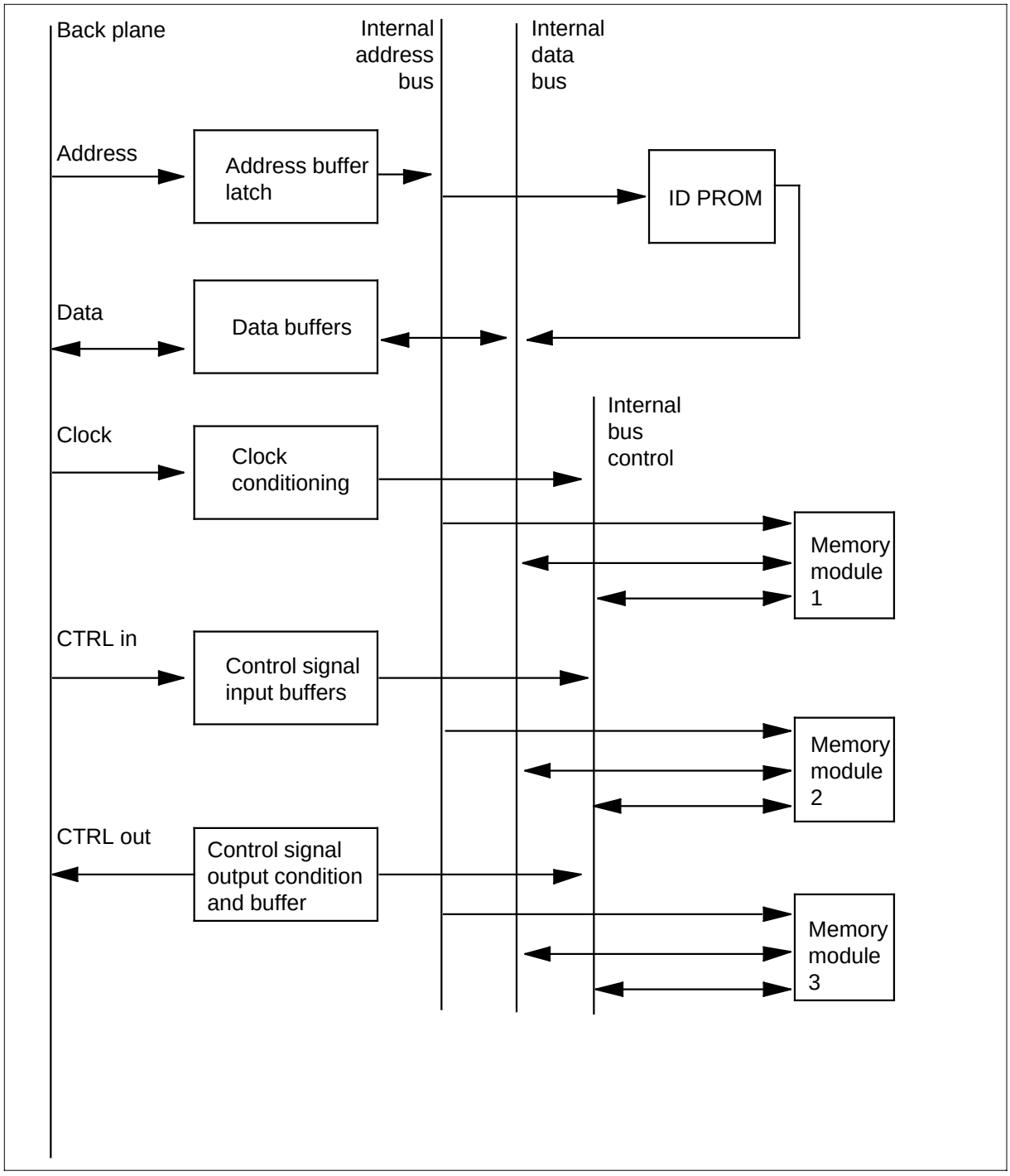
- memory controller application-specific integrated circuit (ASIC)
- memory bank data buffers

- memory address and control buffers
- DRAM banks

The relationship between the functional blocks of the NT9X14EA circuit card appear in the next figure.

NT9X14EA (continued)

NT9X14EA functional blocks of whole card



Address buffer (latch)

The address buffer block contains four 74F373 latches. This block buffers to the backplane address to drive the internal address bus of the NT9X14EA circuit card. Because the memory controllers latch the address internally, it is only necessary to latch it here for ID PROM accesses.

Data buffers

The data buffers block buffers data between the backplane and the internal bus of the board. This block contains two sets of 74F245 buffers in parallel.

Clock conditioning

The backplane clock is first buffered by the clock PAL. The clock PAL is a PAL16L8. This clock PAL contains a PAL equation that filters malfunctions from the rising and falling edges of the clock. The backplane clock is reconditioned and buffered by a phase-locked loop (PLL) device. The reconditioned clock produces clean and stable board clocks at the backplane clock frequency. Frequencies at twice the backplane clock frequency are required for ASIC application

Control signal input

The control signal input block buffers the backplane control input signals. This block is part of the backplane clock buffer PAL. The signals that route through the PAL are treated in a unique way. The clock is run through a debugging equation for safety. The BPWRTN signal is latched when the backplane buffers are activated. The BPWRTN signal is latched to prevent the feed-back of ground bounce noise into the buffer control inputs.

Control signal output

The control signal output block forces the outbound control signals to the backplane. The BPPARENN and BPMEMERRN signals are low driven signals, expected to return as high driven signals through the backplane pull-up resistors. The BPPARITY signal is driven when the BPPARENN signal is asserted.

The remaining signals are bus cycle acknowledgements: PBDTACKN, BPEDTACKN, BPFACKN and BPBACKN. The bus cycle acknowledgements must have good rising edges and are post charged. The acknowledgements are post charged by keeping the active driver enabled for a period of time after the acknowledgements have reached a certain level. The ACTIVxN signals from the memory controllers activate the driver

The ASICs generate synchronous acknowledgements BPFACKN and BPBACKN. The acknowledgements are delayed until the rising edge of the backplane clock by the FACK PAL. The delay gives maximum setup time to

NT9X14EA (continued)

the next rising edge, where the acknowledgments are sampled by the processor.

The BPBACKN signal requires a straight forward D flip-flop. The timing of the advanced FACK signal uses a set-reset latch. The presence of one of the advanced FACK signals (AFACKxN) sets the latch. The AFACKxN signal must occur when the board clock is high and a delayed inverted version of the AFACKxN is low. The system generates the delayed inverted version of the clock and feeds the clock to the FACK PAL.

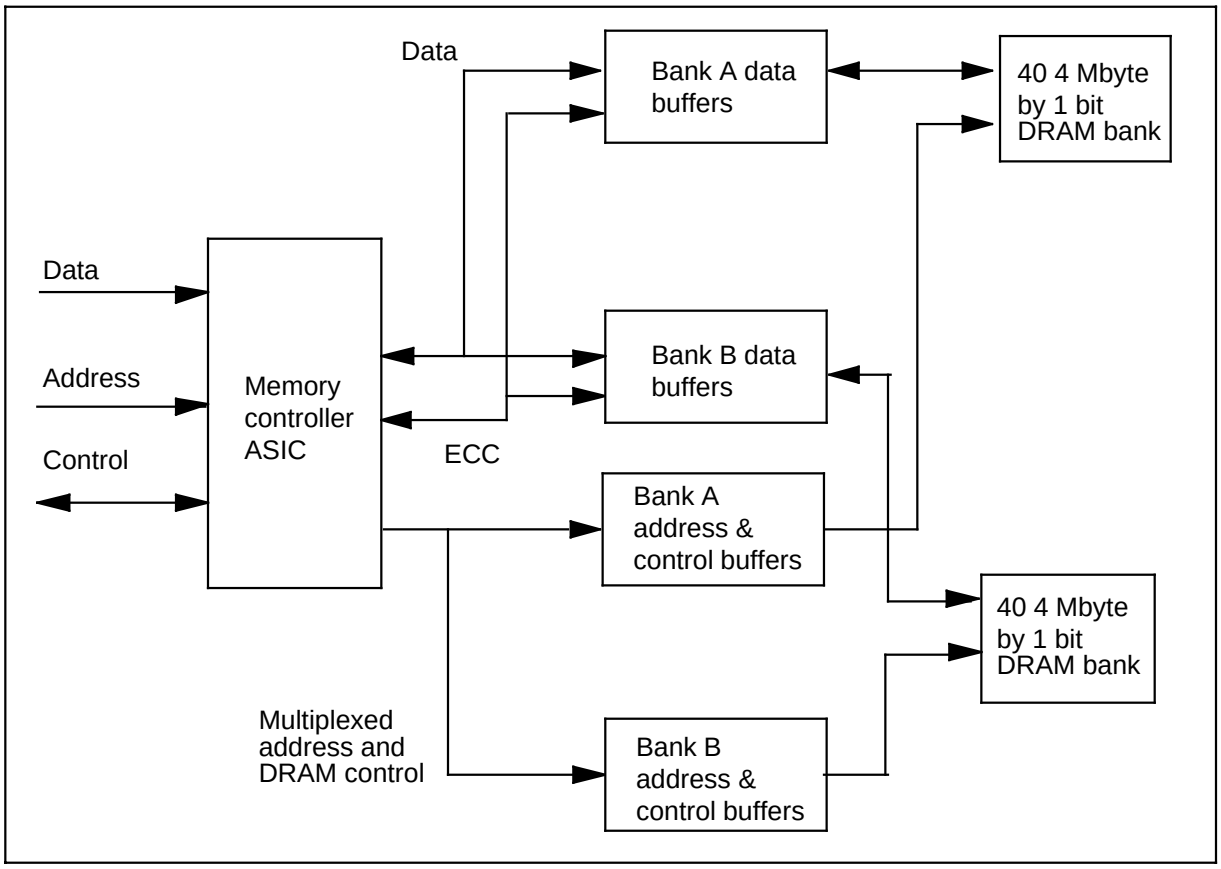
ID PROM

The ID prom block is the ID PROM for the board. The PROM output does not perform additional buffering.

Memory modules

The memory module blocks are three identical memory modules. A functional block diagram of a memory module is in the next illustration.

NT9X14EA memory module



Memory controller ASIC

The memory controller ASIC block is the S49 controller of burst access memory. This memory controller block generates all control information for the module

Memory bank data buffers

The memory bank data buffers contain five bus transceivers. The transceivers separate the data lines of the two banks. This separation prevents the collision of the data drivers during interleaved burst reads. The data drivers are from two different banks of DRAMs.

Memory address and control buffers

Each of the memory address and control buffers block contains two drivers that send the items in this list, to the 40 DRAMs in a bank:

- a multiplexed DRAM address
- the row address strobe
- a column address strobe
- write-enable signals

DRAM banks

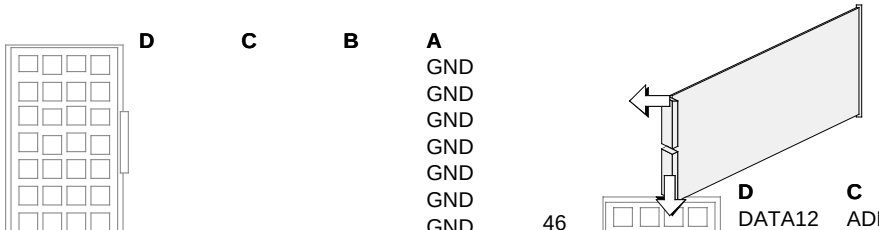
The DRAM blocks contain 40 4 Mbyte by 1 bit DRAMs of which 32 blocks store data and 8 blocks store ECC bits.

Signaling

Pin numbers for the NT9X14EA circuit card appear in the next figure.

NT9X14EA (continued)

NT9X14EA pin numbers



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1				GND
2				GND
3				GND
4				GND
5				GND
6				GND
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9				GND
10				GND
11				GND
12				GND
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16				
17		BUSGRI-		
18		BUSGRO-		
19				
20				
21				
22				
23	RSTOUT-			
24				
25	BEN1-	BEN0-		
26	BEN3-	BEN2-		
27	GND	BAS-		
28	WRT-	GND		
29	EDTACK-	DTACK-		HW4
30	PARITY+	SSR-		
31	PAREN-	MEMERR-		
32	FAS	GND	SH0	
33	DAS32-	CPUCLK+	SH1	
34	DATA00	BACK-		
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06		SPGND
41	DATA07	ADDR07		SPGND
42	DATA08	ADDR08		SPGND
43	DATA09	ADDR09		SPGND
44	DATA10	ADDR10		SP+5V
45	DATA11	ADDR11		SP+5V

	D	C	B	A
46	DATA12	ADDR12		+5V
47	DATA13	ADDR13		+5V
48	DATA14	ADDR14	FACK-	+5V
49	DATA15	ADDR15		+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21		+5V
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57	DATA23	ADDR23		
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79				SPGND
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82				GND
83				GND
84				GND
85				GND
86				GND
87				GND
88				GND
89				GND
90				GND

Technical data

The NT9X14EA circuit card requires a +5V direct current supply.

NT9X14FA

Product description

The NT9X14FA card is a 96 Mbyte memory card that provides storage for the NT9X10DA central processing unit of the DMS SuperNode and DMS SuperNode SE. The card supports error checking and correction (ECC), and parity. The card consists of three identical, independent memory modules. Each module consists of two banks of 40 4 Mbyte by 1 bit dynamic random access memory (DRAM) modules. Each bank contains 32 DRAMs for data, 7 for the ECC bits, and 1 for parity.

The NT9X14FA card does the following:

- contains three independent 32 Mbyte memory modules
- enables memory modules to be mapped on any 2 Mbyte boundary in memory bus (MEMBUS) address space
- retains memory contents intact when a module is moved to a different base address
- supports synchronous memory bus (MEMBUS) accesses and high speed, multi-longword burst accesses
- stores successive longwords in alternate memory banks for interleaved burst accesses
- supports page mode for faster accesses when the row addresses of successive accesses are the same
- provides software with refresh synchronization control. This control allows memory accesses in handshake override mode with NT9X13 and NT9X10 processors. It also enables software control over refresh staggering on the backplane.
- supports error detection and correction
- corrects all possible single-bit errors
- detects all possible single-bit and double-bit errors
- detects errors where any combination of bits in the same NIBBLE (group of four bits on a four-bit boundary) is in error

The card is identical to the NT9X14EA memory card, except that it runs at a higher frequency. The SR70EM 66MHz processor runs at 66 MHz and the backplane bus frequency is 22.184 MHz. The card is compatible with backplane frequencies from 16 MHz to 22.184 MHz.

The is hardware compatible with previous versions of the NT9X14 series memory cards. It uses the same backplane connections and the same asynchronous (PBUS) and MEMBUS protocols. However, the NT9X14FA

card does not drive the SSR- signal. The card has a new memory controller with a different register set and larger memory modules than earlier memory cards. The card requires upgraded firmware and software to support it.

The NT9X14FA memory card is an optional memory extension card designed for use exclusively with the NT9X10DA processor card and the NT9X26GA RTIF card. Do not combine an NT9X14FA card with any other memory card. This results in an invalid memory configuration. Do not use the NT9X14FA memory card with any processor other than the NT9X10DA processor card.

Location

The NT9X14EA memory circuit cards reside in the slots

- 11-16 and slots 23-28 of the computing module (CM) shelf in the DMS SuperNode

  Note: Memory slots not used, slots 7-10 and 29-32, must contain filler circuit cards for the DMS SuperNode.

- 12-16 and slots 23-27 of the CM/system load module (SLM) shelf in the DMS SuperNode SE

Functional description

The card expands memory capacity from 240 Mbytes to 960 Mbytes because of its three independent 32 Mbyte memory module blocks. Write access to one block of memory does not affect access to the other two blocks of memory on the same card.

Functional blocks

The NT9X14FA consists of the following functional blocks:

- address buffer, (latch)
- data buffer
- clock conditioning buffer
- control signal input buffer
- control signal output
- element identification programmable read only memory (ID PROM)
- memory modules

Each memory module has the following functional blocks:

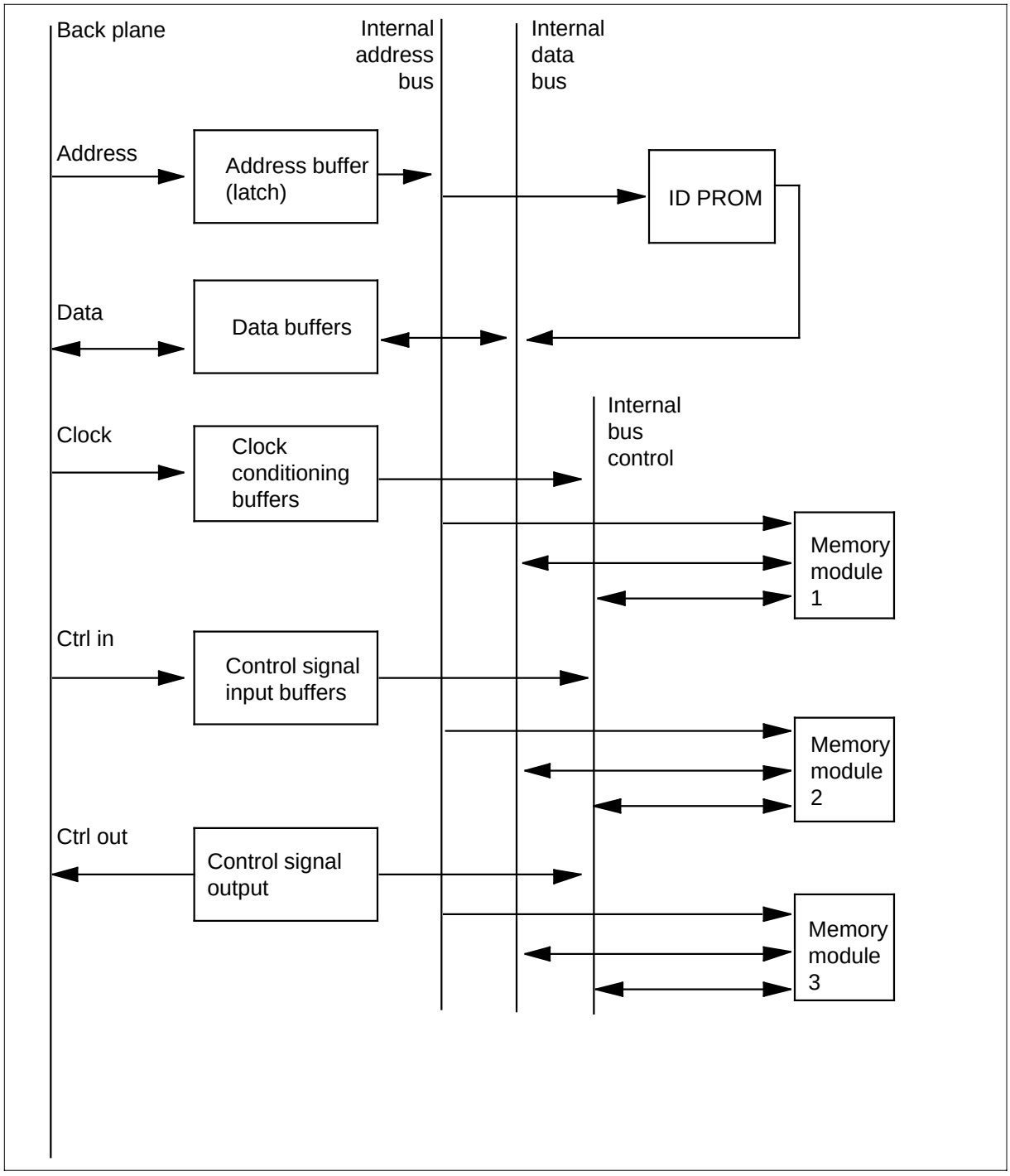
- memory controller application-specific integrated circuit (ASIC)
- memory bank data buffers

NT9X14FA (continued)

- memory address and control buffers
- DRAM banks

The following figure shows the relationship among the functional blocks. Descriptions of each functional block follow the figure.

NT9X14FA functional blocks of whole card



NT9X14FA (continued)

Address buffer (latch)

The address buffer block, made up of four 74F373 latches, buffers the backplane address to drive the internal address bus of the card. Because the memory controllers latch the address internally, it is only necessary to latch it here for ID PROM accesses.

Data buffer

This block acts as a buffer between the backplane and the internal bus. There are two sets of 74F245 buffers in parallel.

Clock conditioning buffer

The clock programmable array logic (PAL) buffers the backplane clock. The clock PAL contains a PAL equation that filters errors from the rising and falling edges of the clock. An MC88915 PLL device reconditions and buffers the backplane clock. This reconditioning produces stable and clean board clocks at both the backplane clock frequency (CLK) and twice the backplane clock frequency (2XCLK), as required by the ASICs. The 0D1 board contains a second MC88915 PLL device that provides early clocks (ECLK and 2XECLK).

Control signal input buffer

This block buffers the backplane control input signals. The control signal input block consists of 1 74F244 buffer. It is also consists of part of the backplane clock buffer PAL. As described above, a debugging equation reconditions the backplane clock. The BPWRTN signal latches when the backplane buffers are enabled, to guard against ground bounce noise that feeds back into the buffer inputs.

Control signal output

This block drives the outbound control signals to the backplane. The BPPARENN and BPMEMERRN are active low signals. The detection of the BPPARENN signal activates the BPPARITY signal. The remaining signals are the bus cycle acknowledgements: PBDTACKN, BPEDTACKN, BPFACKN, and BPBACKN. To provide good rising edges, these signals are post charged. The driver remains enabled until after the signals have gone high. The ACTIVxN signals from the memory controllers enable the driver. The driver delays the clock by one segment of the triple 10-ns delay line.

The ASICs generate and delay the synchronous acknowledgements-BPFACKN and BPBACKN-until the rising edge of the backplane clock by the FACK PAL. The delay allows maximum setup time before the next rising edge. The BPBACKN uses a simple D flip-flop, but the timing of the advanced FACK signals requires a set-reset latch. An advanced FACK signal (AFACKxN) sets the latch while the board clock is high and a delayed,

inverted version of it is still low. The delayed, inverted version of the clock is generated and also fed to the FACK PAL.

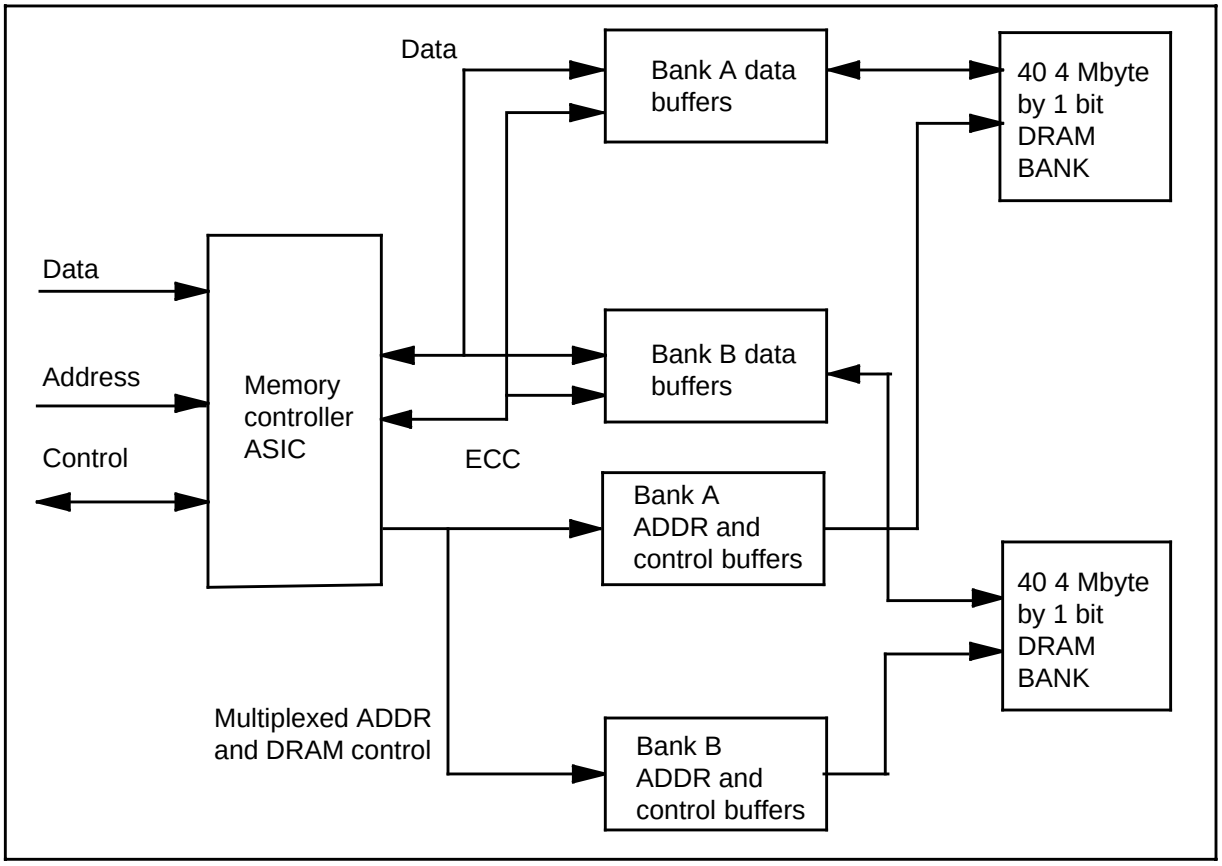
ID PROM

The ID prom block is the ID PROM for the board. The PROM output does not perform additional buffering.

Memory modules

The memory module blocks are three identical memory modules. The following figure provides a functional block diagram of a memory module. The functional blocks are described in the paragraphs that follow.

NT9X14FA functional blocks of memory modules 1, 2, and 3



Memory controller ASIC

The memory controller ASIC block is the S49 controller of burst access memory (CBAM). This memory controller block generates all control information for the module.

NT9X14FA (continued)

Memory bank data buffers

The memory bank data buffers contain five 74ABT245 bus transceivers that separate the data lines of the two banks. This separation prevents the data from one bank of DRAMs from colliding with the data from the other bank during interleaved burst reads.

Memory address and control buffers

Each of the memory address and control buffers block contains two drivers that send the items in this list, to the 40 DRAMs in a bank

- a multiplexed DRAM address
- row address strobe
- a column address strobe
- write-enable signals

DRAM banks

Each of these blocks consists of 40 4 Mbyte by 1 bit DRAMs, of which 32 store data and 8 store ECC bits.

Signaling

Pin outs

The following figure shows the pin outs for the NT9X14FA card.

NT9X14FA pin outs

	D	C	B	A
1				GND
2				GND
3				GND
4				GND
5				GND
6				GND
7				GND
8				GND
9				GND
10				GND
11				GND
12				GND
13				
14				
15				
16				
17		BUSGRI-		
18		BUSGRO-		
19				
20				
21				
22				
23	RSTOUT-			
24				
25	BEN1-	BEN0-		
26	BEN3-	BEN2-		
27	GND	BAS-		
28	WRT-	GND		
29	EDTACK-	DTACK-		HW4
30	PARITY+	SSR-		
31	PAREN-	MEMERR-		
32	FAS	GND		SH0
33	DAS32-	CPUCLK+		SH1
34	DATA00	BACK-		
35	DATA01	ADDR01		
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06		SPGND
41	DATA07	ADDR07		SPGND
42	DATA08	ADDR08		SPGND
43	DATA09	ADDR09		SPGND
44	DATA10	ADDR10		SP+5V
45	DATA11	ADDR11		SP+5V

	D	C	B	A
46	DATA12	ADDR12		+5V
47	DATA13	ADDR13		+5V
48	DATA14	ADDR14	FACK-	+5V
49	DATA15	ADDR15		+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21		+5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70				
71				
72				
73				
74				
75				
76				
77				
78				
79				SPGND
80				SPGND
81				SPGND
82				GND
83				GND
84				GND
85				GND
86				GND
87				GND
88				GND
89				GND
90				GND

NT9X14FA (end)

Technical data

The NT9X14FA circuit card requires a +5 V dc supply.

NT9X15AA

Product description

The NT9X15AA message switch mapper circuit card is part of the message switch. The mapper circuit card changes the addresses on the transaction bus (T-bus) from the logical node ID to the physical address. The software uses the logical node ID. The routing hardware uses the physical address.

Functional description

The NT9X15AA mapper is a memory card with a special function. The card performs logical-to-physical address translation for messages that route between ports. The mapper correlates the two addresses for the same data destination. The correlation of the addresses allows the software to use a logical address. The correlation of the addresses allows the hardware to use a physical address.

A packet switch called the T-bus carries messages through the message switch. In the message transfer, the destination for a data transmission is chosen during an address cycle that occurs before the data transfer.

The address cycle can be in a mapper-bypass mode or a mapper-assist mode. In the mapper-bypass mode, the address is the location address of the destination. In the mapper-assist mode, the address is the logical node ID. The software prefers the logical node ID of this address. The function, and not the location, references the destination. When only the function references the destination, you do not need to know the configuration of the system.

The NT9X15AA performs a monitoring function. The card provides the capability to flag specified logical addresses. The card also provides the capability to notify the message switch processor (MSP) when the addresses are in use.

Functional blocks

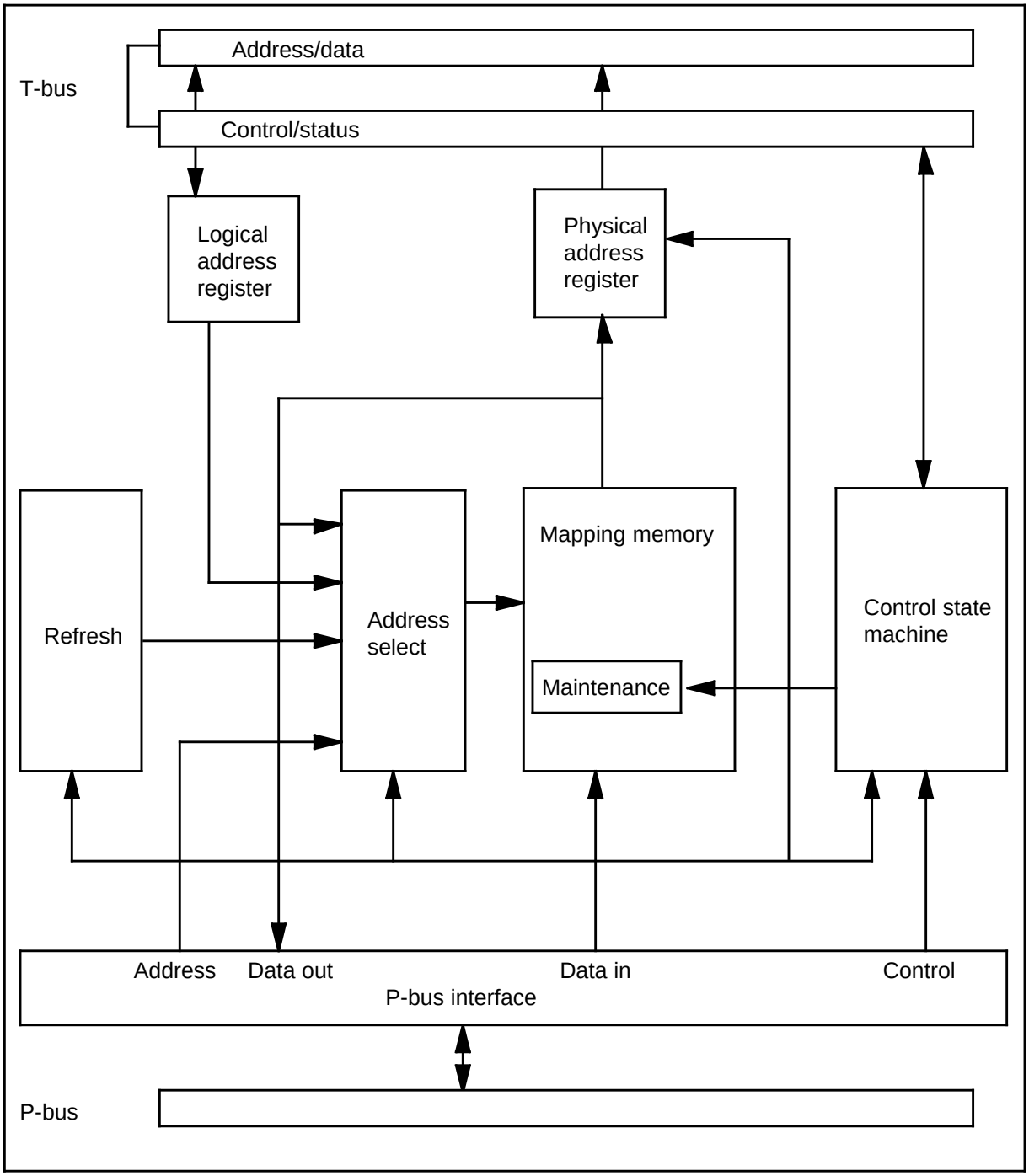
The NT9X15AA has the following functional blocks:

- the logical address register
- the location address register
- the refresh
- the address select
- the mapping memory
- the maintenance
- the control state machine
- the processor bus (P-bus) interface

NT9X15AA (continued)

The relationship between the functional blocks appears in the following figure.

NT9X15AA functional blocks



Logical address register

The logical address register stores the logical address from the message on the T-bus. This address applies to the on-board memory array address lines of the T-bus.

Location address register

The location address register stores the location address that applies to the T-bus address lines. The location address register is the destination of the message. The memory array on the board stores the physical address register.

Refresh

The dynamic RAM (DRAM) requires a continuous refresh cycle. The refresh block writes the data at a given address on top of the refresh block to refresh the DRAM.

Address select

The address select block is a set of multiplexers. This set allows only one of four address inputs to apply to the address lines of the memory array.

The different address inputs appear in the following list:

- converted physical address
- logical address
- refresh address
- P-bus address

The converted location address is the output of the memory array that fed to the input. You can use this address to check the accuracy of the logical-to-location address conversion.

Mapping memory

The mapping memory provides the logical-to-physical address correlation. The memory has DRAMs configured as an array of 256 kbyte by 19 bits.

Maintenance

The maintenance block of the mapper circuit card controls and monitors the following aspects of the mapper operation:

- power-up
- mapper enable
- mapper RAM parity errors
- mapper errors

NT9X15AA (continued)

- mapper/parity error interrupt enables
- error location
- P-bus parity error
- mapper unable to map (MUMP)

Control state machine

The control state machine changes the states of the card in a controlled sequence to control the mapper circuit card. These states are the four memory accesses. The control state machine decides when these accesses must occur.

The four memory accesses follow:

- a refresh
- an MSP access
- a map (mapper assist logical address translation)
- a converted physical address

The control state machine initiates error checking at the end of a MAP sequence.

Processor bus interface

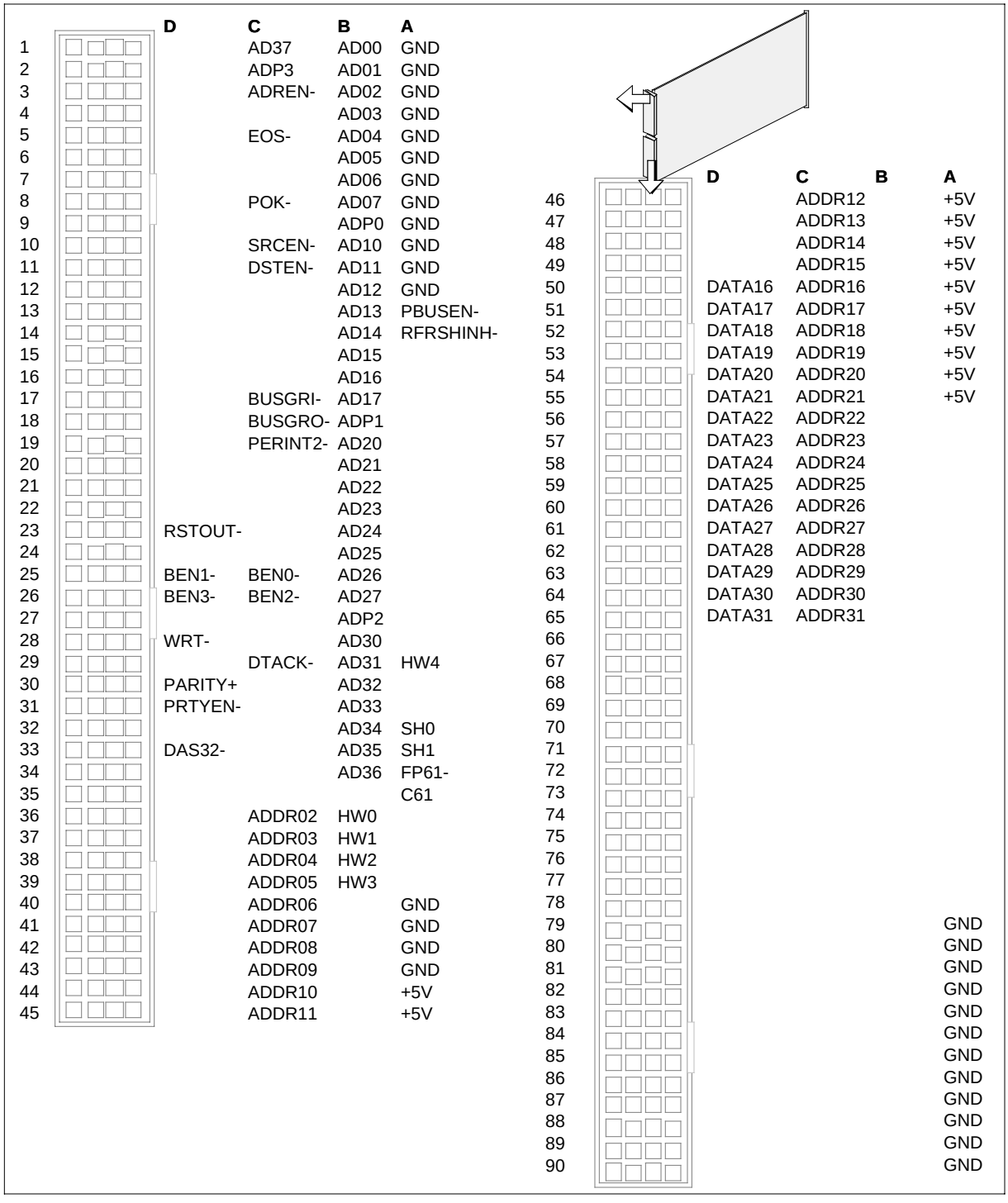
The P-bus interface block connects the mapper to the MSP. The mapper appears as a block of memory to the MSP.

Signaling

Pin numbers

The pin numbers for the NT9X15AA appear in the following feature.

NT9X15AA pin numbers



	D	C	B	A
1		AD37	AD00	GND
2		ADP3	AD01	GND
3		ADREN-	AD02	GND
4			AD03	GND
5		EOS-	AD04	GND
6			AD05	GND
7			AD06	GND
8		POK-	AD07	GND
9			ADP0	GND
10		SRCEN-	AD10	GND
11		DSTEN-	AD11	GND
12			AD12	GND
13			AD13	PBUSEN-
14			AD14	RFRSHINH-
15			AD15	
16			AD16	
17		BUSGRI-	AD17	
18		BUSGRO-	ADP1	
19		PERINT2-	AD20	
20			AD21	
21			AD22	
22			AD23	
23	RSTOUT-		AD24	
24			AD25	
25	BEN1-	BEN0-	AD26	
26	BEN3-	BEN2-	AD27	
27			ADP2	
28	WRT-		AD30	
29		DTACK-	AD31	HW4
30	PARITY+		AD32	
31	PRTYEN-		AD33	
32			AD34	SH0
33	DAS32-		AD35	SH1
34			AD36	FP61-
35				C61
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5V
45		ADDR11		+5V

	D	C	B	A
46		ADDR12		+5V
47		ADDR13		+5V
48		ADDR14		+5V
49		ADDR15		+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21		+5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
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78				
79				GND
80				GND
81				GND
82				GND
83				GND
84				GND
85				GND
86				GND
87				GND
88				GND
89				GND
90				GND

NT9X17AA

Product description

The NT9X15AA message switch four-port card provides a data path for messaging between the message switch (MS) and four external links.

Functional description

The NT9X15AA transfers messages between four links and the transaction bus (T-bus). The T-bus is a packet switch that can connect the links to any port on the MS. The T-bus can connect the links to the message switch processor (MSP). The links can be one of two physical types or one of four logical types. The two physical types are the DS30 and the DS512. The four logical types are the DS30, the DMSX, the DMSY, and the Framer. The on-card maintenance unit (CMU) of the can report the link states and link data transfers to the MSP.

Functional blocks

The NT9X15AA has the following functional blocks:

- bus drivers/receivers
- first-in first-out (FIFO) interface
- access control
- buffer
- bus access circuit (BAC)
- FIFO
- card maintenance unit (CMU)
- link handlers (LH)
- connection memory (CNM)

Bus drivers/receivers

This block drives and receives messages from the T-bus and processor bus (P-bus) to the buffer, BACs and FIFO interface.

First-in first-out interface

This block provides an interface from the buses to the FIFO.

Access control

This block controls access to and from the buses.

Buffer

The buffer provides temporary storage and performs rate conversion. The buffer holds a single message a maximum of 1 kbyte long.

Bus access circuit

The BAC unit provides temporary storage of messages. The BAC unit stores the messages from the time that the messages are present on the link. The BAC stores the messages until the time the message are switched over to the T-bus. The BAC handles most of the T-bus protocol.

First-in first-out

The FIFO provides temporary storage and performs the rate conversion. The FIFO unit can hold any number of messages until the total space required exceeds 8 kbytes.

Card maintenance unit

The CMU is an on-card maintenance unit. The CMU monitors and reports error conditions, and configures the card, gate arrays and the connection memory. The CMU is an on-card processor that the MSP uses to perform tasks more quickly and easily. The CMU is based on an 8031 microcontroller.

Link handlers

The LH maintains and explains the protocol of the link. The LH is the interface between the link data protocol and the rest of the MS. The LH is the translator between the link data protocol and a generic form of the message that the MS uses.

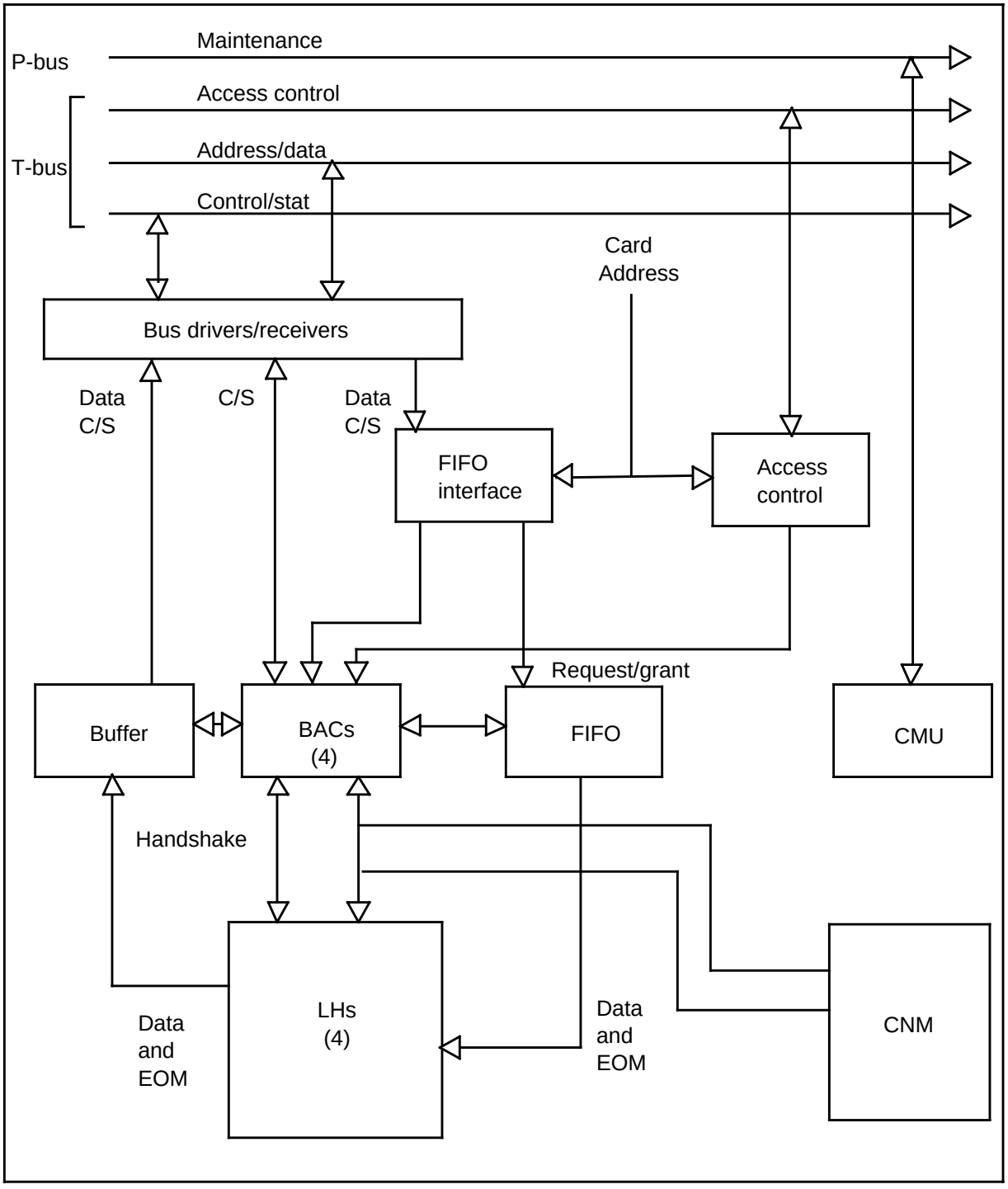
Connection memory

The CNM block enables the different ports on the card to allow the ports to correspond to the port link bandwidth. The CNM is a RAM that a counter addresses. The count reflects the current channel in the frame. The CMU updates the locations in this RAM.

The relationship between these functional blocks appears in the following figure.

NT9X17AA (continued)

NT9X15AA functional blocks



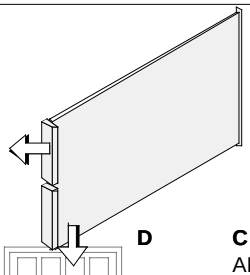
Signaling

Pin numbers

The pin numbers for NT9X15AA appear in the following figure.

NT9X17AA (continued)

NT9X15AA pin numbers



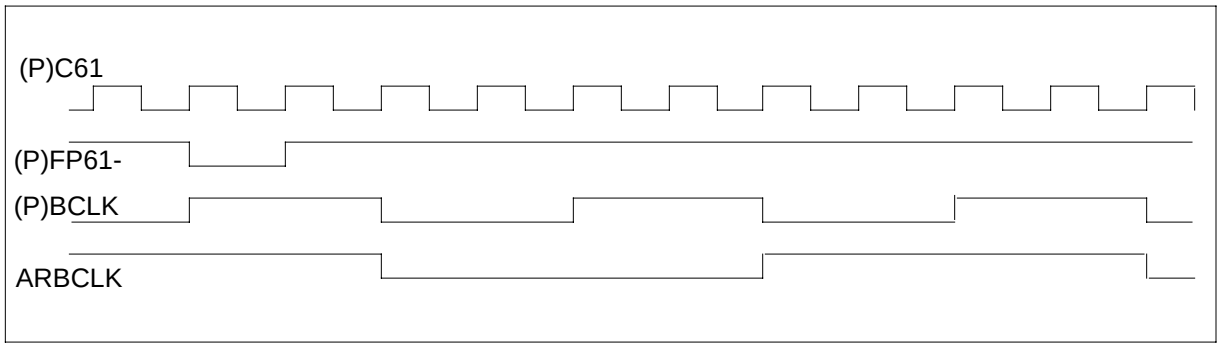
	D	C	B	A
1	IP0	AD37	ADD00	GND
2	OP0	ADP3	ADD01	GND
3	IP1	ADREN	ADD02	GND
4	OP1	DATEN	ADD03	GND
5	IP2	EOS	ADD04	GND
6	OP2	NVB0	ADD05	GND
7	IP3	NVB1	ADD06	GND
8	OP3	POK	ADD07	GND
9	SEG-0	BNF	ADP0	GND
10	SEG-1	SRCEN		GND
11	SEG-2	DSTEN		GND
12	SEG-3	REQ-		GND
13	SEG-4	GRT-		PENB-
14		INH-		PWRT-
15				PDTACK-
16				
17	PERINT6-	BUSGRI-		PADDR00
18	PERINT7-	BUSGRO-	ADP1	PADDR01
19			AD20	PADDR02
20			AD21	PADDR03
21		PERINT4-	AD22	
22		PERINT5-	AD23	PADDR04
23			AD24	PADDR05
24			AD25	PBID0
25	BEN1-	BEN0-	AD26	
26	BEN3-	BEN2-	AD27	
27			ADP2	
28	WRT-		AD30	PBID1
29	PARITY+	DTACK-	AD31	HW4
30			AD32	
31	PRTYEN-		AD33	
32			AD34	SH0
33			AD35	SH1
34			AD36	
35				
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5V
45		ADDR11		+5V

	D	C	B	A
46		ADDR12		+5V
47		ADDR13		+5V
48		ADDR14		+5V
49		ADDR15		+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21		+5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		STDA0
60	DATA26	ADDR26		STDA1
61	DATA27	ADDR27		STDA2
62	DATA28	ADDR28		STDA3
63	DATA29	ADDR29		STDA4
64	DATA30	ADDR30		STDA5
65	DATA31	ADDR31		STDA6
66				STDA7
67				
68				
69				SRDA0
70				SRDA1
71				SRDA2
72				SRDA3
73				SRDA4
74				SRDA5
75				SRDA6
76				SRDA7
77				
78			PDATA00	GND
79			PDATA01	GND
80			PDATA02	GND
81			PDATA03	GND
82			PDATA04	GND
83			PDATA05	GND
84			PDATA06	GND
85			PDATA07	GND
86			PDATA08	GND
87			PDATA09	GND
88			PDATA10	GND
89			PDATA11	GND
90				

Timing

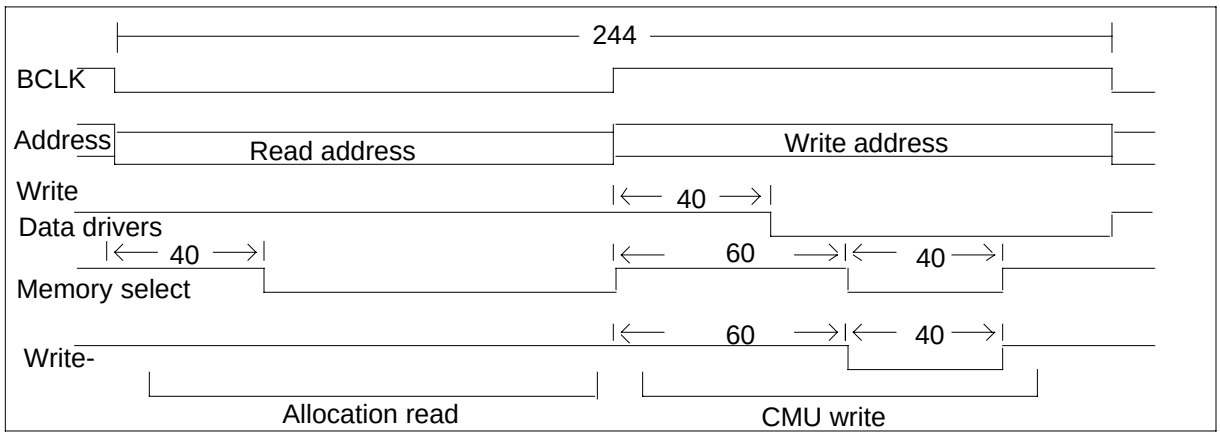
The clock signal timing relationships appear in the following figure.

NT9X15AA clock signal relationships



The RAM control signal timing appears in the following figure.

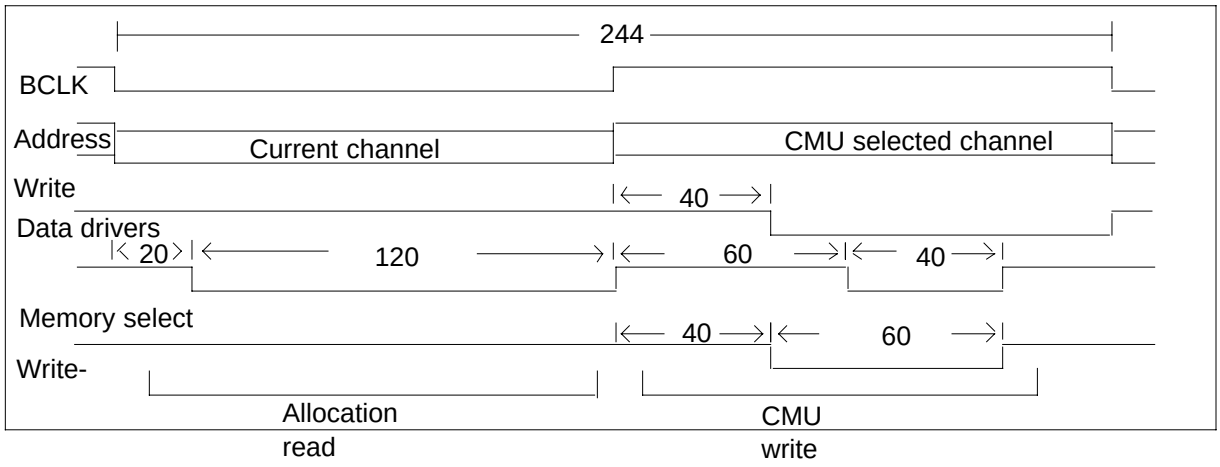
NT9X15AA RAM control signal timing (time is in ns)



The CNM RAM cycle with CMU write timing appears in the following figure.

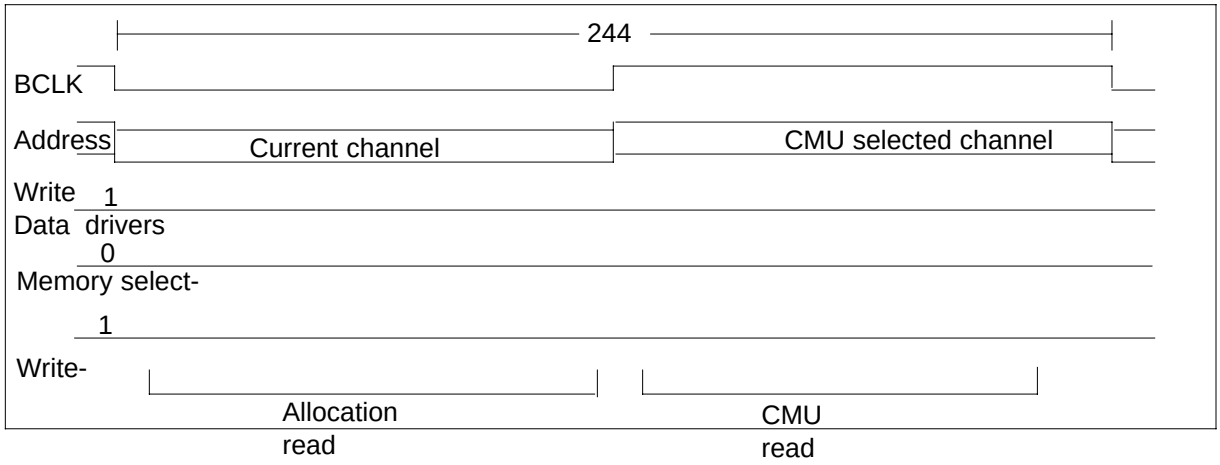
NT9X17AA (end)

NT9X15AA CNM RAM cycle with CMU write (time is in ns)



The CNM RAM cycle with CMU read timing appears in the following figure.

NT9X15AA CNM RAM cycle with CMU read (time is in ns)



Technical data

Power requirements

The NT9X15AA requires +5 V and 3 A of power to function.

NT9X17AC

Product description

The NT9X17AC message switch four-port card provides a data path for messaging. The data path occurs between the message switch (MS) and four subrate (SR512) optical links. The and the NT9X62BA paddle board provide the interface with the fiberized link interface unit shelf (FLIS).

Location

The NT9X17AC is in the MS processor shelf.

Functional description

The NT9X17AC transfers messages between four SR512 links and the transaction bus (T-bus). The T-bus is a packet switch. The T-bus connects data links to any port of the MS or to the message switch processor (MSP). The provides diagnostic capabilities through the NT9X17AC card maintenance unit (CMU). The CMU reports on the link states and the link data transfers to the MSP.

Functional blocks

The NT9X17AC has the following functional blocks:

- bus drivers and receivers
- first-in first-out (FIFO) interface
- access control block
- bus access circuit (BAC)
- buffer block
- FIFO block
- card maintenance unit (CMU)
- link handlers (LH)
- connection memory (CNM)

Bus drivers and receivers

The bus drivers and receivers handle the transfer of messages (data, control and status information). The messages transfer from the T-bus to the buffer, the BAC and the FIFO interface blocks.

FIFO interface

The FIFO interface block provides an interface for the messages from the T-bus to the FIFO.

NT9X17AC (continued)

Access control block

This block performs bus arbitrates for the T-bus.

BAC

The BAC unit (one for each link) provides temporary storage for messages. The BAC unit provides storage from the time the message are present on the SR512 link. The BAC stores the messages until the time the messages switch over to the T-bus. The BAC handles most of the T-bus protocol.

buffer block

The buffer block provides temporary storage and rate conversion for a single message that goes from the SR512 link to the T-bus. The message can be a maximum of 2 kbytes long.

FIFO block

The FIFO provides temporary storage and rate conversion in the opposite direction of the buffer block. The direction is from the T-bus to the SR512 link. The FIFO can hold any number of messages at a time if the following condition applies. The combined storage required must be equal to or less than 8 kbytes.

CMU

The CMU monitors and reports to the MS maintenance processor (MSP) on the link states and link data transfers. The MSP uses the CMU to handle error conditions and to configure the card, the gate arrays, and the connection memory.

LH

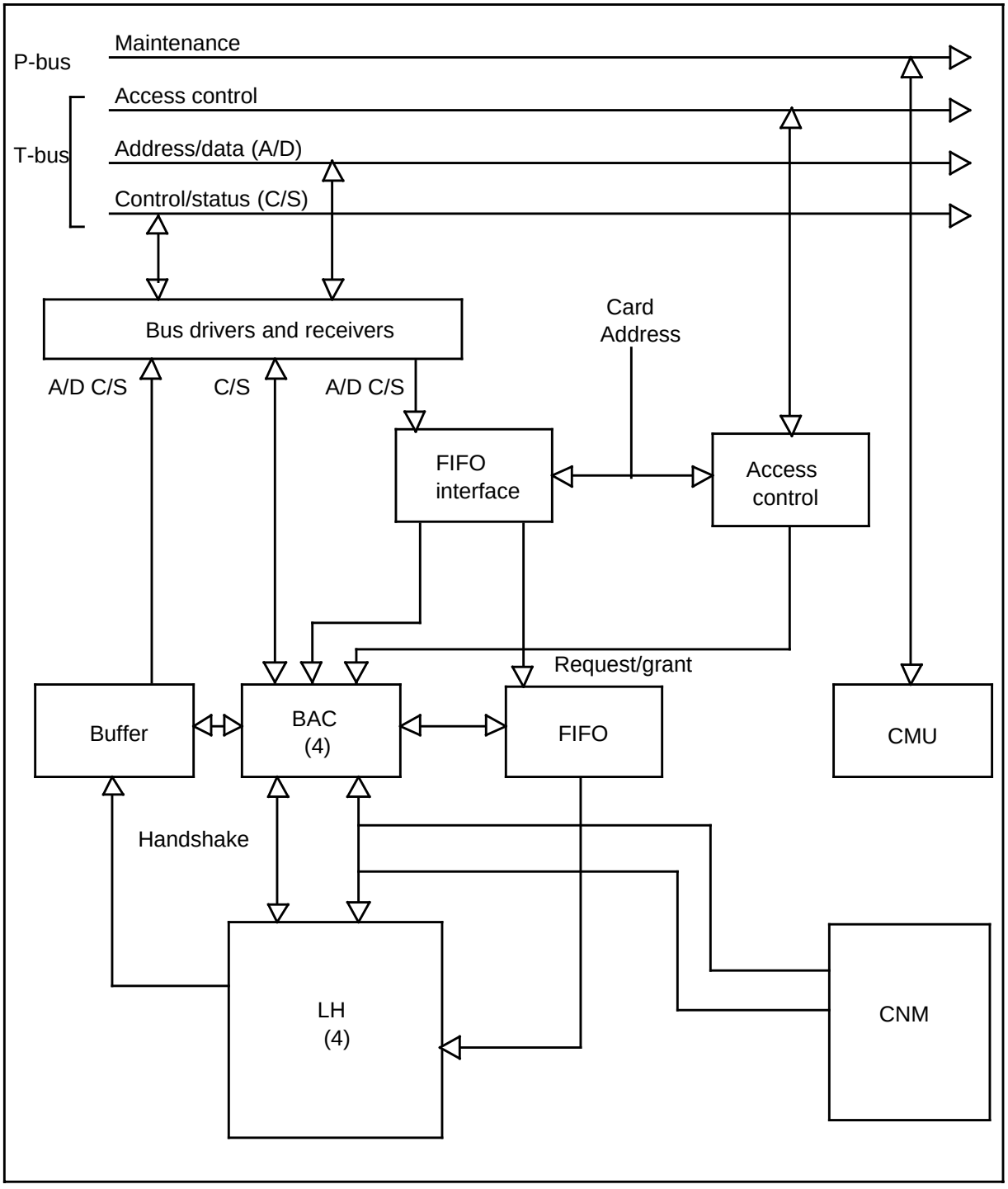
The LH (one for each link) maintains and explains the protocol of the link. The LH provides translation between the link data protocol and the generic form of the message that the rest of the MS uses. The LH replaces the control words that the link protocol uses. The LH replaces the control words with control signals that the BAC can explain.

CNM

The CNM block provides link data transfer rate conversion. The CNM is a RAM that a counter addresses. The count reflects the current channel in the frame. The CMU updates the locations in the CNM.

The relationship between the functional blocks appears in the following figure.

NT9X17AC functional blocks



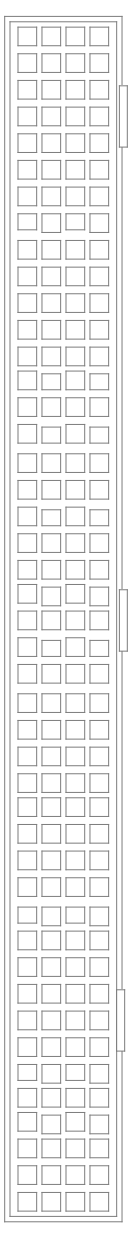
NT9X17AC (continued)

Signaling

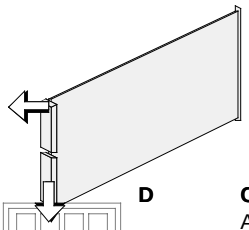
Pin numbers

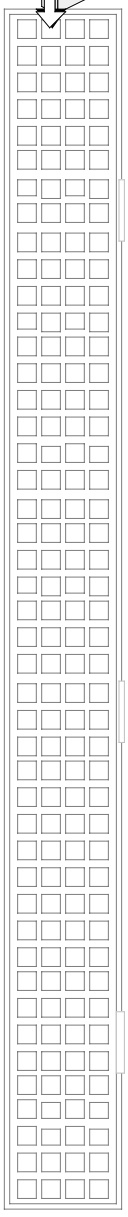
The pin numbers for the NT9X17AC appear in the following figure.

NT9X17AC pin numbers



	D	C	B	A
1	IP0	AD37	ADD00	GND
2	OP0	ADP3	ADD01	GND
3	IP1	ADREN	ADD02	GND
4	OP1	DATEN	ADD03	GND
5	IP2	EOS	ADD04	GND
6	OP2	NVB0	ADD05	GND
7	IP3	NVB1	ADD06	GND
8	OP3	POK	ADD07	GND
9	SEG0–	BNF	ADP0	GND
10	SEG1–	SRCEN	AD10	GND
11	SEG2–	DSTEN	AD11	GND
12	SEG3–	REQ–	AD12	GND
13	SEG4–	GRT–	AD13	PENB–
14		INH–	AD14	PWRT–
15			AD15	PDTACK–
16			AD16	PBLCK
17	PERINT6–	BUSGRI–	AD17	PADDR00
18	PERINT7–	BUSGRO–	ADP1	PADDR01
19			AD20	PADDR02
20			AD21	PADDR03
21		PERINT4–	AD22	DREN–
22		PERINT5–	AD23	PADDR04
23			AD24	PADDR05
24			AD25	PBID0
25	BEN1–	BEN0–	AD26	CPID
26	BEN3–	BEN2–	AD27	PFP61–
27			ADP2	STEN–
28	WRT–		AD30	PBID1
29		DTACK–	AD31	HW4
30	PARITY+		AD32	
31	PRTYEN–		AD33	
32			AD34	SH0
33	DAS32–		AD35	SH1
34			AD36	FP61–
35				C61
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5V
45		ADDR11		+5V





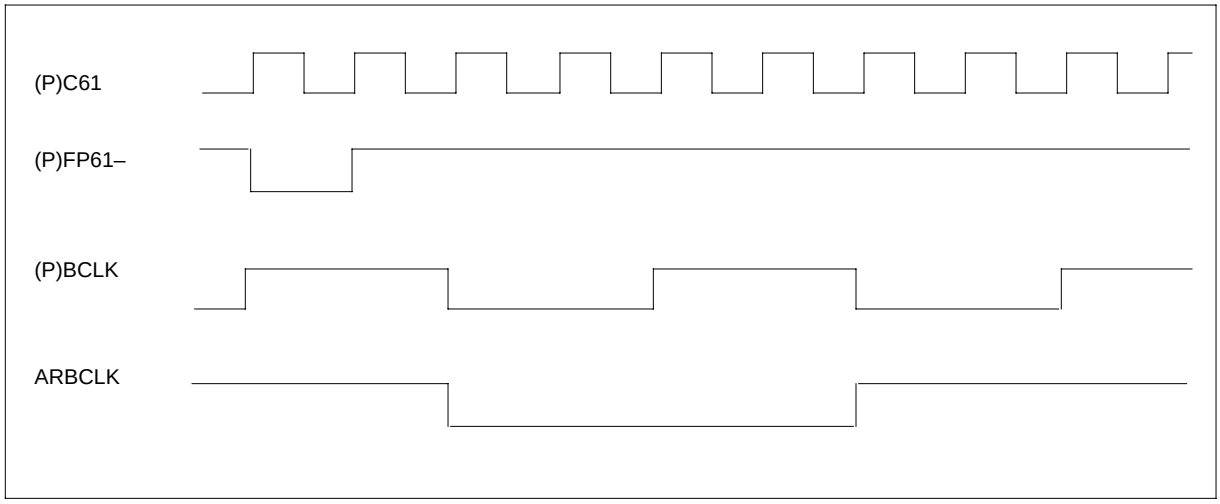
	D	C	B	A
46		ADDR12		+5V
47		ADDR13		+5V
48		ADDR14		+5V
49		ADDR15		+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21		+5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		LTVL
58	DATA24	ADDR24		LRVL
59	DATA25	ADDR25		STDA0
60	DATA26	ADDR26		STDA1
61	DATA27	ADDR27		STDA2
62	DATA28	ADDR28		STDA3
63	DATA29	ADDR29		STDA4
64	DATA30	ADDR30		STDA5
65	DATA31	ADDR31		STDA6
66				STDA7
67				
68				
69				SRDA0
70				SRDA1
71				SRDA2
72				SRDA3
73				SRDA4
74				SRDA5
75				SRDA6
76				SRDA7
77				
78				
79			PDATA00	GND
80			PDATA01	GND
81			PDATA02	GND
82			PDATA03	GND
83			PDATA04	GND
84			PDATA05	GND
85			PDATA06	GND
86			PDATA07	GND
87			PDATA08	GND
88			PDATA09	GND
89			PDATA10	GND
90	PC61		PDATA11	GND

NT9X17AC (continued)

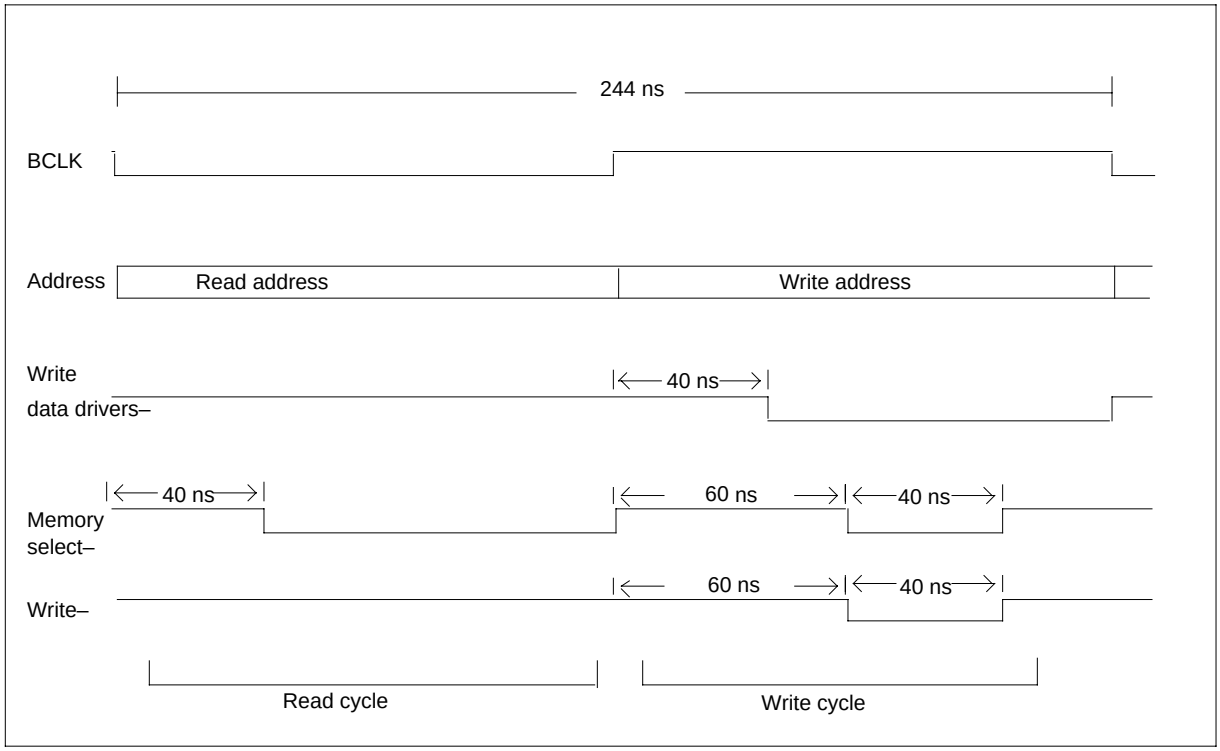
Timing

The timing for NT9X17AC appears in the following figure.

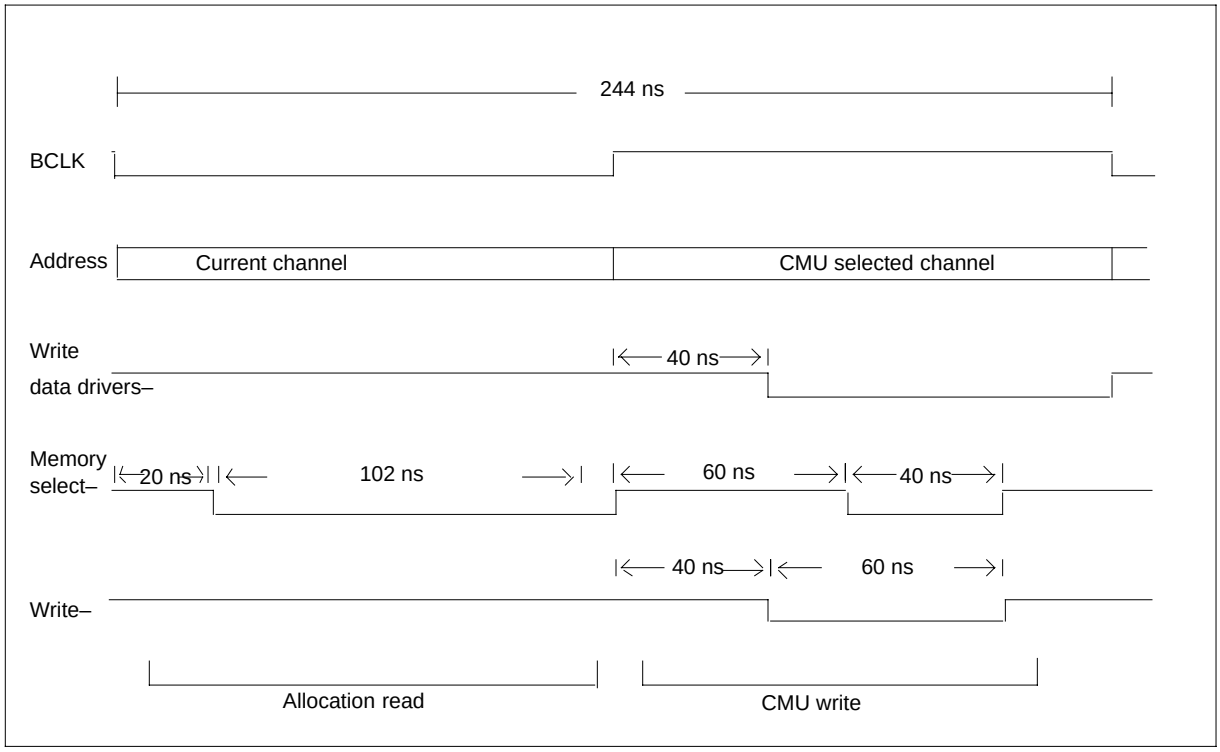
NT9X17AC clock signal relationships



NT9X17AC RAM control signals

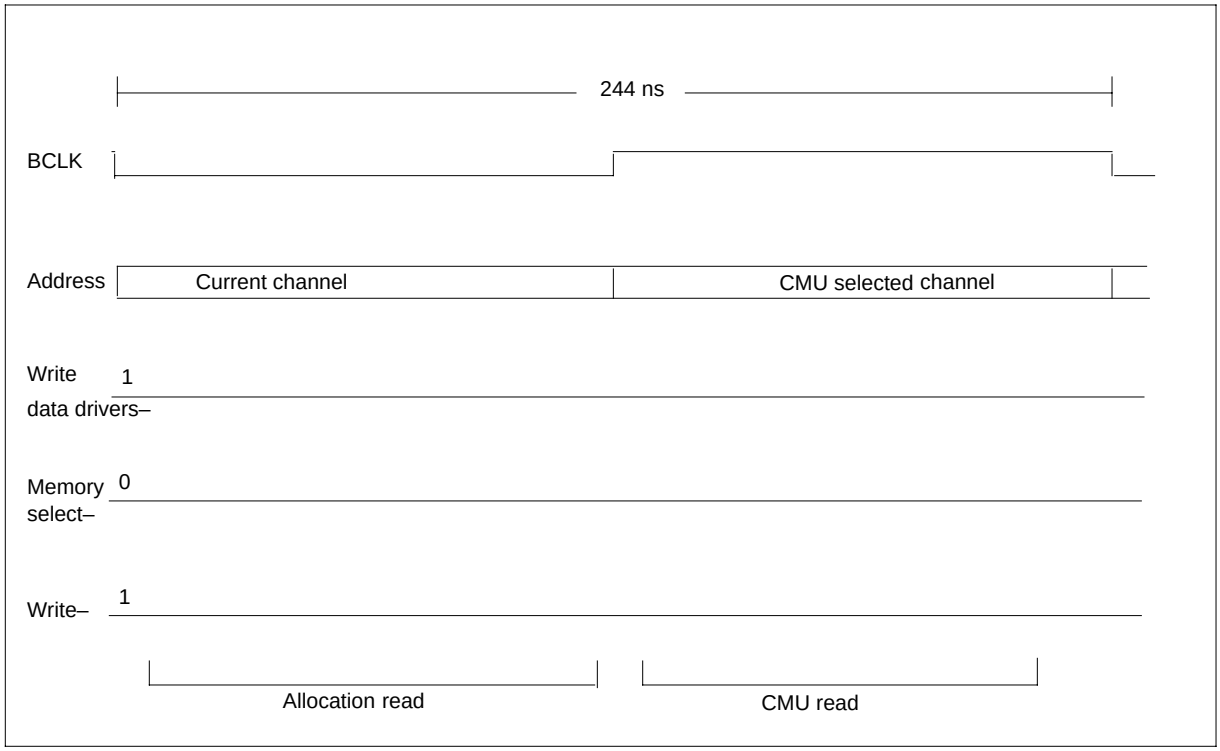


NT9X17AC CNM RAM cycle with CMU write



NT9X17AC (end)

NT9X17AC CNM RAM cycle with CMU read



Technical data

Power requirements

The minimum supply voltage for the NT9X17AA is 5V and the minimum supply current is 3A.

NT9X17AD

Product description

The NT9X17AD message switch (MS) four-port card provides a data path for messaging between the MS and four external links. The NT9X17AD is the same circuit card as the NT9X17AA with firmware, hardware and pin location changes.

The firmware is updated to provide compatibility with the NT9X62BA SR512 paddle board. The PROM for the firmware increases from 8 kbytes to 32 kbytes to allow for additional expansion.

Hardware is added to the NT9X17AD to allow the card to support the NT9X62BA card. The NT9X62BA card operates in one of the following configurations:

- 4 ports that operate at the SR218 rate
- 2 ports that operate at the SR256 rate
- 1 port that operates at the SR512 rate

The system clock C61 pin changes from pin 25A to pin 90D. This change allows the pack to function with the NT9X62BA. Pin 25A is now grounded to provide a mode pin for the NT9X62BA for link timing purposes.

The NT9X17AD uses the N04C single port bus access circuit (BAC).

The NT9X17AD is backward compatible with the NT9X17AA. All current applications use the NT9X17AD.

Location

The NT9X17AD card fits in slots 12 to 31 in all MS shelves of SuperNode. This card also fits in slots 8, 9, 29 and 30 of local message switch (LMS) shelves.

Functional description

The NT9X17AD transfers messages between four data links and the transaction bus (T-bus). The T-bus is a packet switch. The packet switch connects data links to any port on the MS or to the message switch processor (MSP).

NT9X17AD (continued)

The links can be one of the following physical types:

- DS30
- DS512
- SR512

The links can be one of the following logical types:

- DS30
- DMS-X
- DMS-Y
- Framer

The NT9X17AD reports the status of the links and link data transfers the MSP.

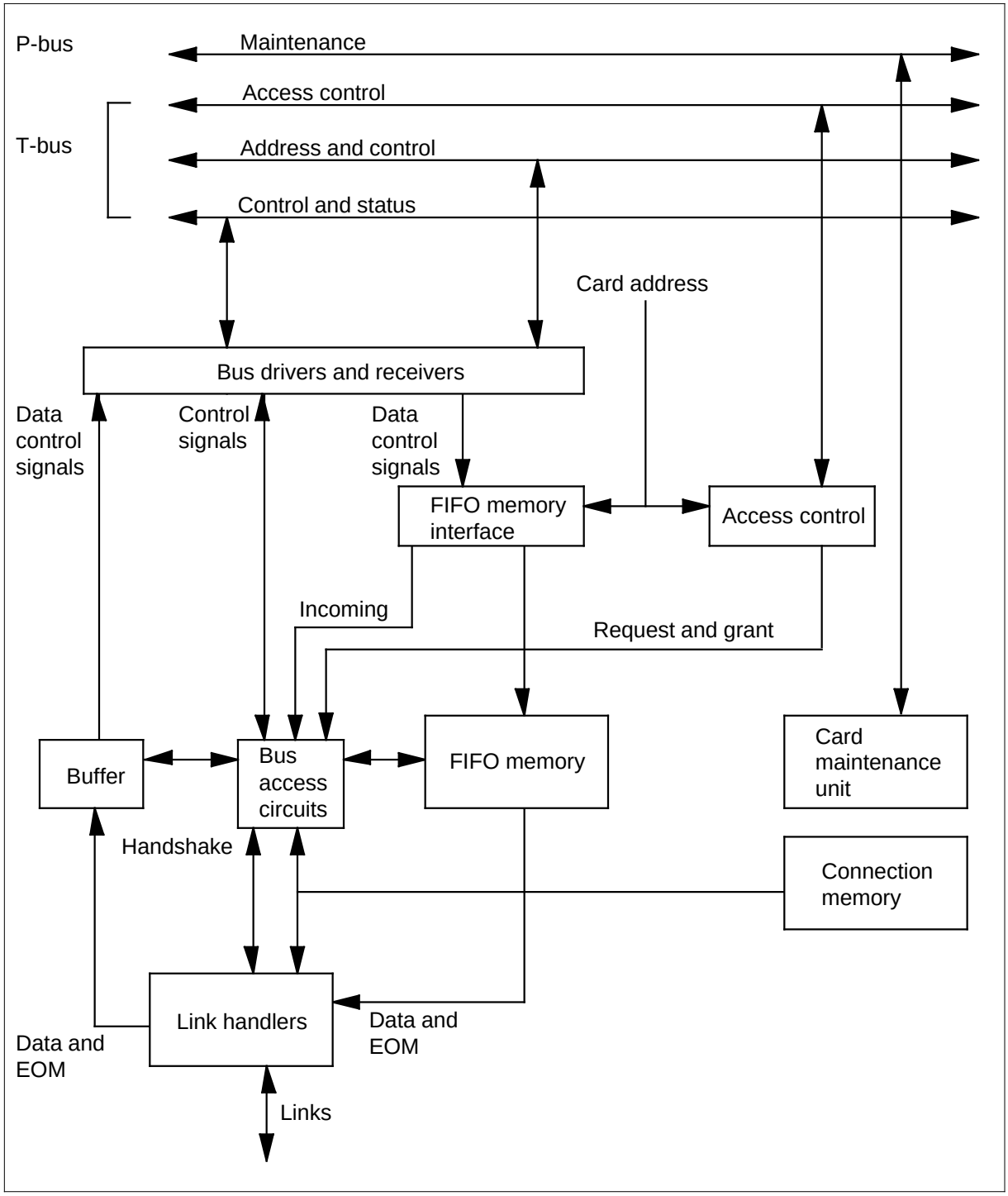
Functional blocks

The NT9X17AD has the following functional blocks:

- card maintenance unit (CMU)
- connection memory (CM)
- bus access circuit (BAC)
- buffer
- link handler (LH)
- access control
- bus drivers and receivers
- first-in first-out (FIFO) memory
- FIFO memory interface

The relationship between the functional blocks appears in the following figure.

NT9X17AD functional blocks



NT9X17AD (continued)

Card maintenance unit

The CMU monitors and reports error conditions. The CMU configures the card, gate arrays and the connection memory. The CMU is an on-card processor that the MSP uses to perform tasks quickly and easily.

The CMU is based on an 8031 microcontroller. The CMU connects to two buses. The CMU connects a synchronous bus to the programmable ROM and data RAM of the CMU. The CMU also connects to the processor bus (P-bus). The MSP controls the P-bus.

Connection memory

The connection memory is a RAM that keeps count of the current channel in the frame. This count allows the ports on the card to correspond to the link bandwidth of the channel. The CMU updates the RAM locations.

Bus access circuit

The BAC gate array provides temporary storage of messages. The BAC stores messages between the time the messages arrive on the link and the time these messages switch to the T-bus. When the message moves from the link to the T-bus, a buffer stores the message. When the message moves from the T-bus to the link, a FIFO stores the message. The BAC handles most of the T-bus protocol. The arbitrator handles some aspects of T-bus protocol.

Buffer

The buffer is a 16-KByte block of static RAM. This buffer stores data that comes from the link through the LH. The BAC transmits the data to the T-bus. The BAC supplies the address and chip selection for the memory.

Link handler

The LH is the interface between the link data protocol and the rest of the MS. The LH handles all the protocol of the link. The LH checks and generates the cyclic redundancy check (CRC) or checksum when necessary.

Access control

The BAC provides the access control to read from and write to the buffer memory and the FIFO memory. This control includes addresses, chip selection and different control signals.

Bus drivers and receivers

The bus drivers and receivers latch data and control the direction of the data transfer.

First-in first-out memory

The FIFO memory block stores incoming data from the T-bus. The LH reads the data and transmits the data to the link.

FIFO memory interface

The FIFO memory interface is a RAM-implemented circular buffer. This interface receives data from the T-bus and transfers the data to the link. The BAC provides the addresses for the memory.

Signaling

All signals on the NT9X17AD use standard transistor-transistor-logic (TTL) voltage levels.

Pin numbers

The pin numbers for NT9X17AD appear in the following figures.

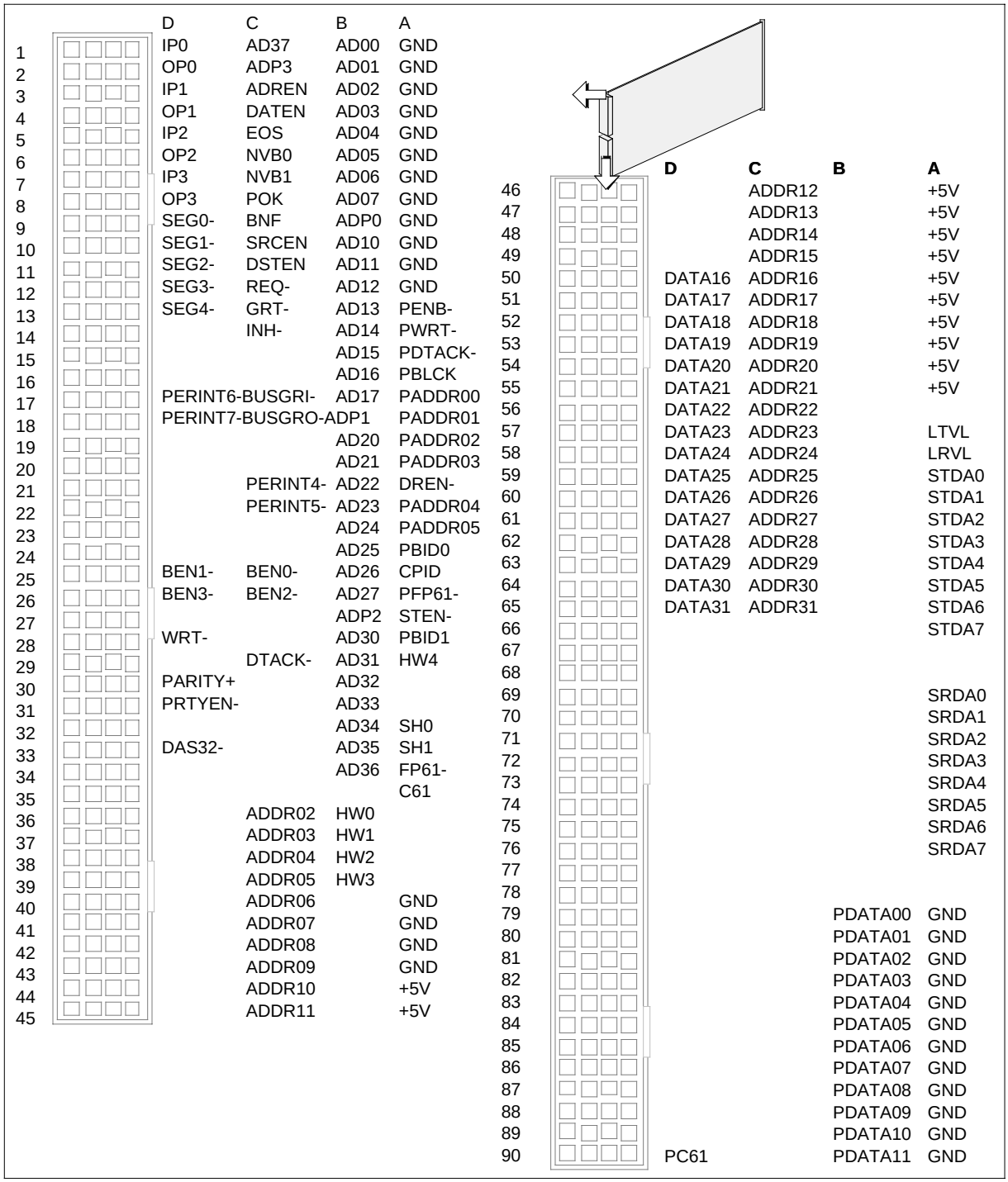
Technical data

Power requirements

The NT9X17AD requires a voltage of +5V and 3A of current.

NT9X17AD (end)

NT9X17AD pin numbers



	D	C	B	A
1	IP0	AD37	AD00	GND
2	OP0	ADP3	AD01	GND
3	IP1	ADREN	AD02	GND
4	OP1	DATEN	AD03	GND
5	IP2	EOS	AD04	GND
6	OP2	NVB0	AD05	GND
7	IP3	NVB1	AD06	GND
8	OP3	POK	AD07	GND
9	SEG0-	BNF	ADP0	GND
10	SEG1-	SRCEN	AD10	GND
11	SEG2-	DSTEN	AD11	GND
12	SEG3-	REQ-	AD12	GND
13	SEG4-	GRT-	AD13	PENB-
14		INH-	AD14	PWRT-
15			AD15	PDTACK-
16			AD16	PBLCK
17	PERINT6-	BUSGRI-	AD17	PADDR00
18	PERINT7-	BUSGRO-	ADP1	PADDR01
19			AD20	PADDR02
20			AD21	PADDR03
21		PERINT4-	AD22	DREN-
22		PERINT5-	AD23	PADDR04
23			AD24	PADDR05
24			AD25	PBID0
25	BEN1-	BEN0-	AD26	CPID
26	BEN3-	BEN2-	AD27	PFP61-
27			ADP2	STEN-
28	WRT-		AD30	PBID1
29		DTACK-	AD31	HW4
30	PARITY+		AD32	
31	PRTYEN-		AD33	
32			AD34	SH0
33	DAS32-		AD35	SH1
34			AD36	FP61-
35				C61
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5V
45		ADDR11		+5V

	D	C	B	A
46		ADDR12		+5V
47		ADDR13		+5V
48		ADDR14		+5V
49		ADDR15		+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21		+5V
56	DATA22	ADDR22		
57	DATA23	ADDR23		LTVL
58	DATA24	ADDR24		LRVL
59	DATA25	ADDR25		STDA0
60	DATA26	ADDR26		STDA1
61	DATA27	ADDR27		STDA2
62	DATA28	ADDR28		STDA3
63	DATA29	ADDR29		STDA4
64	DATA30	ADDR30		STDA5
65	DATA31	ADDR31		STDA6
66				STDA7
67				
68				
69				SRDA0
70				SRDA1
71				SRDA2
72				SRDA3
73				SRDA4
74				SRDA5
75				SRDA6
76				SRDA7
77				
78				
79			PDATA00	GND
80			PDATA01	GND
81			PDATA02	GND
82			PDATA03	GND
83			PDATA04	GND
84			PDATA05	GND
85			PDATA06	GND
86			PDATA07	GND
87			PDATA08	GND
88			PDATA09	GND
89			PDATA10	GND
90	PC61		PDATA11	GND

NT9X17BB

Product description

The NT9X17BB has 32 logically independent ports. Each port corresponds to an individually addressable transaction bus (T-bus) transceiver. Each port can handle one logical message path. The port card uses two 4.096-MHz 8-bit data buses to connect to link interface paddle boards. The two buses are the shorting bus (S-bus). One 8-bit data bus carries transmit data from the port card to the paddle board. The other bus carries receive data from the paddle board to the port card. Each logical message path uses a collection of time slots on the S-bus. Each frame has 512 time slots. The 512 time slots allow between 1 and 512 time slots to be logically assigned to a message path that passes through a single port.

The NT9X17BB has the following features:

- 32 independent ports
- parity generated for data that the buffers store
- faster card maintenance unit (CMU) that allows the use of PROTEL code
- EEPROM for firmware storage that the shelf processor can update
- FIFO-based interface for communication between the CMU and shelf processor
- interface to the S-bus that allows the CMU to emulate the link side of a single messaging path
- double latching of incoming and outgoing S-bus data to guarantee margin
- tristate guard band on S-bus data transactions
- T-bus test features that include parity problems and forced loopbacks
- first-come first-served queue for ports that request access to the T-bus on each card
- signal that indicates buffer availability passed across the S-bus
- ability to configure buffers as FIFOs
- multiple port link handler (MPLH) DMS-Y loopback independent of the S-bus

Location

The S-bus connects the port card to the link interface paddle board. You can place the link interface paddle board in the slot directly opposite the card. The NT9X25AA and BA paddleboards can physically extend the S-bus. The NT9X25AA and BA paddle boards (MS port expander and terminator) allow multiple port boards to access a connected S-bus. Only one link interface paddle board can drive a single S-bus segment.

NT9X17BB (continued)

Functional description

Functional blocks

The NT9X17BB has the following functional blocks:

- clock generator (CLKGEN)
- processor bus (P-bus) interface
- CMU
- T-bus receiver
- T-bus-to-link buffer
- link-to-T-bus buffer
- T-bus driver
- connection memory
- T-bus arbitrator
- port control block
- S-bus interface
- message counter

Clock generator

The clock generator block generates timing signals derived from the 16-MHz backplane clock.

Processor bus interface

The P-bus interface block provides an interface from the backplane P-bus to the CMU, the EEPROM and the paddle board.

Card maintenance unit

The CMU block performs communication, configuration and maintenance.

Transaction bus receiver

The T-bus receiver block receives data from the T-bus and stores the data in the T-bus-to-link buffer.

Transaction bus-to-link buffer

The T-bus-to-link buffer block stores messages from the T-bus that the link receives.

Link-to-transaction bus buffer

The link-to-T-bus buffer block stores messages from the link that the T-bus receives.

Transaction bus driver

The T-bus driver block drives data from the link to T-bus buffer to the T-bus.

Connection memory

The connection memory block allocates S-bus time slots for the MPLH and multiple port bus access circuit (MPBAC).

Transaction bus arbitrator

The T-bus arbitrator block performs intercard and T-bus arbitration between shelves.

Port control

The port control block has one MPBAC and one MPLH. The MPBAC and the MPLH work together to control 32 logical ports. The block controls data transfers to and from the buffers. These data transfers include access to the T-bus and the S-bus.

Shorting bus interface

The S-bus interface block provides an interface between the MPLH and the S-bus, with provision for CMU access.

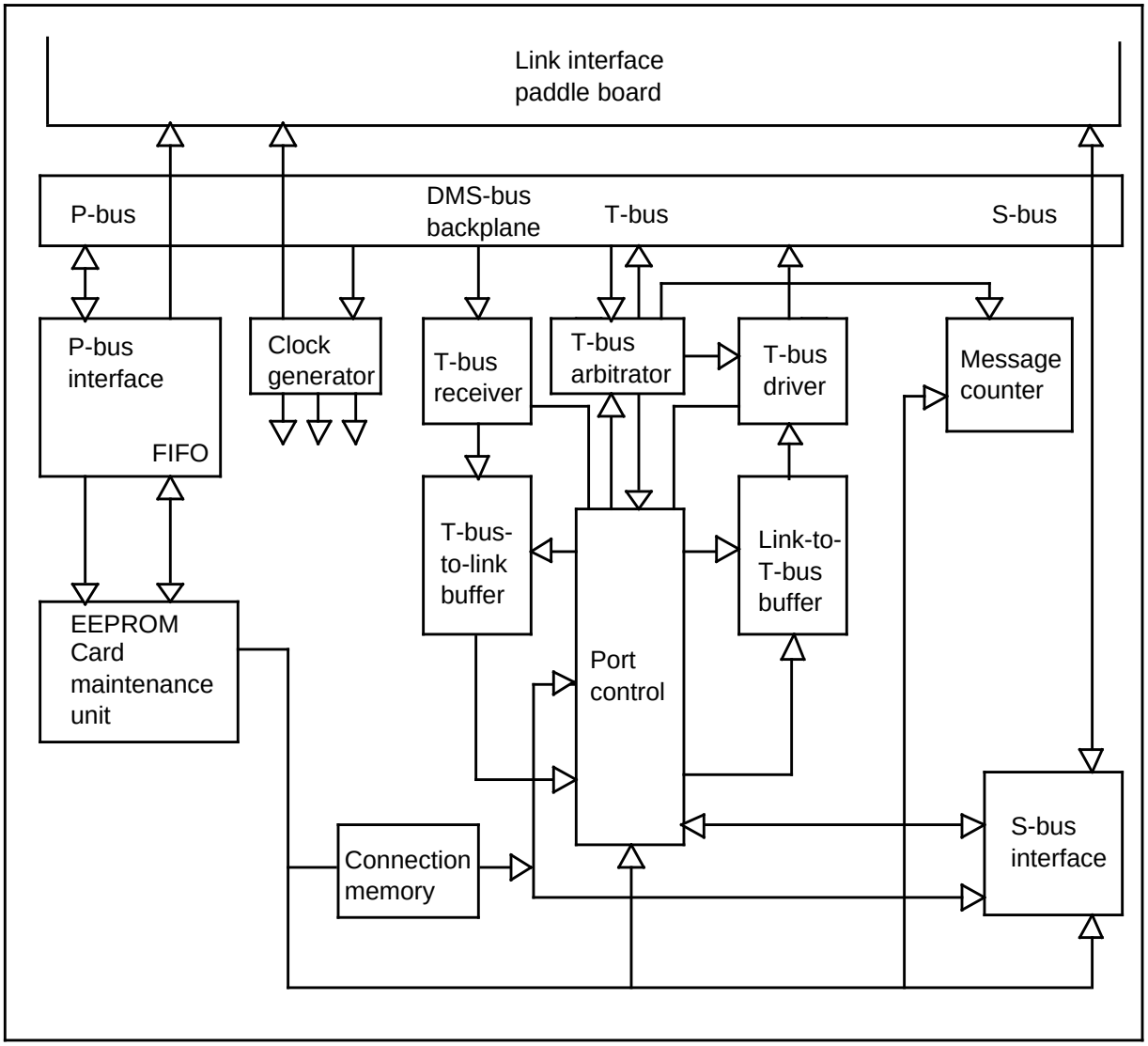
Message counter

The message counter block counts the messages that transmit on the T-bus for each port.

The relationship between the functional blocks appears in the following figure.

NT9X17BB (continued)

NT9X17BB functional blocks



Signaling

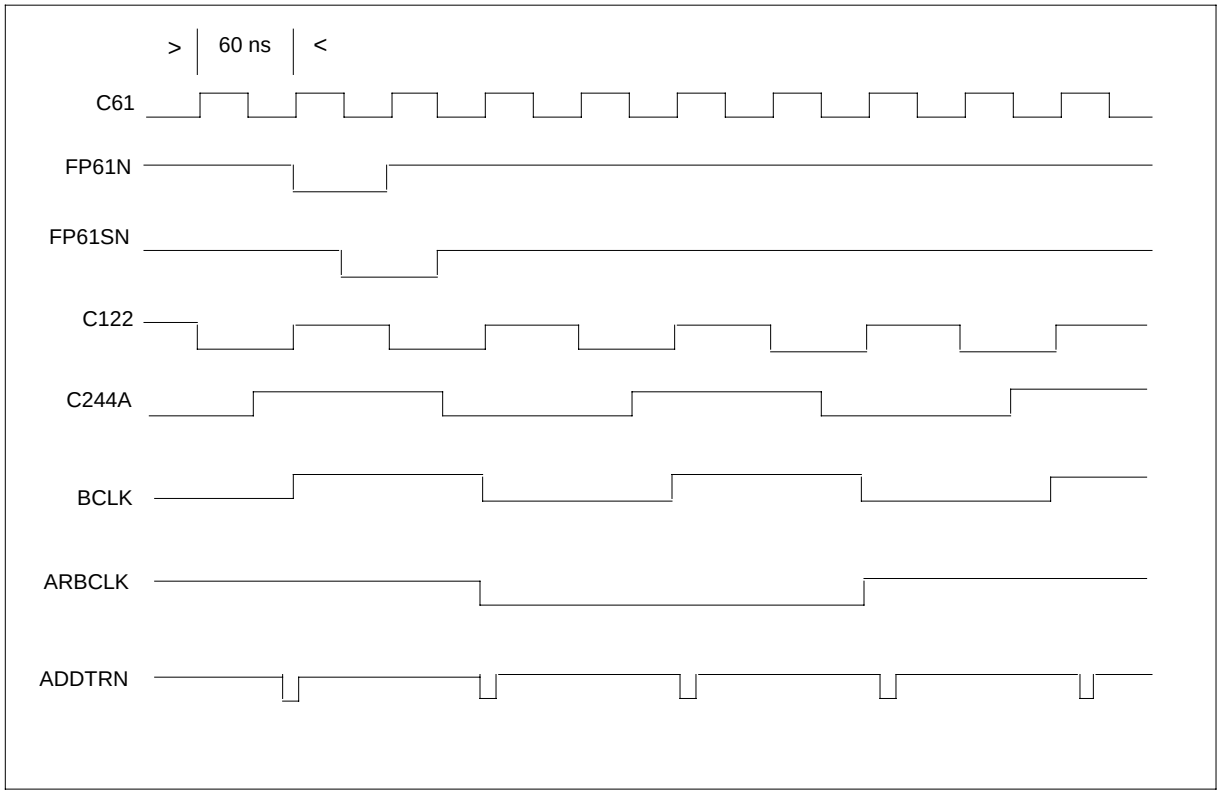
Pin numbers

The pin numbers for the NT9X17BB appear in the following figure.

Timing

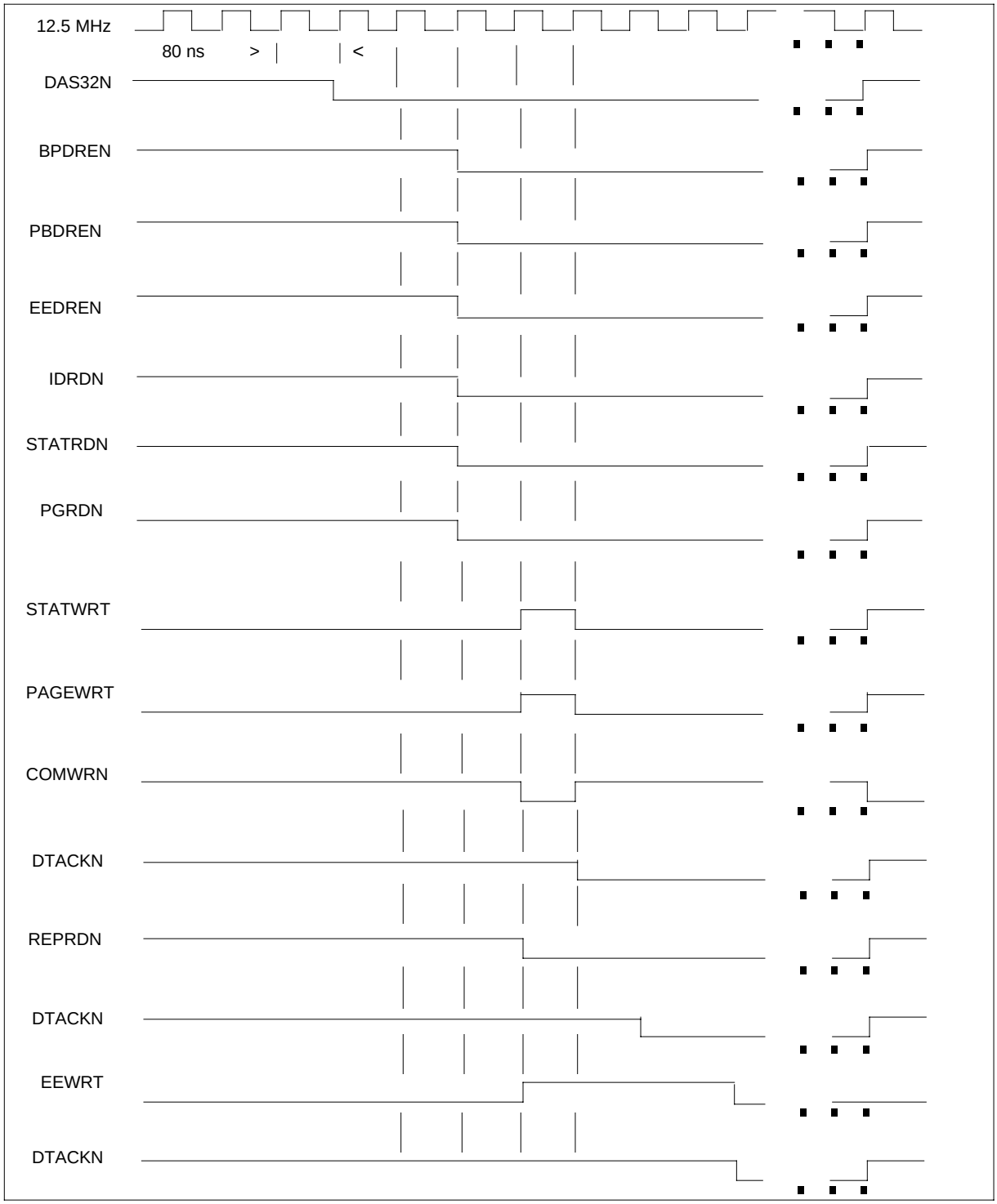
The timing diagrams for the NT9X17BB appear in the following figure.

NT9X17BB clock signal relationships

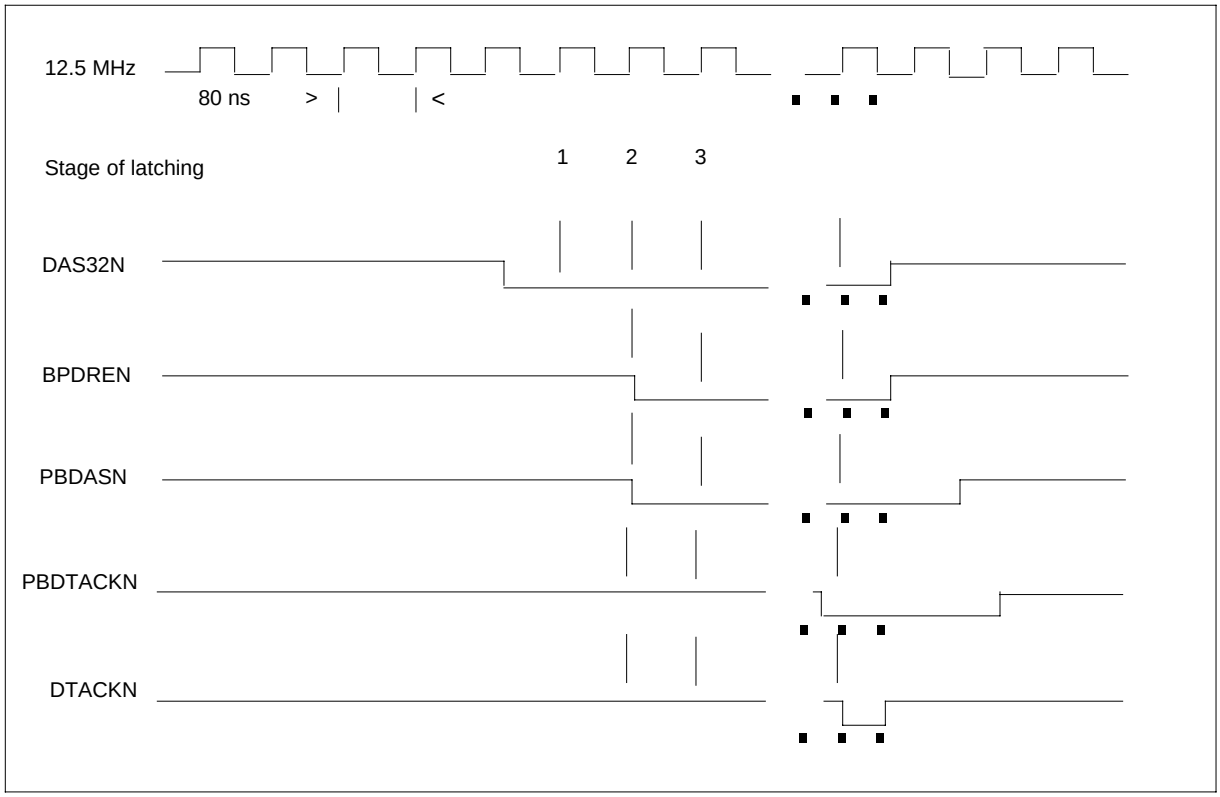


NT9X17BB (continued)

NT9X17BB P-bus timing relationships



NT9X17BB paddle board P-bus timing relationships



Technical data

Power requirements

The power requirements for the NT9X17B Bappear in the following table.

Power requirement

Parameter	Minimum	Nominal	Maximum
Supply voltage	4.75 V	5.0V	5.25V
Supply current		5.5A	

NT9X17CA

Product description

The NT9X17CA is a message switch port card that provides 128 ports on a single card. Each port acts as a separate entity on the T-bus. Each port sends and receives messages. The address of each port identifies each message. Each port represents a bidirectional messaging path. The T-bus provides a routing mechanism.

The NT9X17CA provides the following features:

- 128 separate ports
- parity generated for data that the buffers store
- faster, stronger card maintenance unit that allows code written in PROTEL
- EEPROMs for the card maintenance unit firmware storage that the shelf processor can update
- a first-in- first-out (FIFO) interface to allow communication between the card maintenance unit and the shelf processor
- an interface to the S-bus that allows the card maintenance unit to emulate the link side of a single messaging path
- double latching of incoming and outgoing S-bus data to guarantee enough margin
- a tristate guard band between S-bus data transactions to prevent contention
- T-bus test features that include parity problems and forced loopbacks
- a FIFO queue for ports that request access to the T-bus
- a signal that indicates buffer availability passed across the S-bus
- the capability to configure both buffers as FIFOs
- a FIFO to keep track of ports with babbling links

The NT9X17CA is compatible with current cards that access the T-bus. These cards include the following:

- NT9X15AA
- NT9X17AA
- NT9X17BB
- NT9X17DA
- NT9X29CB

- NT9X52AA
- NT9X49CB

Location

The NT9X17CA is in slots 12 to 31 in the message switch.

Functional description

The NT9X17CA provides the features of the 32-port NT9X17BB and 64-port NT9X17DA cards. The increase to 128 ports per card allows a great increase in density. In DMS SuperNode, the DMS-bus allows packets of data to route between DS30 or DS512 links. The links physically connect to the shelf. Paddle boards interface the physical links to the port cards. Port cards handle the link protocol and provide data buffering and interface to the high speed synchronous T-bus. A buffer stores data that arrives from the links. The system transfers this data across the T-bus to another port card. At this port, another buffer stores the data before the system transmits the data on a link.

Functional blocks

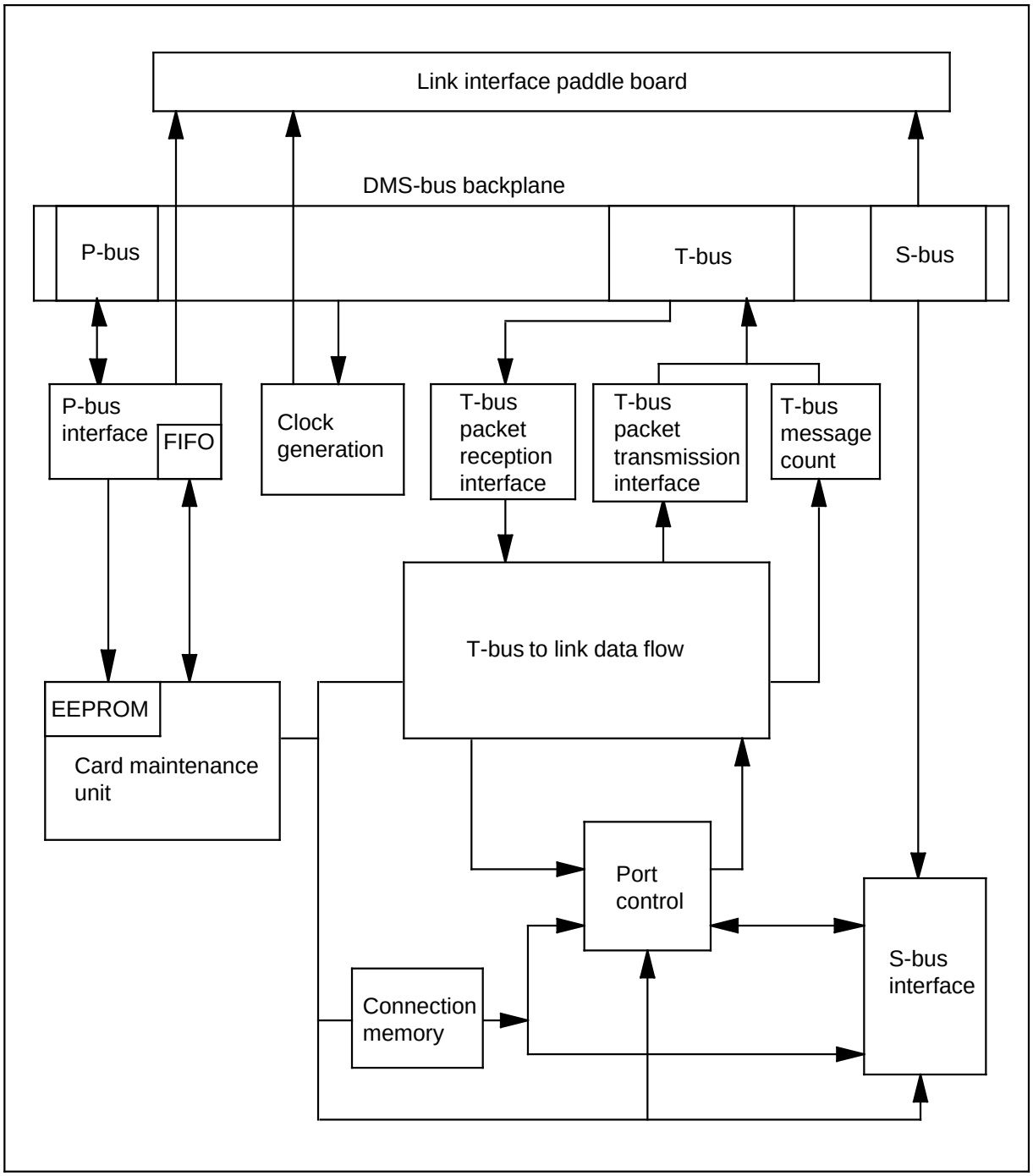
The NT9X17CA has the following functional blocks:

- clock generation
- P-bus interface
- card maintenance unit
- T-bus packet reception interface
- T-bus to link data flow
- T-bus packet transmission interface
- connection memory
- port control
- S-bus interface
- message counter, babbling port detector

The relationship between the functional blocks appears in the following figure.

NT9X17CA (continued)

NT9X17CA functional blocks



Clock generation

This block generates the timing signals the card uses. This block also generates signals required for timing the read-write accesses of the buffers. To make sure that clock drivers do not overload, this block drives several identical clock signals.

P-bus interface

This block provides the interface to the backplane P-bus. This block also buffers all P-bus signals before the system uses the signals on the card. The block contains the following P-bus related features:

- address decoding for all locations the P-bus can address
- buffering of address and data lines the card uses
- generation of the 16-bit slave response (DTACK)
- parity calculation on all P-bus accesses
- IDPROM access
- card maintenance unit messaging interface
- buffered paddle board interface
- access to the EEPROM firmware storage of the the card maintenance unit
- power on and reset control
- direct access to some test and control functions

Card maintenance unit

The card maintenance unit block initializes, controls and maintains the following:

- the multiple port link handler (MPLH)
- the multiple port bus access controller (MPBAC)
- the connection memory commutator (CMCX)

This block monitors the card for error conditions and signals the shelf processor when errors occur. The block tests sections of the card to determine if the hardware is fully functional.

T-bus packet reception interface

This block recognizes messages addressed to a port on the card. This block takes the data from the T-bus and presents the data to memory. The block performs these actions under the supervision of the multiport bus access circuit selected during the address cycle.

NT9X17CA (continued)

T-bus to link data flow

This block combines the link-to-T-Bus and T-Bus-to-link paths of the NT9X17BB/DA versions. In the NT9X17CA, all four MPBACs share buffer memory for both directions. The MPBACs share the memory to reduce power use and save space.

T-bus packet transmission interface

This block takes data from the link to T-bus path and drives this data to the backplane T-bus. This block buffers and times the signals again that go to the T-bus. This block drives 42 T-bus signals and receives two reply signals.

Connection memory

The connection memory block allocates time division multiplexed channels on the S-bus to separate ports on the port card. During each of the 512 channels that occur in a 125 microsecond frame, the system must provide valid port numbers and enables. The multiport bus access circuits and the multiport link handlers must have valid port numbers and enables. Two logical connection memories are present. One memory is for the link transmit direction. The other memory is for the link receive direction.

Port control

The port control block contains four multiport link handlers and four multiport bus access controller gate arrays. These eight gate arrays control the complete data path for 128 logical ports. The system pairs each MPBAC with an MPLH. The link side of the MPBAC receives an allocation. The output port select (OPS) receives an allocation of the corresponding MPLH at the same time.

S-bus interface

The S-bus interface block captures and transmits data on the S-bus to the correct block. This block provides a test access for the card maintenance unit.

Message counter

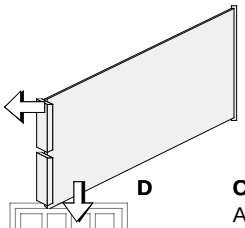
The message count block keeps track of the number of T-bus transmissions on each port. This action allows the system to shut down babbling links before DMS-bus port card overload. A bad maintenance action on the far end of the link to the peripheral can cause a babbling link. The system must detect babbling links and the connection to the associated port must be closed. When these actions do not occur, the babbling link will flood the buffer of the associated port with messages.

Signaling

Pin numbers

The pin numbers for the NT9X17CA appear in the following figure.

NT9X17CA pin numbers



	D	C	B	A
1	IP0	AD37	AD00	GND
2	OP0	ADP3	AD01	GND
3	IP1	ADREN	AD02	GND
4	OP1	DATEN	AD03	GND
5	IP2	EOSN	AD04	GND
6	OP2	NVB0	AD05	GND
7	IP3	NVB1	AD06	GND
8	OP3	POKN	AD07	GND
9	SEG0	BNFN	ADP0	GND
10	SEG1	SRCEN	AD10	GND
11	SEG2	DSTEM	AD11	GND
12	SEG3	REQN	AD12	GND
13	SEG4	GRTN	AD13	PBDASN
14		INHN	AD14	PBWRTN
15			AD15	PBACKN
16			AD16	PBBCLK
17			AD17	PDADD2
18			ADP1	PBADD3
19			AD20	PBADD4
20			AD21	PBADD5
21		PERINT4	AD22	PBSDREN
22			AD23	PBADD6
23	RSTOUTN	AD24	PBADD7	
24			AD25	PBID0
25	BEN1	BEN0	AD26	unused
26	BEN3	BEN2	AD27	PBFP61N
27	GND		ADP2	CPSDREN
28	WRTN	GND	AD30	PBID1
29		DTACKN	AD31	HW4
30	PARITY		AD32	
31	PARITYEN	AD33		
32		GND	AD34	SH0
33	DAS32N		AD35	SH1
34			AD36	FP61N
35				C61
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5
45		ADDR11		+5

	D	C	B	A
46		ADDR12		+5
47		ADDR13		+5
48		ADDR14		+5
49		ADDR15		+5
50	DATA16	ADDR16		+5
51	DATA17	ADDR17		+5
52	DATA18	ADDR18		+5
53	DATA19	ADDR19		+5
54	DATA20	ADDR20		+5
55	DATA21	ADDR21		+5
56	DATA22	ADDR22		
57	DATA23	ADDR23		LTVL
58	DATA24	ADDR24		LRVL
59	DATA25	ADDR25		STDA0
60	DATA26	ADDR26		STDA1
61	DATA27	ADDR27		STDA2
62	DATA28	ADDR28		STDA3
63	DATA29	ADDR29		STDA4
64	DATA30	ADDR30		STDA5
65	DATA31	ADDR31		STDA6
66				STDA7
67				STDA8
68				SRDA0
69				SRDA1
70				SRDA2
71				SRDA3
72				SRDA4
73				SRDA5
74				SRDA6
75				SRDA7
76				
77				
78				
79			PBDAT20	GND
80			PBDAT21	GND
81			PBDAT22	GND
82			PBDAT23	GND
83			PBDAT24	GND
84			PBDAT25	GND
85			PBDAT26	GND
86			PBDAT27	GND
87	PBID4		PBDAT28	GND
88	PBID3		PBDAT29	GND
89	PBID2		PBDAT30	GND
90	PBC61		PBDAT31	GND

NT9X17CA (continued)

Timing

Clock generation provides the timing signals the card uses. Clock generation also provides the signals required to time the read-write accesses of the buffers. The T-bus uses a 4.096-MHz clock called BCLK as a reference. The system generates this clock on each card that accesses the T-bus. The system creates the BCLK from the 16.384-MHz backplane clock (C61). The BCLK edges must have the relationship to the 61-ns frame pulse (FP61N).

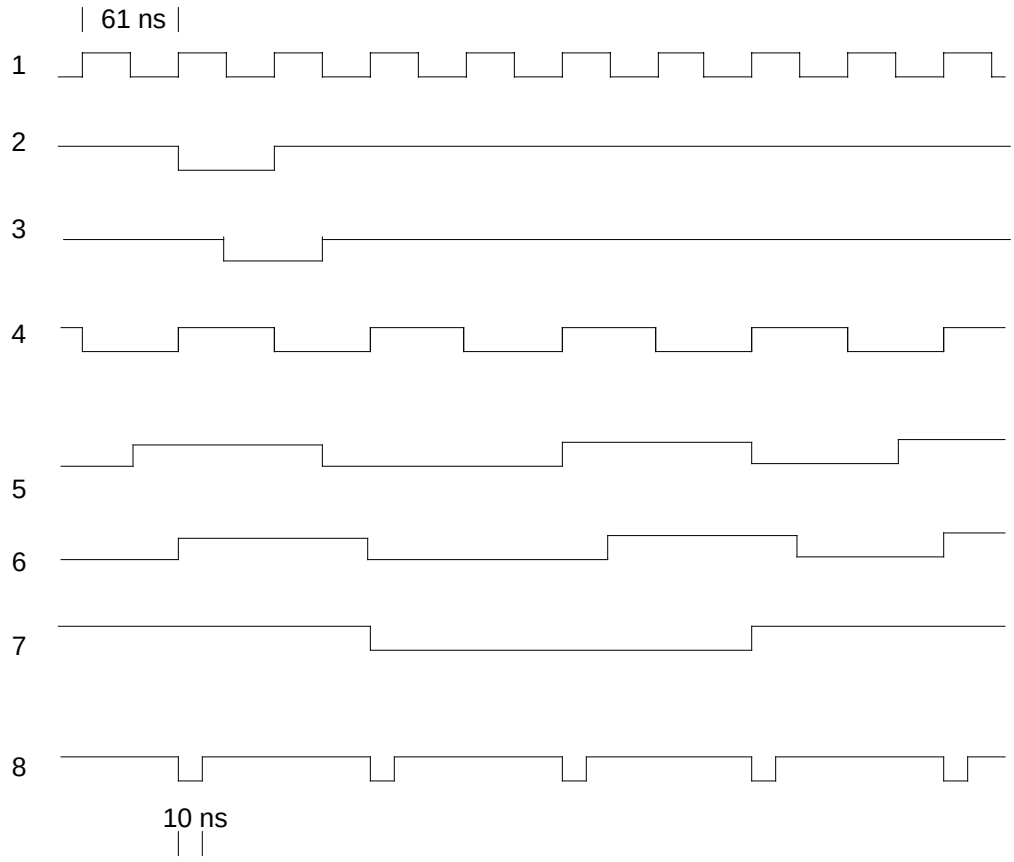
The timing for the NT9X17CA appears in the following figure.

Technical data

Power requirements

The NT9X17CA requires an electrical supply of +5 V.

NT9X17CA timing



LEGEND

1	C61	The 16.381-MHz backplane clock.
2	FP61N	The 61-nx frame pulse.
3	FP61SN	A timed again version of FP61 that the CMCX (R52) requires as a reference.
4	C122	A buffered 8MHz clock to time CNXMEM outputs again, access the arbitration FIFO and create enables on the S-bus.
5	C244A	A 4-MHz clock advanced a nominal 30 ns from BCLK.
6	BCLK	The 4.096-MHz clock that the T-bus uses.
7	ARBCLK	The TBUSTX uses this feature to resolve T-bus arbitration rounds.
8	ADDTRN	The PRTCTL uses this feature to tristate the address buses of the buffer between memory accesses.

NT9X17DA

Product description

The NT9X17DA has 64 logically separate ports. Each port corresponds to a separate addressable transaction bus (T-bus) transceiver. This transceiver can handle one logical message path. The port card uses two 4.096-MHz 8-bit data buses to connect to link interface paddle boards. These 8-bit data buses are the shorting bus (S-bus). One 8-bit data bus carries transmit data from the port card to the paddle board. The other bus carries receive data from the paddle board to the port card. Each logical message path uses a collection of time slots on the S-bus. One frame has 512 time slots. This condition allows the system to logically assign between 1 and 512 time slots to a message path. The message path passes through a single port.

The S-bus connects the port card to the link interface paddle board. You can place this board in the slot directly opposite the card. The NT9X25AA and BA paddle boards (MS port expander and terminator) can physically extend the S-bus. The BA paddle boards allow multiple port boards to access a connected S-bus. Only one link interface paddle board can drive a single S-bus segment.

The NT9X17DA card provides the features now available on the four-port NT9X17AA card. The NT9X17DA obtains greater functional density than the NT9X17AA. The NT9X17DA includes the following features:

- 64 separate ports
- parity generated for data stored in the buffers
- a faster card maintenance unit, that allows the use of PROTEL code
- EPROMs for firmware storage that the shelf processor can update
- a first-in-first-out (FIFO) interface for communication between the card maintenance unit and shelf processor
- an interface to the S-bus that allows the card maintenance unit to emulate the link side of a single messaging path
- double latching of incoming and outgoing S-bus data to guarantee margin
- a tristate guard band on S-bus data transactions
- T-bus test features that include parity problems and forced loopbacks
- a first-come first-served queue for ports that request access to the T-bus on each card
- a signal that indicates buffer availability passed across the S-bus
- the ability to configure both buffers as FIFOs
- multiple port link handler (MPLH) DMS-Y loopback independent of the S-bus

Functional description

Functional blocks

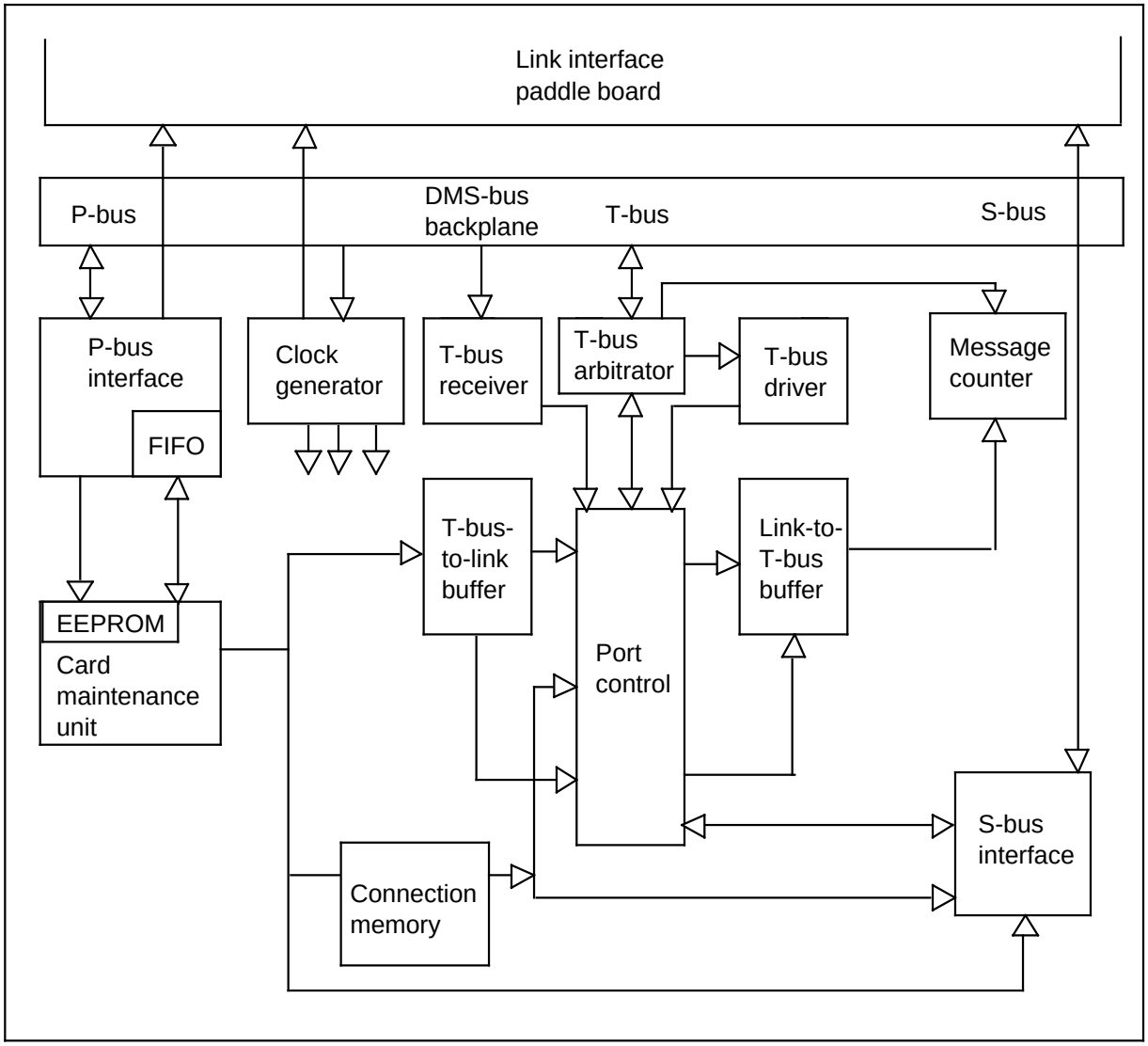
The NT9X17DA has the following functional blocks:

- clock generator (CLKGEN)
- processor bus (P-bus) interface
- card maintenance unit (CMU)
- T-bus receiver
- T-bus-to-link buffer
- link-to-T-bus buffer
- T-bus driver
- connection memory
- T-bus arbitrator
- port control block
- S-bus interface
- message counter

The functional relationship of these blocks appears in the following figure.

NT9X17DA (continued)

NT9X17DA functional blocks



Clock generator

This block generates timing signals derived from the 16-MHz backplane clock.

Processor bus interface

This block interfaces the backplane P-bus to the CMU, EPROM and paddle board.

Card maintenance unit

This block performs communication, configuration and maintenance.

Transaction bus receiver

This block receives data from the T-bus and stores the data in the T-bus-to-link buffer.

Transaction-bus-to-link buffer

This block stores messages from the T-bus that the link receives.

Link-to-transaction-bus buffer

This block stores messages from the link that the T-bus receives.

Transaction bus driver

This block drives data from the link to T-bus buffer to the T-bus.

Connection memory

This block allocates S-bus time slots for the MPLH and multiple port bus access circuit (MPBAC).

Transaction bus arbitrator

This block performs interport and intercard T-bus arbitration.

Port control

This block is a set of two MPBAC/MPLH pairs. These pairs are time multiplexed to provide the control of 64 logical ports. The block controls all data transfers to and from the buffers. These transfers include access to the T-bus and S-bus.

Synchronous bus interface

This block interfaces between MPLH and S-bus, with provision for CMU access.

Message counter

This block maintains a count of messages that transmit on the T-bus for each port.

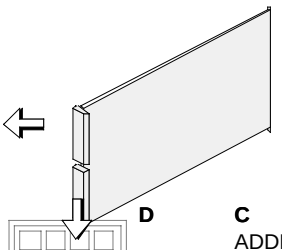
Signaling

Pin numbers

The pin numbers for the NT9X17DA appear in the following figure.

NT9X17DA (continued)

NT9X17DA pin numbers



	D	C	B	A
1	IP0	AD37	ADD00	GND
2	OP0	ADP3	ADD01	GND
3	IP1	ADREN	ADD02	GND
4	OP1	DATEN	ADD03	GND
5	IP2	EOSN	ADD04	GND
6	OP2	NVB0	ADD05	GND
7	IP3	NVB1	ADD06	GND
8	OP3	POKN	ADD07	GND
9	SEG0	BNFN	ADP0	GND
10	SEG1	SRCEN	ADD10	GND
11	SEG2	DSTEN	ADD11	GND
12	SEG3	REQN	ADD12	GND
13	SEG4	GRTN	ADD13	PBDASN
14		INHN	ADD14	PBWRTN
15			ADD15	PBACKN
16			ADD16	PBBCLK
17			ADD1'7	PBADD2
18			ADP1	PBADD3
19			AD20	PBADD4
20			AD21	PBADD5
21		PERINT4	AD22	PBSDREN
22			AD23	PBADD6
23	RSTOUTN		AD24	PBADD7
24			AD25	PBID0
25	BEN1	BEN0	AD26	unused
26	BEN3	BEN2	AD27	PBFP61N
27	GND		ADP2	CPSDREN
28	WRTN	GND	AD30	PBID1
29		DTACKN	AD31	HW4
30	PARITY		AD32	
31	PARITYEN		AD33	
32		GND	AD34	SH0
33	DAS32N		AD35	SH1
34			AD36	FP61N
35				C61
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		
44		ADDR10		+5
45		ADDR11		+5

	D	C	B	A
46		ADDR12		+5
47		ADDR13		+5
48		ADDR14		+5
49		ADDR15		+5
50	DATA16	ADDR16		+5
51	DATA17	ADDR17		+5
52	DATA18	ADDR18		+5
53	DATA19	ADDR19		+5
54	DATA20	ADDR20		+5
55	DATA21	ADDR21		+5
56	DATA22	ADDR22		
57	DATA23	ADDR23		LTVL
58	DATA24	ADDR24		LRVL
59	DATA25	ADDR25		STDA0
60	DATA26	ADDR26		STDA1
61	DATA27	ADDR27		STDA2
62	DATA28	ADDR28		STDA3
63	DATA29	ADDR29		STDA4
64	DATA39	ADDR30		STDA5
65	DATA31	ADDR31		STDA6
66				STDA7
67				STDA8
68				
69				SRDA0
70				SRDA1
71				SRDA2
72				SRDA3
73				SRDA4
74				SRDA5
75				SRDA6
76				SRDA7
77				
78				
79			PBDAT20	GND
80			PBDAT21	GND
81			PBDAT22	GND
82			PBDAT23	GND
83			PBDAT24	GND
84			PBDAT25	GND
85			PBDAT26	GND
86			PBDAT27	GND
87	PBID4		PBDAT28	GND
88	PBID3		PBDAT29	GND
89	PBID2		PBDAT30	GND
90	PBC61		PBDAT31	GND

Technical data

Power requirements

The power requirements for the NT9X17DA appear in the following table.

Power requirements

Parameter	Minimum	Nominal	Maximum
Supply voltage	4.75 V	5.0 V	5.25 V
Supply current		5.5 A	

NT9X20AA

Product description

The NT9X20AA is the fiber interface paddle board that messages links between the computing module (CM) and message switch (MS). The card interface on the backplane side is a synchronous bus (S-bus). This bus runs at an average rate of a maximum of 4.088 Mwords each second.

The S-bus divides to in-band and out-of-band (OOB) segments. The in-band segment has 8 bits. These bits carry the actual messaging information to or from the link handlers. The link handlers are on port cards. The two OOB bits that remain carry system reset information.

The NT9X20AA also has a bidirectional processor bus (P-bus). This bus provides access to the different read and write registers on the card. These registers are for initialization, maintenance activities and system reset requirements.

Functional description

The NT9X20AA is the fiber interface paddle board used for messages links between the CM and MS.

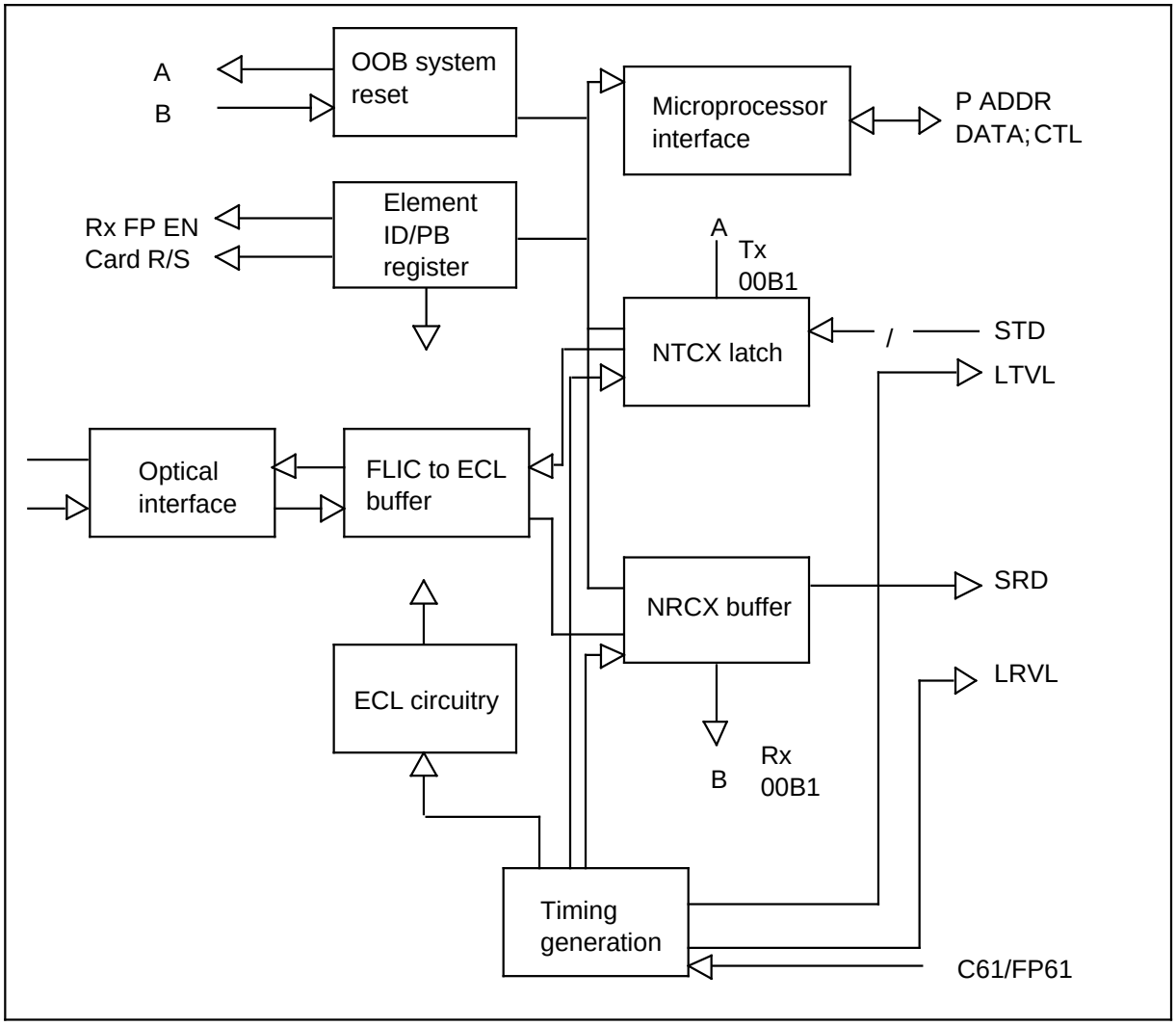
Functional blocks

The NT9X20AA has the following functional blocks:

- fiber link interface chip (FLIC) to emitter-coupled logic (ECL) buffer
- NTCX latch
- NRCX buffer
- timing generation
- ECL circuitry
- OOB system reset
- element ID/PB register
- optical interface
- microprocessor interface

The relationship between these blocks appears in the following figure.

NT9X20AA functional blocks



FLIC/ECL buffer

This block performs the following functions:

- ECL/transistor-transistor logic (TTL) level conversion
- parallel/serial conversion
- receive (Rx) frame detection/frame pulse generation
- local and remote loopbacks for maintenance purposes
- disabling of ECL input/outputs to this block for test purposes

NT9X20AA (continued)

NTCX latch

This block performs the following functions:

- codes data to DS512 10B12B line code
- inserts frame to channel zero
- inserts alarm code
- maintenance functions
- timing of information from link handlers

NRCX buffer

This block performs the following functions:

- decodes 10B12B-encoded Rx data
- elastic store
- detects alarm code
- checks line code problem
- scans concentration and distribution points
- maintenance functions
- interface to S-bus

Timing generation

This block accepts FP61- and C61 from the port card. This block also generates the different frame pulses and flow control signals that the NT9X20AA and port card interface require.

Emitter-coupled logic circuitry

This block performs the following functions:

- synthesis of 49-MHz clock
- generation of 20-ns frame pulse
- isolation of FLIC from ECL drive signals for tests

Out-of-band system reset

This block provides the interface between the RTIF at the CM and the MS modules. At the CM, the reset block accepts 7-bit words of data on the 12-bit paddle board data bus. The reset block converts this data to a serial stream. The block sends this data over the fiber link on one out-of-band bit four times every 125 µs. At the receiving end (the MS end), the system constructs the serial information again to parallel form. This information is available to the CPU again over the paddle board data bus.

Element ID/PB register

This block contains two software addressable entities, a paddle board element identification (ID) PROM and an 8-bit paddle board register. The PROM is part of the overall element ID structure. The PROM contains the standard information list. The register allows the software access to the primary and secondary frame pulse enables used for shelf synchronization.

Optical interface

The optical interface has three custom thick film hybrids: a transmitter, receiver and clock recovery. In the transmit direction, the system takes the serial information from the FLIC. The system converts the information directly to an optical signal. In the receive direction, the system converts the incoming optical signal to a logic signal at the output of the receiver. The system sends the incoming optical signal to the clock recovery. The Rx clock recovery extracts clock information from the incoming serial stream, and uses that clock to sample the data again. The system sends the regenerated data and Rx clock to the FLIC.

Microprocessor interface

This block has a 12-bit bidirectional data bus buffer, address decoding and DTACK reply logic.

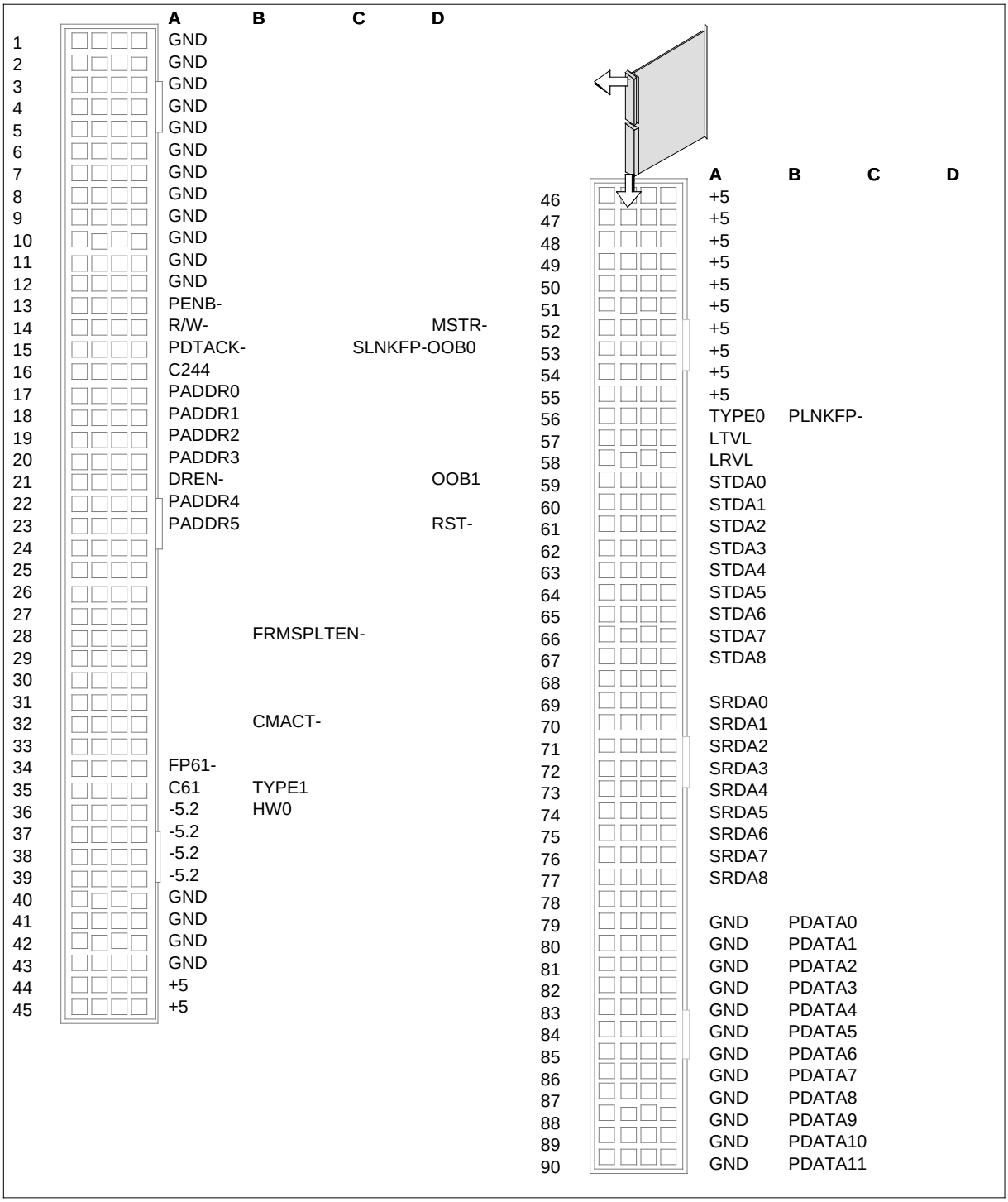
Signaling

Pin numbers

The NT9X20AA pin numbers appear in the following figure.

NT9X20AA (end)

NT9X20AA pin numbers



	A	B	C	D
1	GND			
2	GND			
3	GND			
4	GND			
5	GND			
6	GND			
7	GND			
8	GND			
9	GND			
10	GND			
11	GND			
12	GND			
13	PENB-			
14	R/W-			MSTR-
15	PDTACK-		SLNKFP-	OOB0
16	C244			
17	PADDR0			
18	PADDR1			
19	PADDR2			
20	PADDR3			
21	DREN-			OOB1
22	PADDR4			
23	PADDR5			RST-
24				
25				
26				
27				
28		FRMSPLTEN-		
29				
30				
31				
32		CMACT-		
33				
34	FP61-			
35	C61	TYPE1		
36	-5.2	HW0		
37	-5.2			
38	-5.2			
39	-5.2			
40	GND			
41	GND			
42	GND			
43	GND			
44	+5			
45	+5			

	A	B	C	D
46	+5			
47	+5			
48	+5			
49	+5			
50	+5			
51	+5			
52	+5			
53	+5			
54	+5			
55	+5			
56	TYPE0	PLNKFP-		
57	LTVL			
58	LRVL			
59	STDA0			
60	STDA1			
61	STDA2			
62	STDA3			
63	STDA4			
64	STDA5			
65	STDA6			
66	STDA7			
67	STDA8			
68				
69	SRDA0			
70	SRDA1			
71	SRDA2			
72	SRDA3			
73	SRDA4			
74	SRDA5			
75	SRDA6			
76	SRDA7			
77	SRDA8			
78				
79	GND	PDATA0		
80	GND	PDATA1		
81	GND	PDATA2		
82	GND	PDATA3		
83	GND	PDATA4		
84	GND	PDATA5		
85	GND	PDATA6		
86	GND	PDATA7		
87	GND	PDATA8		
88	GND	PDATA9		
89	GND	PDATA10		
90	GND	PDATA11		

NT9X20BB

Product description

The NT9X20BB is a DMS-bus fiber interface paddle board that messages links between DMS-bus and the enhanced network (ENET). The card interface on the backplane side is a shorting bus (S-bus). The S-bus runs at a maximum rate of 4.088 Mwords each second.

The S-bus has an in-band and out-of-band (OOB) segment. The in-band segment contains 8 bits that carry the accurate messaging information to or from the link handlers. The link handlers are on port cards. The two out-of-band bits that remain, carry system reset information.

The NT9X20BB has a two-direction processor bus (P-bus). The P-bus provides access to the read and write registers on the card. These registers are used for initialization, maintenance activities, and system reset requirements.

Functional description

Functional blocks

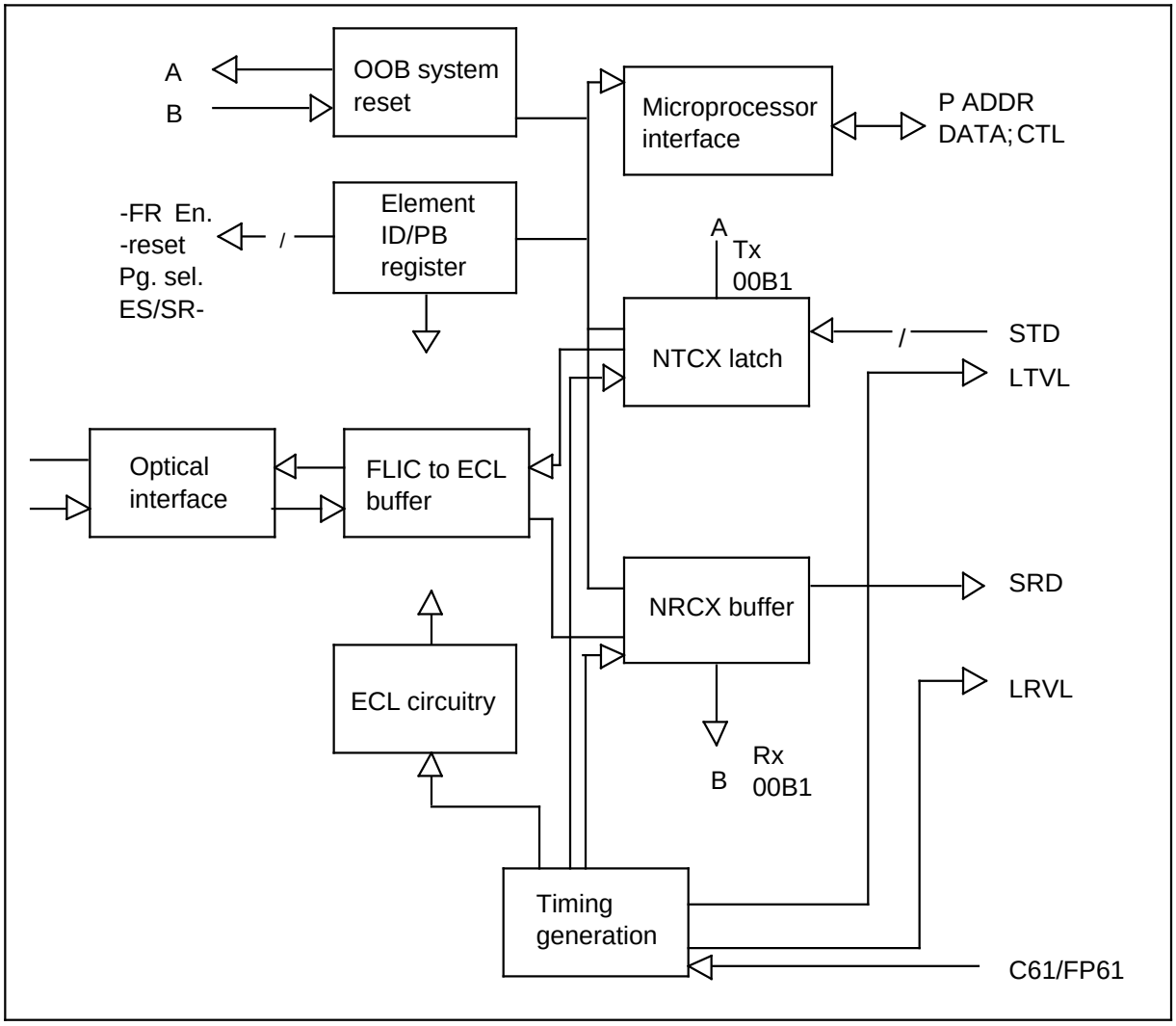
The NT9X20BB has the following functional blocks:

- fiber link interface chip (FLIC) to emitter-coupled logic (ECL) buffer
- NTCX chip/latch
- NRCX chip/retiming
- timing generation
- ECL circuitry
- OOB system reset
- element ID/PB register

NT9X20BB (continued)

- optical interface
- microprocessor interface

NT9X20BB functional blocks



FLIC to ECL buffer

This block performs the following functions:

- ECL/transistor-transistor logic (TTL) level conversion
- parallel/serial conversion
- receive (Rx) frame detection/frame pulse generation

- local and remote loopbacks for maintenance purposes
- disabling of ECL input/outputs to this block for test purposes

NTCX chip latch

This block performs the following functions:

- encodes data into DS512 10B12B line code
- inserts frame into channel zero
- inserts alarm code
- maintenance functions
- times information from link handlers again

NRCX chip retiming

This block performs the following functions:

- decodes 10B12B-encoded Rx data
- elastic store
- alarm code detection
- checks line code problem
- scan concentration and distribution points
- maintenance functions
- interfaces to S-bus

Timing generation

This block accepts FP61- and C61 from the port card. This block generates different frame pulses and flow control signals that internal card operation requires. This condition complies with link-related functions.

Emitter-coupled logic circuitry

This block performs the following functions:

- synthesizes 49-MHz clock
- generates 20-ns frame pulse
- isolates FLIC from ECL drive signals for testing

Out-of-band system reset

This block provides a low-speed serial access to one of the two OOB bits that the SuperNode reset structure defines for use. The NT9X20AA can be used as a master or a slave node. The NT9X20BB can only be used as a master node.

NT9X20BB (continued)

Element ID/PB register

This block contains two software addressable entities, a paddle board element identification (ID) PROM and an 8-bit paddle board register. The PROM is part of the element ID structure. The PROM contains the standard information list. The register allows the software access to different card configuration options, and reset.

Optical interface

The optical interface contains three custom thick film hybrids. These custom thick film hybrids include a transmitter, receiver, and clock recovery. In the transmit direction, serial information is taken from the FLIC and converted directly to an optical signal. In the receive direction, the incoming optical signal converts to a logic signal at the output of the receiver. The logic signal is sent to the clock recovery. The Rx clock recovery extracts clock information from the incoming serial stream. The Rx clock recovery uses the clock to sample the data again. This regenerated data and Rx clock are sent to the FLIC.

P interface

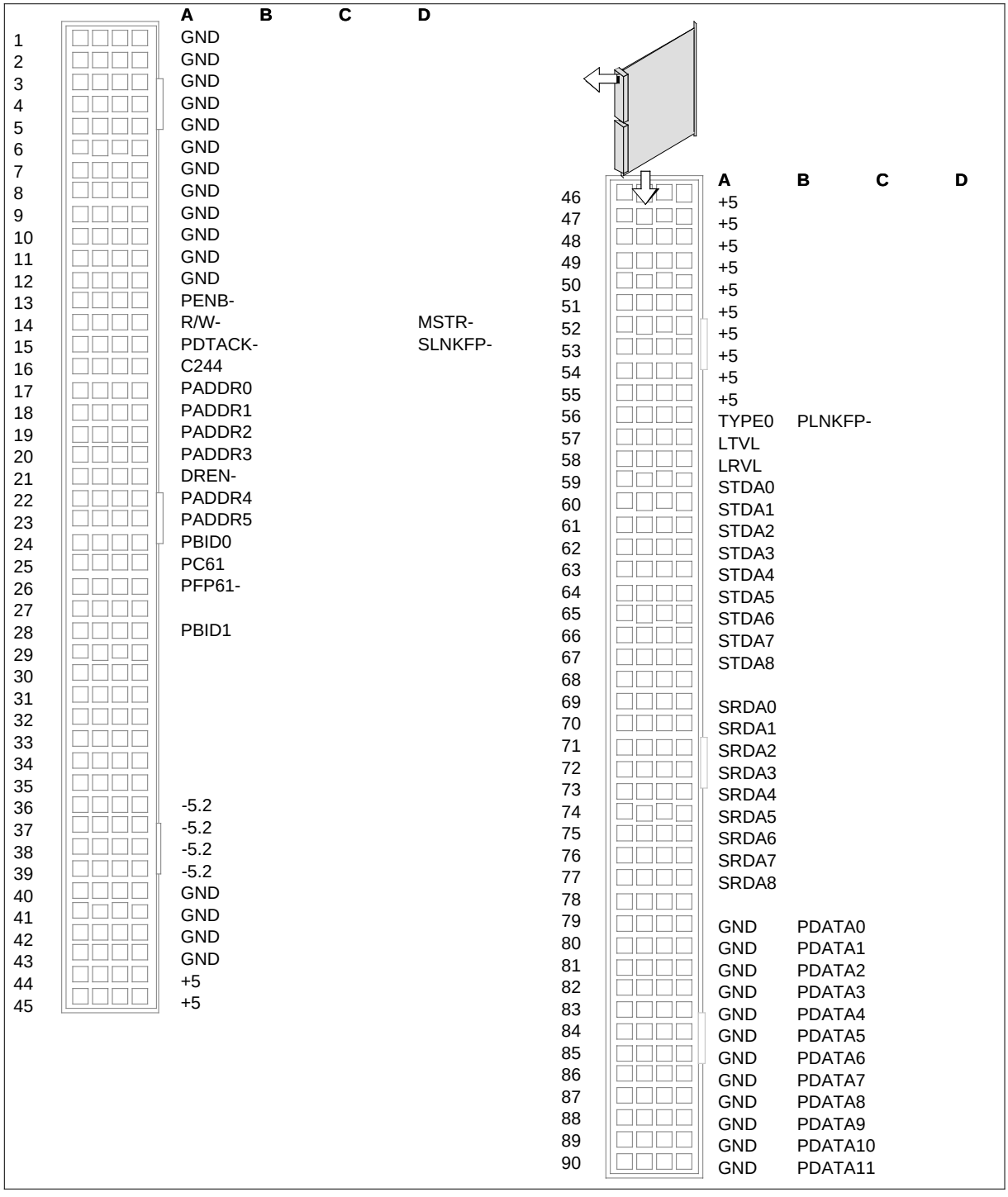
This block contains a 12-bit two-direction data bus buffer, address decoding and DTACK reply logic.

Signaling

Pin numbers

The pin numbers for the NT9X20BB appear in the following figure.

NT9X20BB pin numbers



NT9X20BC

Product description

The NT9X20BC is a DMS-bus fiber interface paddle board that messages links between DMS-bus and the enhanced network (ENET). The card interface on the backplane side is a shorting bus (S-bus). The S-bus runs at a maximum rate of 4.088 Mwords each second.

Note that one main difference is present between NT9X20BC and the 9X20AA. The DMS-bus/DMS-CORE applications use the NT9X20BC and the 9X20AA. The NT9X20AA can be used as a master or a slave node. The NT9X20BC can only be used at a master end.

The S-bus has in-band and out-of-band (OOB) segments. The in-band segment contains 8 bits that carry the accurate messaging information to or from the link handlers. The link handlers are on port cards. The two out-of-band bits that remain carry system reset information.

The NT9X20BC has a two-direction processor bus (P-bus). The P-bus provides access to the read and write registers on the card. These registers are used for initialization, maintenance activities, and system reset requirements.

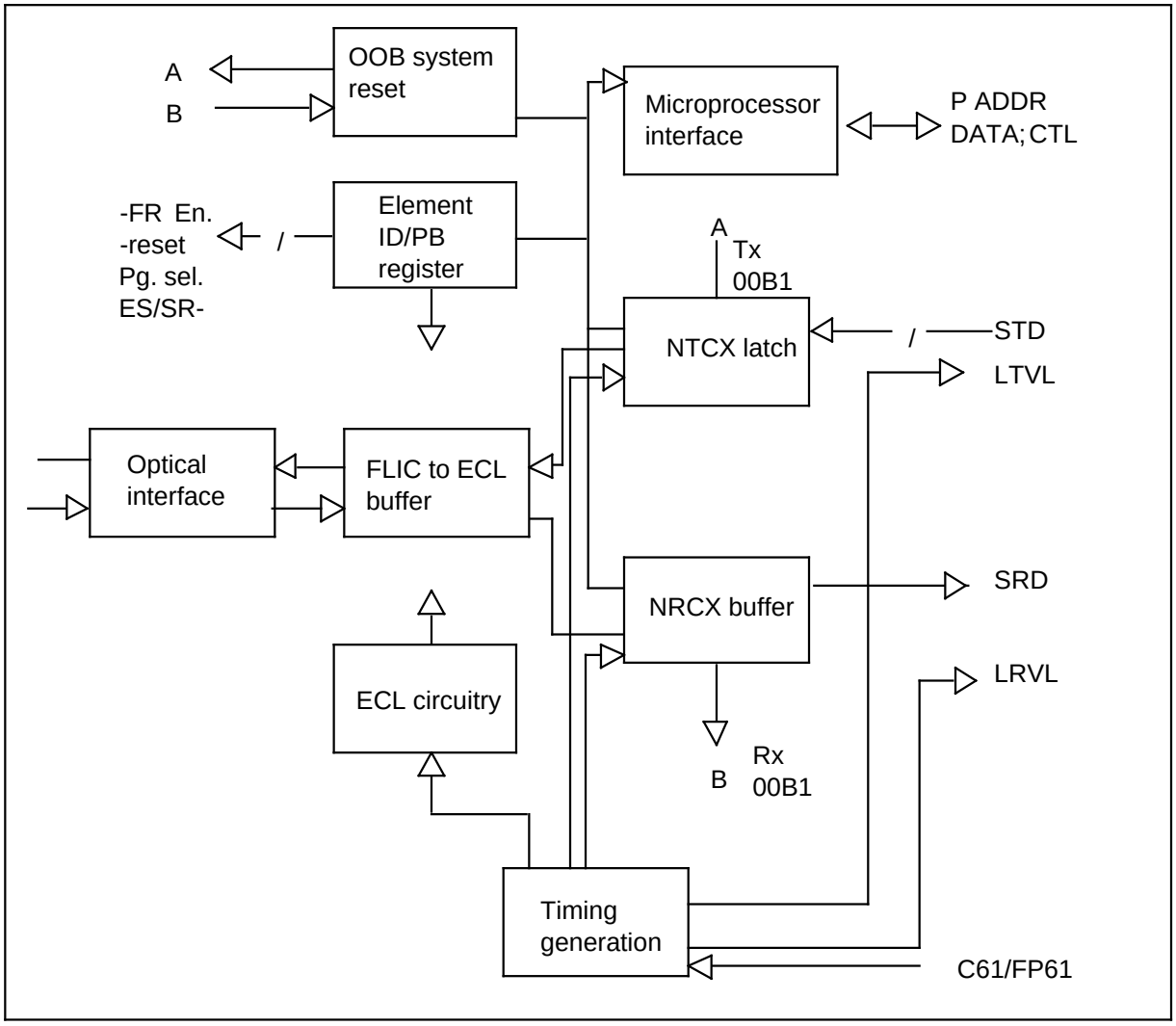
Functional description

Functional blocks

The NT9X20BC has the following functional blocks:

- fiber link interface chip (FLIC) to emitter-coupled logic (ECL) buffer
- NTCX chip/latch
- NRCX chip/retiming
- timing generation
- ECL circuitry
- OOB system reset
- element ID/PB register
- optical interface
- microprocessor interface

NT9X20BC functional blocks



FLIC to ECL buffer

This block performs the following functions:

- ECL/transistor-transistor logic (TTL) level conversion
- parallel/serial conversion
- receive (Rx) frame detection/frame pulse generation
- local and remote loopbacks for maintenance purposes
- disabling of ECL input/outputs to this block for test purposes

NT9X20BC (continued)

NTCX chip latch

This block performs the following functions:

- encodes data into DS512 10B12B line code
- inserts frame into channel zero
- inserts alarm code
- maintenance functions
- retimes information from link handlers

NRCX chip retiming

This block performs the following functions:

- decodes 10B12B-encoded Rx data
- elastic store
- detects alarm code
- checks line code problem
- scan concentration and distribution points
- maintenance functions
- interface to S-bus

Timing generation

This block accepts FP61- and C61 from the port card. This block generates the different frame pulses, and flow control signals that the internal card operation requires. This condition complies with link-related functions.

Emitter-coupled logic circuitry

This block performs the following functions:

- synthesizes 49-MHz clock
- generates 20-ns frame pulse
- isolates FLIC from ECL drive signals for tests

Out-of-band system reset

This block provides a low-speed serial access to one of the two OOB bits that the SuperNode reset structure defines for use. The NT9X20AA can be used as a master or a slave node. The NT9X20BC can only be used at a master node.

Element ID/PB register

This block contains two software addressable entities, a paddle board element identification (ID) PROM and an 8-bit paddle board register. The PROM is

part of the element ID structure. The PROM contains the standard information list. The register allows the software access to different card configuration options, and reset.

Optical interface

The optical interface contains three custom thick film hybrids. The custom thick film hybirds include a transmitter, receiver, and clock recovery. In the transmit direction, serial information is taken from the FLIC and converted directly to an optical signal. In the receive direction, the incoming optical signal converts to a logic signal at the output of the receiver. The logic signal is sent to the clock recovery. The Rx clock recovery extracts clock information from the incoming serial stream. The Rx clock recovery uses that clock to sample the data again. This regenerated data and Rx clock are sent to the FLIC.

P interface

This block contains a 12-bit two-direction data bus buffer, address decoding and DTACK reply logic.

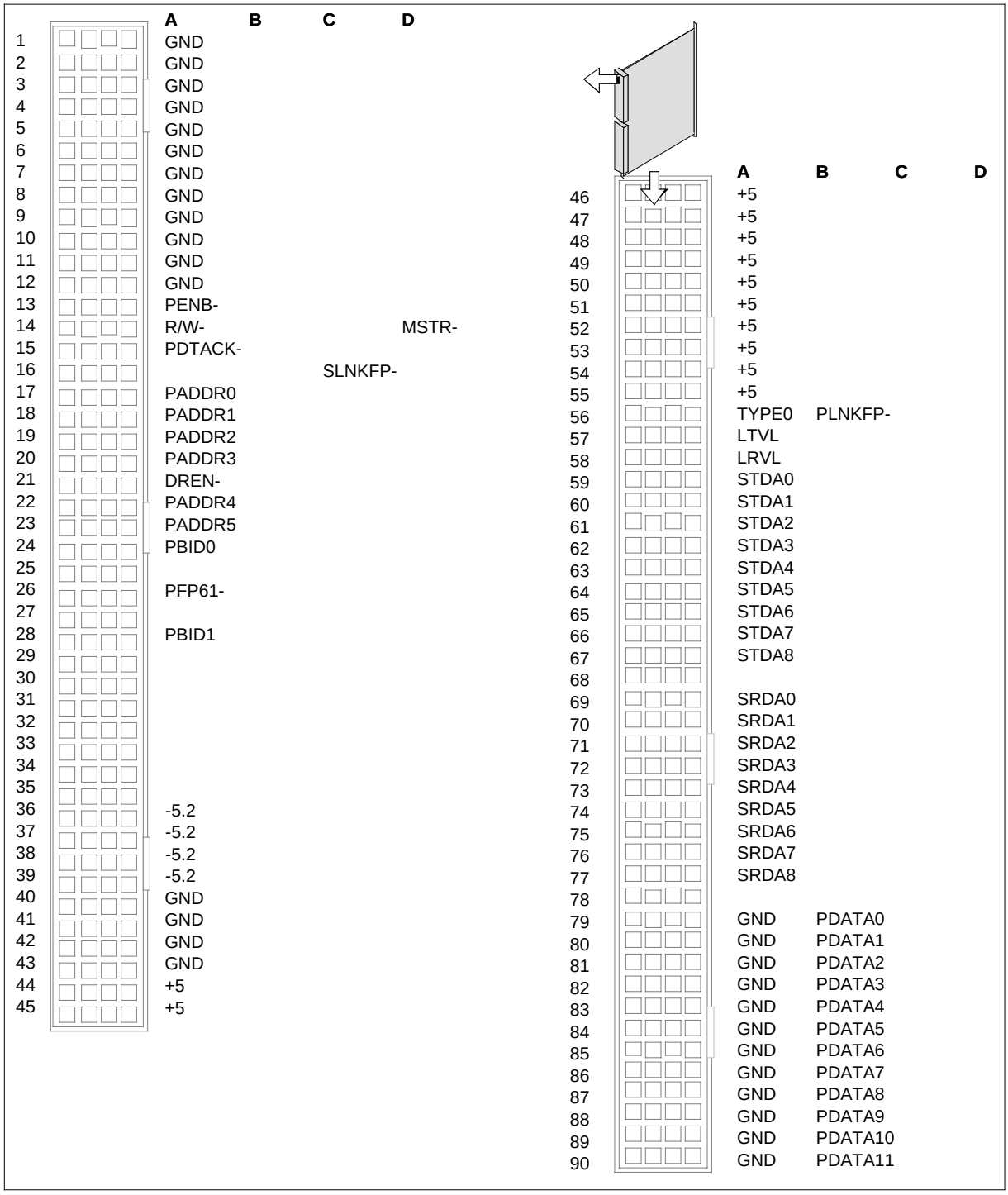
Signaling

Pin numbers

The pin numbers for the NT9X20BC appear in the following figure.

NT9X20BC (continued)

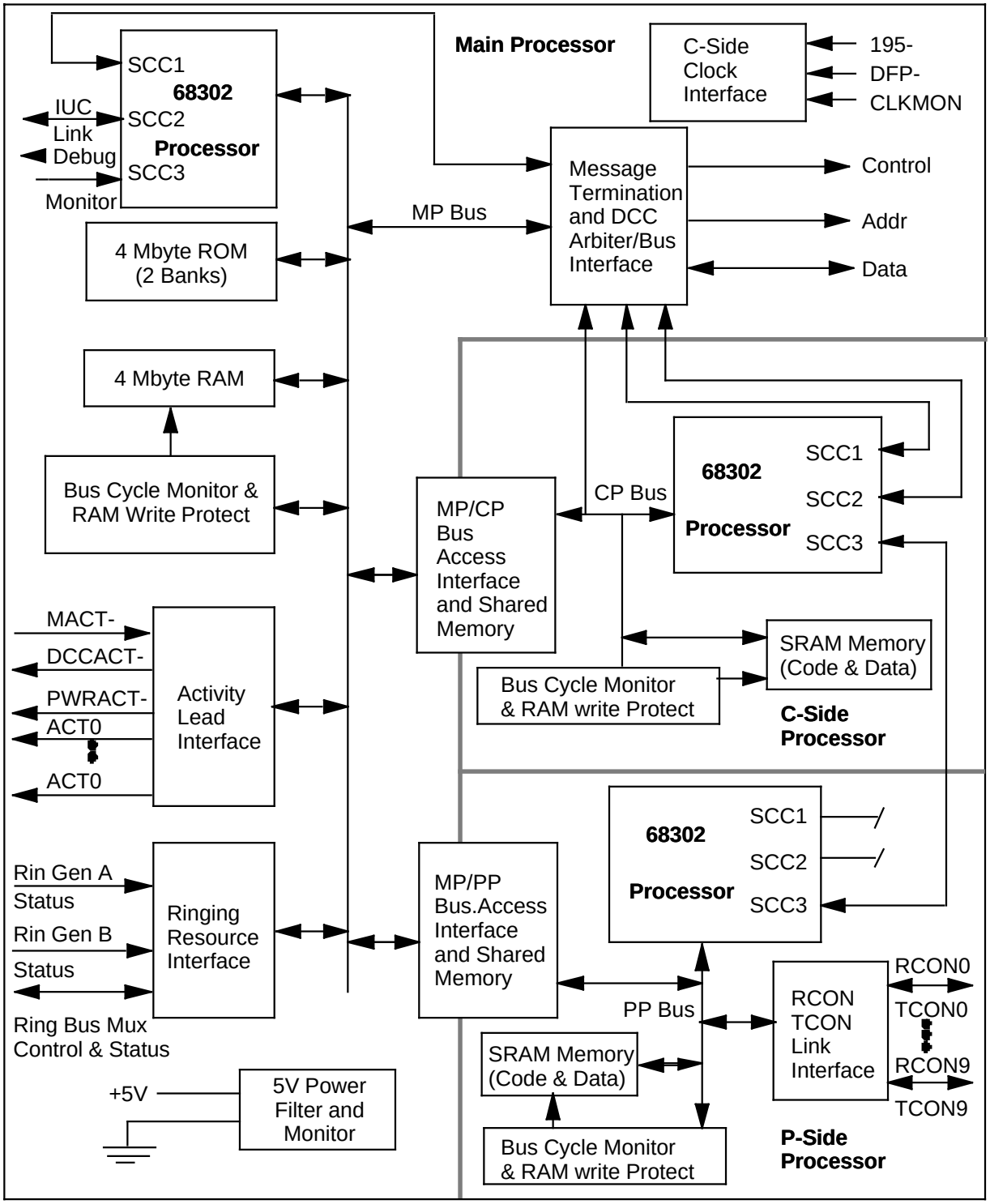
NT9X20BC pin numbers



	A	B	C	D
1	GND			
2	GND			
3	GND			
4	GND			
5	GND			
6	GND			
7	GND			
8	GND			
9	GND			
10	GND			
11	GND			
12	GND			
13	PENB-			
14	R/W-			MSTR-
15	PDTACK-			
16			SLNKFP-	
17	PADDR0			
18	PADDR1			
19	PADDR2			
20	PADDR3			
21	DREN-			
22	PADDR4			
23	PADDR5			
24	PBID0			
25				
26	PFP61-			
27				
28	PBID1			
29				
30				
31				
32				
33				
34				
35				
36	-5.2			
37	-5.2			
38	-5.2			
39	-5.2			
40	GND			
41	GND			
42	GND			
43	GND			
44	+5			
45	+5			

	A	B	C	D
46	+5			
47	+5			
48	+5			
49	+5			
50	+5			
51	+5			
52	+5			
53	+5			
54	+5			
55	+5			
56	TYPE0	PLNKFP-		
57	LTVL			
58	LRVL			
59	STDA0			
60	STDA1			
61	STDA2			
62	STDA3			
63	STDA4			
64	STDA5			
65	STDA6			
66	STDA7			
67	STDA8			
68				
69	SRDA0			
70	SRDA1			
71	SRDA2			
72	SRDA3			
73	SRDA4			
74	SRDA5			
75	SRDA6			
76	SRDA7			
77	SRDA8			
78				
79	GND	PDATA0		
80	GND	PDATA1		
81	GND	PDATA2		
82	GND	PDATA3		
83	GND	PDATA4		
84	GND	PDATA5		
85	GND	PDATA6		
86	GND	PDATA7		
87	GND	PDATA8		
88	GND	PDATA9		
89	GND	PDATA10		
90	GND	PDATA11		

NT9X20BC functional block diagram



NT9X21AA

Description

The NT9X21AA computing module (CM) termination paddle board contains element identification (ID) PROM.

Functional description

The PROMs in the NT9X21AA contain function, configuration, and vintage information that allow system configurations. Scan all element IDs in the system to build a configuration inventory data base. The next step is to determine the hardware and software compatibility of the integrated system. During system initialization, elements of the NT9X21AA are identified through the element block enables. The element block decode circuit provides enables for the paddle board ID PROM, and the ±5V power converter identification (ID) PROMs.

Elements are decoded using a scheme that allows 16 elements for each slot and 64 bytes for each element. The EBENN signals (outputs of the decoder U1) select each element on the NT9X21AA. The system decodes the NT9X21 paddle board as element C. The +5V and –5V power converters are elements D and E.

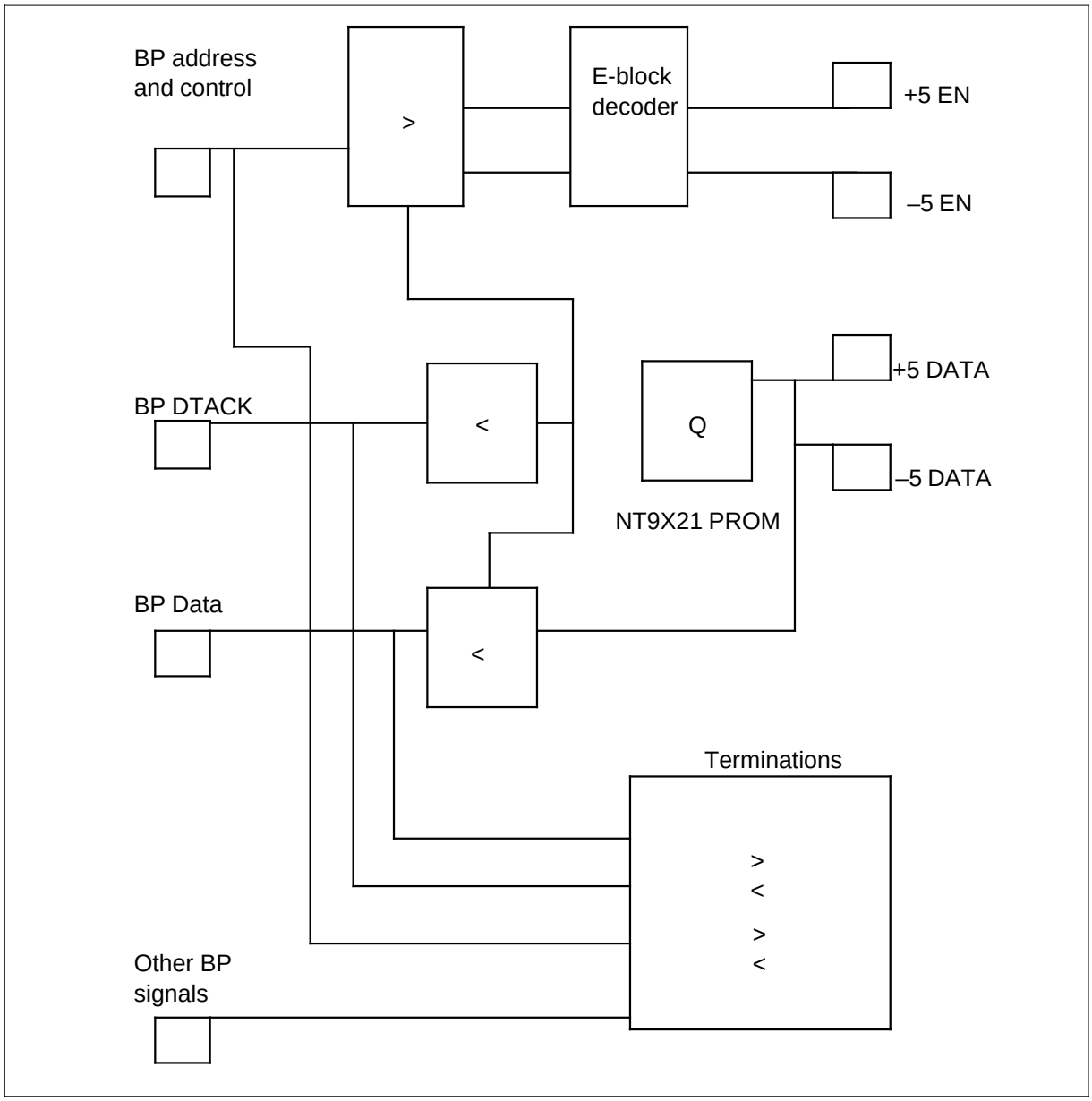
Functional blocks

The NT9X21AA has the following operating blocks:

- backplane (BP) address and control
- element block (E-block) decoder
- BP DTACK
- NT9X21 PROM
- BP data
- terminations

The relationship between the functional blocks appears in the following figure.

NT9X21AA functional blocks



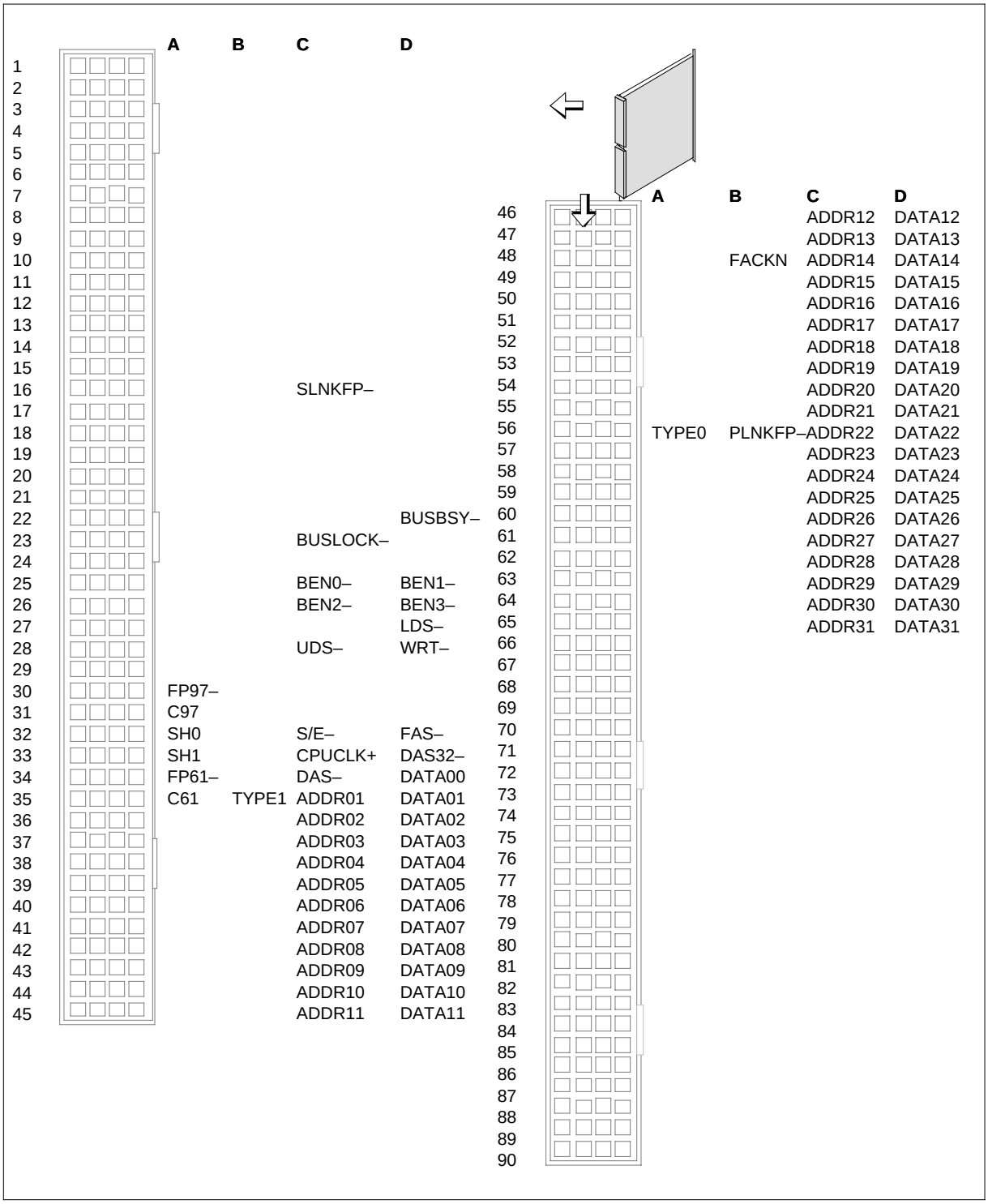
Signaling

Pin numbers

The pin numbers for NT9X21AA appear in the following figure.

NT9X21AA (continued)

NT9X21AA pin numbers



	A	B	C	D
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16			SLNKFP–	
17				
18				
19				
20				
21				
22				BUSBSY–
23			BUSLOCK–	
24				
25			BEN0–	BEN1–
26			BEN2–	BEN3–
27				LDS–
28			UDS–	WRT–
29				
30	FP97–			
31	C97			
32	SH0		S/E–	FAS–
33	SH1		CPUCLK+	DAS32–
34	FP61–		DAS–	DATA00
35	C61	TYPE1	ADDR01	DATA01
36			ADDR02	DATA02
37			ADDR03	DATA03
38			ADDR04	DATA04
39			ADDR05	DATA05
40			ADDR06	DATA06
41			ADDR07	DATA07
42			ADDR08	DATA08
43			ADDR09	DATA09
44			ADDR10	DATA10
45			ADDR11	DATA11

	A	B	C	D
46			ADDR12	DATA12
47			ADDR13	DATA13
48		FACKN	ADDR14	DATA14
49			ADDR15	DATA15
50			ADDR16	DATA16
51			ADDR17	DATA17
52			ADDR18	DATA18
53			ADDR19	DATA19
54			ADDR20	DATA20
55			ADDR21	DATA21
56	TYPE0	PLNKFP–	ADDR22	DATA22
57			ADDR23	DATA23
58			ADDR24	DATA24
59			ADDR25	DATA25
60			ADDR26	DATA26
61			ADDR27	DATA27
62			ADDR28	DATA28
63			ADDR29	DATA29
64			ADDR30	DATA30
65			ADDR31	DATA31
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89				
90				

Technical data

Power requirements

The ac conditions that operate for the NT9X21AA appear in the following table.

ID PROM access

No.	Parameter	Normal (ns)	Maximum (ns)
1	DAS32 High to DTACK High	18	28
2	DAS32 Low to EBENN Low	44	56
3	DAS32 High to EBENN High	9	14
4	DAS32 Low to DTACK Low	53	70
5	DAS32 Low to Data valid	70	101
6	DAS32 High to Data invalid	18	28

NT9X21AB

Product description

The NT9X21AB bus terminator paddle board contains element identification (ID) PROMs.

Functional description

The PROMs in the NT9X21AB contain function, configuration, and vintage information that allows system configurations. Scan all element IDs in the system to build a configuration inventory database. Determine the hardware and software compatibility of the integrated system. During system initialization, elements of the NT9X21AB are identified through the element block enables. The element block decode circuits provide enables for the paddle board ID PROM and the ±50V power converter identification PROMs.

Use a method that allows 16 elements for each slot and 64 bytes for each element to decode these elements. The EBENN signals (outputs of the decoder U12) select the elements on the NT9X21AB. The system decodes the paddle board as element C. The +5V and -5V power converters are elements D and E. A status register (U13) is element F. This register provides the status of the power lock (PLOCK-) signal on data bus bit 25. This register provides the status of the system load module active (SLU+5-) signal on data bus bit 24.

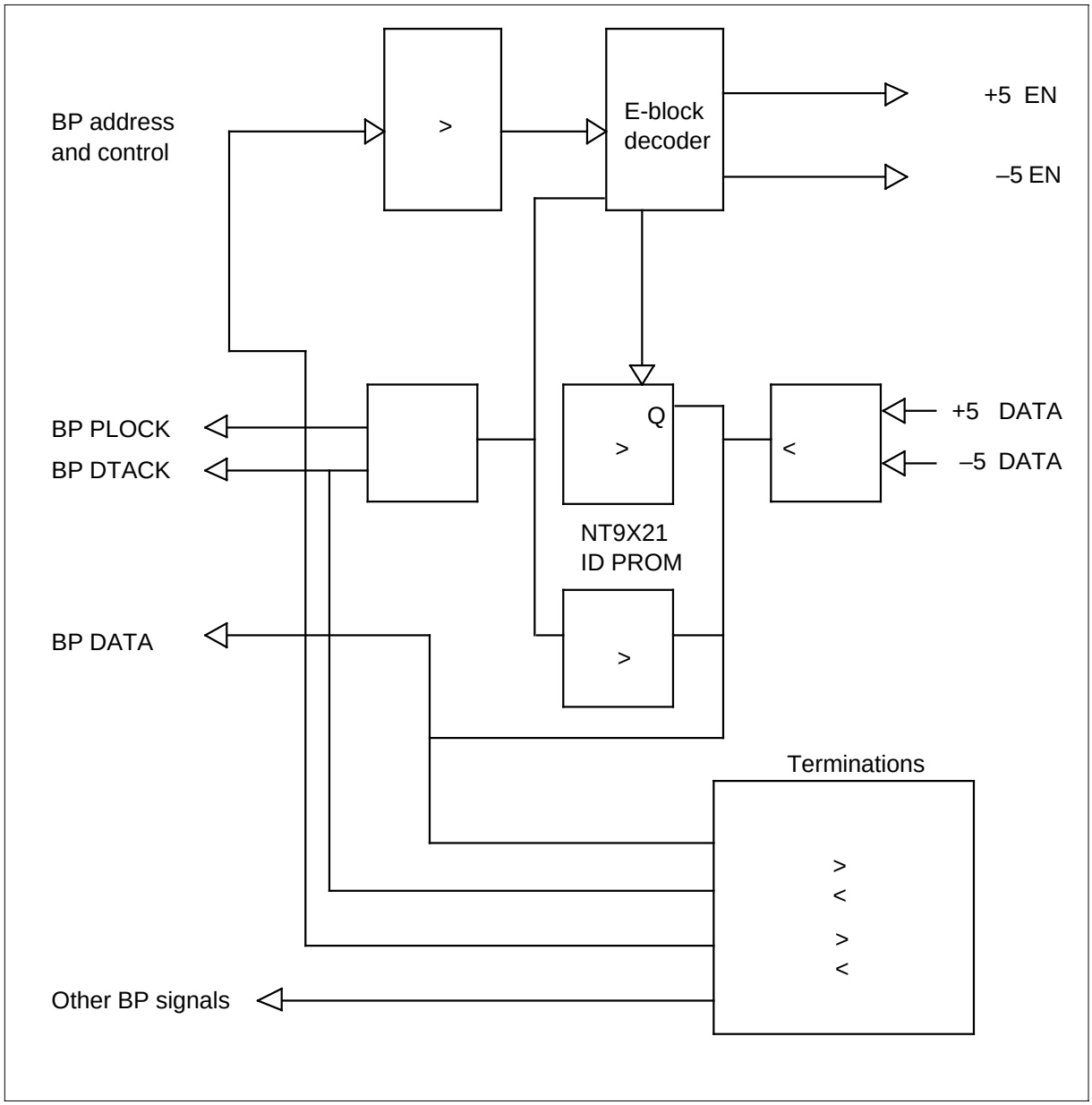
Functional blocks

The NT9X21AB has the following operating blocks:

- backplane (BP) address and control.
- element block (E-block) decoder.
- BP signals.
- NT9X21 ID PROM.
- +5 EN and -5 EN.
- +5DATA and -5DATA.
- terminations.

The relationship between the functional blocks appear in the following figure.

NT9X21AB operating blocks



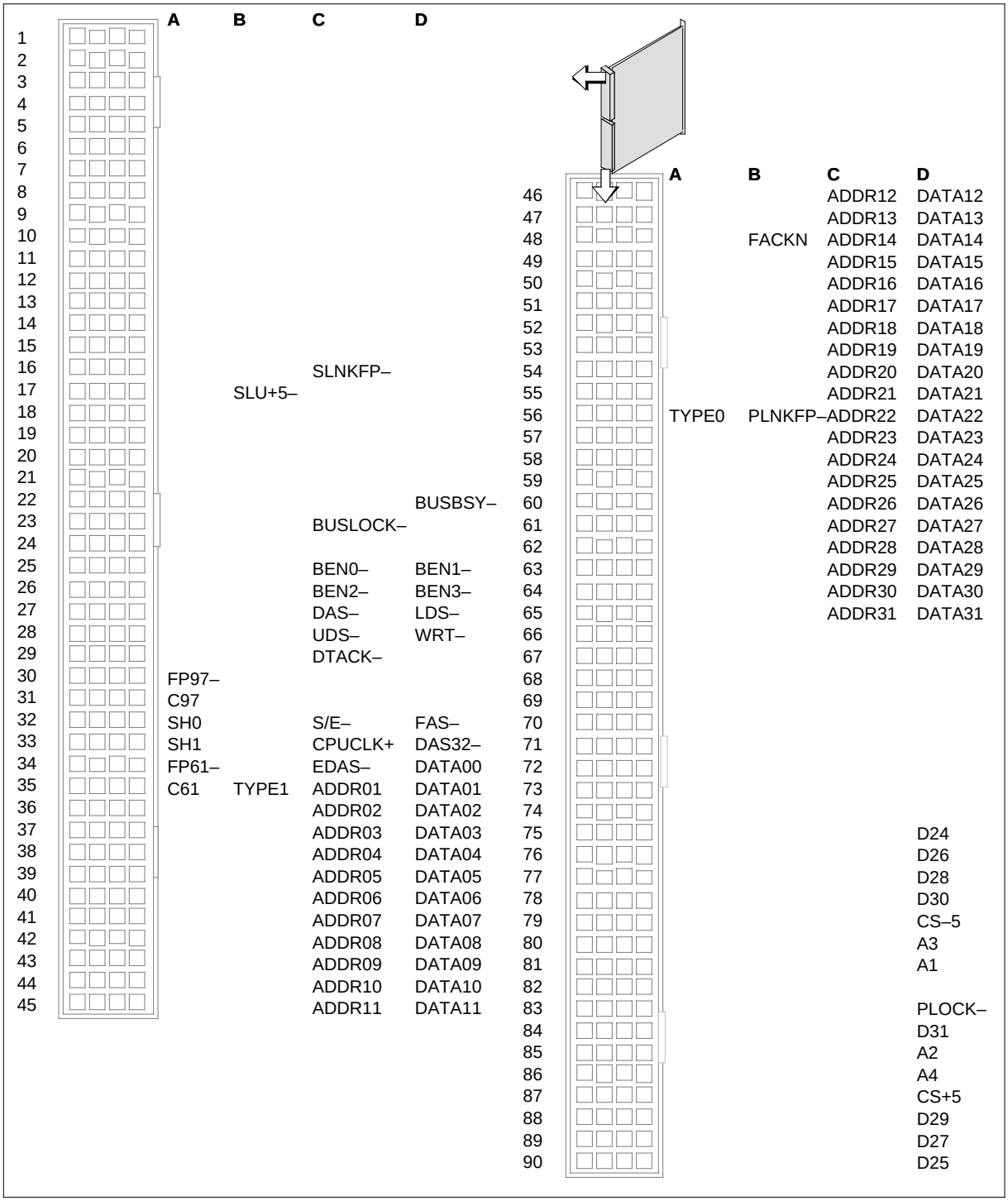
Signaling

Pin numbers

The pin numbers for NT9X21AB appear in the following figure.

NT9X21AB (continued)

NT9X21AB pin numbers



	A	B	C	D
1				
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10				
11				
12				
13				
14				
15				
16			SLNKFP–	
17		SLU+5–		
18				
19				
20				
21				
22				BUSBSY–
23			BUSLOCK–	
24				
25			BEN0–	BEN1–
26			BEN2–	BEN3–
27			DAS–	LDS–
28			UDS–	WRT–
29			DTACK–	
30	FP97–			
31	C97			
32	SH0		S/E–	FAS–
33	SH1		CPUCLK+	DAS32–
34	FP61–		EDAS–	DATA00
35	C61	TYPE1	ADDR01	DATA01
36			ADDR02	DATA02
37			ADDR03	DATA03
38			ADDR04	DATA04
39			ADDR05	DATA05
40			ADDR06	DATA06
41			ADDR07	DATA07
42			ADDR08	DATA08
43			ADDR09	DATA09
44			ADDR10	DATA10
45			ADDR11	DATA11

	A	B	C	D
46			ADDR12	DATA12
47			ADDR13	DATA13
48		FACKN	ADDR14	DATA14
49			ADDR15	DATA15
50			ADDR16	DATA16
51			ADDR17	DATA17
52			ADDR18	DATA18
53			ADDR19	DATA19
54			ADDR20	DATA20
55			ADDR21	DATA21
56	TYPE0	PLNKFP–	ADDR22	DATA22
57			ADDR23	DATA23
58			ADDR24	DATA24
59			ADDR25	DATA25
60			ADDR26	DATA26
61			ADDR27	DATA27
62			ADDR28	DATA28
63			ADDR29	DATA29
64			ADDR30	DATA30
65			ADDR31	DATA31
66				
67				
68				
69				
70				
71				
72				
73				
74				
75				D24
76				D26
77				D28
78				D30
79				CS–5
80				A3
81				A1
82				
83				PLOCK–
84				D31
85				A2
86				A4
87				CS+5
88				D29
89				D27
90				D25

Technical data

Power requirements

The ac conditions that operate for the NT9X21AB appear in the following table.

ID PROM access

No.	Parameter	Normal (ns)	Maximum (ns)
1	DAS32 high to DTACK high	18	28
2	DAS32 low to EBENN low	44	56
3	DAS32 high to EBENN high	9	14
4	DAS32 low to DTACK low	53	70
5	DAS32 low to data valid	70	101
6	DAS32 high to data invalid	18	28

NT9X22CA

Product description

The system uses the subsystem clock paddle board (PB), NT9X22CA, in the computing module (CM) of the DMS-core. One NT9X22CA in each CM plane supplies that plane with a 16.384 MHz clock (C61) and a corresponding 8 kHz frame pulse (FP61-). These signals are for the operation of the message controller (MC). The controller consists of the CM CPU port, NT9X12AA, and the DS512 fiber optic interface, NT9X20AA. The CM communicates with the message switch (MS) through the MC by use of synchronized messages. The subsystem clock (SSC) generates and synchronizes the clock signals (C61 and FP61-) of the CM and the MS.

Functional description

Functional blocks

The NT9X22CA contains the following operating blocks:

- oscillator
- frame phase counter
- digital-to-analog converter (DAC)
- microprocessor
- control state register

Oscillator

The output of a 32.768 MHz voltage-controlled crystal oscillator (VCXO) is buffered. The system buffers the output to produce a 50% duty cycle digital transistor-transistor logic (TTL) clock signal (CLOCK30). The frequency of the clock signal is in proportion to an input analog control voltage over the specified tuning range (TR) of the oscillator. Typical control voltage range is 0 to +4V.

Frame phase counter

The counter chain produces a 12-bit count the signal PHASELEN samples and stores in a register (phase detector). Synchronize the reference frame pulse (REFFP) to CLOCK30 to produce the signal PHASELEN. This action allows the SSC processor to read the phase detector register. This register contains a phase sample that represents the difference phase between the local frame pulse FP61- and the REFFP. The firmware of the SSC uses this difference. The difference determines the required change in the phase of FP61- to phase lock FP61- and REFFP.

Digital-to-analog converter

The DAC is a single chip that contains the following:

- a microprocessor interface
- a double 12-bit buffer
- a voltage reference source
- a DAC section
- an output voltage amplifier

The DAC receives a 12-bit value from the microprocessor and produces an equal dc analog signal. The system sends this signal to the VCXO analog control input. The frequency output of the VCXO is equal to the 12-bit DAC input value. The microprocessor must perform two write cycles to latch the DAC value to the double input buffer. This action is caused by the fact that the microprocessor has an 8-bit bus in comparison to the 12-bit input of the DAC.

Microprocessor

The microprocessor reads the 12-bit count in the phase detector register. The microprocessor reads the count once in a while and uses this value to compare the phase of the local clock. Compare the phase to the phase of the REFFP. This phase error calculates the correct DAC value. The system requires this value to lock the frequency and phase of the regenerated FP and clock. The frequency and phase of the FP and clock are locked to the frequency and phase of the REFFP.

The microprocessor reads the phase error every 160 ms. The microprocessor receives a 4 kHz clock signal, derived from FP61. The system uses this signal as a timer input that interrupts the processor. The system interupts the processor every 160 ms in order to read the phase error and adjust the DAC.

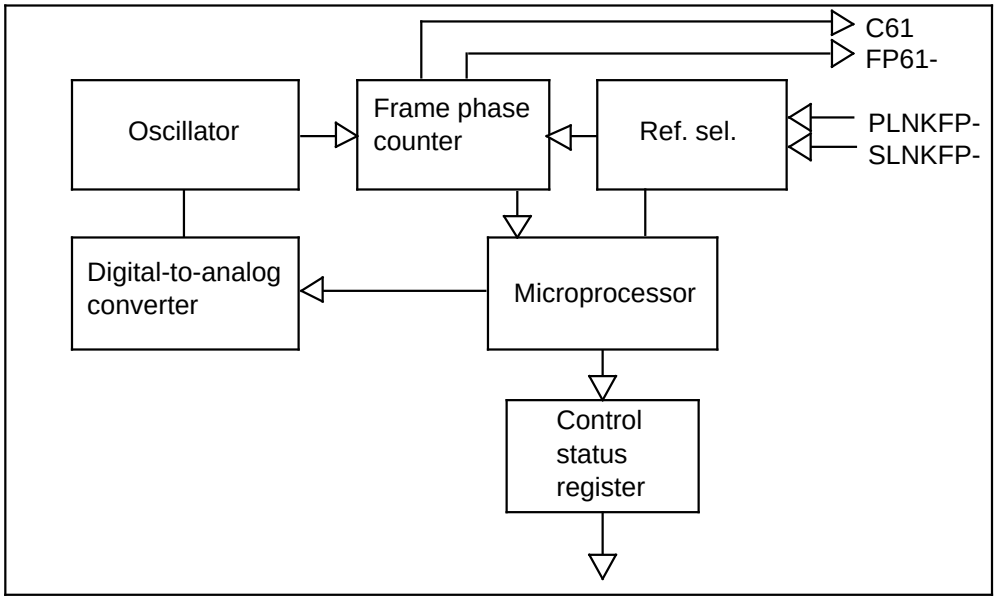
Control status register

Two control functions of the SSC are available. Control of two bits in the control status register on one 9X12AA-CM CPU port in each CM plane accesses these functions. When you use one control function, one 9X12 contains the control status register. The other control function resets the digital phase-locked loop (DPLL). Three status indicators reflect the state of the SSC. The SSC is determined through diagnostics of the SSC.

The relationship between the operating blocks appear in the following figure.

NT9X22CA (continued)

NT9X22CA operating blocks



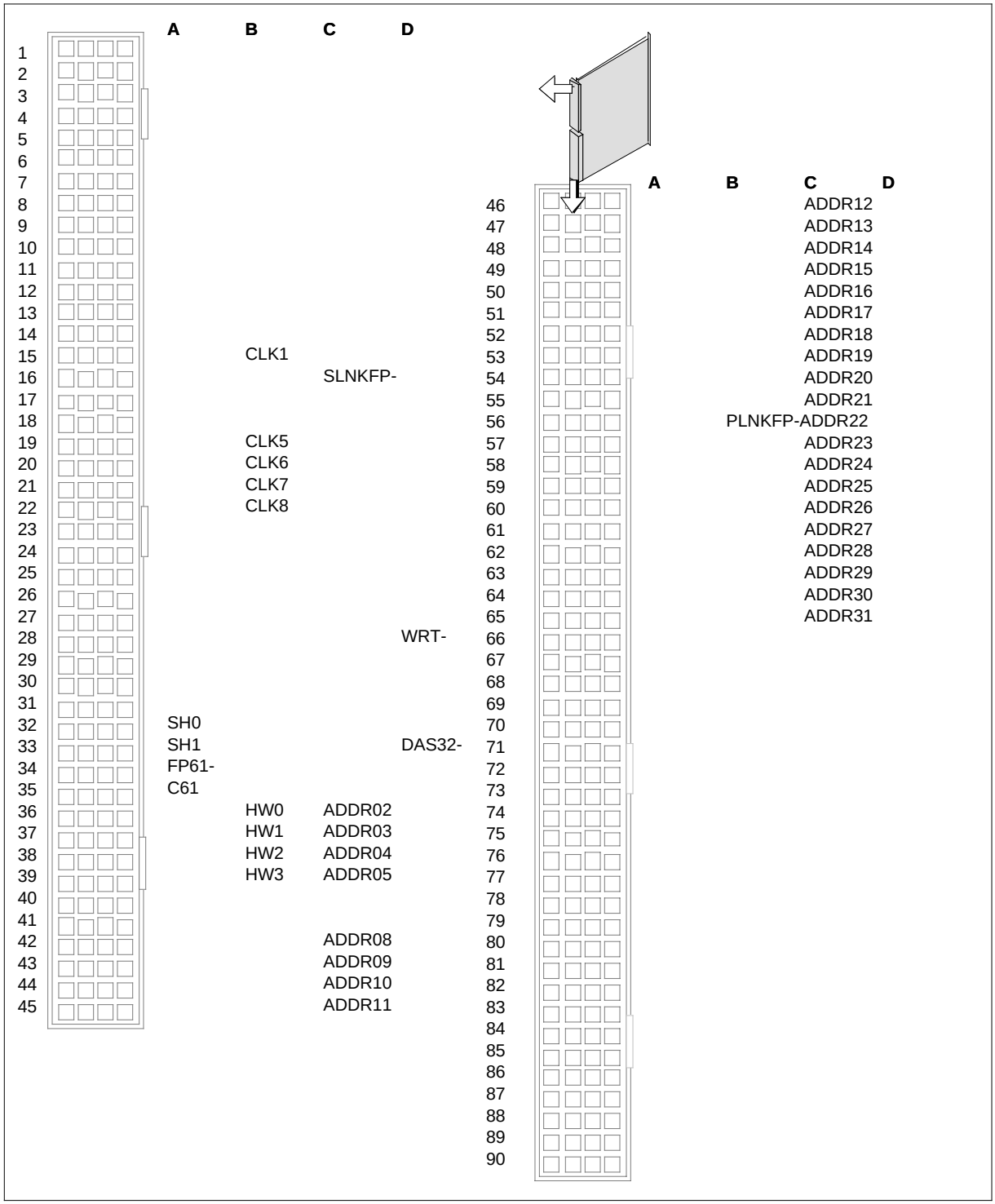
Signaling

Pin numbers

The pin numbers for the NT9X22CA appear in the following figure.

NT9X22CA (continued)

NT9X22CA pin numbers

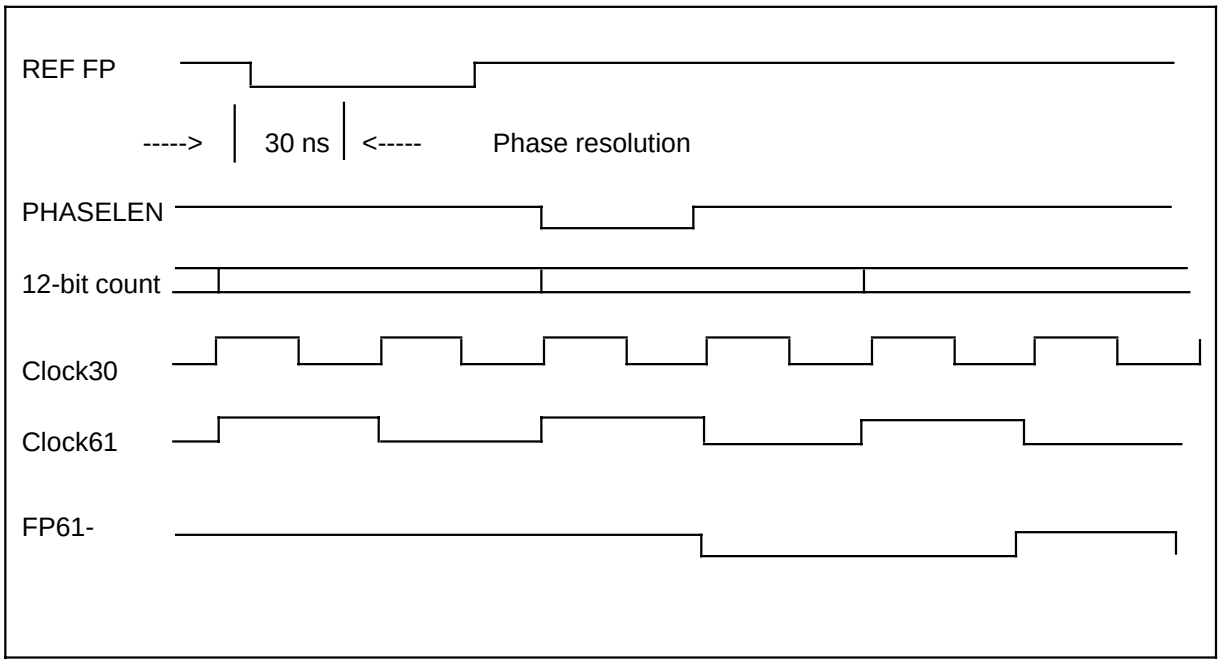


NT9X22CA (end)

Timing

The timing relationships for the NT9X22CA appear in the following figure.

NT9X22CA timing



Technical data

Power requirements

The required voltage is +5V.

NT9X23AA

Product description

The DMS-100 enhanced core system uses the NT9X23AA DS30 four-port paddle board. You can use NT9X23AA the with the NT9X17 message switch four-port card or the NT9X12 CPU port card.

Functional description

The NT9X23AA contains the following functions:

- provide an interface between a parallel 4.096 MHz backplane data bus and the twisted-pair transmission cables associated with four DS30 links
- transmit an out-of-band (OOB) reset code
- provide a local loopback
- provide a reference frame pulse

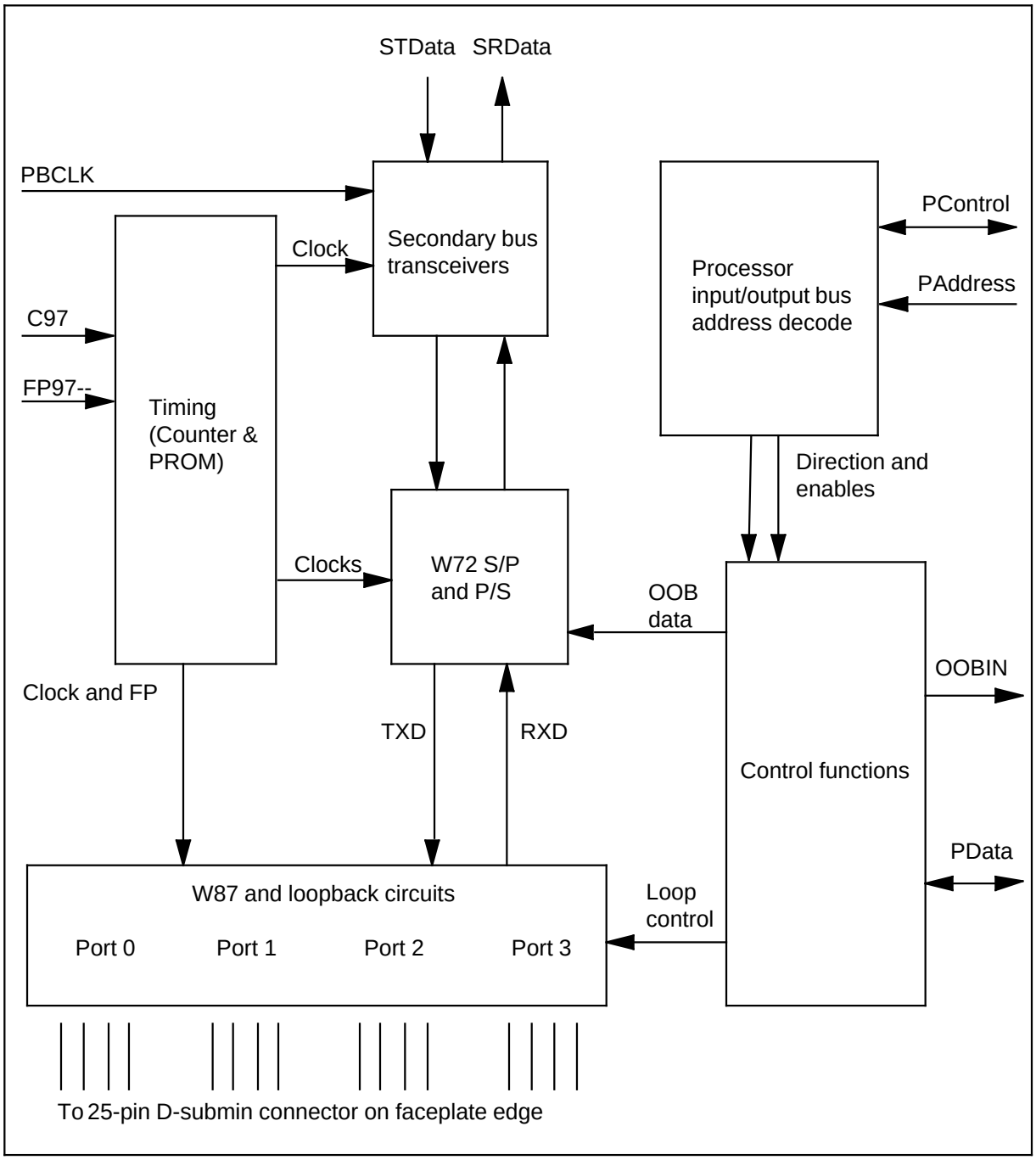
Functional blocks

Four blocks are available on the left side of the block diagram in the following figure. The blocks contain the circuits that transfers data. The right side of the block diagram shows the blocks involved in maintenance and control.

The relationship between the functional blocks appears in the following figure.

NT9X23AA (continued)

NT9X23AA functional blocks



Data transfer

The data transfer section contains circuit that converts parallel 4.096 MHz data to a serial 5.120 MHz stream. The circuits convert serial data to a parallel stream.

The data transfer section includes the following:

- the counter and PROM circuits
- secondary-bus (S-bus) transceivers
- two W72 formatters
- two W87 DS30 interface chips and the associated analog interface

The W72 formatter and the W87 DS30 interface chips require clocks and frame pulses. A PROM generates the clocks and frame pulses. A 5.12 MHz clock drives the counter chain that provides the addresses for the PROM. The backplane provides 10.24 MHz for the 5.12 MHz clock. The PROM and counter circuit generate several signals for OOB signaling.

The interface to the S-bus is the problem on this paddle board that is not hidden. The interface is not hidden in the low-speed interface (LSI) chips. The S-bus is a part of parallel data buses that have one direction that connect the card port to the paddle board (PB) port. The buses transmit and receive at 4.096 MHz.

The two W72 formatters provide serial-to-parallel or parallel-to-serial conversion on 20 ports of 10-bit 2.56 MHz data. Two 10-bit data streams are interleaved at the input and output of the W87 DS30 interface chip. This condition produces a 5.12 MHz clock rate. One formatter converts four channels (ports) of 10-bit parallel data to four serial streams. The other formatter provides serial-to-parallel conversion for another four ports.

Two W87 DS30 interface chips are present. The chips provide functions associated with the conversion of a serial transistor-transistor-logic (TTL) signal. The chips convert TTL to a biphase-encoded, differential signal and the reverse conversion. Each W87 chip has two ports. Each port has input and output pins, except for several shared control functions. Biphase encoding combines the transmit clock, frame pulse, and data for transmission. Differential drivers output the combined functions. A front-end amplifier shapes the received biphase signal for reception. The amplifier shapes the signal before the amplifier passes the signal to the clock recovery circuit and the data and frame pulse decode circuit. The amplifier writes the decoded signal to a 32-bit elastic buffer. A local clock and frame pulse reads the serial TTL data from the elastic buffer. Two ports share the local and transmit clocks and frame pulses.

NT9X23AA (continued)

Maintenance and control

A synchronous processor interface controls some functions of the NT9X23AA. These functions include the following:

- an OOB reset function
- a loopback function
- a reference frame pulse
- access to a rate stop (RS) flip-flop
- a read-only identification PROM

The OOB reset function can enable the transmission of a 5 A (Hex) code in bit 1 of every channel. The OOB function is available on each port.

The loopback function causes a multiplexer on the W87 to receive data inputs instead of the link receive data. The loopback function is available on each port. The data inputs select the transmit data.

The loopback function drives the receive frame pulse from the W87 port 0 on the backplane. This option provides a reference frame pulse for the NT9X22BA 10.240 MHz subsystem clock paddle board. The reference frame pulse for the NT9X22BA clock is available when computing module applications. The pulse is not a feature in 0D1 applications because the CM does not have the NT9X22BA. Provide the NT9X22CA with a reference frame pulse from the fiber link. Use the NT9X20 card to perform this action.

Access to an RS flip-flop function provides access to an RS flip-flop that indicates the PB is reset. The CP or the insertion of the PB in the backplane (power-up reset) resets the PB.

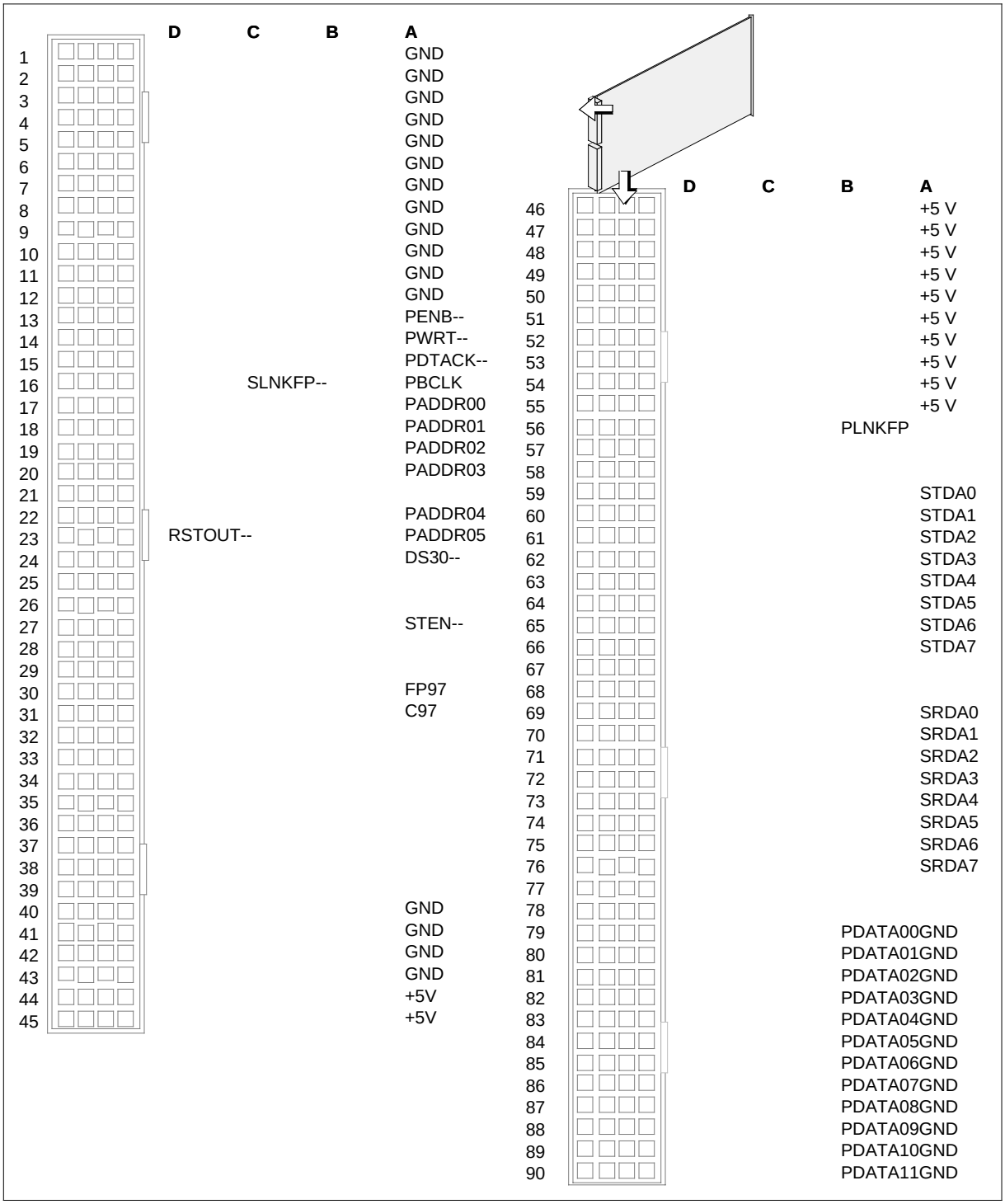
The read-only identification PROM function provides a read-only identification PROM. This PROM provides information about the card type and vintage.

Signaling

Pin numbers

The pin numbers for NT9X23AA appear in the following figure.

NT9X23AA pin numbers



NT9X23BA

Product description

The DS30 four-port paddle board (PB) is in use with the DMS SuperNode. The DS30 four-port PB provides the interface between a parallel 4.096 MHz backplane data bus and the twisted-pair transmission cables. The cables associate with four DS30 links. Secondary functions include:

- the transmission of out-of-band (OOB) data
- the reception of OOB data
- the supply of a reference frame pulse taken from the link

The NT9X23BA is in use with the NT9X17 message switch four-port card.

Functional description

The NT9X23BA contains the following functional blocks:

- data transfer
- maintenance and control

Data transfer

The data transfer section of the PB converts the parallel 4.096MHz data to a serial 5.120 MHz stream. The data transfer section converts in the reverse direction, from 5.120 MHz to 4.096 MHz. The data transfer section of the PB has counter and PROM circuits. The data transfer section of the PB also has shorting bus (S-bus) transceivers. The data transfer section of the PB also has two 72 chips, three W87 chips, and an associated analog interface.

The 72 chips provide conversion on 20 ports of 10-bit 2.56 MHz data. The W87 chips provide functions associated with the conversion of a serial transistor-transistor logic (TTL) signal to a biphase-encoded, differential signal. The conversion can be in the reverse direction biphase-encoded, differential signal to a serial TTL signal. The PROM provides clock and frame pulses the W72 and W87 chips require. The PROM and counter circuit generate signals for OOB signaling.

The S-bus is a pair of parallel data buses that have one direction that connect the port CP to port PB. Data transfers to and from the central processing unit (CPU) can be achieved in asynchronous or iso-synchronous form.

Maintenance and control

An asynchronous processor interface controls the following functions on the NT9X23BA:

- an OOB function on each port that enables the transmission of a byte of data in bit 1 of each channel
- a loopback function on each port that causes a multiplexer on the W87 receive-data inputs to select transmit data instead of link-receive data
- an ability to drive the extracted receive-frame pulse from any port on the backplane
- the access to an RS flip-flop indicates reset on the PB the CP or insertion in the backplane
- a read-only identification PROM provides card type and vintage information
- an enable for the slip RAM on port
- the selection of the port for the primary and secondary received frame pulses

Signaling

Timing

The timing relationship between the 4.096 MHz clock (BCLK) and the 5.120 MHz clock (LCLK) appears in the following figure.

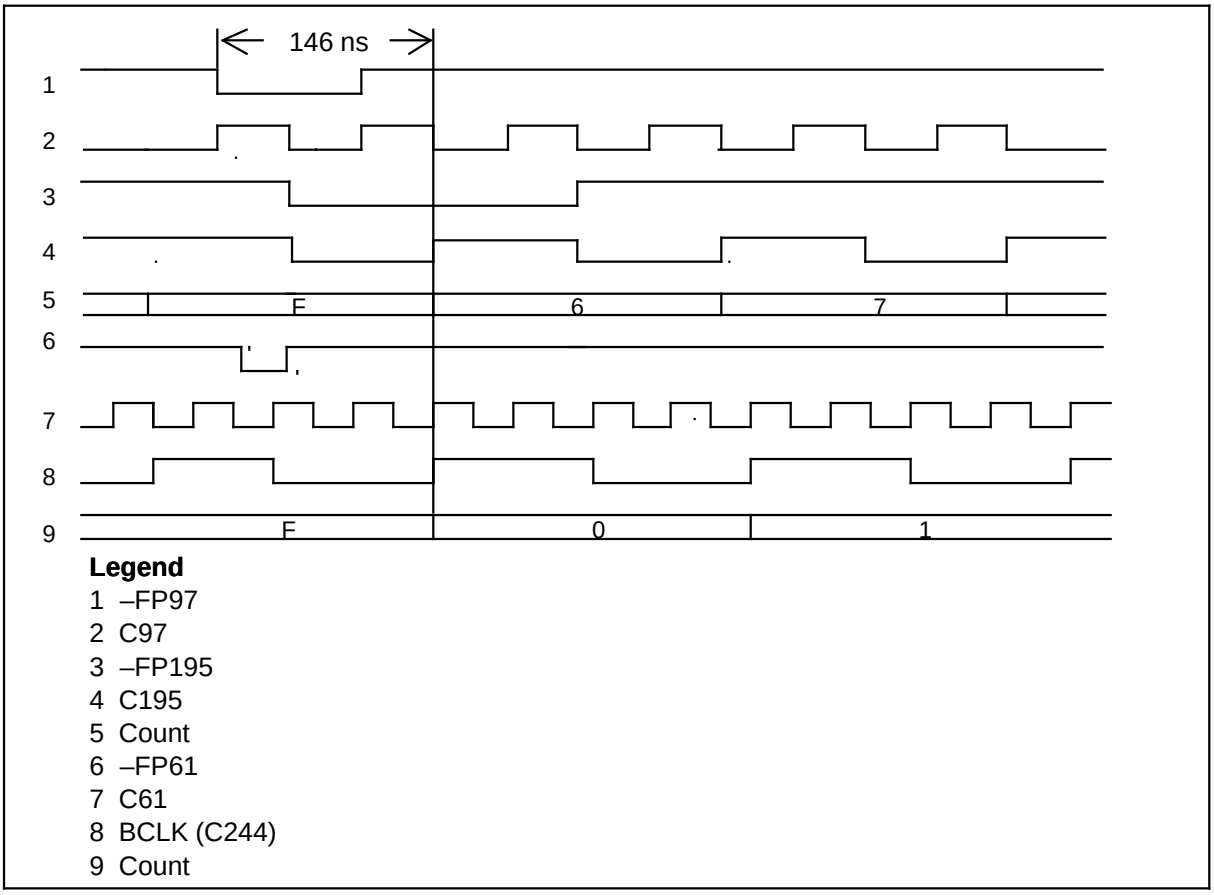
Technical data

Operation requirements

The NT9X23BA operates with a supply voltage of +5.0V dc, ±5%. The standard power requirement is 4.12W.

NT9X23BA (continued)

NT9X23BA timing



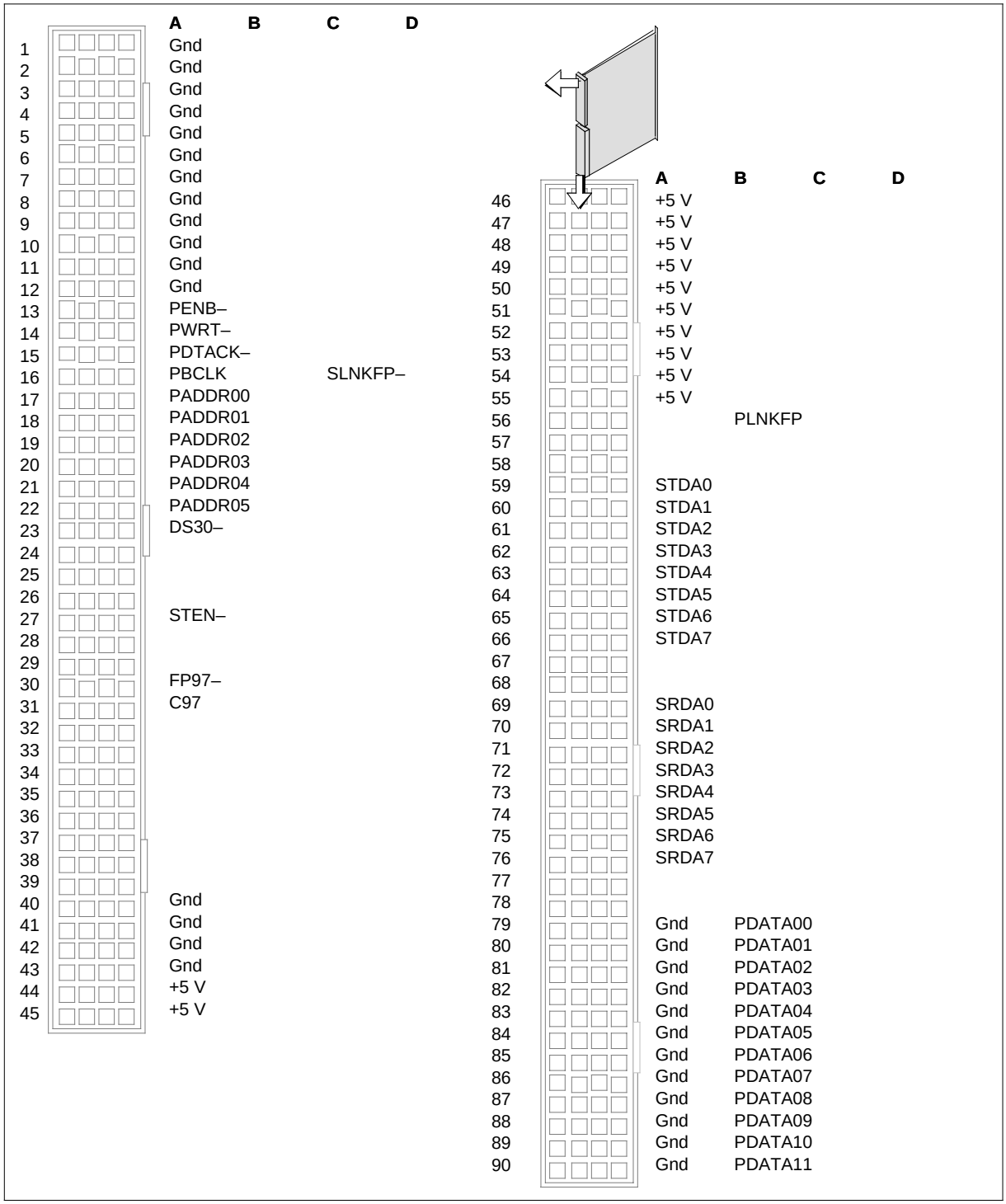
Legend

1 –FP97
2 C97
3 –FP195
4 C195
5 Count
6 –FP61
7 C61
8 BCLK (C244)
9 Count

Pin numbers

The pin numbers for NT9X appear in the following figure.

NT9X23BA pin numbers



NT9X25AA

Product description

In the DMS SuperNode, any DMS-bus allows packets of data to move between DS30 or DS512 links connected to the shelf. Paddle boards NT9X20BB (DS512 MSEN) and or BA connect the links to NT9X17CA port cards through the shorting bus (S-bus). These paddle boards can carry more channels than a single port card can handle. The NT9X25AA allows many port cards to share one link card.

The NT9X25AA uses an NT9X25BA to connect the S-bus of slot N to the S-bus of slot N+1. An NT9X25BA is an MS port expander/terminator paddle board that terminates the chain. The S-bus daisy chain uses the NT9X25AA between an NT9X20BB and an NT9X25BA.

Functional description

The NT9X25AA allows a maximum of four NT9X17CAs to share a NT9X20BB card.

Functional blocks

The NT9X25AA has the following functional blocks:

- processor-bus (P-bus) interface
- S-bus interface

Processor-bus interface

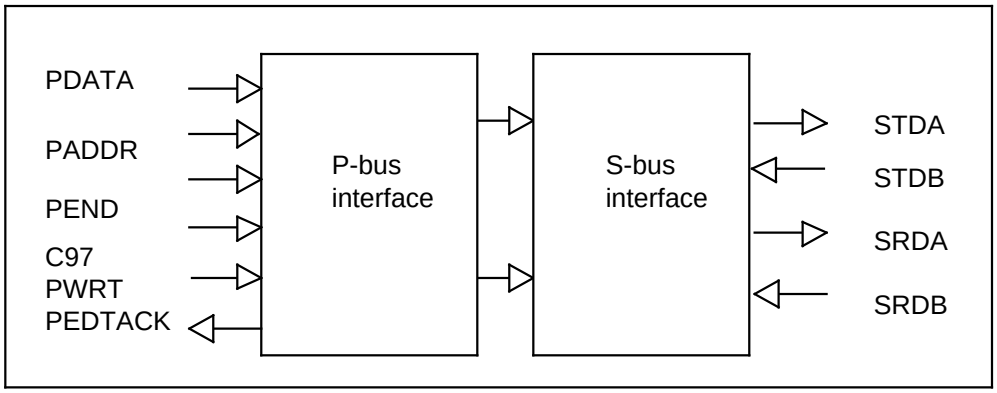
The P-bus interface contains all the logic required to interface the partial P-bus. The NT9X17CA provides the P-bus for the identification (ID) PROM and control register.

Shorting-bus interface

The S-bus interface connects the S-bus of slot N to the S-bus of slot N+1.

The relationship between these function blocks appears in the following figure.

NT9X25AA functional blocks



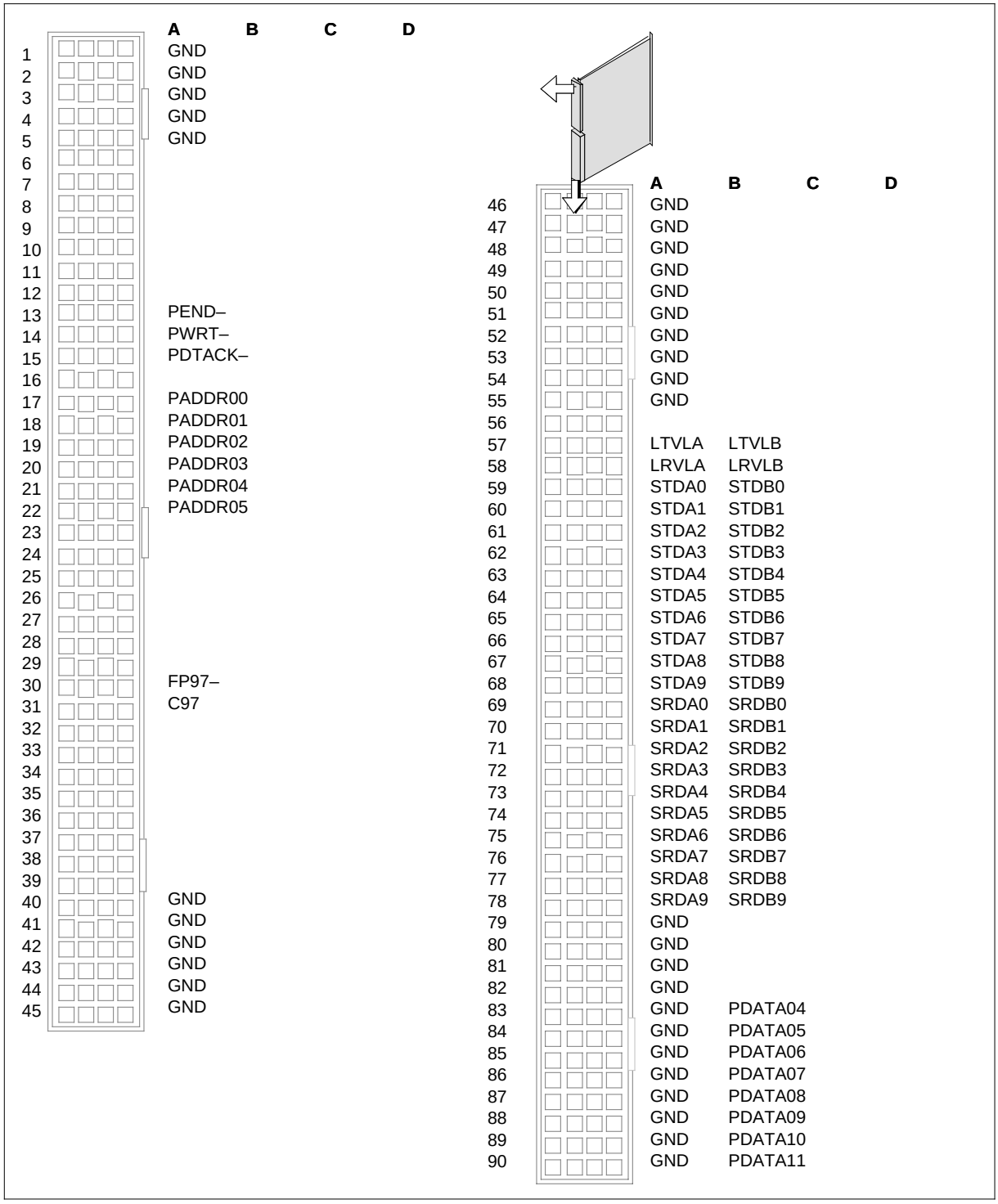
Signaling

Pin numbers

The pin numbers for NT9X25AA appear in the following figure.

NT9X25AA (continued)

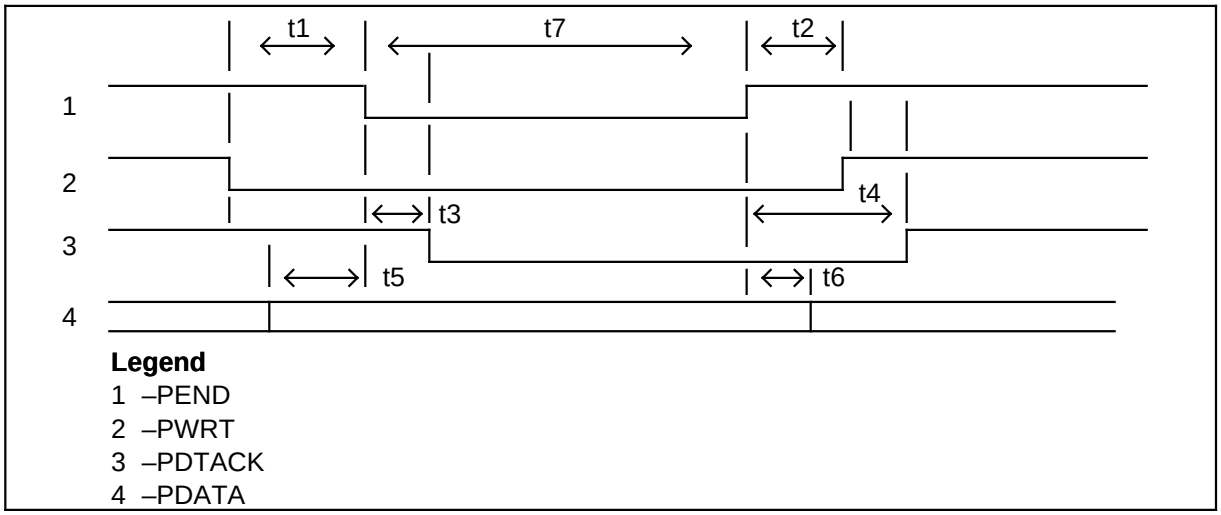
NT9X25AA pin numbers



Timing

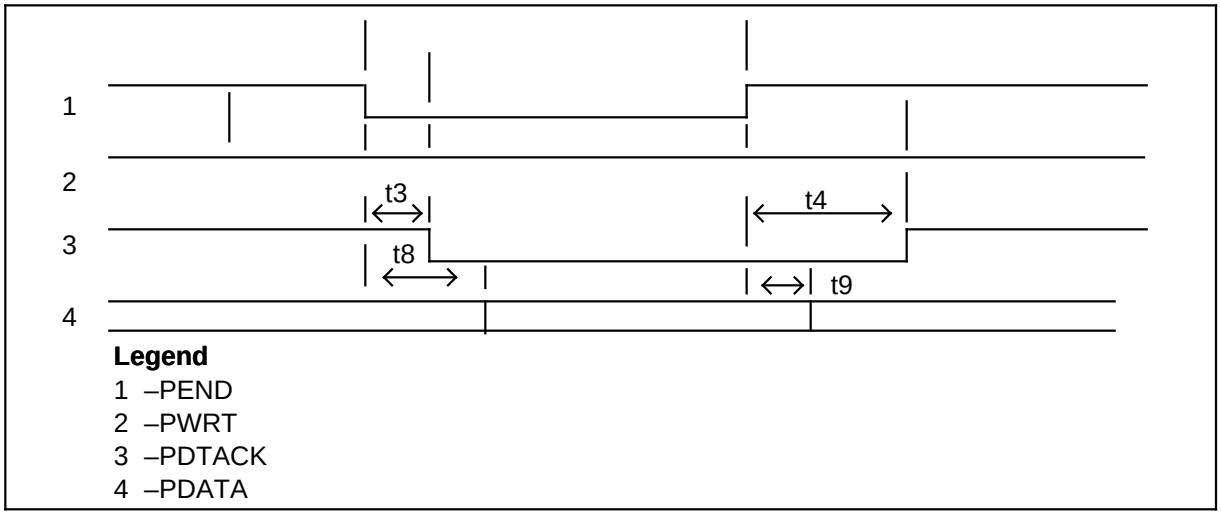
The processor WRITE and READ cycle timing appears in the following figures.

NT9X25AA processor WRITE cycle timing



Legend
1 –PEND
2 –PWRT
3 –PDTACK
4 –PDATA

NT9X25AA processor READ cycle timing



Legend
1 –PEND
2 –PWRT
3 –PDTACK
4 –PDATA

Technical data

Power requirements

The NT9X25AA requires a minimum of 4.25V, a nominal of 5V, and a maximum of 5.25V. The current requirement is 0.2A.

NT9X25BA

Product description

In the DMS SuperNode, any DMS-bus allows packets of data to route between DS30 or DS512 links connected to the shelf. Paddle boards NT9X20BB (DS512 MSEN) and NT9X25BA or NT9X25AA (MS port expander paddle board) connect the links to NT9X17CA port cards through the shorting bus (S-bus). These paddle boards carry more channels than one port card can handle. The NT9X25BA and NT9X25AA allow many port cards to share one link card. The NT9X25BA stops the extended S-bus.

Functional description

The NT9X25BA and NT9X25AA allow a maximum of four NT9X17CAs to share a NT9X20BB. The NT9X25BA is the final paddle board in the daisy chain that connects the S-bus of slot N to the S-bus of slot N+1. The NT9X25BA contains an identification (ID) PROM so the system can identify the card.

Functional blocks

The NT9X25BA contains the following functional blocks:

- processor-bus (P-bus) interface
- S-bus interface

Processor-bus interface

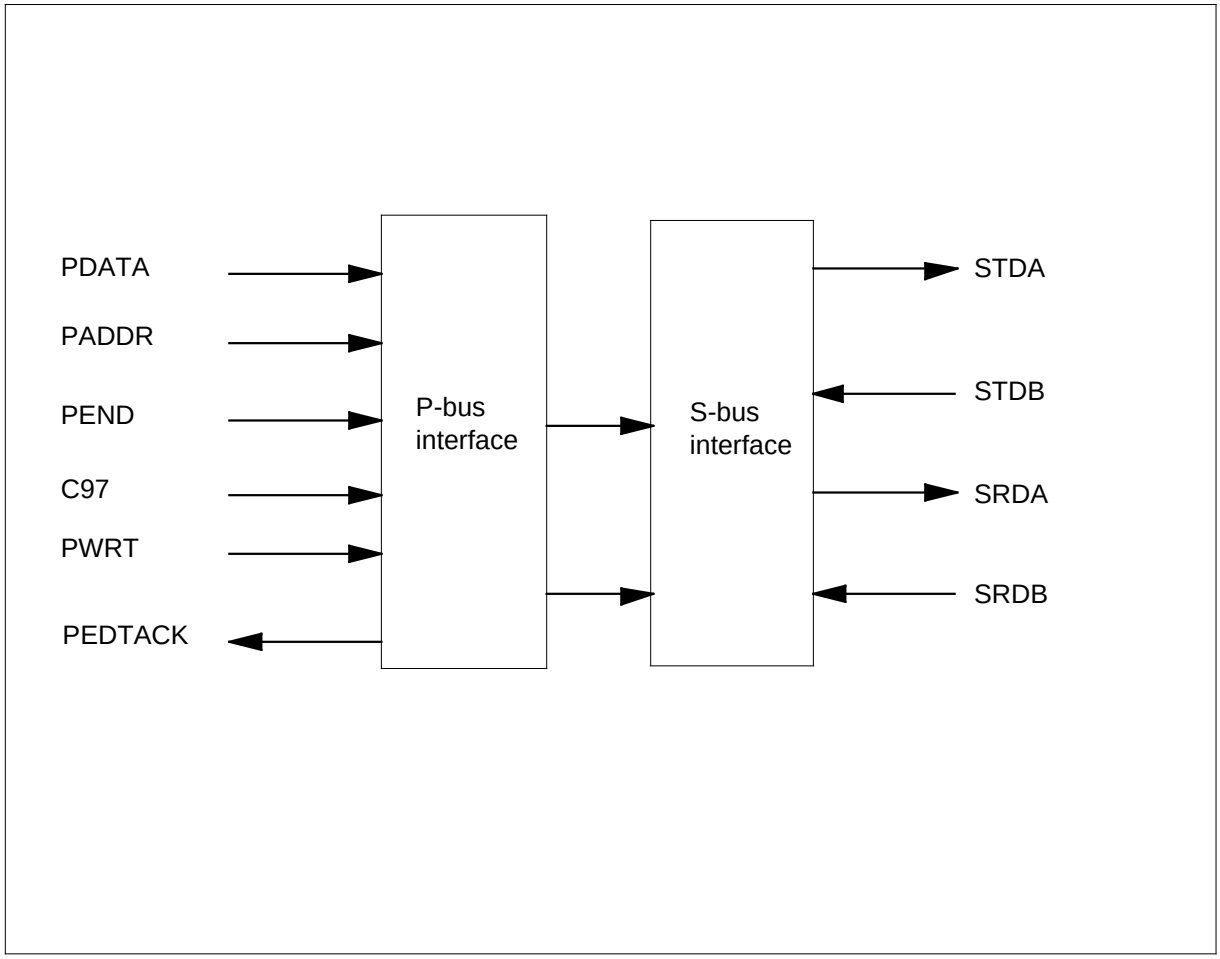
The NT9X17CA to the ID PROM and control register provide a P-bus interface. The P-bus interface contains the logic interface the partial P-bus requires.

Shorting-bus interface

The S-bus interface connects the S-bus of slot N to the S-bus of slot N+1. The S-bus interface also contains resistors to end the S-bus signals.

The relationship between the P-bus interface and the S-bus interface appears in the following figure.

NT9X25BA functional blocks



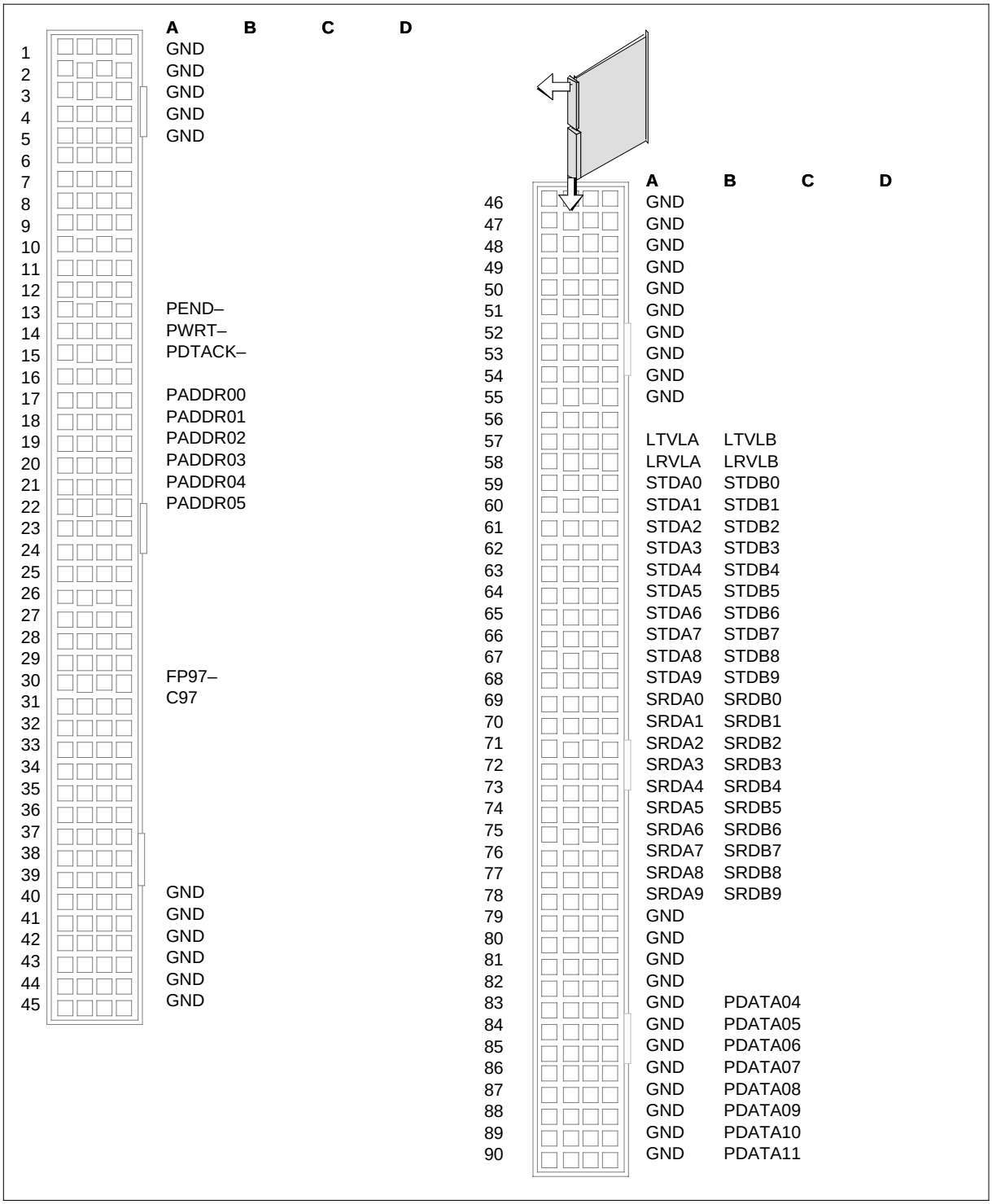
Signaling

Pin numbers

The pin numbers for NT9X25BA appear in the following figure.

NT9X25BA (continued)

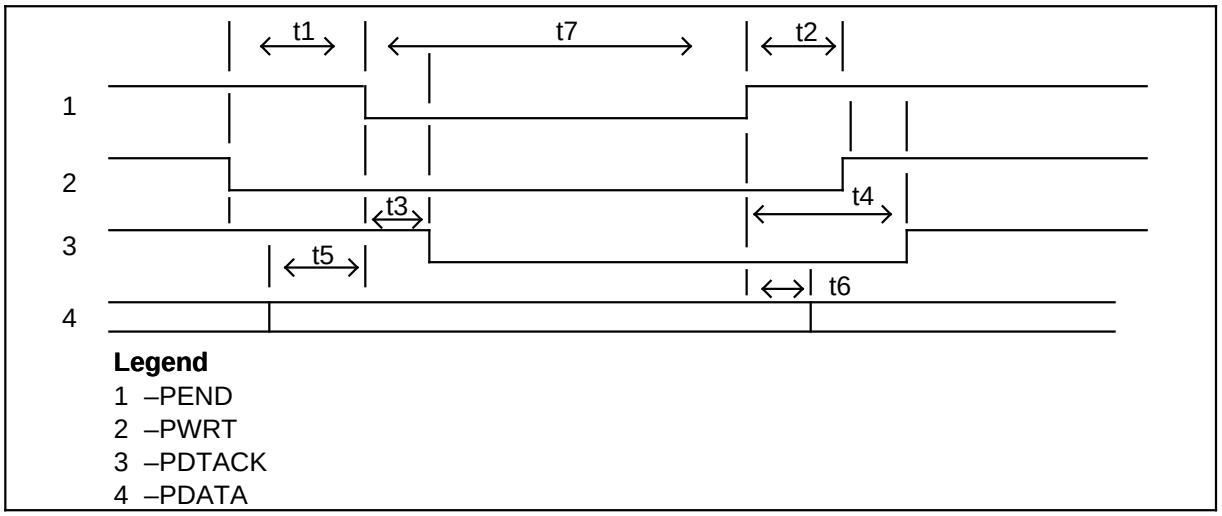
NT9X25BA pin numbers



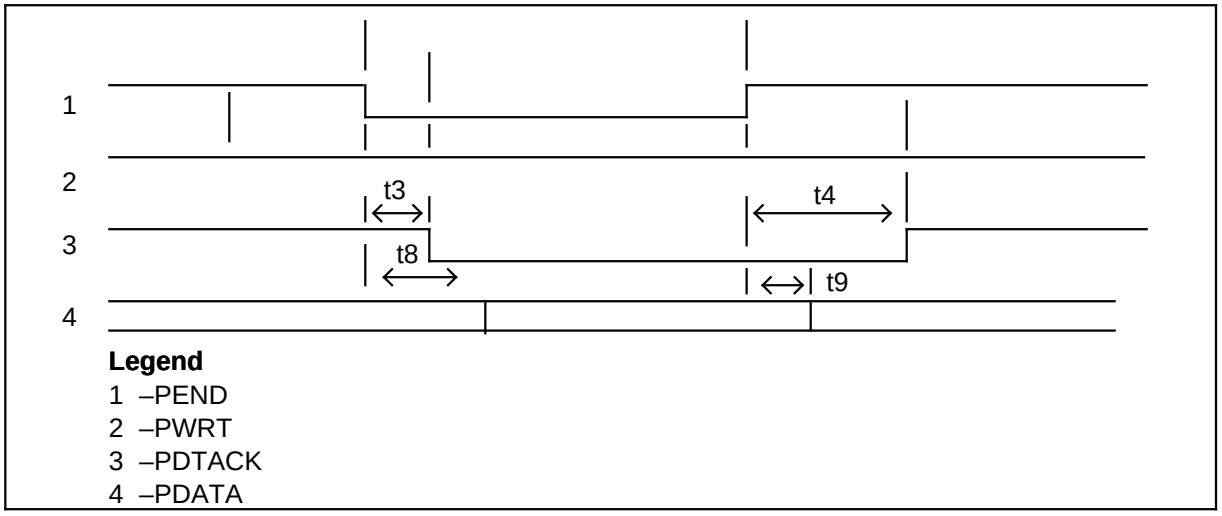
Timing

The processor WRITE and READ cycle timing appear in the following figures.

NT9X25BA processor WRITE cycle timing



NT9X25BA processor READ cycle timing



Technical data

Power requirements

The voltage requirements of the NT9X25BA are a minimum of 4.25V, a nominal of 5V, and a maximum of 5.25V. The current requirement is 0.2A.

NT9X26AA

Product description

The NT9X26AA remote terminal interface (RTIF) card monitors and controls the DMS100 SuperNode.

The remote system contains the following:

- an RTIF behind each 9X13 CPU
- two video display terminals (VDT), one for each DMS-Core RTIF
- an out-of-band (OOB) link between modules

The DMS100 SuperNode RTIF E2A feature provides the following:

- a serial data link to connect the CPU to an E2A digital alarm scanner (DAS)
- remote monitoring of the status of DMS100 SuperNode 9X13 DMS-Core circuit cards
- remote monitoring of the control lines on the DMS100 SuperNode 9X13 DMS-Core circuit cards
- remote control of the 9X13 CPUs

The OOB link between modules allows the DMS-Core to reset other nodes.

The NT9X26AA RTIF controls the following CPUs:

- 9X13BC
- 9X13DB
- 9X13DC
- 9X13FA
- 9X13GA
- 9X13HB
- 9X13JA
- 9X13KA
- 9X13LA
- 9X13MA

Location

The position the NT9X26AA holds in some cabinets appears in the following table.

Location of the NT9X26AA

Cabinet	Shelf	Slot
SuperNode	CM	19, 20
SuperNode	MS	9
ENET	ENET	7
LPP/LIU	LMS	17, 22

Functional description

The NT9X26AA RTIF system operates in a mode that monitors when the SuperNode equipment functions properly. When the equipment fails, operating company personnel use the remote system to return the system to service.

The remote system connects to the master DMS-Core. The master DMS-Core reboots the DMS-bus.

The RTIFs on the DMS-Core receive and run commands from the DMS-Core CPUs or from the VDT of each CPU. The RTIFs on the other SuperNode modules receive and run commands from the CPUs or the OOB links.

The local and remote VDTs provide a man-machine interface (HMI) to enter reset, boot and jam commands.

Functional blocks

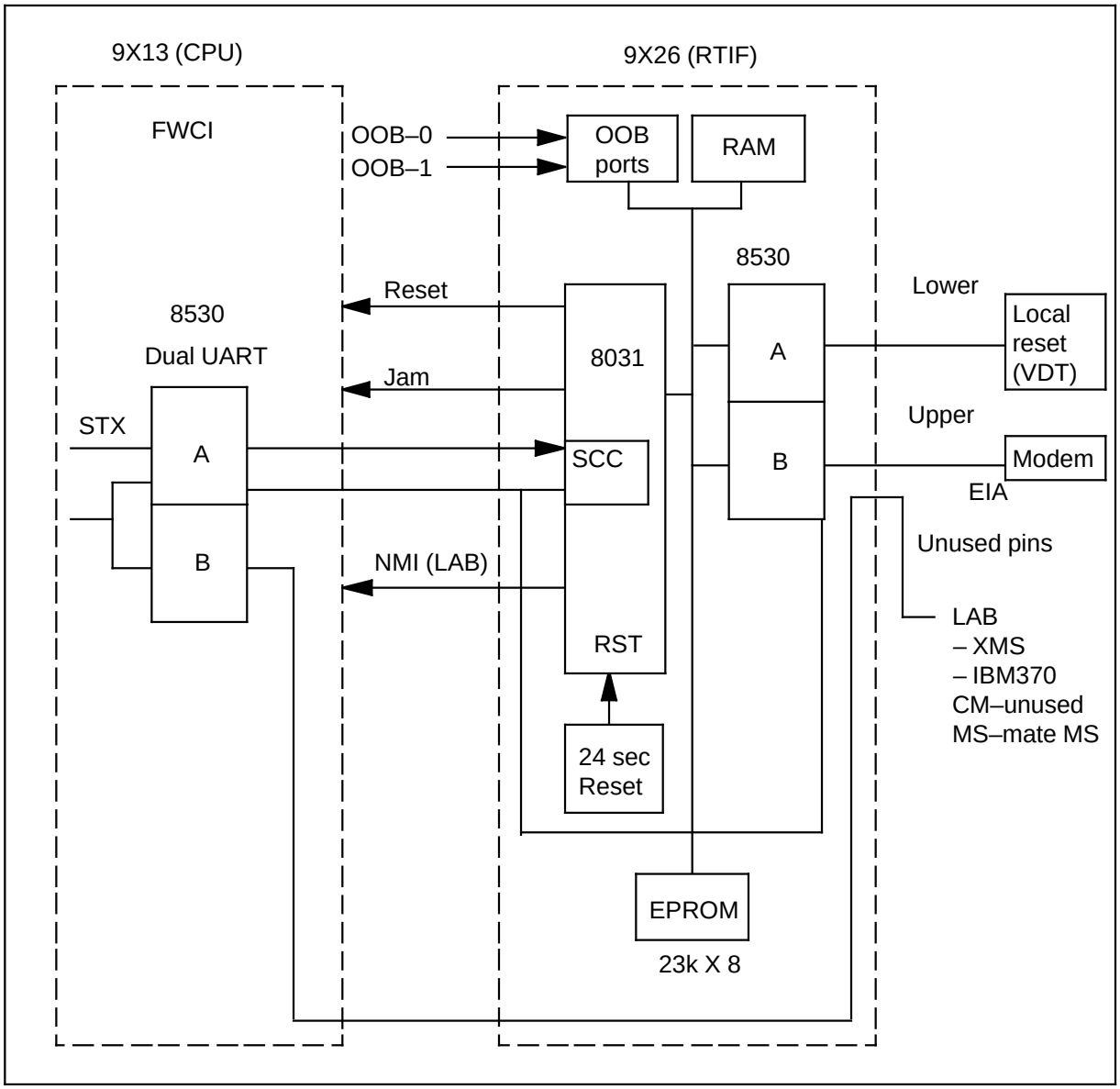
The NT9X26AA has the following functional blocks, or user inputs:

- local VDT
- remote VDT
- 9X13 serial interface
- OOB links

The relationship between the functional blocks appears in the following figure.

NT9X26AA (continued)

NT9X26AA functional blocks



Local video display terminal

The local and remote video display terminals provide a human-machine interface (HMI). Enter reset commands over the HMI. The local VDT has the highest priority of all the inputs.

Remote video display terminal

The remote and local video display terminals provide a human-machine interface (HMI). Enter reset commands over the HMI interface. The remote

VDT can be configured as a remote VDT link. The remote VDT responds like the local terminal, or an E2A link interface.

9X13 serial interface

The 9X13 serial interface is a maintenance link that checks the operation of the reset system. The RTIF operates in the transparent mode. The RTIF passes data between the terminals and the 9X13 interface. The identity of the VDT is not known to the 9X13. The 9X13 interface can accept any command that the VDT can accept. A one-to-one relationship is present between the 9X13 interfaces commands and responses and VDT commands and responses.

Out-of-band links

The OOB link forwards reset and control information between SuperNode modules. The OOB links run in one direction from a far-end module port paddle board to the RTIF. Two OOB links terminate on each RTIF, one from each plane of a DMS-Core or DMS-bus. The OOB link sends reset codes for a subsystem module over the links to the RTIF. The OOB can send any commands entered from the VDT. The system sends the commands to the VDTs because the OOB links do not provide a return path.

NT9X26AB

Product description

The NT9X26AB remote terminal interface (RTIF) paddle board (PB) creates a reset system. The reset system monitors and controls the subsystems of DMS-100 SuperNode and related subsystems like signaling transfer point (STP) and enhanced network (ENET).

A subsystem is a functional block of the DMS-100 that performs a specified task. A subsystem is a shelf or half-shelf of connected cards that work with an NT9X13 CPU.

When a subsystem functions correctly, the reset system is in a monitoring mode. If the CPU of a subsystem requires initialization to a known state starts the reset sequence. The reset system starts the reset sequence to start the NT9X13. Examples of known CPU states are maintenance, bootloading or error recovery.

Functional description

The reset system contains the following:

- an RTIF PB behind each NT9X13 CPU
- two or more video display terminals (VDT). Each DMS-core RTIF has one VDT.
- out-of-band (OOB) links between subsystems

The OOB cannot be blocked. Resets always pass through the OOB. A DS512 or DS30 link between subsystems can create an OOB link. The RTIFs on the DMS-core receive and execute commands from the CPUs, the OOB links, or the VDTs (if attached).

The E2A feature of the RTIF allows remote switching control center (SCC) monitoring and control of the DMS-SuperNode. The feature creates an RS-422 serial data link that provides the DMS-core with an interface to an E2A digital alarm scanner (DAS). This hardware can monitor the status and control lines on the NT9X13 CPU of the DMS-core from a remote terminal. The DAS unit allows some remote control over the SuperNode.

Functional blocks

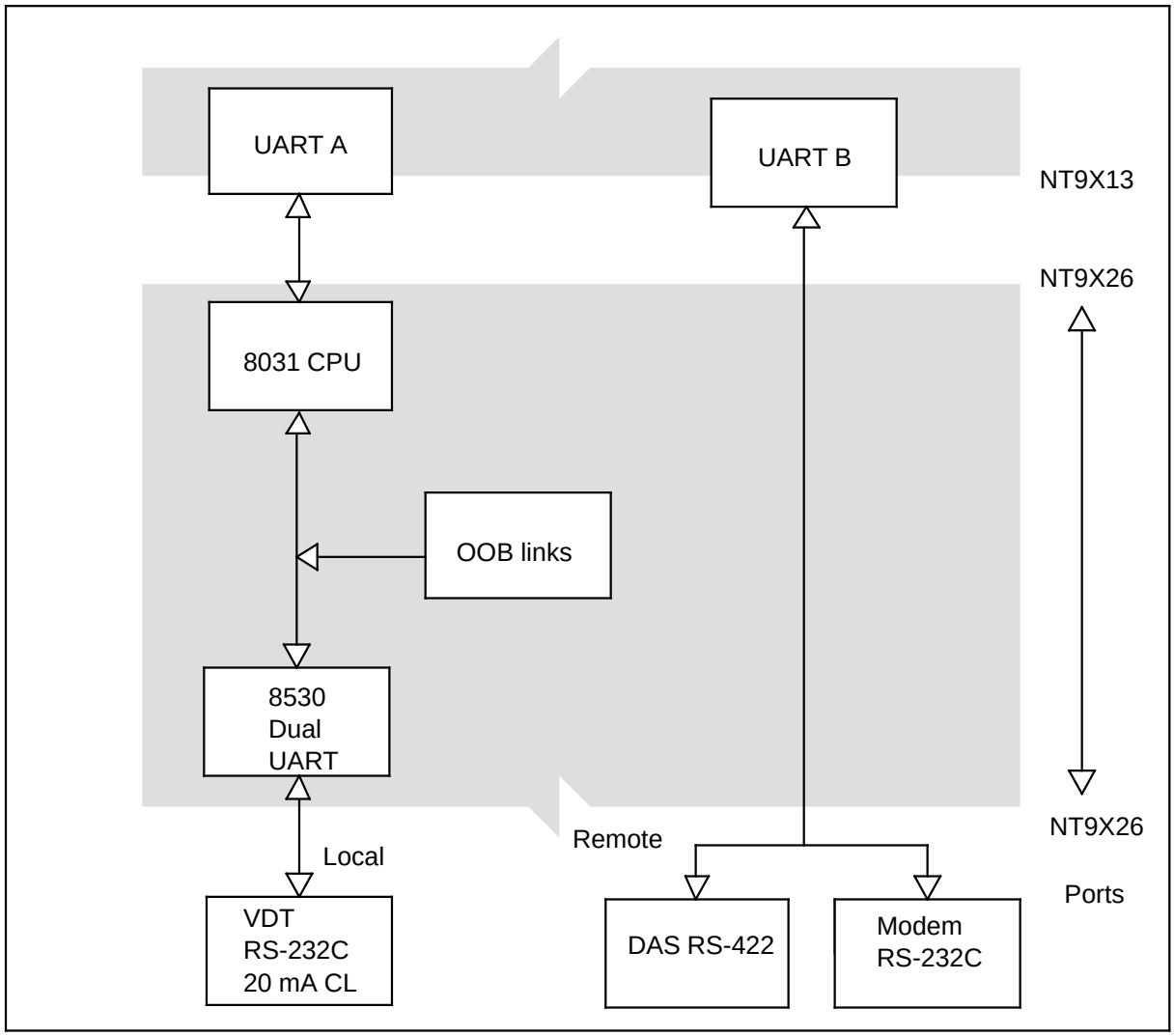
The NT9X26AB contains the following functional blocks:

- single chip controller
- dual universal asynchronous receiver/transmitter (UART)
- sanity timer

- master circuit
- OOB interface
- element identification (ID) PROM circuit
- status light-emitting diodes (LED)

The relationship between the functional blocks appears in the following figure.

NT9X26AB functional blocks



NT9X26AB (continued)

Single chip controller

In the remote terminal interface, the 8031 microcontroller does the following:

- manipulates operands in four address spaces
- initializes and operates the dual UART
- receives and interprets OOB resets
- provides the human-machine interface to the local and remote VDTs

Dual universal asynchronous receiver/transmitter

The RTIF contains a local port and a remote port. The ports provide an interface to a VDT and a modem. The dual UART (8530) is the main part of the interface.

The 8530 is a dual-channel, multiprotocol data communications peripheral. The 8530 is a serial-to-parallel, parallel-to-serial converter. The 8530 can perform a range of serial communications applications. The 8530 also has the diagnostic abilities to detect a failure in the network.

Sanity timer

The sanity timer counters are driven off the local oscillator. After the counters count for 24 s, the 8031 resets. The reset continues for 32 CPU clock pulses (2.9 ms).

Master circuit

When a VDT or modem connects to the local or remote port, the master circuit of the DMS-core RTIF activates. The master circuit prohibits wrong resets from the OOB links.

Out-of-band interface

The OOB interface collects OOB link data from the port PB. The port PB sends the data over the DS512 or DS30 links.

Identification PROM circuit

The ID PROM is burned with the following:

- product equipment code (PEC)
- the hardware release of the card
- the base release
- present release of the firmware

Status light-emitting diodes

The NT9X26AB includes two status indicators on the faceplate. These LEDs have the same function as the LEDs of the DMS-core NT9X13 CPU.

When the top LED (green) glows, the NT9X13 CPU runs in lock-step synchronization with the mate of the NT9X13 CPU. This LED is only important when the RTIF is in a DMS-core shelf.

The bottom LED (red) indicates the maintenance status of the subsystem. If this LED glows, the subsystem NT9X13 CPU is not active (DMS-core) or out-of-service (DMS-bus, DMS0STP, or ENET). If this LED is off, the CPU is active (DMS-core) or in-service (DMS-bus, DMS-STP, or ENET).

NT9X26DA

Product description

The NT9X26DA reduced instruction set computer (BRISC) remote terminal interface (RTIF) paddle board incorporates the features of all current RTIF cards.

The NT9X26DA provides the following:

- CPU firmware (CPUFW) PROM residence for the NT9X10AA and the NT9X13MA CPU cards
- a reset system to monitor and control the subsystems of the DMS-100 SuperNode and related subsystems

Functional description

The NT9X26DA starts the CPU reset sequence for maintenance, bootloading, and error recovery. The NT9X26DA forces the associated CPU to become inactive.

The NT9X26DA repeatedly displays the CPU activity state, synchronization state, clock status and activity. The NT9X26DA also displays the DMS hexadecimal CPU board information.

The NT9X26DA accepts user input from five sources. The five sources follow:

- local and remote interfaces
- the CPU main board
- the two backplane out-of-band (OOB) links

The NT9X26DA can carry the CPU card PROM for executable firmware. The NT9X26DA supports remote splitter control mode for captive office use.

Functional blocks

The NT9X26DA contains the following functional blocks:

- sanity timer
- power fail detector
- OOB subsystem
- microcontroller subsystem
- serial communication controller (SCC) subsystem
- identification (ID) PROM and CPU firmware subsystem
- light-emitting diode (LED) display

Sanity timer

The sanity timer resets the microcontroller. The sanity timer uses the microcontroller if the microcontroller does not receive characters from the following within 24 s:

- the associated CPU card
- the local reset terminal interface
- the remote reset terminal interface

The microcontroller receives an interrupt 0.75 seconds before reset, and resets the sanity timer.

Power fail detector

The power fail detector circuit holds the card in reset mode when the +5V supply is below safe levels for operation.

Out-of-band subsystem

The OOB subsystem sends OOB messages to the microcontroller. The messages reset the associated CPU card if the RTIF is in a slave subsystem. A DMS bus or an enhanced network is a slave subsystem.

Microcontroller subsystem

The microcontroller subsystem contains an Intel 8031 microcontroller and associated registers. Port 3 of the microcontroller communicates directly with channel A of the associated CPU board. The microcontroller can access the CPU card signals to perform the following:

- reset the CPU
- jam the CPU inactive
- disable the CPU sanity timer
- interrupt the CPU at the highest level

The RTIF microcontroller subsystems in the same SuperNode DMS-core processor shelf exchange jam status. The subsystems exchange jam state to make sure that both associated CPUs are not inactive at the same time.

Serial communications controller subsystem

The SCC subsystem provides the serial communications channels A and B. Channel A connects the RTIF microcontroller to the local reset terminal interface.

NT9X26DA (continued)

The microcontroller can switch channel B to one of the following:

- the remote reset terminal at EIA RS232C voltage levels
- the remote reset terminal at EIA RS422 voltage levels
- loopback

The remote reset terminal interface that connects to channel B can bypass channel B. The remote reset terminal interface connects to channel B of the associated CPU card for simplex operation. A DMS bus is a simplex operation.

Identification PROM and CPU firmware subsystem

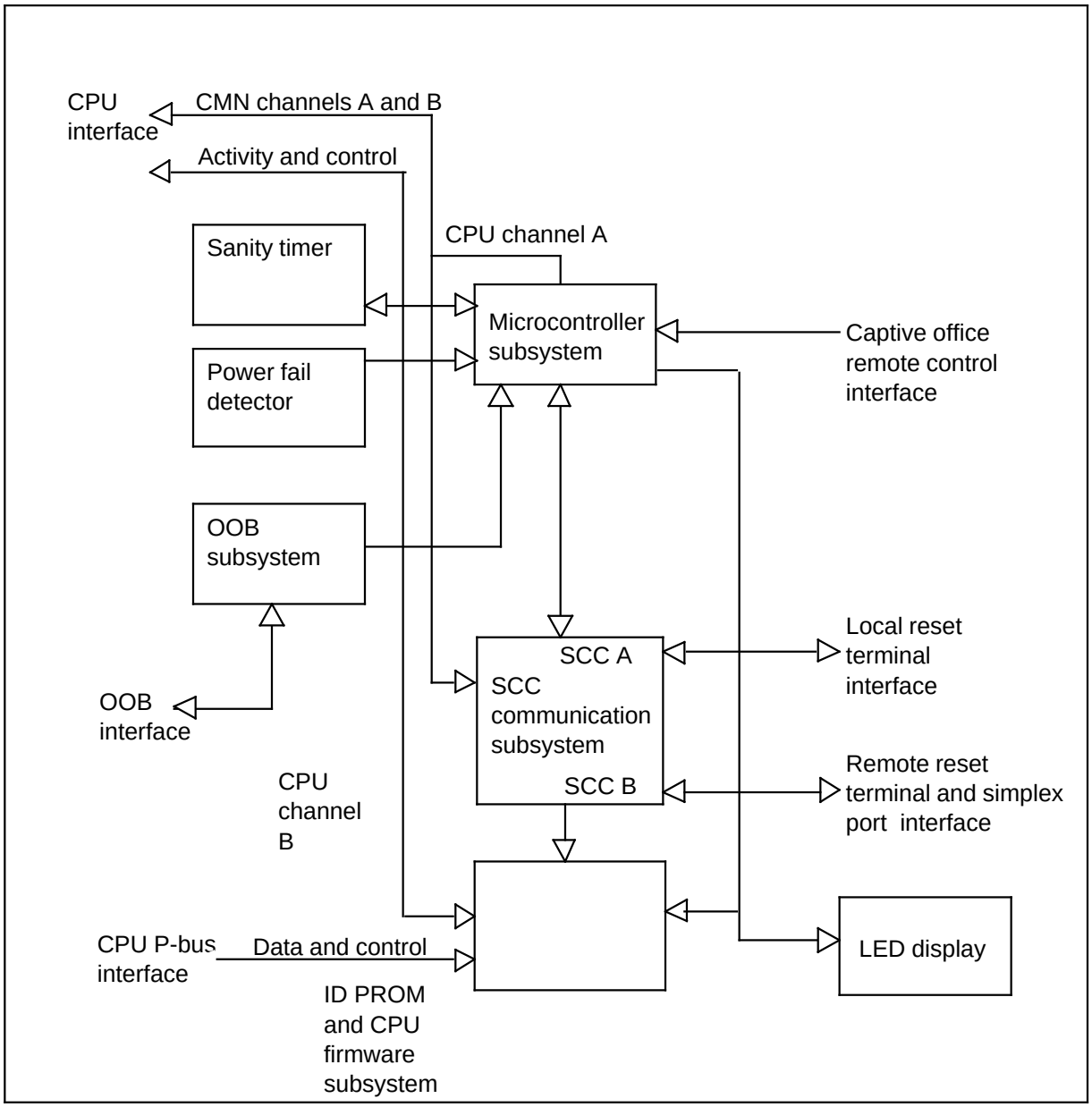
The RTIF provides a standard SuperNode 32B ID PROM which responds on the P-bus as a 32-bit device with even parity.

LED display

The green LED indicates that the local CPU cards in DMS-core applications have synchronization. The red LED indicates that the local plane CPU card is inactive or out of service.

The relationship between the functional blocks appears in the following figure.

NT9X26DA functional blocks



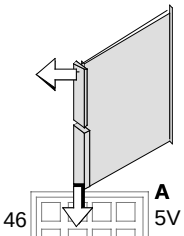
Signaling

Pin numbers

The pin numbers for the NT9X26DA appear in the following figure.

NT9X26DA (continued)

NT9X26DA pin numbers



	A	B	C	D
1	GND			
2	GND			
3	GND			
4	GND			
5	GND			
6				
7				
8				
9				
10				
11				
12				
13	RXDAP			
14	CARTD28			MASTERN
15	CARDT29		IJAMIN	PLN0N
16			GND	OOBIN0
17	DTRAN			
18	TXDAP			
19				
20	DCDAN			
21	RTSAN			OOBIN1
22	BPRXDBP			
23	CARTD30			
24	CARTD31			
25			BEN0N	BEN1N
26	BPDTRBN	BEN2N	BEN3N	
27	BPTXDBP		BASTN	GND
28			GND	WRTN
29			DTACKN	EDTACKN
30				PARITYP
31				PRTYENN
32			GND	
33			CPUCLK	DAS32N
34	FP61N		BACKN	DATA00
35	C61	TYPE1		DATA01
36		HW0	ADDR02	DATA02
37		HW1	ADDR03	DATA03
38		HW2	ADDR04	DATA04
39		HW3	ADDR05	DATA05
40	GND	CMACTN	ADDR06	DATA06
41	GND		ADDR07	DATA07
42	GND	CMSYNCN	ADDR08	DATA08
43	GND	PBRSTP	ADDR09	DATA09
44	5V	PBRSTN	ADDR10	DATA10
45	5V		ADDR11	DATA11

Legend

MVDTDC = MVDTDCDN
MMDMD = MMDMDCDN

	A	B	C	D
46	5V	DABSANN	ADDR12	DATA12
47	5V	GND	ADDR13	DATA13
48	5V	FACKN	ADDR14	DATA14
49	5V	ENOMN	ADDR15	DATA15
50	5V	MVDTDC	ADDR16	DATA16
51	5V	MMDMD	ADDR17	DATA17
52	5V	VDTDCDN	ADDR18	DATA18
53	5V	MDMDCDN	ADDR19	DATA19
54	5V	OJAMIN	ADDR20	DATA20
55	5V	ROMVPP	ADDR21	DATA21
56	TYPE0	ROMPGMP	ADDR22	DATA22
57			ADDR23	DATA23
58			ADDR24	DATA24
59			ADDR25	DATA25
60			ADDR26	DATA26
61	GND	ROMOEN	ADDR27	DATA27
62	CARTCK	CARTD10	ADDR28	DATA28
63	CARTINTN	CARTD11	ADDR29	DATA29
64	CARTD00	CARTD12	ADDR30	DATA30
65	GND	CARTD13	ADDR31	DATA31
66	GND	CARTD14		
67	CARTD01	CARTD15		
68	CARTD02	CARTD16		
69	CARTD03	CARTD17	CARTD27	
70	GND	CARTD18		
71	GND	CARTD19		
72	CARTD04	CARTD20		
73	CARTD05	CARTD21		
74	CARTD06	CARTD22		
75	GND	CARTD23		
76	CARTD07	CARTD24		
77	CARTD08	CARTD25		
78	CARTD09	CARTD26		
79	GND			
80	GND	BPRTSBN		
81	GND			
82	GND			
83	GND			
84	GND	FWPROMN		
85	GND	NMIN		
86	GND	CKFLN		
87	GND	CKACTN		
88	GND	JAMIN		
89	GND	IDPROMN		
90	GND	RISCN		

The pin numbers for the J1 and J2 connectors appear in the following tables.

Connector J1 signals

Pin	Signal	Pin	Signal
1	SGNDM	12	R1N
2	TXDM	13	T1P
3	RXDM	14	T0P
4	RTSM	16	R0P
5	CTSM	18	R0N
6	DCDM	19	T0N
7	GND	21	SPLITP
9	LABP	22	SPLITN
10	LABN	25	T1N
11	R1P		

Connector J2 signals

Pin	Signal	Pin	Signal
1	SGNDV	8	CLENBN
2	TXDV	20	DTRV
3	RXDV	21	CLRXDN
4	RTSV	22	CLRXDP
5	CTSV	23	CLTXDN
6	DCDV	24	CLTXDP
7	GND		

Technical data

Power requirements

The NT9X26DA requires a single +5V ±0.25V. The card uses an estimated 13.5W when equipped for captive office use.

NT9X26DB

Product description

The NT9X26DB reduced instruction set computer (BRISC) remote terminal interface (RTIF) paddle board has the features of all current RTIF cards. The NT9X26DB provides CPU firmware (CPUFW) PROM residence for the NT9X10AA and the NT9X13MA CPU cards. This card provides a reset system to monitor and control the subsystems of the DMS-100 SuperNode and related subsystems.

Functional description

The NT9X26DB starts the CPU reset sequence for maintenance, bootloading and error recovery. The NT9X26DB forces the associated CPU inactive. The NT9X26DB repeatedly displays the CPU activity state, synchronization state, clock status and clock activity. The NT9X26DB displays the DMS hexadecimal CPU board information.

The NT9X26DB accepts user input from five sources. The five sources follow:

- local and remote interfaces
- the CPU main board
- the two backplane out-of-band (OOB) links

The NT9X26DB can carry the CPU card PROM for executable firmware. The NT9X26DB supports a remote splitter control mode for captive office use.

Functional blocks

The NT9X26DB contains the following functional blocks:

- sanity timer
- power fail detector
- OOB subsystem
- microcontroller subsystem
- serial communication controller (SCC) subsystem
- identification (ID) PROM and CPU firmware subsystem
- light-emitting diode (LED) display

Sanity timer

The sanity timer resets the microcontroller. The sanity timer resets the microcontroller if the microcontroller does not receive characters from one of the following within 24 s:

- associated CPU card
- local reset terminal interface
- remote reset terminal interface

The microcontroller receives an interrupt 0.75 seconds before reset, and resets the sanity timer.

Power fail detector

The power fail detector circuit holds the card in reset mode when the +5V supply is below safe levels for operation.

Out-of-band subsystem

The OOB subsystem sends OOB messages to the microcontroller. The messages reset the associated CPU card if the RTIF is in a slave subsystem. A DMS bus or an enhanced network is a slave subsystem.

Microcontroller subsystem

The microcontroller subsystem contains an Intel 8031 microcontroller and associated registers. Port 3 of the microcontroller communicates directly with channel A of the associated CPU board.

The microcontroller can access the CPU card signals to perform the following:

- reset the CPU
- jam the CPU inactive
- disable the CPU sanity timer
- interrupt the CPU at the highest level

The RTIF microcontroller subsystems in the same SuperNode DMS-core processor shelf exchange jam status. The subsystems exchange jam status to make sure that both associated CPUs are not inactive at the same time.

Serial communications controller subsystem

The SCC subsystem provides the serial communications channels A and B. Channel A connects the RTIF microcontroller to the local reset terminal interface.

NT9X26DB (continued)

The microcontroller can switch Channel B to one of the following:

- remote reset terminal at EIA RS232C voltage levels
- remote reset terminal at EIA RS422 voltage levels
- loopback

The remote reset terminal interface that connects to channel B can bypass channel B. The remote reset terminal interface connects to channel B of the associated CPU card for simplex operation. A DMS bus is a simplex operation.

Identification PROM and CPU firmware subsystem

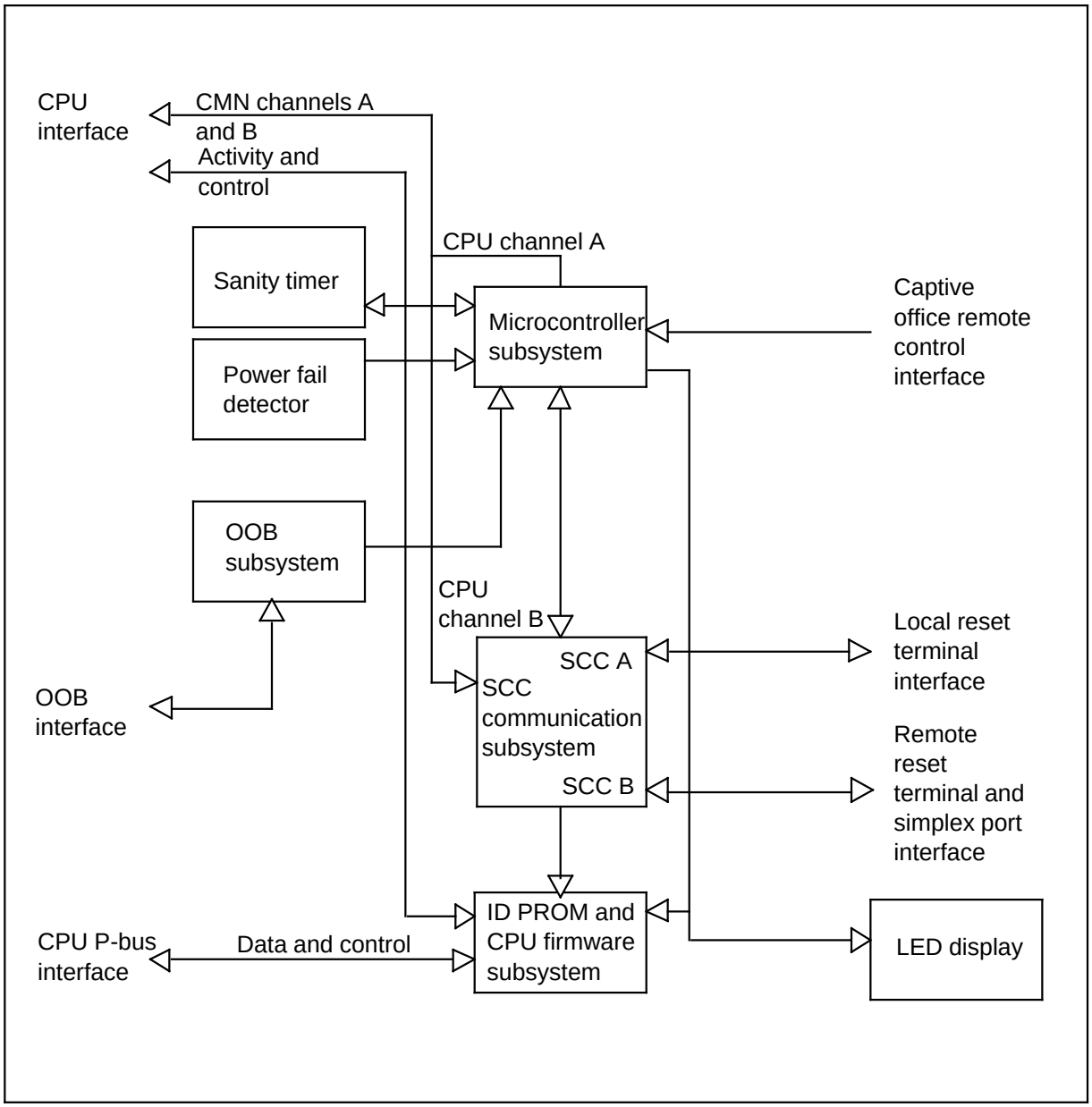
The RTIF provides a standard SuperNode 32B ID PROM which responds on the P-bus as a 32-bit device with even parity.

LED display

The green LED indicates that the local CPU cards in DMS-core applications have synchronization. The red LED indicates that the local plane CPU card is inactive or out of service.

The relationship between the functional blocks appears in the following figure.

NT9X26DB functional blocks



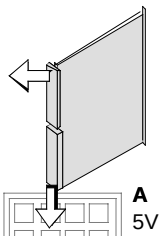
Signaling

Pin numbers

The pin numbers for the NT9X26DB appear in the following figure.

NT9X26DB (continued)

NT9X26DB pin numbers



	A	B	C	D
1	GND			
2	GND			
3	GND			
4	GND			
5	GND			
6				
7				
8				
9				
10				
11				
12				
13	RXDAP			
14	CARTD28			MASTERN
15	CARDT29		IJAMIN	PLN0N
16			GND	OOBIN0
17	DTRAN			
18	TXDAP			
19				
20	DCDAN			
21	RTSAN			OOBIN1
22	BPRXDBP			
23	CARTD30			
24	CARTD31			
25			BEN0N	BEN1N
26	BPDTRBN	BEN2N	BEN3N	
27	BPTXDBP		BASTN	GND
28			GND	WRTN
29			DTACKN	EDTACKN
30				PARITYP
31				PRTYENN
32			GND	
33			CPUCLK	DAS32N
34	FP61N		BACKN	DATA00
35	C61	TYPE1		DATA01
36		HW0	ADDR02	DATA02
37		HW1	ADDR03	DATA03
38		HW2	ADDR04	DATA04
39		HW3	ADDR05	DATA05
40	GND	CMACTN	ADDR06	DATA06
41	GND		ADDR07	DATA07
42	GND	CMSYNCN	ADDR08	DATA08
43	GND	PBRSTP	ADDR09	DATA09
44	5V	PBRSTN	ADDR10	DATA10
45	5V		ADDR11	DATA11

Legend

MVDTDC = MVDTDCDN
MMDMD = MMDMDCDN

	A	B	C	D
46	5V	DABSANN	ADDR12	DATA12
47	5V	GND	ADDR13	DATA13
48	5V	FACKN	ADDR14	DATA14
49	5V	ENOMN	ADDR15	DATA15
50	5V	MVDTDC	ADDR16	DATA16
51	5V	MMDMD	ADDR17	DATA17
52	5V	VDTDCDN	ADDR18	DATA18
53	5V	MDMDCDN	ADDR19	DATA19
54	5V	OJAMIN	ADDR20	DATA20
55	5V	ROMVPP	ADDR21	DATA21
56	TYPE0	ROMPGMP	ADDR22	DATA22
57			ADDR23	DATA23
58			ADDR24	DATA24
59			ADDR25	DATA25
60			ADDR26	DATA26
61	GND	ROMOEN	ADDR27	DATA27
62	CARTCK	CARTD10	ADDR28	DATA28
63	CARTINTN	CARTD11	ADDR29	DATA29
64	CARTD00	CARTD12	ADDR30	DATA30
65	GND	CARTD13	ADDR31	DATA31
66	GND	CARTD14		
67	CARTD01	CARTD15		
68	CARTD02	CARTD16		
69	CARTD03	CARTD17	CARTD27	
70	GND	CARTD18		
71	GND	CARTD19		
72	CARTD04	CARTD20		
73	CARTD05	CARTD21		
74	CARTD06	CARTD22		
75	GND	CARTD23		
76	CARTD07	CARTD24		
77	CARTD08	CARTD25		
78	CARTD09	CARTD26		
79	GND			
80	GND	BPRTSBN		
81	GND			
82	GND			
83	GND			
84	GND	FWPROMN		
85	GND	NMIN		
86	GND	CKFLN		
87	GND	CKACTN		
88	GND	JAMIN		
89	GND	IDPROMN		
90	GND	RISCN		

The pin numbers for the J1 and J2 connectors appear in the following tables.

Connector J1 signals

Pin	Signal	Pin	Heading
1	SGNDM	12	R1N
2	TXDM	13	T1P
3	RXDM	14	T0P
4	RTSM	16	R0P
5	CTSM	18	R0N
6	DCDM	19	T0N
7	GND	21	SPLITP
9	LABP	22	SPLITN
10	LABN	25	T1N
11	R1P		

Connector J2 signals

Pin	Signal	Pin	Heading
1	SGNDV	8	CLENBN
2	TXDV	20	DTRV
3	RXDV	21	CLRXDN
4	RTSV	22	CLRXDP
5	CTSV	23	CLTXDN
6	DCDV	24	CLTXDP
7	GND		

Technical data

Power requirements

The NT9X26DB requires a single +5 V ±0.25V. The card uses an estimated 13.5W when equipped for captive office use.

NT9X26DC

Product description

The NT9X26DC reduced instruction set computer (BRISC) remote terminal interface (RTIF) paddle board has the features of all current RTIF cards. The NT9X26DC provides CPU firmware (CPUFW) PROM residence for the NT9X10AA and the NT9X13MA CPU cards. This card also provides a reset system to monitor and control the subsystems of the DMS-100 SuperNode and related subsystems.

Functional description

The NT9X26DC starts the CPU reset sequence for maintenance, bootloading, and error recovery. The forces the associated CPU inactive. The NT9X26DC repeatedly displays the associated CPU activity state, synchronization state, clock status and clock activity. The NT9X26DC displays the DMS hexadecimal CPU board information.

The NT9X26DC accepts user input from five sources. The five sources follow:

- local and remote interfaces
- the CPU main board
- the two backplane out-of-band (OOB) links

The NT9X26DC can carry the CPU card PROM for executable firmware. The NT9X26DC supports a remote splitter control mode for captive office use.

Functional blocks

The NT9X26DC contains the following functional blocks:

- sanity timer
- power fail detector
- OOB subsystem
- microcontroller subsystem
- serial communication controller (SCC) subsystem
- identification (ID) PROM and CPU firmware subsystem
- light-emitting diode (LED) display
- captive office control

Sanity timer

The sanity timer resets the microcontroller. The sanity timer resets the microcontroller if the microcontroller does not receive characters from one of the following within 24 s:

- associated CPU card
- local reset terminal interface
- remote reset terminal interface

The microcontroller receives an interrupt 0.75 seconds before reset, and resets the sanity timer.

Power fail detector

The power fail detector circuit holds the card in reset mode when the +5V supply is below safe levels of operation.

Out-of-band subsystem

The OOB subsystem sends OOB messages to the microcontroller. The messages the reset the associated CPU card if the RTIF is in a slave subsystem. A DMS bus or an enhanced network is a slave subsystem.

Microcontroller subsystem

The microcontroller subsystem contains an Intel 8031 microcontroller and associated registers. Port 3 of the microcontroller communicates directly with channel A of the associated CPU board.

The microcontroller can access the CPU card signals to perform the following:

- reset the CPU
- jam the CPU inactive
- disable the CPU sanity timer
- interrupt the CPU at the highest level

The RTIF microcontroller subsystems in the same SuperNode DMS-core processor shelf exchange jam status. The subsystems exchange jam status to make sure that both associated CPUs are not inactive at the same time.

Serial communications controller subsystem

The SCC subsystem provides the serial communications channels A and B. Channel A connects the RTIF microcontroller to the local reset terminal interface.

NT9X26DC (continued)

The microcontroller can switch Channel B to one of the following:

- remote reset terminal at EIA RS232C voltage levels
- remote reset terminal at EIA RS422 voltage levels
- loopback

The remote reset terminal interface that connects to channel B can bypass channel B. The remote reset terminal interface connects to channel B of the associated CPU card for simplex operation. A DMS bus is a simplex operation.

Identification PROM and CPU firmware subsystem

The RTIF provides a standard SuperNode 32B ID PROM which responds on the P-bus as a 32-bit device with even parity.

LED display

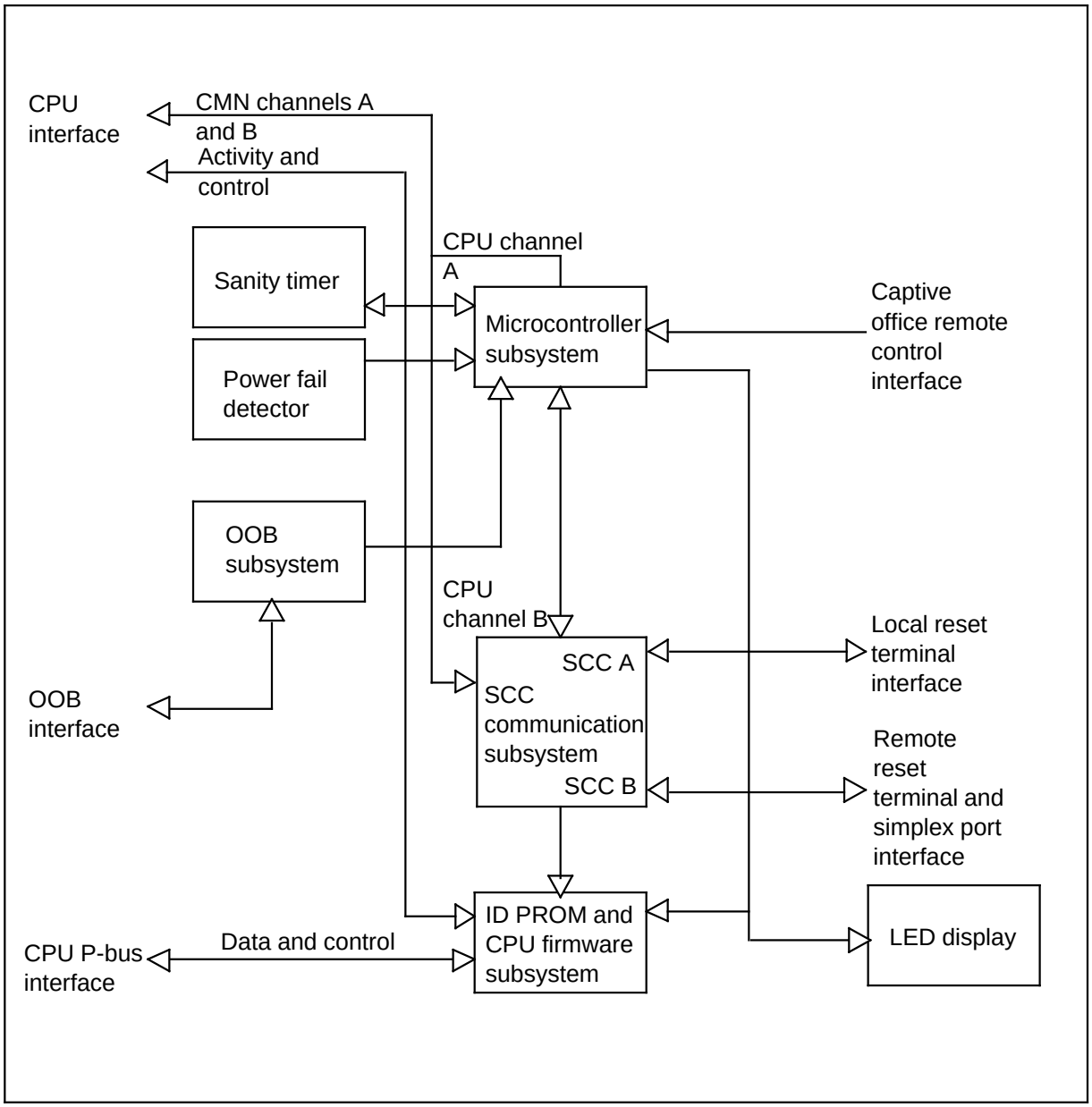
The green LED indicates that the local CPU cards in DMS-core applications have synchronization and the pack is active. The red LED indicates that the local plane CPU card is inactive or out of service.

Captive office control

Captive office control provides an interface for remote control of the splitter. The commands entered from an RTIF terminal can control the splitter mode. Commands entered from an RTIF terminal can send out and receive splitter commands. Commands entered from an RTIF terminal can read splitter commands from the RTIF on the other side. Captive office control also provides the ability to read the mode of the captive office strap.

The relationship between the functional blocks appears in the following figure.

NT9X26DC functional blocks



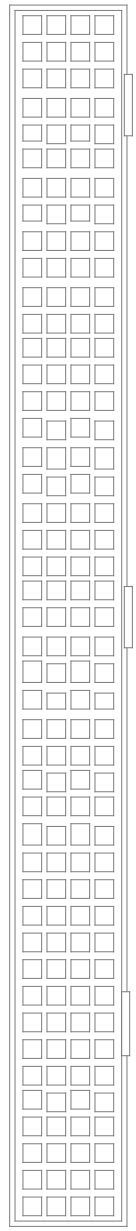
Signaling

Pin numbers

The pin numbers for the NT9X26DC appear in the following figure.

NT9X26DC (continued)

NT9X26DC pin numbers



	A	B	C	D
1	GND			
2	GND			
3	GND			
4	GND			
5	GND			
6				
7				
8				
9				
10				
11				
12				
13	RXDAP			
14	CARTD28			MASTERN
15	CARDT29		IJAMIN	PLN0N
16			GND	OOBIN0
17	DTRAN			
18	TXDAP			
19				
20	DCDAN			
21	RTSAN			OOBIN1
22	BPRXDBP			
23	CARTD30			
24	TXDMISC			
25			BEN0N	BEN1N
26	BPDTRBN	BEN2N	BEN2N	BEN3N
27	BPTXDBP		BASTN	GND
28	CTSMISC		GND	WRTN
29			DTACKN	EDTACKN
30				PARITYP
31				PRTYENN
32			GND	
33			CPUCLK	DAS32N
34	FP61N		BACKN	DATA00
35	C61	TYPE1		DATA01
36		HW0	ADDR02	DATA02
37		HW1	ADDR03	DATA03
38		HW2	ADDR04	DATA04
39		HW3	ADDR05	DATA05
40	GND	CMACTN	ADDR06	DATA06
41	GND		ADDR07	DATA07
42	GND	CMSYNCN	ADDR08	DATA08
43	GND	PBRSTP	ADDR09	DATA09
44	5V	PBRSTN	ADDR10	DATA10
45	5V		ADDR11	DATA11

Legend

MVDTDC = MVDTDCDN
MMDMD = MMDMDCDN

	A	B	C	D
46	5V	DABSANN	ADDR12	DATA12
47	5V	GND	ADDR13	DATA13
48	5V	FACKN	ADDR14	DATA14
49	5V	ENOMN	ADDR15	DATA15
50	5V	MVDTDC	ADDR16	DATA16
51	5V	MMDMD	ADDR17	DATA17
52	5V	VDTDCDN	ADDR18	DATA18
53	5V	MDMDCDN	ADDR19	DATA19
54	5V	OJAMIN	ADDR20	DATA20
55	5V	ROMVPP	ADDR21	DATA21
56	TYPE0	ROMPGMP	ADDR22	DATA22
57			ADDR23	DATA23
58			ADDR24	DATA24
59			ADDR25	DATA25
60			ADDR26	DATA26
61	GND	ROMOEN	ADDR27	DATA27
62	CARTCK	RTSMSIC	ADDR28	DATA28
63	CARTINTN	5V	ADDR29	DATA29
64	CARTD00	5V	ADDR30	DATA30
65	GND	5V	ADDR31	DATA31
66	GND	5V		
67	CARTD01	5V		
68	CARTD02	5V		
69	CARTD03	5V	CARTD27	
70	GND	5V		
71	GND	5V		
72	CARTD04	5V		
73	CARTD05	5V		
74	CARTD06	5V		
75	GND	5V		
76	CARTD07	5V		
77	COENN	5V		
78	CARTD09	CARTD26		
79	GND			
80	GND	BPRTSBN		
81	GND			
82	GND			
83	GND			
84	GND	FWPROMN		
85	GND	NMIN		
86	GND	CKFLN		
87	GND	CKACTN		
88	GND	JAMIN		
89	GND	IDPROMN		
90	GND	RISCN		

The pin numbers for the J1 and J2 connectors appear in the following tables.

Connector J1 signals

Pin	Signal	Pin	Heading
1	SGNDM	15	SPLITOUTP
2	TXDM	16	R0P
3	RXDM	17	SPLITOUTN
4	RTSM	18	R0N
5	CTSM	19	T0N
6	DCDM	21	SPLITP
7	GND	22	SPLITN
9	LABP	23	SPLITINP
10	LABN	24	SPLITINN
11	R1P	25	T1N
12	R1N		
13	T1P		
14	T0P		

Connector J2 signals

Pin	Signal	Pin	Heading
1	SGNDV	8	CLENBN
2	TXDV	20	DTRV
3	RXDV	21	CLRXDN
4	RTSV	22	CLRXDP
5	CTSV	23	CLTXDN
6	DCDV	24	CLTXDP
7	GND		

NT9X26DC (end)

Technical data

Power requirements

The NT9X26DC requires a single +5 V ±0.25V. The card uses an estimated 13.5W when equipped for captive office use.

NT9X26GA

Product description

The NT9X26GA paddle board remote terminal interface (RTIF) paddle board incorporates the features of existing RTIF cards. It provides a CPU firmware (CPUFW) programmable read-only memory (PROM) residence for the NT9X10DA cards. It also provides a reset system that monitors and controls the subsystems of the DMS-100 SuperNode (DMS-core and DMS-bus) and related subsystems.

The NT9X26GA RTIF card, the NT9X10DA processor card, and the optional NT9X14FA memory card are designed to be used together. The NT9X10DA CPU card functions only with the NT9X26GA RTIF paddle board and the optional NT9X14FA extended memory card.

Functional description

The NT9X26GA paddle board initializes the CPU reset sequence for maintenance, boot loading, and error recovery. The NT9X26GA paddle board forces the associated CPU to become inactive, then the board continuously displays the following information:

- activity state
- synchronization state
- clock status
- clock activity
- DMS hexadecimal CPU card information

The NT9X26GA paddle board accepts user input from the following sources:

- local and remote interfaces
- CPU main card
- both backplane out-of-band (OOB) links

The NT9X26GA paddle board can carry the CPUFW PROM so that firmware can be upgraded without changing the processor cards.

The NT9X26GA paddle board provides features for use with captive office. Remote control permits separation of the duplex DMS-core into two simplex

NT9X26GA (continued)

machines. With the installation of a remote splitter adapter, the RTIF terminal can control the internal and external splitting of a DMS switch.

CAUTION
Risk of system failure. Do not use the NT9X26GA paddle board in a link peripheral processor (LPP) shelf or the message switch (MS) shelf.
The NT9X26GA paddle board is not compatible with the LPP in any way, and must not be used in a link peripheral processor (LPP) shelf or message switch (MS) shelf.

Functional blocks

The NT9X26GA paddle board consists of the following functional blocks:

- microcontroller subsystem
- sanity timer
- power fail detector
- OOB subsystem
- serial communication controller (SCC) subsystem
- identification (ID) PROM and CPU firmware subsystem
- light-emitting diode (LED) display
- captive office control

Microcontroller subsystem

The microcontroller subsystem contains the following components:

- an 8031 microcontroller
- 32-kbyte erasable PROM (EPROM)
- 32-kbyte static RAM (SRAM)
- 8-kbyte electrically EPROM (EEPROM)
- associated registers

Port 3 of the microcontroller subsystem communicates directly with Channel A of the associated CPU card.

The microcontroller has access to CPU card signals for the following reasons:

- to reset the CPU
- to force the CPU inactive (jam)

- to disable the CPU sanity timer
- to interrupt the CPU at the highest level

RTIF microcontroller subsystems in the same SuperNode DMS-core processor shelf exchange their "jam" statuses. This exchange prevents both of the associated CPUs from being inactive at the same time.

Sanity timer

The sanity timer resets the microcontroller after 24 s if it has received no characters from the following:

- the associated CPU card
- the local reset terminal interface
- the remote reset terminal interface

The microcontroller receives an interrupt signal 0.75 s prior to reset. Then the microcontroller resets the sanity timer.

Power failure detector

The power failure detector circuit holds the card in reset mode when the +5 V supply is below safe operating levels.

Out-of-band subsystem

The OOB subsystem sends OOB messages to the microcontroller. The messages initiate the reset of the associated CPU card if the RTIF resides in a slave subsystem like a DMS-bus or an enhanced network. The OOB subsystem also asserts the backplane MASTERN signal on the local OOB transmission paddle boards.

Serial communications controller subsystem

The SCC subsystem provides two serial communications channels, A and B. Channel A connects the RTIF microcontroller to the local reset terminal interface.

The microcontroller can switch Channel B to the following:

- the loopback
- the remote reset terminal at EIA RS232C voltage levels
- the remote reset terminal at EIA RS422 voltage levels

When connected to Channel B of the associated CPU card for simplex operation, the remote reset terminal interface can bypass Channel B.

NT9X26GA (continued)

Identification PROM and CPU firmware subsystem

The RTIF provides a standard SuperNode 32-bit IDPROM that responds on the peripheral bus (PBUS) as a 32-bit device with no parity. It also carries 2048 kbytes of 32-bit EEPROM for CPUFW that responds as the following:

- a 32-bit device with parity in NT9X10DA mode
- a 32-bit device with no parity in NT9X13 mode

Light-emitting diode (LED) display

The green LED indicates the synchronization of the local CPU cards in DMS-core applications. The red LED indicates the local plane CPU card is inactive or out of service.

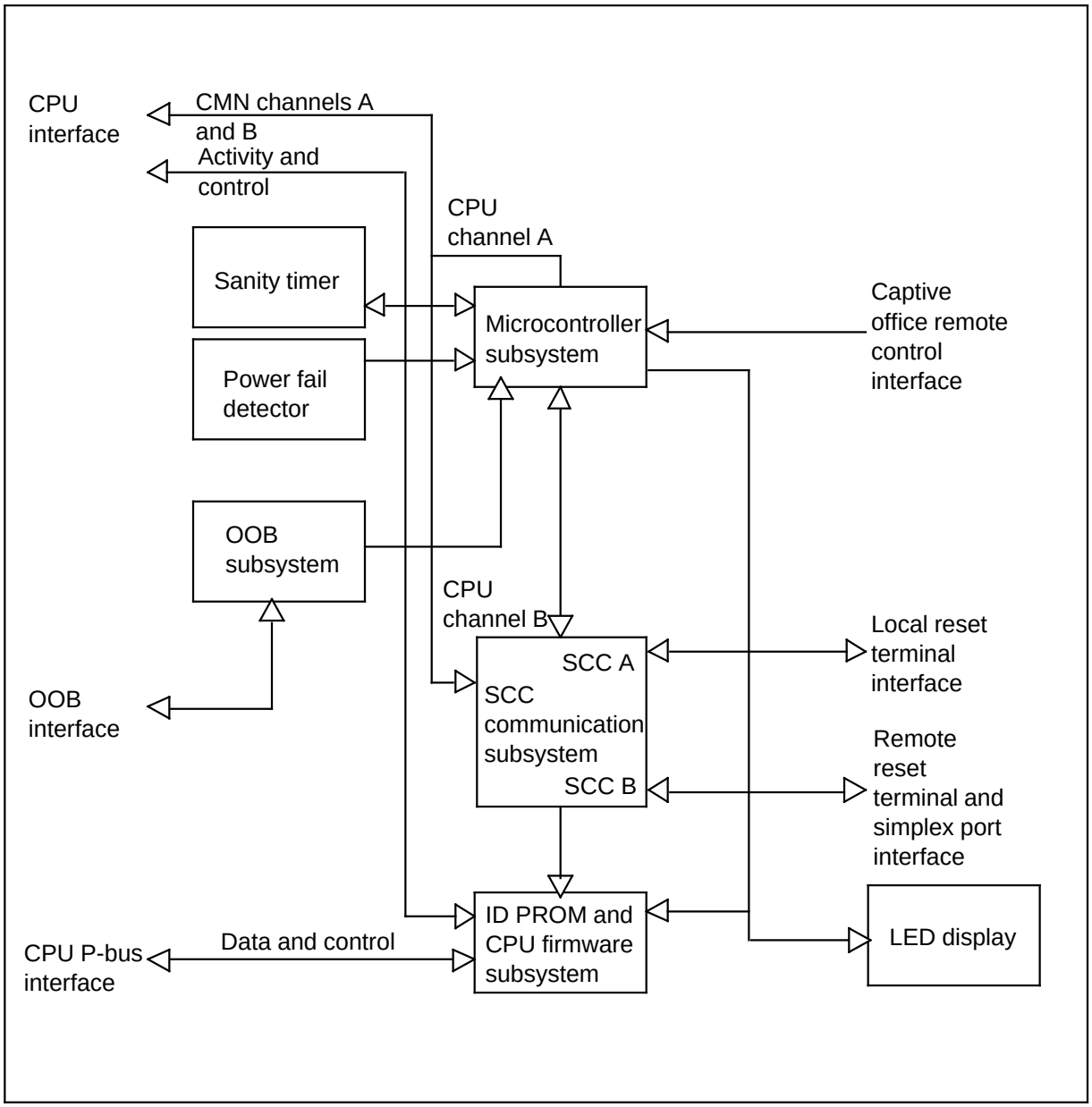
The NT9X26GA paddle board also has a green activity LED that indicates the pack is active. This LED alerts maintenance personnel to the status of the RTIF pack.

Captive office control

The RTIF terminal provides remote control of the splitter mode. From the RTIF terminal, operating company personnel can send and receive splitter commands, and read them from the opposite RTIF. Operating company personnel can also read the mode of the captive office strap.

The following figure shows the relationships between the functional blocks.

NT9X26GA paddle board functional blocks



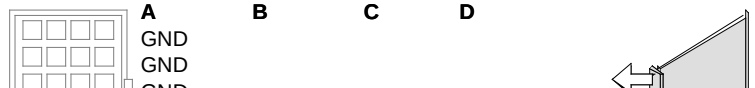
Signaling

Pin outs

The following figure shows the pin outs for the NT9X26GA paddle board.

NT9X26GA (continued)

NT9X26GA paddle board pin outs



	A	B	C	D
1	GND			
2	GND			
3	GND			
4	GND			
5	GND			
6				
7				
8				
9				
10				
11				
12				
13	RXDAP			
14	CARTD28			MASTERN
15	CARDT29		IJAMIN	PLN0N
16			GND	OOBIN0
17	DTRAN			
18	TXDAP			
19	RXDMISC			
20	DCDAN			
21	RTSAN			OOBIN1
22	BPRXDBP			
23				
24	TXDMISC			
25			BEN0N	BEN1N
26	BPDTRBN	BEN2N	BEN2N	BEN3N
27	BPTXDBP		BASTN	GND
28	CTSMISC		GND	WRTN
29			DTACKN	EDTACKN
30				PARITYP
31				PRTYENN
32			GND	
33			CPUCLK	DAS32N
34	FP61N		BACKN	DATA00
35	C61	TYPE1		DATA01
36		HW0	ADDR02	DATA02
37		HW1	ADDR03	DATA03
38		HW2	ADDR04	DATA04
39		HW3	ADDR05	DATA05
40	GND	CMACTN	ADDR06	DATA06
41	GND		ADDR07	DATA07
42	GND	CMSYNCN	ADDR08	DATA08
43	GND	PBRSTP	ADDR09	DATA09
44	5V	PBRSTN	ADDR10	DATA10
45	5V		ADDR11	DATA11

Legend

MVDTDC = MVDTDCDN
MMDMD = MMDMDCDN

	A	B	C	D
46	5V	DABSANN	ADDR12	DATA12
47	5V	GND	ADDR13	DATA13
48	5V	FACKN	ADDR14	DATA14
49	5V	ENOMN	ADDR15	DATA15
50	5V	MVDTDC	ADDR16	DATA16
51	5V	MMDMD	ADDR17	DATA17
52	5V	VDTDCDN	ADDR18	DATA18
53	5V	MDMDCDN	ADDR19	DATA19
54	5V	OJAMIN	ADDR20	DATA20
55	5V	ROMVPP	ADDR21	DATA21
56	TYPE0	ROMPGMP	ADDR22	DATA22
57			ADDR23	DATA23
58			ADDR24	DATA24
59			ADDR25	DATA25
60			ADDR26	DATA26
61	GND	ROMOEN	ADDR27	DATA27
62	JTAGTCK	RTSMSIC	ADDR28	DATA28
63	JTAGTRST	+5V	ADDR29	DATA29
64	JTAGTMS	+5V	ADDR30	DATA30
65	GND	+5V	ADDR31	DATA31
66	GND	+5V		
67	JTAGTDI	+5V		
68	JTAGTDO	+5V		
69		+5V	RTIFROMN	
70	GND	+5V		
71	GND	+5V		
72		+5V		
73		+5V		
74		+5V		
75	GND	+5V		
76		+5V		
77	COENN	+5V		
78				
79	GND			
80	GND	BPRTSBN		
81	GND			
82	GND			
83	GND			
84	GND	FWPROMN		
85	GND	NMIN		
86	GND	CKFLN		
87	GND	CKACTN		
88	GND	JAMIN		
89	GND	IDPROMN		
90	GND	RISCN		

The following tables show the pin outs for the J1 (local interface connector) and the J2 (remote connection signal description) connectors.

Connector J1 signals

Pin	Signal	Pin	Heading
1	SGNDM	15	SPLITOUTP
2	TXDM	16	R0P
3	RXDM	17	SPLITOUTN
4	RTSM	18	R0N
5	CTSM	19	T0N
6	DCDM	21	SPLITP
7	GND	22	SPLITN
9	LABP	23	SPLITINP
10	LABN	24	SPLITINN
11	R1P	25	T1N
12	R1N		
13	T1P		
14	T0P		

Connector J2 signals

Pin	Signal	Pin	Heading
1	SGNDV	8	CLENBN
2	TXDV	20	DTRV
3	RXDV	21	CLRXDN
4	RTSV	22	CLRXDP
5	CTSV	23	CLTXDN
6	DCDV	24	CLTXDP
7	GND		

NT9X26GA (end)

Technical data

Power requirements

The NT9X26GA paddle board requires a single +5 V ±0.25 V power supply. The card consumes an estimated 13.5 W when it is equipped for captive office use.

Power rerouting for the BRISC Series 70 processor

This packaged core power module (PCPM) has 15 pins allocated to reroute +5 V from the internal +5 V to the BRISC Series 70 PCPM.

CAUTION

Risk of system failure. Do not reroute power in an link peripheral processor (LPP) shelf.

This power rerouting change is not compatible with the link peripheral processor (LPP) shelf, and will cause a system failure if used for this application.

NT9X27AA

Product description

The NT9X27AA extends the peripheral bus (P-bus) from the NT9X06AA to the NT9X07AA. The NT9X06AA is the computing module (CM) processor shelf. The NT9X06AA contains the CPU and memory. The NT9X07AA is the CM extension shelf. The NT9X07AA contains the system load unit (SLU). An NT9X27BA card is the CM extension shelf bus extender. The card is installed in the extension shelf and receives the signals from the NT9X27AA. This card buffers the signals on the extension shelf backplane. Two NT9X27AAs are required on a CM processor shelf for each installed extension shelf.

Location

Two NT9X27AAs are installed at the rear of the shelf slots 8 and 31 in the sequence given. If a second extension shelf is required, a second pair of NT9X27AAs is installed in slots 9 and 30.

Functional description

The NT9X27AA performs the following functions:

- buffers P-bus address, data, and control signals
- decodes extension shelf addresses
- provides extension shelf cable presence and positioning identification
- provides element identification (ID) PROM logic information

Signaling

The parts of the P-bus signals that are buffered to and from the NT9X07AA through cabling appear in the following list:

- Address (to extension)
  - — ADDR (01:16,18)
- Data (to and from extension)
  - — DATA (00:31)
- Control (to extension)
  - — RSTOUT-
  - — WRT-
  - — CMACT-
  - — CMSYNC-
  - — BEN (0:3)-

NT9X27AA (continued)

- Control (from extension)
  - — DTACK-
  - — EDTACK-
  - — PRTYEN-
  - — PARITY
- Interrupt
  - — IRQ4
  - — PERINT (0:7)
- Extension shelf access (to extension)
  - — EXDAS32-

Pin numbers

The pin numbers for NT9X27AA appear in the following tables.

J1 signal assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	GND	20	DATA01
2	DATA00	21	DATA03
3	DATA02	22	DATA05
4	DATA04	23	DATA07
5	DATA06	24	DATA08
6	GND	25	DATA10
7	DATA09	26	DATA12
8	DATA11	27	DATA14
9	DATA13	28	GND
10	DATA15	29	DATA17
11	DATA16	30	DATA19
12	DATA18	31	DATA21
13	DATA20	32	DATA23
14	DATA22	33	DATA24

J1 signal assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal
15	GND	34	DATA26
16	DATA25	35	DATA28
17	DATA27	36	DATA30
18	DATA29	37	CAPRES1
19	DATA31		

J2 signal assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	GND	20	-EXDAS32-
2	+EXDAS32-	21	-WRT-
3	+WRT-	22	-RSTOUT-
4	+RSTOUT-	23	GND
5	GND	24	-BEN0-
6	+BEN0-	25	-BEN1-
7	+BEN1-	26	-BEN2-
8	+BEN2-	27	-BEN3-
9	+BEN3-	28	-DTACK-
10	+DTACK-	29	-EDTACK-
11	+EDTACK-	30	-PRTYEN-
12	+PRTYEN-	31	-PARITY
13	+PARITY	32	-CMSYNC-
14	+CMSYNC-	33	-CMACT-
15	+CMACT-	34	NC
16	NC	35	NC
17	NC	36	NC

NT9X27AA (end)

J2 signal assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal
18	NC	37	CAPRES2
19	GND		

J3 signal assignments

Pin	Signal	Pin	Signal
1	GND	20	ADDR01
2	ADDR02	21	ADDR03
3	ADDR04	22	ADDR05
4	ADDR06	23	ADDR07
5	ADDR08	24	GND
6	ADDR09	25	ADDR10
7	ADDR11	26	ADDR12
8	ADDR13	27	ADDR14
9	ADDR15	28	ADDR16
10	ADDR18	29	GND
11	IRQ4-	30	GND
12	PERINT0-	31	GND
13	PERINT1-	32	GND
14	PERINT2-	33	GND
15	PERINT3-	34	GND
16	PERINT4-	35	GND
17	PERINT5-	36	GND
18	PERINT6-	37	CAPRES3
19	PERINT7-		

NT9X27BA

Product description

The NT9X27BA extends the peripheral bus (P-bus) to the NT9X27AA. The NT9X27BA receives the P-bus from the NT9X06AA, which is the computing module (CM) processor shelf. The NT9X06AA houses the central processing unit (CPU) and memory. The NT9X07AA is the CM extension shelf. This shelf houses the system load unit. An NT9X27AA installed in the CM processor shelf buffers the P-bus through cable to the NT9X27BA. The NT9X27AA is the CM processor shelf bus extender. The system requires two NT9X27BAs on a CM extension shelf.

Location

Two NT9X27BAs are at the rear of the shelf in slots 7 and 32.

Functional description

The NT9X27BA performs the following functions:

- buffer of P-bus address, data, and control signals
- regeneration of P-bus high address ADDR (17,19:31)
- identification of cable and position
- generation of +5V interlock signal
- identification (ID) PROM access to the ID PROM and interface for access of power converter ID PROMs

Signaling

The NT9X27BA following is a list of the P-bus signals that the NT927AA buffers to and from the NT9X06AA processor shelf through cabling:

- Address, from NT9X06AA
  - — ADDR (01:16,18)
- Data, to and from NT9X06AA
  - — DATA (00:31)
- Control, from NT9X06AA
  - — RSTOUT-
  - — WRT-
  - — CMACT-
  - — CMSYNC-
  - — BEN (0:3)-

NT9X27BA (continued)

- Control, to NT9X06AA
  - — DTACK-
  - — EDTACK-
  - — PRTYEN-
  - — PARITY-
- Interrupt, to NT9X06AA
  - — IRQ4-
  - — PERINT (0:7)-
- Extension shelf access, from NT9X06AA
  - — EXDAS32-

Pin numbers

The pin numbers for NT9X27BA appear in the following tables.

J1 signal assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	GND	20	DATA01
2	DATA00	21	DATA03
3	DATA02	22	DATA05
4	DATA04	23	DATA07
5	DATA06	24	DATA08
6	GND	25	DATA10
7	DATA09	26	DATA12
8	DATA11	27	DATA14
9	DATA13	28	GND
10	DATA15	29	DATA17
11	DATA16	30	DATA19
12	DATA18	31	DATA21
13	DATA20	32	DATA23
14	DATA22	33	DATA24

J1 signal assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal
15	GND	34	DATA26
16	DATA25	35	DATA28
17	DATA27	36	DATA30
18	DATA29	37	CAPRES1
19	DATA31		

J2 signal assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	GND	20	-EXDAS32-
2	+EXDAS32-	21	-WRT-
3	+WRT-	22	-RSTOUT-
4	+RSTOUT-	23	GND
5	GND	24	-BEN0-
6	+BEN0-	25	-BEN1-
7	+BEN1-	26	-BEN2-
8	+BEN2-	27	-BEN3-
9	+BEN3-	28	-DTACK-
10	+DTACK-	29	EDTACK-
11	+EDTACK-	30	-PRTYEN-
12	+PRTYEN-	31	-PARITY
13	+PARITY	32	-CMSYNC-
14	+CMSYNC-	33	-CMACT-
15	+CMACT-	34	NC
16	NC	35	NC
17	NC	36	NC

NT9X27BA (end)

J2 signal assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal
18	NC	37	CAPRES2
19	GND		

J3 signal assignments

Pin	Signal	Pin	Signal
1	GND	20	ADDR01
2	ADDR02	21	ADDR03
3	ADDR04	22	ADDR05
4	ADDR06	23	ADDR07
5	0ADDR08	24	GND
6	ADDR09	25	ADDR10
7	ADDR11	26	ADDR12
8	ADDR13	27	ADDR14
9	ADDR15	28	ADDR16
10	ADDR18	29	GND
11	IRQ4-	30	GND
12	PERINT0-	31	GND
13	PERINT1-	32	GND
14	PERINT2-	33	GND
15	PERINT3-	34	GND
16	PERINT4-	35	GND
17	PERINT5-	36	GND
18	PERINT6-	37	CAPRES3
19	PERINT7-		

Product description

The NT9X30AA is a dc-to-dc power converter.

Functional description

A 48-V office battery is the power source for the converter. A standard input filter circuit filters the power source.

The input feeds to an auxiliary power supply module, QMS141A, to provide isolation between the input battery and the housekeeping circuits. The output also feeds to the output stage where the switching transformer make sure isolation occurs. The regulator provides +5 V at 86 A and has a current limiter circuit to protect against overload.

The pulse width modulation (PWM) module, QMS143A, drives the output stage. Feedback signals from the output, current condition, and possible fault condition also feed to this module. The process makes sure regulation occurs and prevents damage that internal or external faults can cause.

The QMS142A is a monitor module that supervises the output for over- and under-voltage condition. If the output voltage goes below +4.3 V (±0.3 V) or above +6.5 V (±0.5 V), the following occurs:

- the monitor generates signals for shutdown
- alarm signals appear at the back panel
- the red fault indicator light-emitting diode (LED) turns on
- the converter shuts down

Functional blocks

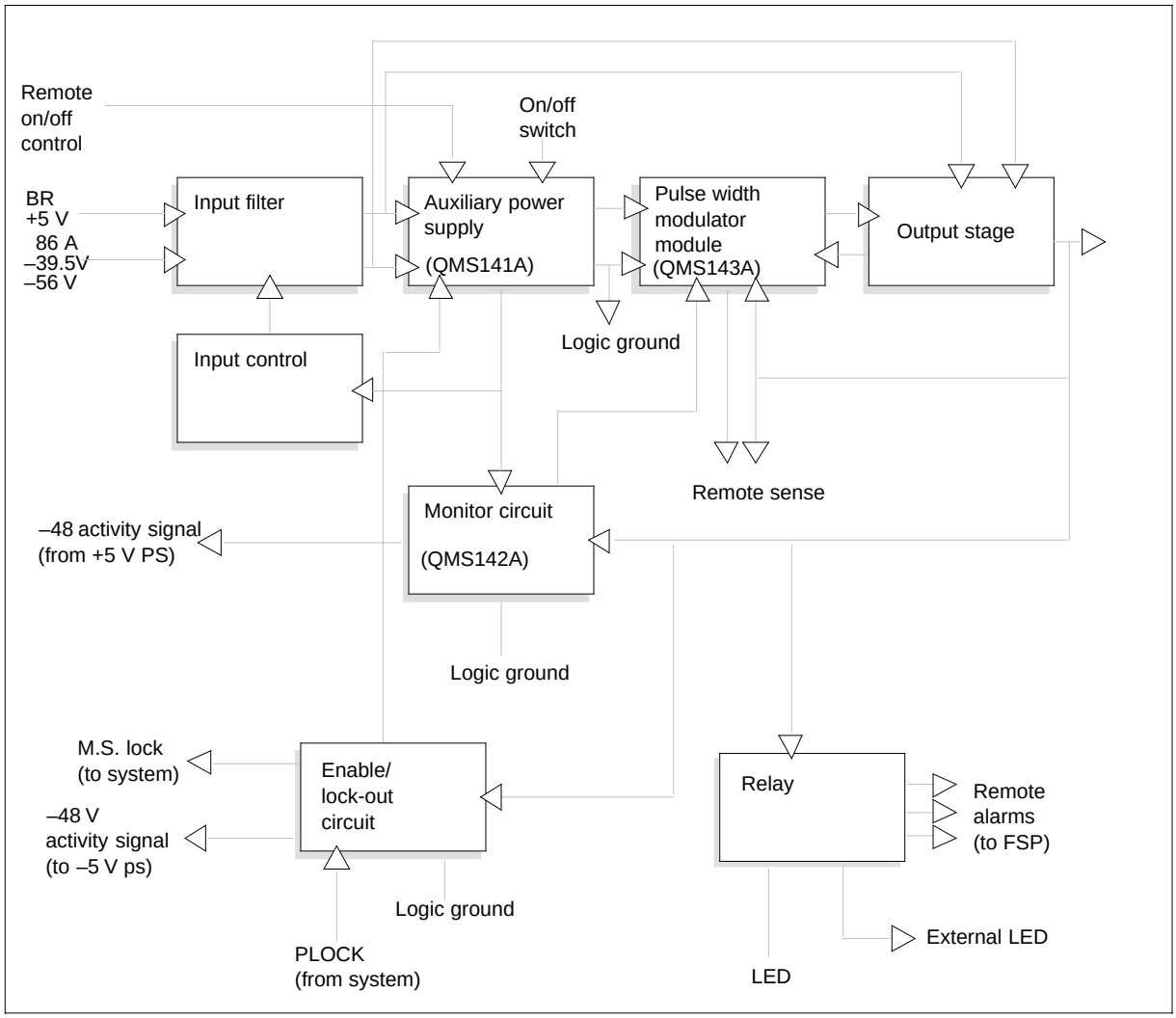
The NT9X30AA has the following operating blocks:

- input filter
- auxiliary power supply
- the PWM module
- output stage, which include transformer, rectifier, and filter
- input control
- monitor circuit

The relationship between the functional blocks appears in the following figure.

NT9X30AA (continued)

NT9X30AA functional blocks



Technical data

Power requirements

Input

The input voltage is -48 V. The allowed voltage range is from -39.5 V to -56 V. The maximum input current is 17 A.

Output

Output specifications	
Voltage	+5.15 V ±2%
High voltage shutdown	+6.5 V ±0.5 V
Low voltage shutdown	+4.3 V ±0.3 V
Ripple	50 mV rms
Maximum current	86 A
Minimum current	2 A
Current limit	98 A ±7 A

NT9X30AB - Manufacture discontinued, replaced by NT9X30AC

Product description

The NT9X30AB is Manufacture Discontinued. It was a dc-to-dc power converter. The NT9X30AB was the 60-V version of the NT9X30AA for SuperNode frames.

Functional description

A 60-V office battery is the power source for the converter. A standard input filter circuit filters the power source. The power source input can be from -39.5 V to -75 V.

The input feeds to an auxiliary power supply module, QMS141A, to isolate the input battery from the housekeeping circuits. At the output stage, the switching transformer makes sure isolation occurs. The regulator provides +5 V at 86 A and has a current limiter circuit to protect against overload.

The pulse width modulation (PWM) module, QMS143A, drives the output stage. Feedback signals from the output, current condition, and possible fault condition also feed to this module. This condition makes sure regulation occurs and prevents damage that internal or external faults can cause.

A monitor module, QMS142A, supervises the output for over- and under-voltage condition. If the output voltage goes below +4.3 V ±0.3 V or above +6.5 V ±0.5 V, the following occur:

- the monitor generates signals for shutdown
- alarm signals appear at the back panel
- the red fault indicator light-emitting diode (LED) turns on
- the converter shuts down

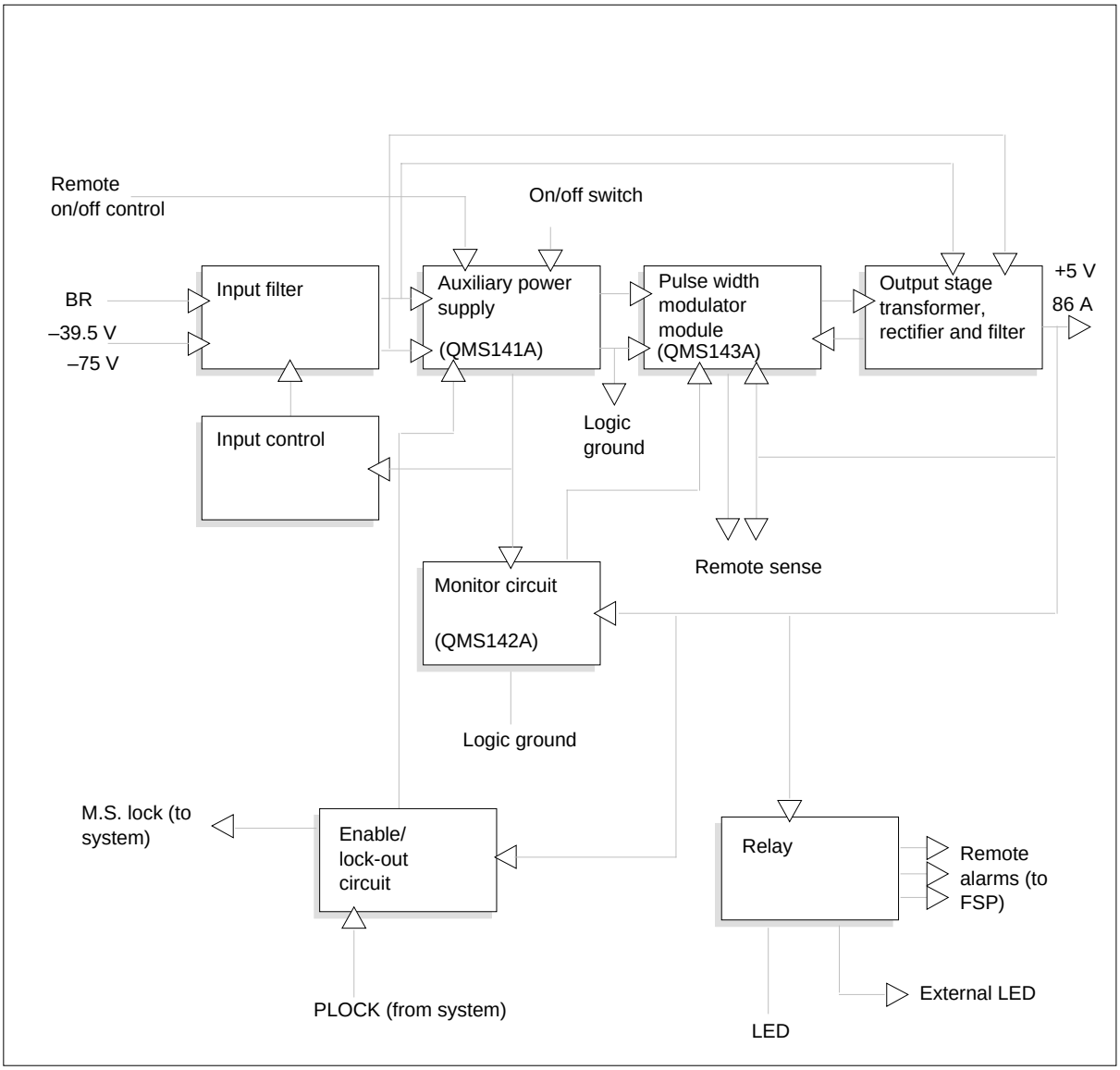
Functional blocks

The NT9X30AB has the following functional blocks:

- input section
- input control
- auxiliary power supply
- the PWM module
- monitor circuit
- output stage (transformer, rectifier, and filter)

The relationship between the functional blocks appears in the following figure.

NT9X30AB functional blocks



Input section

The input section contains the following:

- a metal-oxide clamp across the input that limits the maximum surge voltage
- an inrush thermistor that limits the charging current
- a high-frequency filter that reduces the amount of noise and electromagnetic interference (EMI) that feeds back to the source

NT9X30AB (continued)

Auxiliary power supply

The QMS141 auxiliary supply module provides the power for the QMS143A control and QMS142A monitor circuits.

Input control section

To power up or shut down the converter requires use of the enable switch on the faceplate of the converter. Remote start-up and shut-down signals are also supported. Activation of the enable switch turns on the auxiliary supply module. This module supplies power to the QMS142A monitor circuit and the QMS143A pulse-width modulator (PWM) controller module. Relays are activated when the auxiliary supply voltage is present.

Pulse width modulator module

A current-sense transformer senses the transistor current. This information feeds back to the PWM controller to limit the current in the transistors. The QMS143A PWM controller module connects to the output return and directly senses the output voltage to control the transistor switching. The transistors chop the input dc voltage and apply the ac waveform alternately across the primary input of the power transformer.

Monitor circuit

The regulated output voltage can rise above a fixed level, or fall below a specified level. The QMS142A monitor circuit sends a signal to the PWM to shut down the converter. The converter does not automatically restart. You must restart the converter manually.

Output stage

The transformer provides a lower amplitude ac squarewave, which the system rectifies and filters to produce the correct dc output voltage. A shunt resistor preloads this output and the system provides decoupling at the output.

Signaling

Pin numbers

The pin numbers for the NT9X30AB appear in the following tables.

Connector P1 CBR05 64 pin (Sheet 1 of 2)

Pin	Z	B	D	F
2	D2+5	D1+5	D0+5	DR
4	D5+5	D4+5	D3+5	NC
6	A3+5	CS+5	D6+5	NC

Connector P1 CBR05 64 pin (Sheet 2 of 2)

Pin	Z	B	D	F
8	A0+5	A1+5	A2+5	+15V
10	D7+5	R.A.S./NC	R.A.S./C	SD
12	R.A.S./NO	-ABS	EXT.LED	+5VTEST
14	+SENSE	-BACT.SIG	LRSENSE	-BATT
16	BR.ABS	NO.CON.OUT	+5V	+5V
18	LR	LR	LR	LR
20	+5V	+5V	+5V	+5V
22	LR	LR	LR	LR
24	+5V	+5V	+5V	+5V
26	LR	LR	LR	LR
28	+5V	+5V	+5V	+5V
30	LR	LR	LR	LR
32	+5V	+5V	+5V	+5V

Connector P1 CBR05 64 pin (Sheet 1 of 2)

Pin	Z	B	D	F
2	LR	LR	LR	LR
4	+5V	+5V	+5V	+5V
6	LR	LR	LR	LR
8	+5V	+5V	+5V	+5V
10	LR	LR	LR	LR
12	+5V	+5V	+5V	+5V
14	LR	LR	LR	LR
16	+5V	+5V	+5V	+5V
18	PLOCK	LR	LR	LR

NT9X30AB (end)

Connector P1 CBR05 64 pin (Sheet 2 of 2)

Pin	Z	B	D	F
20	ACT.INTL.NO	ACT.INTL.NC	ACT.INTL.C	NC
22	S.B.I./NO	S.B.I./NC	S.B.I./C	REM.SHDN.
24	EXT.SW.ON	EXT.SW.OFF	EXT.SWT.	REM.START
26	-BAT	-BAT	-BAT	-BAT
28	-BAT	-BAT	-BAT	-BAT
30	BR	BR	BR	BR
32	BR	BR	BR	BR

Technical data

Power requirements

Input

The nominal input voltage is -60 V. The allowed voltage range is from -52 V to -72 V. The maximum input current is 17 A.

Output

Output specifications	
Voltage	+5.15 V ±2%
High voltage shutdown	+6.5 V ±0.5 V
Low voltage shutdown	+4.3 V ±0.3 V
Ripple	50 mV rms
Maximum current	86 A
Minimum current	2 A
Current limit	98 A ±7 A

NT9X30AC - replaces Manufacture Discontinued card NT9X30AB

Product description

The NT9X30AC is a dc-to-dc power converter. The NT9X30AC is the 60-V version of the NT9X30AA for SuperNode frames.

Functional description

A 60-V office battery is the power source for the converter. A standard input filter circuit filters the power source. The power source input can be from -39.5 V to -75 V.

The input feeds to an auxiliary power supply module, QMS141A, to isolate the input battery from the housekeeping circuits. At the output stage, the switching transformer makes sure isolation occurs. The regulator provides +5 V at 86 A and has a current limiter circuit to protect against overload.

The pulse width modulation (PWM) module, QMS143A, drives the output stage. Feedback signals from the output, current condition, and possible fault condition also feed to this module. This condition makes sure regulation occurs and prevents damage that internal or external faults can cause.

A monitor module, QMS142A, supervises the output for over- and under-voltage condition. If the output voltage goes below +4.3 V ±0.3 V or above +6.5 V ±0.5 V, the following occur:

- the monitor generates signals for shutdown
- alarm signals appear at the back panel
- the red fault indicator light-emitting diode (LED) turns on
- the converter shuts down

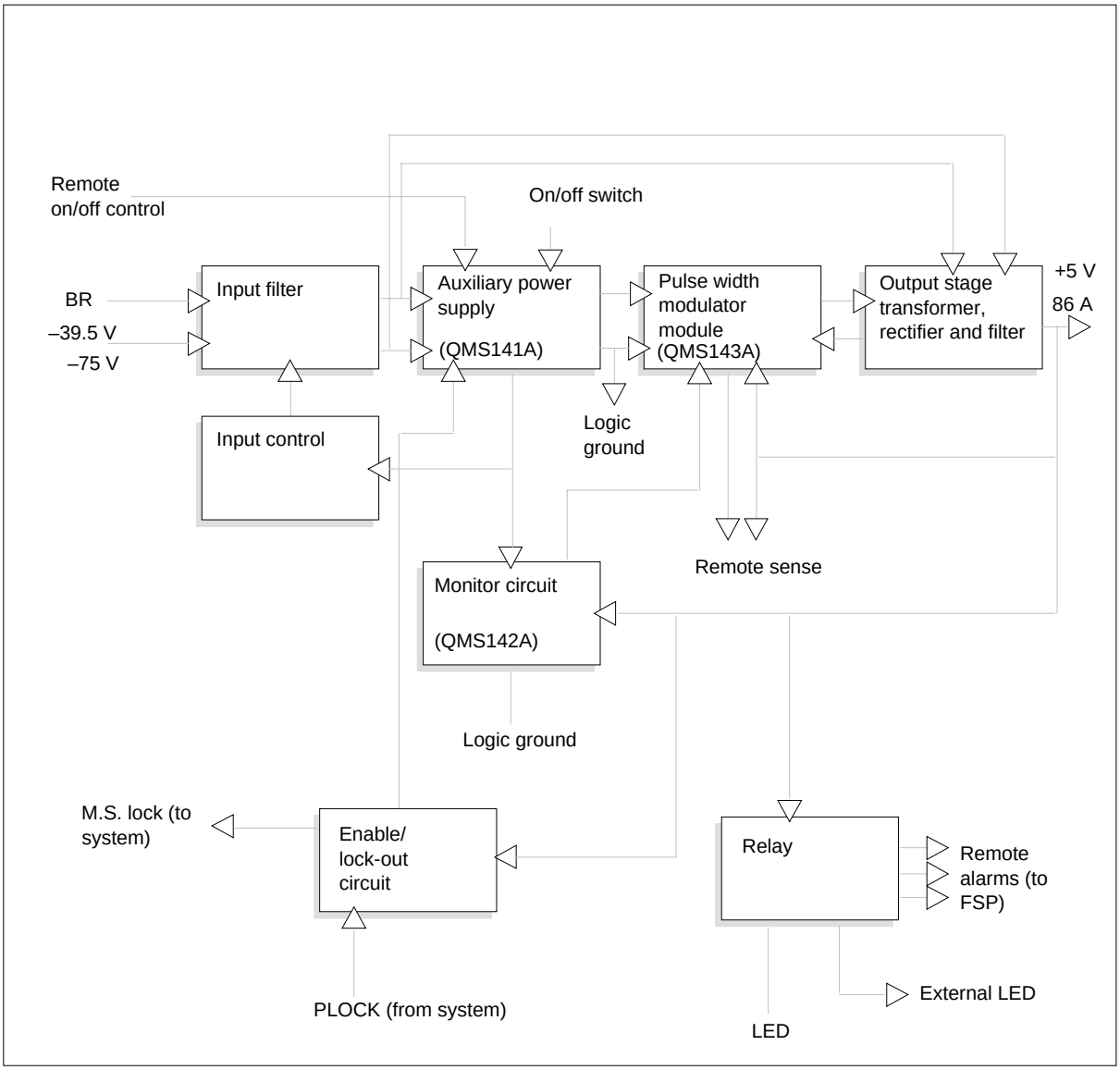
Functional blocks

The NT9X30AC has the following functional blocks:

- input section
- input control
- auxiliary power supply
- the PWM module
- monitor circuit
- output stage (transformer, rectifier, and filter)

The relationship between the functional blocks appears in the following figure.

NT9X30AC functional blocks



Input section

The input section contains the following:

- a metal-oxide clamp across the input that limits the maximum surge voltage
- an inrush thermistor that limits the charging current
- a high-frequency filter that reduces the amount of noise and electromagnetic interference (EMI) that feeds back to the source

NT9X30AC (continued)

Auxiliary power supply

The QMS141 auxiliary supply module provides the power for the QMS143A control and QMS142A monitor circuits.

Input control section

To power up or shut down the converter requires use of the enable switch on the faceplate of the converter. Remote start-up and shut-down signals are also supported. Activation of the enable switch turns on the auxiliary supply module. This module supplies power to the QMS142A monitor circuit and the QMS143A pulse-width modulator (PWM) controller module. Relays are activated when the auxiliary supply voltage is present.

Pulse width modulator module

A current-sense transformer senses the transistor current. This information feeds back to the PWM controller to limit the current in the transistors. The QMS143A PWM controller module connects to the output return and directly senses the output voltage to control the transistor switching. The transistors chop the input dc voltage and apply the ac waveform alternately across the primary input of the power transformer.

Monitor circuit

The regulated output voltage can rise above a fixed level, or fall below a specified level. The QMS142A monitor circuit sends a signal to the PWM to shut down the converter. The converter does not automatically restart. You must restart the converter manually.

Output stage

The transformer provides a lower amplitude ac squarewave, which the system rectifies and filters to produce the correct dc output voltage. A shunt resistor preloads this output and the system provides decoupling at the output.

Signaling

Pin numbers

The pin numbers for the NT9X30AC appear in the following tables.

Connector P1 CBR05 64 pin (Sheet 1 of 2)

Pin	Z	B	D	F
2	D2+5	D1+5	D0+5	DR
4	D5+5	D4+5	D3+5	NC
6	A3+5	CS+5	D6+5	NC

Connector P1 CBR05 64 pin (Sheet 2 of 2)

Pin	Z	B	D	F
8	A0+5	A1+5	A2+5	+15V
10	D7+5	R.A.S./NC	R.A.S./C	SD
12	R.A.S./NO	-ABS	EXT.LED	+5VTEST
14	+SENSE	-BACT.SIG	LRSENSE	-BATT
16	BR.ABS	NO.CON.OUT	+5V	+5V
18	LR	LR	LR	LR
20	+5V	+5V	+5V	+5V
22	LR	LR	LR	LR
24	+5V	+5V	+5V	+5V
26	LR	LR	LR	LR
28	+5V	+5V	+5V	+5V
30	LR	LR	LR	LR
32	+5V	+5V	+5V	+5V

Connector P1 CBR05 64 pin (Sheet 1 of 2)

Pin	Z	B	D	F
2	LR	LR	LR	LR
4	+5V	+5V	+5V	+5V
6	LR	LR	LR	LR
8	+5V	+5V	+5V	+5V
10	LR	LR	LR	LR
12	+5V	+5V	+5V	+5V
14	LR	LR	LR	LR
16	+5V	+5V	+5V	+5V
18	PLOCK	LR	LR	LR

NT9X30AC (end)

Connector P1 CBR05 64 pin (Sheet 2 of 2)

Pin	Z	B	D	F
20	ACT.INTL.NO	ACT.INTL.NC	ACT.INTL.C	NC
22	S.B.I./NO	S.B.I./NC	S.B.I./C	REM.SHDN.
24	EXT.SW.ON	EXT.SW.OFF	EXT.SWT.	REM.START
26	-BAT	-BAT	-BAT	-BAT
28	-BAT	-BAT	-BAT	-BAT
30	BR	BR	BR	BR
32	BR	BR	BR	BR

Technical data

Power requirements

Input

The nominal input voltage is -60 V. The allowed voltage range is from -52 V to -72 V. The maximum input current is 17 A.

Output

Output specifications	
Voltage	+5.15 V ±2%
High voltage shutdown	+6.5 V ±0.5 V
Low voltage shutdown	+4.3 V ±0.3 V
Ripple	50 mV rms
Maximum current	86 A
Minimum current	2 A
Current limit	98 A ±7 A

NT9X31AA

Product description

The NT9X31AA is a dc-to-dc power converter for the DMS SuperNode.

Functional description

A -48V office battery is the power source for the converter board. A standard input filter circuit filters the power source.

The QMS141A is an auxiliary power supply module. The input feeds to QMS141A for isolation between the input battery and the housekeeping circuits. The output feeds to the output stage. The switching transformer assures isolation at the output stage. The regulator provides -5 V at 20 A. A current limiter circuit protects the regulator against overload.

The pulse width modulation (PWM) module QMS143A drives the output stage. Feedback signals from the output current condition and possible fault conditions feed to this module to assure regulation. Feedback signals and fault conditions feed to the module to prevent damage that internal or external faults can cause.

A monitor circuit supervises the output for over- and under-voltage conditions. If the output goes below -4.3 V (+0.3 V) or above -6.5 V (+0.5 V), the following occurs:

- The monitor circuit generates signals for shutdown.
- Alarm signals appear at the back panel.
- The red fault indicator light-emitting diode (LED) lights.
- The converter shuts down.

Functional blocks

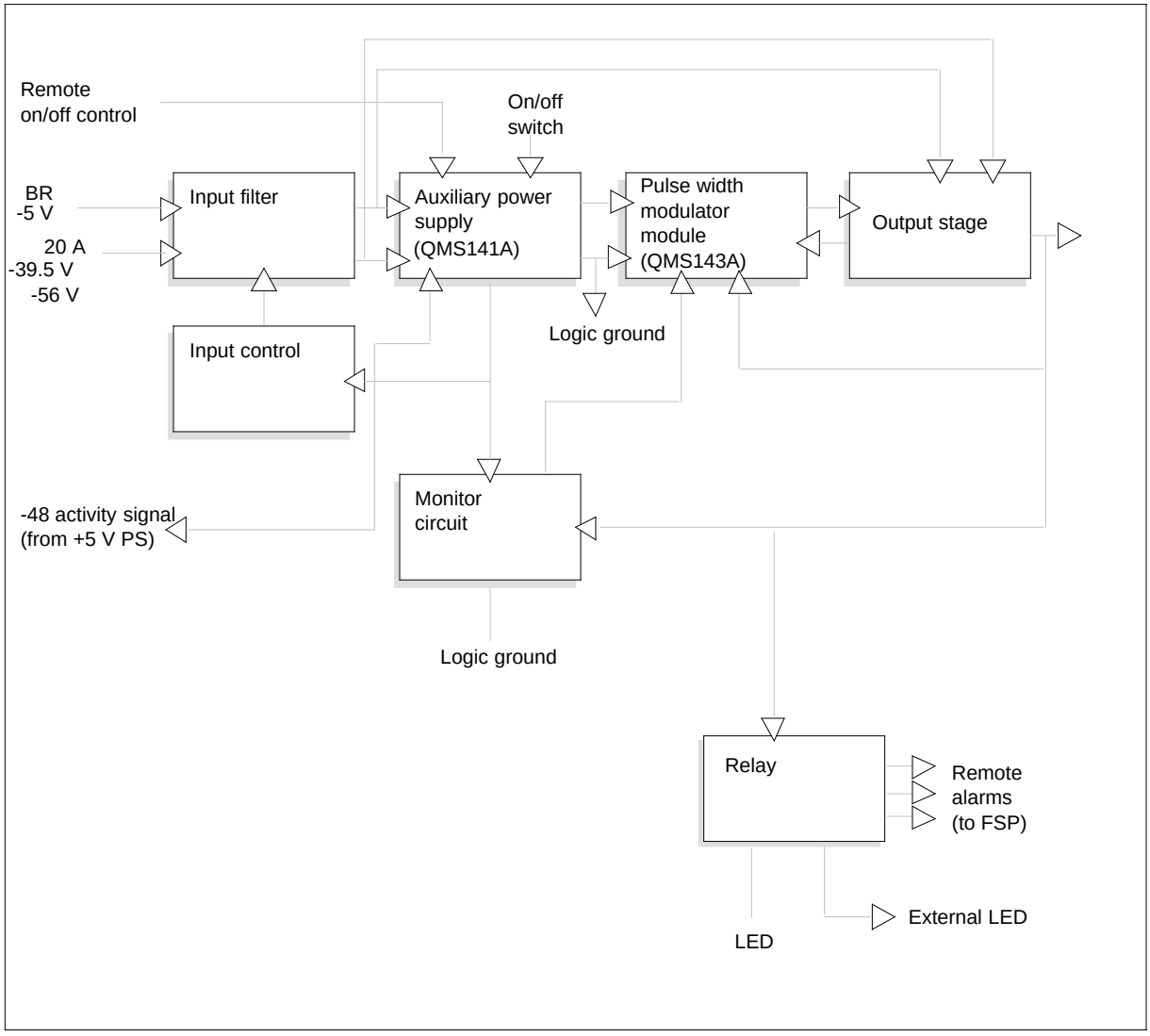
The NT9X31AA contains the following functional blocks:

- input filter
- auxiliary power supply
- the PWM module
- output stage, which includes transformer, rectifier, and filter
- input control
- monitor circuit
- relay

The relationship between the functional blocks appears in the following figure.

NT9X31AA (continued)

NT9X31AA functional blocks



Technical data

Power requirements

Input

The nominal input voltage is -48 V. The allowed range is from a minimum -39.5 V to maximum -56 V. The maximum input current is 4 A.

Output

The output specifications appear in the follwing table.

Output specifications	
Voltage	-5.2 V ±2%
High voltage shutdown	-6.5 V ±0.5V
Low voltage shutdown	-4.3 V ±0.3V
Ripple	50 mV rms
Maximum current	20 A
Minimum current	0 A
Current limit	24 A ±3A

NT9X31AB

Product description

The NT9X31AB is a dc-to-dc power converter. The NT9X31AB is the 60V version of the NT9X31AA for DMS-100 SuperNode frames.

Functional description

A 60-V office battery is the power source for the converter. A standard input filter circuit filters the power source. The power source input can range from -39.5V to -75V.

The QMS141A is an auxiliary power supply module. The input feeds to QMS141A to isolate the input battery from the housekeeping circuits. At the output stage, the switching transformer assures isolation. This converter provides -5.20V at 20A and has a current limiter circuit to protect against overload.

The pulse width modulation (PWM) module, QMS143A, drives the output stage. Feedback signals from the output, current condition, and possible fault condition feed to this module. These signals and conditions feed to the module to assure regulation and prevent damage that internal or external faults can cause.

A monitor circuit supervises the output for over- and under-voltage conditions. If the output voltage goes below -4.3 V ±0.3 V or above -6.5V ±0.5V, the following occurs:

- The monitor generates signals for shutdown.
- Alarm signals appear at the back panel.
- The red fault indicator light-emitting diode (LED) lights.
- The converter shuts down.

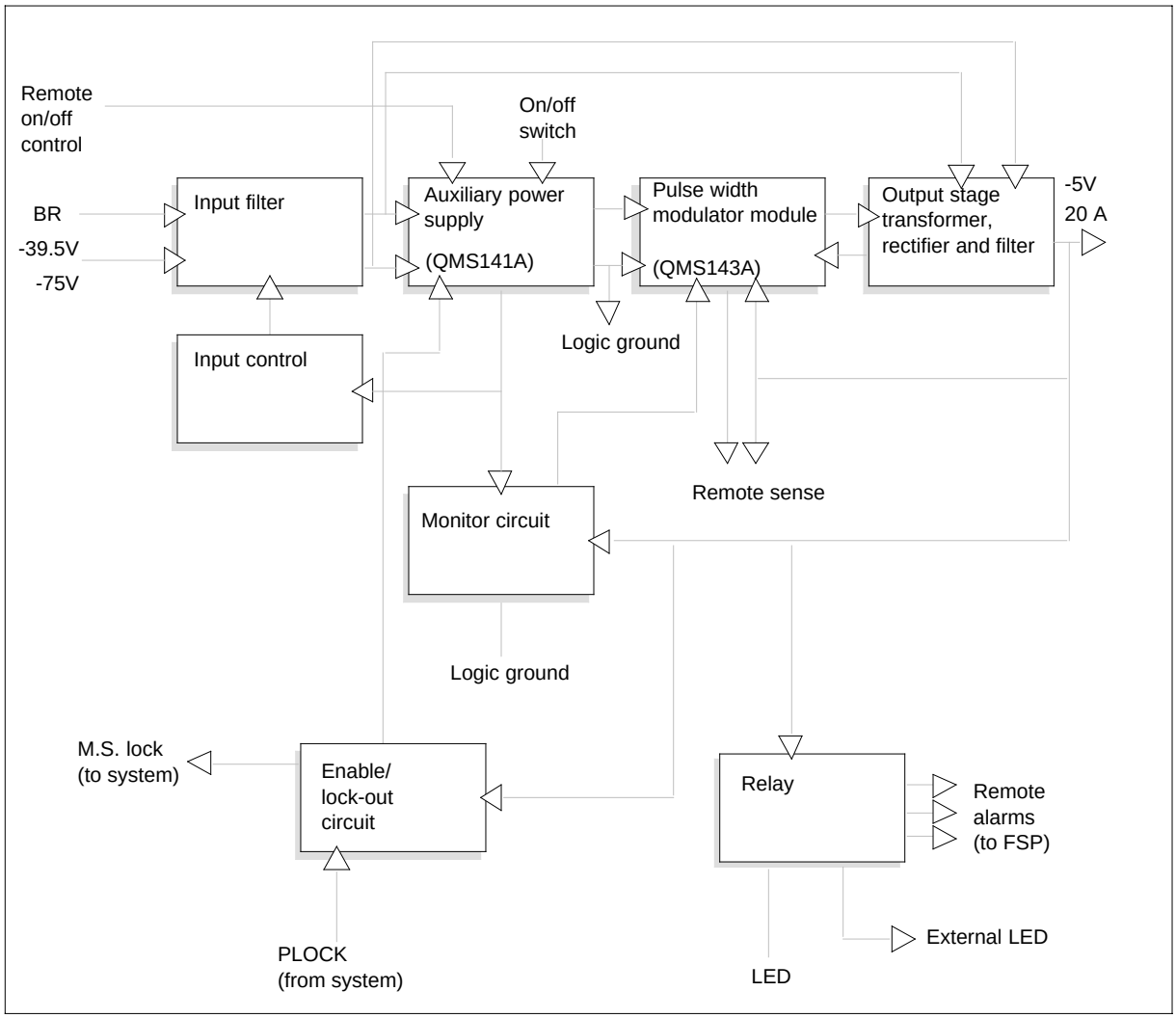
Functional blocks

The NT9X31AB contains the following functional blocks:

- input section
- input control
- auxiliary power supply
- the PWM module
- monitor circuit
- output stage, which includes transformer, rectifier, and filter

The relationship between the functional blocks appears in the following figure.

NT9X31AB functional blocks



Input section

The input section contains the following parts:

- a metal-oxide clamp across the input that limits maximum surge voltage
- an inrush thermistor that limits the charging current
- a high-frequency filter that reduces the amount of noise and electromagnetic interference (EMI) that feeds back to the source

Auxiliary power supply

The QMS141 auxiliary supply module provides the power for the control and monitor circuits.

NT9X31AB (continued)

Input control section

An enable switch is on the faceplate of the converter. To power up or shut down the converter requires use of the enable switch. The system also supports remote start-up and shut-down signals. Activation of the enable switch turns on the auxiliary supply module. This module supplies power to the U2 monitor circuit and the QMS143A pulse-width modulator (PWM) controller module. Relays activate when the auxiliary supply voltage is present.

Pulse width modulator module

A current-sense transformer senses the transistor current. The information feeds back to the PWM controller to limit the current in the single transistor. The QMS143A PWM controller module connects to the output return. The controller directly senses the output voltage to control the transistor switching. The transistor chops the input dc voltage and applies the ac waveform alternately across the primary input of the power transformer.

Monitor circuit

The regulated output voltage can rise above a fixed level, or fall below a specified level. In this occurrence, the monitor circuit sends a signal to the PWM to shut down the converter. The converter does not automatically restart. The converter remains off until you manually start the converter again.

Output stage

The transformer provides a lower amplitude ac squarewave. The squarewave is rectified and filtered to produce the correct dc output voltage. A shunt resistor preloads this output. At the output, decoupling occurs.

Signaling

Pin numbers

The pin numbers for the NT9X31AB appear in the following table.

Connector P1 CBR05 48 pin (Sheet 1 of 2)

Pin	Z	B	D
2	D2-5	D1-5	D0-5
4	D5-5	D4-5	D3-5
6	CS-5	+5V	D6-5
8	A1-5	A2-5	A3-5
10	A0-5	RAS/NC	RAS/C
12	R.A.S./NO	-ABS	EXT.LED

Connector P1 CBR05 48 pin (Sheet 2 of 2)

Pin	Z	B	D
14	D7-5	NOCON-A	NOCON-B
16	BR.ABS	-5V	-5V
18	LR	LR	LR
20	-5V	-5V	-5V
22	LR	LR	LR
24	-5V	-5V	-5V
26	LR	LR	LR
28	-5V	-5V	-5V
30	LR	LR	LR
32	-5V	-5V	-5V

Connector P1 CBR05 48 pin (Sheet 1 of 2)

Pin	Z	B	D
2	LR	LR	LR
4	-5V	-5V	-5V
6	LR	LR	LR
8	-5V	-5V	-5V
10	LR	LR	LR
12	-5V	-5V	-5V
14	LR	LR	LR
16	-5V	-5V	-5V
18	-BACT.SIG	LR	LR
20	SD	REM.START	-BATT
22	REM.SHDN	+15V	-5VTEST
24	EXT.SW.ON	EXT.SW.OFF	EXT.SWT

NT9X31AB (end)

Connector P1 CBR05 48 pin (Sheet 2 of 2)

Pin	Z	B	D
26	-BAT	-BAT	-BAT
28	-BAT	-BAT	-BAT
30	BR	BR	BR
32	BR	BR	BR

Technical data

Power requirements

Input

The nominal input voltage is -60 V. The allowed range is from a minimum of -52 V to a maximum -72 V. The maximum input current is 4 A.

Output

Output specifications	
Voltage	-5.15 V ± 2%
High voltage shutdown	-6.5 V ± 0.5 V
Low voltage shutdown	-4.3 V ± 0.3 V
Ripple	50 mV rms
Maximum current	20 A
Minimum current	0 A
Current limit	24 A ± 3 A

Product description

The NT9X32AA DMS-bus load paddle board is for the DMS-bus environment. The card maintains a constant load distribution on the main clock and frame pulse signals that drive the shelf. This card function is separate from card group or shelf type (master or extension). An improvement in signal edge accuracy, noise margin, and duty cycle on these key signals is the result of this condition.

Location

The NT9X32AA is in a message switch (MS) shelf, in the following slots:

- slot 7, behind the NT9X52 if NT9X24 is not present (master shelf)
- slot 10, behind the NT9X14 (master shelf)
- slot 12-28 if NT9X17 is not present (master shelf)
- slot 8-31 if NT9X17 is not present (extension shelf)

Functional description

Functional blocks

The NT9X32AA contains the following functional blocks:

- load section
- processor interface

Load section

This block provides the correct load distribution in the shelf. The clock frame pulse distribution system in the DMS-bus uses a controlled impedance structure to guarantee signal accuracy. This distribution system contains the following three elements:

- a driver that contains two devices in a single 74F244 pack that connects directly in parallel. The pack connects at the inputs and outputs of the devices
- resistive termination that uses equal values for both registers. Resistive termination establishes a valid logic level if the system disables the clock during maintenance.
- transmission line to join the driver and termination. This line has interconnections along the back panel. This line has short tracks that interconnect on the NT9X52, NT9X49BA, and NT9X49CA also.

Processor interface

This block permits the card to conform to the standard SuperNode element identification and power-up bit structures. To be compatible with SuperNode

cards, the load card responds to a processor access. The load card treats the processor access like a 16-bit machine. Only 80 of the data bits are driven.

NT9X35CA

Product description

The NT9X35CA enhanced network (ENET) crosspoint card performs the nonblocking switching function for the 128-K ENET. The NT9X35CA accepts 16-K pulse code modulation (PCM) input channels. The NT9X35CA receives these channels from the vertical bus (V-bus). The NT9X35CA switches the channels to any of 16-K PCM output channels on the horizontal bus (H-bus). The V-bus receives and carries data from the 128-K ENET interface paddle boards. These paddle boards can be NT9X40BA (ENET+ quad fiber paddle board) with four DS512 links, or NT9X41BA (16-port DS30 paddle board). The NT9X41BA is equal to one DS512.

When the crosspoint card is at the far left and right of the H-bus, the card terminates the H-bus. The card terminates the H-bus with an impedance that matches the backplane.

The NT9X35CA uses a double buffer design. The double buffer design allows a constant one-frame delay for all channels. This condition permits switching of services required for wideband services. The switching of services is not limited. The insertion of PCM data on a specified time slot of the H-bus causes switching. The crosspoint card receives and stores the PCM data. Each crosspoint card has connection memory that controls the output of the card. The correct crosspoint cards receives outgoing PCM data from the H-bus. The data is formatted and serialized for transmission on the fiber optic links or DS30.

Functional description

The NT9X35CA card performs the following functions:

- acceptance of a maximum 2-K input channels (four DS512) from the associated paddle board of the card
- distribution of the four received DS512 to the specified section of the V-bus
- acceptance of a maximum 14-K input channels from the V-bus
- alignment of the incoming V-bus data to the local shelf frame
- store of the 16-K input channels into one half of the data memory
- read-out of 16-K output channels from the other half of the memory and sends the channels on the H-bus
- alternation between the two halves of the memory to provide double buffering
- follow of the V-bus to H-bus mapping stored in the connection memories

NT9X35CA (continued)

- access and read of the section of the H-bus that associates with the card slot where the crosspoint card connects
- interface with the shelf controller (NT9X13) through the processor bus (P-bus)
- insertion and removal of test codes at different points on the card
- insertion and removal of pseudo-random data at different points on the card

Functional blocks

The NT9X35CA contains of the following functional blocks:

- the V-bus interface
- crosspoint modules
- the H-bus interface
- the P-bus interface
- clock generation

Vertical bus interface

The V-bus interface receives data from the paddle board and feeds the data into the main interface mode. The main interface mode connects the data to a V-bus section. The V-bus distributes the data to crosspoint cards in a vertical column in a cabinet. The crosspoint cards associate in pairs, or mates, that are side by side in each shelf. A mate card receives PCM from the V-bus of the mate. The mate card gives PCM from the V-bus to the mate. Each card has 16-K channels of input. A maximum of eight cards in one 128-K ENET cabinet can share the same inputs with this arrangement.

Crosspoint modules

The data streams that the V-bus interface provides transmit to the crosspoint modules for time switching.

Horizontal bus interface

The H-bus distributes switched PCM from the crosspoint cards in each shelf to the fiber optic links. The H-bus distributes switched PCM for transmission out of the 128-K ENET.

Processor bus interface

The P-bus interface block performs the following functions:

- buffer of data and control signals between the P-bus and the NT9X35CA card
- decoding of addresses for access to elements on the card

- identification of PROM that contains the NT9X35CA card code and version numbers
- decoding of addresses for the paddle board enable signal
- control of the lockout feature of the NT9X35CA
- generation of the select strobes for the paddle board

Clock generation

This block receives two clocks and one frame pulse. The block generates all the clocks and frame pulses for the card and the paddle board.

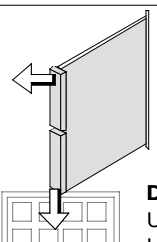
Signaling

Pin numbers

The pin numbers for NT9X35CA appear in the following figures.

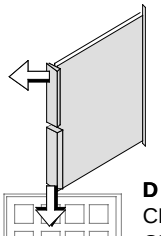
NT9X35CA (continued)

NT9X35CA pin numbers (Part 1 of 2)



	D	C	B	A
1	UAFP	GND	UBFB	GND
2	UA0	UA1	UB0	UB1
3	UA2	UA3	UB2	UB3
4	UA4	UA5	UB4	UB5
5	UA6	UA7	UB6	UB7
6	UA8	UA9	UB8	UB9
7	UCFP	GND	UDFP	GND
8	UC0	UC1	UD0	UD1
9	UC2	UC3	UD2	UD3
10	UC4	UC5	UD4	UD5
11	UC6	UC7	UD6	UD7
12	UC8	UC9	UD8	UD9
13	GND	GND	GND	GND
14	MAFP	GND	MBFB	GND
15	MA0	MA1	MB0	MB1
16	MA2	MA3	MB2	MB3
17	MA4	MA5	MB4	MB5
18	MA6	MA7	MB6	MB7
19	MA8	MA9	MB8	MB9
20	MCFP	GND	MDFP	+5V
21	MC0	MC1	MD0	MD1
22	MC2	MC3	MD2	MD3
23	MC4	MC5	MD4	MD5
24	MC6	MC7	MC6	MD7
25	MC8	MC9	MD8	MD9
26	DA31	RDAT0	RDAT1	GND
27	DA30	RDAT2	RDAT3	+5V
28	DA29	RDAT4	RDAT5	+5V
29	DA28	RDAT6	RDAT7	GND
30	DA27	RDAT8	RDAT9	+5V
31	DA26	WBUS0	WBUS1	+5V
32	DA25	WBUS2	WBUS3	GND
33	DA24	WBUS4	WBUS5	-5V
34	NSEL0	WBUS6	WBUS7	-5V
35	NSEL1	WBUS8	WBUS9	-5V
36	NSEL2	RESET-	RNW	-5V
37	NSEL3	ACK-	DAS32-	GND
38	NSTB0	NMPEN	NSPEN	GND
39	NSTB1			+5V
40	NSTB2	ADDR02	ADDR03	+5V
41	NSTB3	ADDR04	ADDR05	+5V
42		ADDR06	ADDR07	+5V
43		ADDR08	ADDR09	GND
44	NCSEN	ADDR10	ADDR11	+5V
45	CD0	ADDR12	ADDR13	+5V

NT9X35CA pin numbers (Part 2 of 2)



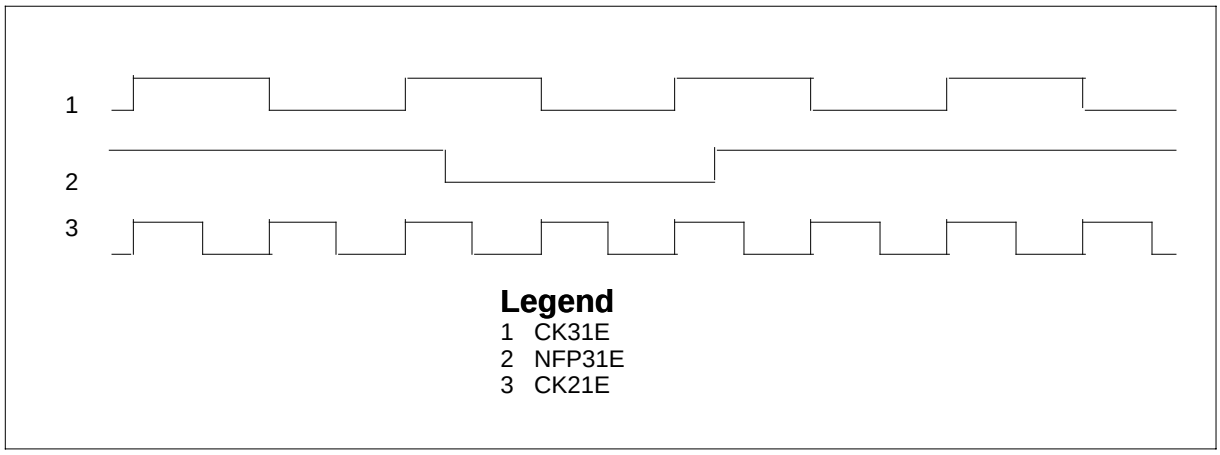
	D	C	B	A
46	CK21P+	ADDR14	CD3	+5V
47	CK21P-	CD1	CD2	+5V
48	NFP21E+			GND
49	NFP21E-			+5V
50	CK61	CK21E-	CK21E+	+5V
51	NFP61	CK31E-	CK31E+	+5V
52	NTFP61	NFP31E-	NFP31E+	+5V
53	GND	GND	CD4	GND
54	H00	H01	H10	H11
55	H02	H03	H12	H13
56	H04	H05	H14	H15
57	H06	H07	H16	H17
58	H08	H09	H18	H19
59	GND	GND	GND	GND
60	H20	H21	H30	H31
61	H22	H23	H32	H33
62	H24	H25	H34	H35
63	H26	H27	H36	H37
64	H28	H29	H38	H39
65	GND	GND	GND	GND
66	H40	H41	H50	H51
67	H42	H43	H52	H53
68	H44	H45	H54	H55
69	H46	H47	H56	H57
70	H48	H49	H58	H59
71	GND	GND	GND	+5V
72	H60	H61	H70	H71
73	H62	H63	H72	H73
74	H64	H65	H74	H75
75	H66	H67	H76	H77
76	H68	H69	H78	H79
77	GND	GND	GND	GND
78	LAFP	GND	LBFB	GND
79	LA0	LA1	LB0	LB1
80	LA2	LA3	LB2	LB3
81	LA4	LA5	LB4	LB5
82	LA6	LA7	LB6	LB7
83	LA8	LA9	LB8	LB9
84	LCFP	GND	LDFP	GND
85	LC0	LC1	LD0	LD1
86	LC2	LC3	LD2	LD3
87	LC4	LC5	LD4	LD5
88	LC6	LC7	LD6	LD7
89	LC8	LC9	LD8	LD9
90	GND	GND	GND	GND

NT9X35CA (end)

Timing

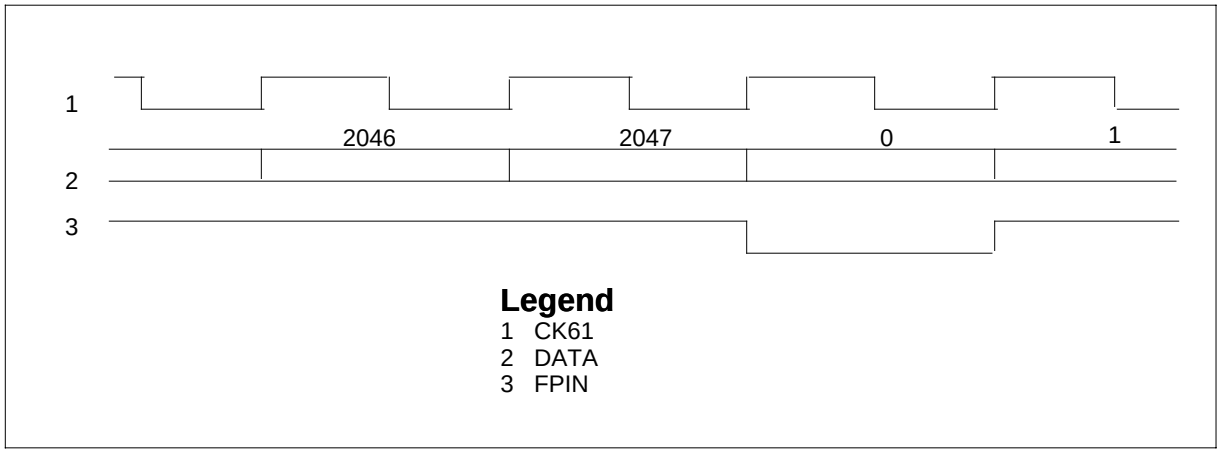
The frame pulse timing of the NT9X35CA appears in the following figure.

NT9X35CA frame pulse timing



The V-bus timing appears in the following figure.

NT9X35CA V-bus timing



Technical data

Power requirements

The NT6X35BA requires a maximum of +5 V and a minimum of -5.2 V, with a variance of ±5%.

NT9X35FA

Product description

The NT9X35FA crosspoint (XPT) card performs a non-blocking switching function for the SuperNode SE, 16K enhanced network (ENET).

This card is a depopulated version of the NT9X35CA crosspoint card. The 128-K ENET system uses the NT9X35CA card. The NT9X35FA does not operate in the 128-K ENET system. The NT9X35CA does not operate in the SuperNode SE, 16-K ENET system.

Functional description

The NT9X35FA crosspoint card performs DS0 switching for a maximum of 4096 pulse code modulated (PCM) incoming channels. The incoming channels are on the vertical bus (V-bus). The card performs DS0 switching for the 8192 PCM outgoing channels on the horizontal bus (H-bus). The card remains nonblocking in all conditions. The NT9X35FA can accept data from the link paddle boards: NT9X40BA, NT9X40BB, NT9X41BA, and NT9X45BA.

The NT9X35FA uses a double buffer that causes a constant one-frame delay for channels that pass through the network. This condition allows switching of N times 64 Kbps services required for wideband applications. The switching is not limited.

The NT9X35FA circuit pack performs the following functions:

- acceptance of a maximum 2-K input channels (4 DS-512) from the associated paddle board of the circuit pack
- distribution of the four received DS-512 channel grouping to section 3 of the V-bus for transmission to the mate card
- acceptance of another 2-K input channels from the mate card V-bus
- store of the 4-K input channels in one half of the data memory
- read of the 8-K output channels from the second half of the memory and transmits the data on the H-bus
- alternation between the two halves of the memory to provide double buffering
- follow of the V-bus to H-bus mapping in the connection memories
- access and read of the section of the H-bus that associate with the card slot of the XPT
- use of the processor bus (P-bus) to connect with the shelf processor (NT9X35FA)

NT9X35FA (continued)

- insertion and removal of test codes
- insertion and removal of pseudo-random data
- termination for the H-bus on each card

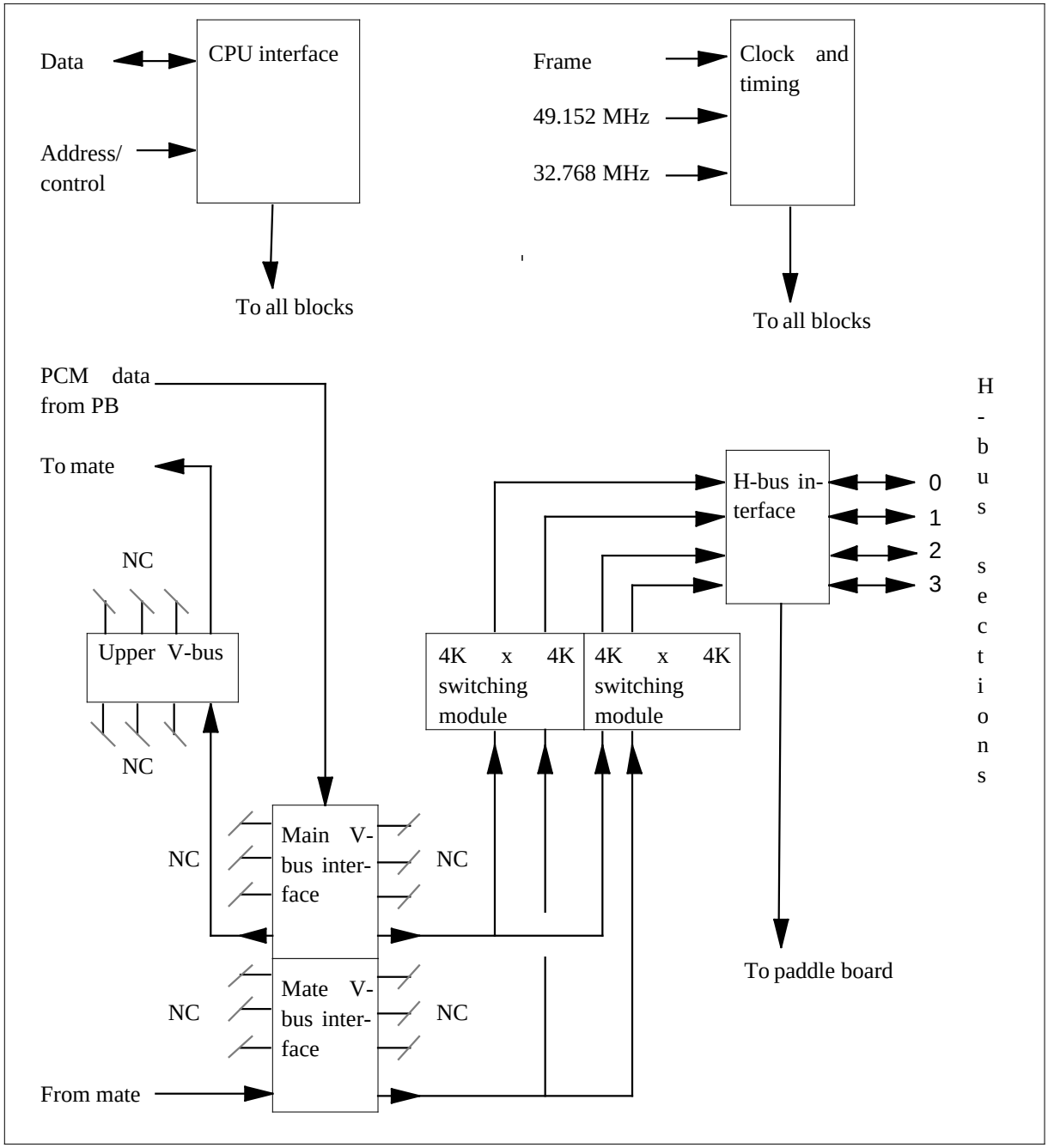
Functional blocks

The NT9X35FA contains the following functional blocks:

- the V-bus interface
- the XPT modules
- the H-bus interface
- the P-bus interface
- clock generation

The relationship between the functional blocks appears in the following figure.

The NT9X35FA functional blocks



Vertical bus interface

The V-bus interface shares the incoming data from the paddle board with the mate card. Data from the paddle board transmits to the main interface V-bus interface chip (BIF). The BIF connects to the V-bus PCM group 3. The XPT

NT9X35FA (continued)

card receives and stores the data. The data passes to the upper V-bus BIF to make the data available to the mate card.

Crosspoint modules

The NT9X35FA has two XPT modules. Each module contains 4-K by 4-K switching modules. The XPT modules perform a time switch of the two data streams that the V-bus interface provides. Each data stream has 2-K channels. A total of 4-K channels are available. All the data buses run at the same time at 16.384 Mbps.

Horizontal bus interface

The H-bus distributes switched PCM data from the XPTs on the shelf to the paddle board links. The H-bus distributes switched PCM data for transmission out of the SNSE 16K ENET. Each H-bus interface receives 2048 channels from the H-bus for the network interface to transmit to the paddle boards. The H-bus is a tri-state bus. This condition allows a card connected to the bus to drive the bus on specified channels.

Processor bus interface

The P-bus interface is an asynchronous bus that allows the shelf processor () to set up connections. The P-bus interface allows the processor to perform maintenance tasks on the NT9X35FA.

Clock generation

The clock generation block receives two clocks and one frame pulse. The block generates the clocks and frame pulses for the card and the paddle board.

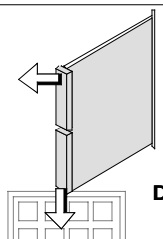
Signaling

All signals are normally single-ended transistor-transistor logic (TTL).

Pin Numbers

The pin numbers for the NT9X35FA appear in the following figures.

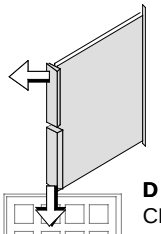
NT9X35FA pin numbers (Part 1 of 2)



	D	C	B	A
1		GND		GND
2				
3				
4				
5				
6				
7		GND	UDFP	GND
8			UD0	UD1
9			UD2	UD3
10			UD4	UD5
11			UD6	UD7
12			UD8	UD9
13	GND	GND	GND	GND
14		GND		GND
15				
16				
17				
18				
19				
20		GND	MNFP	+5V
21			MD0	MD1
22			MD2	MD3
23			MD4	MD5
24			MD6	MD7
25			MD8	MD9
26	DA31	RDAT0	RDAT1	GND
27	DA30	RDAT2	RDAT3	+5V
28	DA29	RDAT4	RDAT5	+5V
29	DA28	RDAT6	RDAT7	GND
30	DA27	RDAT8	RDAT9	+5V
31	DA26	WBUS0	WBUS1	+5V
32	DA25	WBUS2	WBUS3	GND
33	DA24	WBUS4	WBUS5	-5V
34	NSEL0	WBUS6	WBUS7	-5V
35	NSEL1	WBUS8	WBUS9	-5V
36	NSEL2	RESET-	RNW	-5V
37	NSEL3	ACK-	DAS32-	GND
38	NSTB0	NMPEN	NSPEN	GND
39	NSTB1	ADDR00	ADDR01	+5V
40	NSTB2	ADDR02	ADDR03	+5V
41	NSTB3	ADDR04	ADDR05	+5V
42		ADDR06	ADDR07	+5V
43		ADDR08	ADDR09	GND
44	NCSEN	ADDR10	ADDR11	+5V
45	CD0	ADDR12	ADDR13	+5V

NT9X35FA (end)

NT9X35FA pin numbers (Part 2 of 2)



	D	C	B	A
46	CK21P+	ADDR14	CD3	+5V
47	CK21P-	CD1	CD2	+5V
48	NFP21E+			GND
49	NFP21E-			+5V
50	CK61	CK21E-	CK21E+	+5V
51	NFP61	CK31E-	CK31E+	+5V
52	NTFP61	NFP31E-	NFP31E+	+5V
53	GND	GND	CD4	GND
54	H00	H01	H10	H11
55	H02	H03	H12	H13
56	H04	H05	H14	H15
57	H06	H07	H16	H17
58	H08	H09	H18	H19
59	GND	GND	GND	GND
60	H20	H21	H30	H31
61	H22	H23	H32	H33
62	H24	H25	H34	H35
63	H26	H27	H36	H37
64	H28	H29	H38	H39
65	GND	GND	GND	GND
66				
67				
68				
69				
70				
71	GND	GND	GND	+5V
72				
73				
74				
75				
76				
77	GND	GND	GND	GND
78		GND		GND
79				
80				
81				
82				
83				
84		GND		GND
85				
86				
87				
88				
89				
90	GND	GND	GND	GND

NT9X36BA

Product description

The NT9X36BA enhanced network (ENET) message clock card provides two DS512 message links. The message links are between the ENET shelf processor and the message switch. The NT9X36BA provides the clocks and timing signals that the shelf requires. These clocks are synchronized to an incoming DS512 with a phase-locked loop (PLL). The PLL provides system synchronization.

Functional description

The associated paddle board of the NT9X36BA card is NT9X40BA (ENET+ quad fiber paddle board). The NT9X36 BA and the associated paddle board provide two DS512 communication links between the ENET shelf and the duplicated message switches. One link is available for each plane. The card synchronizes the shelf local oscillator to the reference that the message switches provide through the DS512 links provide. The frame pulse of the selected link drives a PLL, which includes the local oscillator. The oscillator generates the necessary clock signals and frame pulses for the shelf. An on-board microcontroller (8031) manages the PLL operation.

The DS512 links to the message switch provide communication with the ENET shelf and with the peripherals. The NT9X36BA intercepts time slots reserved for communication with ENET. All time slots route to an associated crosspoint card. The time slots can cross-connect and transmit to the attached peripherals at the crosspoint card.

The NT9X36BA is a support card for the shelf and the local processor of the shelf. The local processor is on the NT9X13 CPU card. The NT9X36BA provides functions like address decoding and data acknowledge generation.

Functional blocks

The NT9X36BA contains the following functional blocks:

- pulse code modulation (PCM) interface
- the PLL
- transitor-transitor logic (TTL) clock and frame pulse generation
- emitter-coupled logic (ECL) clock and frame pulse generation
- message interface
- processor bus (P-bus) interface

NT9X36BA (continued)

Pulse code modulation interface

The network PCM interface receives PCM from the receive data (RDAT) bus. The RDAT contains the received data removed from all four DS512 links. The NT9X40BA paddle board removes the data from the links. The NT9X36BA uses links A and C for messaging to the network shelf processor. The RDAT bus goes to a dedicated crosspoint card pair for switching of channels to external peripheral modules (PM).

The H-bus interface latch obtains data from the 2-K channel horizontal bus (H-bus). Time slot data for links B and D are time aligned and transmit directly to the NT9X40BA paddle board. Data from links A and B combine with the message data from the message interface and transmit to the paddle board. Software programs a configuration design to control the message time slot allocation. The message time slot allocation is for the receive and transmit direction of the message links.

Phase locked loop

This block contains the digital PLL for clock synchronization. The PLL contains the following components:

- two phase comparators
- a 12-bit digital-to-analog converter (DAC)
- a 98.304-MHz VCXO
- an 8031 processor to implement the loop filter

Emitter-coupled logic clocks and frame pulse generation

The voltage controlled crystal oscillator (VCXO) output (98.304 MHz) produces three clocks. These clocks run at 49.152 MHz, 32.768 MHz, and 16.384 MHz. Differential ECL drivers distribute the three frame pulses. One driver is for each crosspoint card pair in the shelf to minimize the skew between the three signals. The 32.768-MHz clock resamples the 32.768-MHz frame pulse before the frame pulse works on the NT9X35BA crosspoint cards. The 49.152-MHz clock clocks the resampled 49.152-MHz frame pulse to generate the frame pulse on the crosspoint clocks.

The NT9X41BA (16-port DS30 paddle board) requires the 10.24-MHz clock. The NT9X41BA uses ECL to generate the clock. The 98.304-MHz clock is alternatively divided by 9 and 10. The 10.24 MHz converts to TTL level for transmission to the backplane. The 10.24-MHz clock synchronizes to the 16.384 divider chain. The clock synchronizes to this chain to phase lock the 16.384-MHz frame pulses with the 10.24-MHz frame pulse.

The 16.384 MHz divider chain generates the 10.24-MHz frame pulse. The 10.24-MHz clock clocks the frame pulse again to maintain the correct pulse width.

TTL clocks and frame pulse generation

The ECL clocks translate into TTL levels. The TTL clock section uses the ECL clocks for other board functions. The 16.384-MHz clock feeds into a divider change to generate a 125-µs frame period. System ECL frame pulses, and different 16.384-MHz frame pulses result from this condition.

Message interface

The block handles the link control protocol for message transfer on the DS512 links between the message switch and the SP. The block includes the buffer and first-in first-out (FIFO) memory to store or retrieve messages for the SP.

Processor-bus interface

The P-bus interface block performs the following functions:

- buffer of address, data, and control signals
- decoding of addresses for access to elements on the card
- identification (ID) PROM that contains the NT9X36BA card code and version numbers
- decoding of addresses for the maintenance and suds pages for the other shelf cards
- decoding of addresses for the power converter ID PROMs
- decoding of the byte enable lines BEN0-to BEN3- to generate address bits ADD0 and ADD1 again. The crosspoint cards use these address bits.
- pull up of the P-bus data bus

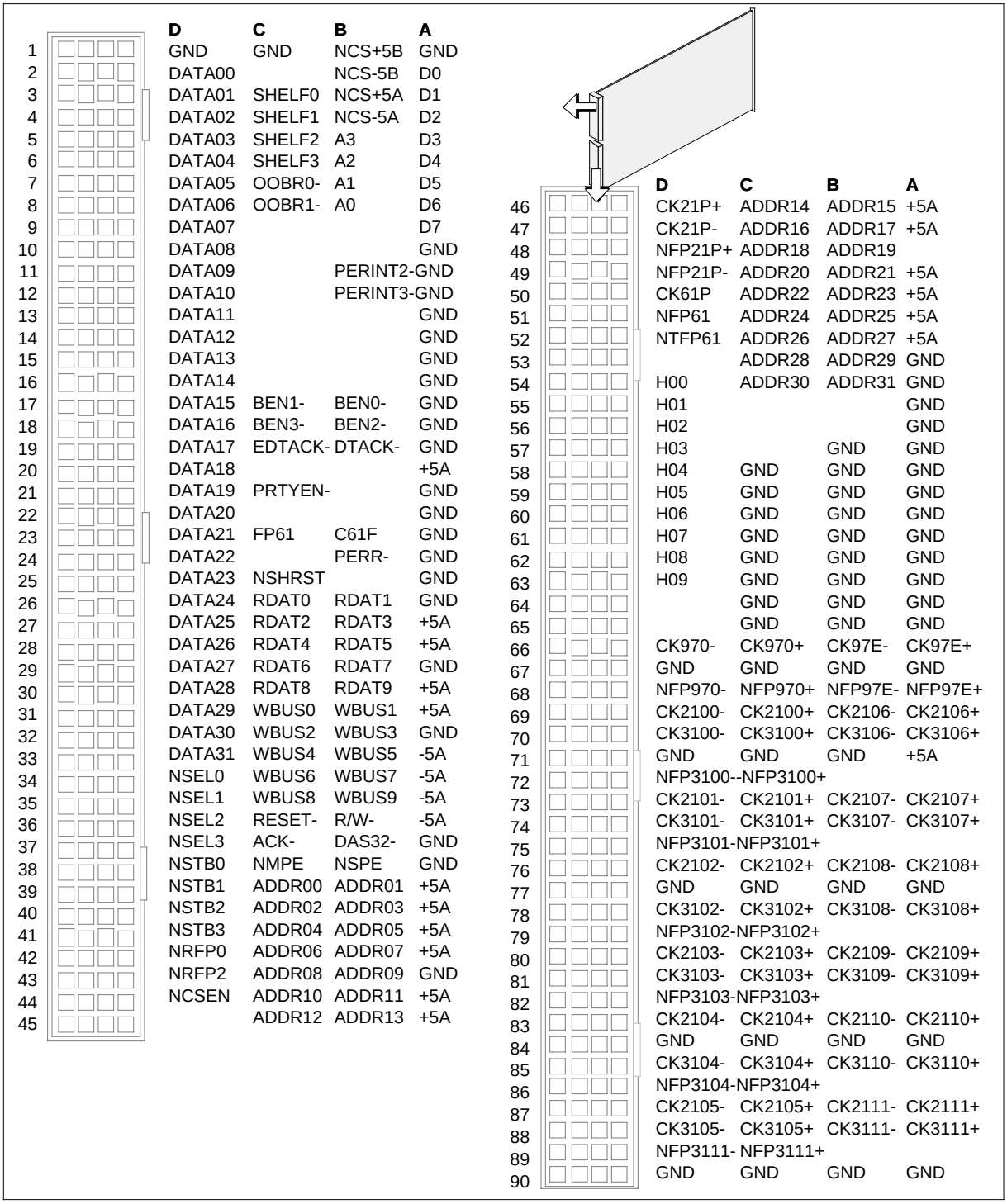
Signaling

Pin numbers

The pin numbers for the NT9X36BA appear in the following figure.

NT9X36BA (continued)

The NT9X36BA pin numbers



	D	C	B	A
1	GND	GND	NCS+5B	GND
2	DATA00		NCS-5B	D0
3	DATA01	SHELF0	NCS+5A	D1
4	DATA02	SHELF1	NCS-5A	D2
5	DATA03	SHELF2	A3	D3
6	DATA04	SHELF3	A2	D4
7	DATA05	OOBR0-	A1	D5
8	DATA06	OOBR1-	A0	D6
9	DATA07			D7
10	DATA08			GND
11	DATA09		PERINT2-	GND
12	DATA10		PERINT3-	GND
13	DATA11			GND
14	DATA12			GND
15	DATA13			GND
16	DATA14			GND
17	DATA15	BEN1-	BEN0-	GND
18	DATA16	BEN3-	BEN2-	GND
19	DATA17	EDTACK-	DTACK-	GND
20	DATA18			+5A
21	DATA19	PRTYEN-		GND
22	DATA20			GND
23	DATA21	FP61	C61F	GND
24	DATA22		PERR-	GND
25	DATA23	NSHRST		GND
26	DATA24	RDAT0	RDAT1	GND
27	DATA25	RDAT2	RDAT3	+5A
28	DATA26	RDAT4	RDAT5	+5A
29	DATA27	RDAT6	RDAT7	GND
30	DATA28	RDAT8	RDAT9	+5A
31	DATA29	WBUS0	WBUS1	+5A
32	DATA30	WBUS2	WBUS3	GND
33	DATA31	WBUS4	WBUS5	-5A
34	NSEL0	WBUS6	WBUS7	-5A
35	NSEL1	WBUS8	WBUS9	-5A
36	NSEL2	RESET-	R/W-	-5A
37	NSEL3	ACK-	DAS32-	GND
38	NSTB0	NMPE	NSPE	GND
39	NSTB1	ADDR00	ADDR01	+5A
40	NSTB2	ADDR02	ADDR03	+5A
41	NSTB3	ADDR04	ADDR05	+5A
42	NRFP0	ADDR06	ADDR07	+5A
43	NRFP2	ADDR08	ADDR09	GND
44	NCSEN	ADDR10	ADDR11	+5A
45		ADDR12	ADDR13	+5A

	D	C	B	A
46	CK21P+	ADDR14	ADDR15	+5A
47	CK21P-	ADDR16	ADDR17	+5A
48	NFP21P+	ADDR18	ADDR19	
49	NFP21P-	ADDR20	ADDR21	+5A
50	CK61P	ADDR22	ADDR23	+5A
51	NFP61	ADDR24	ADDR25	+5A
52	NTFP61	ADDR26	ADDR27	+5A
53		ADDR28	ADDR29	GND
54	H00	ADDR30	ADDR31	GND
55	H01			GND
56	H02			GND
57	H03		GND	GND
58	H04	GND	GND	GND
59	H05	GND	GND	GND
60	H06	GND	GND	GND
61	H07	GND	GND	GND
62	H08	GND	GND	GND
63	H09	GND	GND	GND
64		GND	GND	GND
65		GND	GND	GND
66	CK970-	CK970+	CK97E-	CK97E+
67	GND	GND	GND	GND
68	NFP970-	NFP970+	NFP97E-	NFP97E+
69	CK2100-	CK2100+	CK2106-	CK2106+
70	CK3100-	CK3100+	CK3106-	CK3106+
71	GND	GND	GND	+5A
72	NFP3100-	-NFP3100+		
73	CK2101-	CK2101+	CK2107-	CK2107+
74	CK3101-	CK3101+	CK3107-	CK3107+
75	NFP3101-	NFP3101+		
76	CK2102-	CK2102+	CK2108-	CK2108+
77	GND	GND	GND	GND
78	CK3102-	CK3102+	CK3108-	CK3108+
79	NFP3102-	NFP3102+		
80	CK2103-	CK2103+	CK2109-	CK2109+
81	CK3103-	CK3103+	CK3109-	CK3109+
82	NFP3103-	NFP3103+		
83	CK2104-	CK2104+	CK2110-	CK2110+
84	GND	GND	GND	GND
85	CK3104-	CK3104+	CK3110-	CK3110+
86	NFP3104-	NFP3104+		
87	CK2105-	CK2105+	CK2111-	CK2111+
88	CK3105-	CK3105+	CK3111-	CK3111+
89	NFP3111-	NFP3111+		
90	GND	GND	GND	GND

Timing

The timing specifications for the input and output of the card appear in the following table.

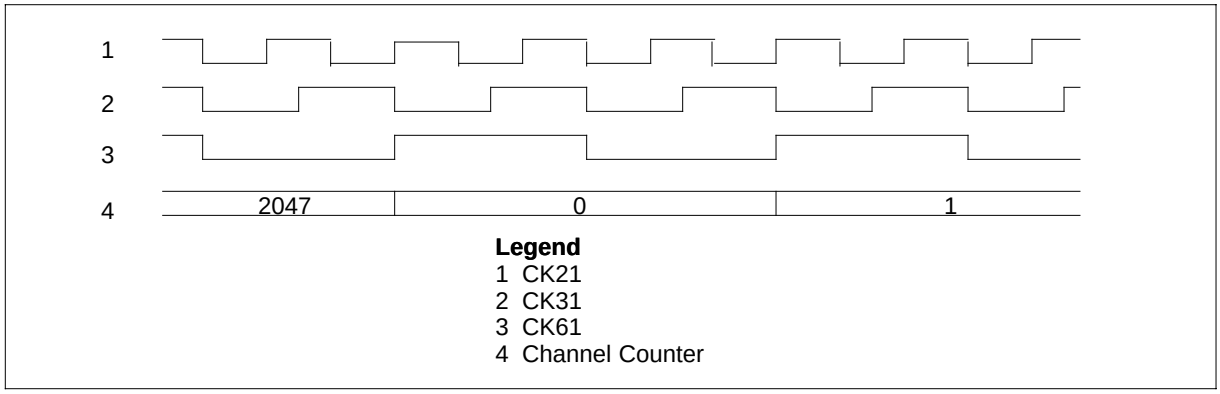
Timing specifications for NT9X36BA clocks and frame pulses

Clocks and frame pulses	Frequency	Duty cycle	Level
CK2100+, CK2100- to CK2111+, CK2111	-49.152 MHz	nominal 50%, worst case 48-52%	ECL, differential
CK3100+, CK3100- to CK3111+, CK3111	-32.768 MHz	nominal 50%, worst case ±2%	ECL, differential
CK61	16.384 MHz	nominal 50%, worst case 45-55%	TTL
NFP21P+, NFP21P	-8.0 kHz	high 6143 cycles, low 1 cycle of the CK21 clock	ECL, differential
NFP3100+, NFP3100- to NFP3111+, NFP3111	-8.0 kHz	high 4095 cycles, low 1 cycle of the CK31 clock	ECL differential
NFP61, NTFP61, FP61	8.0 kHz	high 2047 cycles, low 1 cycle of the CK61 clock	TTL
CK97E+, CK97E-, CK970+, CK970	-10.24 MHz	nominal 50%, worst case 40-60%	TTL
NFP97E+, NFP97E-, NFP970+, NFP970	-8.0 kHz	high 1279 cycles, low 1 cycle of the CK97 clock	TTL

The phase relationship of card clocks and channel counters appears in the following figure.

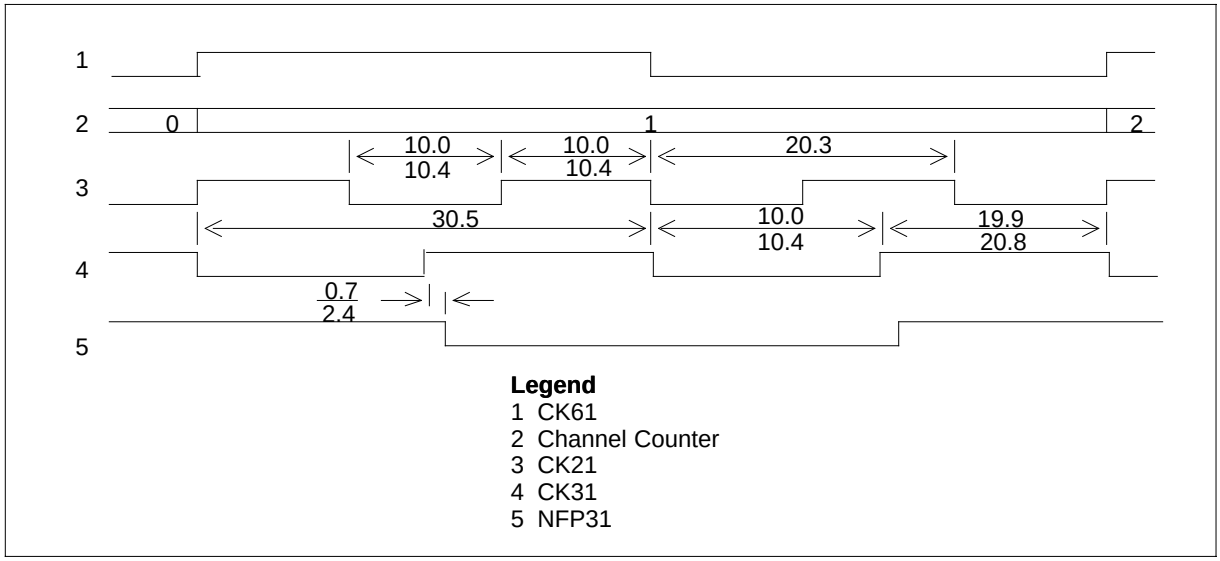
NT9X36BA (continued)

NT9X36BA phase relationship of card clocks and channel counter



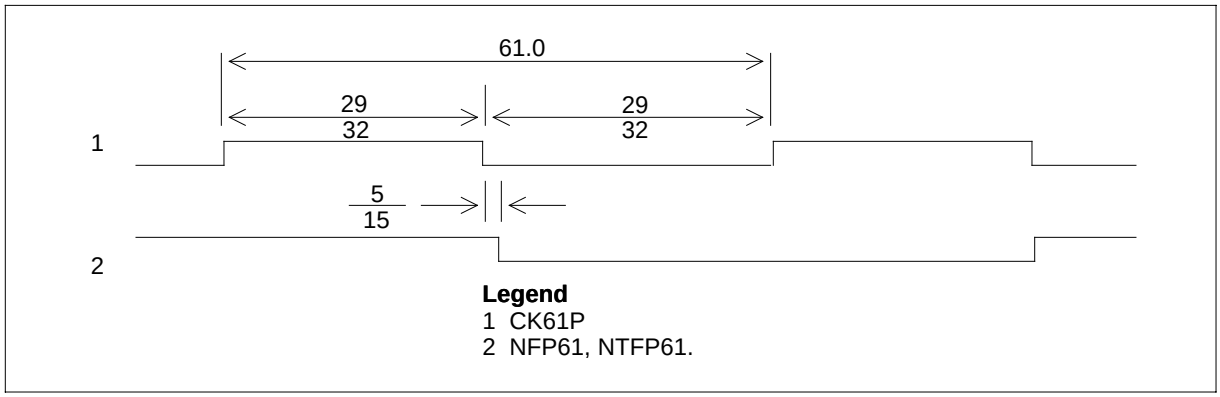
The crosspoint card clocks and frame pulse timing appear in the following figure.

NT9X36BA crosspoint card clocks and frame pulse timing



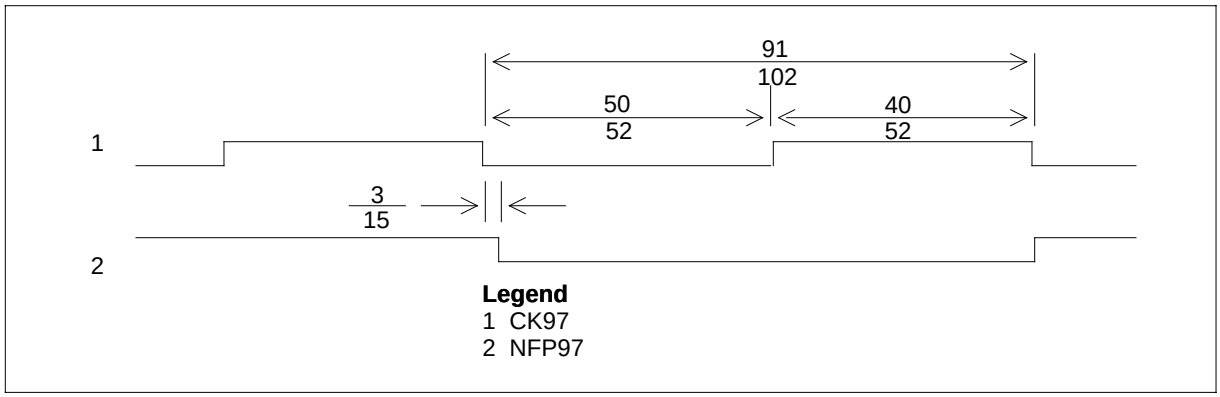
The crosspoint card clocks and frame pulse timing for paddle board clocks appear in the following figure.

NT9X36BA paddle board crosspoint card clocks and frame pulse timing



The DS30 clock and frame pulse timing appears in the following figure.

NT9X36BA DS30 clock and frame pulse timing



Technical data

Power requirements

The supply voltage required for NT9X36BA is +5.0 V, ±5%.

The power requirements for the NT9X36BA are 20 W and 3.8 A on -5.2 V, and 25 W and 5.0 A on +5.0 V.

NT9X40BA

Product description

The NT9X40BA is an enhanced network (ENET+) quad fiber interface paddle board. The NT9X40BA receives, transmits and repeats four DS512 fiber links. The NT9X40BA performs all the conversion necessary to go from the DS512 fiber serial format to a parallel bus (P bus) type interface with the crosspoint card (XPT). The NT9X40BA is also the DS512 interface to the message switch.

Functional description

The NT9X40BA is an ENET+ quad fiber interface paddle board. The NT9X40BA receives, transmits and repeat four DS512 fiber links.

Functional blocks

The NT9X40BA contains the five functional blocks:

- electro-optical receiver
- electro-optical transmitter
- QFLIC block
- DTRC block
- Processor bus (P-bus) interface

Electro-optical receiver

The electro-optical receiver converts the incoming light on the DS512 fiber link to differential ECL signals. The electro-optical receiver converts the ECL signals to signal ended TTL signals. The electro-optical receiver transmits the TTl signals to the QFLIC. Specification NPS25273-02 has additional details on this receiver. The receiver is optically compatible with the current DS512 receiver, NT5L76CC.

Electro-optical transmitter

This block converts the incoming electrical signal to light for transmission on the DS512 fiber link. Specification NPS25273-01 has full detail on this transmitter. The transmitter is optically compatible with the current DS512 transmitter, NT5L77CC.

QFLIC block

This block acts as the interface between the optical fiber modules and the DTRC. The QFLIC interfaces to four DS512 signals in both transmit and receive directions. In the receive direction, the QFLIC receives the electrical signal from the receive fiber module. The QFLIC recovers a clock digitally. The QFLIC uses the recovered clock to convert the data to parallel format. The QFLIC sends the data to the DTRC. In the transmit direction, the QFLIC

receives parallel data from the DTRC. The QFLIC serializes the data and sends the data to the transmit fiber module.

DTRC block

After the QFLIC processes the data, the four DTRCs interface to both the transmit and receive direction of a DS512 link.

Processor-bus interface

The P-bus is an asynchronous bus. The P-bus allows the shelf processor (NT9X13) to access the QFLIC and DTRC chips and the ID PROM on the card.

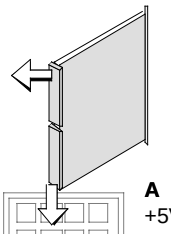
Signaling

Pin numbers

The pin numbers for the NT9X40BA appear in the following figure.

NT9X40BA (continued)

NT9X40BA pin numbers



	A	B	C	D
1				
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14				
15				
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20				
21				
22				
23				
24				
25				
26	GND	RDAT1	RDAT0	DATA24
27	+5V	RDAT3	RDAT2	DATA25
28	+5V	RDAT5	RDAT4	DATA26
29	GND	RDAT7	RDAT6	DATA27
30	+5V	RDAT9	RDAT8	DATA28
31	+5V	WBUS1	WBUS0	DATA29
32	GND	WBUS3	WBUS2	DATA30
33	–5.2V	WBUS5	WBUS4	DATA31
34	–5.2V	WBUS7	WBUS6	NSEL0
35	–5.2V	WBUS9	WBUS8	NSEL1
36	–5.2V	RNW		NSEL2
37	GND	DAS–		NSEL3
38	GND	NSPE	NMPE	NSTB0
39	+5V	ADDR1	ADDR0	NSTB1
40	+5V	ADDR3	ADDR2	NSTB2
41	+5V	ADDR5	ADDR4	NSTB3
42	+5V	ADDR7	ADDR6	NRFP0
43	GND	ADDR9	ADDR8	NRFP2
44	+5V			NCSEN
45	+5V			

	A	B	C	D
46	+5V			CK21P+
47	+5V			CK21P–
48	GND			NFP21P+
49	+5V			NFP21P–
50	+5V			CK61
51	+5V			NFP61
52	+5V			
53	GND			MODE
54				
55				
56				
57				
58				
59	GND	GND	GND	
60				
61				
62				
63				
64				
65	GND	GND	GND	GND
66				
67				
68				
69				
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Technical data

Environmental conditions

The following table describes the ambient conditions of the NT9X40BA.

NT9X40BA ambient conditions

Condition	Operating range
Temperature	0 to 70*C
Relative humidity	20 to 95%

Power requirements

The standard power requirements for the NT9X40BA are 2.6 W from a -5.2V±5% supply and 6.9 W from a +5.0V±5% supply.

NT9X40BB

Product description

The NT9X40BB is an enhanced network (ENET+) quad fiber interface paddle board. The NT9X40BB receives, transmits and repeats four DS512 fiber links. The NT9X40BB performs all the conversion necessary to go from the DS512 fiber serial format to a parallel bus (P-bus) type interface. The NT9X40BB uses the crosspoint (XPT) card to perform conversion. The NT9X40BB is also the DS512 interface to the message switch.

Note: This hardware description is almost identical to the NT9X40BA. This description uses the latest version of the DS512 treatment receiver controller (DTRC).

Functional description

The NT9X40BB is an ENET+ quad fiber interface paddle board. The NT9X40BB receives, transmits and repeats four DS512 fiber links.

Functional blocks

The NT9X40BB has five functional blocks:

- electro-optical receiver
- electro-optical transmitter
- QFLIC block
- DTRC block
- Processor bus (P-bus) interface

Electro-optical receiver

The electro-optical receiver converts the incoming light on the DS512 fiber link to differential ECL signals. The electro-optical receiver converts the ECL signals to signal ended TTL signals. The electro-optical receiver transmits the TTL signals to the QFLIC. The specification NPS25273-02 has additional details on this receiver. The receiver is optically compatible with the current DS512 receiver, NT5L76CC.

Electro-optical transmitter

This block converts the incoming electrical signal to light for transmission on the DS512 fiber link. Specification NPS25273-01 has full details on this transmitter. The transmitter is optically compatible with the current DS512 transmitter, NT5L77CC.

QFLIC block

This block acts as the interface between the optical fiber modules and the DTRC. The QFLIC interfaces to four DS512 signals in both transmit and

receive directions. In the receive direction, the QFLIC receives the electrical signal from the receive fiber module. The QFLIC digitally recovers a clock. The QFLIC uses the recovered clock to convert the data to parallel format. The QFLIC sends the data to the DTRC. In the transmit direction, the QFLIC receives parallel data from the DTRC. The QFLIC serializes the data and sends the data to the transmit fiber module.

DTRC block

After the QFLIC processes the data, the four DTRCs interface to both the transmit and receive direction of a DS512 link.

Processor-bus interface

The P-bus is an asynchronous bus. The P-bus allows the shelf processor (NT9X13) to access the QFLIC and DTRC chips and the ID PROM on the card.

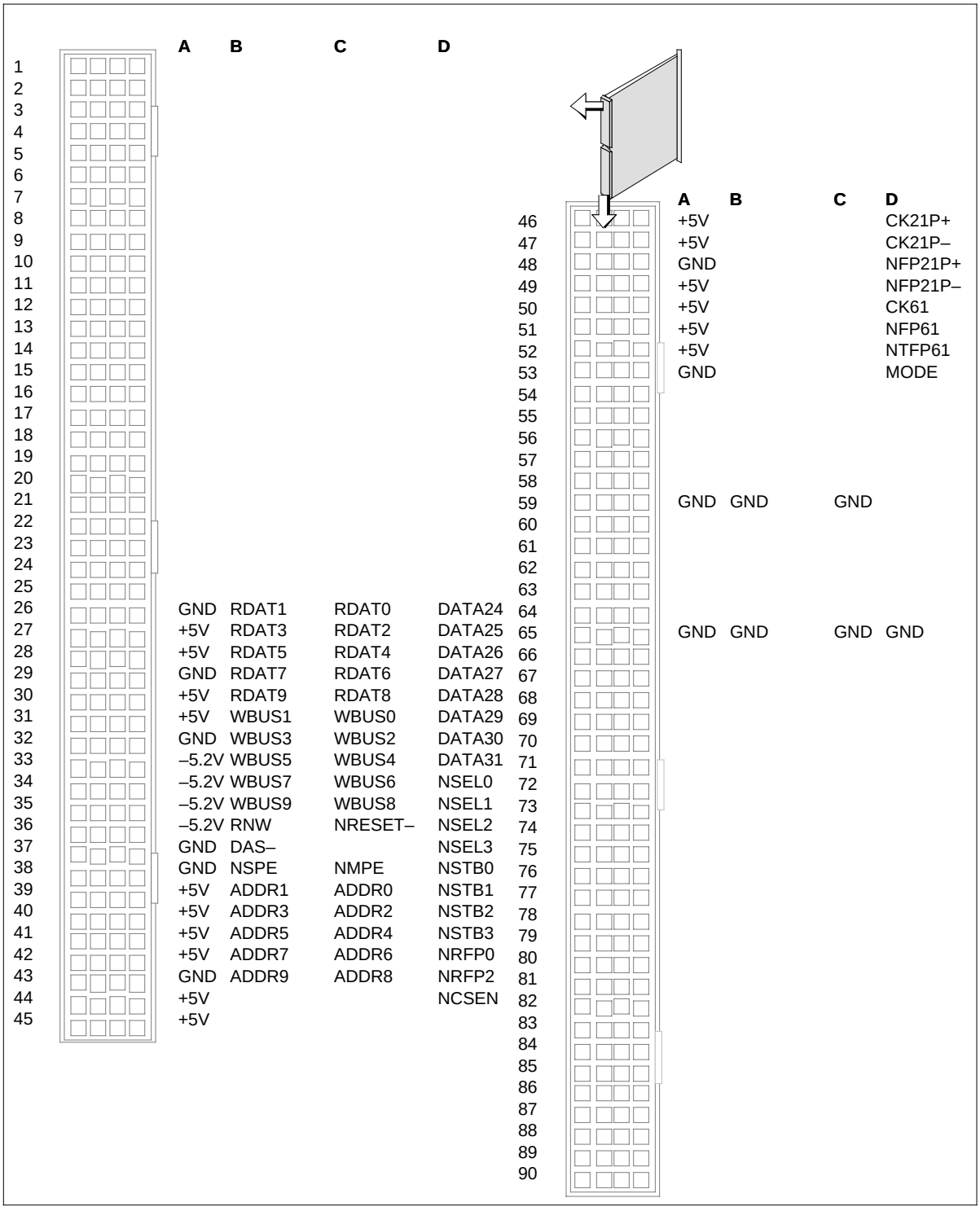
Signaling

Pin numbers

The pin numbers for the NT9X40BB appear in the following figure.

NT9X40BB (continued)

NT9X40BB pin numbers



Technical data

Environmental conditions

The following table describes the ambient conditions of the NT9X40BB.

NT9X40BB ambient conditions

Condition	Operating range
Temperature	0 to 70°C
Relative humidity	20 to 95%

Power requirements

The standard power requirements for the NT9X40BB are 6.9W from a -5.2V±5% supply and 2.6W from a +5.0V±5% supply.

NT9X41BA

Product description

The NT9X41BA 16-port DS30 paddle board links DS30 peripherals to the enhanced network through twisted-pair copper cables.

Functional description

The NT9X41BA provides DS30 links between the enhanced network and current DS30-based peripherals. The replaces the NT9X40BA when a DS30 link retrofit is necessary. The converts link 0 to the DS30 rate and format, in both the receive and transmit direction. The NT9X41BA cannot multiplex or demultiplex data for links 1, 2 and 3 from the backplane bus.

Functional blocks

The NT9X41BA has two functional blocks:

- bit rate converter
- DS30 interface circuits

Bit rate converter

The bit rate converter block converts the 10 bit parallel backplane data to serial format. The converter performs pulse code modulation (PCM) gain or loss through the digital pads. The bit rate changes in this block. The backplane provides a processor interface to allow the shelf processor to communicate with the bit rate converter.

DS30 interface circuitry

The W87 (DS30 interface chip) provides DS30 interface circuits for two bidirectional DS30 links. The NT5L67AA DS30 ceramic hybrid single inline package (SIP) provides dual bidirectional DS30 link termination. There are 8 W87s and 8 NT5L67AAs in the DS30 interface block to support the 16-port DS30 paddle board. The DS30 interface block also provides different timing and address decoding functions.

Signaling

Pin numbers

The DS30 port signals for the transmit and receive connectors J1 and J2 appear in the following tables.

NT9X41BA DS30 port transmit signals for connector J1 (Sheet 1 of 2)

Pin	Name
1	TXP0
2	TXP1
3	TXP2
4	TXP3
5	TXP4
6	TXP5
7	TXP6
8	TXP7
9	TXP8
10	TXP9
11	TXP10
12	TXP11
13	TXP12
14	TXP13
15	TXP14
16	TXP15
20	TXN0
21	TXN1
22	TXN2
23	TXN3
24	TXN4

NT9X41BA (continued)

NT9X41BA DS30 port transmit signals for connector J1 (Sheet 2 of 2)

Pin	Name
25	TXN5
26	TXN6
27	TXN7
28	TXN8
29	TXN9
30	TXN10
31	TXN11
32	TXN12
33	TXN13
34	TXN14
35	TXN15

NT9X41BA DS30 port receive signals for connector J2 (Sheet 1 of 2)

Pin	Name
1	RXP0
2	RXP1
3	RXP2
4	RXP3
5	RXP4
6	RXP5
7	RXP6
8	RXP7
9	RXP8
10	RXP9
11	RXP10

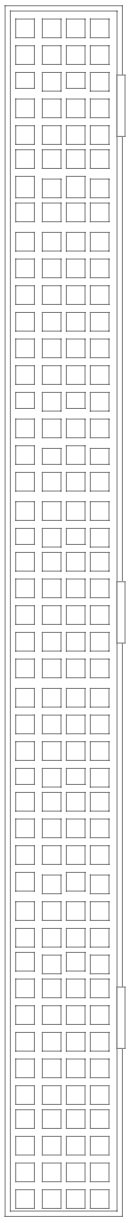
NT9X41BA DS30 port receive signals for connector J2 (Sheet 2 of 2)

Pin	Name
12	XP11
13	RXP12
14	RXP13
15	RXP14
16	RXN15
20	RXN0
21	RXN1
22	RXN2
23	RXN3
24	RXN4
25	RXN5
26	RXN6
27	RXN7
28	RXN8
29	RXN9
30	RXN10
31	RXN11
32	RXN12
33	RXN13
34	RXN14
35	RXN15

The pin numbers for connector P1 appear in the following figure.

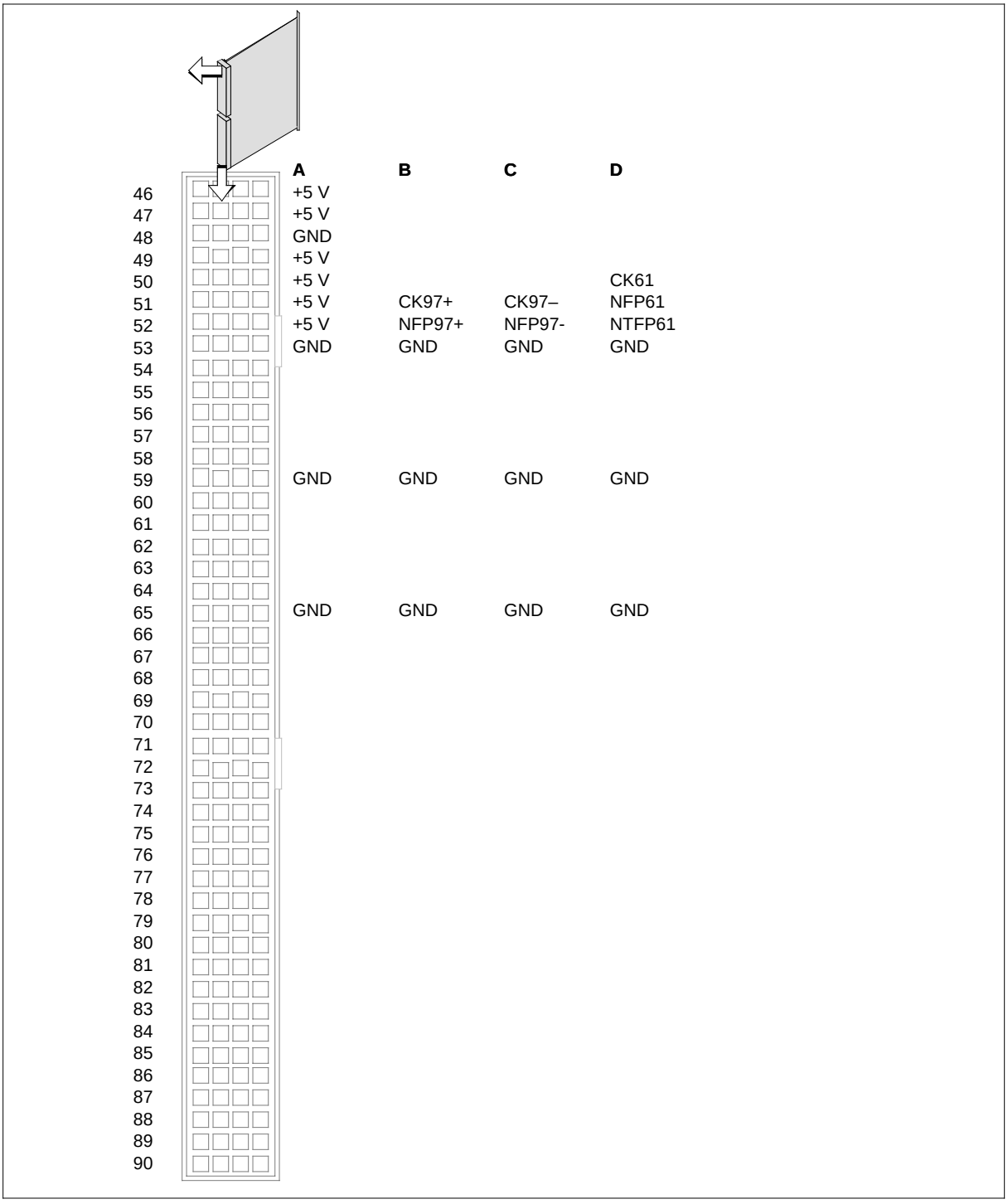
NT9X41BA (continued)

The NT9X41BA pin numbers (Part 1 of 2)



	A	B	C	D
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				
23				
24				
25				
26	GND	RDAT1	RDAT0	DAT24
27	+5V	RDAT3	RDAT2	DAT25
28	+5 V	RDAT5	RDAT4	DAT26
29	GND	RDAT7	RDAT6	DAT27
30	+5 V	RDAT9	RDAT8	DAT28
31	+5 V	WBUS1	WBUS0	DAT29
32	GND	WBUS3	WBUS2	DAT30
33		WBUS5	WBUS4	DAT31
34		WBUS7	WBUS6	
35		WBUS9	WBUS8	
36		RNW	RESET–	
37	GND	DAS32–		
38	GND	NSPE	NMPE	
39	+5 V	ADDR1	ADDR0	
40	+5 V	ADDR3	ADDR2	
41	+5 V	ADDR5	ADDR4	
42	+5 V			
43	GND	ADDR9		
44	+5 V			NCSEN
45	+5 V			

NT9X41BA pin numbers (Part 2 of 2)



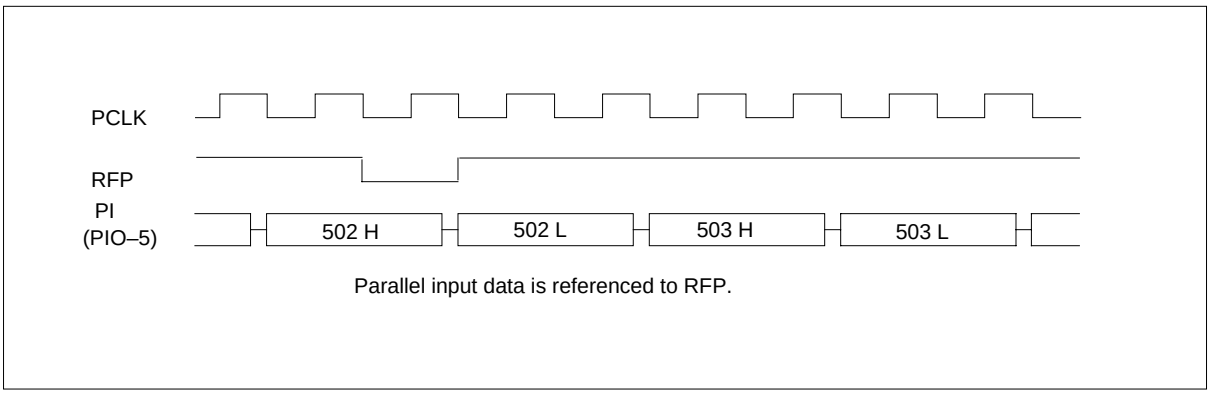
	A	B	C	D
46	+5 V			
47	+5 V			
48	GND			
49	+5 V			
50	+5 V			CK61
51	+5 V	CK97+	CK97–	NFP61
52	+5 V	NFP97+	NFP97-	NTFP61
53	GND	GND	GND	GND
54				
55				
56				
57				
58				
59	GND	GND	GND	GND
60				
61				
62				
63				
64				
65	GND	GND	GND	GND
66				
67				
68				
69				
70				
71				
72				
73				
74				
75				
76				
77				
78				
79				
80				
81				
82				
83				
84				
85				
86				
87				
88				
89				
90				

NT9X41BA (continued)

Timing

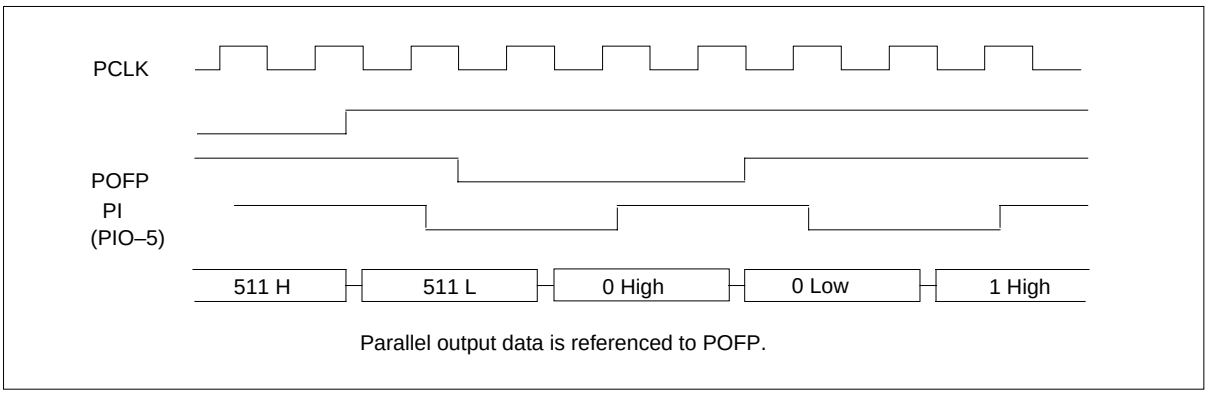
The parallel input port channel timing appears in the following figure.

NT9X41BA parallel input port channel timing



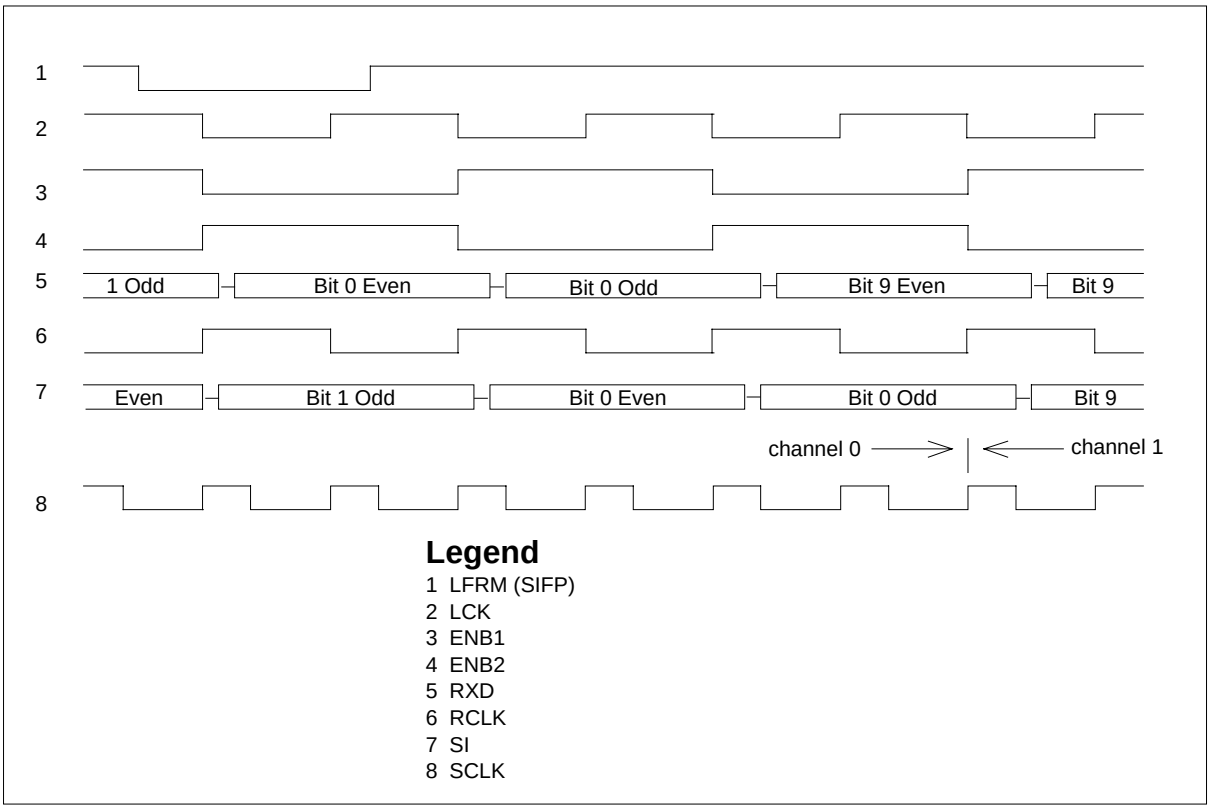
The parallel output port channel timing appears in the following figure.

NT9X41BA parallel output port channel timing



The serial input port channel timing appears in the following figure.

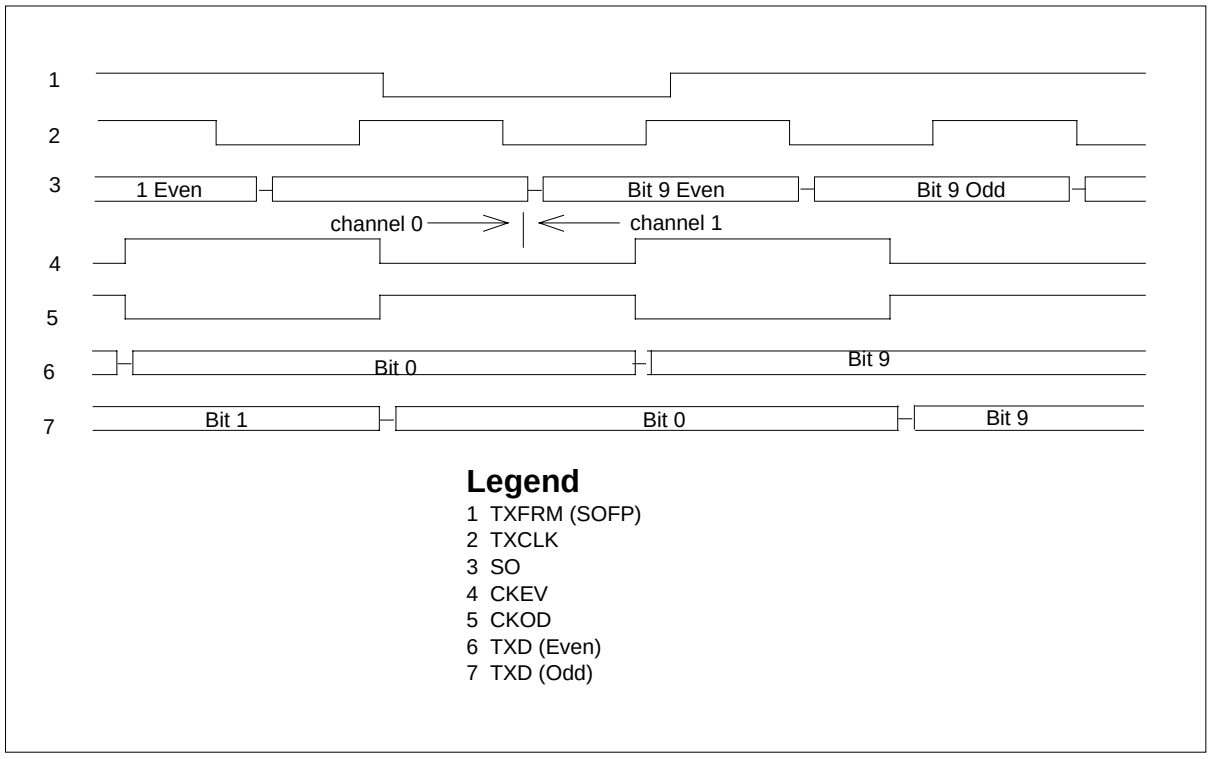
NT9X41BA serial input port channel timing



The serial output port channel timing appears in the following figure.

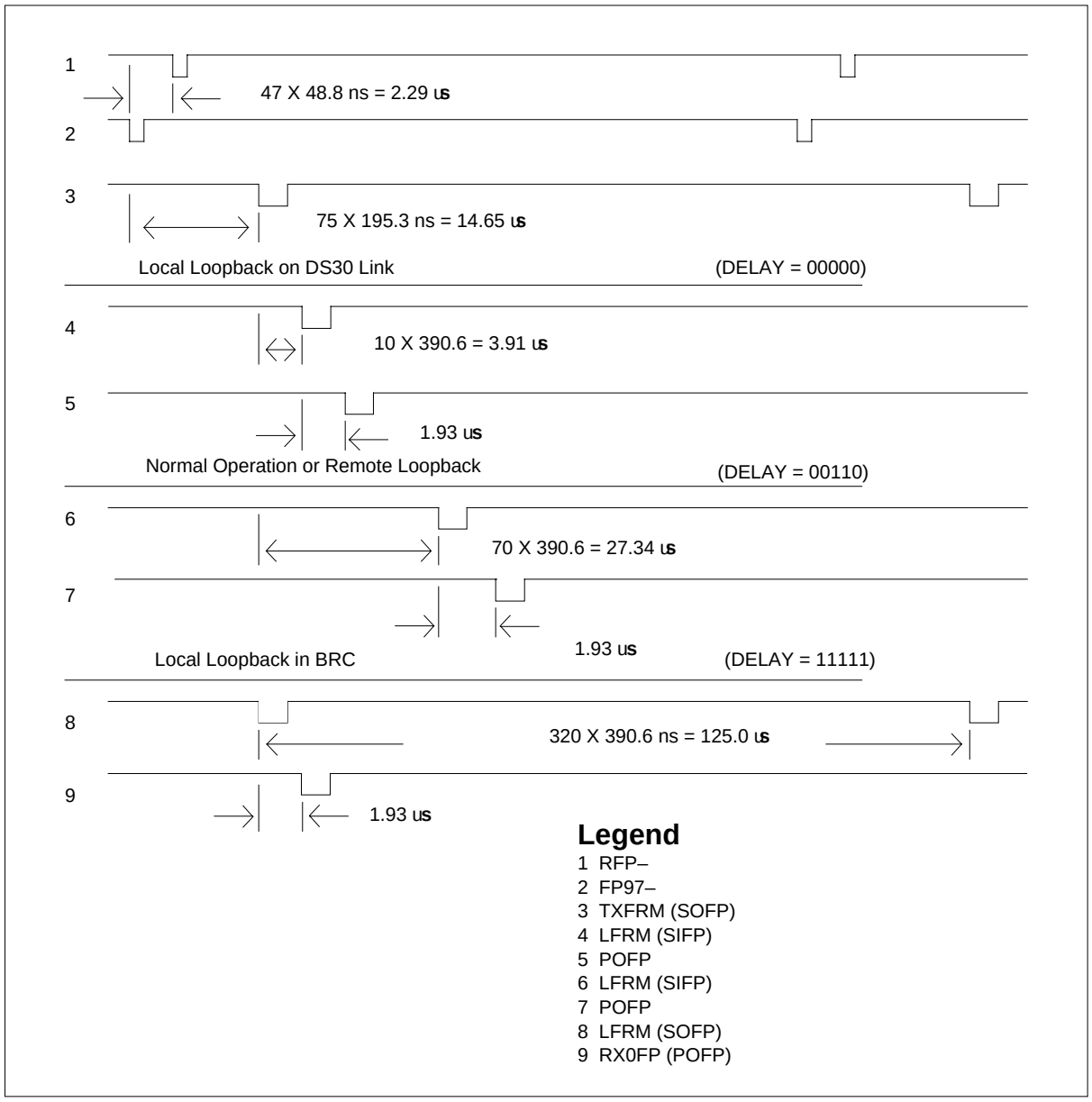
NT9X41BA (continued)

NT9X41BA serial output port channel timing



The frame pulse timing appears in the following figure.

NT9X41BA frame pulse timing



Technical data

Power requirements

The required supply voltage for NT9X41BA is +5.0 V±5%. The required power is 4.70 W.

NT9X41BA (end)

Drive Specifications

Drive specifications

Signal	Maximum logic low	Maximum logic high
RDAT0-9	2 mA	-2 mA
DATA24-31	48 mA	-15 mA

Load Specifications

Load specifications

Signal	Maximum logic low	Maximum logic high
ADDR00-05, ADDR09	-100 uA	20 uA DATA24-31, RNW
RESET, NSPE, NMPE	-250 uA	25 uA NCSEN, CK61
All other inputs	1 Mohms	

NT9X44AB

Product description

The NT9X44AB system load module II (SLM) is the software image storage and loading device for the DMS SuperNode computing module. The main function of the NT9X44AB is to boot the switch. The NT9X44AB provides the following features:

- emergency bootload of the computing module and message switch from disk or tape
- image dump to disk
- offline transfers from tape to disk or disk to tape

The NT9X44AB is an assembly that contains a controller card, a 5.25 in. Winchester disk, and a tape cartridge drive. The disk is a Maxtor XT-8760SH or Seagate ST4766N. The disk provides 600 Mbytes of storage. The tape cartridge drive is an Archive ST105 0.25 in. The tape cartridge drive uses DC6150 QIC–type cartridges. The DC6150 QIC–type cartridges provide a maximum of 150 Mbytes of storage.

To accommodate BRISC processors with 96 Mbyte memory, the tape cartridge drive can have the DC6250 cartridge. This DC6250 cartridge provides 250 Mbytes of storage.

The tape runs in streaming mode and not start–stop mode. Streaming mode minimizes gaps on the tape to provide higher storage density and increased transfer rate. The NT9X44A stores images on disk for transfer to tape. The NT9X44A transfers the images to tape offline to provide backup storage.

The disk drive connects to logic ground and not frame ground to prevent electrostatic discharge through the frame. The tape drive connects to frame ground to prevent logic disturbances from electrostatic discharge. Logic disturbances from electrostatic discharge can occur when insertion of a tape cartridge in the SLM occurs.

The faceplate of the SLM has a light–emitting diode (LED) that indicates the following three states:

- When the LED is on, the disk drive spins at operational speed.
- When the LED flashes, the disk drive spins up to operational speed or slows down to stop.
- When the LED is off, the disk drive does not run and the safe removal of the SLM from the shelf can occur.

NT9X44AB (continued)

Location

The NT9X44AB is in the bottom shelf of a DMS SuperNode frame. The NT9X44AB occupies eight card slots. The shelf normally contains the SLM0 and SLM1 SLM assemblies. The SLM0 occupies slot 8 and SLM1 occupies slot 23 in the SLM shelf of the DMS SuperNode.

The NT9X44AB weighs 9 kg (20 lbs) and has a folding carrying handle on top and two locking latches. The first locking latch is on the faceplate of the SLM. You must lift the first locking latch before you can open the locking levers on the SLM. The second locking latch is on top of the SLM. The second locking latch holds the SLM partly in the shelf. You can fold the carrying handle up or down without the danger of dropping the unit. When you insert the SLM in the shelf, the locking latch engages. You must press the locking latch before you can remove the SLM.

Functional description

The NT9X44AB SLM can store five or more image files. The NT9X44AB SLM stores one image file on tape and four or more on disk. The central processing units of the computing modules can load from the SLMs through the crossover bus. If power loss occurs to one SLM, the other SLM only loads the central processing unit linked directly to the other SLM. This action also occurs if NT9X12 port card is defective.

The disk can store customer billing data that is later copied to a data cartridge in the tape drive. A downstream billing processor processes the data. This function reduces the number of images that the NT9X44AB can store on the disk.

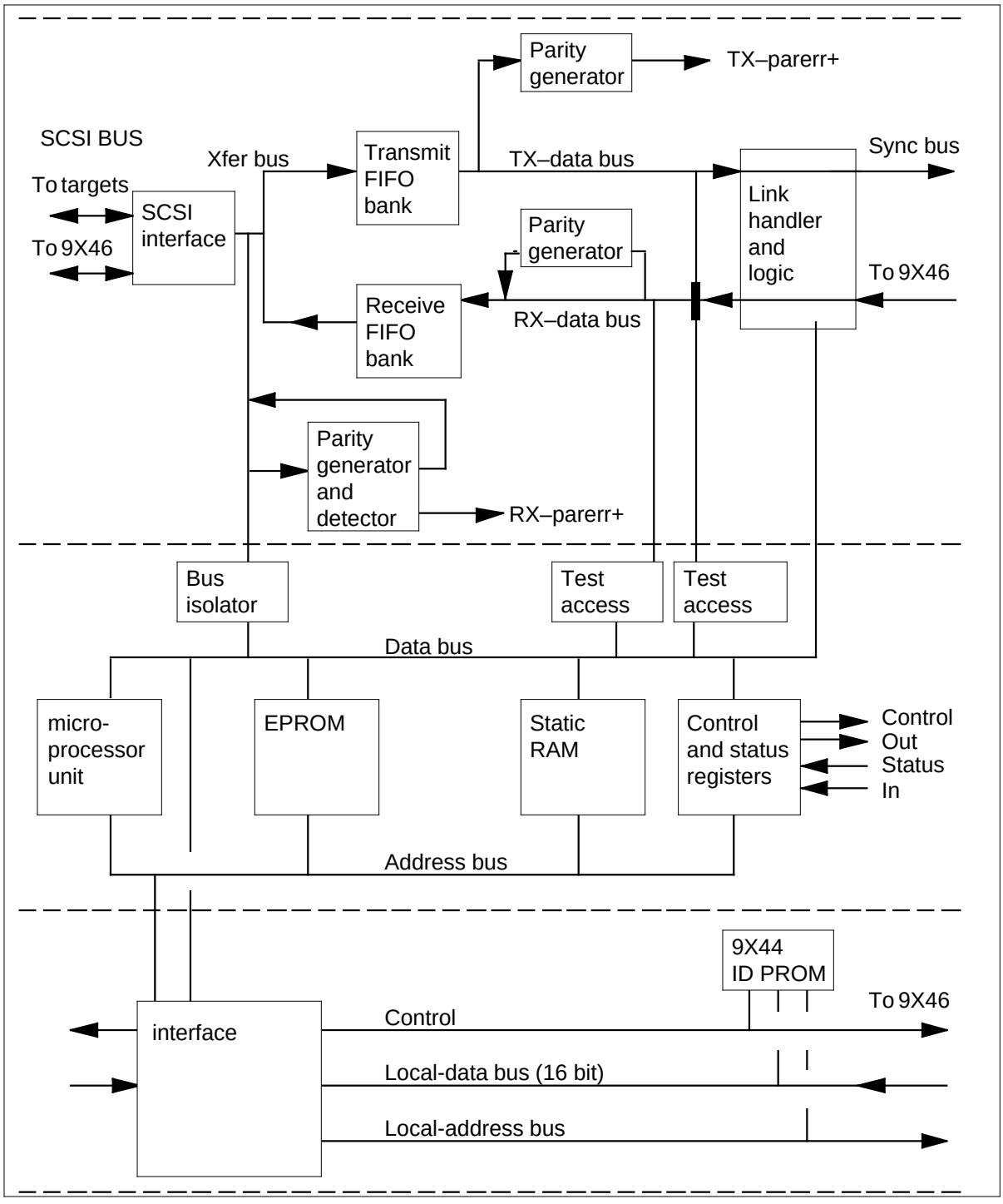
Functional blocks

The NT9X44AB has the following functional sections:

- top section
- middle section
- bottom section

The relationship of the functional sections appears in the following figure.

NT9X44AB functional blocks



NT9X44AB (continued)

Top section of figure

The top section represents the main data path between the CM port card and the peripheral storage devices. The CM post card is at the link handler end. The peripheral storage devices are at the SCSI end. The top section has the following main hardware entities:

- link handler and associated driving logic
- the SCSI interface and associated driving logic
- transmit and receive first–in–first–out (FIFO) banks
- parity generation and detection circuits

The link handler and associated driving logic section connects to the NT9X12 port card over a synchronous bus. The bus routes to the port card through an NT9X46AA parallel CM port interface paddle board. The CM port interface paddle board is behind the SLM. The bus connects through a twisted pair cable to an NT9X46AA paddle board. The NT9X46AA paddle board is behind the port card. A cyclic redundancy check (CRC) generator and detector in the link handler monitors the accuracy of data transmission over the link.

The SCSI interface and associated driving logic section connects to SCSI target devices. The target devices are data storage devices of the SLM. The SCSI interface and SCSI bus contain parity generation and detection hardware. This hardware monitors the accuracy of data transmission between the SCSI interface and targets of the SCSI interface.

The transmit and receive FIFO banks function as buffers for data transfers. The link handler section and the SCSI interface section can direct memory access (DMA) transfers of data between the buses and the FIFO banks. This capability allows a high data flow rate between the two buses.

Parity generation and detection circuits on FIFO banks monitor the accuracy of the data when the data resides in the FIFOs.

Middle section of figure

The middle section represents the controlling layer and test functions. The middle section has the following main hardware entities:

- microprocessor unit
- EPROM program memory
- static RAM
- card status and control registers

- bus isolator
- FIFO test access ports

The microprocessor unit uses a program in the EPROM to control the SLM card. The microprocessor unit uses the static RAM for data buffering functions. The card status and control registers control and monitor different card functions.

The bus isolator controls the interaction between the transfer bus and the data bus of the microprocessor unit. When DMA data transfers occur between the SCSI interface and an FIFO bank, the isolator keeps the two buses separate. Without this separation, the isolator gives the microprocessor unit access to the FIFO banks and the internal registers. The internal registers are in the SCSI interface. The microprocessor unit uses control and status registers to control the state of isolation.

The FIFO test access ports give the microprocessor unit access to the FIFO banks. The microprocessor units can access the FIFO banks from the end of the microprocessor unit that connects to the link handler. This design allows a test of the accuracy of the FIFOs without the use of the link handler. This design enables operating company personnel to perform special data control operations that can be necessary during controller operation.

Bottom section of figure

The bottom section represents the interface to the ID PROM and the interface to the system through the NT9X46AA paddle board. The controller card on the NT9X44AB interfaces directly to the NT9X46AA.

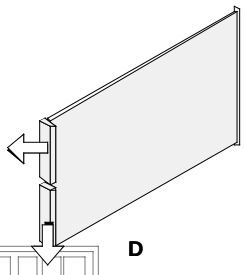
Signaling

Pin numbers

The pin numbers for the NT9X44AB appear in the following figure.

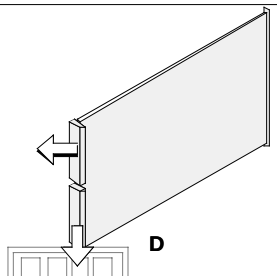
NT9X44AB (continued)

NT9X44AB pin numbers (Part 1 of 2)



	D	C	B	A
1			+12 V	GND
2			+12 V	GND
3			+12 V	GND
4			+12 V	GND
5			+12 V	GND
6			+12 V	GND
7			+12 V	GND
8			+12 V	GND
9				GND
10			12V–CONV–ON–	GND
11			SLU–RESET–	GND
12				GND
13				PENB–
14				R/W–
15	OOBIN0		CLK*1	PDTACK–
16			CLK*2	C244
17			SLU+5*–	PADDR0
18			CLK*4	PADDR1
19			CLK*5	PADDR2
20			CLK*6	PADDR3
21	OOBIN1		CLK*7	DREN–
22			CLK*8	PADDR4
23	RSTOUT–	BUSLOCK–		PADDR5
24				
25				
26				
27				
28	PWRT–			
29		DTACK–		HW4
30				
31				
32				SH0
33	DAS32–			SH1
34				–FP61
35		ADDR01	TYPE1	C61
36		ADDR02	HW0	+12
37		ADDR03	HW1	+12
38		ADDR04	HW2	+12
39		ADDR05	HW3	+12
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5
45		ADDR11	MR–/W+	+5

NT9X44AB pin numbers (Part 2 of 2)



	D	C	B	A
46		ADDR12		+5
47		ADDR13	MSEL–	+5
48		ADDR14		+5
49		ADDR15	M–DTK–	+5
50	DATA16	ADDR16		+5
51	DATA17	ADDR17		+5
52	DATA18	ADDR18		+5
53	DATA19	ADDR19		+5
54	DATA20	ADDR20	MA00	+5
55	DATA21	ADDR21	MA01	+5
56	DATA22	ADDR22		TYPE0
57	DATA23	ADDR23	–D0	LTVL
58	DATA24	ADDR24	–D1	LRVL
59	DATA25	ADDR25	–D2	STDA0
60	DATA26	ADDR26	–D3	STDA1
61	DATA27	ADDR27	–D4	STDA2
62	DATA28	ADDR28	–D5	STDA3
63	DATA29	ADDR29	–D6	STDA4
64	DATA30	ADDR30	–D7	STDA5
65	DATA31	ADDR31	–DP	STDA6
66		MA02	–REQ	STDA7
67		MA03	–ACK	
68		MA04	–BSY	
69		MA05	–C/D	SRDA0
70		MA06	–I/O	SRDA1
71		MA07	–MSG	SRDA2
72		MA08	–ATN	SRDA3
73		MA09	–SEL	SRDA4
74		MA10	–RST	SRDA5
75		MA11		SRDA6
76		MA12		SRDA7
77		MA13		
78		MA14		
79			PDATA0	GND
80			PDATA1	GND
81		ENA–MON–	PDATA2	GND
82	12V-CONV-ON	8MHZ	PDATA3	GND
83	MD0	2MSEC	PDATA4	GND
84	MD1	MDS–	PDATA5	GND
85	MD2	M–INT–	PDATA6	GND
86	MD3		PDATA7	GND
87	MD4		PDATA8	GND
88	MD5		PDATA9	GND
89	MD6		PDATA10	GND
90	MD7		PDATA11	GND

NT9X44AB (end)

Technical data

Power requirements

The power requirements for the NT9X44AB appear in the following table.

Power requirements of the NT9X44AB

	Standard	Maximum	Units
Current	4	6.0	amperes
Voltage	5	æ	volts
	12	æ	volts

NT9X44AC

Product description

The NT9X44AC system load module 1A (SLM) is the software image storage and loading device for the DMS SuperNode SE computing module. The main function of the NT9X44AC is to boot the switch. The NT9X44AC provides the following features:

- emergency bootload of the computing module and message switch from disk or tape
- image dump to disk
- offline transfers from tape to disk, or disk to tape

The NT9X44AC is an assembly that contains a controller card, a 5.25 in. Winchester disk and a tape cartridge drive. The disk provides 300 Mbytes of storage. The tape cartridge drive is an Archive ST105 0.25 in. The tape cartridge drive uses DC6150 or DC6250 QIC-type cartridges. The DC6150 cartridges provide 150 Mbytes of storage. The DC6250 QIC-type cartridges provide 250 Mbytes of storage.

The tape runs in streaming mode and not start-stop mode. Streaming mode minimizes gaps on the tape to provide higher storage density and increased transfer rate. The NT9X44AC stores images on disk to transfer to tape. The NT9X44AC transfers the images to tape offline to provide backup storage.

The disk drive connects to logic ground and not frame ground to prevent electrostatic discharge through the frame. The tape drive connects to frame ground to prevent logic damage from electrostatic discharge. Logic damage from electrostatic discharge can occur when insertion of a tape cartridge in the SLM occurs.

The faceplate of the SLM has a light-emitting diode (LED) to indicate the following three states:

- When the LED is on, the disk drive spins at operational speed.
- When the LED flashes, the disk drive spin up to operational speed or slowing down to stop.
- When the LED is off, the disk drive does not run and you can safely remove the SLM from the shelf.

Location

The NT9X44AC is in the bottom shelf of a DMS SuperNode SE frame. The NT9X44AC occupies five card slots. The shelf normally contains the two SLM assemblies, SLM0 and SLM1. The SLM0 occupies slot 7 and SLM1 occupies slot 28 in the CPU shelf of the DMS SuperNodeSE.

NT9X44AC (continued)

The NT9X44AC weighs 6 kg (14 lb) and has a folding carrying handle on top and two locking latches. The first locking latch is on the faceplate of the SLM. You must lift the first latch before you open the locking levers on the SLM. The second locking latch is on top of the SLM. The second latch holds the SLM partly in the shelf. You can fold the carrying handle of the second latch up or down without the danger of dropping the unit. When you insert the SLM in the shelf, the locking latch engages. You must press the locking latch before you can remove the SLM.

Functional description

The NT9X44AC SLM can store two or more image files. The NT9X44AC can store one image file on tape and one or more image file on disk. The central processing units of the computing module can be loaded from SLMs through the crossover bus. When one plane of the shelf loses power, the other SLM loads only the central processing unit linked directly to that SLM. This action also occurs if the NT9X12 port card is defective.

The disk can also store customer billing data that is later copied to a data cartridge in the tape drive. A downstream billing processor processes the data. This function reduces the number of images that the NT9X44AC can store on the disk.

The size of the software load of the central office determines the actual number of image files stored on the disk.

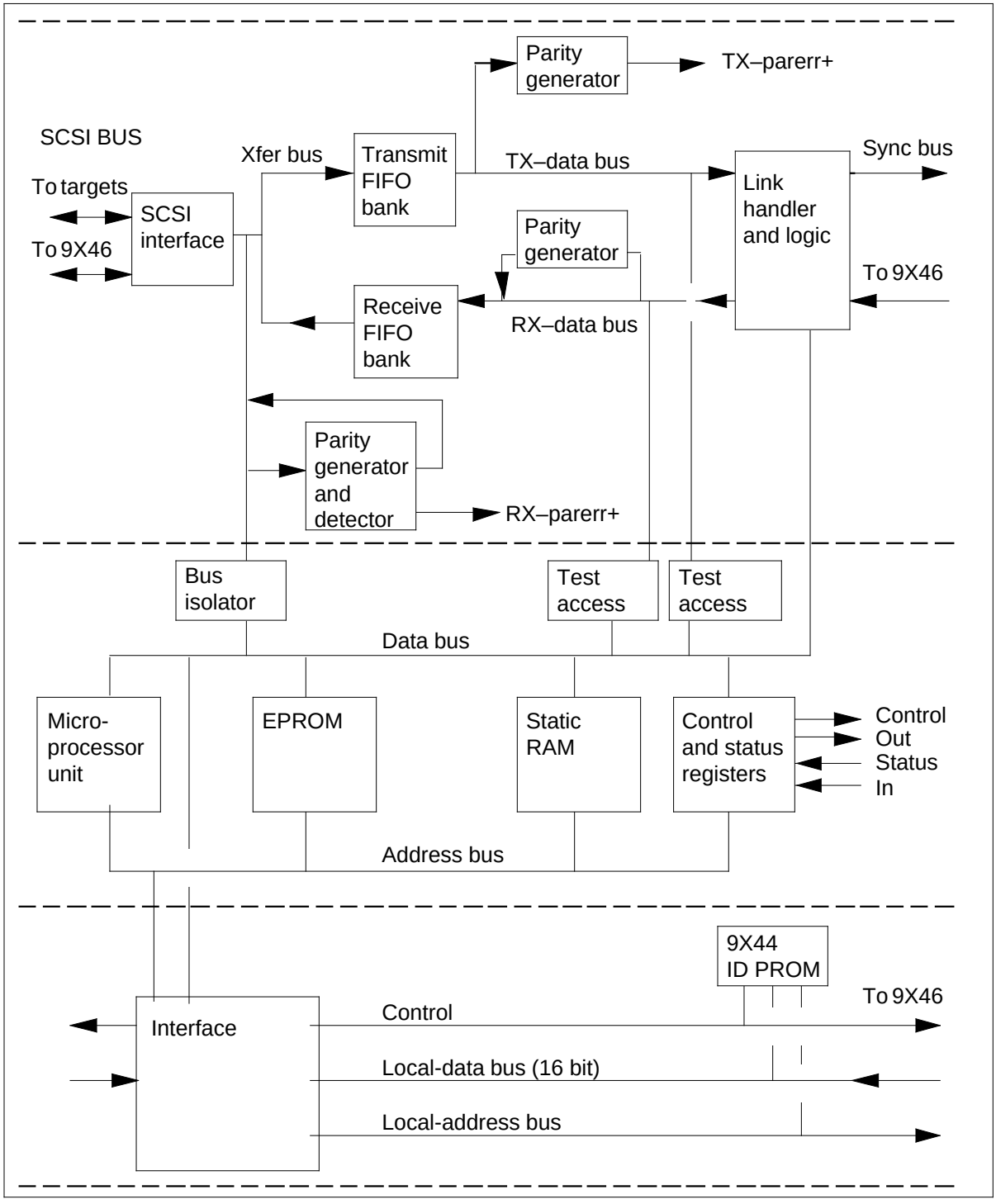
Functional blocks

The NT9X44AC has the following functional sections:

- top section
- middle section
- bottom section

The relationship for the functional sections appears in the following figure.

NT9X44AC functional blocks



NT9X44AC (continued)

Top section of figure

The top section represents the main data path between the CM port card and the peripheral storage devices. The CM port card is at the link handler end and the peripheral devices are at the SCSI end. The top section has the following main hardware entities:

- link handler and associated driving logic
- SCSI interface and associated driving logic
- transmit and receive first-in-first-out (FIFO) banks
- parity generating and detection circuits

The link handler and associated driving logic section connects to the NT9X12 port card over a synchronous bus. The bus routes to the port card through an NT9X46AA parallel CM port interface paddle board. The NT9X46AA paddle board is behind the SLM. The bus connects through a twisted pair cable to an NT9X46AA paddle board. The NT9X46AA paddle board is behind the port card. A cyclic redundancy check (CRC) generator and detector in the link handler monitors the accuracy of data transmission over the link.

The SCSI interface and associated driving logic section connects to SCSI target devices. The target devices are data storage devices of the SLM. The SCSI interface and SCSI bus contain parity generation and detection hardware. The parity generation and detection hardware monitors accuracy of data transmission between the SCSI interface and the targets of the SCSI.

The transmit and receive FIFO banks function as buffers for data transfers. The link handler section and the SCSI interface section can direct memory access (DMA) transfers of data between the buses and the FIFO banks. This capability allows a high data flow rate between the two buses.

Parity generation and detection circuits on FIFO banks monitor the accuracy of the data when the data resides in the FIFOs.

Middle section of figure

The middle section represents the controlling layer and test functions. The middle section has the following main hardware entities:

- microprocessor unit
- EPROM program memory
- static RAM
- card status and control registers

- bus isolator
- FIFO test access ports

The microprocessor unit uses a program in the EPROM to control the SLM. The microprocessor unit uses the static RAM for data buffering functions. The card status and control registers control and monitor different card functions.

The bus isolator controls the interaction between the transfer bus and the data bus of the microprocessor unit. When direct memory access data transfers occur between the SCSI interface and an FIFO bank, the isolator keeps the two buses separate. Without this separation, the isolator gives the microprocessor unit access to the FIFO banks and the internal registers. The internal registers are in the SCSI interface. The microprocessor unit uses control and status registers to control the state of isolation.

The FIFO test access ports provide the microprocessor unit access to the FIFO banks. The microprocessor unit accesses the FIFO banks from the end of the microprocessor unit that connects to the link handler. This configuration allows tests of the accuracy of the FIFOs without the use of the link handler. This configuration allows operating company personnel to perform special data control operations during controller operation.

Bottom section of figure

The bottom section represents the interface to the ID PROM and the interface to the system through the NT9X46AA paddle board. The controller card on the NT9X44AC interfaces directly to the NT9X46AA.

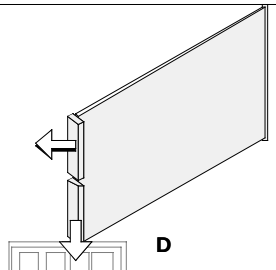
Signaling

Pin numbers

The pin numbers for the NT9X44AC appear in the following figure.

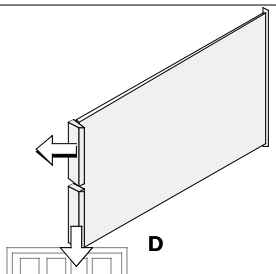
NT9X44AC (continued)

NT9X44AC pin numbers (Part 1 of 2)



	D	C	B	A
1			+12 V	GND
2			+12 V	GND
3			+12 V	GND
4			+12 V	GND
5			+12 V	GND
6			+12 V	GND
7			+12 V	GND
8			+12 V	GND
9				GND
10			12V–CONV–ON–	GND
11			SLU–RESET–	GND
12				GND
13				PENB–
14				R/W–
15	OOBIN0		CLK*1	PDTACK–
16			CLK*2	C244
17			SLU+5*–	PADDR0
18			CLK*4	PADDR1
19			CLK*5	PADDR2
20			CLK*6	PADDR3
21	OOBIN1		CLK*7	DREN–
22			CLK*8	PADDR4
23	RSTOUT–	BUSLOCK–		PADDR5
24				
25				
26				
27				
28	PWRT–			
29		DTACK–		HW4
30				
31				
32				SH0
33	DAS32–			SH1
34				–FP61
35		ADDR01	TYPE1	C61
36		ADDR02	HW0	+12
37		ADDR03	HW1	+12
38		ADDR04	HW2	+12
39		ADDR05	HW3	+12
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5
45		ADDR11	MR–/W+	+5

NT9X44AC pin numbers (Part 2 of 2)



	D	C	B	A
46		ADDR12		+5
47		ADDR13	MSEL–	+5
48		ADDR14		+5
49		ADDR15	M–DTK–	+5
50	DATA16	ADDR16		+5
51	DATA17	ADDR17		+5
52	DATA18	ADDR18		+5
53	DATA19	ADDR19		+5
54	DATA20	ADDR20	MA00	+5
55	DATA21	ADDR21	MA01	+5
56	DATA22	ADDR22		TYPE0
57	DATA23	ADDR23	–D0	LTVL
58	DATA24	ADDR24	–D1	LRVL
59	DATA25	ADDR25	–D2	STDA0
60	DATA26	ADDR26	–D3	STDA1
61	DATA27	ADDR27	–D4	STDA2
62	DATA28	ADDR28	–D5	STDA3
63	DATA29	ADDR29	–D6	STDA4
64	DATA30	ADDR30	–D7	STDA5
65	DATA31	ADDR31	–DP	STDA6
66		MA02	–REQ	STDA7
67		MA03	–ACK	
68		MA04	–BSY	
69		MA05	–C/D	SRDA0
70		MA06	–I/O	SRDA1
71		MA07	–MSG	SRDA2
72		MA08	–ATN	SRDA3
73		MA09	–SEL	SRDA4
74		MA10	–RST	SRDA5
75		MA11		SRDA6
76		MA12		SRDA7
77		MA13		
78		MA14		
79			PDATA0	GND
80			PDATA1	GND
81		ENA–MON–	PDATA2	GND
82		8MHZ	PDATA3	GND
83	MD0	2MSEC	PDATA4	GND
84	MD1	MDS–	PDATA5	GND
85	MD2	M–INT–	PDATA6	GND
86	MD3		PDATA7	GND
87	MD4		PDATA8	GND
88	MD5		PDATA9	GND
89	MD6		PDATA10	GND
90	MD7		PDATA11	GND

NT9X44AC (end)

Technical data

Power requirements

The power requirements for the NT9X44AC appear in the following table.

Power requirements	
Standard voltage	5 V, 12 V
Standard current	4 A, (6 A maximum)

NT9X44AD

Product description

The NT9X44AD system load module 3 (SLM 3) is the software image storage and loading device for the DMS SuperNode SE computing module. The main function of the NT9X44AD is to boot the switch. The NT9X44AD provides the following features:

- emergency bootload of the computing module and message switch from disk or tape.
- image dump to disk or tape.
- load mate inactive CPU (while active CPU is call processing).
- offline transfers from tape to disk, or disk to tape.

The NT9X44AD is an assembly that consists of a controller card, a 3.5 in disk drive, and a tape cartridge drive. The disk provides greater than 1 Gbyte of storage. The tape cartridge drive is the quarter inch cartridge (QIC) unit. The tape cartridge drive has a minimum capacity of 500 Mbytes.

The tape runs in streaming mode. The tape does not run in start–stop mode. The streaming mode minimizes gaps on the tape, which provides higher storage density and increases transfer rate. Disks store images before the transfer of the images to tape offline. This process provides backup storage.

The disk drive connects to logic ground. The disk drive does not connect to frame ground. The connection to logic ground prevents electrostatic discharge through the frame. The tape drive connects to frame ground to prevent logic interruptions from electrostatic discharge when you insert a tape cartridge in the SLM.

The controller card is the NT9X4421. The controller card consists of the following components:

- the DS512 and the SCSI interfaces.
- two kByte FIFO memories to buffer data in each direction.
- a 68008 microprocessor.

The microprocessor controls the messages between the DS512 and the SCSI interfaces. The microprocessor controls diagnostics and error handling. Parity is present from the SCSI peripherals to the SCSI ASIC, and through the first in, first out (FIFO) memories to the Link Handler ASIC. This parity protects data. The performance of the SLM 3 appears in the following section:

NT9X44AD (continued)

Transfer rate

- Disk—50 kBytes/sec (2–kByte FIFO, Interrupt I/O)
- Tape—100 kBytes/sec (copy command, there is no FIFO limit)

Minimum capacity

- Disk—1 Gbyte
- Tape—150 Mbytes (or 250 Mbytes with extended tape)

The faceplate of the SLM has a light–emitting diode (LED) to indicate the following three states:

- When the LED is on, the disk drive spins at operational speed.
- When the LED is flashing, the disk drive spins towards operational speed or slows down to stop.
- When the LED is off, the disk drive is stopped and you can remove the SLM from the shelf safely.

Location

The bottom shelf of a DMS SuperNode SE frame contains the NT9X44AD. The NT9X44AD occupies five card slots. The shelf normally contains two SLM assemblies. The SLM0 occupies slot 7 and SLM1 occupies slot 28 in the CPU shelf of the DMS SuperNodeSE. Each SLM 3 installed requires three filler packs. These filler packs are installed in card slots 13, 14, 15, 29, 30, and 31.

The NT9X44AD weighs 6 kg (14 lb). The NT9X44AD has a handle on top. This handle folds, and you can use the handle to carry the NT9X44AD. The NT9X44AD has two locking latches. The first locking latch is on the faceplate of the SLM. You must lift the latch before you can open the locking levers on the SLM. The second locking latch is on top of the SLM. This latch holds the SLM partially in the shelf. This position allows the carrying handle to fold up or down without the danger of dropping the unit. When you insert the SLM in the shelf, the locking latch automatically engages. You must press the locking latch before you can remove the SLM.

Functional description

The NT9X44AD SLM can store two or more image files. The NT9X44AD stores one file on tape, and one or more files on disk. Each central processing unit of the computing module can be loaded from any SLM through the crossover bus. One plane of the shelf can lose power, and the NT9X12 port card can be defective. If one of these conditions is present, the SLM that

remains can load only one central processing unit (CPU). This CPU is the CPU that links directly to the SLM on the same plane.

The disk can store customer billing data that is later copied to a data cartridge in the tape drive. A downstream billing processor processes this data. The use of the disk for this function reduces the number of images that the disk can store.

The disk can store a number of image files. This number depends on the size of the software load of the central office.

The SLM 12–V control function only allows the SLM to start the converter when this action is necessary. To turn on the 12–V power converter, you must turn the ON–OFF switch ON and activate the SLM control. The power converter turns OFF if you deactivate the SLM control and turn the switch OFF. Software controls an interlock. This interlock prevents power–down if the CPU is active.

Functional blocks

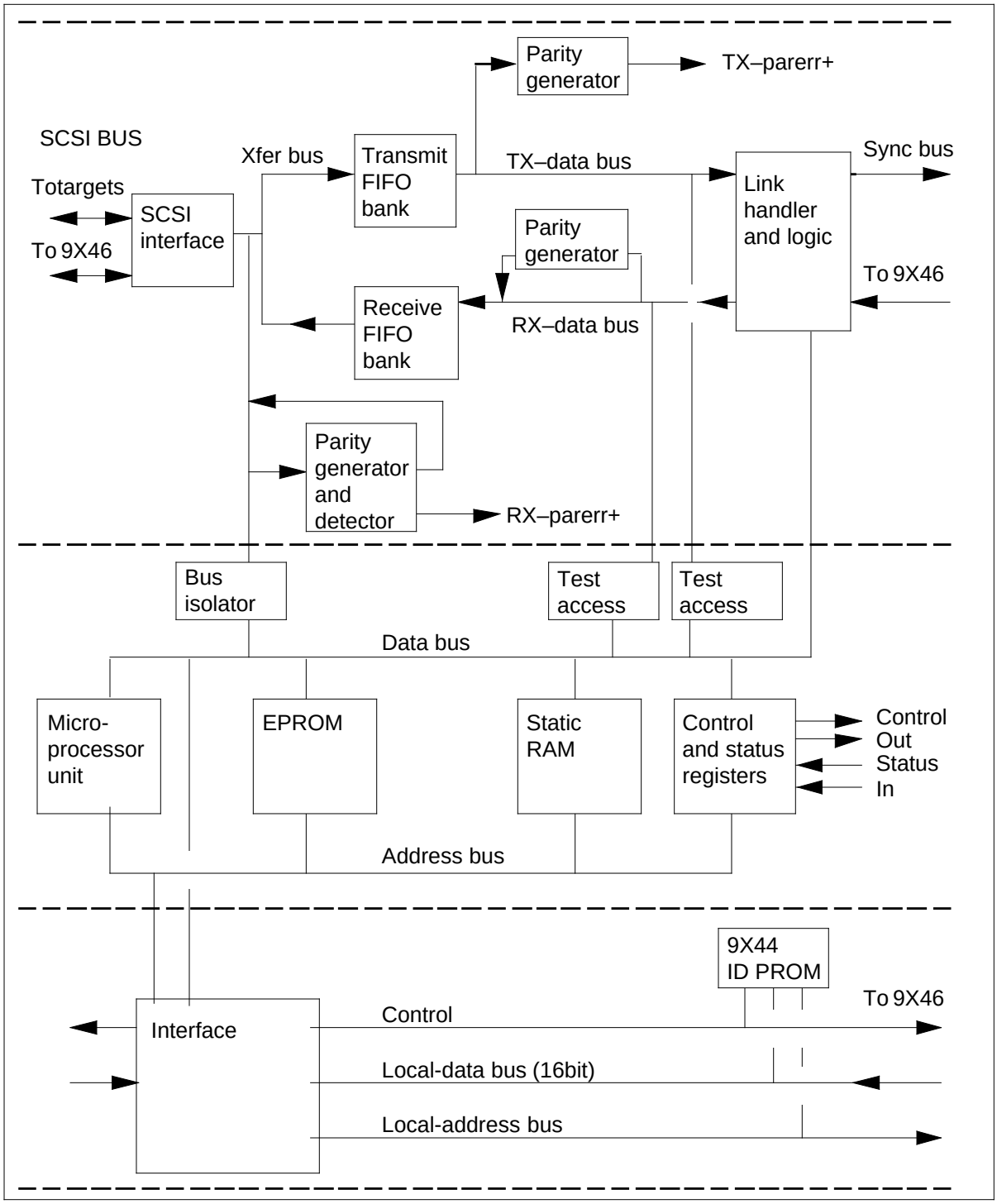
The NT9X44AD contains the following functional sections:

- top section
- middle section
- bottom section

The relationship between the functional sections appears in the following figure.

NT9X44AD (continued)

NT9X44AD functional blocks



Top section of figure

The top section of the figure represents the main data path between two ends. This path is between the CM port card (link handler end) and the peripheral storage devices (SCSI end). The top section has the following main hardware entities:

- link handler and associated driving logic
- SCSI interface and associated driving logic
- transmit and receive first in, first out (FIFO) banks
- detection circuits and circuits that generate parity

The link handler and associated driving logic section connects to the NT9X12 port card over a synchronous bus. The bus routes to the port card through an NT9X46AA parallel CM port interface paddle board. This paddle board is behind the SLM. The bus connects through a twisted pair cable to an NT9X46AA paddle board that is behind the port card. A cyclic redundancy check (CRC) generator and detector in the link handler monitors the integrity of data transmission over the link.

The SCSI interface and associated driving logic section connects to SCSI target devices. The SCSI target devices are data storage devices of the SLM. The SCSI interface and SCSI bus contain parity generation and detection hardware. This hardware monitors the integrity of data transmission between the SCSI interface and the SCSI targets.

The transmit and receive FIFO banks act as buffers for data transfers. The link handler section and the SCSI interface section can perform direct memory access (DMA) transfers of data. These transfers occur between the buses and FIFO banks of the link handler. These transfers occur between the buses and FIFO banks of the SCSI interface sections. This capability allows a high data flow rate between the two buses.

Parity generation and detection circuits on both FIFO banks monitor the integrity of the data while the data resides in the FIFOs.

Middle section of figure

The middle section of the figure represents the controlling layer and test functions. The middle section has the following main hardware entities:

- microprocessor unit
- EPROM program memory
- static RAM
- card status and control registers

NT9X44AD (continued)

- bus isolator
- FIFO test access ports

To control the SLM card, the microprocessor unit uses a program . This program resides in the EPROM. The microprocessor unit uses the static RAM for data buffering functions. The card status and control registers control and monitor different card functions.

The bus isolator controls interaction between the transfer bus and the data bus of the microprocessor unit. When direct memory access data transfers occur between the SCSI interface and a FIFO bank, the isolator separates the two buses. In other conditions, the isolator provides the microprocessor unit with access. This access is to the FIFO banks and the internal registers in the SCSI interface. The microprocessor unit uses control and status registers to control the state of isolation.

The FIFO test access ports provide the microprocessor unit with access to the FIFO banks. The ports provide this access from the end of the microprocessor unit that connects to the link handler. This configuration allows tests of the integrity of the FIFOs to occur without the use of the link handler. This configuration also allows the performance of special data control operations. Controller operation can require this special data control.

Bottom section of figure

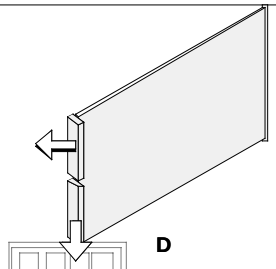
The bottom section of the figure represents the interface to the ID PROM. The bottom section of the figure also represents and the interface to the system through the NT9X46AA paddle board. The controller card on the NT9X44AD interfaces directly to the NT9X46AA.

Signaling

Pin numbers

The pin numbers for the NT9X44AD appear in the following figure.

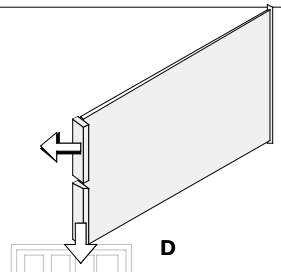
NT9X44AD pin numbers (Part 1 of 2)



	D	C	B	A
1			+12 V	GND
2			+12 V	GND
3			+12 V	GND
4			+12 V	GND
5			+12 V	GND
6			+12 V	GND
7			+12 V	GND
8			+12 V	GND
9				GND
10			12V–CONV–ON–	GND
11			SLU–RESET–	GND
12				GND
13				PENB–
14				R/W–
15	OOBIN0		CLK*1	PDTACK–
16			CLK*2	C244
17			SLU+5*–	PADDR0
18			CLK*4	PADDR1
19			CLK*5	PADDR2
20			CLK*6	PADDR3
21	OOBIN1		CLK*7	DREN–
22			CLK*8	PADDR4
23	RSTOUT–	BUSLOCK–		PADDR5
24				
25				
26				
27				
28	PWRT–			
29		DTACK–		HW4
30				
31				
32				SH0
33	DAS32–			SH1
34				–FP61
35		ADDR01	TYPE1	C61
36		ADDR02	HW0	+12
37		ADDR03	HW1	+12
38		ADDR04	HW2	+12
39		ADDR05	HW3	+12
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5
45		ADDR11	MR–/W+	+5

NT9X44AD (continued)

NT9X44AD pin numbers (Part 2 of 2)



	D	C	B	A
1			+12 V	GND
2			+12 V	GND
3			+12 V	GND
4			+12 V	GND
5			+12 V	GND
6			+12 V	GND
7			+12 V	GND
8			+12 V	GND
9				GND
10			12V–CONV–ON–	GND
11			SLU–RESET–	GND
12				GND
13				PENB–
14				R/W–
15	OOBIN0		CLK*1	PDTACK–
16			CLK*2	C244
17			SLU+5*–	PADDR0
18			CLK*4	PADDR1
19			CLK*5	PADDR2
20			CLK*6	PADDR3
21	OOBIN1		CLK*7	DREN–
22			CLK*8	PADDR4
23	RSTOUT–	BUSLOCK–		PADDR5
24				
25				
26				
27				
28	PWRT–			
29		DTACK–		HW4
30				
31				
32				SH0
33	DAS32–			SH1
34				–FP61
35		ADDR01	TYPE1	C61
36		ADDR02	HW0	+12
37		ADDR03	HW1	+12
38		ADDR04	HW2	+12
39		ADDR05	HW3	+12
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5
45		ADDR11	MR–/W+	+5

Technical data

Power requirements

The following table lists the power requirements for the NT9X44AD.

Power requirements	
Standard voltage	5V, 12V
Standard current	4A, (6A maximum)

NT9X45BA

Product description

The 3-DS512 link and 16-DS30 port paddle board combines an enhanced network (ENET) paddle board and the full capacity of NT9X41BA. The ENET paddle board is equivalent to three quarters of the functionality of NT9X40BA.

Functional description

The NT9X45BA provides 16 DS30 links between ENET and current DS30-based peripherals. The NT9X45BA provides the interface for three DS512 fiber links. The performs all the conversion that an interface requires. This interface is of DS512 fiber links with the parallel processor bus (P-bus) and the crosspoint (XPT) card (NT9X35BA/CA).

Functional blocks

The NT9X45BA contains the following functional blocks:

- fiber interface block
- fiber input/output (I/O) block
- P-bus interface and timing block
- bit rate converter (BRCX)
- DS30 interface block

Fiber interface block

The fiber interface block consists of the quad-fiber link interface chip (QFLIC) and three DS512 transmit/receive controllers (DTRC). The QFLIC is the interface between the optical fiber modules (fiber input/output block) and the DTRC. The QFLIC serves as interface in the transmit and receive directions. In the receive direction, the QFLIC receives the electrical signal from the receive fiber module (fiber I/O block). The QFLIC converts the data to parallel transmission and sends the data to the DTRC. In the transmit direction, the QFLIC receives parallel data from the DTRC. The QFLIC converts the data to serial transmission and sends the data to the transmit fiber module (fiber I/O block).

Fiber input/output block

The fiber I/O block consists of a TTL-to-ECL and ECL-to-TTL translator. This translator provides a two-way conversion between transistor-transistor logic (TTL) signals and differential emitter coupled logic (ECL) signals. The fiber modules of this block perform two-way electro-optical conversion. The fiber modules perform this conversion between the ECL signals and light that transmission on a DS512 fiber link requires.

Processor-bus interface and timing block

The P-bus interface and timing block performs functions that address, data buffer, time and decode. The P-bus interface is the central processor interface to the NT9X45BA paddle board.

Bit rate converter

The BRCX block consists of the R41 chip. The R41 chip provides timing signals for the N03 chip in the DS30 interface block and a DTRC. The BRCX block facilitates local and remote loopback modes that operate. Tests use these modes.

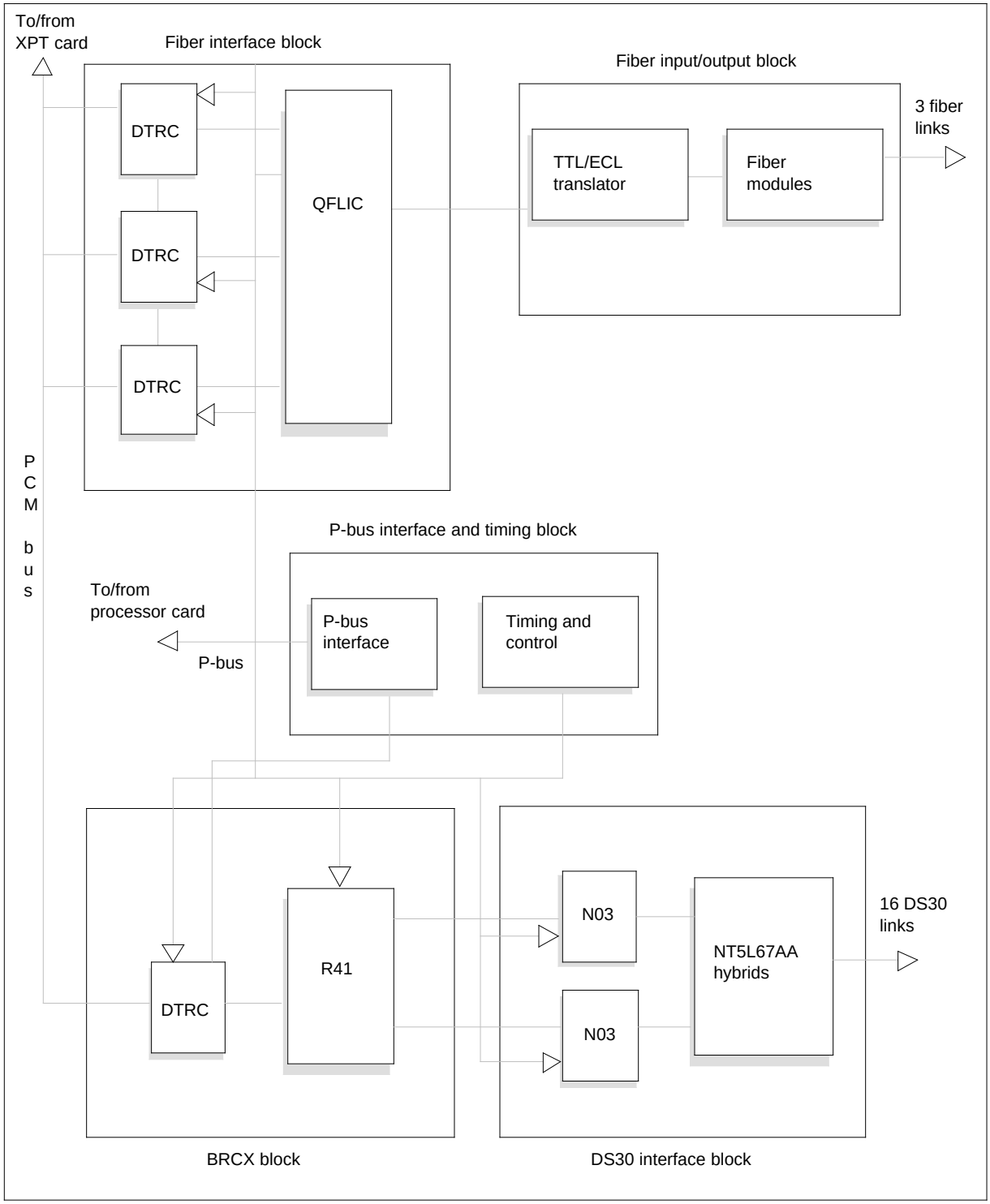
DS30 interface block

The DS30 interface block uses two N03 chips to each handle eight bidirectional DS30 links. These chips replace the W87 chips that the NT9X41BA uses. The DS30 interface block continues to contain eight NT5L67AA DS30 hybrids. These hybrids provide two bidirectional link terminations. The NT9X41B also contains eight hybrids.

The relationship between the functional blocks appears in the following figure.

NT9X45BA (continued)

NT9X45BA functional blocks



Signaling

Pin numbers

The faceplate connections of the NT9X45BA appear in the following tables.

NT9X45BA fiber port assignments

Connector	Zone	Color	Connector	Zone	Color
TX16	1	orange	RX17	4	green
RX16	2	blue	TX18	5	orange
TX17	3	brown	RX18	6	blue

NT9X45BA DS30 port signals for connector J1 (Zone 8)

Pin	Name	Pin	Name
4	OUTP1	8	INP1
5	OUTN1	9	INN1

NT9X45BA DS30 port signals for connector J2 (Zone 12) (Sheet 1 of 2)

Pin	Name	Pin	Name
1	OUTP0	32	INP8
2	OUTN0	33	INN8
3	INP0	34	OUTP11
4	INN0	35	OUTN11
5	OUTP4	36	INP11
6	OUTN4	37	INN11
7	INP4	38	OUTP14
8	INN4	39	OUTN14
9	OUTP7	40	INP14
10	OUTN7	41	INN14
11	INP7	42	
12	INN7	43	OUTP3

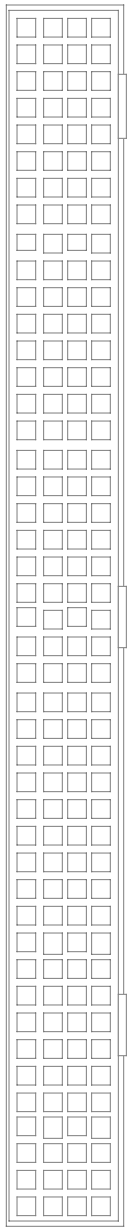
NT9X45BA (continued)

NT9X45BA DS30 port signals for connector J2 (Zone 12) (Sheet 2 of 2)

Pin	Name	Pin	Name
13	OUTP10	44	OUTN3
14	OUTN10	45	INP3
15	INP10	46	INN3
16	INN10	47	OUTP6
17	OUTP13	48	OUTN6
18	OUTN13	49	INP6
19	INP13	50	INN6
20	INN13	51	OUTP9
21		52	OUTN9
22	OUTP2	53	INP9
23	OUTN2	54	INN9
24	INP2	55	OUTP12
25	INN2	56	OUTN12
26	OUTP5	57	INP12
27	OUTN5	58	INN12
28	INP5	59	OUTP15
29	INN5	60	OUTN15
30	OUTP8	61	INP15
31	OUTN8	62	INN15

The pin numbers for the NT9X45BA appear in the following figures.

NT9X45BA pin numbers (Part 1 of 2)



	A	B	C	D
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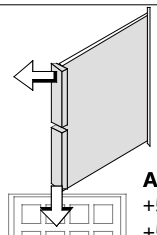
24				
25				
26	GND	RDAT1	RDAT0	DATA24
27	+5V	RDAT3	RDAT2	DATA25
28	+5V	RDAT5	RDAT4	DATA26
29	GND	RDAT7	RDAT6	DATA27
30	+5V	RDAT9	RDAT8	DATA28
31	+5V	WBUS1	WBUS0	DATA29
32	GND	WBUS3	WBUS2	DATA30
33	--5.2V	WBUS5	WBUS4	DATA31
34	--5.2V	WBUS7	WBUS6	NSEL0
35	--5.2V	WBUS9	WBUS8	NSEL1
36	--5.2V	RNW	BPRST	NSEL2
37	GND	DAS		NSEL3
38	GND	NSPE	NMPE	NSTB0
39	+5V	ADDR1	ADDR0	NSTB1
40	+5V	ADDR3	ADDR2	NSTB2
41	+5V	ADDR5	ADDR4	NSTB3
42	+5V	ADDR7	ADDR6	NRFP0
43	GND	ADDR9	ADDR8	NRFP2
44	+5V			NCSEN
45	+5V			

NT9X45BA (continued)

NT9X45BA pin numbers (Part 2 of 2)



	A	B	C	D
46	+5V			CK21P+
47	+5V			CK21P--
48	GND			NFP21P+
49	+5V			NFP21P--
50	+5V			CK61
51	+5V	CK97+	CK97--	NFP61
52	+5V	NFP97+	NFP97--	NTFP61
53	GND			
54				
55				
56				
57				
58	GND	GND	GND	
59				
60				
61				
62				
63				
64	GND	GND	GND	GND
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68				
69				
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90				

Technical data

Power requirements

NT9X45BA power requirements

Supply	Minimum	Nominal	Maximum
Supply voltage 1	-4.94V	-5.2V	-5.46V
Supply voltage 2	+4.75V	+5.0V	+5.25V
Supply current 1		.94A	
Supply current 2		1.7A	

NT9X46AA

Product description

The NT9X46AA parallel computing module (CM) port interface paddle board operates as a pair. One paddle board mounts behind an NT9X12 CPU port card. The other paddle board mounts behind an NT9X4402 system load module (SLM) controller. An interconnect cable joins the two paddle boards.

The paddle boards and interconnect cable replace the shorting bus (S-bus) on the backplane. The S-bus provides a message link between NT9X12 port cards and the paddle boards of the ports cards. The message link also can be between NT9X12 port cards and parent boards next to the ports cards.

In SLM applications, the NT9X4402 SLM controller communicates with the NT9X12 synchronous bus connection of the port card. The SLM can reside a maximum of several card slot positions away from the NT9X12 port card. The interconnect cable allows the paddle boards to traverse slot positions. The paddle boards can traverse the number of slot positions required to connect the following two S-busses. This connection is between the S-bus on the NT9X12 and the S-bus of the NT9X4402.

Functional description

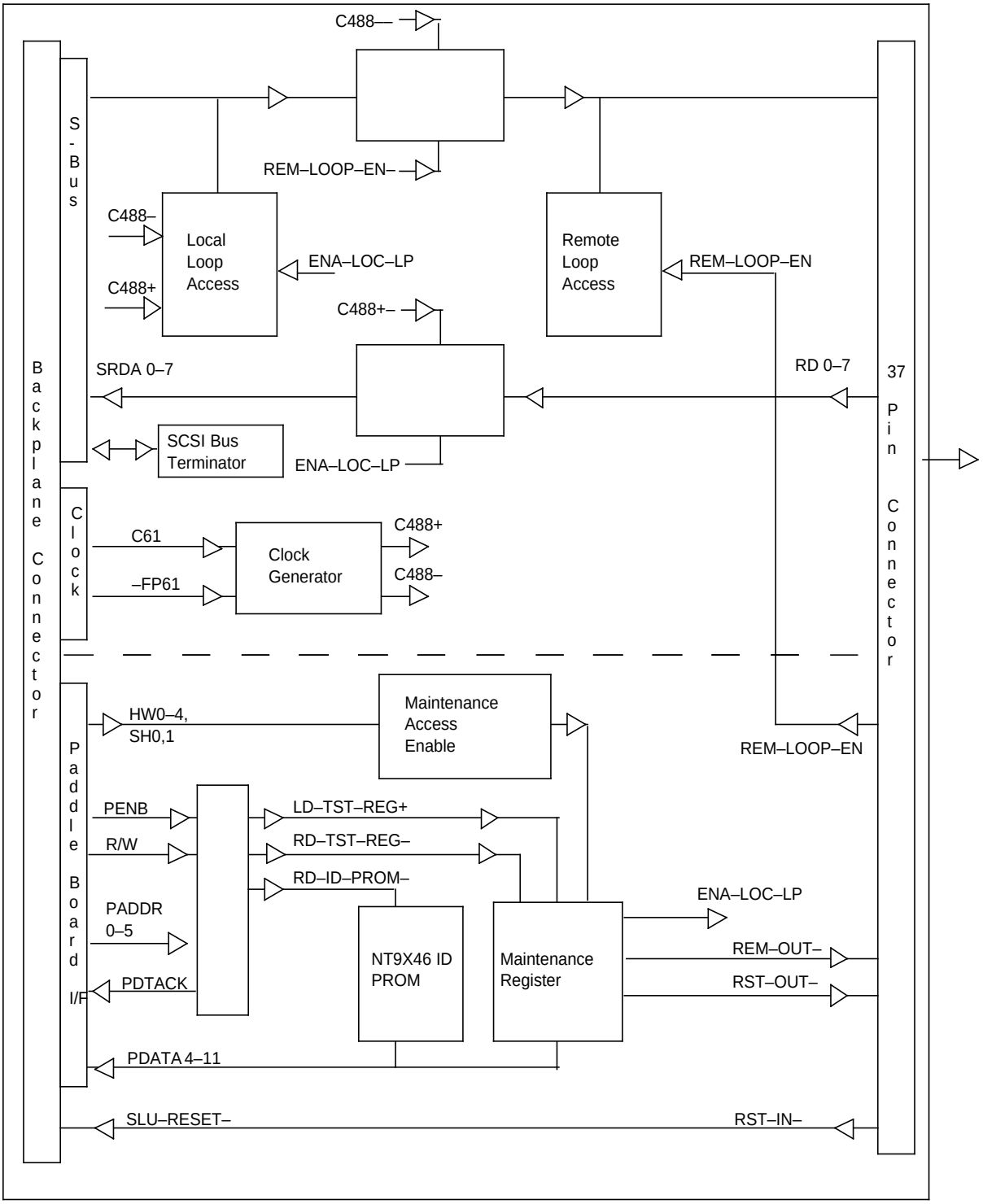
Functional blocks

The NT9X46AA contains the following functional blocks:

- local loop access
- remote loop access
- small computer system interface (SCSI) bus terminator
- clock generator
- maintenance access enable
- NT9X46 identification (ID) PROM
- maintenance register

The relationship between these blocks appears in the following figure.

NT9X46AA functional blocks



NT9X46AA (continued)

Local loop access

The local loop access block allows a direct data loop. This data loop is from the NTX12 S-bus transmit data (STDA) bus to the NT9X12 S-bus receive data (SRDA) bus. This loop allows tests of the NT9X12 link handler interface and bus connection to the local NT9X46AA to occur. The loop activates the local NT9X46AA paddle board.

Remote loop access

The remote loop access block allows data that originates on the NT9X12 SRDA bus to loop back to the NT9X12 SRDA bus. This process occurs after the data traverses the interconnect cable. This process allows tests of the interconnect cable and latches associated with transmission and reception in the local NT9X46AA paddle board. Activation of the remote loop access occurs through the maintenance register on the local NT9X46AA paddle board.

Small computer system interface bus terminator

The SCSI bus terminator is not part of the S-bus. The SCSI bus terminator terminates the SCSI bus of the NT9X44AA. This termination occurs through a part of the S-bus interface that is not in use.

Clock generator

The clock generator provides the 488-ns clock. This clock drives the latches used to handle data transfers.

Maintenance enable

The maintenance enable block makes sure of the following condition. The maintenance functions on the NT9X46AA paddle board only can be active when the paddle board is plugged into a slot. The NT9X12 CPU port card uses this slot. The block controls the remote and local loop back functions and the SLM paddle board reset function. A maintenance enable circuit makes sure of the following condition. The maintenance functions only can be active when the paddle board is plugged into the shelf behind an NT9X12 port card slot.

NT9X46 Identification PROM

The ID PROM is the identification element of the paddle board. The ID PROM contains:

- the NT product engineering code (PEC) of the parallel CM port interface paddle board.
- the manufacturing release of the board.
- the base hardware, software vintage.
- the current hardware, software vintage.

The processor bus in the paddle board address space of the NT9X12 port card provides access to the ID PROM.

Maintenance register

The maintenance register block controls the enabling and disabling of the local and remote loopback functions and the paddle board reset function.

The figure on page two shows the relationship between these functional blocks. The top part of the figure represents the S-bus hardware. The bottom part represents the ID PROM and maintenance access to the paddle board.

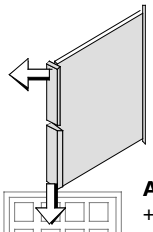
Signaling

Pin numbers

The pin numbers for the NT9X46AA appear in the following figure.

NT9X46AA (continued)

NT9X46AA pin numbers



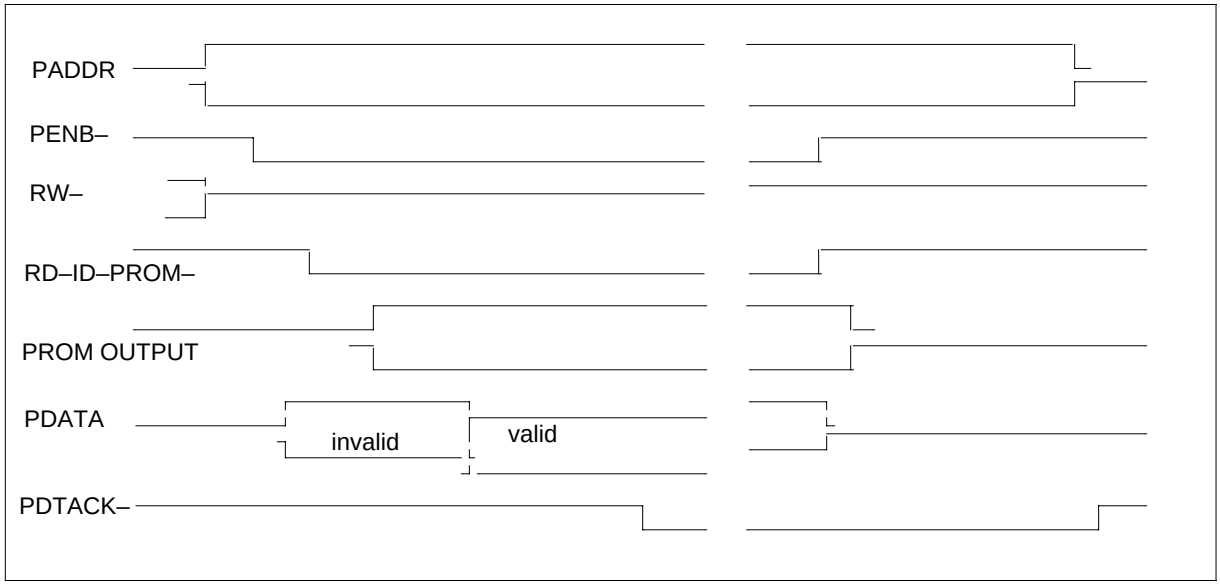
	A	B	C	D
1	GND	+12 V		
2	GND	+12 V		
3	GND	+12 V		
4	GND	+12 V		
5	GND	+12 V		
6	GND	+12 V		
7	GND	+12 V		
8	GND	+12 V		
9	GND			
10	GND			
11	GND	SLU–RST–		
12	GND			
13	PENB–			
14	R/W–			
15	PDTACK–			
16				
17	PADDR0			
18	PADDR1			
19	PADDR2			
20	PADDR3			
21				
22	PADDR4			
23	PADDR5			
24				
25				
26				
27				
28				
29	HW4			
30				
31				
32	SH0			
33	SH1			
34	–FP61			
35	C61	TYPE1		
36	+12	HW0		
37	+12	HW1		
38	+12	HW2		
39	+12	HW3		
40	GND			
41	GND			
42	GND			
43	GND			
44	+5			
45	+5			

	A	B	C	D
46	+5			
47	+5			
48	+5			
49	+5			
50	+5			
51	+5			
52	+5			
53	+5			
54	+5			
55	+5			
56	TYPE0			
57	PLTVL			
58	PLRVL			
59	STDA0			
60	STDA1			
61	STDA2			
62	STDA3			
63	STDA4			
64	STDA5			
65	STDA6			
66	STDA7			
67				
68				
69	SRDA0			
70	SRDA1			
71	SRDA2			
72	SRDA3			
73	SRDA4			
74	SRDA5			
75	SRDA6			
76	SRDA7			
77				
78				
79	GND			
80	GND			
81	GND			
82	GND			
83	GND	PDATA4		
84	GND	PDATA5		
85	GND	PDATA6		
86	GND	PDATA7		
87	GND	PDATA8		
88	GND	PDATA9		
89	GND	PDATA10		
90	GND	PDATA11		

Timing

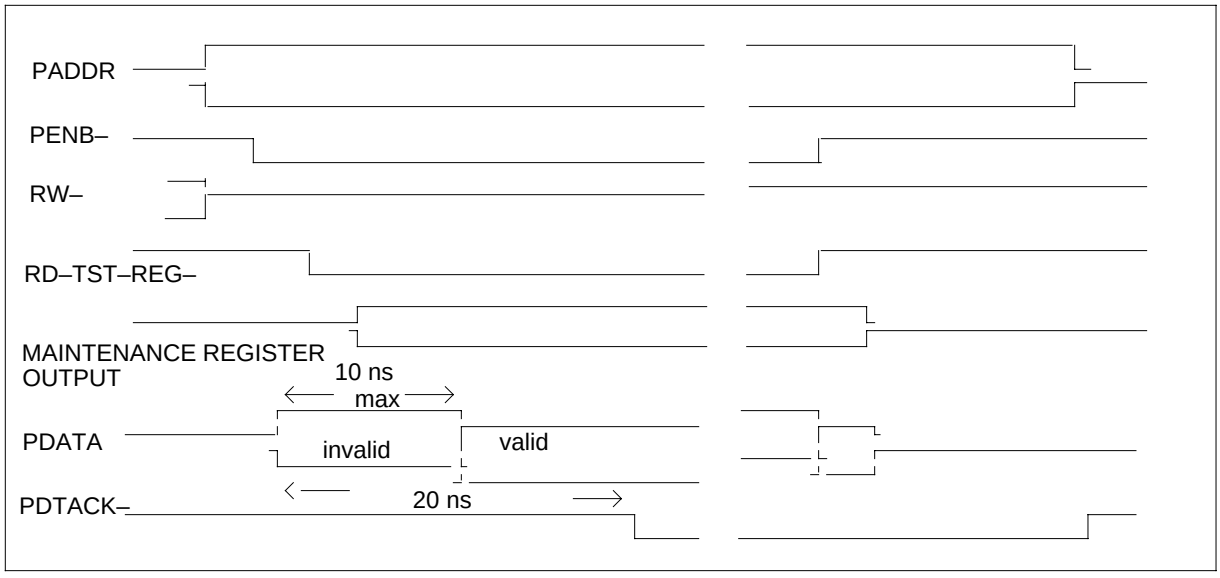
The ID PROM read timing appears in the following figure.

NT9X46AA ID PROM read timing



The maintenance register read timing appears in the following figure.

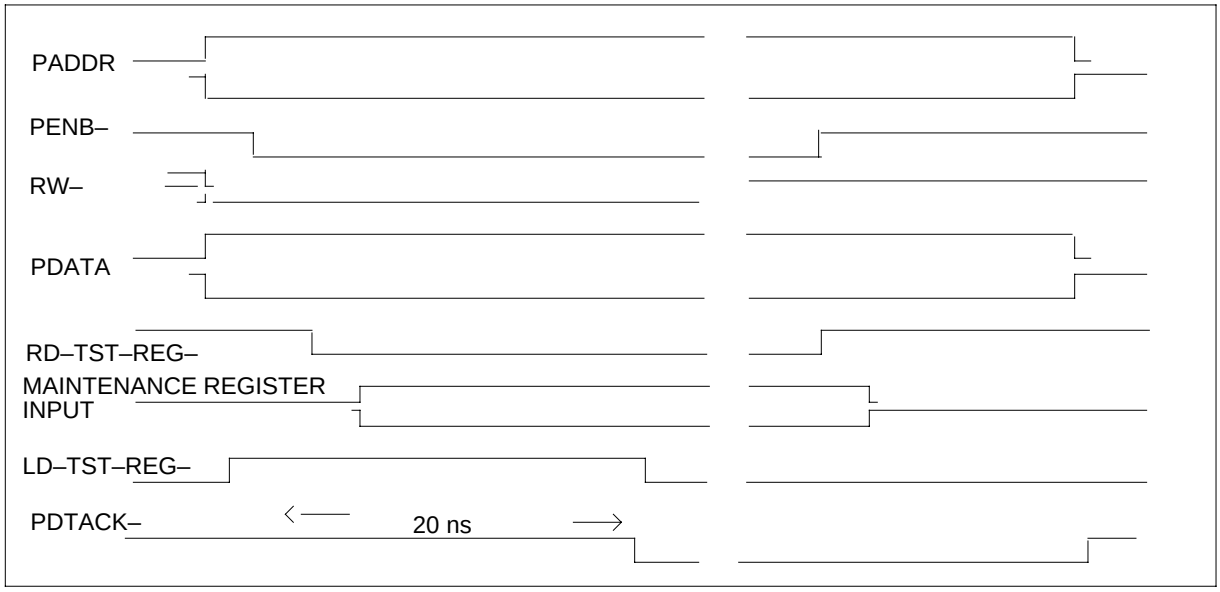
NT9X46AA maintenance register read timing



The maintenance register write timing appears in the following figure.

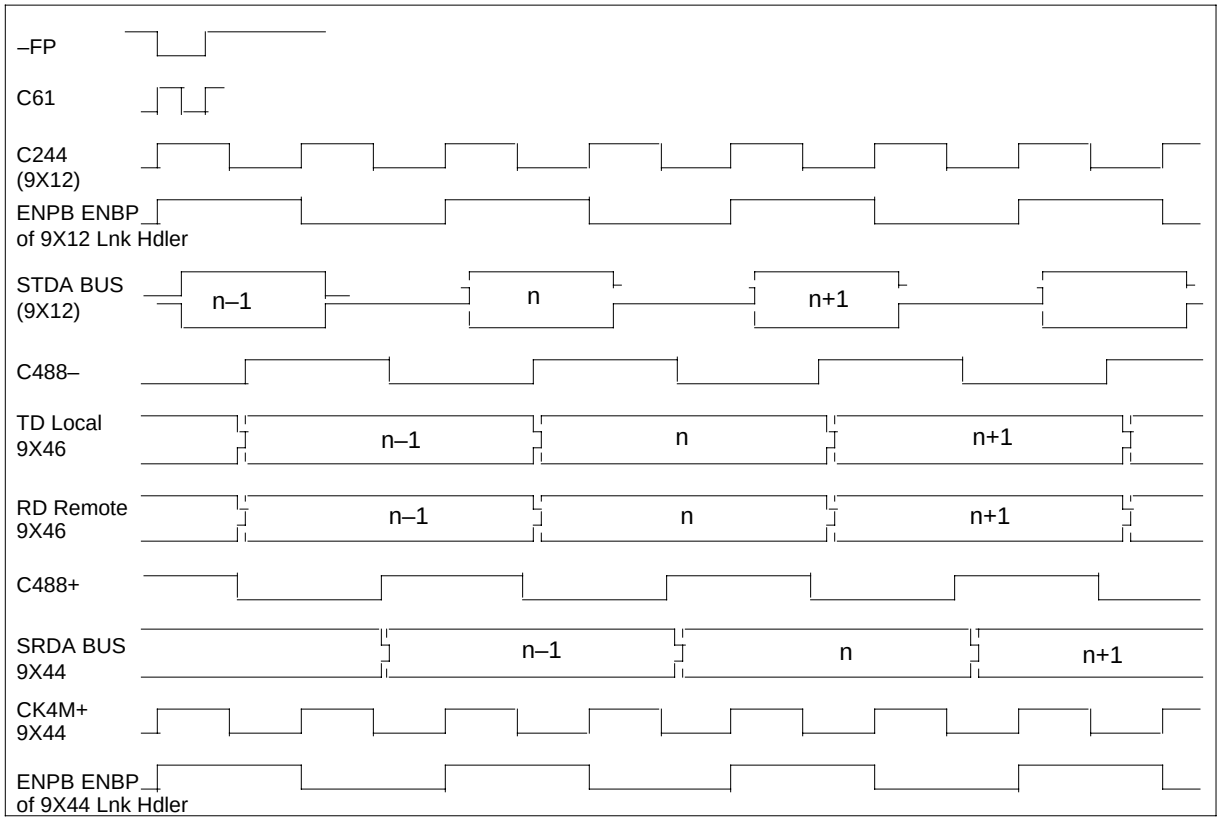
NT9X46AA (continued)

NT9X46AA maintenance register write timing



The link data transfer of NT9X12 to NT9X4402 timing appears in the following figure.

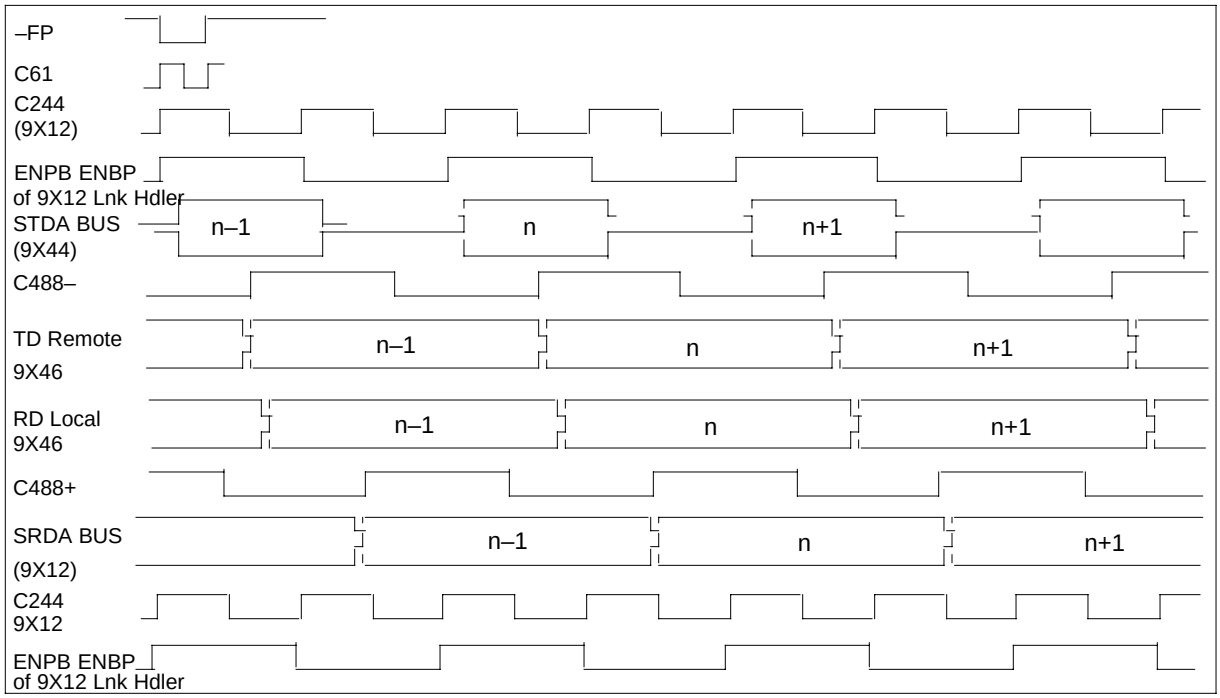
NT9X46AA link data transfer: NT9X12 to NT9X4402 timing



The link data transfer of NT9X4402 to NT9X12 timing appears in the following figure.

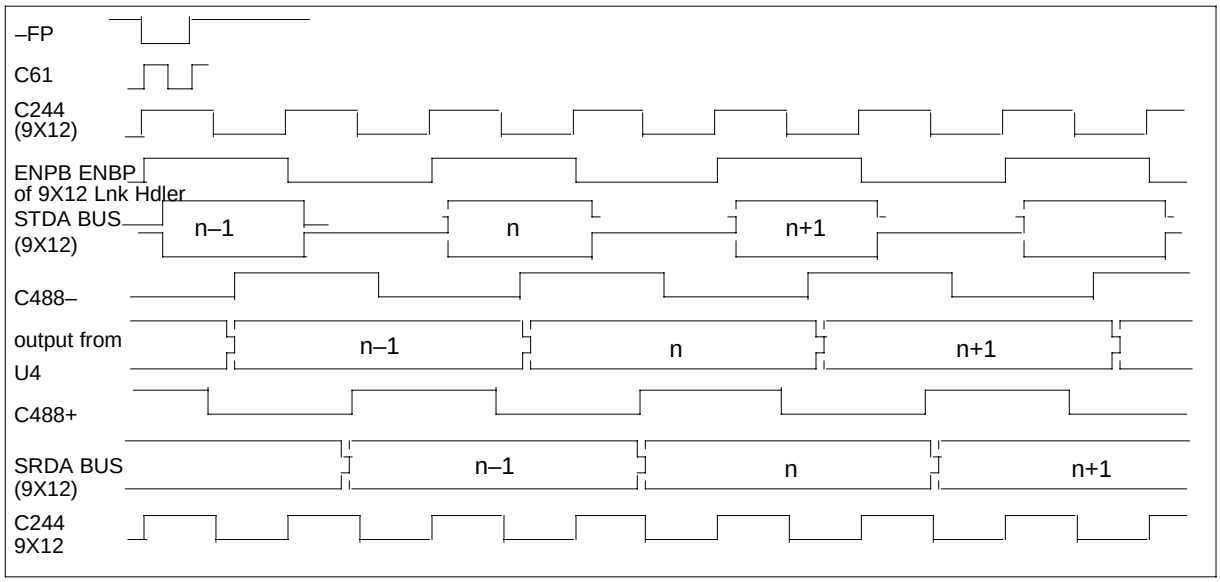
NT9X46AA (continued)

NT9X46AA link data transfer: NT9X4402 to NT9X12 timing



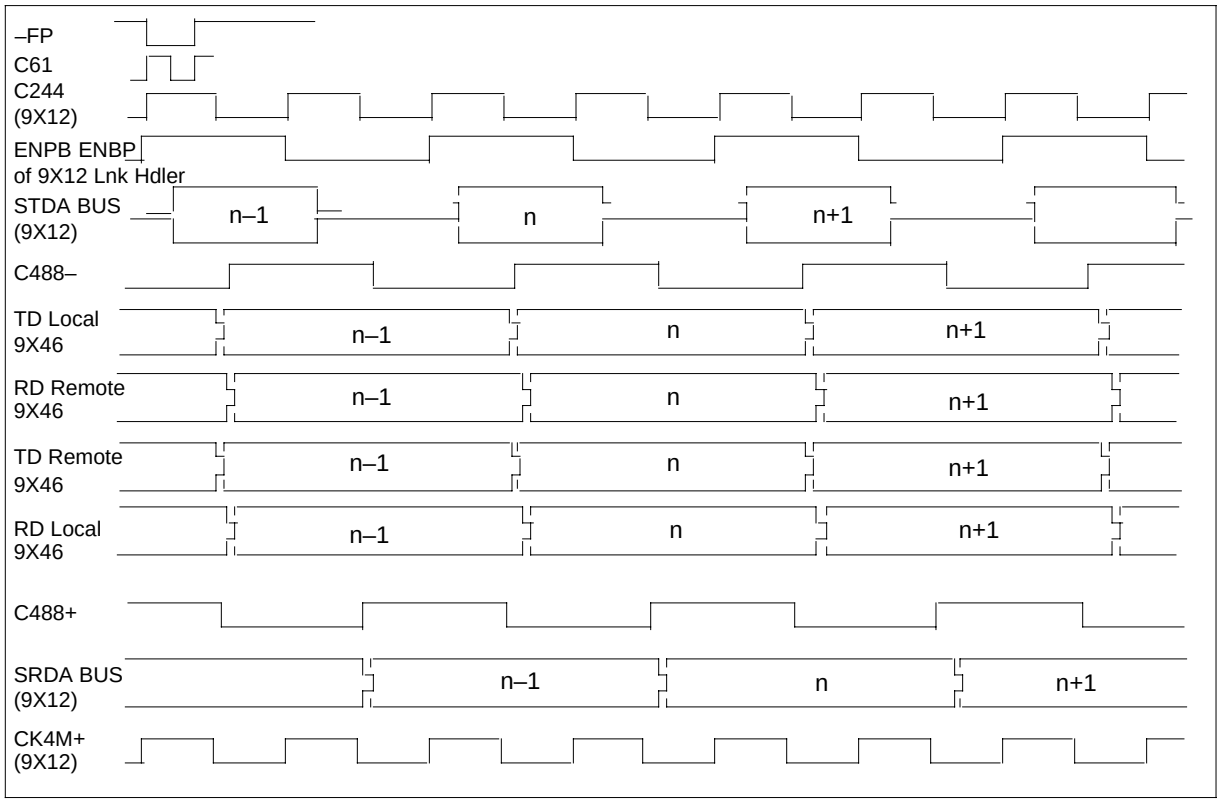
The local data loop of NT9X12 to to NT9X12 timing appears in the following figure.

NT9X46AA local data loop: NT9X12 to NT9X46AA to NT9X12 timing



The remote data loop of NT9X12 to to NT9X12 timing appears in the following figure.

NT9X46AA remote data loop: NT9X12 to NT9X46AA to NT9X12 timing



Technical data

Power requirements

The NT9X46AA requires 5V, ±5%, or 12V, ±5%.

NT9X47AA

Product description

The NT9X47AA +12V power converter provides power to the NT9X44 system load module (SLM). The card uses the NT9X03 frame supervisory panel (FSP) to interface with DMS–100 alarm circuits.

Location

The power converter has two card connectors that plug into female backplane connectors on the DMS SuperNode power converter backpanel.

Functional description

The NT9X47AA converts input power (-42V to -56V) to +12V output. The converter sends error signals to the FSP if the output voltage differs from an internal reference voltage. The converter sends a shutdown signal to indicate overvoltage and undervoltage conditions.

Functional blocks

The NT9X47AA contains the following functional blocks:

- input filter
- input control
- auxiliary power supply
- pulse width modulator (PWM)
- monitor circuit
- output circuit
- enable circuit
- relays

Input filter

The input filter receives the office battery voltage and sends a dc output to the auxiliary power supply. To perform this function, the input filter converts the voltage to an isolated square wave signal and filters the signal.

Input control

The input control receives the office battery voltage. The input control holds the power supply until operating company personnel activate the auxiliary power supply circuit.

Auxiliary power supply

The auxiliary power supply receives a –48V nominal input. This power supply transmits an isolated +15V output. Operating company personnel turn the ON/OFF switch to ON to activate the power supply.

Operating company personnel can apply temporary battery return (BR) to the appropriate connector pins. This process activates and deactivates the power supply.

Pulse width modulator

The PWM uses power threshold signals, shutdown signals and voltage error signals to adjust the duty cycle of the switching signal. The modulator provides variable duty cycle pulses to drive the power switch. The modulator uses a 64–kHz frequency to perform switches.

Monitor circuit

The monitor circuit monitors the primary current in the power switch. If the current exceeds a designated threshold, the following action occurs. The modulator sends a signal to the PWM to reduce the duty cycle of the switching signal.

Output circuit

The output circuit receives the dc voltage from the PWM and outputs a +12V, 10A current. The circuit sends a shutdown signal to the PWM if overvoltage or undervoltage conditions occur.

Operating company personnel can ground the appropriate connector pin. This process places the output circuit in a standby mode. The circuit output stops, but the functions remain active.

Operating company personnel can apply a -48V current to the appropriate connector pin and bypass the ON/OFF switch of the circuit. This process locks the circuit in the ON position.

Enable circuit

The enable circuit receives an activation signal from the 5V power supply and activates the auxiliary power supply.

NT9X47AA (continued)

Relays

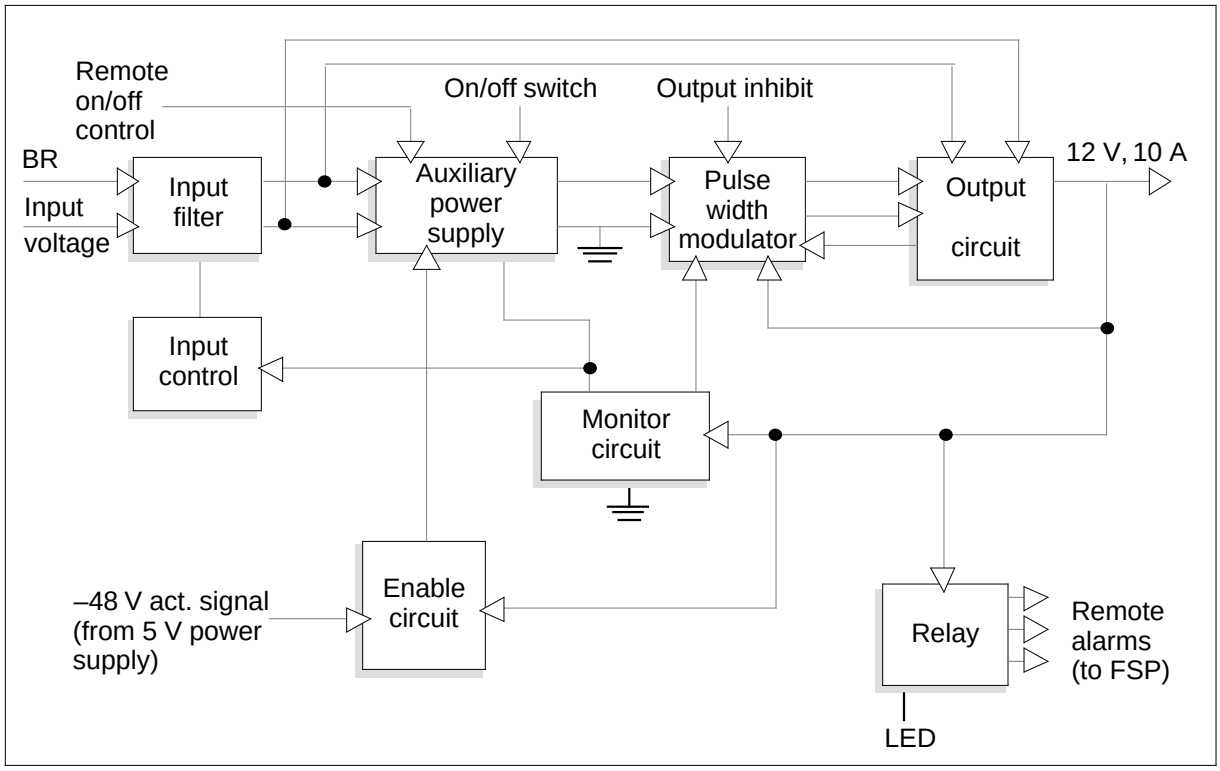
This feature provides two relays to send alarm signals to the FSP. The following table lists the relays and relay functions.

Relay operation

Relay	Operated	Released
K1	Normal operation.	Generates an alarm signal when the output voltage drops.
K2	Normal operation.	Generates an alarm signal when the output voltage drops.

The relationship between the functional blocks appears in the following figure.

NT9X47AA functional blocks



Technical data

The following table lists the electrical characteristics that NT9X47AA the outputs.

Electrical characteristics

Characteristic	Value
Voltage	+12V ±2%
High voltage shutdown	+14V ±1V
Low voltage shutdown	+10V ±1V
Steady state ripple	50mV rms
Maximum current	10A
Minimum current	0.5A
Current limit	13A ±2A
Transient response	90mV peak to peak (±7A step, 0.5A minimum load).

Physical dimensions

The dimensions for the NT2X35AB follow:

- total height: 26.7 cm (10.5 in)
- total depth: 37.3 cm (14.7 in)
- total width: 6.4 cm (2.5 in)

Power requirements

The following table lists the power requirements for the NT2X35AB.

Power requirements

Voltage	Current
-42V minimum	4A
-48V nominal	4A
-56V maximum	4A

NT9X47AB

Product description

The NT9X47AB +12V power converter provides power to the NT9X44 system load module (SLM). The card interfaces with DMS–100 alarm circuits. The card uses the NT9X03 frame supervisory panel (FSP) to interface with the DMS–100 alarm circuits. The NT9X47AB is the 60 V version of the NT9X47AA.

Location

The power converter has two card connectors that plug into female backplane connectors on the DMS SuperNode power converter backpanel.

Functional description

The NT9X47AB converts office–battery voltage ranging from -39 V to -75 V to an output of +12 V. The converter shuts down under overvoltage and undervoltage conditions. A fixed internal reference voltage determines these conditions. Shutdown of a converter sends an alarm signal to the FSP.

Functional blocks

The NT9X47AB has the following functional blocks:

- input filter
- input control
- auxiliary power supply
- pulse width modulator (PWM)
- output monitor circuit
- output stage

Input filter

The input filter receives the office battery voltage. The input filter provides high frequency common–mode filtering. This filtering reduces noise and electromagnetic interference (EMI) fed back to the source. A differential filter reduces noise that the converter switching causes. An inrush thermistor limits the charging current when the thermistor applies the battery voltage across the converter input.

Input control

Use a switch mounted on the faceplate of the converter to power up or shut down the converter. Remote start–up and shut–down signals have support. When the power switch is enabled, the auxiliary supply module turns on. This module supplies power to the QMS142A monitor circuit and the QMS143A

pulse–width modulator (PWM) controller module. The system activates the relays when the auxiliary supply voltage exists.

Auxiliary power supply

The auxiliary power supply receives office–battery input. This supply transmits an isolated +15 V output. To activate the power supply, turn the ON/OFF switch to ON.

To activate and deactivate the power supply, apply temporary battery return (BR) to the remote–start pin. To deactivate the power supply, apply temporary BR to the remote–shutdown pin.

Pulse width modulator

A current–sense transformer senses the incoming current. This information feeds back to the PWM controller. This feedback limits the current in the transistors. The system references the QMS143A PWM controller module to the output return. The system directly senses the output voltage that controls the transistor switching. The transistors reduce the input dc voltage. The transistors apply an ac waveform alternately across the two primary windings of the power transformer.

Output monitor circuit

The regulated output voltage can rise above, or fall below a specified level. When this condition occurs, the QMS142A monitor circuit sends a signal to the PWM to shut down the converter. The converter does not automatically restart. The converter remains off until a manual restart occurs.

Lock the circuit in the ON position and apply the negative battery voltage to the correct pin (-BAT.ACT.SIG). This action overrides the ON/OFF switch of the circuit.

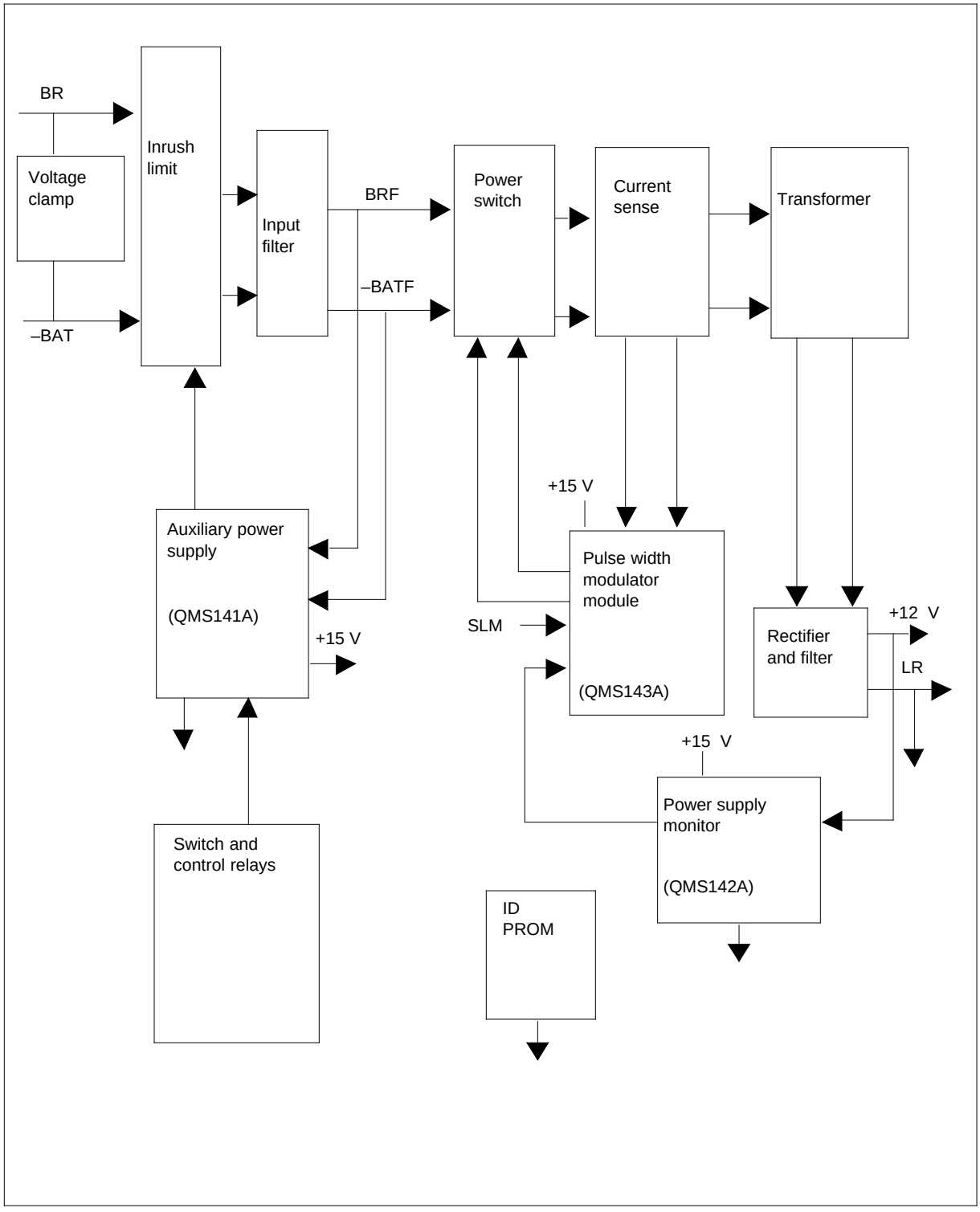
Output stage

The winding of the secondary transformer provides a low–amplitude ac squarewave. The system rectifies this squarewave and filters to produce the correct dc output voltage. A shunt resistor preloads this output. The system provides decoupling at the output.

The relationship between the functional blocks appears in the following figure.

NT9X47AB (continued)

NT9X47AB functional blocks



Signaling

Pin numbers

The pin numbers for the NT9X47AB appear in the following tables.

Connector P1 CBR05 48 pin

Pin	Z	B	D
2	D2-5	D1-5	D0-5
4	D5-5	D4-5	D3-5
6	CS-5	+5V	D6-5
8	A1-5	A2-5	A3-5
10	A0-5	RAS/NC	RAS/C
12	RAS/NO	-ABS	EXT.LED
14	D7-5	NOCON-A	NOCON-B
16	BR.ABS	+12V	+12V
18	LR	LR	LR
20	+12V	+12V	+12V
22	LR	LR	LR
24	+12V	+12V	+12V
26	LR	LR	LR
28	+12V	+12V	+12V
30	LR	LR	LR
32	+12V	+12V	+12V

Connector P2 CBR05 48 pin (Sheet 1 of 2)

Pin	Z	B	D
2	LR	LR	LR
4	+12V	+12V	+12V
6	LR	LR	LR
8	+12V	+12V	+12V

NT9X47AB (continued)

Connector P2 CBR05 48 pin (Sheet 2 of 2)

Pin	Z	B	D
10	LR	LR	LR
12	+12V	+12V	+12V
14	LR	LR	LR
16	+12V	+12V	+12V
18	-BAT.ACT.SIG	LR	LR
20	SD	REM.START	-BT
22	REM.SHDN	+15V	OV/UV.TEST
24	EXT.SW.ON	EXT.SW.OFF	EXT.SWT
26	-BAT	-BAT	-BAT
28	-BAT	-BAT	-BAT
30	BR	BR	SLM
32	BR	BR	BR

Technical data

Power requirements

The nominal input voltage is –48 V, but a range of –39 V to –75 V is acceptable. The maximum input current is 4 A.

Output

The output specifications for the NT9X47AB appear in the following table.

Output specifications (Sheet 1 of 2)

Pin	Z	B	D
Voltage		+12 V ±5%	
High voltage shutdown		+14 V ±1 V	
Low voltage shutdown		+10 V ±1 V	
Steady state ripple		50 mV rms	
Maximum current		10 A	

Output specifications (Sheet 2 of 2)

Pin	Z	B	D
Minimum current		0.5 A	
Current limit		13 A ±2 A	
Transient response		90 mV peak to peak (±7 A step, 0.5 A minimum load)	

NT9X49BA

Product description

The message switch (MS) transaction bus (T-bus) of the terminator card provides bus termination on the T-bus. The NT9X49BA contains T-bus shelf arbitration logic and a set of buffers for the system clocks.

Location

The NT9X49BA is in slot one at the end of the MS shelf.

Functional description

Functional blocks

The NT9X49BA has the following functional blocks:

- T-bus termination
- T-bus shelf arbitration logic
- system clock distribution buffers

Transaction bus termination

Forty-eight bus termination resistor pairs match the impedance on the T-bus. These resistors have a 220-ohms pull-up and a 330-ohms pull-down.

Transaction bus shelf arbitration logic

The T-bus shelf arbitration logic arbitrates between shelves for the use of the global bus. A message source can assert the request line. The U121-13, 12 inverts the message source and the message source passes to the T-bus extender card. The T-bus extender card "ORs" the request with a global bus signal PBUSY. The request signal gates the shelf address to the GSEG bus. The system drives both PBUSY and GSEG on the NT9X49BA. The system compares GSEG address (U28) with the shelf address. If the GSEG address is the same as the shelf address and PBUSY is true, a grant (-GRT) generates and returns to the local T-bus. If the GSEG address is less than the shelf address, a REQ inhibit (INH) issues back to the local bus. This signal stops requests of higher priority that can disturb the current access.

If the shelf does not contain a T-bus extension card, signal EXTP+ goes low. This action allows signal shelf operation of the T-bus without global bus arbitration.

This section includes the shelf address set switches. These switches set the hardware address of the shelf and must be provisioned.

System clock distribution

The NT9X49BA buffers the main system clocks for the MS shelves. The source of the clock is the local shelf clock cards for the MS CPU. The other source of the clock is the shelf extension paddle board for the secondary shelves.

Technical data

Power requirements

The NT9X49BA requires +5 V input voltage. The NT9X49BA requires 1.02 A input current and 5.1 W input power.

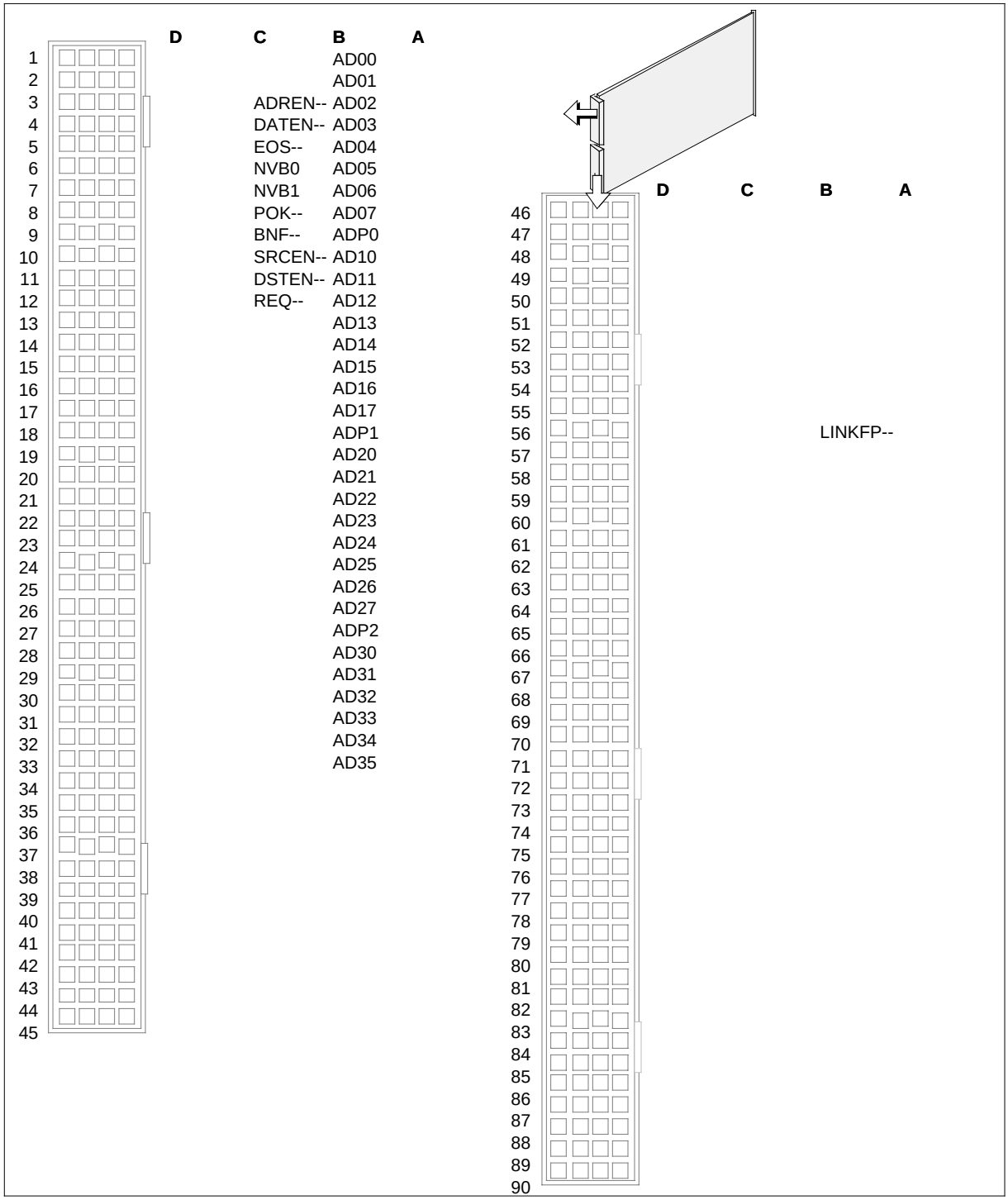
Signaling

Pin numbers

The pin numbers for the NT9X49BA appear in the following figure.

NT9X49BA (end)

NT9X49BA pin numbers



NT9X49CA

Product description

The NT9X49CA message switch (MS) processor–bus (P–bus) terminator circuit card provides termination for MS backplane tracks. The message switch processor (MSP) uses the MS backplane tracks. The NT9X49CA provides an interface to the P–bus extender paddle board (PB) (NT9X48AA). The NT9X49CA provides a time–out on the MS transaction bus (T–bus).

Location

The NT9X49CA is in the far right CP slot on every shelf of the MS.

Functional description

The NT9X49CA performs the following functions in the MS:

- terminates transitor–transitor logic (TTL) backplane signals associated with the P–bus
- provides an interface to control the P–bus extender cards
- drives the upper address bits on secondary shelves
- provides a data strobe to the P–bus extender when secondary shelves are accessed
- provides signals to clear the T–bus when timeouts occur
- locks the power converters on an active MS
- provides access to identification (ID) PROMs. These PROMs are on the NT9X48AA, NT9X30AA and NT9X31AA (power converters on the right side of the shelf), and the CP.

The MS allows packets of information to pass between port cards. Port cards exchange packets of information over a synchronous data bus. The synchronous data bus is the T–bus. Other cards in the system provide clocks, additional memory, and interfaces to data links.

A processor card based on the Motorola MC68020 microprocessor supervises the configuration and maintenance of the cards in an MS. This card communicates with cards in the MS over the P–bus. The length and speed of the P–bus requires termination resistors to be present at one end of the bus. These resistors reduce the amplitude of reflections on backplane signals.

The NT9X49CA on the MSP shelf of the message switch controls the enabling of NT9X48AA P–bus extension paddle boards on all shelves. This feature allows the MSP to disable all shelves without going over the P–bus of the MSP shelf.

NT9X49CA (continued)

The NT9X49CA monitors the T–bus for the following timeout conditions:

- no response (BNF) to an address cycle (ADREN)
- no response (BNF) to a data cycle (DATEN)

These conditions result in 256 ms of dead time on the T–bus until the gate arrays time out.

When the backplane signal CMACT - asserts (low), the message switch is active. When this condition occurs, the NT9X49CA sends a signal (PCLOCK-) to the power converters. The signal disables the faceplate power switch of the converters. The switches on the power converters cannot cause an accidental power down of an active message to occur.

The NT9X49CA provides access to the ID PROMs. The ID PROMS are on the two power converters on the right side of the shelf. The NT9X49CA provides access to the ID PROM on the NT9X48AA.

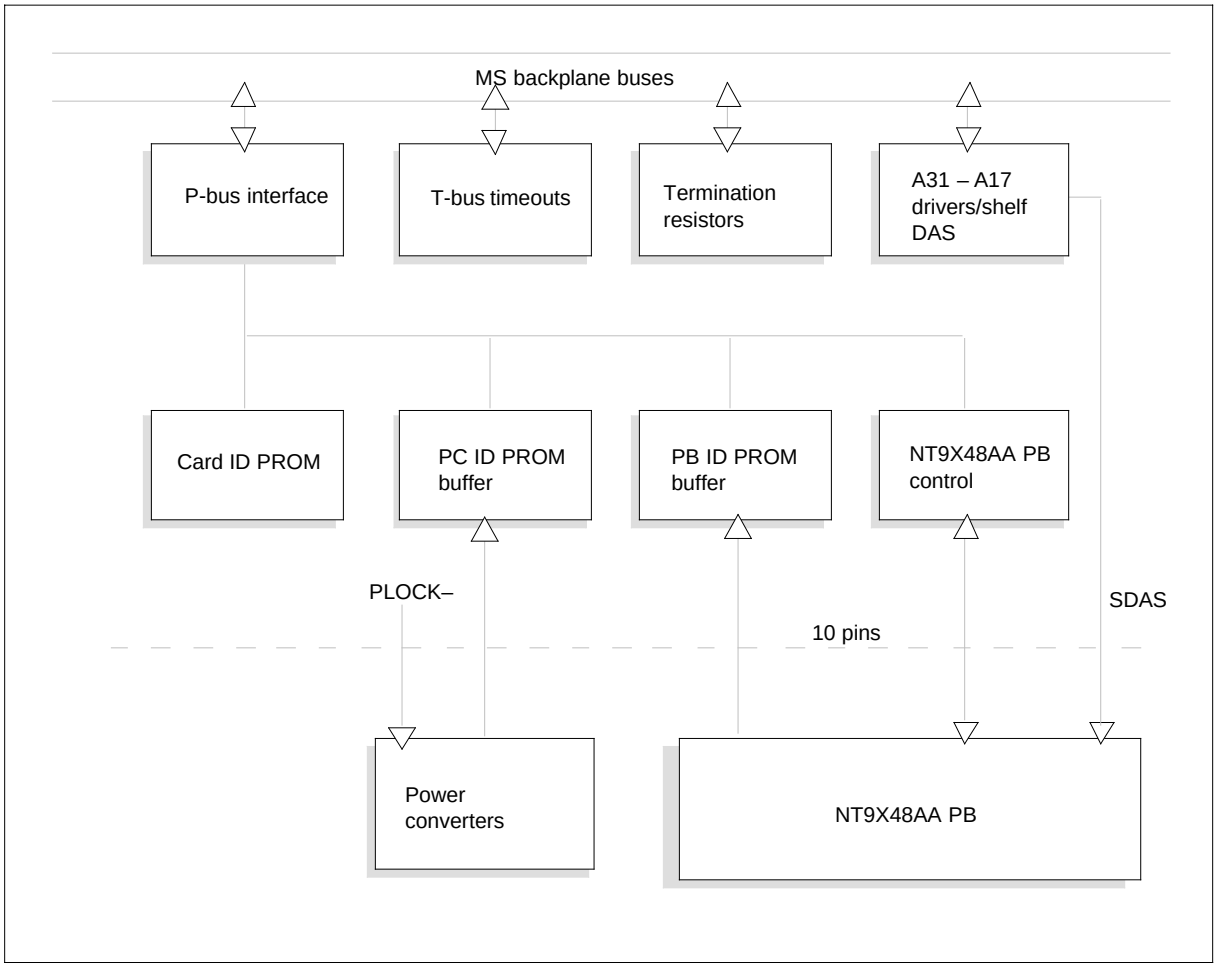
Functional blocks

The NT9X49CA has the following functional blocks:

- P–bus interface
- T–bus timeouts
- termination resistors
- A31–A17 drivers/shelf DAS
- card ID PROM
- PC ID PROM buffer
- PB ID PROM buffer
- NT9X48AA PB control
- power converters
- NT9X48AA PB

The relationship between the functional blocks appears in the following figure.

NT9X49CA functional blocks



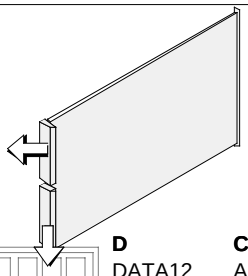
Signaling

Pin numbers

The pin numbers for the NT9X49CA appear in the following figure.

NT9X49CA (continued)

NT9X49CA pin numbers



	D	C	B	A
1				
2				
3		ADREN–		
4		DATEN–		
5				
6				
7				
8		POK–		
9		BNF–		
10				
11		DSTEN–		
12				
13		GRT–		EXTP–
14		INH–		SDAS–
15	PLN0–			PBCLR
16	OOB–IN0	SLNKFP–		PBPWUP
17				
18				ENSH0–
19				ENSH1–
20	SRST–			ENSH2–
21	OOB–IN1			ENSH3–
22	BUSBSY–			
23		BUSLOCK–		PEXTEN–
24				
25	BEN1–	BEN0–		
26	BEN3–	BEN2–		
27	LDS–	DAS–		
28	WRT–	UDS–		
29	HW4	DTACK–		
30	PARITY+			FP97–
31	PARITYEN–			C97
32	FAS–	S/E–		SH0
33	DAS32–	CPUCLK+		SH1
34	DATA00	EDAS–		FP61–
35	DATA01	ADDR01		C61
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	
41	DATA07	ADDR07		
42	DATA08	ADDR08	CMSYNC	
43	DATA09	ADDR09		
44	DATA10	ADDR10		
45	DATA11	ADDR11		

	D	C	B	A
46	DATA12	ADDR12		
47	DATA13	ADDR13		
48	DATA14	ADDR14	FACKN	
49	DATA15	ADDR15		
50	DATA16	ADDR16		
51	DATA17	ADDR17		
52	DATA18	ADDR18		
53	DATA19	ADDR19		
54	DATA20	ADDR20		
55	DATA21	ADDR21		
56	DATA22	ADDR22	LINKFP–	TYPE0
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70		LLBEN		
71				
72				
73				
74				
75	PCDAT0			
76	PCDAT2			
77	PCDAT4			
78	PCDAT6			
79	PCPROMM–		PBDAT0	
80	PCADD3		PBDAT1	
81	PCADD1		PBDAT2	
82			PBDAT3	
83	PLOCK–		PBDAT4	
84	PCDAT7		PBDAT5	
85	PCADD2		PBDAT6	
86	PCADD4		PBDAT7	
87	PCPROMP–		PBADD1	
88	PCDAT5		PBADD2	
89	PCDAT3		PBADD3	
90	PCDAT1		PBADD4	

Signal termination

The signal termination for the NT9X49CA. appears in the following table.

Signal termination

Pin	Termination	Pin	Termination	Pin	Termination
35C - 64C	110/165	28D	220/330	30A	120/120
25C	110/165	32C	220/330	16D	220/330
25D	110/165	34D - 65D	220/330	21D	220/330
26C	110/165	56A	220/330	40B	220/330
26D	110/165	15D	220/330	42B	220/330
33C	100/100	13C	220/330	23C	220/330
33D	220/330	14C	220/330	22D	220/330
27C	220/330	56B	220/330	70C	220/330
34C	220/330	16C	220/330	20D	220/330
32D	100/100	35A	121/75	48B	220/330
27D	220/330	31A	121/75		
28C	220/330	34A	200/200		

Technical data

Power requirements

The NT9X49CA requires a voltage of +5 V.

NT9X49CB

Product description

The NT9X49CB is a logic analyzer that traces transaction bus (T-bus) messages. The message switch processor can configure the NT9X49CB. The NT9X49CB acts as a T-bus activity monitor with programmable threshold detection. The NT9X49CB acts as a processor bus (P-bus) terminator. The NT9X49CB performs the same functions as the NT9X49CA (MS P-bus terminator card). The NT9X49CB replaces the NT9X49CA in card 26 of DMS-bus shelf 0.

Functional description

Functional blocks

The NT9X49CB has the following functional blocks:

- clock generation circuits
- T-bus interface
- P-bus interface
- operational measurements (OM) circuits
- cyclic redundancy check (CRC) circuits
- trigger-checking circuits
- termination block
- first-in, first-out memory (FIFO) block

Clock generation circuits

The clock generation circuits governs the generation of 8-MHz and 4-MHz clocks and the time-of-day counter. Each clock has a F224 driving positive and negative polarities to the various blocks.

Transaction bus interface

Address, data, and control information on the T-bus latches in on the negative edge of the 4-MHz T-bus clock. Two 12-bit registers capture the source and destination addresses. The trigger circuit and statistics RAM use the physical source and destination addresses. The system appends the physical source and destination addresses to the traced messages.

The following are the main functions of this block:

- time-out circuits
- sink function

- map failure indicator
- byte count

Processor-bus interface

The system decodes a P-bus access to the trace card and sets a card-access-valid (CAV) bit. The system holds the trace card in reset until the system writes the power-up bit in the NT9X49CA control register to 1.

Operational measurement circuits

This block counts the number of times a port operates as a source or destination.

Cyclic redundancy check checking circuits

The block checks the 16-bit CRC that the system appends to all P-bus messages. A 16-bit parallel shift occurs every 122 ns (8 MHz). The system implements CRC checks during the correct point in the message cycle. The correct point in the message cycle occurs after the system shifts the two CRC bytes.

Trigger checking circuits

The trigger checking circuits block controls the address match triggering feature. Trigger checking circuits perform the trigger masking.

Termination block

This termination block provides termination for the P-bus. The termination block provides termination to other signals that this block can terminate. The termination block is at the far right position on the backplane.

First-in first-out block

The FIFO block provides storage for four types of messages:

- the T-bus data of the message
- the time of day when the system stores the message
- the source and destination addresses
- the byte count and trigger status of the message

The FIFO block manages different options available in the configuration and control registers.

NT9X49CB (continued)

Technical data

Power requirements

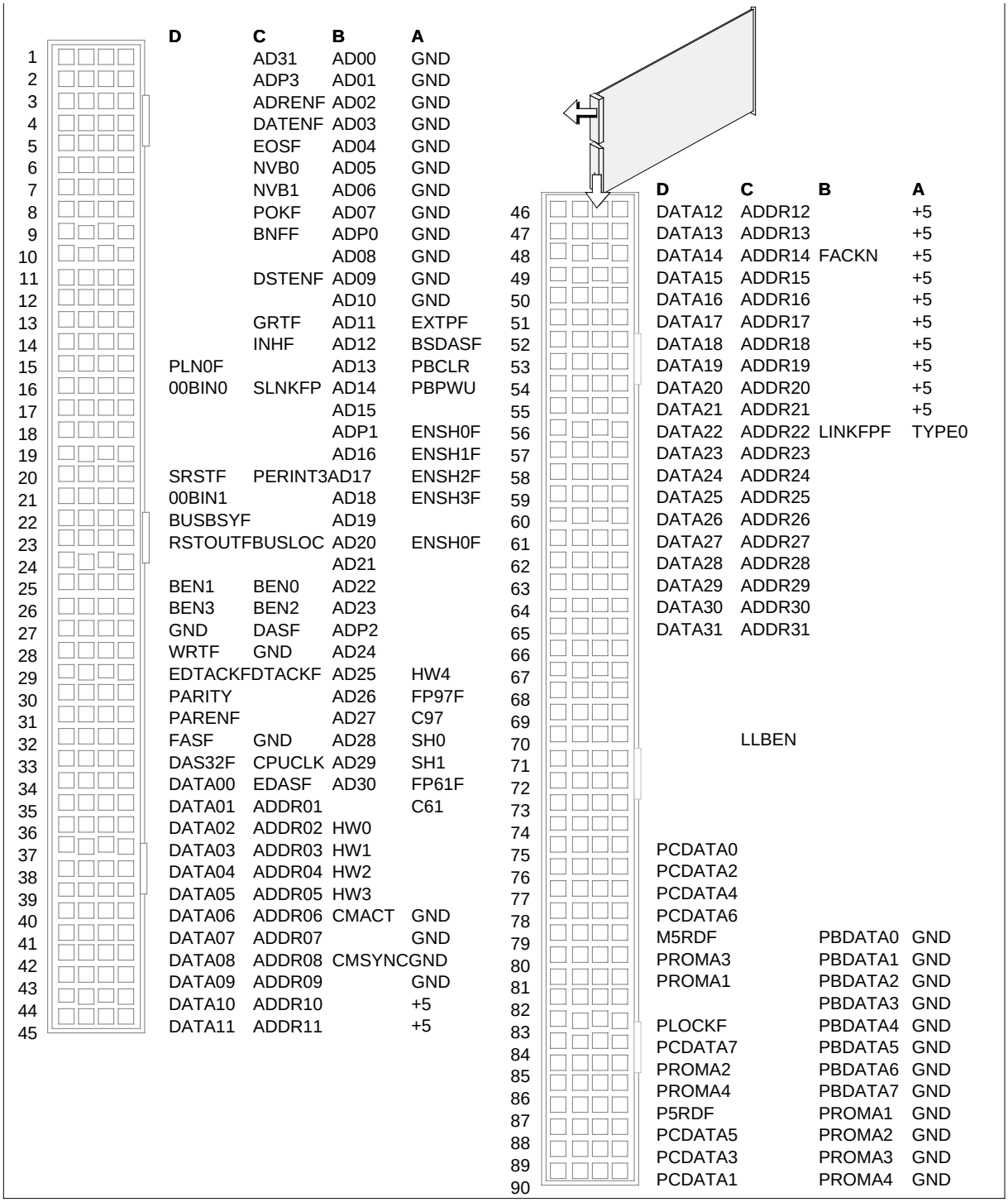
The normal power requirements for the NT9X49CB are 6.8 A from a +5 V supply, with a maximum of 10 A from a +5 V supply.

Signaling

Pin numbers

The pin numbers for the NT9X49CB appear in the following figure.

NT9X49CB pin numbers



	D	C	B	A
1		AD31	AD00	GND
2		ADP3	AD01	GND
3		ADRENF	AD02	GND
4		DATENF	AD03	GND
5		EOSF	AD04	GND
6		NVB0	AD05	GND
7		NVB1	AD06	GND
8		POKF	AD07	GND
9		BNFF	ADP0	GND
10			AD08	GND
11		DSTENF	AD09	GND
12			AD10	GND
13		GRTF	AD11	EXTPF
14		INHF	AD12	BSDASF
15	PLN0F		AD13	PBCLR
16	00BIN0	SLNKFP	AD14	PBPWU
17			AD15	
18			ADP1	ENSH0F
19			AD16	ENSH1F
20	SRSTF	PERINT3	AD17	ENSH2F
21	00BIN1		AD18	ENSH3F
22	BUSBSYF		AD19	
23	RSTOUTF	BUSLOC	AD20	ENSH0F
24			AD21	
25	BEN1	BEN0	AD22	
26	BEN3	BEN2	AD23	
27	GND	DASF	ADP2	
28	WRTF	GND	AD24	
29	EDTACKF	DTACKF	AD25	HW4
30	PARITY		AD26	FP97F
31	PARENF		AD27	C97
32	FASF	GND	AD28	SH0
33	DAS32F	CPUCLK	AD29	SH1
34	DATA00	EDASF	AD30	FP61F
35	DATA01	ADDR01		C61
36	DATA02	ADDR02	HW0	
37	DATA03	ADDR03	HW1	
38	DATA04	ADDR04	HW2	
39	DATA05	ADDR05	HW3	
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10		+5
45	DATA11	ADDR11		+5

	D	C	B	A
46	DATA12	ADDR12		+5
47	DATA13	ADDR13		+5
48	DATA14	ADDR14	FACKN	+5
49	DATA15	ADDR15		+5
50	DATA16	ADDR16		+5
51	DATA17	ADDR17		+5
52	DATA18	ADDR18		+5
53	DATA19	ADDR19		+5
54	DATA20	ADDR20		+5
55	DATA21	ADDR21		+5
56	DATA22	ADDR22	LINKFPF	TYPE0
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70		LLBEN		
71				
72				
73				
74				
75	PCDATA0			
76	PCDATA2			
77	PCDATA4			
78	PCDATA6			
79	M5RDF		PBDATA0	GND
80	PROMA3		PBDATA1	GND
81	PROMA1		PBDATA2	GND
82			PBDATA3	GND
83	PLOCKF		PBDATA4	GND
84	PCDATA7		PBDATA5	GND
85	PROMA2		PBDATA6	GND
86	PROMA4		PBDATA7	GND
87	P5RDF		PROMA1	GND
88	PCDATA5		PROMA2	GND
89	PCDATA3		PROMA3	GND
90	PCDATA1		PROMA4	GND

NT9X49CC

Product description

The NT9X49CC message switch (MS) processor-bus (P-bus) terminator circuit pack (CP) provides termination for message switch backplane tracks. The message switch processor (MSP) uses the message switch backplane tracks. Only SuperNode SE configurations can use the NT9X49CC.

This pack provides a time-out on the MS transaction bus (T-bus). The time-out on the MS T-bus is longer for the NT9X49CC than for the NT9X49CA.

Location

The NT9X49CC is in slots 07 and 32 in the combined MS of SuperNode SE.

Functional description

The NT9X49CC MS P-bus terminator CP performs the following functions:

- provides signals to clear the T-bus when time-outs occur
- locks the power converters on an active MS
- provides access to identification (ID) PROMs on the NT9X30AA and NT9X31AA power converters (PC) on the combined MS. Provides ID PROMs on the CP.

The NT9X49CC message switch allows packets of information to pass between port cards. Other cards in the system provide clocks, additional memory, and connections to data links.

A processor card based on the 68020 microprocessor supervises the configuration and maintenance of the cards in an MS. The processor card communicates with cards in the MS over the P-bus. The length and speed of the P-bus requires termination resistors to be present at one end of the bus. The termination resistors reduce the amplitude of reflections on backplane signals.

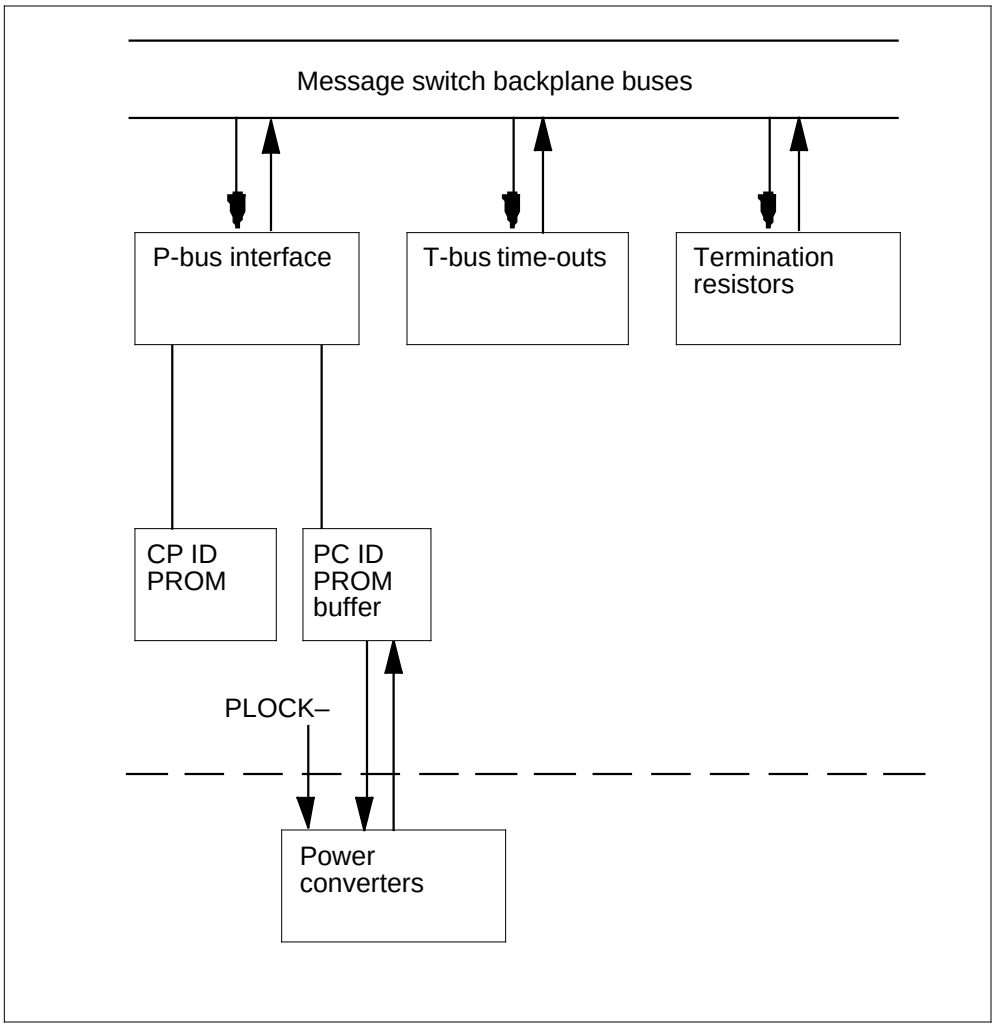
Functional blocks

The NT9X49CC has the following functional blocks:

- P-bus interface
- T-bus time-outs
- termination resistors
- CP ID PROM
- PC ID PROM buffer
- PLOCK

The relationship between the functional blocks appears in the following figure.

NT9X49CC functional blocks



Processor bus interface

The MS processor can access the P-bus interface directly. The processor supervises the card for maintenance and configuration status.

Transaction bus time-outs

Processor interrupt signals notify the MS processor of the time-out condition on the T-bus. Other signals on this block monitor activity on the T-bus.

Termination resistors

Termination resistors terminate signals that include transistor-transistor-logic (TTL) backplane signals associated with the P-bus.

NT9X49CC (continued)

Circuit pack identification PROM

The MS processor reads the CP ID PROM to identify the CP ID and vintage information.

Power converter identification PROM buffer

The MS processor reads the PC ID PROM buffer to access PC ID PROMs.

PLOCK

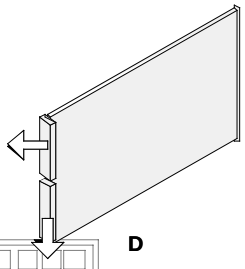
When the system asserts the PLOCK signal, the associated power converters cannot switch off.

Signaling

Pin numbers

The pin numbers for the NT9X49CC appear in the following figure.

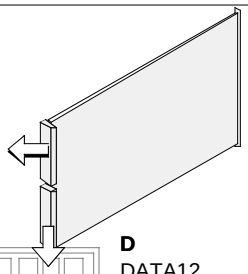
NT9X49CC pin numbers (Part 1 of 2)



	D	C	B	A
1				GND
2				GND
3		ADREN–		GND
4		DATEN–		GND
5				GND
6				GND
7				GND
8		POK–		GND
9		BNF–		GND
10				GND
11		DSTEN–		GND
12				GND
13		GRT–		EXTP–
14		INH–		SDAS–
15	PLN0–			PBCLR
16	OOB-IN0	SLNKFP–		PBPWUP
17				
18				ENSH0
19				ENSH1–
20	SRST–			ENSH2–
21	OOB-IN1			ENSH3–
22	BUSBSY–			
23		BUSLOCK–		PEXTEN–
24				
25	BEN1–	BEN0–		
26	BEN3–	BEN2–		
27	LDS	DAS–	DAS–	
28	WRT–	UDS		
29		DTACK–		HW4
30	PARITY+			FP97–
31	PARITYEN–			C97
32	FAS–	SE		SH0
33	DAS32–	CPUCLK+		SH1
34	DATA00	EDAS–	EDAS–	FP61–
35	DATA01	ADDR01		C61
36	DATA02	ADDR02	HW0	–5V
37	DATA03	ADDR03	HW1	–5V
38	DATA04	ADDR04	HW2	–5V
39	DATA05	ADDR05	HW3	–5V
40	DATA06	ADDR06	CMACT	GND
41	DATA07	ADDR07		GND
42	DATA08	ADDR08	CMSYNC	GND
43	DATA09	ADDR09		GND
44	DATA10	ADDR10		+5V
45	DATA11	ADDR11		+5V

NT9X49CC (continued)

NT9X49CC pin numbers (Part 2 of 2)



	D	C	B	A
46	DATA12	ADDR12		+5V
47	DATA13	ADDR13		+5V
48	DATA14	ADDR14	FACKN	+5V
49	DATA15	ADDR15		+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21		+5V
56	DATA22	ADDR22	LINKFP–	TYPE0
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70		LLBEN		
71				
72				
73				
74				
75	PCDAT0			
76	PCDAT2			
77	PCDAT4			
78	PCDAT6			
79	PCPROMM–			PBDAT0
80	PCADD3			PBDAT1
81	PCADD1			PBDAT2
82				PBDAT3
83	PLOCK–			PBDAT4
84	PCDAT7			PBDAT5
85	PCADD2			PBDAT6
86	PCADD4			PBDAT7
87	PCPROMP–			PBADD1
88	PCDAT5			PBADD2
89	PCDAT3			PBADD3
90	PCDAT1			PBADD4

Technical data

Power requirements

The NT9X49CC uses a supply voltage of +5.00 V (±0.25 V) and a supply current of 3 A.

NT9X52AA

Product description

The NT9X52AA message switch processor (MSP) transaction bus (T–bus) access card provides the interface between the MSP and the T–bus in the MSP. This interface allows the MSP to use links that connect to the message switch to transmit and receive messages. The message switch passes packets of information between links that connect to the following:

- the imput/output controller (IOC)
- the network
- the computing module
- the peripherals

Location

The NT9X52AA fits in slot 7 (hard–wired slot 1) of the NT9X40AA message switch backplane. The NT9X52AA must be in the same shelf as the MSP, shelf 00.

Functional description

The NT9X52AA performs the following functions in the message switch:

- interfaces the processor bus (P–bus) with the T–bus. This function allows the MSP to receive and transmit messages on the T–bus.
- generates and verifies cyclic redundancy checks (CRC) for T–bus messages that the MSP sends and receives
- allows address replacements during the T–bus address cycle. This function permits message loopbacks to be performed on port cards
- terminating transitor–transitor (TTL) backplane signals that associate with the T–bus
- provides part of the T–bus intershelf arbitration logic. The remainder of the T–bus intershelf arbitration logic is on the NT9X24AA T–bus extender paddle board.
- buffers clock signals that the NT9X53AA generates
- provides an interface to control the T–bus extender card
- provides access to the identification (ID) PROMs on the NT9X24AA, the NT9X30AA, the NT9X31AA and the card
- locks the power converters on an active message switch

Functional blocks

The NT9X52AA has the following functional blocks:

- P–bus interface
- intershelf arbitration
- termination resistors
- T–bus interface
- clock buffers
- NT9X24 paddle board control
- paddle board ID PROM buffer
- bus access circuit (BAC)
- card maintenance unit (CMU)
- receive first–in first–out (FIFO) memory
- PCs ID PROM buffer
- CP ID PROM
- CRC state machine
- transmit buffer memory
- loopback register

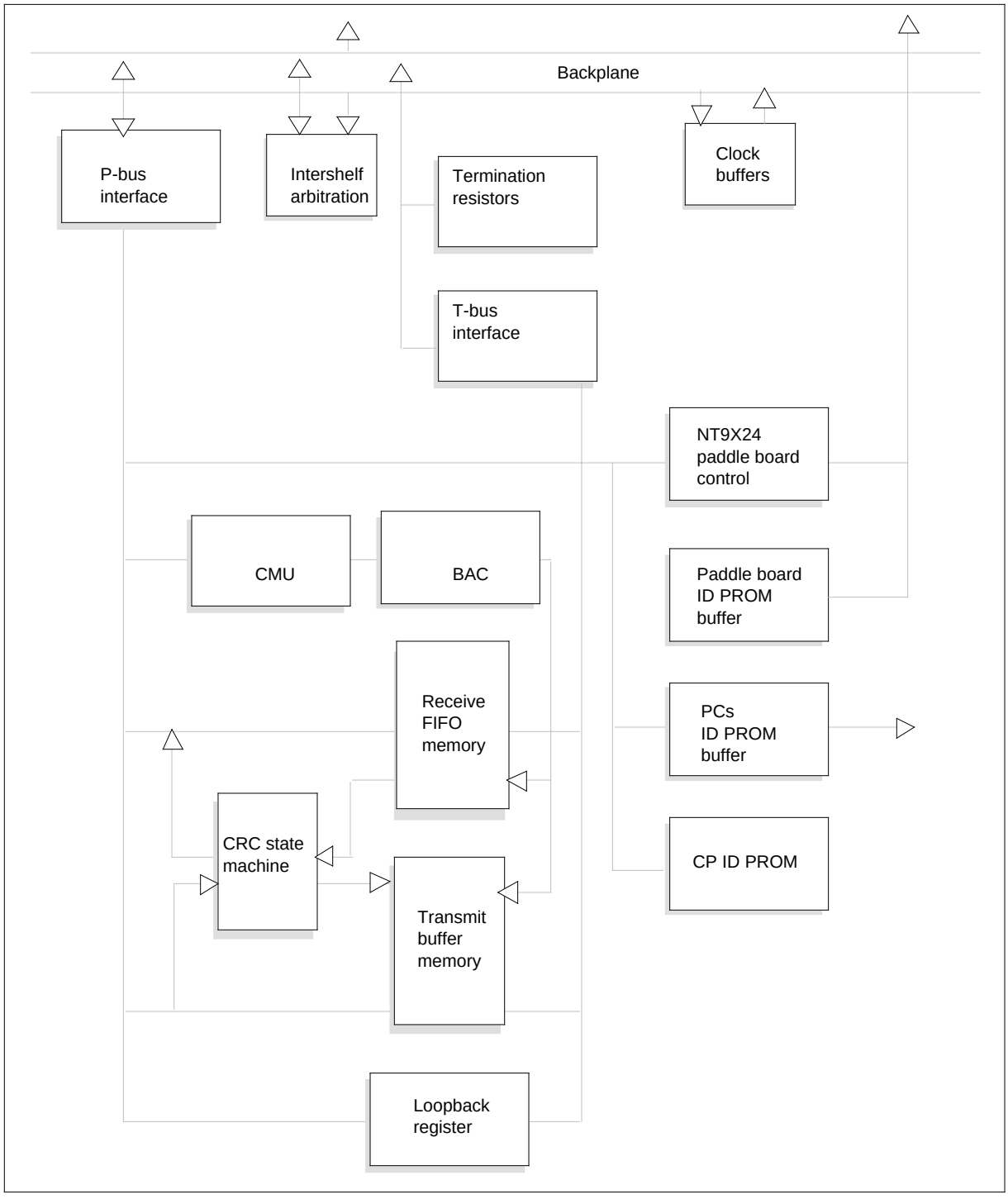
The P–bus to T–bus interface on the NT9X52 allows the MSP to communicate with another system node like the CM. This communication takes place through the T–bus and a DS30 or DS512 link. Data from the MSP is presented to the buffer and BAC. This data is presented with use of the same control signals that accompany data from a link handler in an NT9X17AA. Signals control data flow from the FIFO. These signals are the same signals that control data that goes to a link handler in an NT9X17AA.

Data that travels from the P–bus to the T–bus goes through a buffer. This buffer can hold a single message of a maximum of 2 Kbytes or 512 longwords in length. Data that travels from the T–bus to the P–bus goes through the FIFO. The FIFO can store a number of messages if the combined storage required is not greater than 16 Kbytes or 4096 longwords. The BAC gate array handles control of the buffer, the FIFO and access to the T–bus.

The relationship between these functional blocks appears in the following figure.

NT9X52AA (continued)

NT9X52AA functional blocks



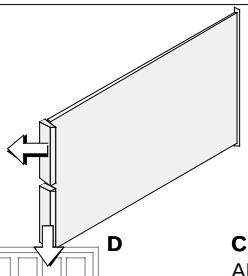
Signaling

Pin numbers

The pin numbers for the NT9X52AA appear in the following figure.

NT9X52AA (continued)

NT9X52AA pin numbers



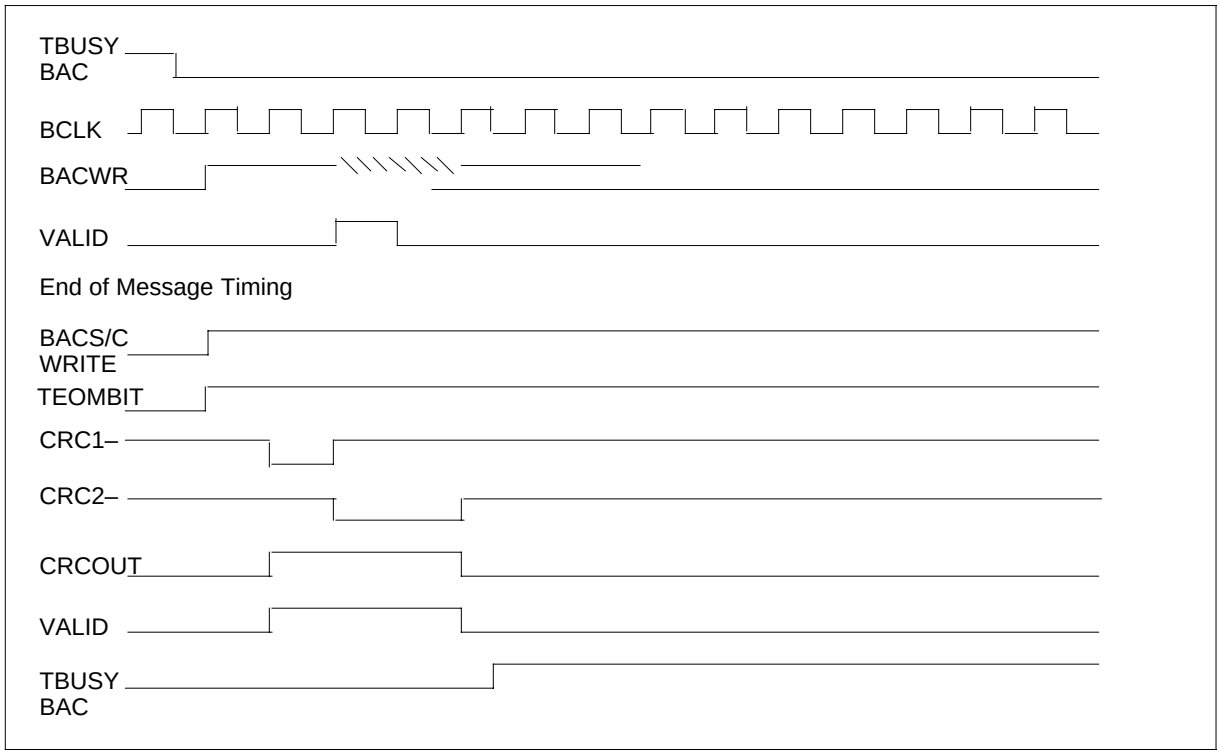
	D	C	B	A
1	IP0	AD37	ADD00	GND
2	OP0	ADP3	ADD01	GND
3	IP1	ADREN–	ADD02	GND
4	OP1	DATEN–	ADD03	GND
5	IP3	EOS–	ADD04	GND
6	OP2	NVB0	ADD05	GND
7		NVB1	ADD06	GND
8	OP3	POK–	ADD07	GND
9	SEG0	BNF–	ADP0	GND
10	SEG1	SRCEN–	ADD10	GND
11	SEG2	DSTEN–	ADD11	GND
12	SEG3	REQ–	ADD12	GND
13	SEG4	GRT–	ADD13	EXTP–
14		INH–	ADD14	PLNKDCTL
15			ADD15	PBCLR
16		SLNKFP–	ADD16	PBPWUP
17			ADD17	
18			ADP1	REQ
19			ADD20	PBUSY
20			ADD21	GSEG0
21		PERINT4–	ADD22	GSEG1
22			ADD23	
23			ADD24	TEXTEN
24	PERINT1–	PERINT0–	ADD25	
25	BEN1–	BEN0–	ADD26	
26	BEN3–	BEN2–	ADD27	STRPSH0
27			ADP2	STRPSH1
28	WRT–		ADD30	
29		DTACK–	ADD31	HW4
30	PARITY+		ADD32	FP97–
31	PARITYEN–		ADD33	C97
32			ADD34	SH0
33	DAS32–		ADD35	SH1
34			ADD36	FP61–
35				C61
36		ADDR02	HW0	–5
37		ADDR03	HW1	–5
38		ADDR04	HW2	–5
39		ADDR05	HW3	–5
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5
45		ADDR11		+5

	D	C	B	A
46		ADDR12		+5
47		ADDR13		+5
48		ADDR14		+5
49		ADDR15		+5
50	DATA16	ADDR16		+5
51	DATA17	ADDR17		+5
52	DATA18	ADDR18		+5
53	DATA19	ADDR19		+5
54	DATA20	ADDR20		+5
55	DATA21	ADDR21		+5
56	DATA22	ADDR22	LINKFP–	
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70				
71				
72				UBFP97–
73				
74				UBFP61–
75	PCDAT0			
76	PCDAT2			UBC97
77	PCDAT4			
78	PCDAT6			UBC61
79	PCPROMM–		PBDAT0	GND
80	PCADD3		PBDAT1	GND
81	PCADD1		PBDAT2	GND
82			PBDAT3	GND
83	PLOCK–		PBDAT4	GND
84	PCDAT7		PBDAT5	GND
85	PCADD2		PBDAT6	GND
86	PCADD4		PBDAT7	GND
87	PCPROMP–		PBADD1	GND
88	PCDAT5		PBADD2	GND
89	PCDAT3		PBADD3	GND
90	PCDAT1		PBADD4	GND

Timing

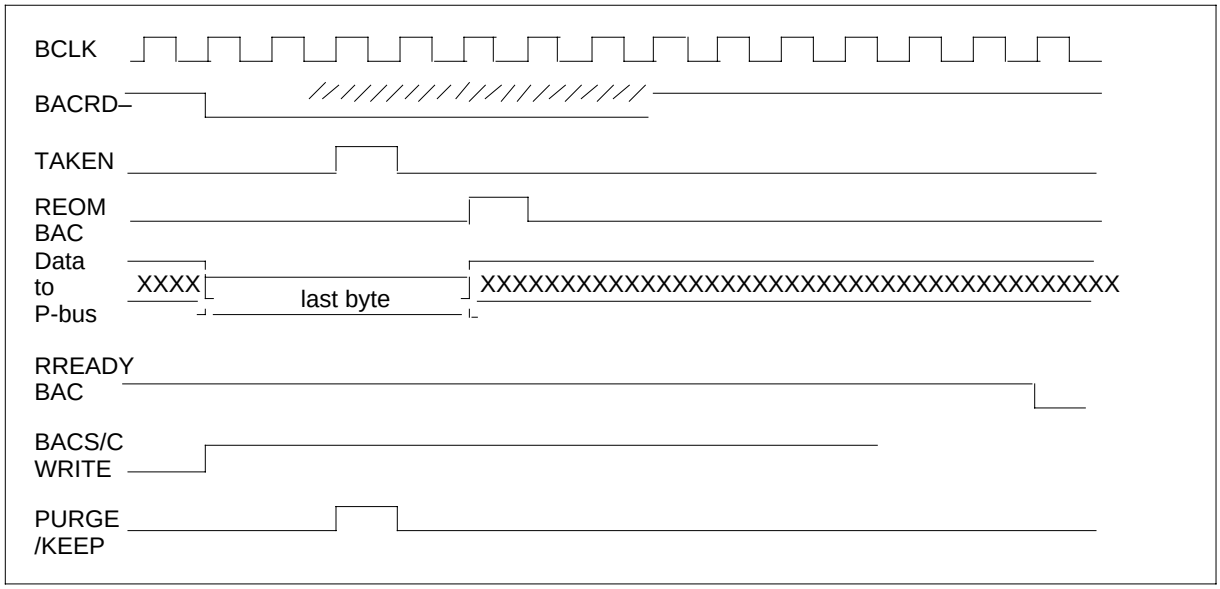
The timing for the NT9X52AA appears in the following figure.

NT9X52AA P–bus to buffer data transfer timing

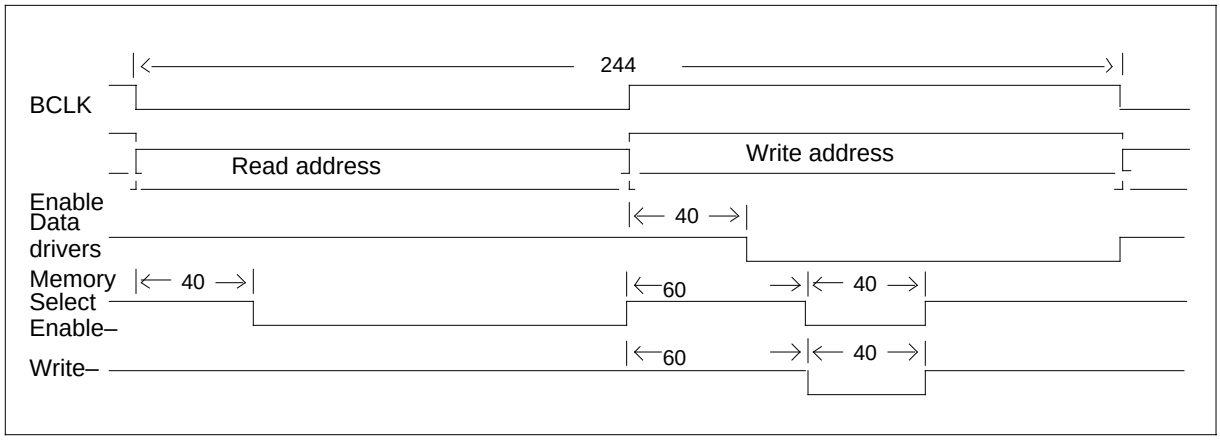


NT9X52AA (end)

NT9X52AA FIFO to P–bus data transfer timing



NT9X52AA FIFO to P–bus data transfer timing



Technical data

Power requirements

The NT9X52AA requires 20 W of power.

NT9X53AA

Product description

The NT9X53AA message switch system clock card generates accurate timing signals from two digital phase-locked loops (DPLL). These loops use Stratum 3 oscillators. With a remote clock, the DPLL can use a Stratum 2 or 2.5 oscillator. The DPLLs generate clock signals and 8-kHz frame pulse signals.

The clock card can lock on a highly accurate external clock source, like a Stratum 1 (cesium) oscillator.

Location

The NT9X53AA clock card occupies a slot on the message switch (MS).

Functional description

The NT9X53AA provides timing signals for the MS. The NT9X53AA generates timing information. This information is in the form of a 10.240-MHz clock, a 16.384-MHz clock and frame pulses. The card uses two phase-locked loops (PLL) to lock these oscillators to one of a number of reference sources.

Functional blocks

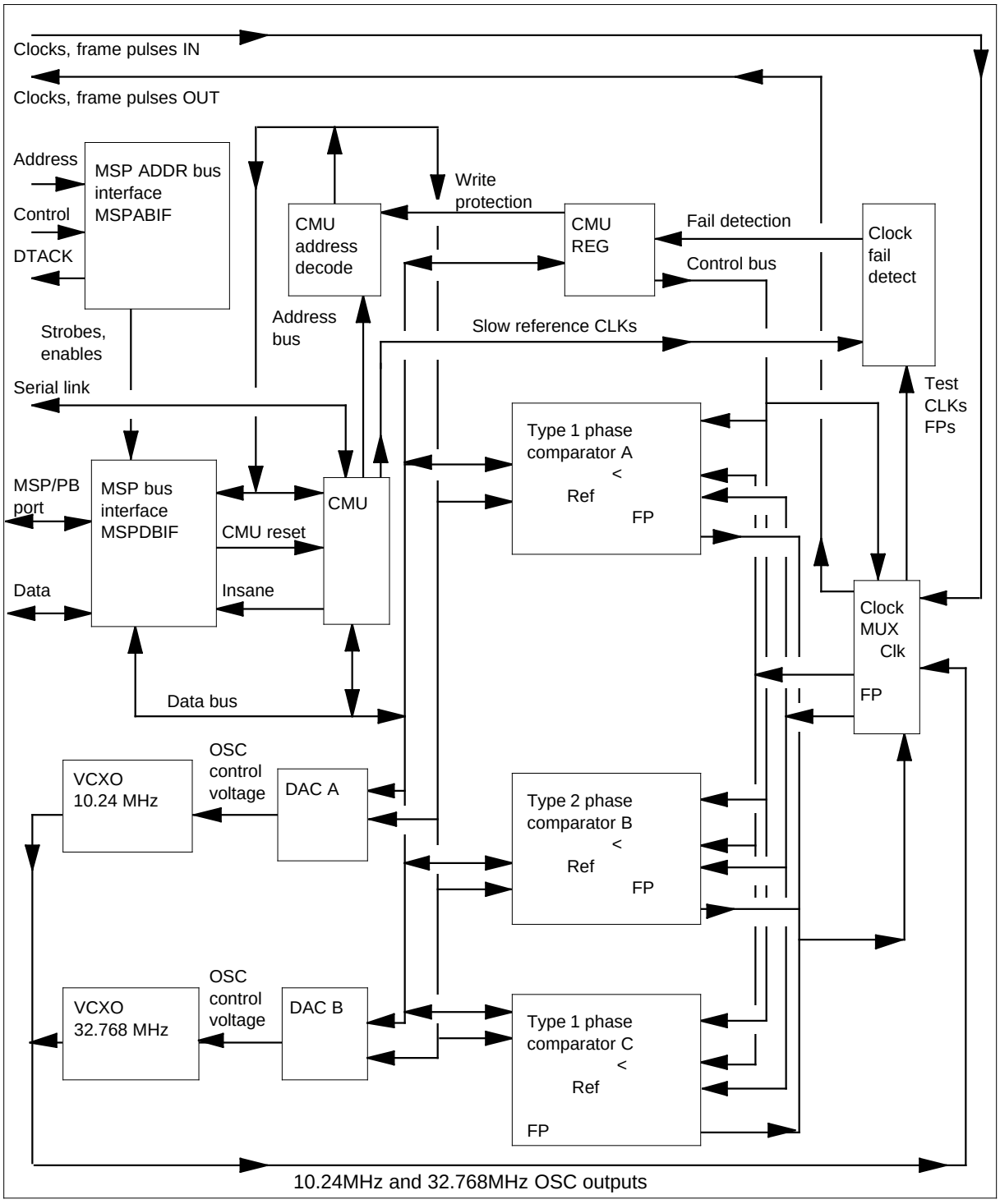
The NT9X53AA has the following functional blocks:

- card maintenance unit (CMU)
- CMU address decoders
- message switch processor (MSP) address bus interface
- MSP data bus interface
- CMU registers
- phase comparator 1
- phase comparator 2
- digital-to-analog converter (DAC) block
- voltage-controlled crystal oscillators (VCXO)
- clock fail detect block
- clock multiplexer (MUX) block

The relationship between these functional blocks appears in the following figure.

NT9X53AA (continued)

NT9X53AA functional blocks



Card maintenance unit

The CMU has an 8031 microprocessor, RAM and EPROM. The 8031 has an integrated serial interface to a remote clock. The serial link output can loop back to the input for diagnostics.

A 12-MHz clock generates a clock for the CPU.

The CMU resets the sanity timer as the timer executes the firmware of the CNU. If the CMU does not reset the sanity timer, the CMU sends a signal to the MSP data bus interface.

The CMU contains a power-up reset circuit that resets the CMU.

Card maintenance unit address decoders

The CMU address decoder generates the strobes or enables other blocks necessary for data bus transfers with the CMU. The decoder enforces write protection of registers when the corresponding write protection bits are set.

Message switch processor address bus interface

The MSP address bus interface decodes addresses that the MSP generates. The MSP decodes these addresses in to strobes or enables for the registers in the MSP data bus interface. The interface generates handshake signals for the MSP bus.

Message switch processor data bus interface

The MSP interface contains registers that interact with the MSP data bus. The MSP generates data bus parity for bus transactions.

Card maintenance unit registers

The CMU registers contain the CMU-accessible registers. These registers are not in the MSP data bus interface, phase comparator or DAC blocks. The CMU registers provide an interface between the CMU data bus and the different control or state points of this board.

Phase comparator 1

There are two phase 1 comparators on the card. Each phase comparator divides an input clock down through a counter chain to generate an 8-kHz frame pulse. The counter loads a preset value from a CMU-accessible register. The counter counts up to 0 and reloads the value and the cycle repeats. Each reload generates a frame pulse.

NT9X53AA (continued)

Phase comparator 2

This block is functionally identical to phase comparator 1, except this block provides a different clock output. The clock output of this block is one-half the frequency of the input clock.

Digital-to-analog converter block

The DAC block supplies the voltage-controlled crystal oscillators with control voltage. The control voltage adjusts the frequency of these oscillators. Each block contains a 12-bit DAC, dc-to-dc converter and power failure detection circuits. The dc-to-dc converter generates the required supply voltages ±15 V and regulated +5V. The power failure detection circuits determines if the converter shave fails.

Voltage-controlled crystal oscillators

The two VCXOs oscillate with center frequencies of 10.240 MHz and 32.768 MHz. The DAC control voltage can pull these frequencies from center. The 32.768-MHz clock divides by two to create the 16.384-MHz clock signal the system requires.

Clock fail detect block

The clock fail detect block monitors clock and frame pulse signals on the card.

Clock multiplexer block

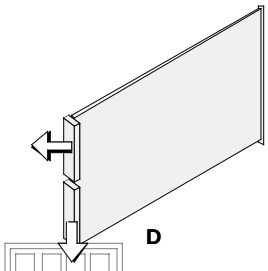
The clock MUX block routes the clocks and reference frame pulses to each of the three phase comparators. This block contains many fault insertion points. This block provides buffering of the clocks and frame pulses to the backplane and from the backplane.

Signaling

Pin numbers

The pin numbers for the NT9X53AA appear in the following figure.

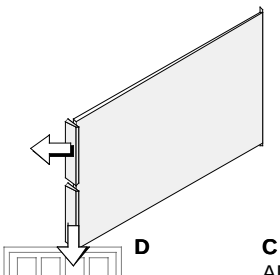
NT9X53AA pin numbers (Part 1 of 2)



	D	C	B	A
1				GND
2				GND
3				GND
4				GND
5				GND
6				GND
7				GND
8				GND
9				GND
10				GND
11				GND
12				GND
13				PRC97–
14				PRFP97–
15				ST2TXD
16		SLINKFP–		
17				MATEFPI–
18				ST2RSET
19				PRREFA
20				BITSOUT
21		PERINT4–		
22				ST2BACT–
23				STRAT2
24				ST2RXD
25	BEN1–	BEN0–		MATEFPO–
26	BEN3–	BEN2–		TOMTFPD–
27				PBREGWR
28	WRT–			PBREGRD–
29		DTACK–		HW4
30	PARITY			FP97–
31	PARITYEN–			C97
32				SH0
33	DA32–			SH1
34				FP61–
35				C61
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06	CMACT–	
41		ADDR07		
42		ADDR08		
43		ADDR09		
44		ADDR10		+5 V
45		ADDR11	INT4–	+5 V

NT9X53AA (continued)

NT9X53AA pin numbers (Part 2 of 2)



	D	C	B	A
46		ADDR12		+5 V
47		ADDR13		+5 V
48		ADDR14		+5 V
49		ADDR15		+5 V
50	DATA16	ADDR16		+5 V
51	DATA17	ADDR17		+5 V
52	DATA18	ADDR18		+5 V
53	DATA19	ADDR19		+5 V
54	DATA20	ADDR20		+5 V
55	DATA21	ADDR21		+5 V
56	DATA22	ADDR22	PLINKFP–	
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70				
71				
72			UBFP97–	
73				
74			UBFP61–	
75				
76			UBC97	
77				
78			UBC61	
79	CS/RB/LC		PBDATA0	GND
80			PBDATA1	GND
81	SYNCFP–		PBDATA2	GND
82			PBDATA3	GND
83	PRC61		PBDATA4	GND
84	PRFP61–		PBDATA5	GND
85	PRPLFP–		PBDATA6	GND
86	PREXTFP–		PBDATA7	GND
87	PBPROMR–		PBADDR1	GND
88	EXREF		PBADDR2	GND
89			PBADDR3	GND
90			PBADDR4	GND

Technical data

Power requirements

The power requirements for NT9X53AA appear in the following table.

Power requirements for NT9X53AA

Supply	Minimum	Normal	Maximum
Supply voltage (V)	4.75	5.00	5.25
Supply ripple (mV)			25
Supply current (A)			5 (estimate)

NT9X53AB

Product description

The NT9X53AB SuperNode clock card generates accurate timing signals from two digital phase-locked loops (DPLL). These loops use Stratum 3 oscillators. With a remote clock, one of the DPLLs can use a Stratum 2 or 2.5 oscillator. The DPLLs generate clock signals and 8-kHz frame pulse signals.

The clock card can lock on a highly accurate external clock source, like a Stratum 1 (Cesium) oscillator.

Location

The NT9X53AB clock card occupies a slot on the message switch. This slot is one of the main subsystems of the DMS SuperNode.

Functional description

The NT9X53AB provides timing signals for the message switch (MS). The NT9X53AB generates timing information. This information takes the form of 10.240-MHz and 16.384-MHz clocks and frame pulses. The card uses two phase-locked loops to lock these oscillators to one reference sources.

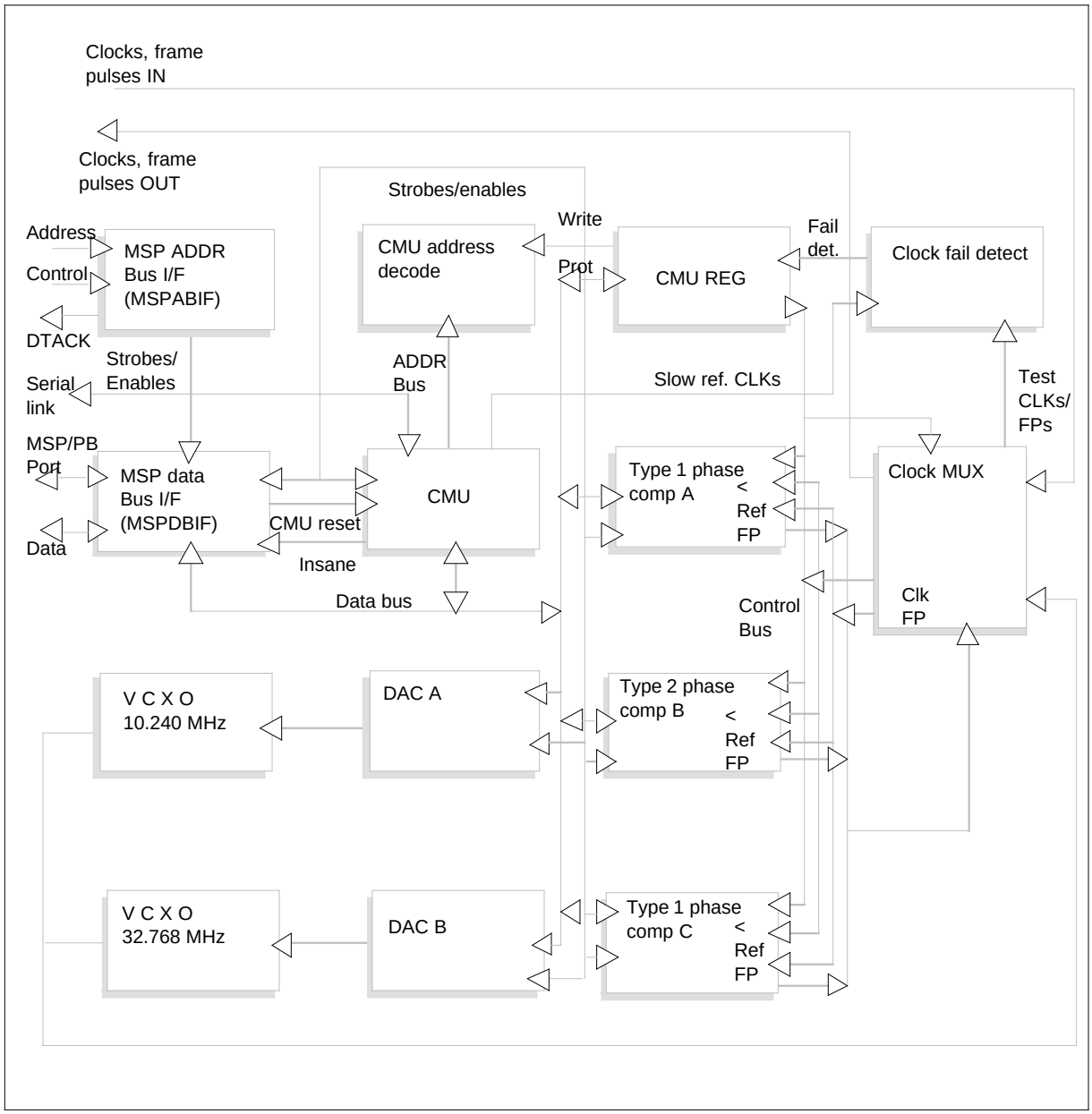
Functional blocks

The NT9X53AB has the following functional blocks:

- card maintenance unit (CMU)
- CMU address decoders
- message switch processor (MSP) address bus interface
- MSP data bus interface
- CMU registers
- phase comparator 1
- phase comparator 2
- digital-to-analog converters (DAC)
- voltage-controlled crystal oscillators (VCXO)
- clock fail detect
- clock multiplexer

The functional relationship of these blocks appear in the following figure.

NT9X53AB functional blocks



Card maintenance unit

The CMU contains an 8031 microprocessor, RAM and EPROM. The 8031 has an integrated serial interface to a remote clock. The serial link output can loop back to the input for diagnostics.

NT9X53AB (continued)

A 12-MHz clock generates a clock for the CPU. This 12-MHz clock divides for use on other areas of the card.

The CMU resets the sanity timer as the timer executes the firmware of the timer. If the CMU does not reset the sanity timer, the CMU sends a signal to the MSP data bus interface.

The CMU contains a power-up reset circuit that resets the CMU.

Card maintenance unit address decoders

The CMU address decoder generates the strobes and enables that other blocks require for data bus transfers with the CMU. The decoder enforces write protection of fixed registers when write-protection bits that correspond are set.

Message switch processor address bus interface

The MSP address bus interface decodes addresses that the MSP generates. The interface decodes the addresses in to strobes and enables for the registers in the MSP data bus interface. The interface generates handshake signals for the MSP bus.

Message switch processor data bus interface

This block contains registers that interact with the MSP data bus. This block generates data bus parity for bus transactions.

Card maintenance unit registers

The CMU registers contain the CMU accessible registers that are not in the MSP data bus interface, phase comparator or DAC blocks. The CMU registers provide an interface between the CMU data bus and the different control and state points of this board.

Phase comparator 1

Three identical phase comparators are available on the card. Each phase comparator takes an input clock and divides the clock through a counter chain. This action generates an 8 kHz frame pulse. The counter loads in a preset value from a CMU accessible register. The counter counts to a maximum of 0. The counter reloads the value and the cycle repeats. Each reload generates a frame pulse.

Phase comparator 2

This block is functionally identical to phase comparator 1, except that this block provides a clock output. The output of this clock is one-half the frequency of the input clock.

Dialog-to-analog converters

The DACs supply the voltage-controlled crystal oscillators with the control voltages. The control voltages adjust the frequency of the voltage-controlled crystal oscillators. Each block contains a 12-bit dc-to-dc converter and power failure detection circuits. The dc-to-dc converter generates the required supply voltages (±15V). The power failure detection circuits determines if the converters fail.

Voltage-controlled crystal oscillators

The two VCXOs oscillate with center frequencies of 10.240 MHz and 32.768 MHz. The DAC control voltage can pull the VCXOs from center.

Clock fail detect

The clock fail detect block monitors different clock and frame pulse signals on the card.

Clock multiplexer

This block routes the clocks and reference frame pulses to each of the four phase comparators. This block contains many of the fault insertion points. This block provides buffering of the clocks and frame pulses to the backplane and from the backplane.

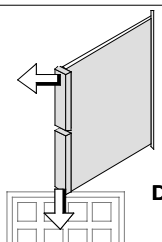
Signaling

Pin numbers

The pin numbers for NT9X53AB appear in the following figures.

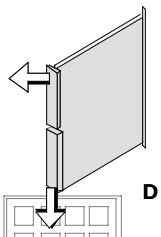
NT9X53AB (continued)

NT9X53AB pin numbers (Part 1 of 2)



	D	C	B	A
1				Gnd
2				Gnd
3				Gnd
4				Gnd
5				Gnd
6				Gnd
7				Gnd
8				Gnd
9				Gnd
10				Gnd
11				Gnd
12				Gnd
13				PRC97–
14				PRFP97–
15				ST2TXD
16	SLINKFP–			
17				MATEFPI–
18				ST2RSET
19				PRREFA
20				BITSOUT
21	PERINT4–			
22				ST2BACT–
23				STRAT2
24				ST2RXD
25	BEN1–	BEN0–		MATEFPO–
26	BEN3–	BEN2–		TOMTFPD–
27				PBREGWR
28	WRT–			PBREGRD–
29		DTACK–		HW4
30	PARITY			FP97–
31	PARITYEN–			C97
32				SH0–
33	DA32–			SH1
34				FP61–
35				C61
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06	CMACT–	
41		ADDR07		
42		ADDR08		
43		ADDR09		
44		ADDR10		+5V
45		ADDR11	INT4–	+5V

NT9X53AB pin numbers (Part 2 of 2)



	D	C	B	A
46		ADDR12		+5V
47		ADDR13		+5V
48		ADDR14		+5V
49		ADDR15		+5V
50	DATA16	ADDR16		+5V
51	DATA17	ADDR17		+5V
52	DATA18	ADDR18		+5V
53	DATA19	ADDR19		+5V
54	DATA20	ADDR20		+5V
55	DATA21	ADDR21		+5V
56	DATA22	ADDR22	PLINKFP–	
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70				
71				
72			UBFP97–	
73				
74			UBFP61–	
75				
76			UBC97	
77				
78			UBC61	
79	CS/RB/LC		PBDATA0	Gnd
80			PBDATA1	Gnd
81	SYNCFP–		PBDATA2	Gnd
82			PBDATA3	Gnd
83	PRC61		PBDATA4	Gnd
84	PRFP61–		PBDATA5	Gnd
85	PRPLFP–		PBDATA6	Gnd
86	PREXTFP–		PBDATA7	Gnd
87	PBPROMR–		PBADDR1	Gnd
88	EXREF		PBADDR2	Gnd
89			PBADDR3	Gnd
90			PBADDR4	Gnd

NT9X53AB (end)

Technical data

Power requirements

The power requirements for NT9X53AB appear in the following table.

Power requirements for NT9X53AB

Supply	Minimum	Normal	Maximum
Supply voltage (V)	4.75	5.00	5.25
Supply ripple (mV)			25
Supply current (A)			5 (estimate)

NT9X53AC

Product description

The NT9X53AC generates accurate timing signals from two digital phase-locked loops (DPLL). The two DPLL use Stratum 3 oscillators. With a remote clock, one DPLL can use a Stratum 2 or 2.5 oscillator. The DPLLs generate clock signals and 8-kHz frame pulse signals.

The NT9X53AC can lock on a highly accurate external clock source, like a Stratum 1 (Cesium) oscillator.

Location

The NT9X53AC occupies a slot on the message switch (MS).

Functional description

The NT9X53AC provides timing signals for the MS. The timing information generated takes the form of 10.240 MHz and 16.384 MHz clocks and frame pulses. The card uses two phase-locked loops to lock these oscillators to one of several reference sources.

Functional blocks

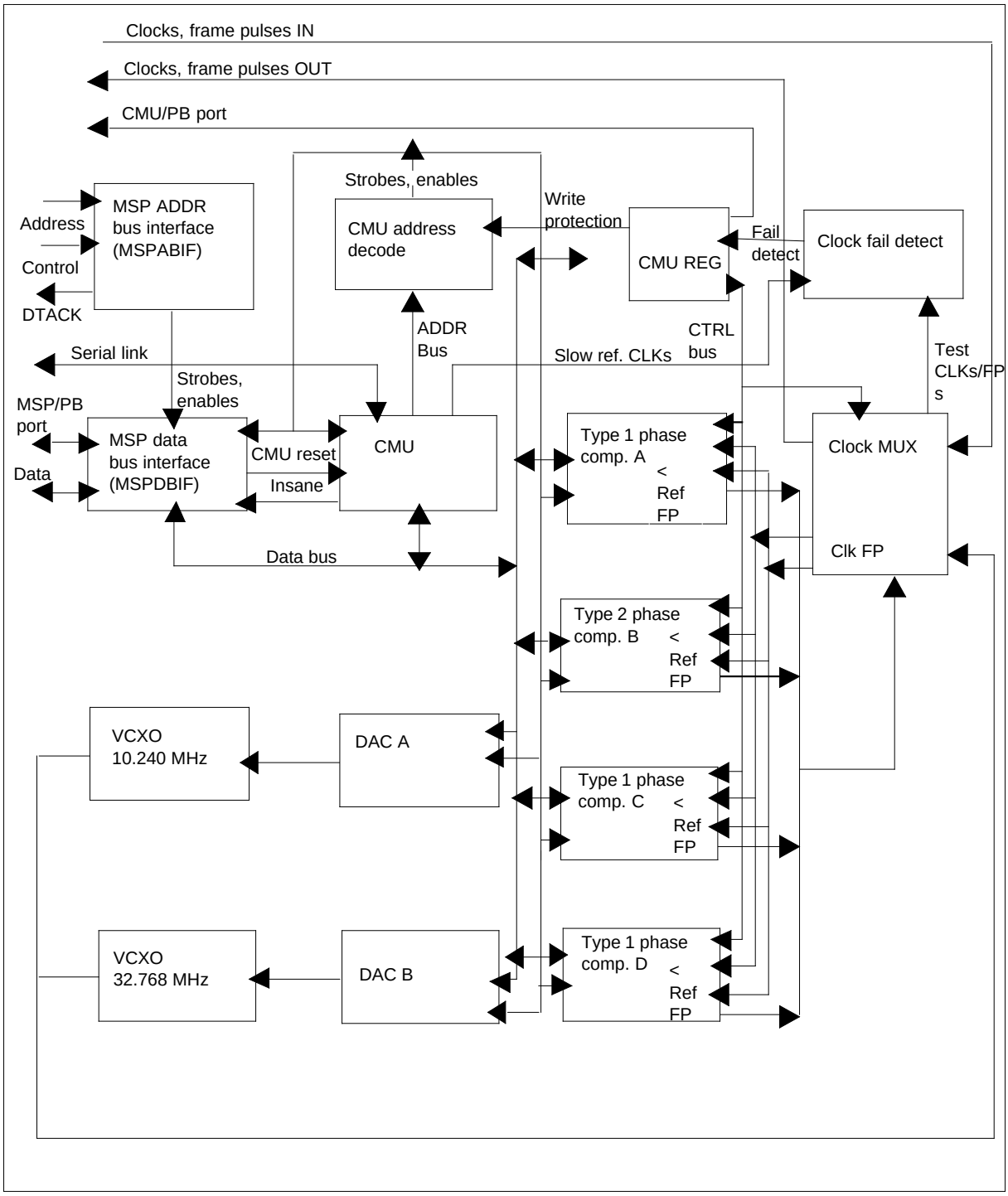
The NT9X53AC has the following functional blocks:

- card maintenance unit (CMU)
- CMU address decoders
- message switch processor (MSP) address bus interface
- MSP data bus interface
- CMU registers
- phase comparator 1
- phase comparator 2
- digital-to-analog converters (DAC)
- voltage controlled crystal oscillators (VCXO)
- clock fail detect
- clock multiplexer

The functional relationship of these blocks appears in the following figure.

NT9X53AC (continued)

NT9X53AC functional blocks



Card maintenance unit

The CMU has an 8031 microprocessor, RAM, an erasable programmable read-only memory (EPROM) and an EEPROM. The 8031 microprocessor has a built-in serial interface to a remote clock. The serial link output can loop back to the input for diagnostics.

A 12 MHz clock generates a clock for the CPU. This 12 MHz clock divides for use on other places on the card.

The CMU resets the sanity timer as the timer executes the firmware. If the CMU does not reset the sanity timer. The CMU asserts a signal to the MSP data bus interface.

The CMU contains a power-up reset circuit. This circuit resets the CMU.

Card maintenance unit address decoder

The CMU address decoder generates the strobes and enables. Other blocks need these strobes and enables for data bus transfers with the CMU. The decoder enforces write protection of certain registers when the corresponding write-protection bits are set.

Message switch processor address bus interface

The MSP address bus interface decodes addresses into strobes and enables for the registers in the MSP data bus interface. The MSP generates these addresses. The MSP address bus interface generates handshake signals for the MSP bus.

Message switch processor data bus interface

The MSP data bus interface contains the registers that interact with the MSP data bus. The MSP data bus generates data bus parity for bus transactions.

Card maintenance unit registers

The CMU registers contain the CMU accessible registers that are not in the MSP data bus interface, phase comparator or DAC blocks. The CMU registers provide an interface between the CMU data bus and the different control and state points of this board.

Phase comparator 1

Each of the three phase comparator 1s takes an input clock and divides the input clock down through a counter chain. This action generates an 8 kHz frame pulse. The counter loads in a preset value from a CMU accessible register, counts to a maximum of zero and reloads the value. The cycle repeats. Each reload generates a frame pulse.

NT9X53AC (continued)

An external reference frame pulse latches the value of the counter. This value represents the phase relationship between the input clocks frame pulse and the reference frame pulse. Latching the count makes the external reference frame pulse accessible to the microprocessor.

Phase comparator 2

Phase comparator 2 is functionally identical to phase comparator 1, except that phase comparator 2 provides a different clock output. This clock output is half the frequency of the input clock.

Digital-to-analog converters

The DACs supply the VCXOs with the control voltage. This voltage adjusts the frequency of the VCXO. Each block contains a 16-bit dc-to-dc converter to generate the required supply voltages (±15V). Each block has a a power failure detection circuitry. This circuitry determines if the converters fails.

Voltage controlled crystal oscillators

Two VCXOs oscillate with center frequencies of 10.240 MHz and 32.768 MHz. The DAC control voltage can pull the VCXO from center.

Clock fail detect

The clock fail detect block monitors different clock and frame pulse signals on the card.

Clock multiplexer

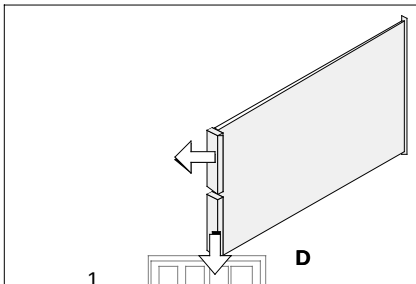
The clock multiplexer routes the clocks and reference frame pulses to each of the four phase comparators. The clock multiplexer contains many of the fault insertion points. This feature provides buffering of the clocks and frame pulses to and from the backplane.

Signaling

Pin numbers

The pin numbers for the NT9X53AC appear in the following figure.

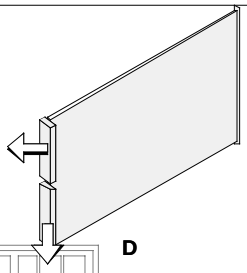
NT9X53AC pin numbers (Part 1 of 2)



	D	C	B	A
1			GND	
2			GND	
3			GND	
4			GND	
5			GND	
6			GND	
7			GND	
8			GND	
9			GND	
10			GND	
11			GND	
12			GND	
13			PRC97	
14			PRFP97–	
15			ST2TXD	
16		SLINKFP–		
17				MATEFPI–
18				ST2RESET
19				
20				BITSOUT
21		PERINT4–		
22				ST2BACT–
23				STRAT2
24				ST2RXD
25	BEN1–	BEN0–		MATEFPO–
26	BEN3–	BEN2–		TOMTFPD–
27				PBREGWR
28	WRT–			PBREGRD–
29	EDTACK–	DTACK–		HW4
30	PARITY			FP97–
31	PARITYEN			C97
32				SH0
33	DAS32–			SH1
34			FP61–	
35			C61	
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06	CMACT–	
41		ADDR07		
42		ADDR08		
43		ADDR09		
44		ADDR10		+5 V
45		ADDR11	INT4–	+5 V

NT9X53AC (continued)

NT9X53AC pin numbers (Part 2 of 2)



	D	C	B	A
46		ADDR12		+5 V
47		ADDR13		+5 V
48		ADDR14		+5 V
49		ADDR15		+5 V
50	DATA16	ADDR16		+5 V
51	DATA17	ADDR17		+5 V
52	DATA18	ADDR18		+5 V
53	DATA19	ADDR19		+5 V
54	DATA20	ADDR20		+5 V
55	DATA21	ADDR21		+5 V
56	DATA22	ADDR22	PLINKFP–	
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70				
71				
72			UBFP97–	
73				
74			UBFP61–	
75				
76			UBC97	
77				
78	CMUA0		UBC61	
79	CS/RB/LC		PBDATA0	
80	CMUADDR1		PBDATA1	GND
81	SYNCFP–		PBDATA2	GND
82	CMUADDR3		PBDATA3	GND
83	PRC61	CMUDATA0	PBDATA4	GND
84	PRFP61–	CMUDATA1	PBDATA5	GND
85	CMUADDR2	CMUDATA2	PBDATA6	GND
86	PREXTFP–	CMUDATA3	PBDATA7	GND
87	PBPROMR–	CMUDATA4	PBADDR1	GND
88	EXREF	CMUDATA5	PBADDR2	GND
89	PBCMURD–	CMUDATA6	PBADDR3	GND
90	PBCMUWR	CMUDATA7	PBADDR4	GND

Technical data

Power requirements

The power requirements for the NT9X53AC appear in the following table.

Power requirements for NT9X53AC

Supply	Minimum	Normal	Maximum
Supply voltage	4.74 V	5.00 V	5.25 V
Supply ripple			25 mV
Supply current		7.2 A	10 A (estimate)

NT9X53AD

Product description

The NT9X53AD generates accurate timing signals from a digital phase–locked loop (DPLL). The DPLL uses a dual frequency Stratum 3 oscillator. With a remote clock, the DPLL can use a Stratum 2 or 2.5 oscillator. The DPLL generates clock signals and 8 kHz frame pulse signals.

The NT9X53AD can lock on a highly accurate external clock source, like a Stratum 1 (Cesium) oscillator.

Location

The NT9X53AD occupies slot 2 on the message switch (MS).

Functional description

The NT9X53AD provides timing signals for the MS. The timing information generated is 10.240 MHz and 16.384 MHz clocks and frame pulses. The card uses one phase–locked loop to lock these clocks and frame pulses to one of several reference sources.

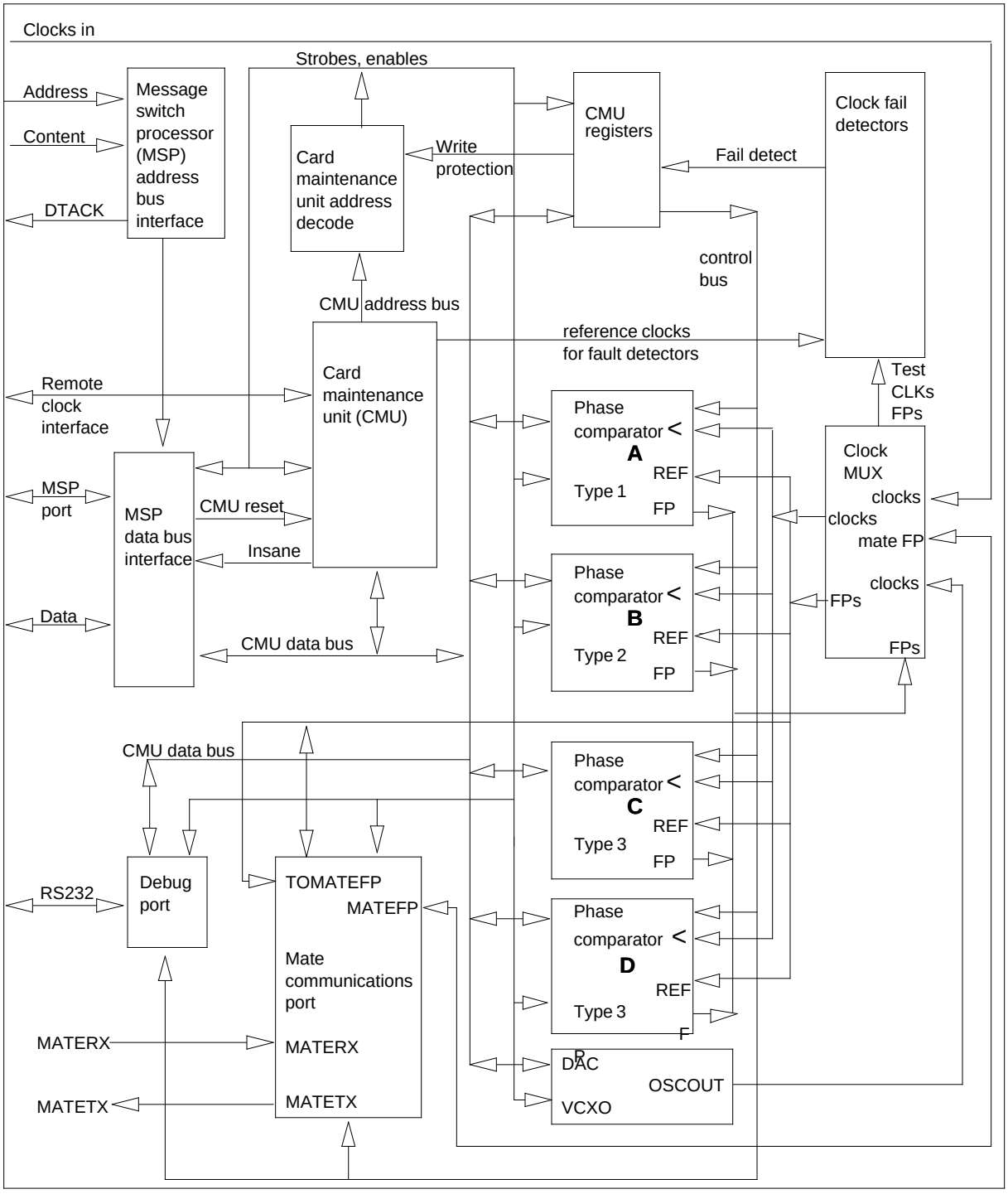
Functional blocks

The NT9X53AD contains the following functional blocks:

- card maintenance unit (CMU)
- CMU address decoders
- message switch processor (MSP) address bus interface
- MSP data bus interface
- CMU registers
- phase comparators (4)
- digital–to–analog converter (DAC)
- voltage controlled dual frequency crystal oscillator (VCXO)
- clock fail detect
- clock multiplexer
- mate communications port
- debug port

The functional relationship of these blocks appears in the following figure.

NT9X53AD functional blocks



NT9X53AD (continued)

Card maintenance unit

The CMU contains an 80C31 microprocessor, data RAM, erasable programmable read–only memory (EPROM) and program RAM. The 80C31 microprocessor has a built–in serial interface to a remote clock. The serial link output can loop back to the input for diagnostics.

A 12 MHz clock generates a clock for the CPU. The system divides the 12 MHz clock for use at other locations on the card.

The CMU resets the sanity timer as the timer executes the firmware of the timer. If the CMU does not reset the sanity timer, the timer sends a signal to the MSP data bus interface.

The CMU contains a power–up reset circuit that resets the CMU.

Card maintenance unit address decoder

The CMU address decoder generates the strobes. The CMU address decoder enables the strobes that other blocks require for data bus transfers with the CMU. The CMU address decoder enforces write protection of specified registers when the write–protection bits that correspond are set.

Message switch processor address bus interface

The MSP address bus interface decodes addresses that the MSP generates. The MSP address bus interface decodes addresses in to strobes and enables for the registers in the MSP data bus interface. The MSP address bus interface generates handshake signals for the MSP bus.

Message switch processor data bus interface

The MSP data bus interface contains all registers that interact with the MSP data bus. The system generates data bus parity for all bus transactions.

Card maintenance unit registers

The CMU registers contain the CMU accessible registers that are not in the following:

- the MSP data bus interface
- the phase comparator
- the DAC blocks

The CMU registers provide an interface between the CMU data bus and the various control and state points of this board.

Phase comparators

Each of the four phase comparators takes an input clock and divides the clock down through a counter chain. The comparators take this action to generate an 8 kHz frame pulse. The counter loads in a preset value from a CMU accessible register, counts to a maximum of FFF, and reloads the value. The cycle repeats. Each reload generates a frame pulse.

An external reference frame pulse latches the value of the counter. This value represents the phase relationship between the input clocks frame pulse and the reference frame pulse. The count is accessible to the microprocessor when the external pulse latches the count.

Digital–to–analog converter

The 16–bit DAC supplies the VCXO with the control voltage to adjust the frequency of the VCXO. This block contains 2 dc–to–dc converters to generate the required supply voltages. The converters are ±15V regulated and +5V. This block also contains a power failure detection circuitry to determine if failure occurred to other converters. This block also has a 12–bit analog–to–digital (A/D) converter used to detect DAC faults.

Voltage controlled dual frequency crystal oscillator

The VCXO oscillates with center frequencies of 10.240 MHz and 32.768 MHz. The DAC control voltage can pull the VCXO off center. The oscillator uses one internal crystal and multiplies and divides the frequency of the oscillator to get the two required frequencies. This action keeps the frequency relationship between the two outputs constant.

Clock fail detect

The clock fail detect block monitors different clock and frame pulse signals on the card.

Clock multiplexer

The clock multiplexer routes the clocks and reference frame pulses to each of the four phase comparators. The clock multiplexer contains many of the fault insertion points and provides buffers for the clocks and frame pulses to and from the backplane.

Mate communications port

The mate communications port supplies a messaging link between the clock cards in the two message switches. This link enables improved control between the clocks on the two message switches.

NT9X53AD (continued)

Debug port

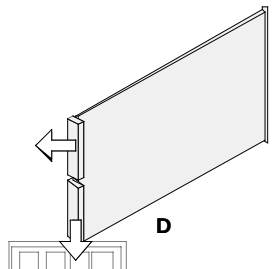
The debug port supplies an interface between the CMU and a VT100 type terminal. This interface allows external access to CMU registers and states. This interface contains an EEPROM that stores fault information for use by Northern Telecom. Northern Telecom uses this information to diagnose problems if the user returns the card. The factory does not install the debug interface.

Signaling

Pin numbers

The pin numbers for the appear in the following figures.

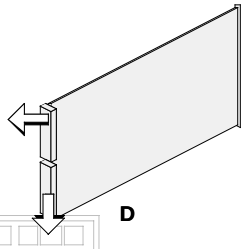
NT9X53AD pin numbers (Part 1 of 2)



	D	C	B	A
1				GND
2				GND
3				GND
4				GND
5				GND
6				GND
7				GND
8				GND
9				GND
10				GND
11				GND
12				GND
13				PRC97
14				PRFP97–
15				ST2TXD
16		SLINKFP–		
17				MATEFPI–
18				ST2RESET
19				
20				BITSOUT
21		PERINT4–		
22				ST2BACT–
23				STRAT2
24				ST2RXD
25	BEN1–	BEN0–		MATEFPO–
26	BEN3–	BEN2–		TOMTFPD–
27				PBREGWR
28	WRT–	PBREGRD–		
29	EDTACK–	DTACK–		HW4
30	PARITY			FP97–
31	PARITYEN			C97
32				SH0
33	DAS32–			SH1
34				FP61–
35				C61
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06	CMACT–	
41		ADDR07		
42		ADDR08		
43		ADDR09		
44		ADDR10		+5 V
45		ADDR11	INT4–	+5 V

NT9X53AD (continued)

NT9X53AD pin numbers (Part 2 of 2)



	D	C	B	A
46		ADDR12		+5 V
47		ADDR13		+5 V
48		ADDR14		+5 V
49		ADDR15		+5 V
50	DATA16	ADDR16		+5 V
51	DATA17	ADDR17		+5 V
52	DATA18	ADDR18		+5 V
53	DATA19	ADDR19		+5 V
54	DATA20	ADDR20		+5 V
55	DATA21	ADDR21		+5 V
56	DATA22	ADDR22	PLINKFP–	
57	DATA23	ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70				
71				
72			UBFP97–	
73				
74			UBFP61–	
75				
76			UBC97	
77				
78	CMUA0		UBC61	
79	CS/RB/LC		PBDATA0	
80	CMUADDR1		PBDATA1	GND
81	SYNCFP–		PBDATA2	GND
82	CMUADDR3		PBDATA3	GND
83	PRC61	CMUDATA0	PBDATA4	GND
84	PRFP61–	CMUDATA1	PBDATA5	GND
85	CMUADDR2	CMUDATA2	PBDATA6	GND
86	PREXTFP–	CMUDATA3	PBDATA7	GND
87	PBPROMR–	CMUDATA4	PBADDR1	GND
88	EXREF	CMUDATA5	PBADDR2	GND
89	PBCMURD–	CMUDATA6	PBADDR3	GND
90	PBCMUWR	CMUDATA7	PBADDR4	GND

Technical data

Power requirements

The power requirements for the NT9X53AD appear in the following table.

Power requirements for NT9X53AD

Supply	Minimum	Normal	Maximum
Supply voltage	4.74V	5V	5.25V
Supply ripple			25mV
Supply current		5.4A (6.0A during warm–up)	10A (estimate)

NT9X54AA

Product description

The NT9X54AA DMS-bus clock interface paddle board provides external cable connections for the NT9X53AA card (MS clock).

Location

The NT9X54AA resides in the DMS-bus, behind the NT9X53AA MS clock card. The NT9X54AA provides external cable connections for the NT9X53AA card.

Functional description

Functional blocks

The NT9X54AA contains the following blocks:

- stratum 1 interface
- stratum 2/2.5 interface
- mate interface
- monitor interface
- NT9X53AA data interface

Stratum 1 interface

The stratum 1 clock signal is input to the NT9X54AA paddle board through faceplate jack J1. A 50-ohm or 75-ohm termination terminates this signal on the paddle board. Three different types of clock signals can be input to J1. Each different clock type signal passes through receiver circuits. The system sends two different transitor-transitor logic (TTL) signals to the NT9X53AA. A frame pulse reference signal can be input to the NT9X54AA through jack J1. Circuits on the paddle board receives this signal. The circuits sends this signal as a TTL signal (SYNCFP-) to the NT9X53AA.

Stratum 2/2.5 interface

The stratum 2/2.5 interface contains the following signal groups:

- control signals that include the following:
  - — data signals
  - — reset signals
  - — activity signals
  - — power interlock signals
- clock signals that include the following:
  - — a 10.24 MHz sinewave clock signal from the NT3X16AA (stratum 2 oscillator)
  - — A 10.24 MHz squarewave clock signal from the NT3X16BA card (stratum 2.5 oscillator)

Mate interface

The DMATEFP-,+ is a differential frame pulse signal received from the mate DMS-bus. The system converts the signal to TTL levels and sends the signal to the NT9X53AA as MATEFP-. The NT9X53AA sends TOMATEFP-, a TTL level signal, to the NT9X54AA. The NT9X54AA converts to a differential signal, TOMATEFP-,+. The system sends this signal to the mate DMS-bus where the signal is received as signal DMATEFP-,+.

Monitor interface

Signal monitor outputs are available from connector P3, connector P2, and jack J3.

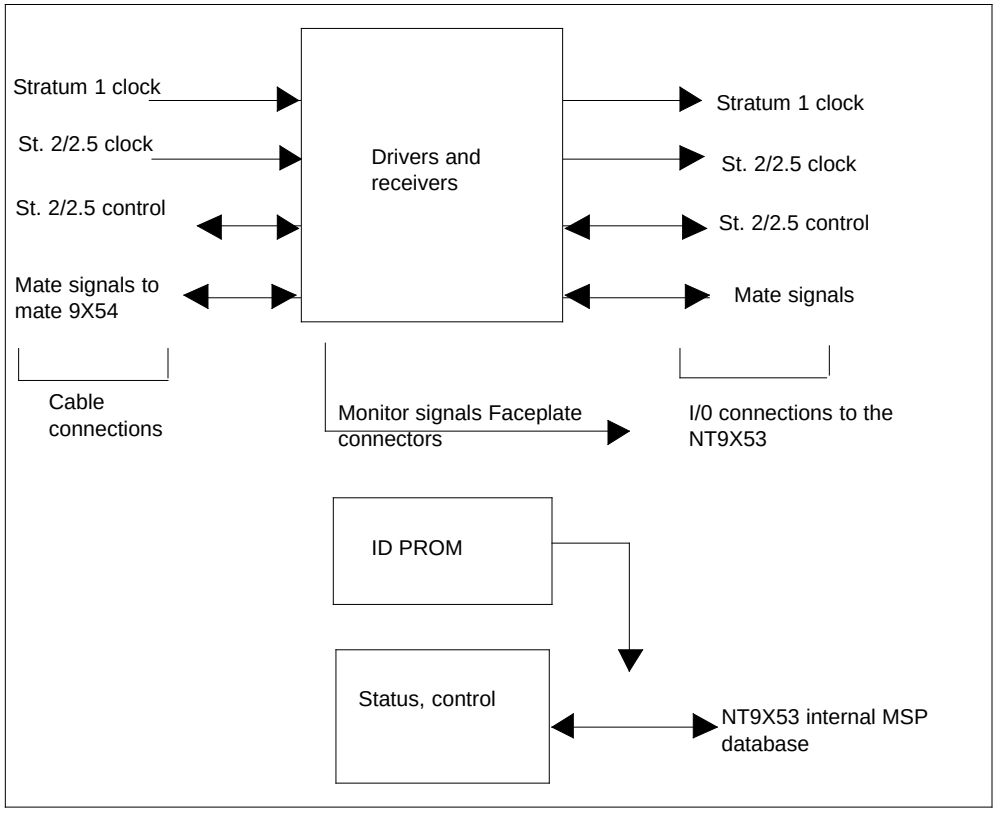
NT9X53AA data interface

The NT9X53AA data interface contains the state/control interface and the identification (ID) PROM interface. Access to these interfaces occurs through the processor bus (P-bus) interface of the NT9X53AA card.

The relationship between the functional blocks appears in the following figure.

NT9X54AA (continued)

NT9X54AA functional blocks

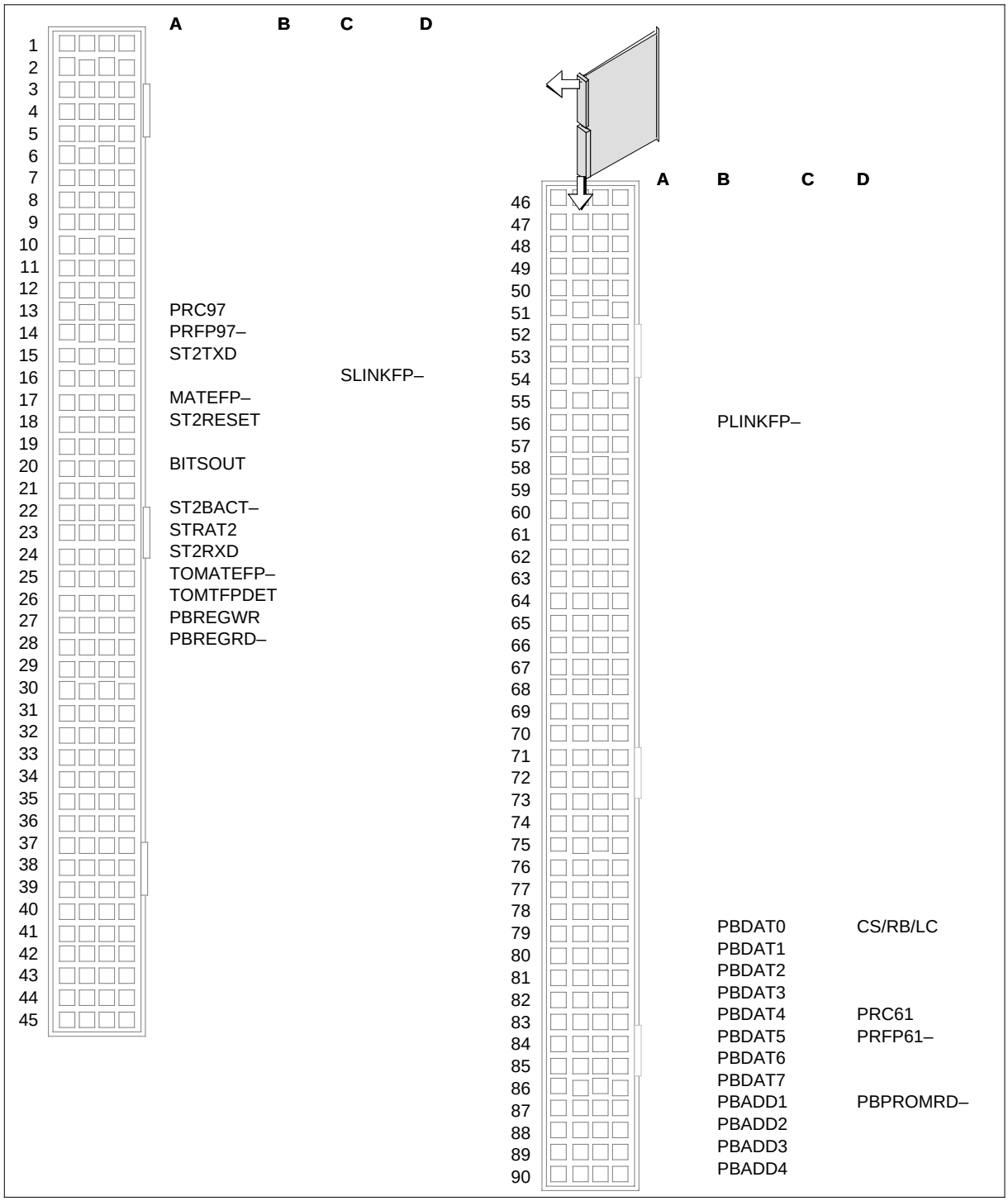


Signaling

Pin numbers

The pin numbers for NT9X54AA connector P1 appear in the following figure.

NT9X54AA connector P1 pin numbers



NT9X54AA (end)

The pin numbers for connectors J1 and J2 appear in the following tables.

NT9X54AA connector J1 pin number signals

Pin	Signal	Pin	Signal
1	ST2RXD+	14	ALM0
2	ST2RXD-	20	ST2RESET+
3	CLKINTLKA	21	ST2RESET-
4	ST2TXD+	22	ST2BACT-
5	ST2TXD-	23	CLKINTLKB
8	TOMATEFP+	26	DMATEFP+
9	TOMATEFP-	27	DMATEFP-
12	BITS+	32	ALM1
13	BITS-	36	MRFBACT-

NT9X54AA connector J2 pin number signals

Pin	Signal	Pin	Signal
1	PRC97	6	PREXTFP-
2	PRFP97-	7	MATEFP-
3	PRC61	8	BSLINKFP-
4	PRFP61-	9	BSTRAT2
5	BPLINKFP-		

Technical data

Power requirements

The NT9X54AA requires a nominal value of 5V, with a minimum of 4.75V and a maximum of 5.25V.

NT9X54AC

Product description

The NT9X54AC external clock interface paddle board provides the correct interfaces. The NT9X54AC provides interfaces to convert remote and external analog reference signals. The signals are at transistor–transistor logic (TTL) levels acceptable to the system clock circuit card.

The NT9X54AC uses the standard common features for DMS–bus paddle boards.

Location

The NT9X54AC is used in a SuperNode switch and resides in the DMS–bus behind the system clock card.

Functional description

The NT9X54AC provides the following:

- a mate interface
- a clock–frame pulse monitor interface
- a P–bus accessed status and control interface
- an element identification (ID) PROM interface

The card provides remote control cable connections to the remote input–output equipment frame

Functional blocks

The NT9X54AC consists of the following functional blocks:

- external clock interface
- remote interface
- mate interface
- monitor interface
- data interface
- power interrupt detector
- signal level detectors

NT9X54AC (continued)

External clock interface

Three different types of external clock signals can be input to the NT9X54AC:

- cesium, rubidium clock source
- Loran C
- composite clock source for North America

Remote interface

The cesium, rubidium and Loran C interfaces use the coaxial connector on the faceplate. The composite clock source interface uses two pins on the 37–pin faceplate connector (J1). The remote interface consists of control and clock signals. The control signals leave the SuperNode bulkhead connector (J1) to go to the remote clock shelf (NT3X95). The remote clock shelf is in the input/output equipment (IOE) frame (NT0X43AD). The remote clock shelf can contain stratum 2 or stratum 2.5 cards. The requirement determines the card that is present.

When SuperNode requires a remote clock, the clock cards must be intersystem–ground (ISG) compatible. The NT9X54AC is an ISG–compliant paddle board.

The card to shelf compatibilities for the J1 connector appear in the following table.

Card–shelf compatibility

Card	Remote clock shelf	Compatibility
Stratum 2	NT3X16AA CP in NT3X95AA shelf NT3X16AB CP in NT3X95AB shelf	not ISG compatible ISG compatible
Stratum 2.5	NT3X16BA CP in TX3X95BA shelf NT3X16BB CP in NT3X95BB shelf	not ISG compatible ISG compatible

The pin numbers for the J1 connector appear in the following table.

J1 connector pin numbers (Sheet 1 of 2)

Pin	Signal
1	ST2RXD+
2	ST2RXD-
3	CLKINTLKA

J1 connector pin numbers (Sheet 2 of 2)

Pin	Signal
4	ST2TXD+
5	ST2TXD-
8	TOMATEFP+
9	TOMATEFP-
12	BITS+
13	BITS-
14	ALM0
20	ST2RESET+
21	ST2RESET-
22	ST2BACT-
23	CLKINTLKB
26	DMATEFP+
27	DMATEFP-
32	ALM1
36	MRFBACT-

Mate interface

The mate interface receives a differential TTL frame pulse signal from the mate DMS–bus. The system sends the signal single–ended to the NT9X53 card (MS clock) as MATEFP-.

Monitor interface

The monitor interface provides outputs for access by the NT9X54 and NT9X53 cards. The NT9X54 and the NT9X53 cards are accessed through

NT9X54AC (continued)

connector J2, a 9–pin D–type small connector. The J2 connector pin numbers appear in the following table.

J2 connector pin numbers

Pin	Signal
1	PRC97
2	PRFP97-
3	PRC61
4	PRFP61-
5	BPLINKFP-
6	PREXTFP-
7	MATEFP-
8	BSLINKFP-
9	BSTRAT2

Data interface

The NT9X53 data interface contains the following hardware elements:

- status–control interface, accessed through the P–bus interface of the NT9X53 central processor
- ID PROM interface, accessed through the P–bus interface of the NT9X53 central processor

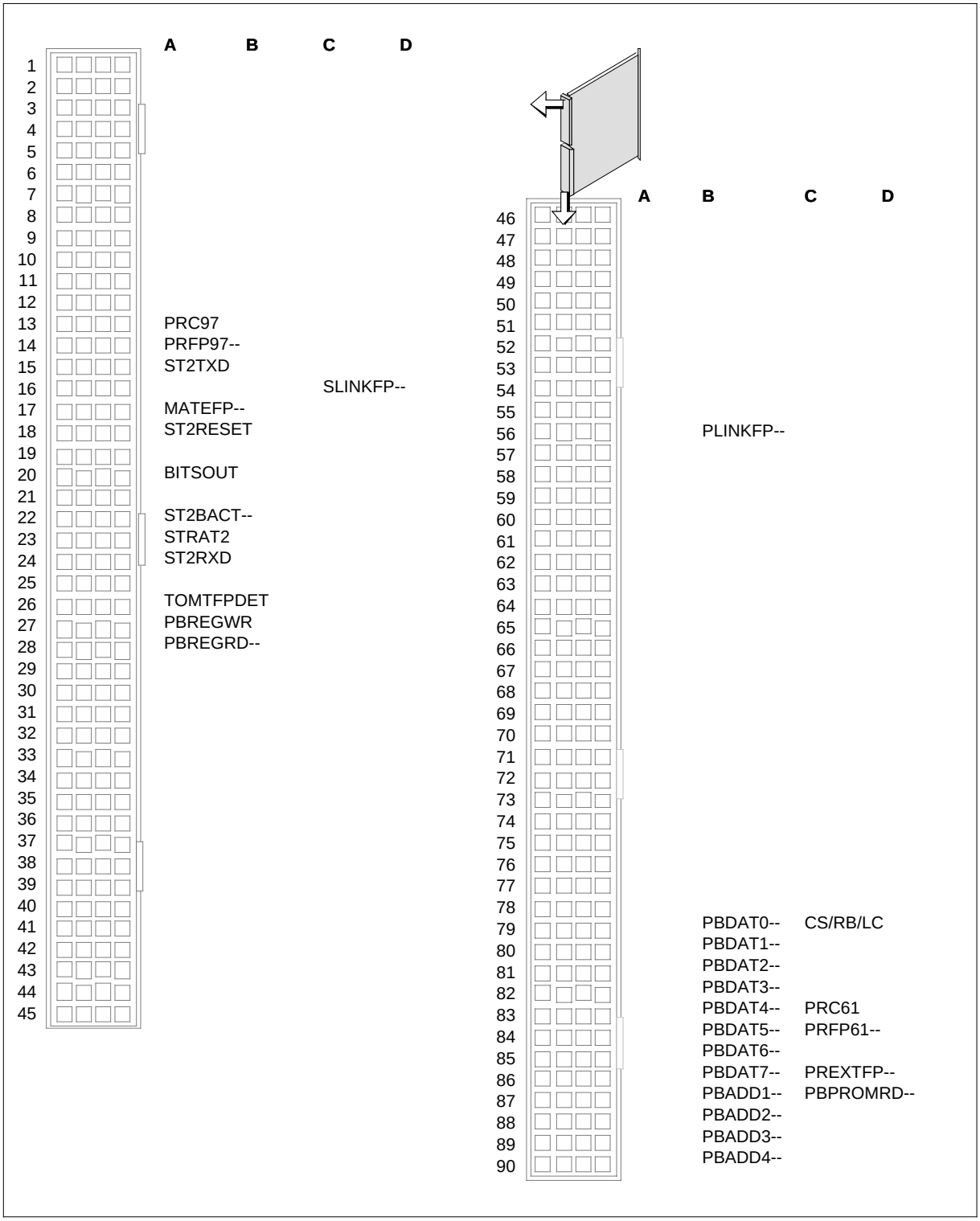
Signaling

Pin numbers

The pin numbers for the NT9X54AC appear in the following figure.

NT9X54AC (continued)

NT9X54AC pin numbers



NT9X54AC (end)

Technical data

Power requirements

The power requirements for appear in the following table.

Power requirements for NT9X54AC

Supply	Minimum	Normal	Maximum
Supply voltage (V)	4.75	5	5.25
Supply ripple (V)			0.1 peak–to–peak

Product description

The NT9X54AD paddle board provides the correct interfaces to convert remote and external analog reference signals to transistor–transistor logic (TTL) levels. The system clock circuit card considers these levels as acceptable. The NT9X54AD uses the standard common features for DMS–bus paddle boards.

Location

The NT9X54AD is used in a SuperNode switch and resides in the DMS–bus. The NT9X54AD is behind the system clock card.

Functional description

The NT9X54AD provides the following:

- a mate interface
- a clock–frame pulse monitor interface
- a P–bus accessed status
- a control interface
- an element identification (ID) PROM interface
- remote control cable connections to the remote input–output equipment frame (NT0X43AD)

Functional blocks

The NT9X54AD contains the following functional blocks:

- external clock interface
- remote interface
- mate interface
- monitor interface
- data interface
- power interrupt detector
- signal level detectors

External clock interface

Three different types of external clock signals can be input to the NT9X54AD:

- cesium, rubidium clock source
- Loran C
- digital clock source (DCS) for Japan (composite clock)

NT9X54AD (continued)

Remote interface

The cesium/rubidium and Loran C interfaces use the coaxial connector on the faceplate. The DCS interface uses two pins on the 37–pin faceplate connector (J1). The remote interface contains control and clock signals. The control signals leave the SuperNode bulkhead connector (J1) to go to the remote clock shelf (NT3X95). The remote clock shelf is in the input/output equipment (IOE) frame (NT0X43AD). This shelf can contain stratum 2 or stratum 2.5 cards. The requirement determines the card that is present.

When SuperNode requires a remote clock, the clock cards must be intersystem–ground (ISG) compatible. The NT9X54AD is an ISG–compliant paddle board.

The card to shelf compatibilities appear in the following table.

Card–shelf compatibility

Card	Remote clock shelf	Compatibility
Stratum 2	NT3X16AA CP in NT3X95AA shelf NT3X16AB CP in NT3X95AB shelf	non–ISG compatible ISG compatible
Stratum 2.5	NT3X16BA CP in TX3X95BA shelf NT3X16BB CP in NT3X95BB shelf	non–ISG compatible ISG compatible

The pin numbers for the J1 connector appear in the following table.

J1 connector pin numbers (Sheet 1 of 2)

Pin	Signal
1	ST2RXD+
2	ST2RXD-
3	CLKINTLKA
4	ST2TXD+
5	ST2TXD-
8	TOMATEFP+
9	TOMATEFP-
12	BITS+
13	BITS-

J1 connector pin numbers (Sheet 2 of 2)

Pin	Signal
14	ALM0
20	ST2RESET+
21	ST2RESET-
22	ST2BACT-
23	CLKINTLKB
26	DMATEFP+
27	DMATEFP-
32	ALM1
36	MRFBACT-

Mate interface

The mate interface receives a differential TTL frame pulse signal from the mate DMS–bus. The system sends the signal single–ended to the NT9X53 card (MS clock) as MATEFP-.

Monitor interface

The monitor interface provides outputs for access by the NT9X54 and NT9X53 cards. The user can access NT9X54 and NT9X53 through connector J2, a 9–pin D–type small connector. The J2 connector pin–number appear in the following table.

J2 connector pin numbers (Sheet 1 of 2)

Pin	Signal
1	PRC97
2	PRFP97-
3	PRC61
4	PRFP61-
5	BPLINKFP-
6	PREXTFP-
7	MATEFP-

NT9X54AD (continued)

J2 connector pin numbers (Sheet 2 of 2)

Pin	Signal
8	BSLINKFP-
9	BSTRAT2

Data interface

The NT9X53 data interface contains the following hardware elements:

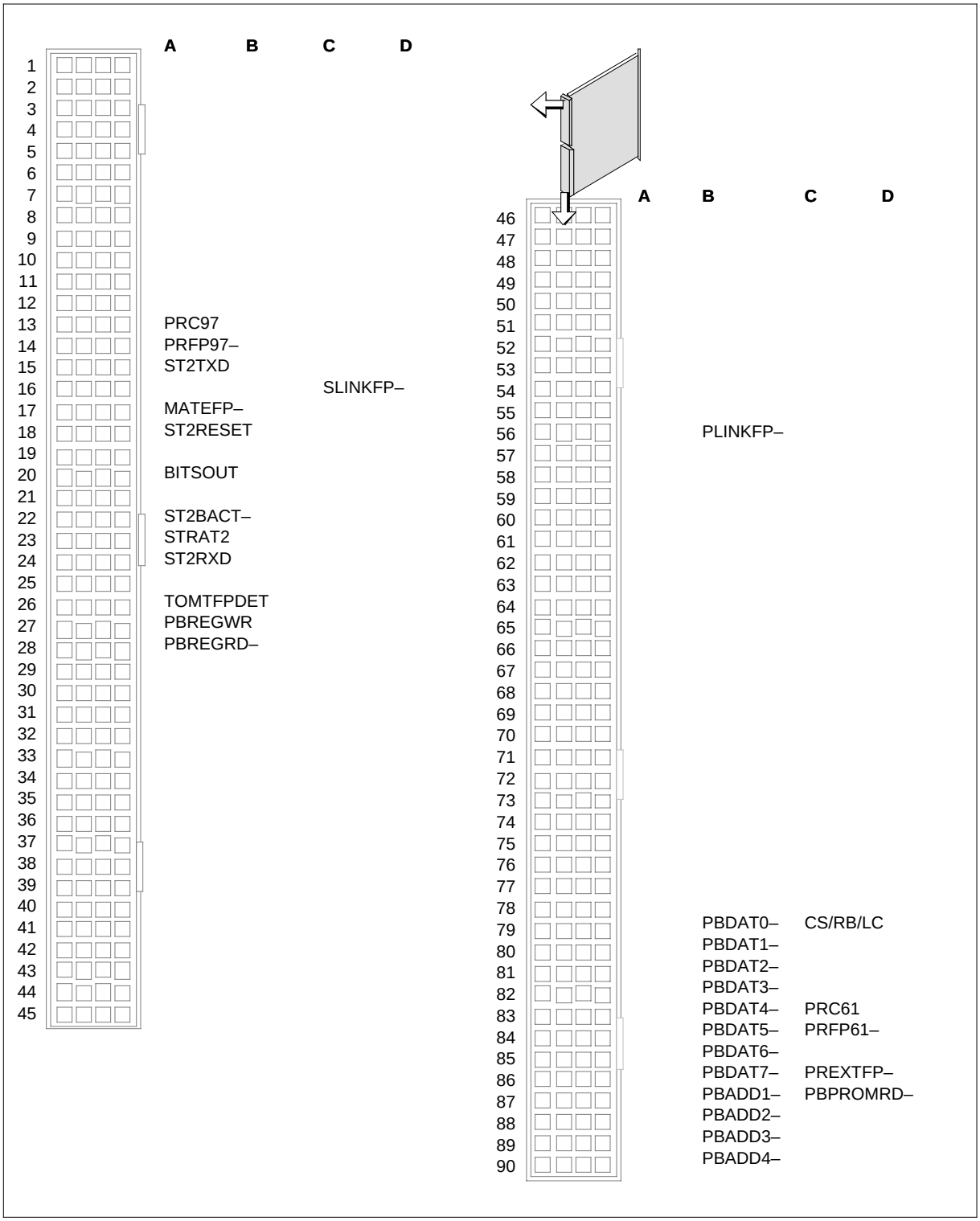
- state–control interface, accessed through the P–bus interface of the NT9X53 central processor
- ID PROM interface, accessed through the P–bus interface of the NT9X53 central processor

Signaling

Pin numbers

The pin numbers for the NT9X54AD appears in the following figure.

NT9X54AD pin numbers



NT9X54AD (end)

Technical data

Power requirements

The power requirements for NT9X54AD appear in the following table.

Power requirements for NT9X54AD

Supply	Minimum	Normal	Maximum
Supply voltage (V)	4.75	5.00	5.25
Supply ripple (V)			0.10 peak–to–peak

NT9X62AA

Product description

Use the NT9X62AA is with the dual–port message controller card (NT9X86AA). The NT9X62AA and the NT9X86AA work in the following locations:

- the network programming platform (NPP) application processor
- the NPP file processor
- the DMS–core

Functional description

The NT9X62AA has two main functions. The NT9X62AA provides an interface between an NT9X86AA and two subrate 512 (SR–512) optical links. The NT9X62AA generates the shelf 16.384 MHz clock and 8 KHz frame pulses (FP). The clock and frame pulses are locked to a reference frame pulse. The system removes this frame pulse from one of the SR–512 optical links.

Functional blocks

The functional blocks of the NT9X62AA appear in the following figures.

SR–512 section

The SR–512 contains the following functional blocks:

- optical transmit (OPT TX) and optical receive (OPT RX)
- transistor–transistor logic (TTL) to emitter–coupled logic (ECL), conversion (TEC) and ECL–to–TTL conversion (ETC)
- delay and FP retime
- quad fiber link interface chip (QFLIC)
- data transmitter receiver chip (DTRC) 0 and DTRC 1
- S28
- identification (ID) PROM
- power–up reset

Optical transmit and optical receive The OPT RX and OPT TX blocks are the optical modules. The OPT RX modules convert the optical signals from the fibers to ECL–compatible signals. The OPT TX modules convert ECL signals to 1300–nm optical signals for transmission on fiber.

TEC and ETC blocks The TEC block converts TTL–level signals to the ECL–level signals required to drive the optical modules. The ETC block

NT9X62AA (continued)

converts the ECL signals from the optical modules to the TTL levels that the QFLIC requires.

Delay and FP21 retime Three taps of a 25DL delay line supply the QFLIC with three delayed phases of the 49.152 MHz clock, CK21. The FP21R frame pulse from the FP21 GEN block is timed again before the application to the QFLIC.

Quad fiber link interface chip The QFLIC block performs different functions in the receive and transmit directions.

In the receive direction, the QFLIC block:

- recovers data from asynchronous serial inputs
- converts each serial input to a 6–bit parallel bus format
- provides a remote loopback mode that connects the serial input to the serial output

In the transmit direction, the QFLIC block:

- converts data from four 6–bit parallel buses to four serial outputs
- provides a local loopback mode that connects the serial output to the serial input

Data transmitter receiver chips 0 and 1 The DTRC blocks perform different functions in the receive and transmit directions.

In the receive direction, the DTRC blocks

- convert 10B12B data from the QFLIC to the original 10–bit data
- provide a one–frame elastic store
- latch alarm codes the system recently detected
- check the validity of received pseudo–random sequences
- enable data output to the 10–bit shorting bus (S–bus) receive data (SRDA) during the assigned time slots

In the transmit direction, the DTRC blocks

- sample data from the 10–bit S–bus transmit data (STDA) during the assigned time slots
- code data into a 10B12B code
- insert alarm codes or pseudo–random sequences in place of data when necessary

- transmit the frame word when a transmit frame pulse occurs
- convert 10B12B data to two 6–bit nibbles for output to the QFLIC block

The DTRC blocks provide link control functions and link state information through registers accessible to the processor bus (P–bus).

S28

The S28 block performs the following functions:

- generates the subrate timing signals required to multiplex two DTRC blocks to one S–bus
- buffers out–of–band (OOB) messages in the receive direction for two links
- provides the ability to transmit OOB messages on two links
- provides P–bus address decoding for all registers on the
- provides a page selection function to access DTRC registers
- generates the reference frame pulse from which the shelf frame pulse derives

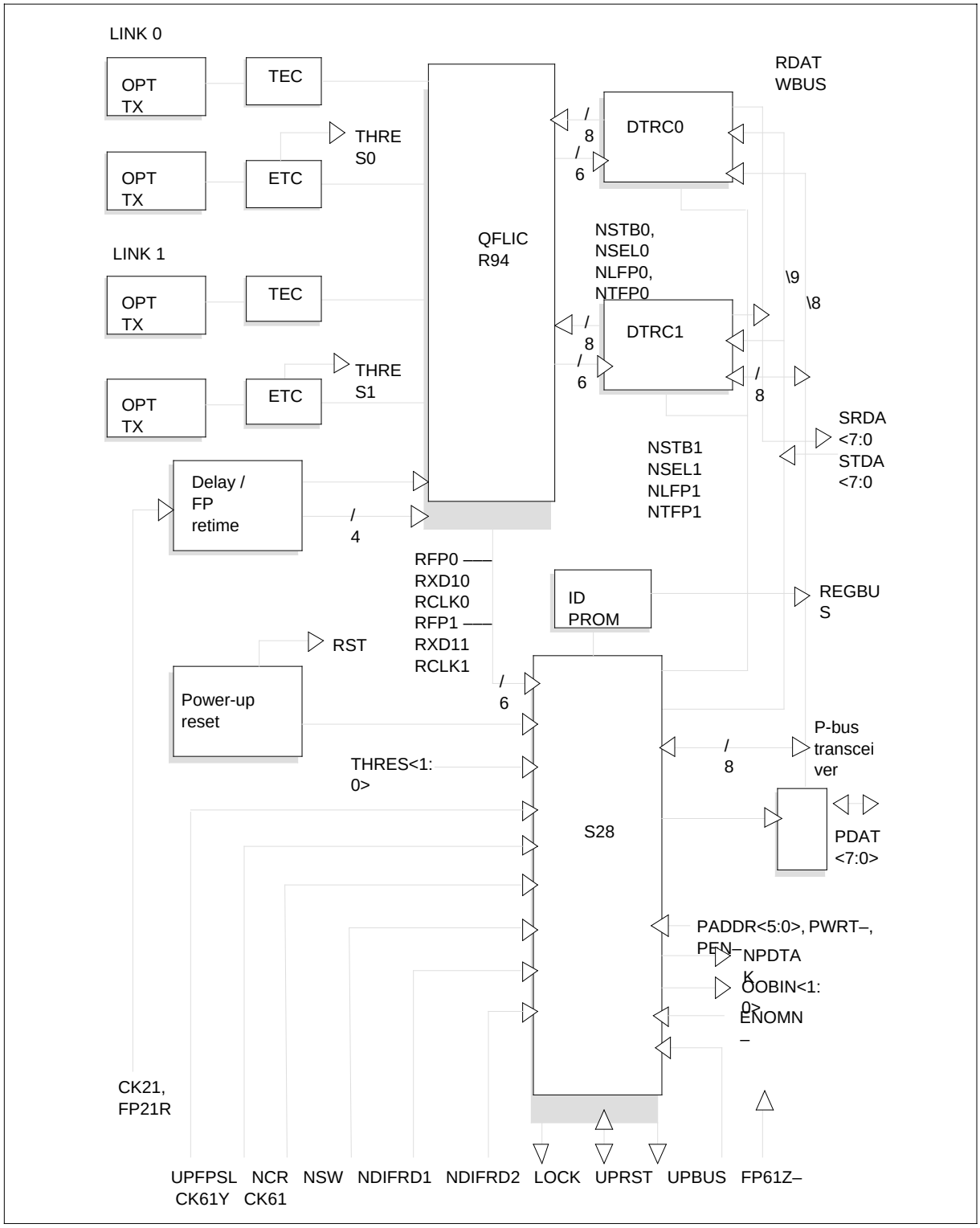
Identification PROM The ID PROM provides a processor–accessible identification of the paddle board.

Power–up reset The power–up reset block applies a reset signal to all application–specific integrated circuits (ASIC) on the NT9X62AA. The power–up reset block applies the reset signal for a minimum period of 100 ms after the application of power to the card.

The blocks of the SR–512 link section appear in the following figure.

NT9X62AA (continued)

NT9X62AA functional blocks



Clock section

The clock section contains the following functional blocks:

- 8751 microcontroller
- control voltage register
- digital–to–analog converter (DAC)
- 49.152 MHz voltage–controlled oscillator (VCXO)
- divide–by–2
- divide–by–3
- 16.384 MHz analog phase–locked loop (PLL)
- FP21 generator (GEN)

8751 microcontroller The 8751 microcontroller performs the following functions:

- reads the difference between the shelf frame pulse and the reference frame pulse from the S28
- computes the response of the PLL
- sets the voltage applied to the VCXO
- monitors the presence of the reference and secondary frame pulses
- provides a lock state bit. The lock state bit indicates when the shelf frame pulse locks to the reference frame pulse
- provides additional state bits

Control voltage register The control voltage register stores the 12 bit value used in the DAC.

Dialog–to–analog converter The DAC is a 12–bit converter with an output voltage range of 0 to 4.5V.

49.152 MHz voltage controlled oscillator The 49.152 MHz VCXO has a minimum tuning range of ±40 ppm when the control voltage changes from 0.5 to 3.5V.

Divide–by–2 The divide–by–2 block divides the 16.384 MHz clock by 2 to supply the microcontroller with an 8.192 MHz clock.

Divide–by–3 The divide–by–3 block generates a 16.384 MHz clock from the 49.152 MHz clock.

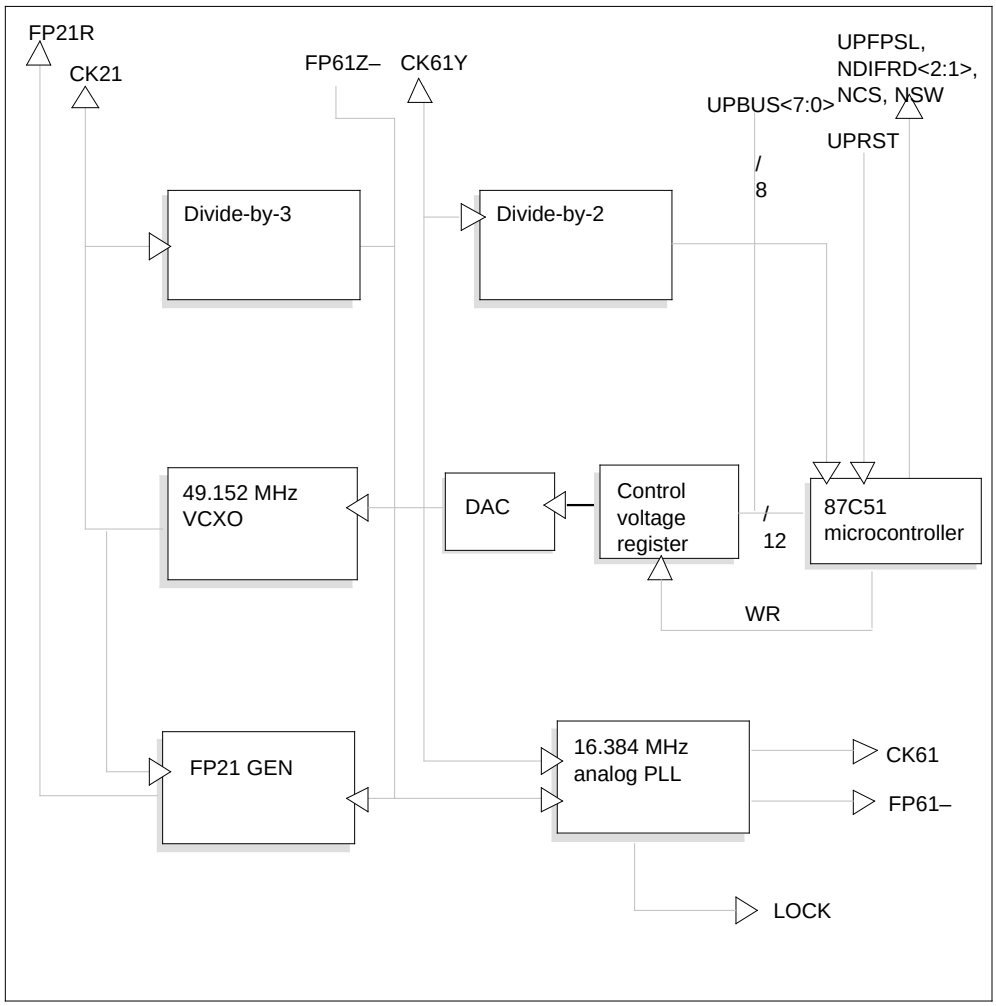
NT9X62AA (continued)

16.384 MHz analog phase–locked loop The 16.384 MHz analog PLL locks output of a 16.384 MHz VCXO to the 16.384 MHz signal. The divide–by–3 block generates the 16.384 MHz signal.

FP21 generator The FP21 GEN block generates a 21 ns frame pulse from the reference frame pulse generated by the QFLIC.

The blocks of the clock section appears in the following figure.

NT9X62AA Functional blocks

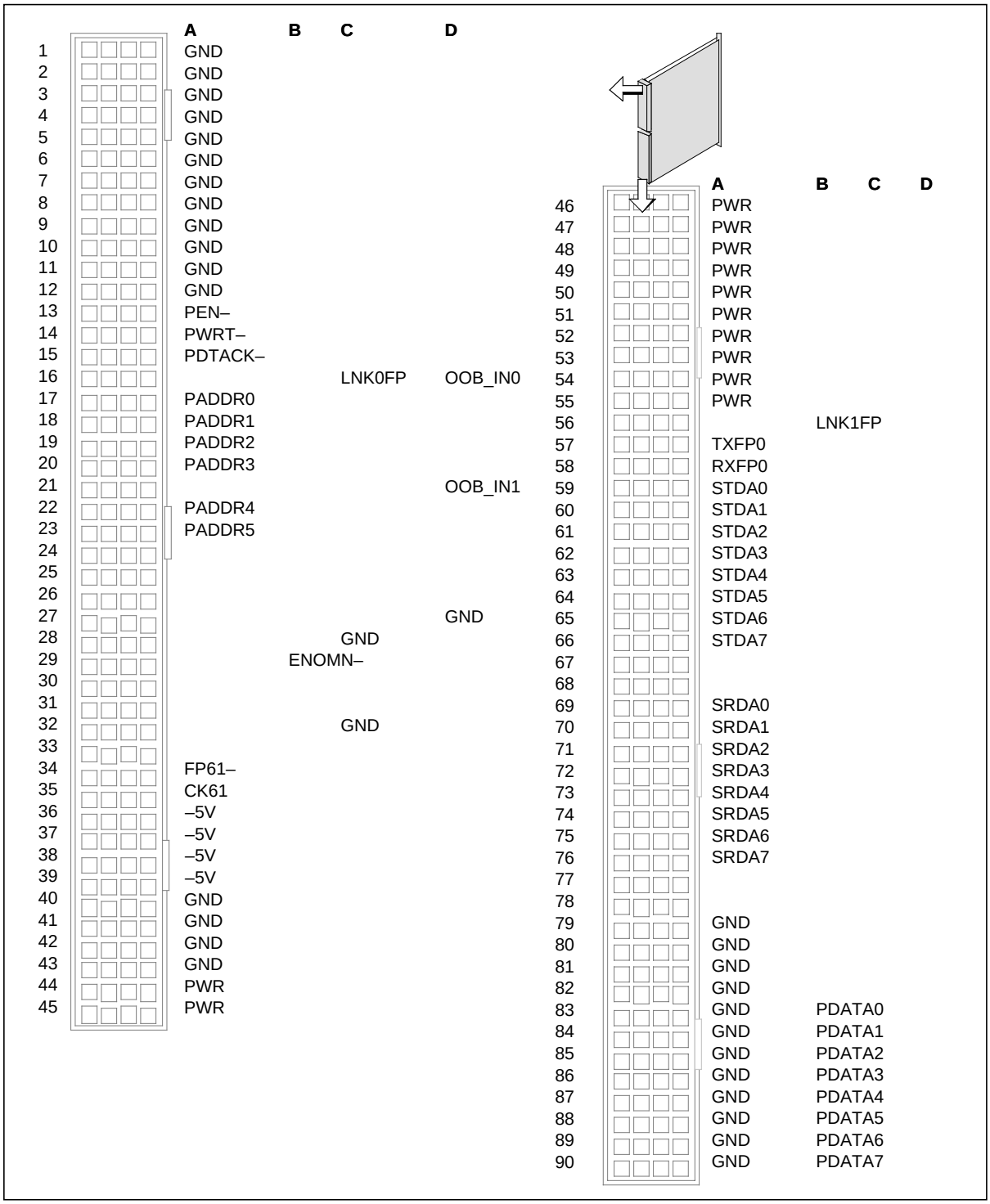


Signaling

Pin numbers

The pin numbers for the NT9X62AA appears in the following figure.

NT9X62AA pin numbers

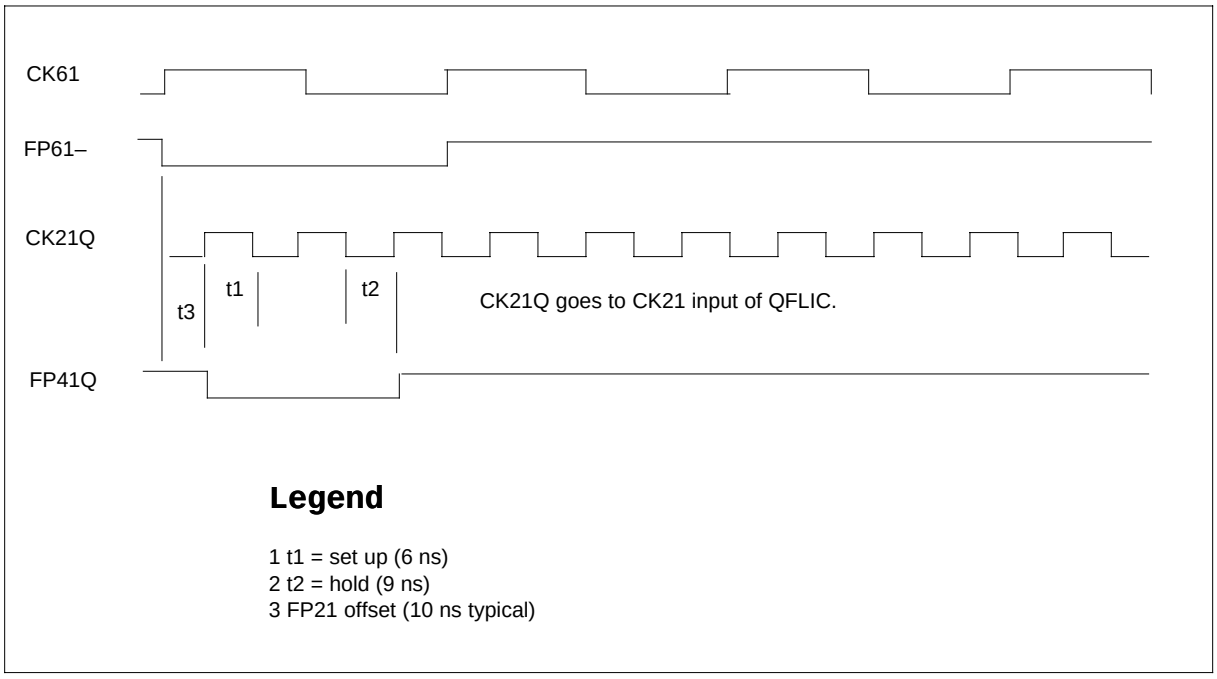


NT9X62AA (continued)

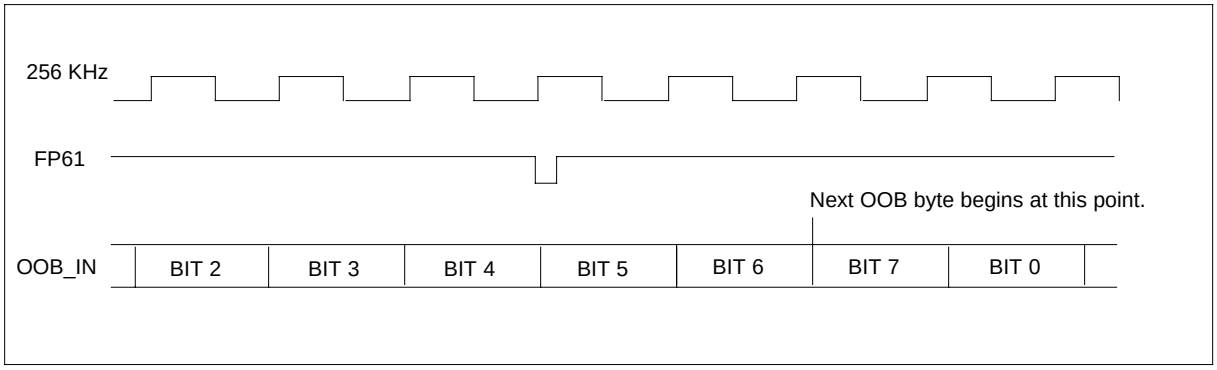
Timing

The timing for the appears in the following figures and tables.

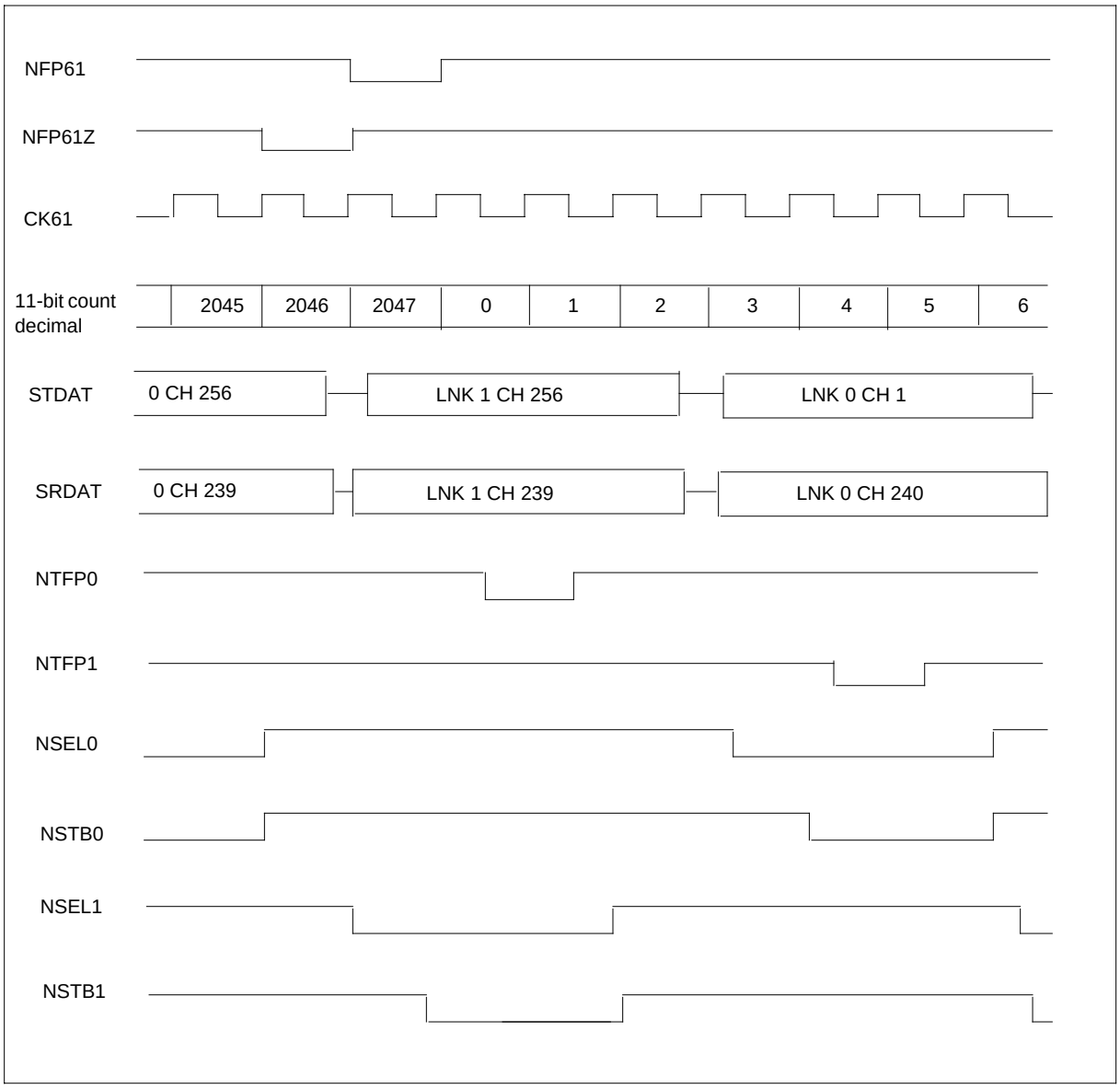
NT9X62AA CK21 and FP41 synchronization timing



NT9X62AA Out–of–band serial format to the backplane timing

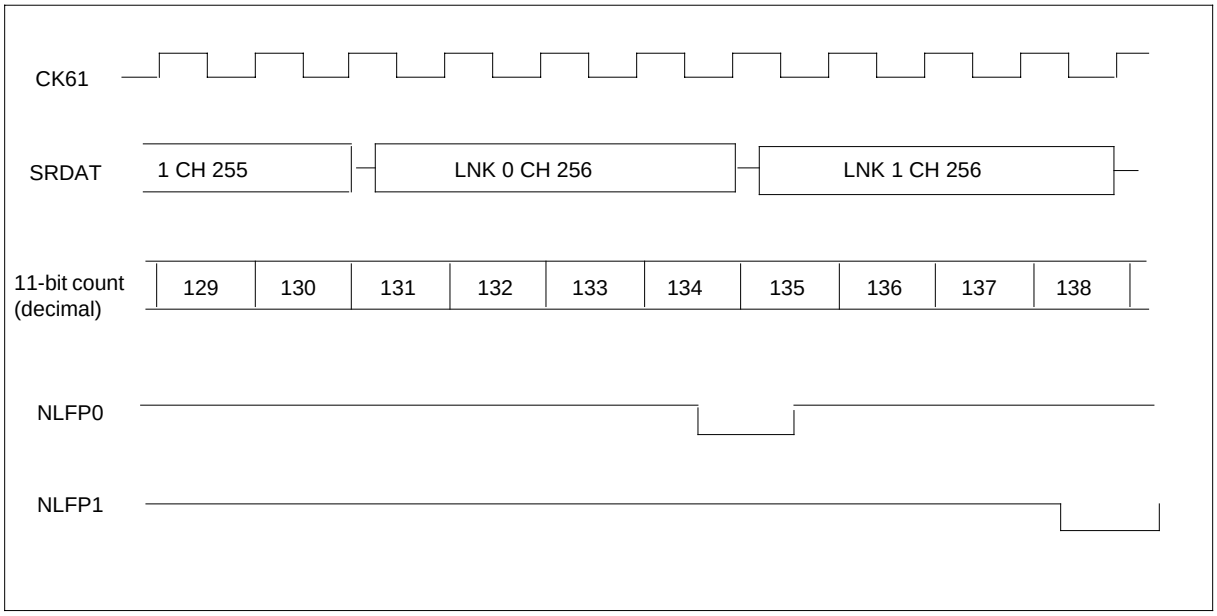


NT9X62AA S02 frame pulse, strobe and select signals

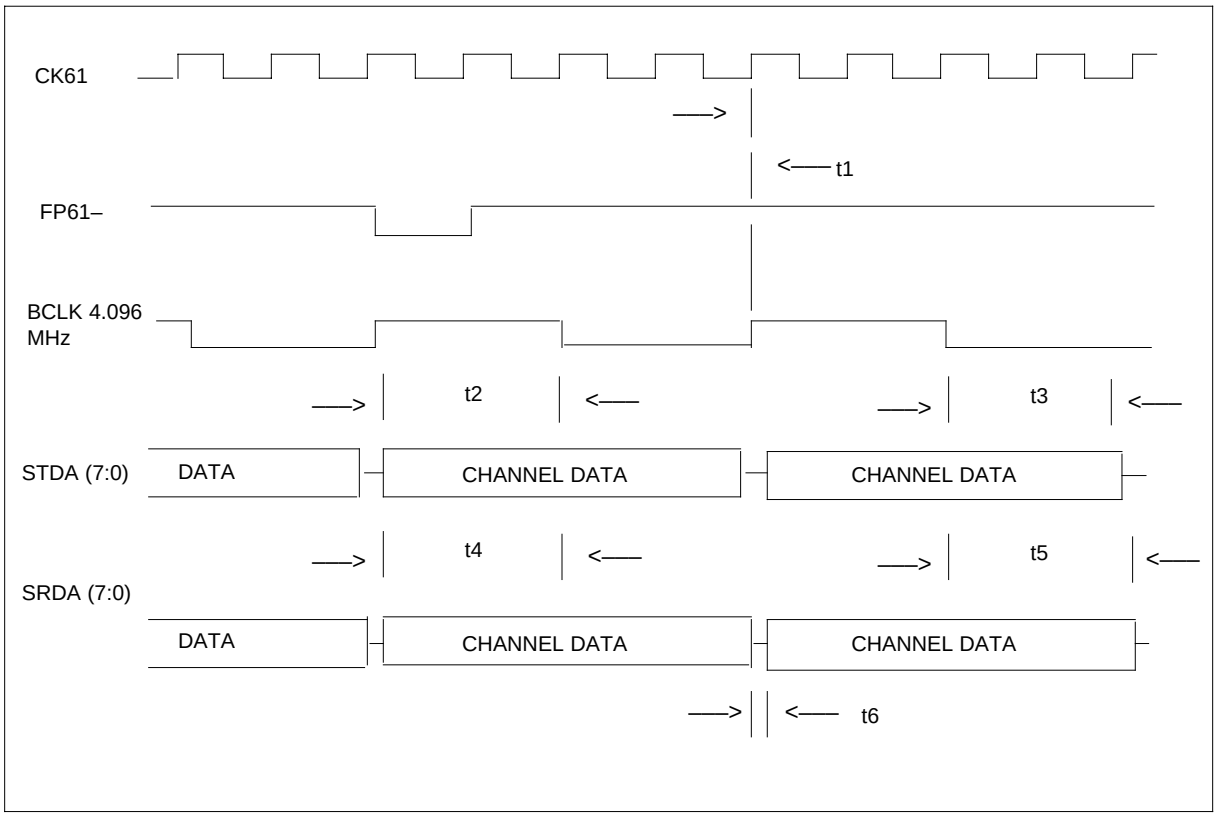


NT9X62AA (continued)

NT9X62AA signals for 256–channel for each frame subrate mode



NT9X62AA S–bus timing specification at backplane

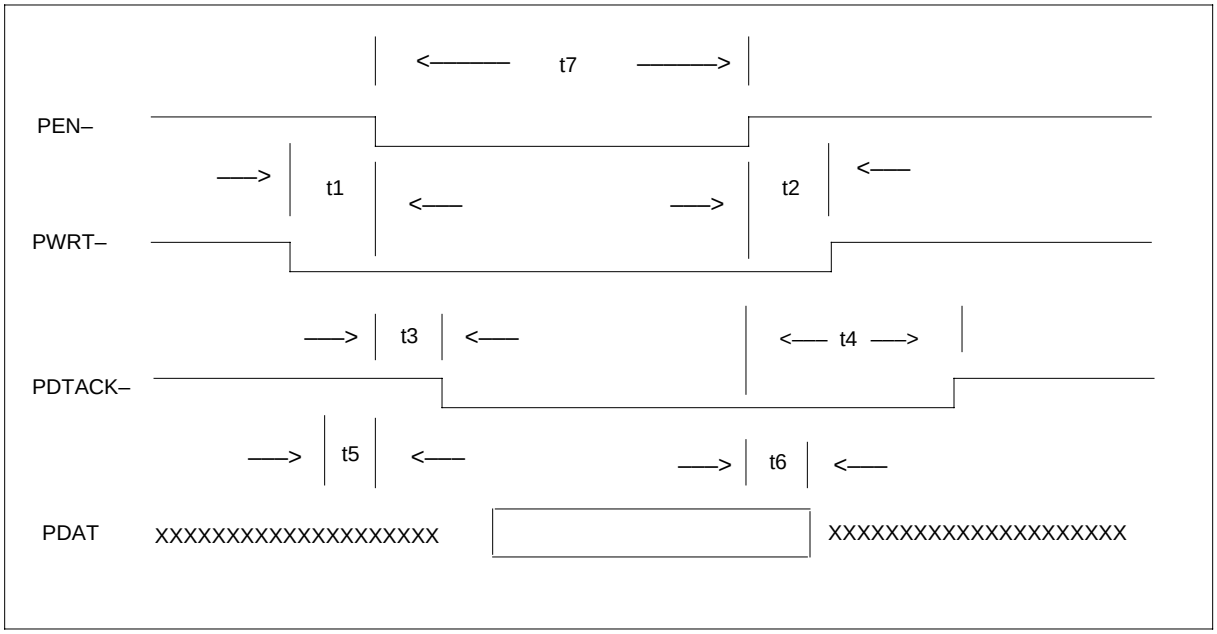


S–bus timing specification at backplane

Symbol	Parameter	Minimum	Nominal	Maximum
t1	Difference between C61 and BCLK	0 ns		±30 ns
t2	Required setup	22 ns		92 ns
t3	Required hold	62 ns		122 ns
t4	Set–up	32 ns		122 ns
t5	Hold	92 ns		122 ns
t6	Guard time		60 ns	

NT9X62AA (continued)

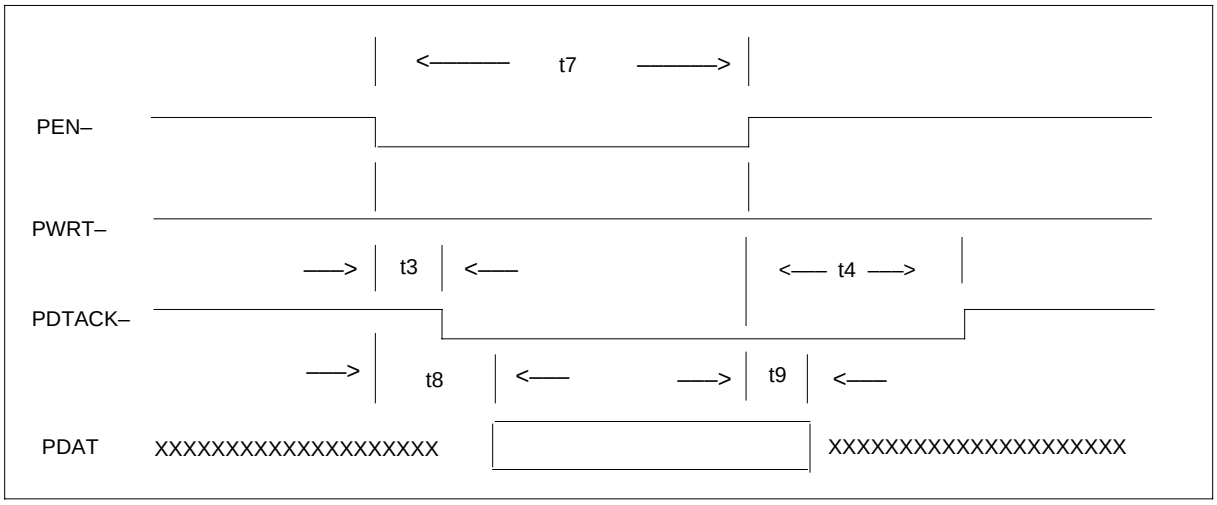
NT9X62AA P–bus interface timing (write cycle)



P–bus interface timing (write cycle)

Symbol	Parameter	Minimum	Nominal	Maximum
1	PWRT- valid to PEN-	0 ns		
2	PEN- released to PWRT- released	0 ns		
3	PEN- valid to PDTACK asserted	300 ns		360 ns
4	PEN-released to PDTACK- released			40 ns
5	DATA valid to PEN-	-60 ns		
6	PEN- released to DATA valid	0 ns		
7	PEN- pulse width	360 ns		

NT9X62AA P–bus interface timing (read cycle)

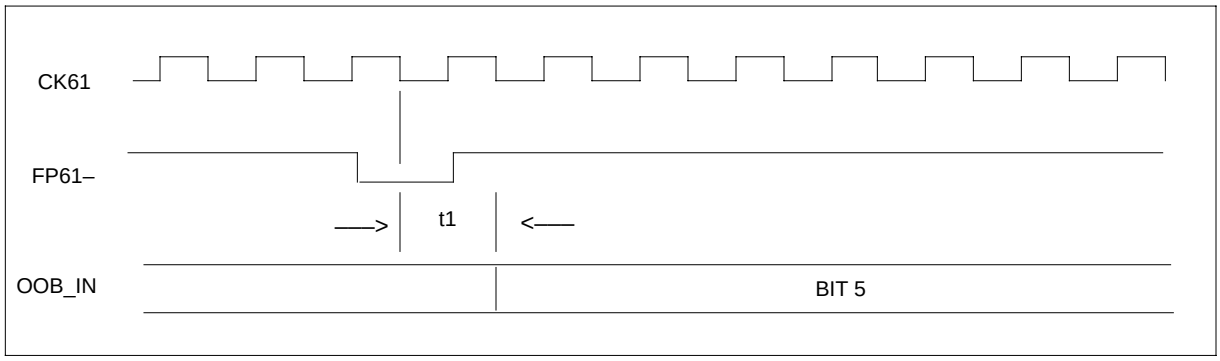


P–bus interface timing (read cycle)

Symbol	Parameter	Minimum	Nominal	Maximum
t3	PEN- valid to PDTACK- asserted	300 ns		360 ns
t4	PEN- released to PDTACK- released			40 ns
t7	PEN- pulse width	360 ns		
t8	PEN- asserted to PDAT valid	240 ns		300 ns
t9	PEN- released to PDAT released			10 ns

NT9X62AA (end)

NT9X62AA OOB_IN timing specification



OOB_IN timing specification

Symbol	Parameter	Minimum	Nominal	Maximum
t1	Shift register output delay		15 ns	500 ns

Technical data

Power requirements

The power requirements for the NT9X62AA appear in the following table. The supply ripple voltage specification is measured peak–to–peak.

Power requirement

Parameter	Minimum	Nominal	Maximum
Supply voltage	4.75 V	5.0 V	5.25 V
Supply ripple			0.1 V
Supply current		1.6 A	2.2 A

Power requirement

Parameter	Minimum	Nominal	Maximum
Supply voltage	-5.46 V	-5.2 V	-4.94 V
Supply ripple			0.1 V
Supply current			0.55 A

NT9X62BA

Description

The NT9X62BA provides an interface between the message switch port card (an NT9X17CA or DA) and four fiber optic links.

Functional description

The NT9X62BA performs functions on the receive path and the transmit path.

The NT9X62BA performs the following functions on the receive path:

- converts optical data to electrical data
- converts serial data to parallel data
- receives the frame pulse and alarm codes
- receives the out–of–band (OOB) reset

The NT9X62BA performs the following functions on the transmit path:

- converts parallel data to serial data
- converts electrical data to optical data
- transmits the frame pulse and alarm codes
- generates LTBUFF overflow signaling
- generates OOB reset signaling

The NT9X62BA also performs remote and local loopback of data.

Functional blocks

The NT9X62BA contains the following functional blocks:

- 49 MHz phase–locked loop (PLL)
- FP21 generator
- delay line
- quad fiber link interface chip (QFLIC)
- emitter–coupled logic (ECL) and transistor–transistor logic (TTL) drivers
- fiber transmit (TX) and receive (RX)
- data transmitter receiver chip (DTRC)
- frame pulse generator
- subrate controller (SRC) application–specific integrated circuit (ASIC)

NT9X62BA (continued)

- shorting bus (S–bus) interface
- identification (ID) PROM

49 MHz phase–locked loop

The 49 MHz PLL block contains a digital PLL circuit. The circuit generates and locks the 49.152 MHz clock to the 16.384 MHz clock.

FP21 generator

The FP21 generator block generates a 21 ns wide frame pulse for the QFLIC.

Delay line

The delay line block contains a delay line with 5 ns steps. The QFLIC uses the 5 ns steps to sample and extract data.

Quad fiber link interface chip

The QFLIC block provides an interface to the four fiber links. The interface provides data recovery, clock recovery, link frame pulse recovery, and loopbacks.

Emitter–coupled logic and transistor–transistor logic drivers

The ECL and TTL drivers provide an interface between the TTL circuits and the ECL circuits.

Fiber transmit and receive

The fiber TX modules convert the electrical data to optical data. The fiber RX modules convert the optical data to electrical data.

Data transmitter receiver chip

The DTRC block contains four DTRC application–specific integrated circuits (ASIC). The circuits act as an interface between the S–bus and the QFLIC.

Frame pulse generator

The frame pulse generator block creates all transmit and receive frame pulses for the four DTRCs.

Subrate controller application–specific integrated circuit

The SRC ASIC block performs the following functions:

- generates the frame pulse and strobe timing for the DTRCs
- selects primary and secondary frame pulses (from a group of four frame pulses) the block drives to the backplane
- receives and transmits the OOB data

- provides separate ENET and DMS–core channel alignment settings for each link
- provides subrates that you can program
- provides a P–bus interface
- provides register access to optical receiver module threshold indicators

Shorting bus interface

The S–bus block separates the S–bus transmit data (STDA) lines and S–bus receive data (SRDA) lines of the card from the DRTC lines. The S–bus block generates the handshaking signals for frame synchronization in 511 channel mode.

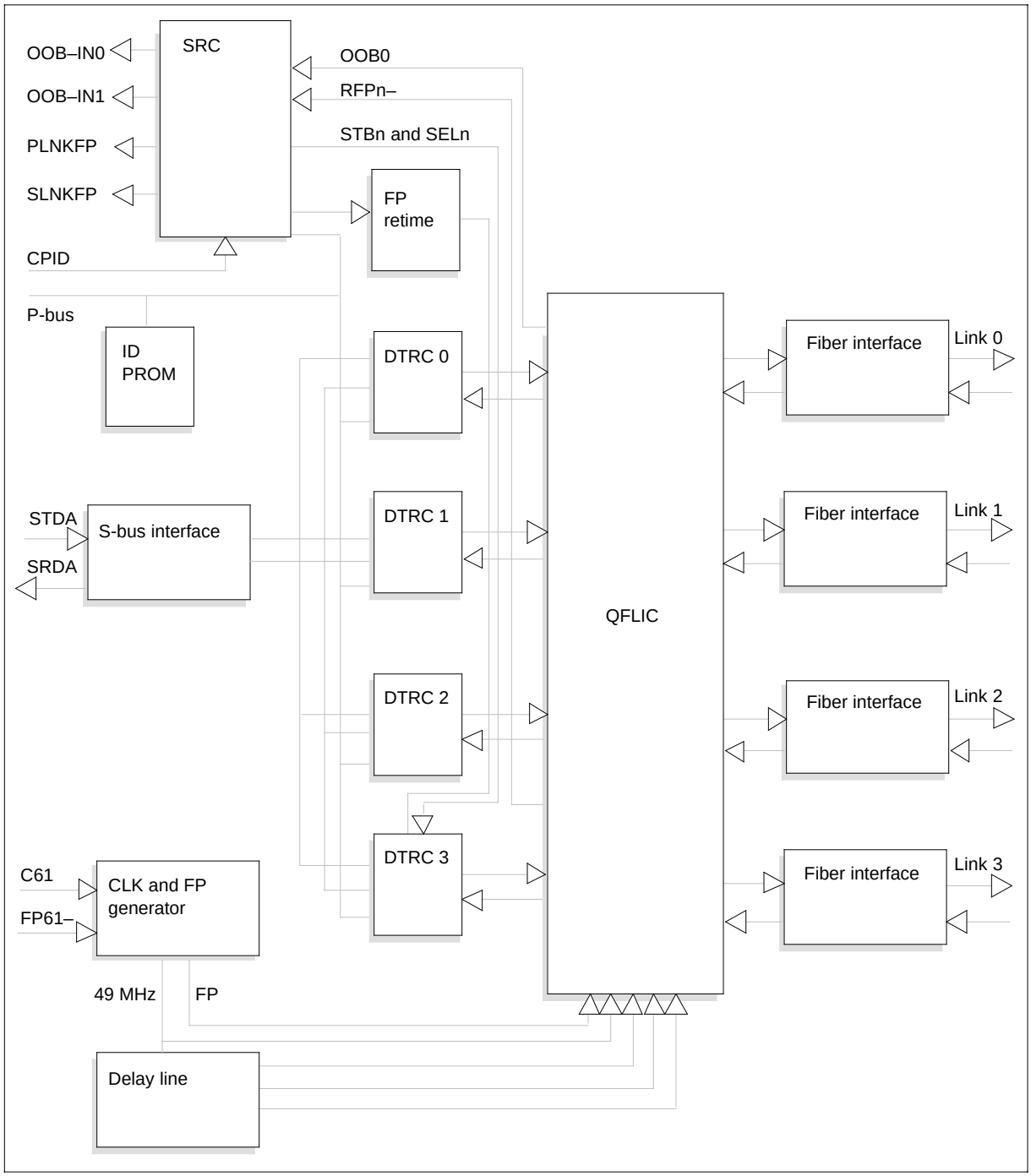
Identification PROM

The ID PROM identifies cards.

The relationship between functional blocks appears in the following figure.

NT9X62BA (continued)

NT9X62BA functional blocks



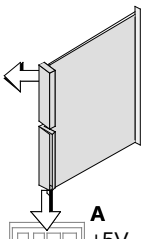
Signaling

Pin numbers

The pin numbers for NT9X62BA appear in the following figure.

NT9X62BA (end)

NT9X62BA pin numbers



	A	B	C	D
1	GND			
2	GND			
3	GND			
4	GND			
5	GND			
6	GND			
7	GND			
8	GND			
9	GND			
10	GND			
11	GND			
12	GND			
13	PBDAS–			
14	PBWRT–			
15	PBACK–			
16			SLNKFP–	OOB–IN0
17	PBADD2			
18	PBADD3			
19	PBADD4			
20	PBADD5			
21	PBSDREN			OOB–IN1
22	PBADD6			
23	PBADD7			
24	PBID0			
25				
26	PBFP61–			
27	CPSDREN			GND
28	PBID1		GND	
29	HW4			
30				
31				
32			GND	
33				
34				
35		TYPE1		
36	–5V	HW0		
37	–5V	HW1		
38	–5V			
39	–5V	HW3		
40	GND			
41	GND			
42	GND			
43	GND			
44	+5V			
45	+5V			

	A	B	C	D
46	+5V			
47	+5V			
48	+5V			
49	+5V			
50	+5V			
51	+5V			
52	+5V			
53	+5V			
54	+5V			
55	+5V			
56	TYPE0	PLNKFP–		
57	LTVL			
58	LRVL			
59	STDA0			
60	STDA1			
61	STDA2			
62	STDA3			
63	STDA4			
64	STDA5			
65	STDA6			
66	STDA7			ETYPE0
67	STDA8			
68				
69	SRDA0			
70	SRDA1			
71	SRDA2			
72	SRDA3			
73	SRDA4			
74	SRDA5			
75	SRDA6			
76	SRDA7			
77				
78				
79	GND			
80	GND			
81	GND			
82	GND			
83	GND	PBDAT24		
84	GND	PBDAT25		
85	GND	PBDAT26		
86	GND	PBDAT27		
87	GND	PBDAT28		
88	GND	PBDAT29		
89	GND	PBDAT30		
90	GND	PBDAT31		PBC61

Use this template for DMS SuperNode paddleboards.
This message does NOT print.

NT9X62BB

Product description

The NT9X62BB card provides an interface between the message switch port card (NT9X17AD) and four fiber-optic SR-128 links. The SR-128 links are used to send messages between the DMS-bus and the link peripheral processor (LPP) or enhanced LPP (ELPP).

The NT9X62BB card performs the same functions as the NT9X62BA with the following added features:

- aligned frame pulses
- subsystem frame pulse control
- reception of the out-of-band (OOB) messages on link 0

Location

The NT9X62BB card is located behind the NT9X17AD card on a local message switch (LMS) shelf in an LPP or ELPP cabinet. The MS side of the link must also be provisioned with an NT9X62BB behind an NT9X17AD.

Functional description

The NT9X62BB card performs functions on the receive path and transmit path.

The NT9X62BB card performs the following functions on the receive path:

- converts optical data to electrical data
- converts serial data to parallel data
- recovers clock, frame pulse, and alarm codes
- detects data errors (18% of single bit error)
- controls remote and local loopback of data
- receives the OOB messages on link 0

The quad fiber link interface chip (QFLIC) recovers data, clock, and frame pulse from the link. Data is fed to the data transmitter receiver chip (DTRC). The DTRC converts the 12-bit data to a 10-bit word and sends 8 bits as data and 1 bit as status bit. The remaining 1 bit is used for reception of the OOB reset messages on link 0.

The NT9X62BB card performs the following functions on the transmit path:

- converts parallel data to serial data
- converts electrical data to optical data

NT9X62BB (continued)

- transmits clock, frame pulse, and alarm codes
- generates OOB signaling

Data is fed from the MS port card through the shorting bus (S-bus) to the DTRC, where it is encoded to the 10B12B format. It is then transmitted to QFLIC. The QFLIC provides four serial outputs that connect to the optical transmit modules. Data is then transmitted onto the links.

The NT9X62BB also performs general functions, such as element identification and testability.

Functional blocks

NT9X62BB has the following functional blocks:

- clock and frame pulse generator
- delay line
- QFLIC
- fiber interface
- DTRC
- subrate controller (SRC)
- S-bus interface
- frame pulse (FP) retiming
- identification (ID) electrically erasable programmable read-only memory (EEPROM)
- automated test environment (ATE) interface

Clock and frame pulse generator

A clock hybrid module generates and locks a 49.152-MHz clock to the system 16.384-MHz clock. The QFLIC needs the 49.152-MHz clock and a 21-ns-wide frame pulse.

Delay line

This block consists of a delay line that outputs four 49.152-MHz clock signals, each shifted by 5 ns. The QFLIC uses these signals for data sampling and extraction.

Quad fiber link interface chip

The QFLIC connects to four fiber links. It provides functions like data recovery, clock recovery, link frame pulse recovery, and loopbacks.

Fiber interface

The transmit fiber modules convert electrical data to optical data. The receive fiber modules convert optical data to electrical data. The receiver threshold output indicates the incoming optical link power. To connect the transistor-transistor logic (TTL) circuitry to the emitter-couple logic (ECL) circuitry, ECL/TTL translators are required. The optical modules require ECL/TTL translators because optical modules have ECL interface characteristics.

Data transmitter receiver chip

Four DTRC application-specific integrated circuits (ASIC) provide an interface between the S-bus and the QFLIC. Each DTRC provides functions like elastic storage, 10B12B encoding and decoding, and 10B12B alarm code detection and insertion. Each DTRC also provides maintenance functions, such as loopback control for QFLIC.

Subrate controller

The SRC generates the timing for the circuit board and provides the processor interface and OOB messaging.

S-bus interface

This block provides termination of the S-bus and buffering of the S-bus data between the NT9X62BB card and the NT9X17AD port card.

Frame pulse retiming

This block retimes the transmit and local FPs before they are applied to the DTRCs. The transmit FP signals are aligned to eliminate skew between primary and secondary FP signals on the LMS backplane.

Identification EEPROM

The ID EEPROM is used for card identification.

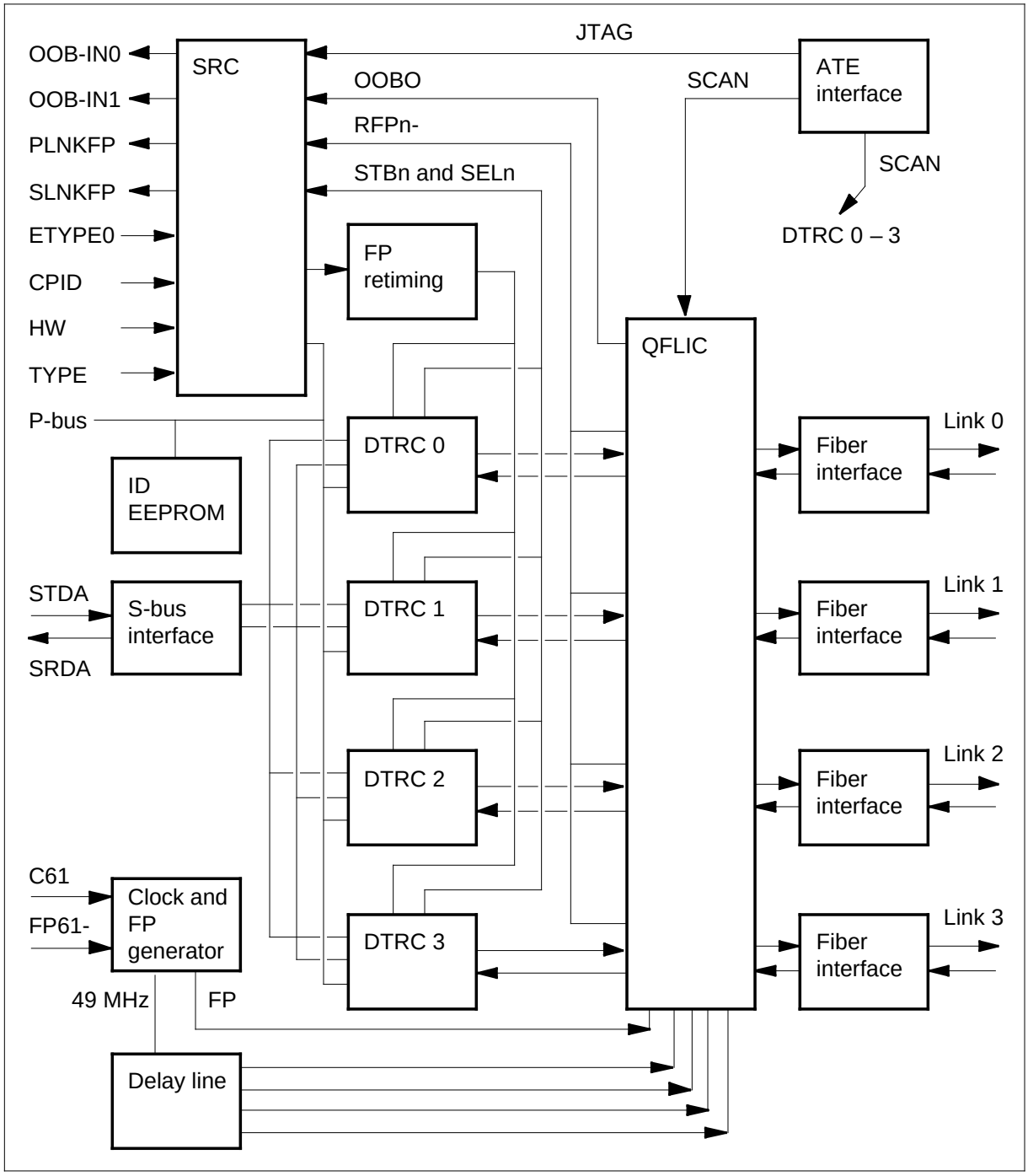
Automated test environment interface

The SRC ASIC can be tested at the ATE stage with the joint test action group (JTAG) method. The DTRC and QFLIC can be tested at the ATE stage with internal scan chain test method.

The following figure shows the relationship of the functional blocks.

NT9X62BB (continued)

NT9X62BB functional blocks

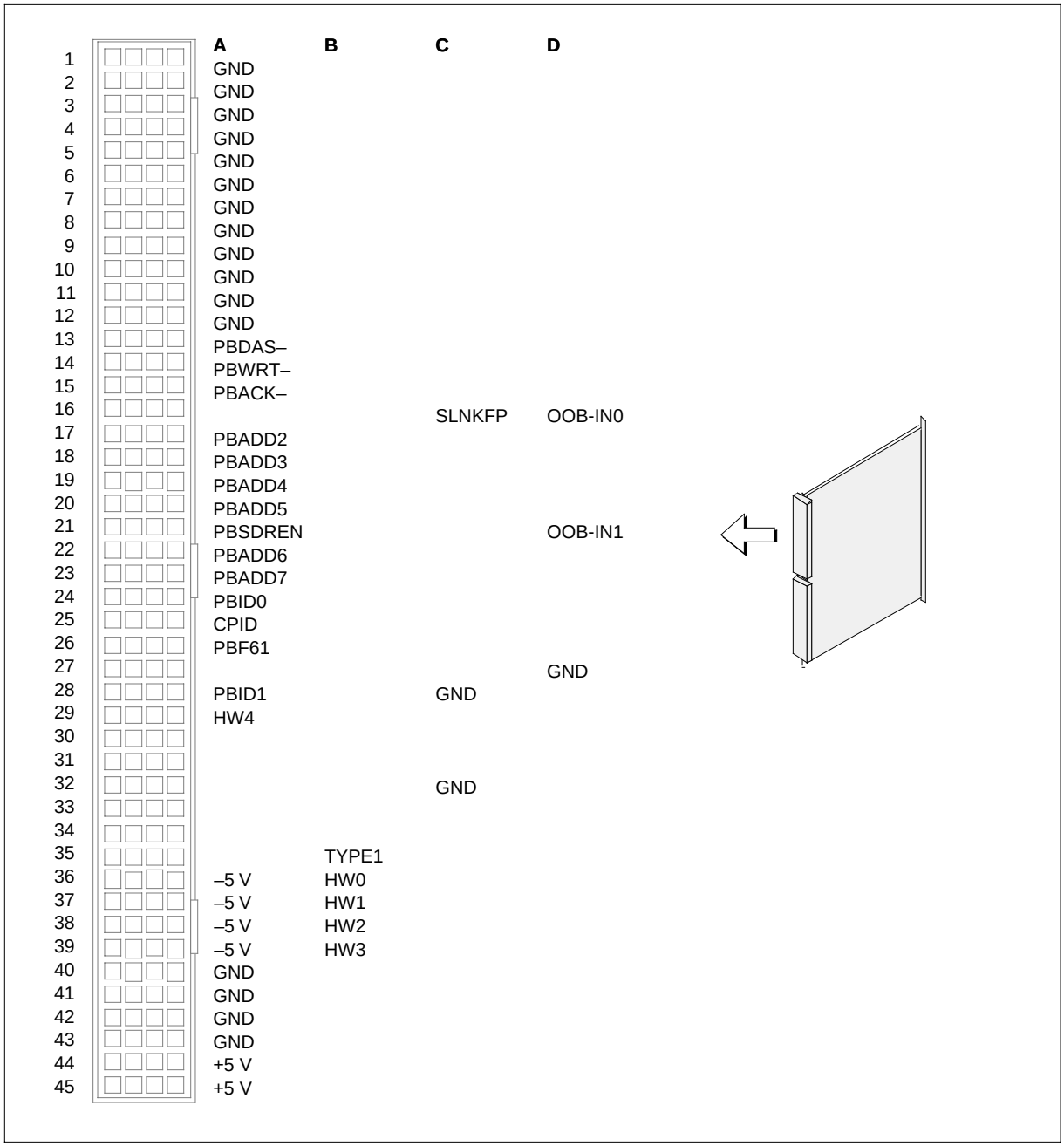


Signaling

Pin outs

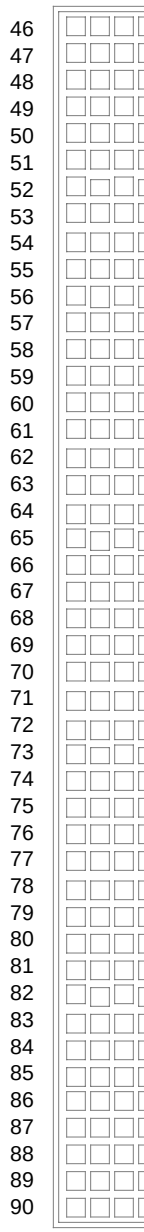
The following figure shows the pin outs for NT9X62BB.

NT9X62BB pin outs (part 1 of 2)

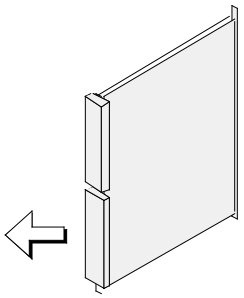


NT9X62BB (continued)

NT9X62BB pin outs (part 2 of 2)



	A	B	C	D
46	+5 V			
47	+5 V			
48	+5 V			
49	+5 V			
50	+5 V			
51	+5 V			
52	+5 V			
53	+5 V			
54	+5 V			
55	+5 V			
56	TYPE0	PLNKFP		
57	LTVL			
58	LRVL			
59	STDA0			
60	STDA1			
61	STDA2			
62	STDA3			
63	STDA4			
64	STDA5			
65	STDA6			
66	STDA7			ETYPE0
67	STDA8			
68				
69	SRDA0			
70	SRDA1			
71	SRDA2			
72	SRDA3			
73	SRDA4			
74	SRDA5			
75	SRDA6			
76	SRDA7			
77	SRDA8			
78				
79	GND			
80	GND			
81	GND			
82	GND			
83	GND	PBDAT24		
84	GND	PBDAT25		
85	GND	PBDAT26		
86	GND	PBDAT27		
87	GND	PBDAT28		
88	GND	PBDAT29		
89	GND	PBDAT30		
90	GND	PBDAT31		PBC61



Technical data

Power requirements

The following table shows the power requirements for the NT9X62BB.

NT9X62BB power requirements

Parameter	Minimum	Nominal	Maximum
Supply voltage:			
VDD	4.75 V	5.0 V	5.25 V
VEE	-4.94 V	-5.2 V	-5.46 V
Supply current:			
VDD	1.06 A	1.11 A	1.16 V
VEE	0.94 A	0.99 A	1.04 A

NT9X62CA

Product description

The NT9X62CA message switch link SR–512 subrate paddle board provides an interface. The interface occurs between the message switch port card (NT9X17AD/BB/CA/DA) and two fiber optic links. The paddle board performs subrate selection for 128, 256, or 511 channels for each frame.

The NT9X62CA performs functions like the NT9X62BA, except that the NT9X62CA can receive out–of–band (OOB) information on two fiber links. These functions are necessary when the NT9X62CA links to the computing module.

Location

The NT9X62CA paddle board can link to the computing module (CM) shelf. When this condition occurs, the paddle board is in a dedicated slot behind the port card in the SuperNode SE message switch shelf. The NT9X62CA paddle board is not linked to the CM shelf. The NT6X62CA can be in a provisionable slot on the message switch shelf.

Functional description

The NT9X62CA functions include element identification and test functions. The quad fiber link interface chip (QFLIC) and the data transmitter receiver chip (DTRC) perform these functions. The NT9X62CA is also a message link between the message switch and the 16K enhanced network (16K ENET) on the SNSE cabinet.

The NT9X62CA links communicates between the SNSE message switch and the following shelves in the SNSE cabinet:

- 16K ENET
- CM

The 2–link paddle board provides a processor–bus (P–bus) access for the DTRC and other on–board devices.

The transmit path has the following functions:

- conversion of parallel data to serial data
- conversion of electrical data to optical data
- transmission of clock, frame pulse, and alarm codes
- generation of the link–to–transaction–bus (T–bus) buffer overflow state
- generation of OOB reset signaling

On the transmission side, data is fed from the NT9X17, over the shorting bus (S–bus) to the DTRC. At the DTRC, the 10B12B format codes the data. The DTRC also provides functions like alarm code insertion and loopback control. The QFLIC provides serial outputs that connect to the optical transmit modules. Data transmits to the links.

The receive path has the following functions:

- conversion of serial data to parallel data
- conversion of optical data to electrical data
- clock, frame pulse, and alarm codes recovery
- data error detection (18% of single–bit error)
- remote/local loopback of data
- OOB reset signaling reception

On the receive side, the QFLIC recovers the data, the clock, and the frame pulse from the link. A 49.152 MHz clock, derived from the 16.384 MHz system clock, drives the QLFIC.

Functional blocks

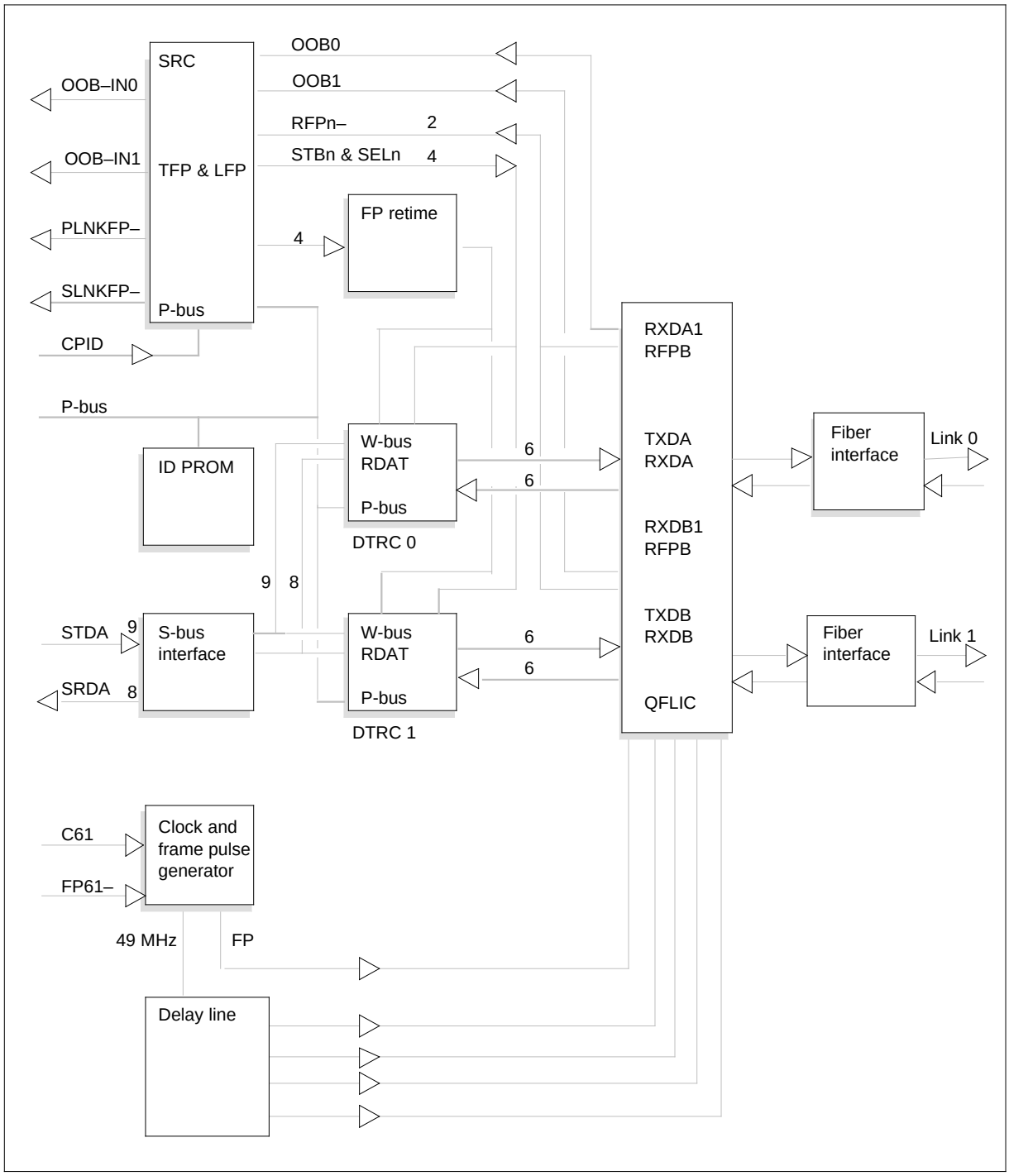
The NT9X62CA has the following functional blocks:

- clock and frame pulse generator
- delay line
- QFLIC
- fiber interface
- DTRC
- subrate controller (SRC)
- S–bus interface
- frame pulse retiming
- identification (ID) PROM

The relationship between functional blocks appears in the following figure.

NT9X62CA (continued)

NT9X62CA functional blocks



Clock and frame pulse generator

A clock hybrid module uses the system 16.384 MHz clock to generate a 49.152 MHz clock. The QFLIC needs the 49.152 MHz clock and a 21 ns–wide frame pulse.

Delay line

This block is a delay line with 5 ns steps. The QFLIC uses the delay line to sample and extract correct data.

Quad fiber link interface chip

The R94 QFLIC can connect to a maximum of four fiber links. The chip provides functions like data recovery, clock recovery, link frame recovery. The chip also provides functions like loopback and parallel data to serial data conversion.

Fiber interface

The transmit fiber modules convert electrical data to optical data. The receive fiber modules convert optical data to electrical data. The receiver threshold bit indicates when the optical power level drops below a specified performance level. The ECL/TTL translators connect the transistor–transistor logic (TTL) circuits to the emitter–couple logic (ECL) circuits. The ECL/TTL translators are necessary because the optical modules have ECL interface characteristics.

Data transmitter receiver chip

Two DTRC application–specific integrated circuits (ASIC) provide a connection between the S–bus and the QFLIC. Each DTRC provides functions like elastic storage, 10B12B encoding and decoding, 10B12B alarm code detection and insertion, and loopback control. The write–bus (W–bus) acts as the input bus from the S–bus interface.

Subrate controller

The SRC generates the timing for the circuit board timing, and provides the processor connection and OOB messaging.

Shorting bus interface

This block buffers the S–bus data between the NT9X62CA and the NT9X17 port card. The NT9X62CA paddle board can connect to a maximum of eight NT9X17 port cards. An NT9X25AA paddle board chains the NT9X17 cards together. The NT9X25BA is the last paddle board in the chain. The S–bus terminates at both ends. The NT9X62CA provides terminations at one end. The NT9X25BA provides terminations at the other end.

NT9X62CA (continued)

Frame pulse retiming

This block times the transmit and local frame pulses again before the pulses are applied to the DTRCs.

Identification PROM

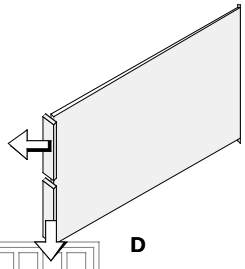
The ID PROM identifies cards.

Signaling

Pin numbers

The pin numbers for NT9X62CA appear in the following figures.

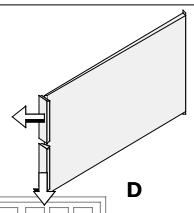
NT9X62CA pin numbers (Part 1 of 2)



	D	C	B	A
1				GND
2				GND
3				GND
4				GND
5				GND
6				GND
7				GND
8				GND
9				GND
10				GND
11				GND
12				GND
13				PBDAS–
14				PBWRT–
15				PBACK–
16	OOB-IN0	SLNKFP–		
17				PBADD2
18				PBADD3
19				PBADD4
20				PBADD5
21	OOB-IN1			PBSDREN
22				PBADD6
23				PBADD7
24				PBID0
25				CPID
26				PBFP61–
27	GND			
28		GND		PBID1
29				HW4
30				
31				
32		GND		
33				
34				
35			TYPE1	
36			HW0	–5V
37			HW1	–5V
38				–5V
39			HW3	–5V
40				GND
41				GND
42				GND
43				GND
44				+5V
45				+5V

NT9X62CA (end)

NT9X62CA pin numbers (Part 2 of 2)



	D	C	B	A
46				+5V
47				+5V
48				+5V
49				+5V
50				+5V
51				+5V
52				+5V
53				+5V
54				+5V
55				+5V
56			PLNKFP–	TYPE0
57				LTVL
58				LRVL
59				STDA0
60				STDA1
61				STDA2
62				STDA3
63				STDA4
64				STDA5
65				STDA6
66	ETYPE0			STDA7
67				STDA8
68				
69				SRDA0
70				SRDA1
71				SRDA2
72				SRDA3
73				SRDA4
74				SRDA5
75				SRDA6
76				SRDA7
77				
78				
79				GND
80				GND
81				GND
82				GND
83			PBDAT24	GND
84			PBDAT25	GND
85			PBDAT26	GND
86			PBDAT27	GND
87			PBDAT28	GND
88			PBDAT29	GND
89			PBDAT30	GND
90	PBC61		PBDAT31	GND

NT9X69AA

Product description

The NT9X69AA is a 16–port DS30 link interface paddle board. The paddle board provides DS30 links between the message switch and the current DS30–based junctor networks (JNET). The paddle board interfaces to the NT9X17DA or CA. This action provides a high–density DS30 interface capability when you retrofit JNETs with enhanced network (ENET) in large offices.

Functional description

The NT9X69AA provides the following functions:

- the interface to 16 DS30 links that interface to JNETs
- non–channelized mapping to all 512 channels of the shorting bus (S–bus)
- a loopback capability for diagnostics
- the standard identification (ID) PROM in all SuperNode packs
- compatibility with the NT9X17DA and CA

Functional blocks

The NT9X69AA has the following functional blocks:

- bit rate converter (BRCX)
- DS30 interface circuits (DS30IF)

Bit rate converter

The BRCX block converts the 8–bit parallel backplane data to serial format. The bit rate changes in this block. The backplane provides a processor interface to allow the shelf processor to communicate with the card. This communication process includes access to an ID PROM, a loopback control register and a power–up status register. The BRCX block also provides miscellaneous timing and address decoding functions.

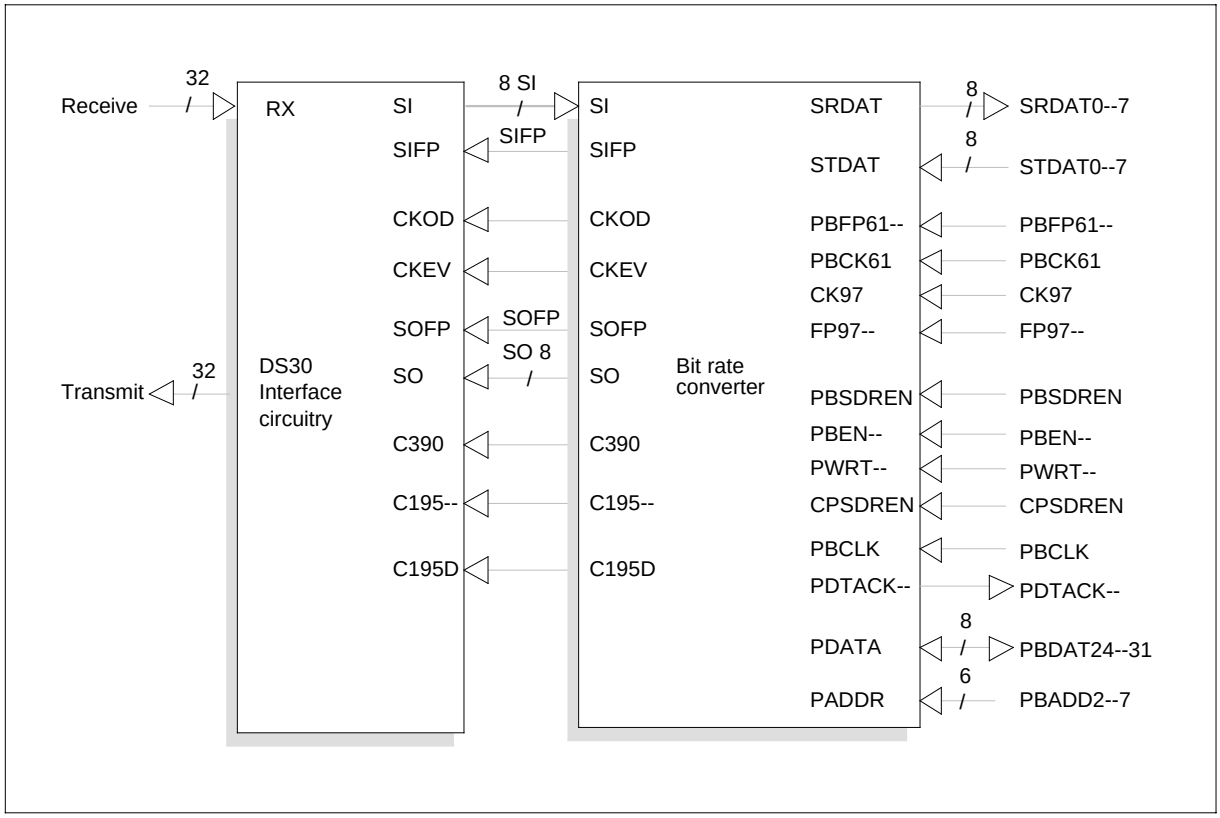
DS30 interface circuits

The W87D provides the DS30IF for two bidirectional DS30 links. The NT5L67AA provides dual bidirectional DS30 link termination.

The relationship of the functional blocks appears in the following figures.

NT9X69AA (continued)

NT9X69AA functional blocks



Signaling

Pin numbers

The pin numbers for NT9X69AA appear in the following tables.

Connector P1 S–bus clocking signals

Pin	Signal
16A	PBCLK
90D	PBCK61
26A	PBFP61-

Connector P1 DS30 clocking signals

Pin	Signal
31A	CK97
30A	FP97

Connector P1 S–bus data interface signals, receive

Pin	Signal	Pin	Signal
69A	SRDAT0	73A	SRDAT4
70A	SRDAT1	74A	SRDAT5
71A	SRDAT2	75A	SRDAT6
72A	SRDAT3	76A	SRDAT7

Connector P1 S–bus data interface signals, transmit

Pin	Signal	Pin	Signal
59A	SRDAT0	63A	SRDAT4
	SRDAT1	64A	SRDAT5
60A			
61A	SRDAT2	65A	SRDAT6
62A	SRDAT3	66A	SRDAT7

Connector P1 S–bus interface signals, miscellaneous

Pin	Signal
27A	CPSDREN
21A	PBSDREN

Connector P1 P–bus signals (Sheet 1 of 2)

Pin	Signal	Pin	Signal
17A	PBADD2	86B	PDATA07
18A	PBADD3	87B	PDATA08
19A	PBADD4	88B	PDATA09

NT9X69AA (continued)

Connector P1 P–bus signals (Sheet 2 of 2)

Pin	Signal	Pin	Signal
20A	PBADD5	89B	PDATA10
22A	PBADD6	90B	PDATA11
23A	PBADD7	13A	PBEN-
83B	PDATA04	14A	PWRT-
84B	PDATA05	15A	PDTACK-
85A	PDATA06		

Connector P2 DS30 port signals, transmit

Pin	Signal	Pin	Signal
1	TXP0	20	TXN0
2	TXP1	21	TXN1
3	TXP2	22	TXN2
4	TXP3	23	TXN3
5	TXP4	24	TXN4
6	TXP5	25	TXN5
7	TXP6	26	TXN6
8	TXP7	27	TXN7
9	TXP8	28	TXN8
10	TXP9	29	TXN9
11	TXP10	30	TXN10
12	TXP11	31	TXN11
13	TXP12	32	TXN12
14	TXP13	33	TXN13
15	TXP14	34	TXN14
16	TXP15	35	TXN15

Connector P2 DS30 port signals, receive

Pin	Signal	Pin	Signal
1	RXP0	20	RXN0
2	RXP1	21	RXN1
3	RXP2	22	RXN2
4	RXP3	23	RXN3
5	RXP4	24	RXN4
6	RXP5	25	RXN5
7	RXP6	26	RXN6
8	RXP7	27	RXN7
9	RXP8	28	RXN8
10	RXP9	29	RXN9
11	RXP10	30	RXN10
12	RXP11	31	RXN11
13	RXP12	32	RXN12
14	RXP13	33	RXN13
15	RXP14	34	RXN14
16	RXP15	35	RXN15

Connector 1 miscellaneous signals (Sheet 1 of 2)

Pin	Signal	Pin	Signal
44A	+5V	40A	GND
45A	+5V	41A	GND
46A	+5V	42A	GND
	+5V		GND
47A	+5V	43A	GND
48A	+5V	79A	GND

NT9X69AA (continued)

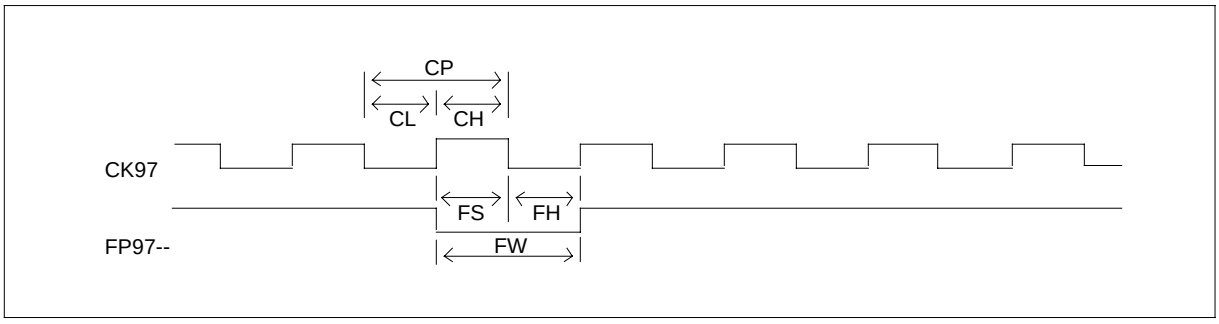
Connector 1 miscellaneous signals (Sheet 2 of 2)

Pin	Signal	Pin	Signal
49A	+5V	80A	GND
50A	+5V	81A	GND
51A	+5V	82A	GND
52A	+5V	83A	GND
53A	+5V	84A	GND
54A	+5V	85A	GND
55A	+5V	86A	GND
1A	+5V	87A	GND
2A	+5V	88A	GND
3A	+5V	89A	GND
4A	+5V	90A	GND
5A	+5V	27D	GND
6A	GND	28C	GND
7A	GND	32C	GND
8A	GND	24A	PBID0
9A	GND	28A	PBID1
10A	GND	89D	PBID2
11A	GND	88D	PBID3
12A	GND	87D	PBID4

Timing

The timing for appears in the following figures.

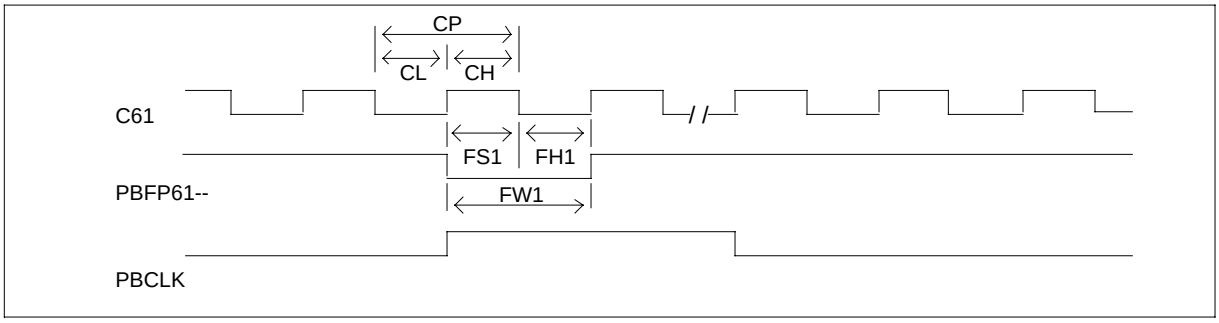
NT9X69AA 10.24 MHz input timing



10.24 MHz input timing

Symbol	Parameter	Min	Nom	Max	Units
CP	CK97 Clock Period		97.7		ns
CH	CK97 Clock High	42.0	49	57.7	ns
CL	CK97 Clock Low	42.0	49	57.7	ns
FW	FP97-, pulse width		49		
FS	FP97-, setup	23.0		60	ns
FH	FP97-, hold	13.0		60	ns

NT9X69AA 16.384 MHz clock input timing



16.384 MHz clock input timing (Sheet 1 of 2)

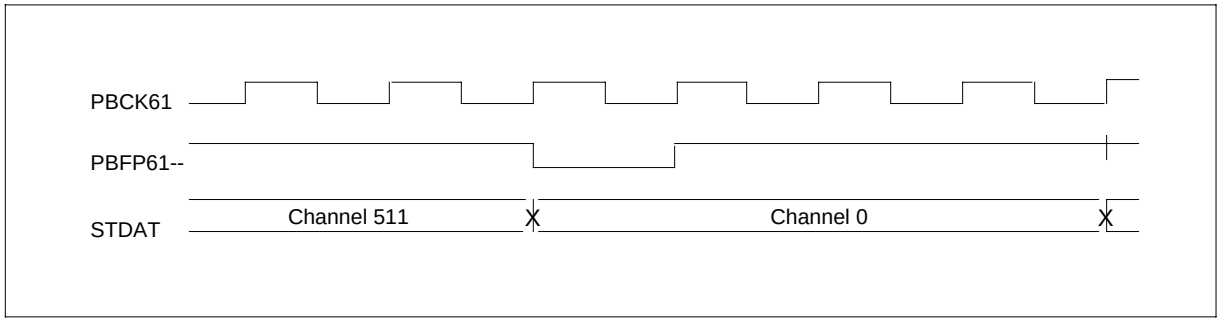
Symbol	Parameter	Min	Nom	Max	Units
CP	CK61 Clock Period		61.0		ns
CH	CK61 Clock High	21.0	30.0	40.0	ns
CL	CK61 Clock Low	21.0	30.0	40.0	ns

NT9X69AA (continued)

16.384 MHz clock input timing (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Units
FS1	PBFP61-, setup	10.0	30.0		ns
FH1	PBFP61-, hold	10.0	30.0		ns
FW1	PBFP61-, pulse width		61		ns

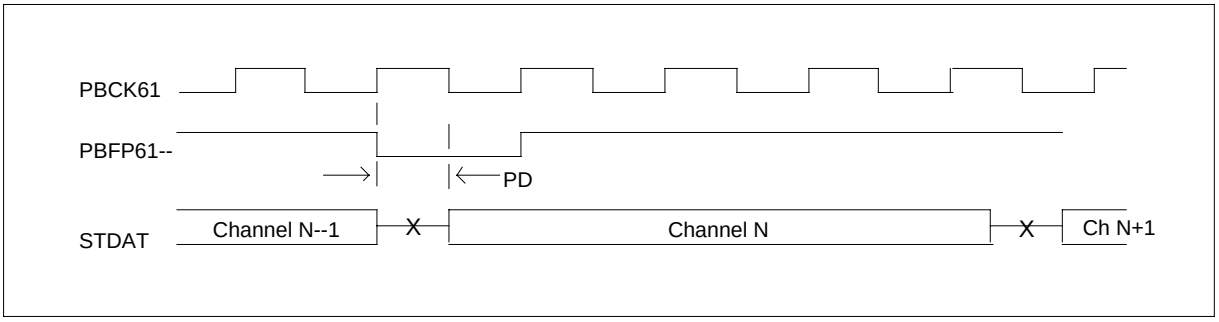
NT9X69AA S–bus to NT9X69AA data timing



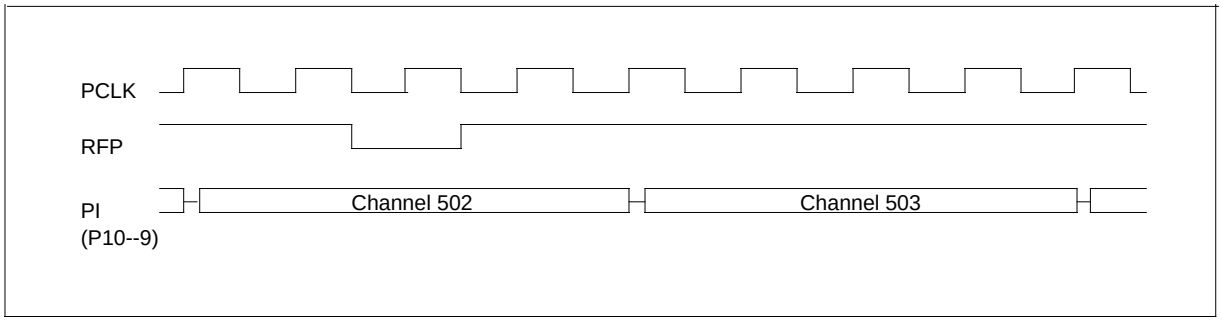
NT9X69AA S–bus to NT9X69AA data timing

Symbol	Parameter	Min	Nom	Max	Units
WS	STDAT data setup	10.0	30		ns
WH	STDAT data hold	10.0	30		ns

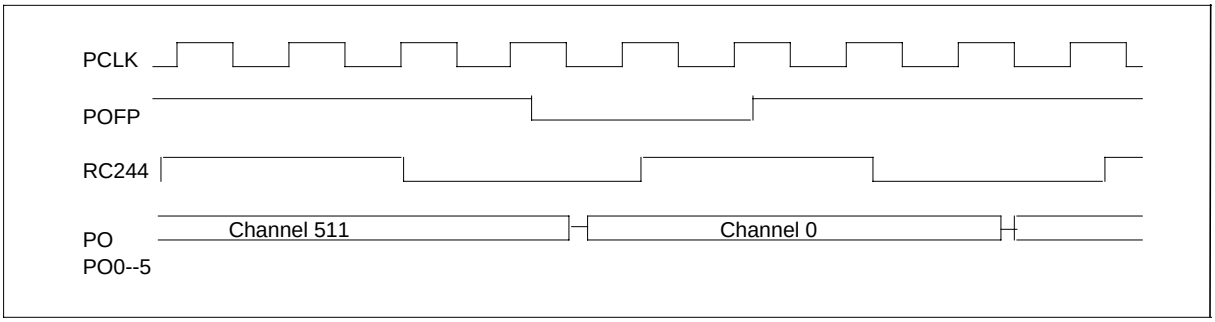
NT9X69AA to S–bus data timing



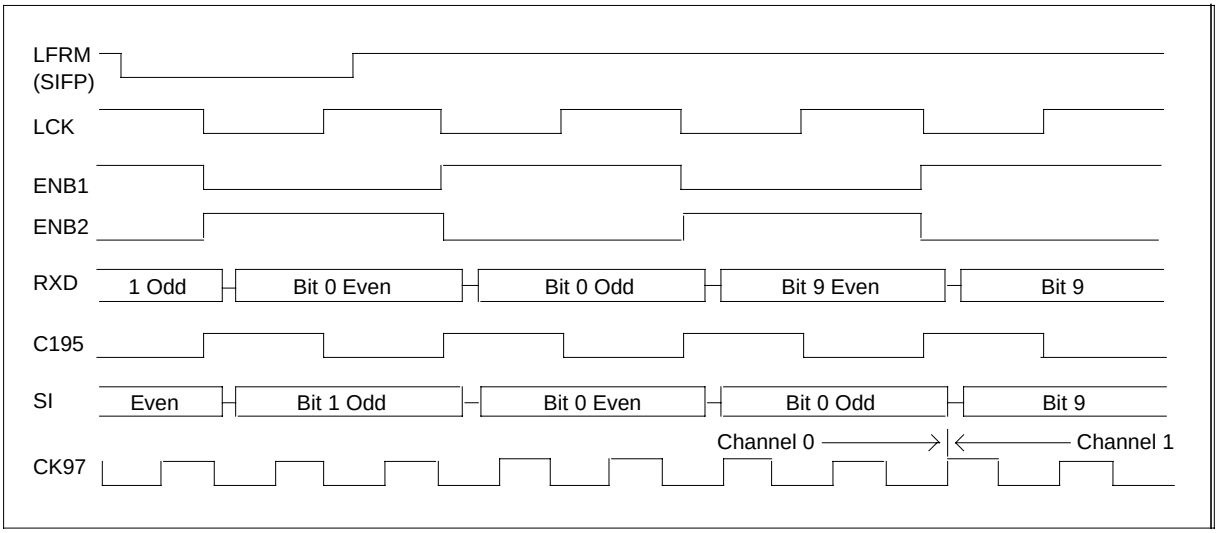
NT9X69AA parallel input port channel timing



NT9X69AA parallel output port channel timing

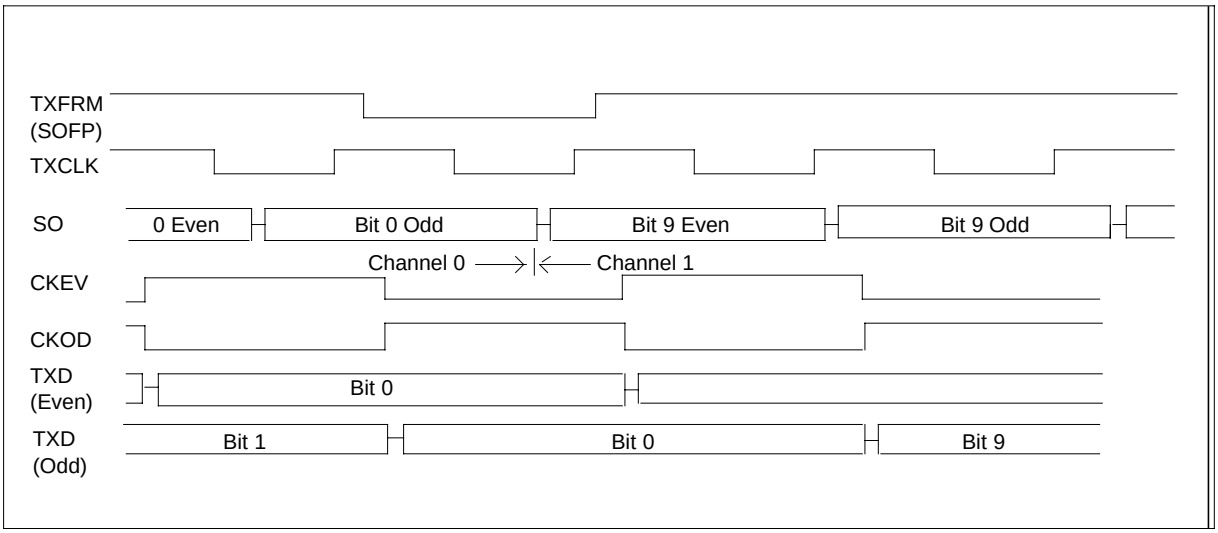


NT9X69AA serial input port channel timing



NT9X69AA (end)

NT9X69AA serial output port channel timing



Technical data

Power requirements

The NT9X69AA requires a minimum supply voltage of minimum 4.5V, a nominal of 5.0V, and a maximum of 5.5V.

NT9X69BA

Product description

The NT9X69BA is a 16–link DS30 paddle board that provides DS30 links between the message switch and the computing module (CM), the current DS30–based junctor networks (JNET), and the input/output controller (IOC).

This card also provides one asynchronous computing module interface card link with out–of–band (OOB) message reception.

Functional description

The NT9X69BA provides the following functions:

- the interface to 16 DS30 links that interface to the CM, JNETs, and IOCs
- non–channelized mapping to all 512 channels of the shorting bus (S–bus)
- a loopback capability for diagnostics
- the standard identification (ID) PROM in all SuperNode packs
- compatibility with the NT9X17BB and the NT9X17DA
- DS30 link 0 OOB reception on one DS30 link

Functional blocks

The NT9X69BA has the following functional blocks:

- bit rate converter (BRCX)
- DS30 interface circuits (DS30IF)

Bit rate converter

The BRCX converts the 8–bit parallel backplane data to serial format and changes the bit rate. The backplane provides a processor interface that allows the shelf processor and the NT9X69BA to communicate. The interface provides access to the following:

- an ID PROM
- loopback control registers
- OOB message registers
- a power–up status register

The BRCX block also provides miscellaneous timing and address decoding functions.

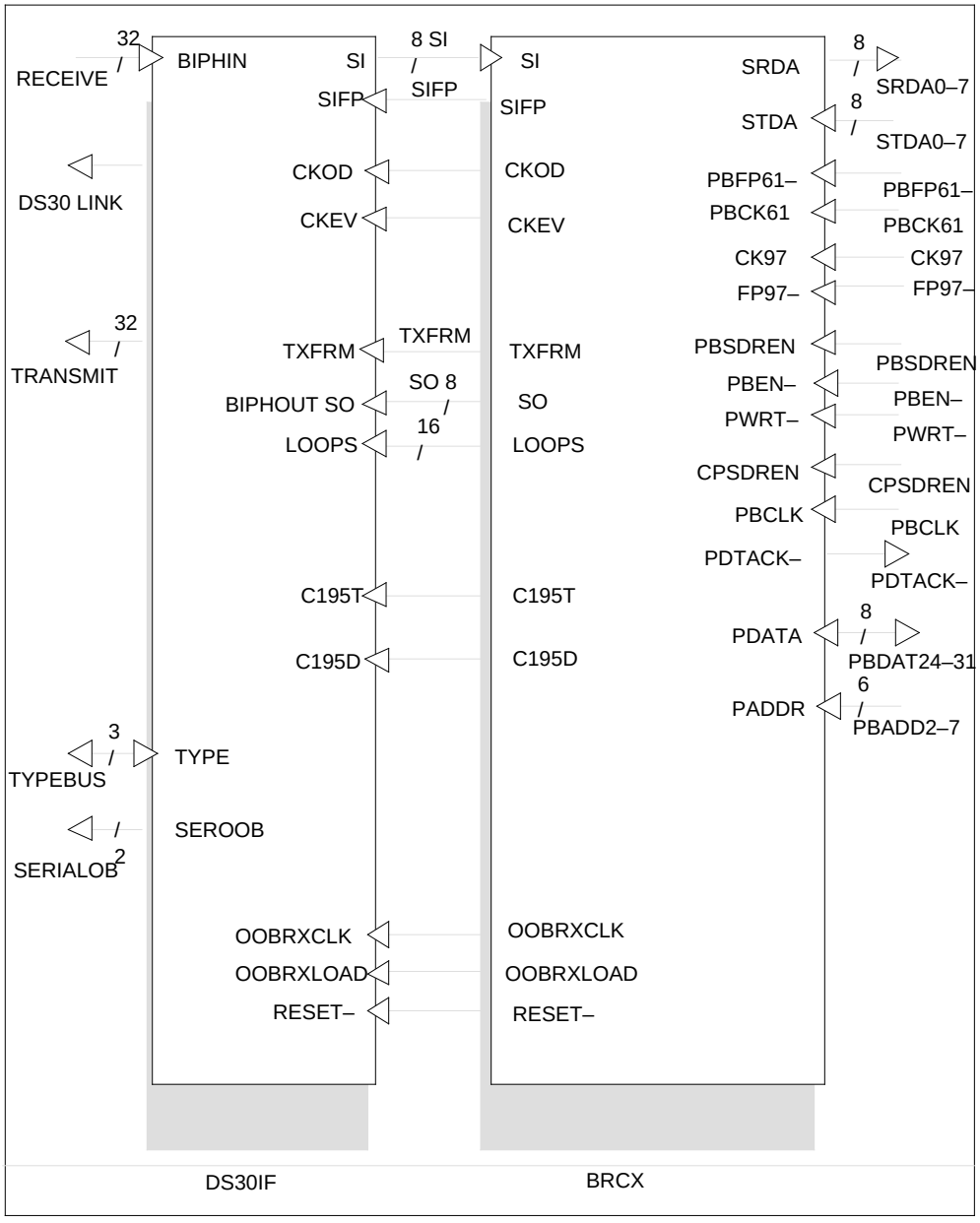
NT9X69BA (continued)

DS30 interface circuits

Two N03s and one W87D provide the DS30IF for 16 bidirectional DS30 links. The NT5L67AA provides dual bidirectional DS30 link termination.

The relationship between the functional blocks appear in the following figure.

NT9X69BA functional blocks



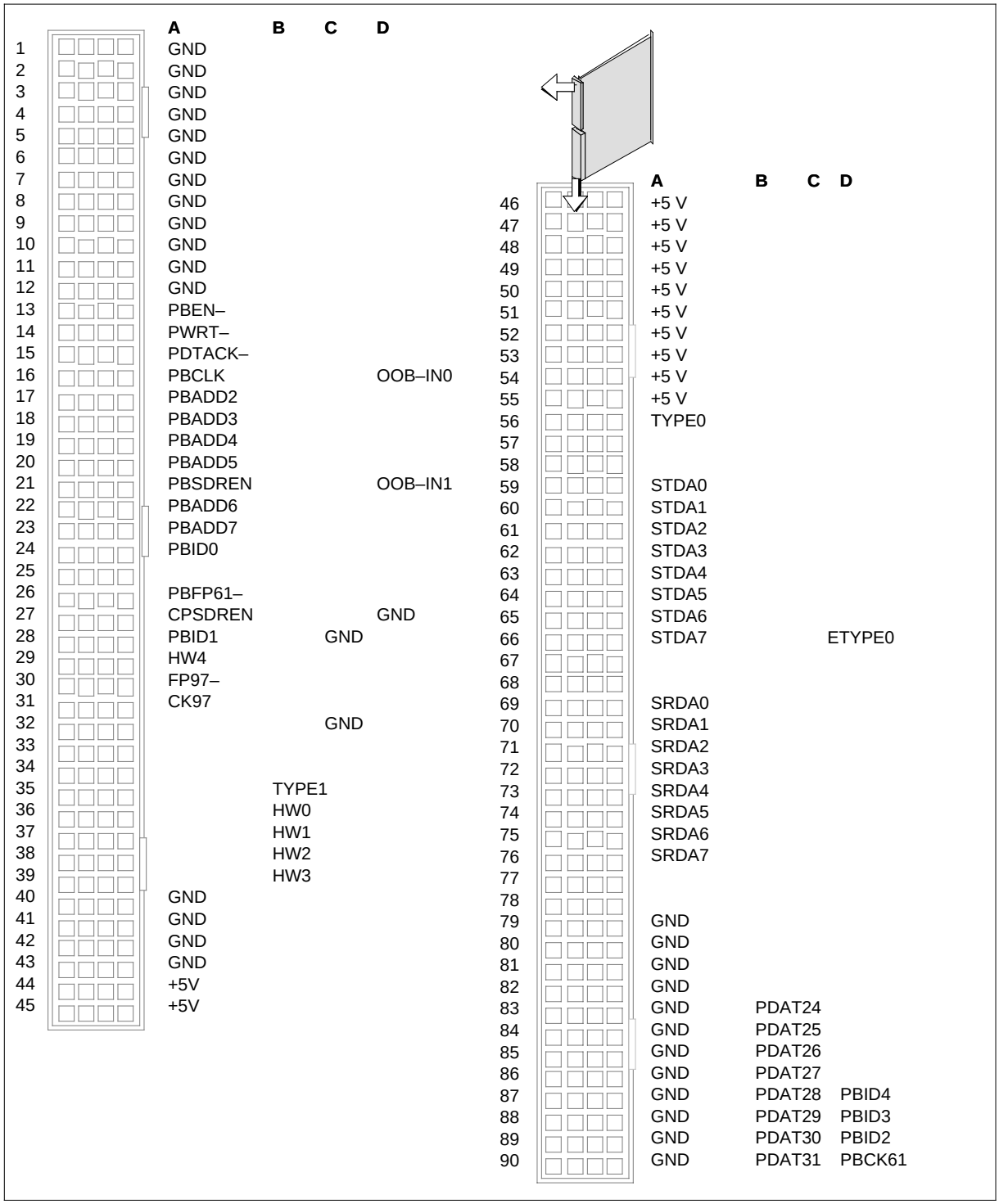
Signaling

Pin numbers

The pin numbers for the NT9X69BA appear in the following figure.

NT9X69BA (continued)

NT9X69BA pin numbers



	A	B	C	D
1	GND			
2	GND			
3	GND			
4	GND			
5	GND			
6	GND			
7	GND			
8	GND			
9	GND			
10	GND			
11	GND			
12	GND			
13	PBEN–			
14	PWRT–			
15	PDTACK–			
16	PBCLK			OOB–IN0
17	PBADD2			
18	PBADD3			
19	PBADD4			
20	PBADD5			
21	PBSDREN			OOB–IN1
22	PBADD6			
23	PBADD7			
24	PBID0			
25				
26	PBFP61–			
27	CPSDREN			GND
28	PBID1		GND	
29	HW4			
30	FP97–			
31	CK97			
32			GND	
33				
34				
35		TYPE1		
36		HW0		
37		HW1		
38		HW2		
39		HW3		
40	GND			
41	GND			
42	GND			
43	GND			
44	+5V			
45	+5V			

	A	B	C	D
46	+5 V			
47	+5 V			
48	+5 V			
49	+5 V			
50	+5 V			
51	+5 V			
52	+5 V			
53	+5 V			
54	+5 V			
55	+5 V			
56	TYPE0			
57				
58				
59	STDA0			
60	STDA1			
61	STDA2			
62	STDA3			
63	STDA4			
64	STDA5			
65	STDA6			
66	STDA7			ETYPE0
67				
68				
69	SRDA0			
70	SRDA1			
71	SRDA2			
72	SRDA3			
73	SRDA4			
74	SRDA5			
75	SRDA6			
76	SRDA7			
77				
78				
79	GND			
80	GND			
81	GND			
82	GND			
83	GND	PDAT24		
84	GND	PDAT25		
85	GND	PDAT26		
86	GND	PDAT27		
87	GND	PDAT28		PBID4
88	GND	PDAT29		PBID3
89	GND	PDAT30		PBID2
90	GND	PDAT31		PBCK61

The pin numbers for the DS30 link signals appear in the following tables.

Connector J1 DS30 link signals(transmits)

Pin	Signal	Pin	Signal
1	TXP0	20	TXN0
2	TXP1	21	TXN1
3	TXP2	22	TXN2
4	TXP3	23	TXN3
5	TXP4	24	TXN4
6	TXP5	25	TXN5
7	TXP6	26	TXN6
8	TXP7	27	TXN7
9	TXP8	28	TXN8
10	TXP9	29	TXN9
11	TXP10	30	TXN10
12	TXP11	31	TXN11
13	TXP12	32	TXN12
14	TXP13	33	TXN13
15	TXP14	34	TXN14
16	TXP15	35	TXN15

Connector J2 DS30 link signals(receive) (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	RXP0	20	RXN0
2	RXP1	21	RXN1
3	RXP2	22	RXN2
4	RXP3	23	RXN3
5	RXP4	24	RXN4

NT9X69BA (continued)

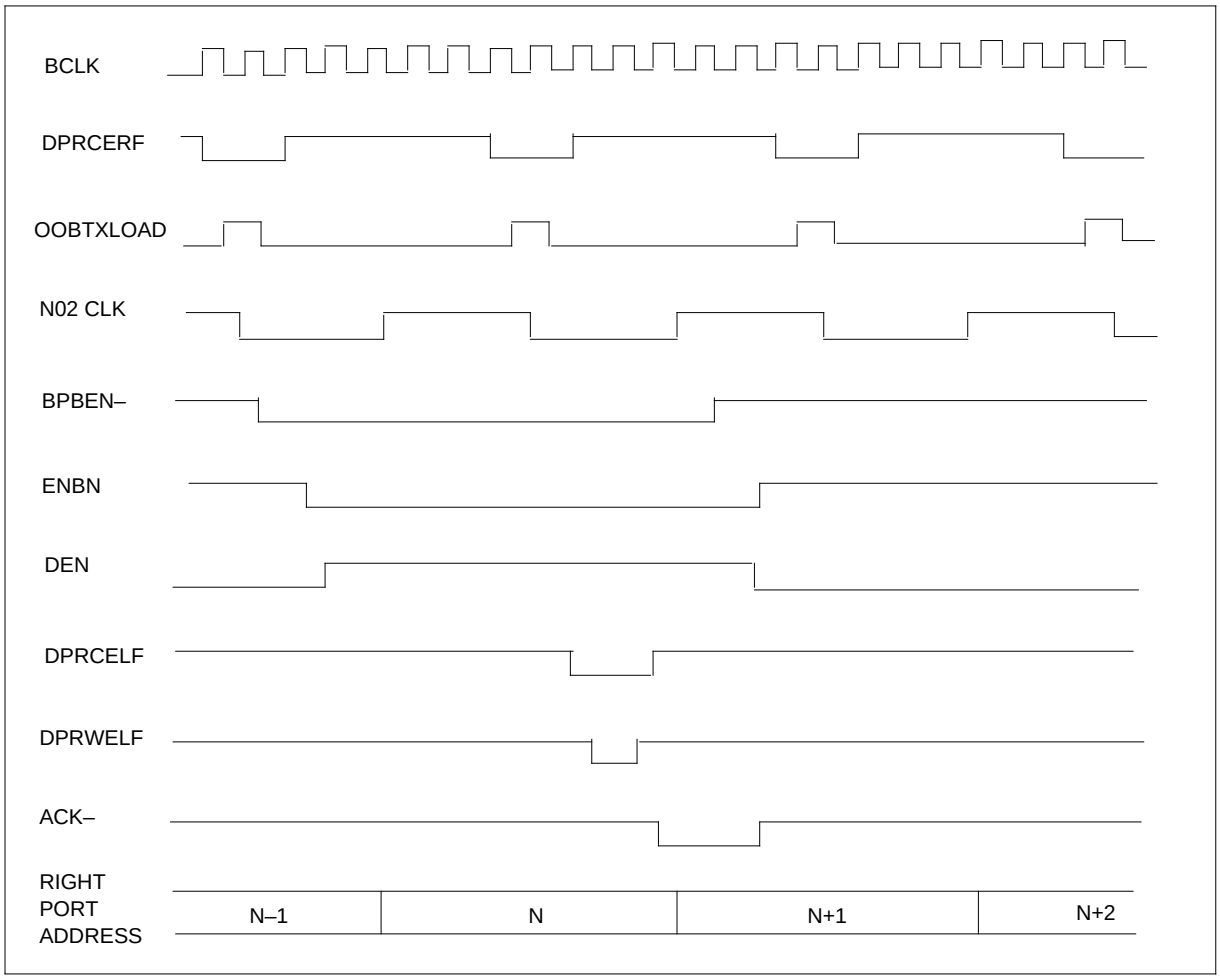
Connector J2 DS30 link signals(receive) (Sheet 2 of 2)

Pin	Signal	Pin	Signal
6	RXP5	25	RXN5
7	RXP6	26	RXN6
8	RXP7	27	RXN7
9	RXP8	28	RXN8
10	RXP9	29	RXN9
11	RXP10	30	RXN10
12	RXP11	31	RXN11
13	RXP12	32	RXN12
14	RXP13	33	RXN13
15	RXP14	34	RXN14
16	RXP15	35	RXN15

Timing

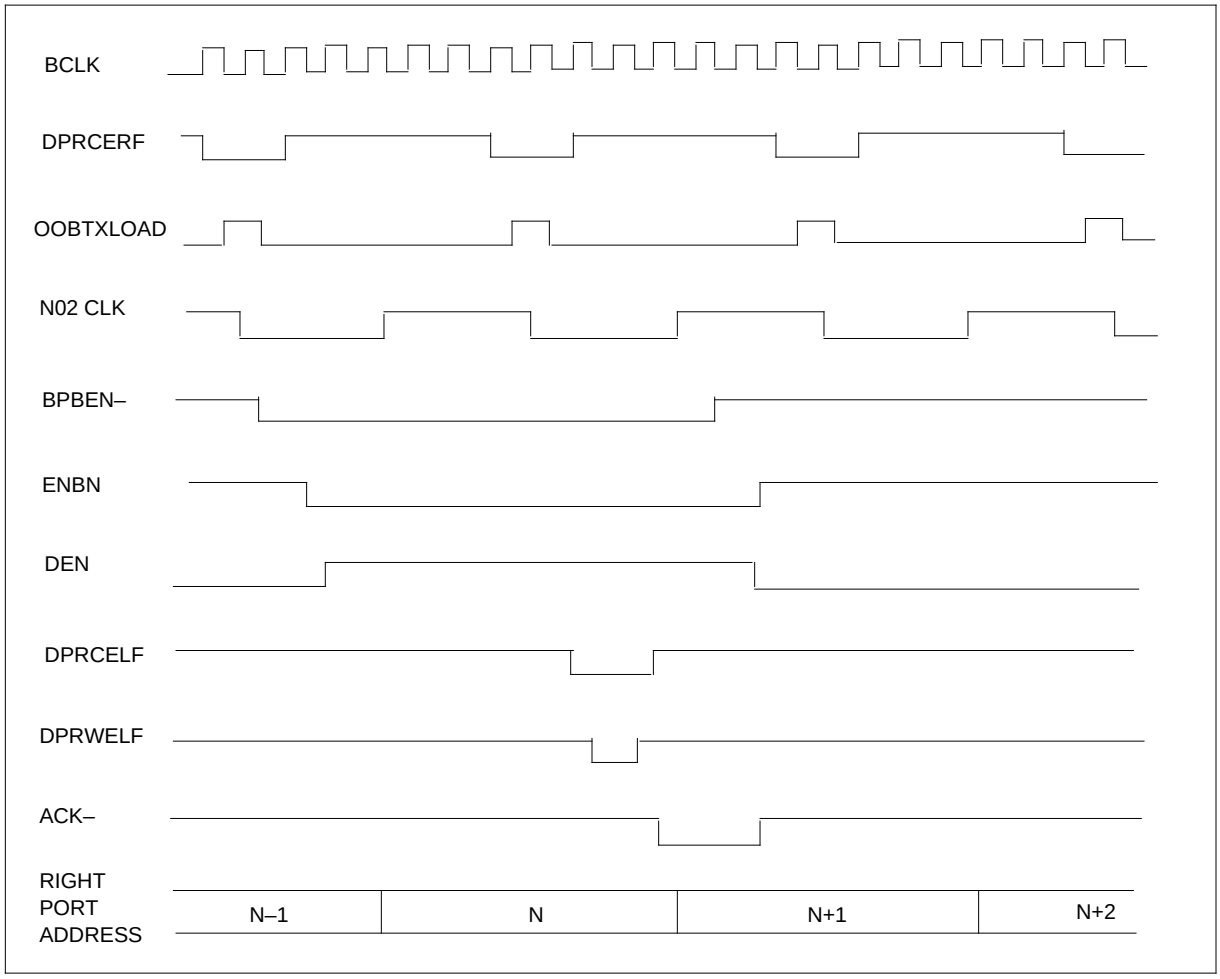
The timing for the NT9X69BA appears in the following figures.

CLRPCM timing diagram

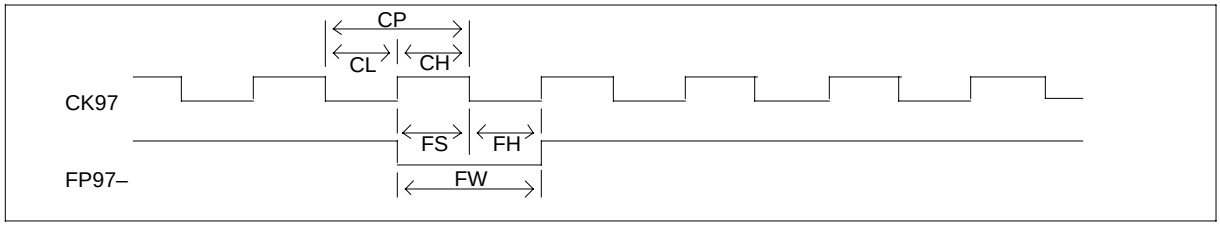


NT9X69BA (continued)

Dual–port RAM timing



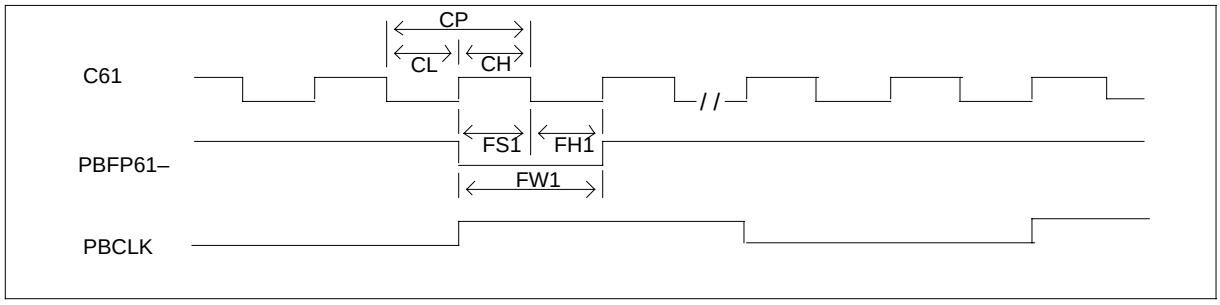
10.24 MHz input timing



10.24 MHz clock input timing

Symbol	Parameter	Min	Nom	Max	Units
CP	CK97 clock period		97.7		ns
CH	CK97 clock high	42.0	49	57.7	ns
CL	CK97 clock low	42.0	49	57.7	ns
FW	FP97-, pulse width		97.7		
FS	FP97-, setup	20.0			ns
FH	FP97-, hold	10.0			ns

16.384 MHz clock input timing



16.384 MHz clock input timing (Sheet 1 of 2)

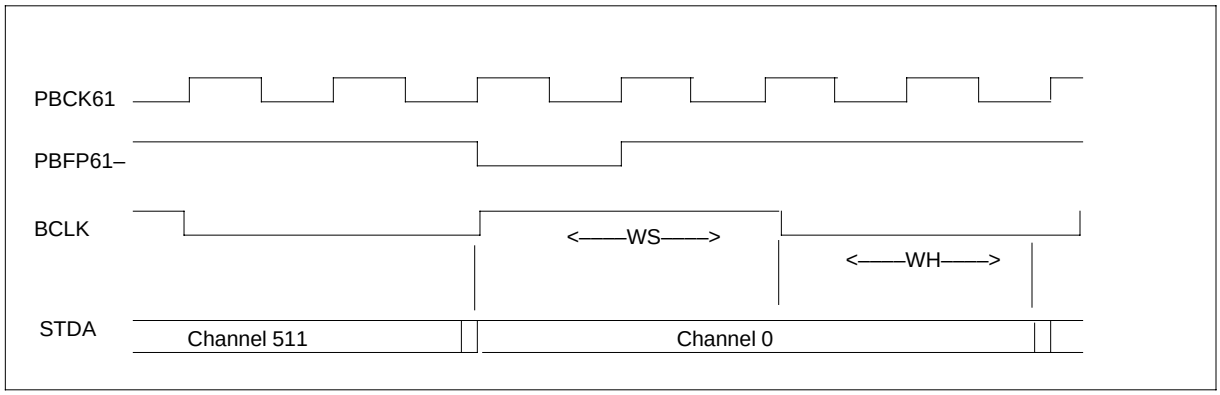
Symbol	Parameter	Min	Nom	Max	Units
CP	C61 clock period		61.0		ns
CH	C61 clock high	21.0	30.5	40.0	ns
CL	C61 clock low	21.0	30.5	40.0	ns
FS1	PBFP61-, setup	20.0			ns

NT9X69BA (continued)

16.384 MHz clock input timing (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Units
FH1	PBFP61-, hold	10.0			ns
FW1	PBFP61-, pulse width		61		ns

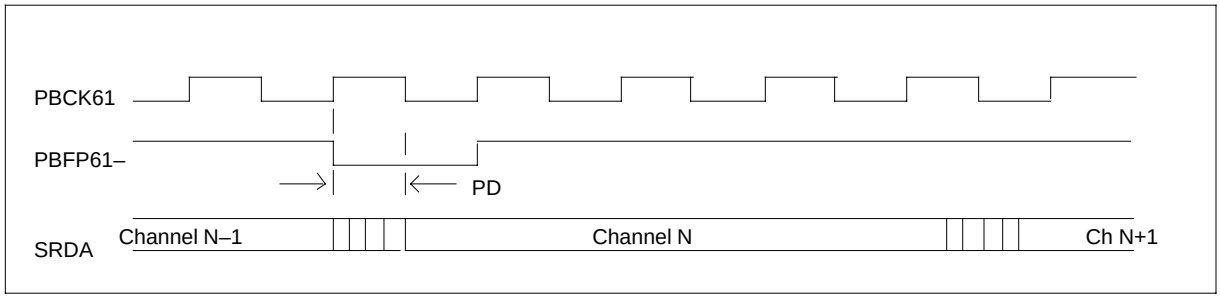
S–bus to NT9X69BA data timing



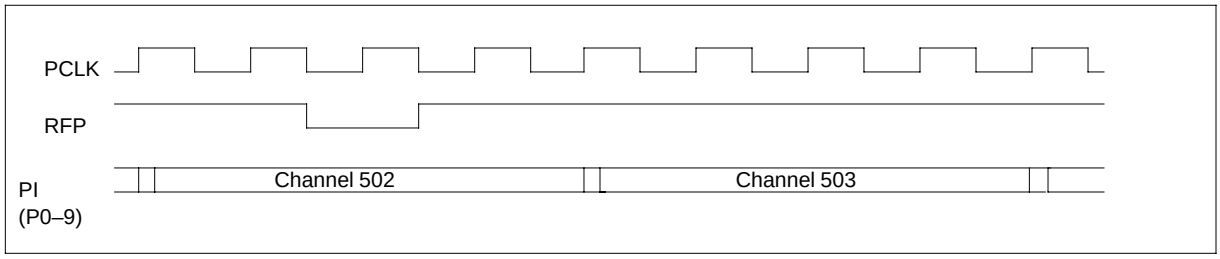
S–bus to NT9X69BA data timing

Symbol	Parameter	Min	Nom	Max	Units
WS	STDA data setup	10.0			ns
WH	STDA data hold	0			ns

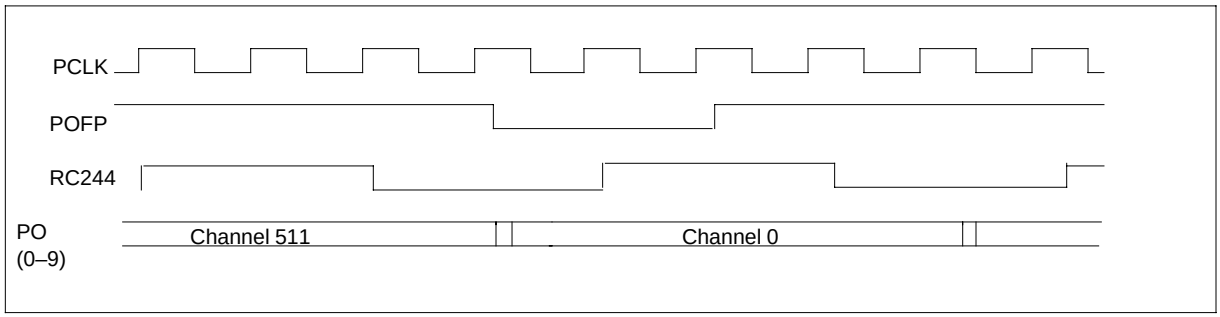
NT9X69AA to S–bus data timing



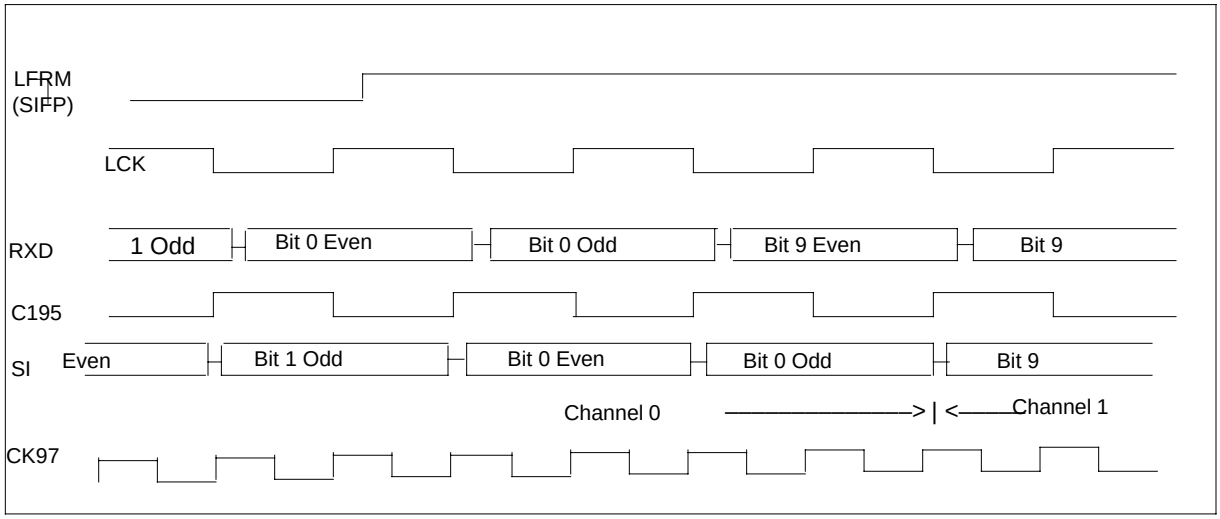
Parallel input link channel timing



Parallel output link channel timing

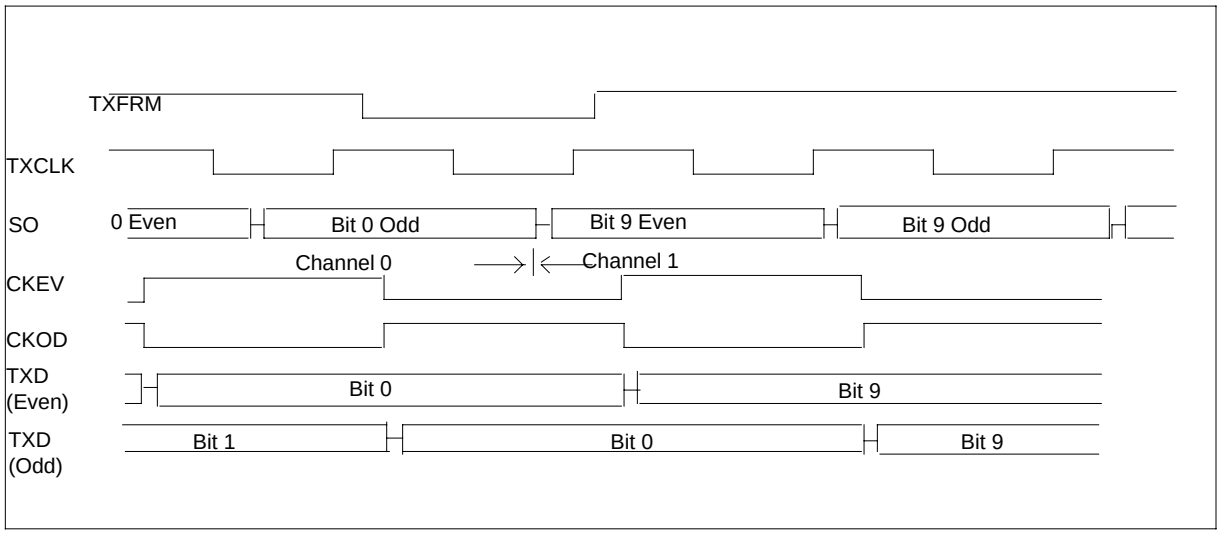


Serial input link channel timing

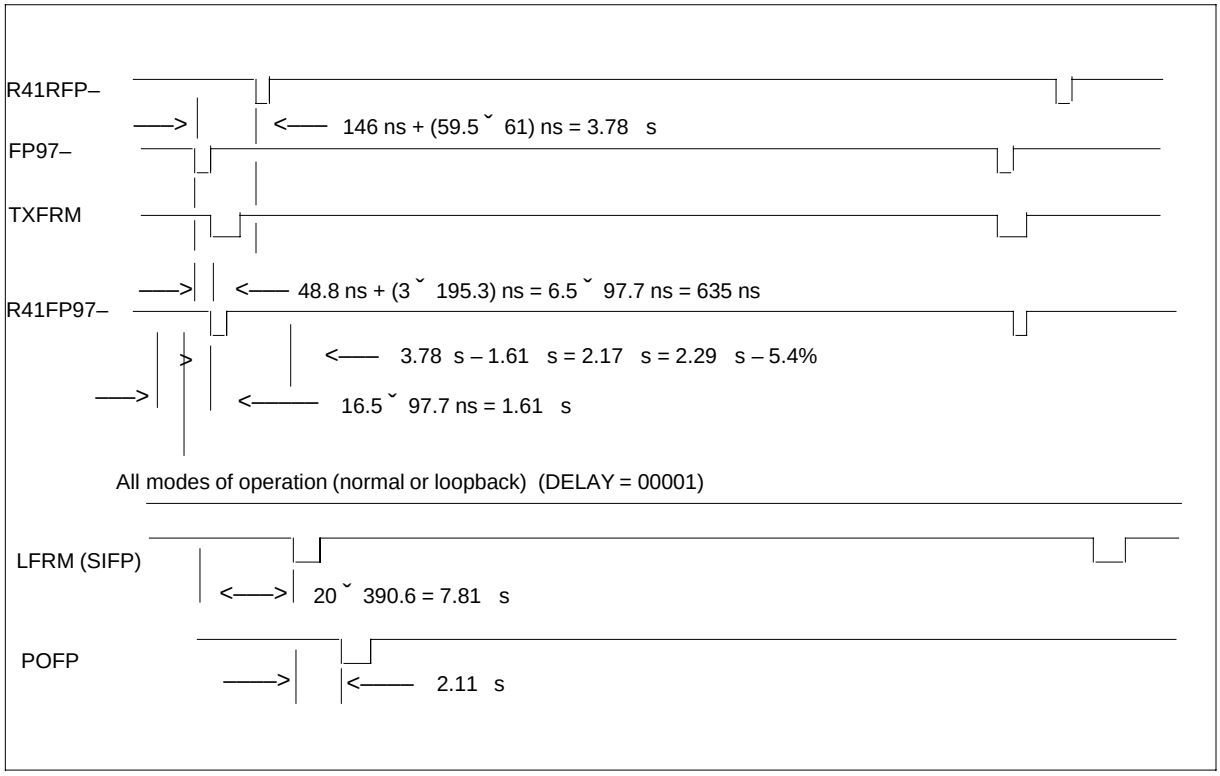


NT9X69BA (continued)

Serial output link channel timing



Frame pulse timing



Technical data

Power requirements

The NT9X69BA requires a minimum supply voltage of 4.5V, a nominal of 5.0V, and a maximum of 5.5V.

NT9X70AA

Product description

The link peripheral processor cabinet (LPP) is a DMS SuperNode type equipment cabinet for the DMS signaling transfer point (DMS-STP). The cabinet contains the following types of peripheral modules (PM):

- a link interface module (LIM)
- common channel signaling #7 (CCS7) link interface units (LIU7)

The LIM controls messages between link interface units in the LPP and between the LPP and the DMS-bus. A LIM contains two local message switches (LMS) and two frame transport buses (F-bus).

The CCS7 LIU7s are sets of cards on the link interface shelves (LIS). Each LIS contains a maximum of eight sets of LIU7 cards.

Note: An optional upgrade kit (NT9X70ZA) is available for the international market to upgrade existing NT9X70AA LPP cabinets to the Fiberized Link Processor Peripheral (FLPP) cabinet.

Parts

The NT9X70AA contains the following parts:

- A0323984—Cooling unit (CU)
- NT9X03AA—Frame supervisory panel (FSP)
- NT9X71AA—Local message switch shelf (LMS)
- NT9X72—Link interface shelf
- CCS7 LIU7
- F-bus

Cooling unit

The core CU provides mechanical ventilation for equipment in the link interface module cabinet.

Frame supervisory panel

The NT9X03AA FSP provides alarm, maintenance, and miscellaneous supervisory functions. The FSP is in the top shelf position in the NT9X70AA. To access the front and rear of the NT9X03AA open the cabinet doors. An associated frame light is visible when the doors are closed.

Power from the power distribution center frame comes to the FSP. Power transmits to different power supply modules in the cabinet. The NT9X30AA

and NT9X31AA power converters are examples of these modules. The power supply modules contains all power control. Power control is separate from the FSP.

Local message switch shelf

The LMS shelf contains two LMSs, LMS0 and LMS 1. Together, the LMs form a LIM. The LIM is a PM that controls messaging between link interface units (LIU) in an LPP. The LIM also controls messaging between the LPP and the DMS-bus.

A LIM contain the two LMSs and two frame transport buses, frame transport bus (F-bus) 0 and F-bus 1.

Link interface shelf

The CCS7 LUI7 is a PM that processes messages. These messages enter and leave an LPP through a separate signaling data link. Each LIU7 consists of the following set of cards and paddle boards (PB):

- NT9X75—Processor bus (P-bus) to F-bus interface card
- NT9X13CA—Link general processor card
- NT9X76—Signaling terminal card
- NT9X78AA or BA—DS-0A interface PB

The LIS contains LIU7s. A maximum of eight sets of LIU7 cards can be in a link interface shelf. A total of 24 LIU7s can be in an LPP.

Frame transport bus

An F-bus provides data communication between a local message switch and the CCS7 LIU7s provisioned in an LPP. The F-bus has eight bits. To make sure reliability is present, an LPP provides two load-sharing F-buses. Each F-bus is for the two LMSs:

- F-bus 0 is for LMS 0
- F-bus 1 is for LMS 1

The F-bus contains two types of functional resources:

- taps
- medium

Taps are bus access points. For an F-bus, a tap is part of one of the following:

- the F-bus adapter card (NT9X73) an LMS uses
- the P-bus to F-bus interface card (NT9X75) an LIU7 uses

NT9X70AA (continued)

Note: The NT9X73 rate adapter card is an F-bus tap. The man-machine interface (MMI) for the DMS-STP includes the rate adapter card. The card is part of the medium because the card controls the F-bus. At the PM level of the MAP, the F-bus is the bus.

Medium is the F-bus structure. The structure contains a number of different cards, PBs, and interconnecting cables that link the F-bus components. The F-bus components are dispersed in the LPP. Cards and PBs are provisioned as part of the LMS shelf and all three link interface shelves.

The F-bus rate adapter card (NT9X73) performs rate translation. At the LMS shelf, the card converts messages between the Transaction bus (T-bus) of the LMS and the F-bus. The F-bus extender PB (NT9X79BA) provides an interface to the F-bus ribbon cables. The cables are intershelf F-bus cables that provide F-bus communication between the shelves of the LPP.

At each of the three link interface shelves, the F-bus extender PB is the connection point for intershelf F-bus cabling. The F-bus extender PB has two versions, the NT9X79AA and BA.

The NT9X79AA F-bus extender PB extends the intershelf F-bus ribbon cables between shelves in the LPP.

The NT9X79BA F-bus extender PB extends the intershelf ribbon cables between shelves in the LPP. The extender PB also provides resistant termination for the F-bus in the top and bottom shelves of the LPP. The NT9X79BA card can be in the LMS shelf. When this process occurs, the card accepts the DS-0A composite clock signal for the associated LMS.

The LMS repeater card (NT9X74) clocks all F-bus signaling between the intershelf F-bus cables and the intrashelf F-bus again. The NT9X74 repeats all F-bus signaling between the bus cables and the intrashelf. The intrashelf F-bus contains F-bus cards and the backplane of the shelf. Every F-bus repeater card can drive one of the two separate intrashelf F-buses.

The intra F-bus terminator PBs (NTEX20AA and NTEX20BA) provide intrashelf F-bus termination. The NTEX20AA provides intrashelf termination for F-bus 0 signals. The NTEX20BA provides intrashelf termination for F-bus 1 signals.

The backplane of the shelf provides intrashelf F-bus communication. The LIU7s access the two intrashelf F-buses through the P-bus to F-bus interface card (NT9X75). This card serves as the F-bus tap.

The F-bus contains the following:

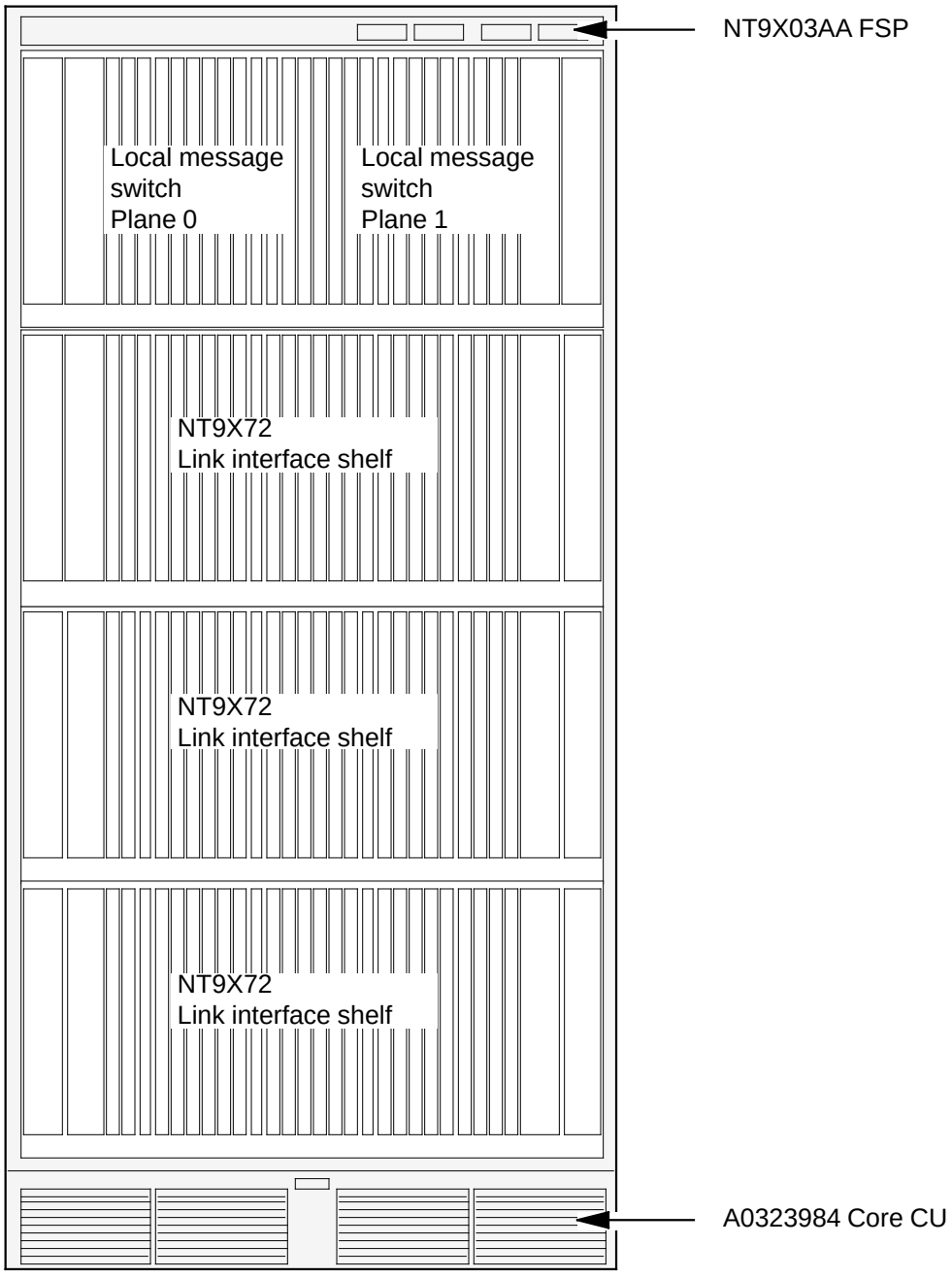
- NTEX20AA—Intra F-bus 0 termination PB (on LIS)
- NTEX20BA—Intra F-bus 1 termination PB (on LIS)
- NT9X73AA—F-bus rate adapter card (on LMS)
- NT9X74—F-bus repeater with termination card (on LIS shelf)
- NT9X79AA—F-bus extender PB (on top and middle LIS)
- NT9X79BA—F-bus extender PB (on LMS)
- NT9X79BA—F-bus extender PB (on bottom LIS)

Design

The NT9X70AA design appears in the following figure.

NT9X70AA (end)

NT9X70AA parts



Product description

The link peripheral processor cabinet (LPP) is a DMS SuperNode type equipment cabinet for the DMS signaling transfer point (DMS-STP). The LPP contains two types of peripheral modules (PM):

- a link interface module (LIM)
- Common Channel Signaling 7 (CCS7) link interface units (LIU7)

The LIM controls messaging between link interface units in the LPP and between the LPP and the DMS-bus. A LIM consists of two local message switches (LMS) and two frame transport buses (F-bus).

The LIU7s are sets of cards, two cards and one paddle board (PB), mounted on the link interface shelves (LIS). Each of the three LISs mounted in the NT9X70BA cabinet contain a maximum of 12 sets of LIU7 cards.

The NT9X70BA replaces the NT9X70AA cabinet. The NT9X70AA cabinet had a capacity of three sets of eight LIU7 cards.

Note: An optional ungrade kit (NT9X70ZA) is available for the international market to upgrade existing NT9X70BA LPP cabinets to the Fiberized Link Processor Peripheral (FLPP) cabinet.

Parts

The NT9X70BA consists of the following parts:

- A0323984—Cooling unit (CU)
- NT9X03AA—Frame supervisory panel (FSP)
- NT9X71AB—Local message switch shelf (LMS)
- NT9X72BA—Link interface shelf
- CCS7 LIU7
- Frame transport bus (F-bus)

Cooling unit

The A0323984 core cooling unit provides mechanical ventilation for equipment in the link interface module cabinet.

Frame supervisory panel

The NT9X03AA FSP provides alarm, maintenance and different supervisory functions. The FSP is in the top shelf position in the NT9X70BAAA. To access

NT9X70BA (continued)

the front and rear of the NT9X03AA, open the cabinet doors. An associated frame light is visible when doors are closed or open.

Power from the power distribution center frame comes into the FSP. The FSP distributes the power to different power supply module in the cabinet, like the NT9X30AA and NT9X31AA power converters. All power control is in the power supply modules. Power control is independent of the FSP.

Local message switch shelf

The LMS shelf contains two LMSs, LMS0 and LMS 1. The two LMSs form a LIM. The LIM is a PM that controls messaging between link interface units in a LPP. The LIM controls messaging between the LPP and the DMS-bus.

A LIM contains two LMSs and two frame transport buses, F-bus 0 and F-bus 1.

Link interface shelf

The CCS7 LUI7 is a PM that processes messages that enter and leave an LPP through a signaling data link. Each LIU7 consists of two circuit cards and one PB:

- NTEX22AA—Link general processor card
- NT9X76AA—Signaling terminal card
- NT9X78BA—DS-0A or V.35 interface PB

The LIS houses LIU7. A link interface shelf can have a maximum of 12 sets of LIU7 cards provisioned. These cards make total of 36 LIU7s in an NT9X70BA LPP.

Frame transport bus

A F-bus is an 8 bit bus. The F-bus provides data communication between a local message switch and the LIU7s provisioned in a LPP. There are two load-sharing F-buses in an LPP to make sure of reliability. Each F-bus is dedicated to one of the two LMSs. The F-bus 0 is dedicated to LMS 0. The F-bus 1 is dedicated to LMS 1.

The F-bus consists of the following two types of functional resources:

- taps
- medium

Taps are bus access points. For an F-bus, a tap can be part of the F-bus adapter card (NT9X73) that an LMS uses. The tap can be part of the processor bus (P-bus) to F-bus interface card (NT9X75) that an LIU7 uses.

Note: The NT9X73 rate adapter card is an F-bus tap. The man-machine interface (MMI) for the DMS-STP includes the rate adapter card as part of the medium. The MMI includes the card as part of the medium because it controls the F-bus. At the PM level of the maintenance and administrative position (MAP), the F-bus is the bus.

Medium is the F-bus structure. The structure consists of a number of cards, PBs, and cables that interconnect and link the F-bus parts. The F-bus parts are distributed in the LPP. The cards and PBs are provisioned as part of the LMS shelf and all three link interface shelves.

At the LMS shelf the F-bus rate adapter card (NT9X73) performs rate translation. The NT9X73 converts messages between the transaction bus (T-bus) of the LMS and the F-bus. The F-bus extender PB (NT9X79BA) provides the interface to the F-bus ribbon cables. The F-bus ribbon cables provide F-bus communication between the shelves of the LPP. The cables are the intershelf F-bus.

At each of the three link interface shelves, the F-bus extender PB serves as the connection point for intershelf F-bus cabling. There are two versions of the F-bus extender PB, the NT9X79AA and BA.

The NT9X79AA F-bus extender PB extends the intershelf F-bus ribbon cables between shelves in the LPP.

The NT9X79BA F-bus extender PB extends the intershelf ribbon cables between shelves in the LPP. The F-bus extender PB provides resistive termination for the F-bus in the top and bottom shelves of the LPP. When the NT9X79BA is in the LMS shelf, the NT9X79BA accepts the DS-0A composite clock signal for the associated LMS.

The LMS repeater card (NT9X74) clocks again and repeats F-bus signaling between the intershelf F-bus cables and the intrashelf F-bus. The intrashelf F-bus consists of the F-bus cards and the backplane of the shelf. Each F-bus repeater card can drive one of the two intrashelf F-buses.

The intra F-bus terminator PBs, NTEX20AA and NTEX20BA, provide intrashelf F-bus termination. The NTEX20AA provides intrashelf termination for F-bus 0 signals. The NTEX20BA provides intrashelf termination for F-bus 1 signals.

NT9X70BA (continued)

The backplane of the shelf provides intrashelf F-bus communication. The LIU7s access the two intrashelf F-buses through the P-bus to F-bus interface card (NT9X75). The NT9X75 serves as the F-bus tap.

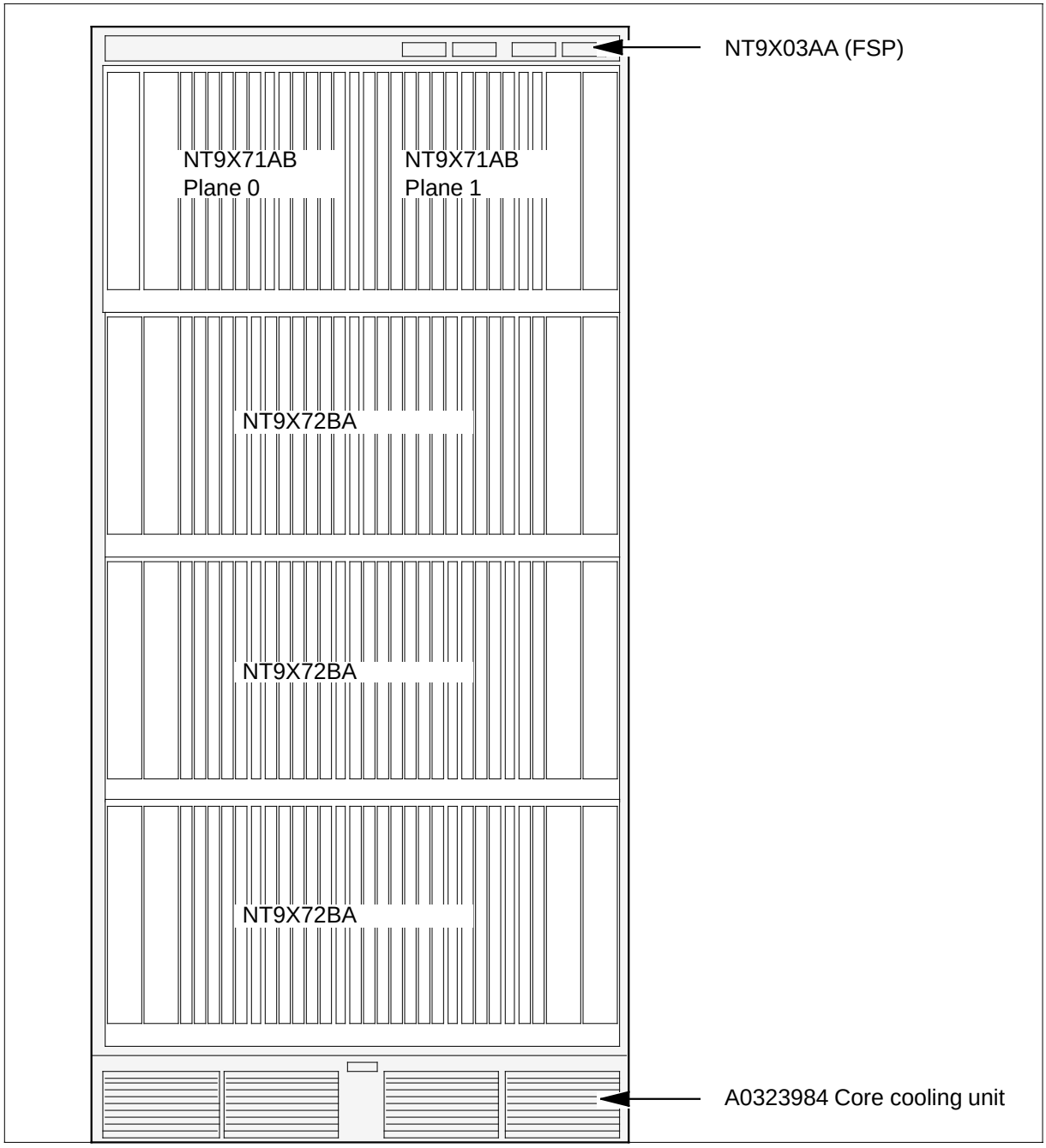
The F-bus consists of the following parts:

- NTEX20AA—Intra F-bus 0 termination PB (located on LIS)
- NTEX20BA—Intra F-bus 1 termination PB (located on LIS)
- NT9X73AA—F-bus rate adapter card (located on LMS)
- NT9X74—F-bus repeater with termination card (on LIS shelf)
- NT9X79AA—F-bus extender PB (on top and middle LIS)
- NT9X79BA—F-bus extender PB (located on LMS)
- NT9X79BA—F-bus extender PB (located on bottom LIS)

Design

The design of the NT9X70BA appears in the following figure.

NT9X70BA parts



Note: This figure is not drawn to scale.

NT9X70BB

Product description

The NT9X70BB link interface module (LIM) enhanced cabinet is a DMS SuperNode type equipment cabinet for the DMS signaling transfer point (DMS-STP). The NT9X70BB contains two of the following types of peripheral modules (PM):

- link interface module (LIM)
- link interface unit (LIU7)
- Ethernet interface unit (EIU)
- frame relay interface unit (FRIU)

The LIM controls messaging between interface units in the LIM and between the LIM and the DMS-bus. An LIM consists of two local message switches (LMS) and two frame transport buses (F-bus).

The LIU7s are sets of cards, two cards and one paddle board (PB), mounted on the link interface shelves (LIS). Each of the three LISs mounted in the NT9X70BB cabinet contains a maximum of 12 sets of three interface cards.

The NT9X70BB replaces the NT9X70AA cabinet. The NT9X70AA has a capacity of three sets of eight interface cards.

Parts

The NT9X70BB has following parts:

- A0377580—core cooling unit, -48V (dc)
- A0382102—core cooling unit, -60V (dc)
- NT9X03AA—SuperNode frame supervisory panel, -48V (dc)
- NT9X03BA—SuperNode frame supervisory panel, -60V (dc)
- NT9X7101—shelf assembly
- NT9X71AB—LMS shelf
- NT9X7204—LIU shelf assembly
- NT9X72BA—LIU7/DCP shelf common fill
- F-bus

Core cooling unit

The core cooling unit (CU) provides mechanical ventilation for equipment in the link interface module cabinet. The CU is for dc voltages of -48V

(A0377580) or -60V (A0382102). This condition depends on power requirements.

SuperNode frame supervisory panel

The NT9X03AA, -48V (dc) or NT9X03BA, -60V (dc) SuperNode frame supervisory panel (FSP) provides alarm, maintenance and supervisory functions. The FSP is in the top shelf position of the NT9X70BB. Open cabinet doors to access or view the front and rear faces of the NT9X03BA. A frame alarm light is in the cabinet. The light is visible with the cabinet doors closed.

Power from the power distribution center frame comes into the FSP. The FSP distributes the power to power supply modules in the cabinet, like the NT9X30AA, NT9X30AB and NT9X31AB power converters. The power supply modules contain power control. Power supply is independent of the FSP.

Local message switch shelf

The NT9X71AB LMS shelf contains two LMSs, LMS0 and LMS 1. The two LMSs together form an LIM. The LIM is a PM that controls messaging between link interface units in an LIM cabinet. The LIM controls messaging between the LIM cabinet and the DMS-bus.

An LIM consists of the two LMSs and two F-buses, F-bus 0 and F-bus 1. The two NT9X71AB LMSs are mounted on an NT9X7101 shelf assembly.

Link interface shelf

The NT9X7204 shelf assembly can have a maximum of 12 interface units (LIU, EIU, or FRIU) mounted. The interface unit is a PM that processes messages that enter and leave an LIM cabinet through a signaling data link.

A link interface shelf can have a maximum of 12 sets of cards provisioned. A total of 36 LIU7s, EIUs, FRIUs or some group is present in an NT9X70BB LIM.

Link interface unit/data communication port shelf common fill

The NT9X72BA contains the following:

- STP filler (NT9X19EA)
- +5 V power converter (NT9X30AA)
- F-bus repeater and termination card (NT9X74CA)
- intra F-bus B-termination paddle board (NTEX20BA)
- paddle board filler faceplate (NT9X19BA)

NT9X70BB (continued)

Frame transport bus

An F-bus is an 8-bit bus. The F-bus provides data communication between a local message switch and the LIU7s provisioned in an LIM. Two load-sharing F-buses are present in an LIM to make sure of reliability. Each F-bus is dedicated to one of the two LMSs. The F-bus 0 is dedicated to LMS 0. The F-bus 1 is dedicated to LMS 1.

The F-bus has two types of functional resources, taps and medium.

Taps are bus access points. For an F-bus, a tap can be part of the F-bus adapter card (NT9X73BA) that an LMS uses. A tap can be part of the processor bus (P-bus) to F-bus interface card, NT9X75, that LIU7 uses.

> ***Note:*** The NT9X73 rate adapter card is an F-bus tap. The human-machine interface for the DMS-STP includes the rate adapter card as part of the medium because the card controls the F-bus. At the PM level of the maintenance and administration position (MAP) terminal, the F-bus is the bus.

Medium is the F-bus structure. Medium consists of a number of cards, PBs, and cables that interconnect and link all the F-bus parts. The F-bus parts are distributed in the LIM. The cards and PBs are provisioned as part of the LMS shelf and all three link interface shelves.

At the LMS shelf, the F-bus rate adapter card, NT9X73BA, performs rate translation. The NT9X73BA converts messages between the transaction bus (T-bus) of the LMS and the F-bus. The F-bus extender PB, NT9X79BA, is the interface to the F-bus ribbon cables that provide F-bus communication between the shelves of the LIM. The cables are the intershelf F-bus.

At each of the three link interface shelves, the F-bus extender PB is the connection point for intershelf F-bus cabling. The two versions of the F-bus extender PB are the NT9X79AA and BA.

The NT9X79AA F-bus extender PB extends the intershelf F-bus ribbon cables between shelves in the LIM.

The NT9X79BA F-bus extender PB extends the intershelf ribbon cables between shelves in the LIM. The NT9X70BA provides resistive termination for the F-bus in the top and bottom shelves of the LIM. When the NT9X79BA card is in the LMS shelf, the card accepts DS-0A composite clock signals for the associated LMS.

The LMS repeater card (NT9X74CA) reclocks and repeats all F-bus signaling between the intershelf F-bus cables and the intrashelf F-bus. The intrashelf

F-bus consists of the F-bus cards and the back plane of the shelf. Each F-bus repeater card can drive one of the two intrashelf F-buses.

The intrashelf F-bus terminator PBs, NTEX20AA and NTEX20BA, provide intrashelf F-bus termination. The NTEX20AA provides intrashelf termination for F-bus 0 signals. The NTEX20BA provides intrashelf termination for F-bus 1 signals.

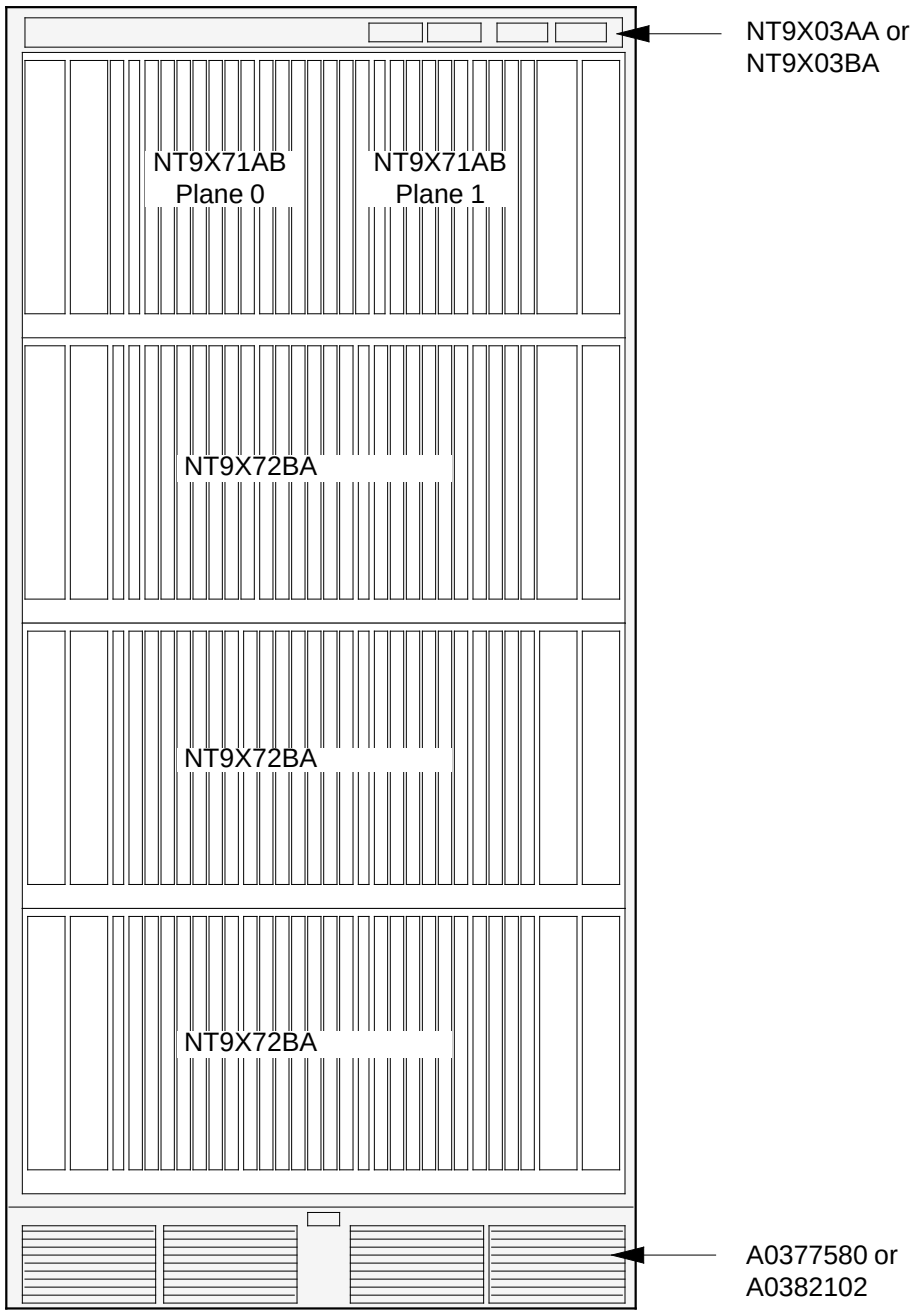
The back plane of the shelf provides intrashelf F-bus communication. The LIU7s access the two intrashelf F-buses through the P-bus to F-bus interface card (NT9X75). The NT9X75 acts as the F-bus tap.

Design

The design of the NT9X70BB appears in the following figure.

NT9X70BB (end)

NT9X70BB parts



Product description

The NT9X70CA enhanced link peripheral processor (ELPP) cabinet is a DMS SuperNode equipment cabinet for the DMS signaling transfer point (DMS-STP). The NT9X70CA cabinet contains the following peripheral modules (PM):

- link interface module (LIM)
- Common Channel Signaling 7 (CCS7) dual-link interface units (DLIU)

The LIM controls messaging between link interface units in the ELPP and between the ELPP and the DMS-bus. A LIM consists of two local message switches (LMS) with a triple frame transport bus (F-bus) on each LMS.

A DLIU is a set of high-speed link (HSL) termination hardware. Each set consists of:

- a high-speed link interface unit (HLIU)
- a high-speed link router (HSLR)

The DLIU sets are mounted on three link interface shelves (LIS). Each LIS contains up to four sets of DLIU cards.

Note: An optional upgrade kit (NT9X70ZA) is available for the international market to upgrade existing NT9X70CA ELPP cabinets to the Fiberized Link Processor Peripheral (FLPP) cabinet.

Components

The NT9X70CA cabinet consists of the following major components (not including cables):

- NT9X03AA—SuperNode frame supervisory panel (FSP), -48 V (dc) or NT9X03BA—SuperNode FSP -60 V (dc)
- NT9X7101—LMS shelf assembly
- NT9X71AC—LMS shelf circuit pack fill
- three NT9X7204—LIS assembly
- three NT9X72BA—LIS circuit pack fill
- NT9X95CU—C42 cooling unit, -48 V (dc) or NT9X95GU—C42 cooling unit, -60 V (dc)

SuperNode frame supervisory panel

The NT9X03AA or NT9X03BA FSP provides alarm, maintenance, and miscellaneous supervisory functions. The FSP is located in the top shelf

NT9X70CA (continued)

position of the NT9X70CA cabinet. The cabinet's doors must be opened to access or view the front and rear faces of the NT9X03BA. A frame alarm light is located in the cabinet so that the inside of the cabinet is visible when the cabinet doors are closed.

Power from the power distribution center frame enters the FSP and is distributed to various power supply modules within the cabinet, such as the NT9X30AB and NT9X31AB power converters. All power control is contained within the power supply modules and is independent of the FSP.

Local message switch shelf

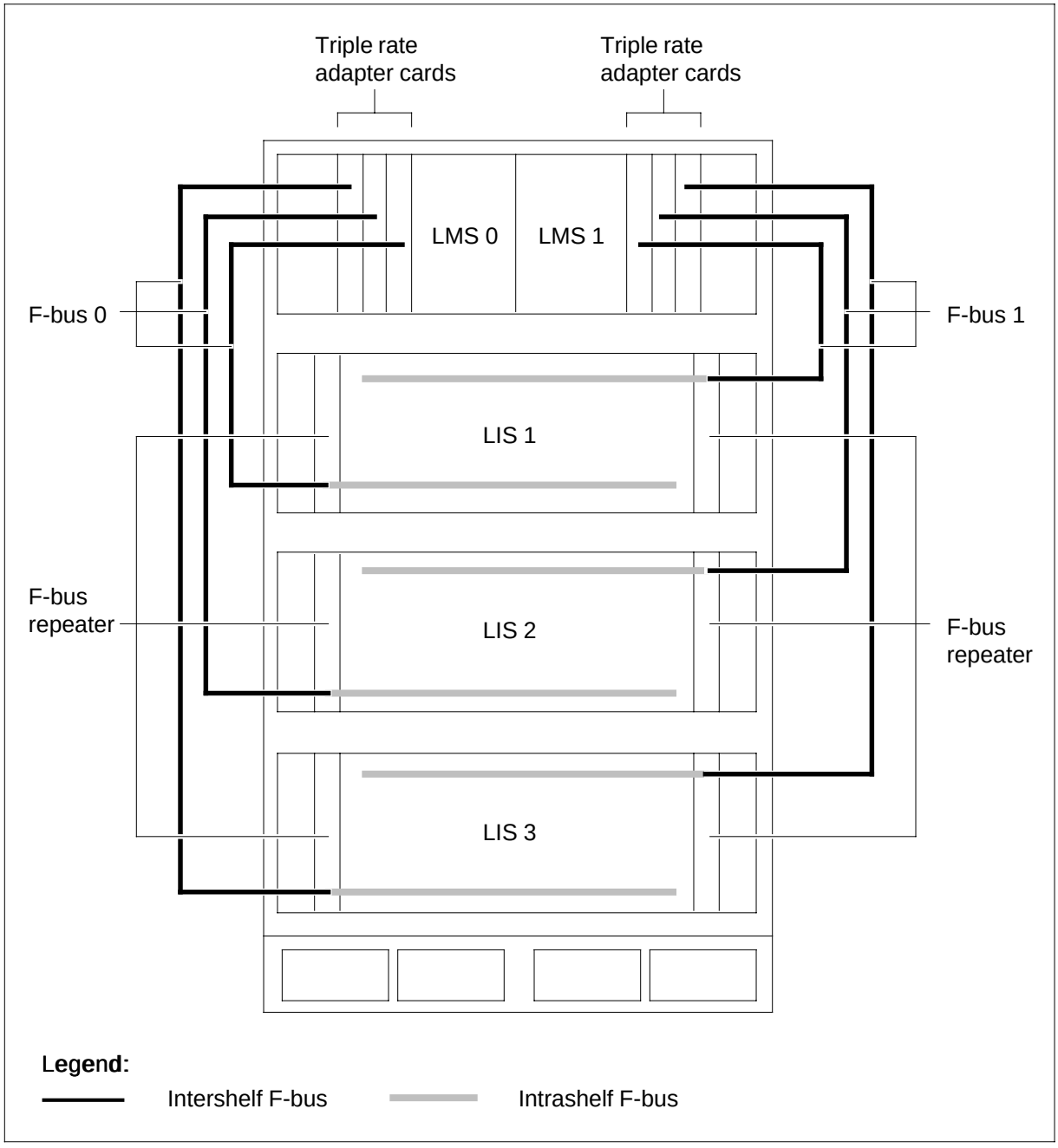
The NT9X71AB LMS shelf houses two LMSs: LMS 0 and LMS 1, which, together with the triple F-bus, form a LIM. The LIM in an ELPP cabinet exchanges messages with DLIUs. The LIM also controls messaging between the ELPP cabinet and the DMS-bus. The LIM is connected to each plane of the DMS-bus through SR-128 fiber links.

Each LMS supports a separate F-bus connection to each LIS. This type of configuration increases the internal messaging capacity and reliability of the ELPP.

Link interface shelf

The NT9X7204 LIS assembly contains the NT9X72BA LIS circuit pack fill. Separate F-buses connect each LMS with all three LISs independently. This type of configuration increases internal messaging capacity. The following figure illustrates the triple F-bus configuration in an ELPP cabinet.

NT9X70CA Triple F-bus configuration in an ELPP cabinet



Each LIS can house up to 4 DLIUs, which means a total of 12 DLIUs in an ELPP cabinet. The DLIU terminates and processes messages that enter and leave the ELPP through DS-1 (1.544 Mbit/s) signaling data links.

NT9X70CA (continued)

A DLIU hardware unit consists of the following blocks:

- a high-speed link interface unit (HLIU) that contains the following cards:
- NTEX22CA (32-Mbyte processor and F-bus controller)
- NTEX76AA (High-speed signaling terminal)
- NTEX78AA (DS-1 interface paddle board)
- a high-speed link router (HSLR) that contains the NTEX22CA card

The LIS also contains the following cards:

- NT9X19EA (STP power filler card)
- NT9X19BA (Filler paddle board CP)
- NT9X30AB (+5V power converter)
- NT9X74DA (F-bus repeater)
- NT9X79BA (F-bus termination paddle board)
- NTEX20AA (Intrashelf F-bus 0 termination paddle board)
- NTEX20BA (Intrashelf F-bus 1 termination paddle board)

Cooling unit

The cooling unit (CU) provides mechanical ventilation for equipment that is housed in the ELPP cabinet. Depending on power requirements, the CU is provisioned for dc voltages of either -48 V (NT9X95CU) or -60 V (NT9X95GU).

Frame transport bus

An F-bus is an 8-bit bus that provides data communication between an LMS and the DLIUs that are provisioned in the ELPP cabinet. To ensure reliability, two load-sharing F-buses are provided in an ELPP cabinet. Each F-bus on each LIS is dedicated to one of the two LMSs: F-bus 0 to LMS 0 and F-bus 1 to LMS 1. In the ELPP cabinet, three F-buses provide three separate connections between an LMS and each of the three LISs. With this triple configuration, each LIS is maintained as a separate entity, which means that when a connection between an LMS and one LIS is lost, the message load from only that one LIS is shifted to the F-bus on the mate LMS unit. The remaining F-buses for the other two LISs do not alter their messaging configuration.

At the LMS shelf, the NT9X73BB card converts messages between the transaction bus (T-bus) of the LMS and the F-bus. The NT9X79BB card (F-bus extension/termination paddle board) serves as the physical interface to the F-bus cables that provide an F-bus communication between the LMS shelf and the LIS. These cables are referred to as the intershelf F-bus.

At each of the three LISs, the NT9X79BA (F-bus termination paddle board) serves as the connection point for the intershelf F-bus cabling.

The NT9X74DA (F-bus repeater) card re-clocks and repeats all F-bus signaling between the intershelf F-bus cables and the intrashelf F-bus.

The NTEX20AA (intrashelf F-bus 0 termination paddle board) provides intrashelf termination for the F-bus 0 signals. The NTEX20BA (intrashelf F-bus 1 termination paddle board) provides intrashelf termination for the F-bus 1 signals.

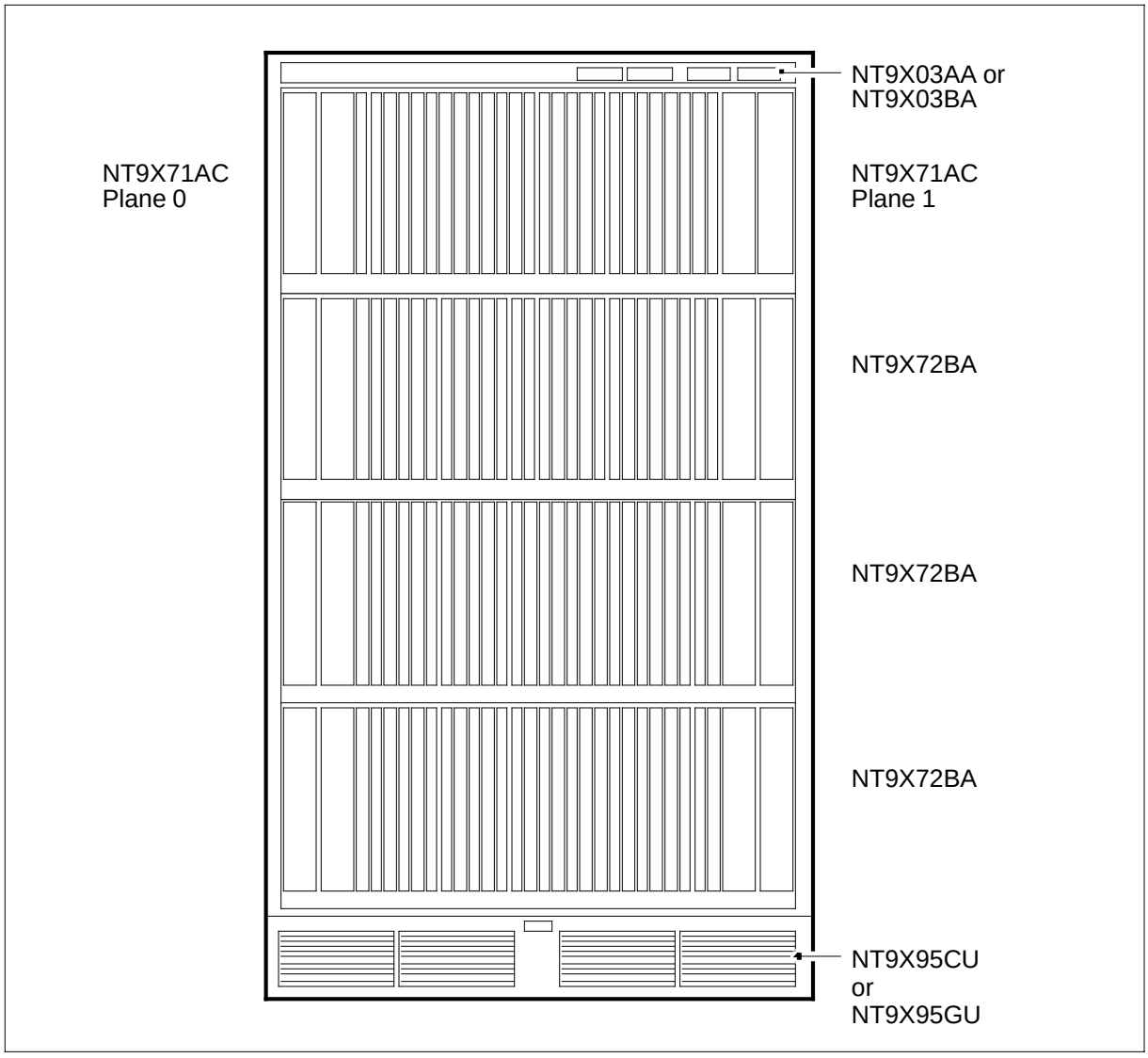
The intrashelf F-buses are located on the back plane of the shelf. DLIUs access the two intrashelf F-buses through the NTEX22CA card.

Layout

The following figure shows the layout of cabinet.

NT9X70CA (end)

NT9X70CA components



NT9X71AA

Product description

A NT9X71AA local message switch shelf houses two local message message switches (LMS), LMS0 (plane 0) and LMS 1 (plane 1). The two LMSs form a link interface module (LIM). The LMSs form the LIM together to make sure the DMS-STP is reliable during an LMS failure. During an LMS failure each LMS plane can carry the full message load of an LIM.

A LMS is a high-capacity communication hub. The LMS controls messaging between the Common Channel Signaling 7 (CCS7) link interface units (LIU7) in a link peripheral processor (LPP). The LMS controls messaging between the LPP and the DMS-bus.

A LIM consists of the two LMSs and two frame transport buses, F-bus 0 and F-bus 1.

To communicate with the LIU7s in the LPP, the LMS uses an 8 bit F-bus. Each LMS has a F-bus for reliability. If one LMS goes out of service, the performance of the LIM is not affected.

The LMS accepts the external composite clock signals that provide network timing for the DS-0A signaling data links. The DS-0A signaling links connect to the LIU7s. For reliability, one clock signal is present for each LMS and LIU7 has two sources for the composite clock signal.

For reliability each LMS connects through two DS30 links to each plane of the DMS-bus. The LMSs connect to each other through two DS30 links.

Parts

The NT9X71AA has the following parts:

- NT9X13DB—LMS processor card
- NT9X14BB—6 Mbyte memory card
- NT9X15AA—Mapper card
- NT9X17AA—four-port card
- NT9X19AA—Filler face plate
- NT9X19BA—Paddle board (PB) filler face plate
- NT9X19EA—Filler face panel
- NT9X23BA—DS30 four-port PB
- NT9X26AA—Remote terminal interface PB
- NT9X30AA—Power converter, +5V

NT9X71AA (continued)

- NT9X49CA—Processor bus (P-bus) terminator card
- NT9X52AA—Transaction bus (T-bus) access card
- NT9X53AA—System clock card
- NT9X73AA—F-bus rate adapter card
- NT9X79BA—F-bus extender PB

Design

Descriptions of NT9X71AA shelf parts appear in the following table.

NT9X71AA parts (Sheet 1 of 3)

PEC	Slot	Description
NT9X13DB	17F, 22F	*Local message switch processor (MSP) card* The NT9X13DB is a high performance microcomputer CPU card based on the Motorola MC68020 20 MHz, 32-bit microprocessor.
NT9X14BB	16F, 23F	*6 Mbyte memory card* The NT9X14BB is 6 Mbyte card equipped with error checking and correction (ECC). The NT9X14BB can has three separate 2-Mbyte memory modules. The organization of each module is: a 2X40 array of 256X1 digital recording announcement machines (DRAM). The NT9X14BB modules further subdivide to banks of 1X40 DRAMs. The 40 bit memory width contains 32 bits of data, 7 check bits and 1 parity bit.
NT9X15AA	15F, 24F	*Mapper card* The NT9X15AA is a specialized memory card that takes a software address and translates it to a physical address for routing. The CPU provides the software address. The NT9X15AA provides route status information. The route status is open or closed.
NT9X17AA	9F, 10F, 29F, 30F	*Four-port card* The NT9X17AA provides a data path for messaging between the message switch (MS) and four external links.
NT9X19AA	11F-14F, 25F-28F	*Card filler face plates* The NT9X19AA fills card slots that are not used.

NT9X71AA parts (Sheet 2 of 3)

PEC	Slot	Description
NT9X19BA	7R, 11R-16R, 18R-21R, 23R-28R, 32R	*Paddle board filler face plates* The NT9X19BA fills in PB slots that are not used.
NT9X19EA	1F, 33F	*Filler facepanel* The NT9X19EA fills in the slots 1F and 33F that are not used.
NT9X23BA	9R, 10R, 29R, 30R	*DS30 four-port paddle board* The NT9X23BA provides the interface between a parallel 4.096-MHz backplane data bus and the twisted-pair transmission cables associated with four DS30 links. The NT9X23BA transmits and receives out-of-band (OOB) data and provides a reference frame pulse extracted from the link. The NT9X23BA is for use with the NT9X17AA MS 4-port card.
NT9X26AA	17R, 22R	*Remote terminal interface paddle board* The NT9X26AA creates a reset system. The reset system allows monitoring and control of the subsystems of the signaling transfer point (STP).
NT9X30AA	4F, 36F	*Power converter, +5V card* The NT9X30AA is a dc-to-dc power converter that uses the -48V (nominal) office battery input to provide a +5V supply to the LMS shelf.
NT9X49CA	7F, 32F	*P-Bus terminator card* The NT9X49CA provides termination for MS backplane tracks that the MSP card uses. The NT9X49CA provides an interface to the P-bus PB extender and a time-out on the MS T-bus.
NT9X52AA	19F, 20F	*T-Bus access card* The NT9X52AA provides the interface between the MSP and the T-bus in the MSP. The NT9X52AA provides the MSP with the ability to transmit and receive messages. The MSP uses the links that connects to the message switch to transmit and receive messages.

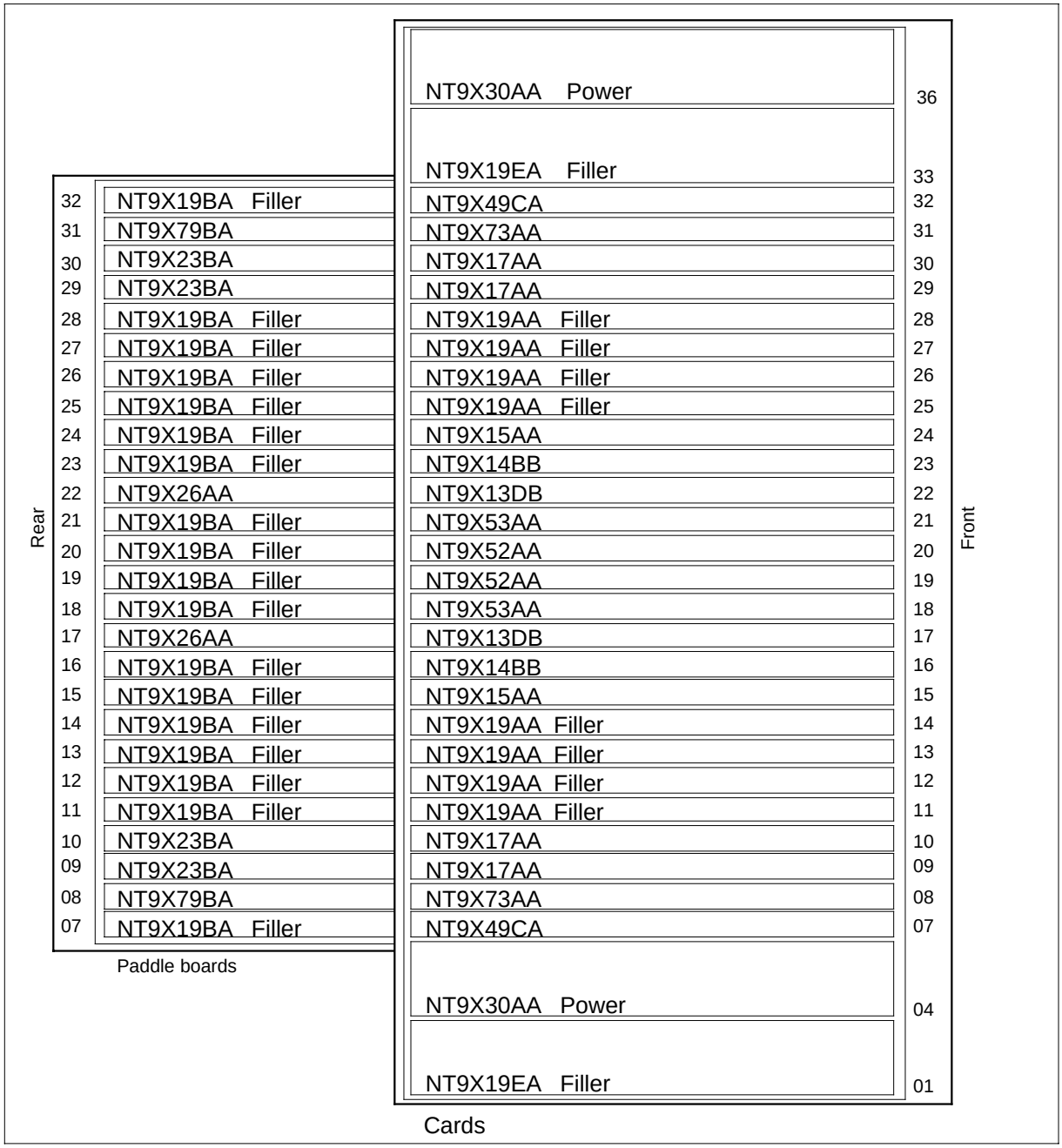
NT9X71AA (continued)

NT9X71AA parts (Sheet 3 of 3)

PEC	Slot	Description
NT9X53AA	18F, 21F	*System clock card* The NT9X53AA generates accurate timing signals from two digital phased locked loops (DPLL). The DPLLs use Stratum 3 oscillators. A remote clock allows one of the DPLLs can use a Stratum 2 or 2.5 oscillator. The DPLLs generate clock signals and 8-KHz frame pulse signals. The BT9X43AA can lock on to an accurate external clock source, like a Stratum 1 (caesium) oscillator.
NT9X73AA	8F, 31F	*F-Bus rate adapter card* The NT9X73AA transfers packets from the 32 bit LMS T-bus to the 8 bit F-bus. The NT9X73AA transfers packets from the 8 bit F-bus to the 32 bit LMT T-bus. The LIU7s sit on the F-bus. The F-bus is a duplicated F-bus for reliability.
NT9X79BA	8R, 31R	*F-Bus extender paddle board* The NT9X79BA F-bus extender paddle board extends the intershelf F-bus ribbon cables between shelves in the NT9X70 LPP. The NT9X79BA provides resistive termination for the F-bus in the top and bottom shelves of the LPP. When the LMS shelf has the NT9X79BA card, the NT9X79BA accepts the DS-0A composite clock signal for the associated LMS.

The design of the NT9X71AA appears in the following figure.

The NT9X71AA parts



NT9X71AB

Product description

A NT9X71AB local message switch shelf houses two local message switches (LMS), LMS0 (plane 0) and LMS 1 (plane 1). The LMSs form a link interface module (LIM). The LMSs form the LIM for DMS-Signaling transfer point (STP) reliability in the event of an LMS failure. During an LMS failure, each LMS plane can carry the full message load of an LIM.

A LMS is a high-capacity communication hub. The LMS controls messaging between the Common Channel Signaling 7 (CCS7) link interface units (LIU7) in a link peripheral processor (LPP). The LMS controls messaging between the LPP and the DMS-bus.

A LIM consists of the two LMSs and two frame transport buses, F-bus 0 and F-bus 1.

To communicate with the LIU7s in the LPP, the LMS uses an 8 bit F-bus. Each LMS has an F-bus for reliability. If one LMS goes out of service, the performance of the LIM is not affected.

The LMS accepts external composite clock signals. The external composite clock signals provide network timing for the DS-0A signaling data links. The DS-0A signaling data links connect to the LIU7s. For reliability, one clock signal is present for each LMS and each LIU7 has two sources for the composite clock signal.

For reliability each LMS connects to each plane of the DMS-bus. The LMS connect to the DMS-bus through two DS30 links. Both LMSs connect to each other through two DS30 links.

Parts

The NT9X71AB has the following parts:

- NT9X13—LMS processor (CPU) card
- NT9X14BB—6 Mbyte memory card
- NT9X15AA—Mapper card
- NT9X17AA—Four-port card
- NT9X19AA—Filler face plate
- NT9X19BA—Paddle board (PB) filler face plate
- NT9X19EA—Filler face panel
- NT9X23BA—DS30 four-port PB

- NT9X26AA—Remote terminal interface PB
- NT9X30AA—Power converter, +5V
- NT9X49CA—Processor bus (P-bus) terminator card
- NT9X52AA—Transaction bus (T-bus) access card
- NT9X53AA—System clock card
- NT9X73—F-bus rate adapter card
- NT9X79BA—F-bus extender PB

Design

Descriptions of the NT9X71AB shelf parts appear in the following table.

NT9X71AB parts (Sheet 1 of 3)

PEC	Slot	Description
NT9X13	17F, 22F	*Local message switch processor (MSP) card* The NT9X13 is a high performance microcomputer CPU card based on a Motorola MC68000-series microprocessor. Job engineering information specifies the correct provisioning for the specified MSP.
NT9X14BB	16F, 23F	*6 Mbyte memory card* The NT9X14BB is a 6 Mbyte card equipped with error checking and correction (ECC). Functional division of the NT9X14BB can occur into three separate 2 Mbyte memory modules. The organization of each module is in a 2X40 array of 256X1 digital recording announcement machines (DRAM). The NT9X14BB modules subdivide into banks of 1X40 DRAMs. The 40 bit memory width contains 32 bits of data, 7 check bits and 1 parity bit.
NT9X15AA	15F, 24F	*Mapper card* The NT9X15AA is a specialized memory card that takes a software addresses and translates it to a physical address for routing. The CPU provides the software address. The NT9X15AA provides route status information. The route status is open or closed.

NT9X71AB (continued)

NT9X71AB parts (Sheet 2 of 3)

PEC	Slot	Description
NT9X17AA	9F, 10F, 29F, 30F	*Four-port card* The NT9X17AA provides a data path for messaging between the message switch (MS) and four external links.
NT9X19AA	11F-14F, 25F-28F	*Card filler face plates* The NT9X19AA fills in card slots that are not in use.
NT9X19BA	7R, 11R-16R, 18R-21R, 23R-28R, 32R	*Paddle board filler face plates* The NT9X19BA fills in PB slots that are not in use.
NT9X19EA	1F, 33F	*Filler face panel* The NT9X19EA fills in the slots 1F and 33F that are not in use.
NT9X23BA	9R, 10R, 29R, 30R	*DS30 four-port paddle board* The NT9X23BA provides the interface between a parallel 4.096 MHz backplane data bus and the twisted-pair transmission cables. The cables associate with four DS30 links. The NT9X23BA transmits and receives out-of-band (OOB) data and provides a reference frame pulse extracted from the link. The NT9X23BA is for use with with the NT9X17AA MS 4-port card.
NT9X26AA	17R, 22R	*Remote terminal interface paddle board* The NT9X26AA creates a reset system. The reset system allows monitoring and control of the subsystems of the STP.
NT9X30AA	4F, 36F	*Power converter, +5V card* The NT9X30AA is a dc-to-dc power converter that uses the -48V (nominal) office battery input to provide a +5V supply to the LMS shelf.
NT9X49CA	7F, 32F	*P-bus terminator card* The NT9X49CA provides termination for MS backplane tracks that the MSP card uses. The NT9X49CA provides an interface to the P-bus extender PB and a time-out on the MS T-bus.

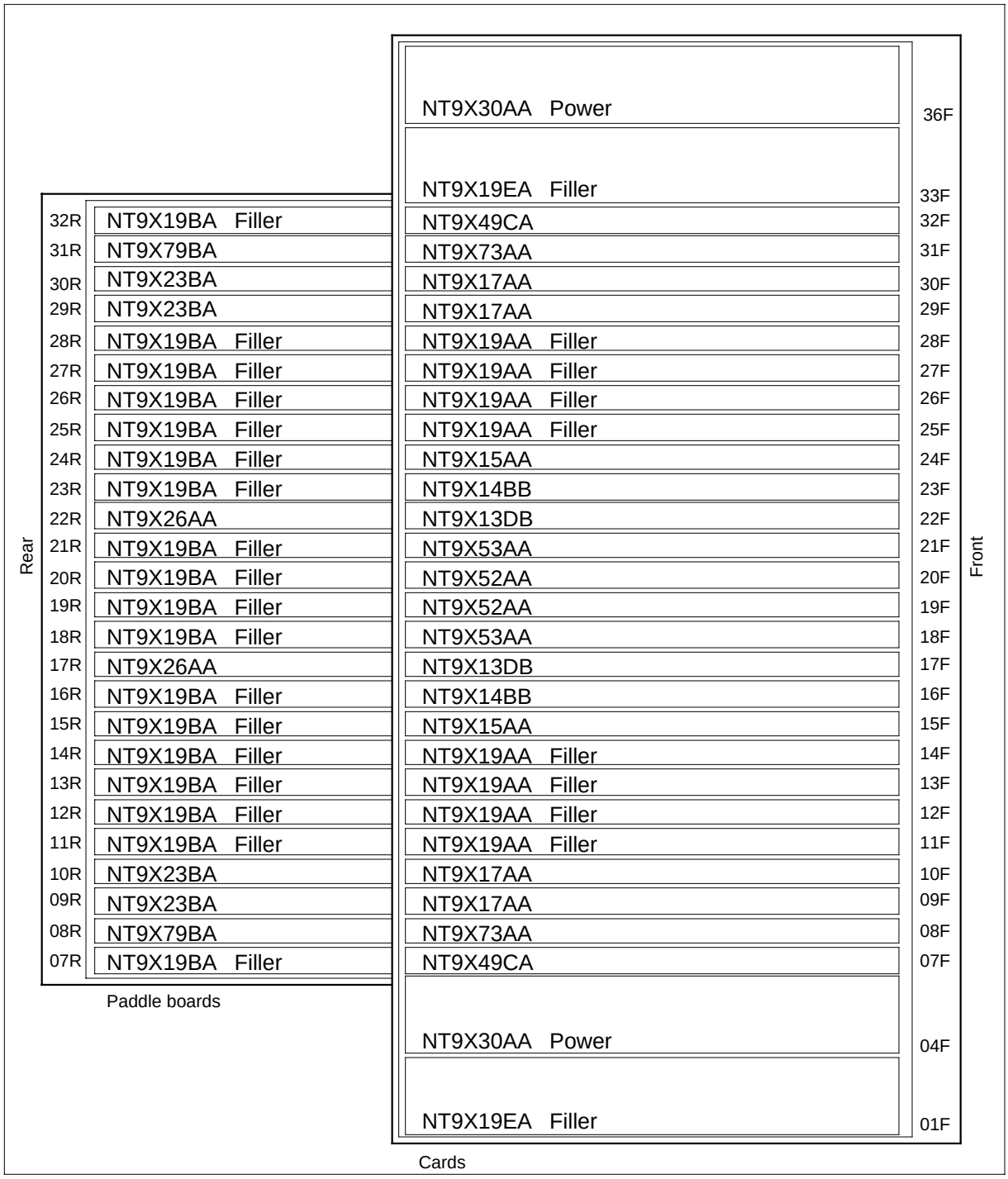
NT9X71AB parts (Sheet 3 of 3)

PEC	Slot	Description
NT9X52AA	19F, 20F	*T-bus access card* The NT9X52AA provides the interface between the MSP and the T-bus in the MSP. The NT9X52AA provides the MSP with the ability to transmit and receive messages. The MSP uses the links that connects to the message switch to transmit and receive messages.
NT9X53AA	18F, 21F	*System clock card* The NT9X53AA generates accurate timing signals from two digital phased locked loops (DPLL). The DPLLs use Stratum 3 oscillators. A remote clock allows one of the DPLLs to use a Stratum 2 or 2.5 oscillator. The DPLLs generate clock signals and 8-KHz frame pulse signals. The NT9X53AA can lock on to an accurate external clock source, like a Stratum 1 (caesium) oscillator.
NT9X73	8F, 31F	*F-bus rate adapter card* The NT9X73 transfers packets from the 32 bit LMS T-bus to the 8 bit F-bus. The NT9X73 transfers packets from the 8 bit F-bus to the 32 bit LMS T-bus. The LIU7s sit on the F-bus. A duplication of the F-bus occurs, for reliability. The job engineering information specifies the provisioning of the F-bus adapter card.
NT9X79BA	8R, 31R	*F-Bus extender paddle board* The NT9X79BA F-bus extender PB extends the intershelf F-bus ribbon cables between shelves in the NT9X70 LPP. The NT9X79BA provides resistive termination for the F-bus in the top and bottom shelves of the LPP. When the NT9X79BA is in the LMS shelf, the NT9X79BA accepts the DS-0A composite clock signal for the associated LMS.

The design of the NT9X71AB appears in the following figure.

NT9X71AB (end)

NT9X71AB parts



NT9X71AC

Product description

An NT9X71AC local message switch (LMS) shelf houses two local message switches: LMS 0 (plane 0) and LMS 1 (plane 1). Two LMSs together with triple frame transport buses (F-bus) form a link interface module (LIM). The two LMSs operate in a load-sharing mode with each other. In the event of an LMS failure this ensures DMS signaling transfer point (STP) reliability because either LMS plane can carry the full message load of a LIM.

The LMS in an enhanced link peripheral processor (ELPP) cabinet exchanges messages between the Common Channel Signaling 7 (CCS7) dual-link interface units (DLIU). A DLIU is a set of high-speed link (HSL) termination hardware that consists of the following blocks:

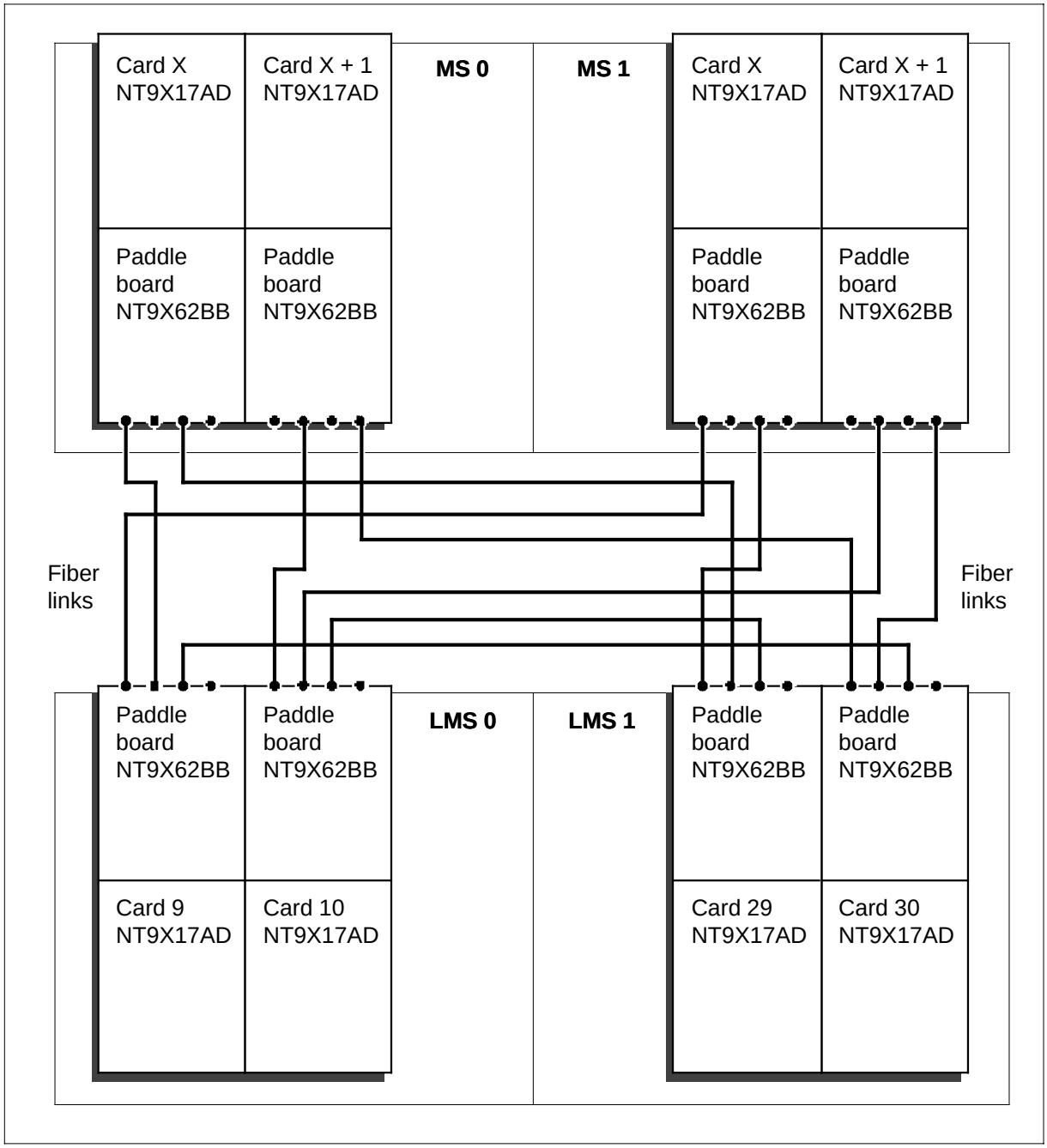
- a high-speed link interface unit (HLIU)
- a high-speed link router (HSLR)

The LMS also controls messaging between the ELPP cabinet and the DMS-bus.

For reliability, each LMS is connected through two DS512 (SR-128) fiber links to each plane of the DMS-bus, and both LMSs are connected to each other through two DS512 fiber links. The following figure shows the LIM fiberized DS512 configuration.

NT9X71AC (continued)

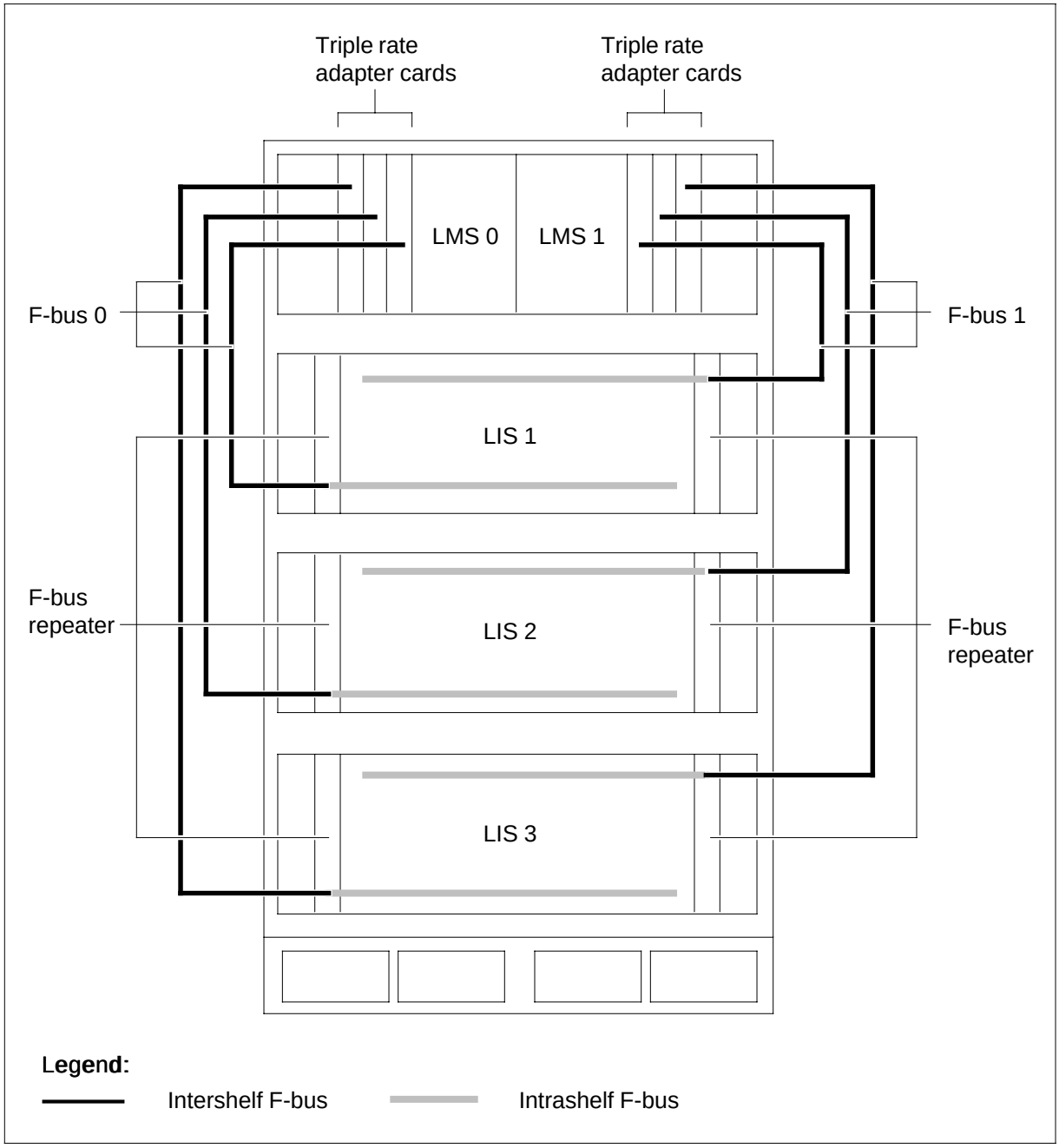
LIM fiberized DS512 configuration



To communicate with the DLIUs within the ELPP, each LMS uses a separate 8-bit F-bus: LMS 0 uses three F-bus 0s and LMS 1 uses three F-bus 1s. Each LMS provides three separate F-bus connections to each of the three LISs. With this triple configuration, each LIS is maintained as a separate entity, which

means that when a connection between an LMS and one LIS is lost, the message load from only that one LIS is shifted to the F-bus on the mate LMS unit. The remaining F-buses for the other two LISs do not alter their messaging configuration. The following figure illustrates the triple F-bus configuration in an ELPP cabinet.

Triple F-bus configuration in an ELPP cabinet



NT9X71AC (continued)

The LMS also accepts the external composite clock signals that provide network timing for the DS-1 signaling data links that are connected to the DLIUs. To ensure reliability, one clock signal is provided for each LIS, which means that each DLIU is provided with two sources for its composite clock signal.

Components

NT9X71AC consists of the following components:

- NT9X13DE (16-MHz DRAM simplex CPU card)
- NT9X15AA (Mapper card)
- NT9X17AD (MS four-port card)
- NT9X19BA (Filler paddle board CP)
- NT9X19AA (Filler card)
- NT9X26AB (Remote terminal interface paddle board)
- NT9X30AB (Global +5V 86-A power converter card)
- NT9X31AB (Global -5V 20-A power converter card)
- NT9X49CC (MS P-bus terminator card)
- NT9X52AA (MSP T-bus access card)
- NT9X53AA (MS system clock card)
- NT9X62BB (Four-link SR-128 subrate paddle board)
- NT9X73BB (Triple rate adapter card)
- NT9X79BB (F-bus extension/termination paddle board)

Layout

The following table lists the cards in NT9X71AC.

NT9X71AC cards (Sheet 1 of 2)

Card PEC	Slot	Description
NT9X13DE	17F, 22F	*16-MHz DRAM simplex CPU card* The NT9X13DE central processing unit (CPU) is a high-performance microcomputer board based on a Motorola MC68020 32-bit microprocessor.
NT9X15AA	15F, 24F	*Mapper card* The NT9X15AA mapper card is a specialized memory card that takes a logical address provided by the CPU and translates it to the physical address for routing. The NT9X15AA mapper card keeps route status information: route open or closed.
NT9X17AD	9F, 10F, 29F, 30F	*MS four-port card* The NT9X17AD card provides a data path for messages between the message switch (MS) and four external links.
NT9X19AA	8F, 14F, 16F, 23F, 25F, 31F	*Filler card* The NT9X19AA card fills in the unused card slots.
NT9X19BA	7R, 8R, 14R-16R, 18R-21R, 23-25R, 31R, 32R	*Filler paddle board CPs* The NT9X19BA paddle board fills in unused paddle board (PB) slots.
NT9X26AB	17R, 22R	*Remote terminal interface paddle board* The NT9X26AB paddle board creates a reset system that allows monitoring and control of the subsystems of the DMS-100 SuperNode switch and other related subsystems, such as an STP.
NT9X30AB	4F, 36F	*Global +5V 86-A power converter card* The NT9X30AB card is a dc-to-dc power converter that uses the -60V or -48V office battery input to provide a +5V supply to the LMS shelf.

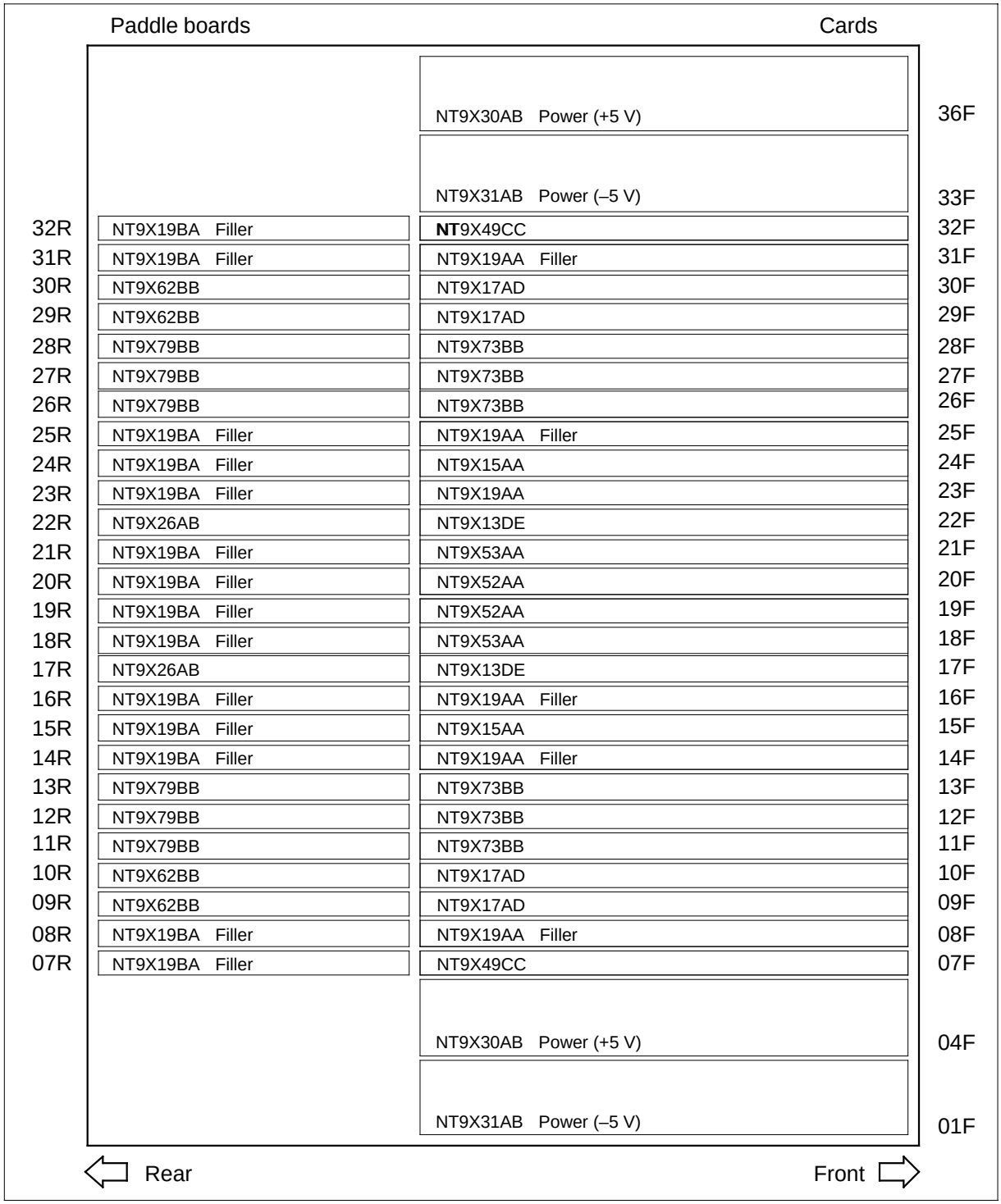
NT9X71AC (continued)

NT9X71AC cards (Sheet 2 of 2)

Card PEC	Slot	Description
NT9X31AB	1F, 33F	*Global -5V 20-A power converter card* The NT9X31AB card is a dc-to-dc power converter that uses the -60V or -48V office battery input to provide a -5V supply to the LMS shelf.
NT9X49CC	7F, 32F	*MS P-bus terminator card* The NT9X49CC card provides the processor bus (P-bus) termination for MS backplane tracks used by the message switch processor (MSP).
NT9X52AA	19F, 20F	*MSP T-bus access card* The NT9X52AA card provides the interface between the MSP and the T-bus. This interface provides the MSP with the capability to transmit and receive T-bus messages.
NT9X53AA	18F, 21F	*MS system clock card* The NT9X53AA card provides timing signals for the MS. The card generates timing signals from two digital phased locked loops (DPLL), which use Stratum 3 oscillators. For a remote clock, one of the DPLLs can use a Stratum 2 or 2.5 oscillator.
NT9X62BB	9R, 10R, 29R, 30R	*Four-link SR-128 subrate paddle board* The NT9X62BB paddle board provides an interface between the MS port card (NT9X17AD) and four fiber-optic links.
NT9X73BB	11F-13F, 26F-28F	*Triple rate adapter card* The NT9X73BB card converts messages between the 32-bit transaction bus (T-bus) of the LMS and the 8-bit F-bus.
NT9X79BB	11R-13R, 26R-28R	*F-bus extension/termination paddle board* The NT9X79BB paddle board terminates and distributes the intershelf F-bus signaling. It also terminates and distributes the DS-0 composite clock input to the ELPP frame.

The following figure shows the layout of NT9X71AC.

NT9X71AC components



NT9X72AA

Product description

A NT9X72AA link interface shelf (LIS) contains a maximum of eight Common Channel Signaling No. 7 (CCS7) link interface units (LIU7).

The LIU7 is a peripheral module. The LIU7 processes messages that enter and leave a link peripheral processor (LPP) through a signaling data link.

Each LIU7 consists of a set of cards and paddle boards (PB). The cards and PBs are provisioned in one of the following LISs of an LPP:

- NT9X75AA—Processor bus (P-bus) to Frame transport bus (F-bus) interface card
- NT9X13CA—Link general processor card (LGP)
- NT9X76AA—Signaling transfer point (STP) terminal card
- NT9X78—DS-0A interface PB

You can install less than eight LIU7s, four cards for each LIU7. The NT9X19AA filler face plates and NT9X19BA filler PB fill the empty card and PB slots.

Parts

The NT9X72AA consists of the following parts:

- NT9X13CA—Link general processor (CPU) card
- NT9X19AA—Filler face plate
- NT9X19BA—PB filler face plate
- NT9X19EA—Filler face panel
- NT9X30AA—Power converter, +5V
- NT9X74AA—F-bus repeater with termination card
- NT9X75AA—P-bus to F-bus interface card
- NT9X76AA—Signaling terminal card
- NT9X78—DS-0A terminator PB
- NT9X79—F-bus extender PB
- NTEX20AA—Intra F-bus 0 termination PB
- NTEX20BA—Intra F-bus 1 termination PB

Design

Descriptions of the NT9X72AA shelf parts appear in the following table.

NT9X72AA parts (Sheet 1 of 2)

PEC	Slot	Description
NT9X13CA	8F, 11F, 14F, 17F, 20F, 23F 26F, 29F	*Link general processor card* The NT9X13CA is a high performance microcomputer CPU card based on a Motorola MC68020, 20-MHz, 32-bit microprocessor.
NT9X19AA	Provisionable: 8F-31F	*Card filler face plates* The NT9X19AA fills in card slots that are not in use.
NT9X19BA *(always required)*	8R, 11R, 13R, 14R, 16R, 17R, 19R, 20R, 22R, 23R, 25R, 26R, 28R, 29R	*Paddle board filler face plates* The NT9X19BA fills in PB slots that are not in use.
NT9X19BA *(for unequipped LIU7 slots)*	9R, 12R, 15R,18R, 21R, 24R, 27R, 30R	*Paddle board filler face plates* The NT9X19BA fills in PB slots that are not in use.
NT9X19EA	1F, 33F	*Filler face panel* The NT9X19EA fills in the slots 1F and 33F that are not in use.
NT9X30AA	4F, 36F	*Power converter, +5V* The NT9X30AA is a dc-to-dc power converter that uses the -48V (nominal) office battery input to provide a +5V supply to the LIS shelf.
NT9X74AA	7F, 32F	*F-bus repeater with termination card* The NT9X74AA reclocks and repeats all F-bus communication between the intershelf F-bus and the intrashelf F-bus. The NT9X74AA contains circuits to drive one of the two buses. The NT9X74AA contains loopback circuits. Loopback circuits allow the following: • fault isolation • a microcontroller to read the pack Identifications (ID) • circuits to transfer information to the rate adapter card (NT9X73) over a serial link

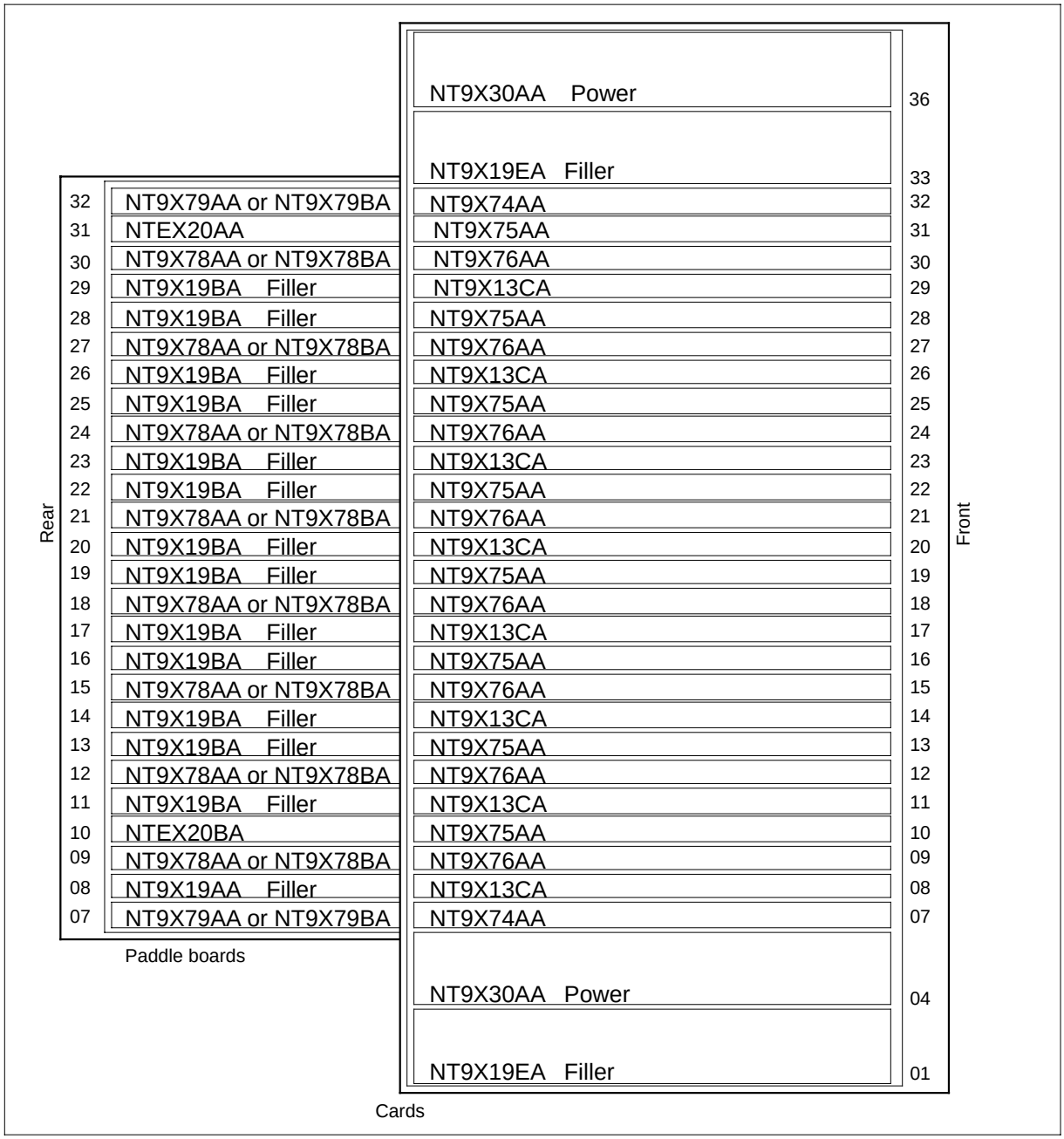
NT9X72AA (continued)

NT9X72AA parts (Sheet 2 of 2)

PEC	Slot	Description
NT9X75AA	10F, 13F, 16F, 19F, 22F, 25F, 28F, 31F	*P-bus to F-bus interface card* The NT9X75AA provides an interface between the link general processor card (NT9X13CA) and each F-bus. The F-bus interfaces of the NT9X75 AA are duplicated and full independent.
NT9X76AA	9F, 12F, 15F, 18F, 21F, 24F, 27F, 30F	*Signaling terminal card* The NT9X76AA provides error detection and correction and alignment and flow control functions. The NT9X76AA performs the level two functions of the message transfer part (MTP) protocol.
NT9X78AA or BA	9R, 12R, 15R, 18R, 21R, 24R, 27R, 30R	*DS-0A terminator paddle board* The NT9X78 provides layer 1 functions like level shifting drivers/receivers between the signaling terminal and a digital line.
NT9X79AA or BA	7R, 32R	*F-bus extender paddle board* The NT9X79 has two main functions. The NT9X79 terminates and distributes the differential intershelf F-bus. The NT9X79 provides the termination and distribution for the DS0 composite clock input to the LPP.
NT9X79BA	8R, 31R	*F-bus extender paddle board* The NT9X79BA F-bus extender PB extends the intershelf F-bus ribbon cables between shelves in the NT9X70 LPP. The NT9X79BA provides resistive termination for the F-bus in the top and bottom shelves of the LPP.
NTEX20AA	31R	*Intra F-bus 0 termination paddle board* The NTEX20AA terminates the F-bus A (FBUS A) and the channel support bus A (CBUS A).
NTEX20BA	10R	*Intra F-bus 1 termination paddle board* The NTEX20BA terminates the F-bus B (FBUS B) and the C-bus B (CBUS B).

The design of a completely equipped NT9X72AA appears in the following figure.

NT9X72AA parts



NT9X72AC

Product description

A NT9X72AC link interface shelf (LIS) contains a maximum of eight Common Channel Signaling No. 7 (CCS7) link interface units (LIU7).

The LIU7 is a peripheral module. The LIU7 processes messages that enter and leave a link peripheral processor (LPP) through a signaling data link.

Each LIU7 consists of a set of cards and paddle boards (PB). The cards and PBs are provisioned in one of LISs of an LPP. The four differences of LIU7s that the NT9X72AC shelf can have appear in the figure on page 7.

You can install less than 8 LIU7s, four cards for each LIU7. The NT9X19AA filler face plates and NT9X19BA filler PBs fill the empty card and PB slots.

Parts

The NT9X72AC consists of the following parts:

- NT9X13CA—Link general processor (CPU) card
- NT9X19AA—Filler face plate
- NT9X19BA—PB filler face plate
- NT9X19EA—Filler face panel
- NT9X30AA—Power converter, +5V
- NT9X74BA—Frame transport bus (F–bus) repeater with termination card
- NT9X75AA—Processor bus (P–bus) to F–bus interface card
- NT9X76AA—Signaling terminal card
- NT9X77AA—STP V.35 interface PB
- NT9X78AA or BA—DS–0A terminator PB
- NT9X79AA or BA—F–bus extender PB
- NT9X84AA—Ethernet interface circuit pack (CP)
- NT9X85AA—Ethernet AUI PB
- NTEX20AA—Intra F–bus 0 termination PB
- NTEX20BA—Intra F–bus 1 termination PB
- NTEX22AA—Signaling transfer point (STP) integrated processor and F–bus interface
- NTEX30AA—Frame relay T1 PB
- NTEX31AA—Frame relay access processor

Design

Descriptions of the NT9X72AC shelf parts appear in the following table.

NT9X72AC parts (Sheet 1 of 5)

PEC	Slot	Description
NT9X13CA	8F, 11F, 14F, 17F, 20F, 23F 26F, 29F	Link general processor card The NT9X13CA is a high performance microcomputer CPU card based on a Motorola MC68020, 20–MHz, 32–bit microprocessor.
NT9X19AA	Provisionable: 8F, 11F, 14F, 17F, 20F, 23F, 26F, 29F	Card filler face plates The NT9X19AA fills in card slots that are not in use.
NT9X19BA (always required)	8R, 11R, 13R, 14R, 16R, 17R, 19R, 20R, 22R, 23R, 25R, 26R, 28R, 29R	Paddle board filler face plates The NT9X19BA fills in PB slots that are not in use.
NT9X19BA (for unequipped LIU7 slots)	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	Paddle board filler face plates The NT9X19BA fills in PB slots that are not in use.
NT9X19EA	1F, 33F	Filler face panel The NT9X19EA fills in the slots 1F and 33F that are not in use.
NT9X30AA	4F, 36F	Power converter, +5V The NT9X30AA is a dc–to–dc power converter that uses the -48V (nominal) office battery input to provide a +5V supply to the LIS shelf.

NT9X72AC (continued)

NT9X72AC parts (Sheet 2 of 5)

PEC	Slot	Description
NT9X74BA	7F, 32F	F–bus repeater with termination card The NT9X74BA reclocks and repeats all F–bus communication between the intershelf F–bus and the intrashelf F–bus. The NT9X74BA contains circuits to drive one of the buses. The NT9X74BA contains loopback circuits. The loopback circuits allow the following: • fault isolation • a microcontroller to read the pack identifications (ID) • circuits to transfer information to the rate adapter card (NT9X73) over a serial link
NT9X75AA	10F, 13F, 16F, 19F, 22F, 25F, 28F, 31F	P–bus to F–bus interface card The NT9X75AA provides an interface between the link general processor card (NT9X13CA) and each F–bus. The F–bus interfaces of the NT9X75AA are duplicated and full independent.
NT9X76AA	9F, 12F, 15F, 18F, 21F, 24F, 27F, 30F	Signaling terminal card The NT9X76AA provides error detection and correction and alignment and flow control functions. The NT9X76AA performs the level two functions of the message transfer part (MTP) protocol.
NT9X77AA	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	STP V.35 interface paddle board The NT9X77AA provides the electrical interface between the LIU and the CCS7 link.
NT9X78AA or BA	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	DS–0A terminator paddle board The NT9X78 provides layer 1 functions like level shifting drivers/receivers between the signaling terminal and a digital line.
NT9X79AA or BA	7R, 32R	F–bus extender paddle board The NT9X79BA F–bus extender PB extends the intershelf F–bus ribbon cables between shelves in the NT9X70 LPP. The NT9X79BA provides resistive termination for the F–bus in the top and bottom shelves of the LPP.

NT9X72AC parts (Sheet 3 of 5)

PEC	Slot	Description
NT9X84AA	9F, 12F, 15F, 18F, 21F, 24F, 27F, 30F	Ethernet interface card The NT9X84AA provides temporary storage for incoming/outgoing (I/O) link messages. The NT9X84AA provides protocol management and handshaking for Ethernet CSMA/CD. The NT9X84AA generates voltage and impedance levels to drive standard twisted pair drop cable signal lines.
NT9X85AA	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	Ethernet AUI paddle board The NT9X85AA provides an interface between the motherboard, the Ethernet interface card (EIC) and the attachment unit interface (AUI) cable.
NTEX20AA	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	Intra F–bus 0 termination paddle board The NTEX20AA terminates the F–bus A (FBUS A) and the channel support bus A (CBUS A).
NTEX20BA	10R	Intra F–bus 1 termination paddle board The NTEX20BA terminates the F–bus B (FBUS B) and the C–bus B (CBUS B).
NTEX22AA	10F, 13F, 16F, 19F, 22F, 25F, 28F, 31F	STP integrated processor & F–bus interface card (IPF) The NTEX22AA provides a LIU7 link general processor. The NTEX22AA provides two F–bus interface abilities. The NTEX22AA is for use in the LIU7 of the STP switch. The NTEX22AA replaces the NT9X13CA link general processor and the NT9X75AA F–bus to F–bus interface.

NT9X72AC (continued)

NT9X72AC parts (Sheet 4 of 5)

PEC	Slot	Description
NTEX30AA	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	Frame relay T1 paddle board The NTEX30AA performs the following functions: • provides basic T1 framing and synchronization functions • provides the alarm monitoring and generation facilities • provides signaling bit insertion and extraction (A/B bits) • generates loss of signal (yellow alarm) and blue alarm signal • provides jitter control • clock recovery • analog loop backs for hardware diagnostics • T1 analog drivers and receivers for alternative mark inversion (AMI) transmission

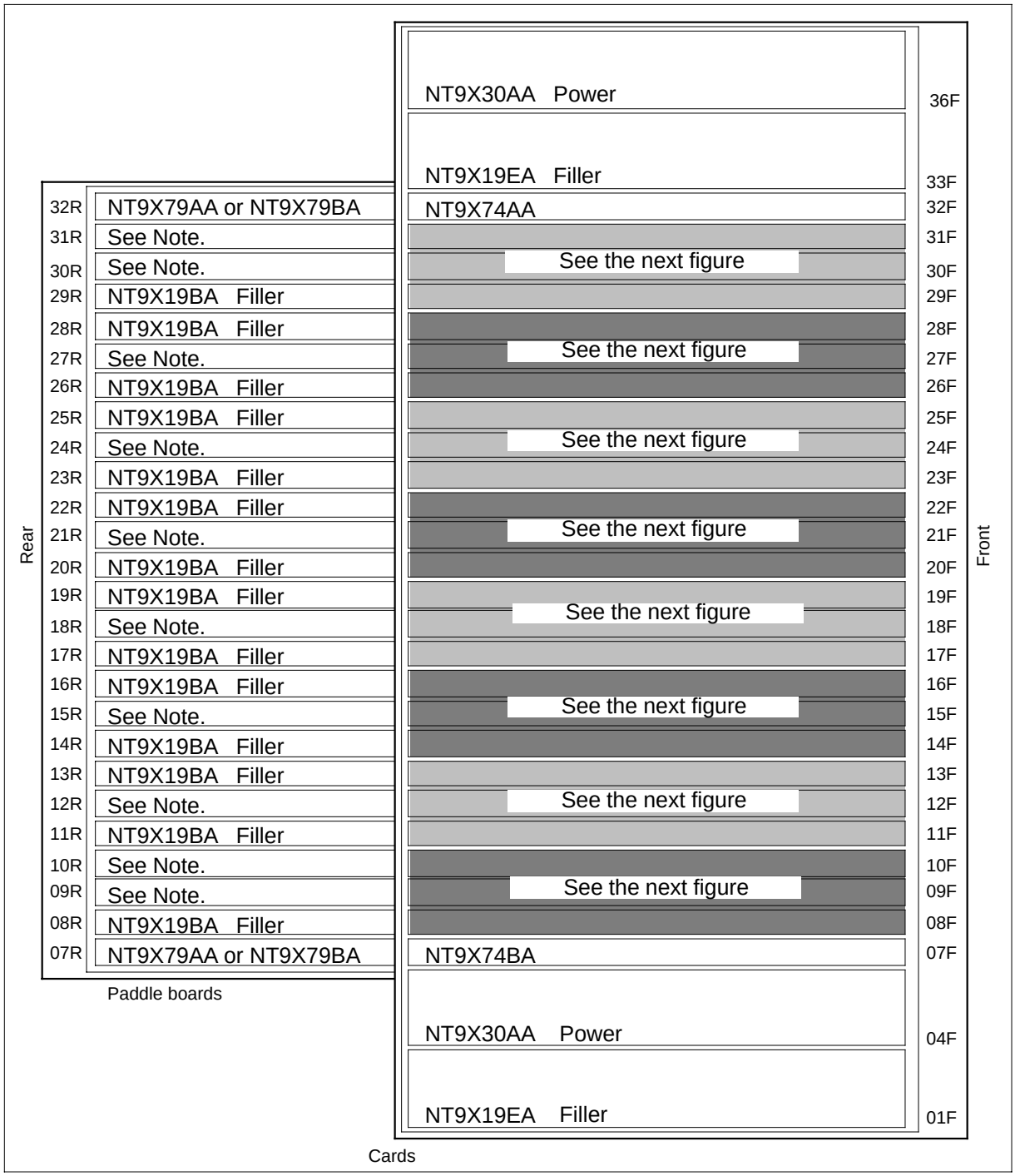
NT9X72AC parts (Sheet 5 of 5)

PEC	Slot	Description
NTEX31AA	9F, 12F, 15F, 18F, 21F, 24F, 27F, 30F	Frame relay access processor (FRAP) The NTEX31AA is the main processor for the frame relay interface unit (FRIU). The NTEX31AA provides the following: • an interface to the frame relay T1 access PB for the transmission and reception of pulse code modulated (PCM) data. The PCM data is in the shape of frames • an integrated system digital network and direct memory interface link layer controller. Provides concurrent access of a maximum of 32 channels in high level data level data link control (HDLC) or non–HDLC modes. Transfers the data in 8 bit parallel format to and from an external buffer shared with the host IPF • four register types, for the following functions: — a configuration register to configure the FRAP in the correct mode — control registers to control static and dynamic operational features and maintenance features — status registers to report the T1 alarms — error registers to capture T1 error conditions — A/B bit signaling registers for use during the transmit and receive cycle – shared random access memory (RAM) to control FRAP operations and report frame status – a clock to provide timing for the FRAP – provides loop back operations that verify the FRIU

The design of an equipped NT9X72AC appears in the following figure.

NT9X72AC (continued)

NT9X72AC parts



Note: Provisionable: NT9X19BA, NT9X78AA, NT9X78BA or NT9X77AA and NT9X79AA NTEX20AA and NTEX20BA or NT9X85AA or NTRX80AA

The different configurations for the LIU7s appear in the following figure.

NT9X72AC LIU7 configuration options

NT9X75AA	10F, 13F, 16F, 19F, 22F, 25F, 28F, 31F
NT9X76AA	09F, 12F, 15F, 18F, 21F, 24F, 27F, 30F
NT9X13CA	08F, 11F, 14F, 17F, 20F, 23F, 26F, 29F

The standard LIU7 configuration

NTEX22AA	10F, 13F, 16F, 19F, 22F, 25F, 28F, 31F
NT9X76AA	09F, 12F, 15F, 18F, 21F, 24F, 27F, 30F
NT9X19AA	08F, 11F, 14F, 17F, 20F, 23F, 26F, 29F

The 2-card LIU7 configuration

NTEX22AA	10F, 13F, 16F, 19F, 22F, 25F, 28F, 31F
NT9X84AA	09F, 12F, 15F, 18F, 21F, 24F, 27F, 30F
NT9X19AA	08F, 11F, 14F, 17F, 20F, 23F, 26F, 29F

The Ethernet LIU7 configuration

NTEX22AA	10F, 13F, 16F, 19F, 22F, 25F, 28F, 31F
NTEX31AA	09F, 12F, 15F, 18F, 21F, 24F, 27F, 30F
NT9X19AA	08F, 11F, 14F, 17F, 20F, 23F, 26F, 29F

The LIU7 with frame relay access processor configuration

NT9X72AD

Product description

A NT9X72AD link interface shelf (LIS) contains a maximum of eight Common Channel Signaling No. 7 (CCS7) link interface units (LIU7).

The LIU7 is a peripheral module. The LIU7 processes messages that enter and leave a link peripheral processor (LPP) through a signaling data link.

Each LIU7 consists of a set of cards and paddle boards (PB). The LIS of an LPP contains these cards and paddle boards. The four types of LIU7s that the NT9X72AD shelf can contain appear in the figure on page 7.

The shelf can contain less than eight LIU7s, 4 cards for each LIU7. The NT9X19AA filler face plates and NT9X19BA filler PBs fill the empty card and PB slots.

Parts

The NT9X72AD contains the following parts:

- NT9X13CA—Link general processor (CPU) card
- NT9X19AA—Filler face plate
- NT9X19BA—PB filler face plate
- NT9X19EA—Filler face panel
- NT9X30AA—Power converter, +5V
- NT9X74BA—Frame transport bus (F-bus) repeater with termination card
- NT9X75AA—Processor bus (P-bus) to F-bus interface card
- NT9X76AA—Signaling terminal card
- NT9X77AA—STP V.35 interface PB
- NT9X78AA or BA—DS-0A terminator PB
- NT9X79AA or BA—F-bus extender PB
- NT9X84AA—Ethernet interface circuit pack (CP)
- NT9X85AA—Ethernet AUI PB
- NTEX20AA—Intra F-Bus 0 termination PB
- NTEX20BA—Intra F-Bus 1 termination PB
- NTEX22AA—STP integrated processor and F-bus interface
- NTEX30AA—Frame relay T1 PB
- NTEX31AA—Frame relay access processor

Design

Descriptions of the parts of the NT9X72AC shelf appear in the following table.

NT9X72AD parts (Sheet 1 of 4)

PEC	Slot	Description
NT9X13CA	8F, 11F, 14F, 17F, 20F, 23F, 26F, 29F	Link general processor card High performance microcomputer CPU card based on a Motorola MC68020, 20-MHz, 32-bit microprocessor.
NT9X19AA	Provisionable: 8F, 11F, 14F, 17F, 20F, 23F, 26F, 29F	Card filler face plates. Fill in card slots that are not in use.
NT9X19BA *(always required)*	8R, 11R, 13R, 14R, 16R, 17R, 19R, 20R, 22R, 23R, 25R, 26R, 28R, 29R	Paddle board filler face plates. Fill in PB slots that are not in use.
NT9X19BA *(for unequipped LIU7 slots)*	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	Paddle board filler face plates. Fills in PB slots that are not in use.
NT9X19EA	1F, 33F	Filler face panel. Fill in slots 1F and 33F, that are not in use.
NT9X30AA	4F, 36F	Power converter, +5V. A dc-to-dc power converter that uses the -48V (nominal) office battery input to provide a +5V supply to the LIS shelf.
NT9X74BA	7F, 32F	F-bus repeater with termination card Reclocks and repeats F-bus communication between the intershelf F-bus and the intrashelf F-bus. Contains the circuits that drive one of the two independent buses. Contains loopback circuits to isolate faults. Contains a microcontroller to read the pack identifications (ID). Contains circuits to transfer this information to the rate adapter card (NT9X73) over a serial link.

NT9X72AD (continued)

NT9X72AD parts (Sheet 2 of 4)

PEC	Slot	Description
NT9X75AA	10F, 13F, 16F, 19F, 22F, 25F, 28F, 31F	P-bus to F-bus interface card Provides an interface between the link general processor card (NT9X13CA) and each of the two F-buses. Both F-bus interfaces of the NT9X75AA are duplicated and fully independent.
NT9X76AA	9F, 12F, 15F, 18F, 21F, 24F, 27F, 30F	Signaling terminal card Provides error detection and correction and alignment and flow control functions. Performs level 2 functions of the message transfer part (MTP) protocol.
NT9X77AA	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	STP V.35 interface paddle board Provides the electrical interface between the LIU and the CCS7 link.
NT9X78AA or BA	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	DS-0A terminator paddle board Provides layer 1 functions like level shifting drivers/receivers between the signaling terminal and a digital line.
NT9X79AA or BA	7R, 32R	F-bus extender paddle board The NT9X79 F-bus extender PB extends the intershelf F-bus ribbon cables between shelves in the NT9X70 LPP. The NT9X79 provides resistive termination for the F-bus in the top and bottom shelves of the LPP.
NT9X84AA	9F, 12F, 15F, 18F, 21F, 24F, 27F, 30F	Ethernet interface card Provides temporary storage for incoming/outgoing (I/O) link messages. Provides protocol management and handshaking for Ethernet CSMA/CD. Generates correct voltage and impedance levels to drive standard twisted pair drop cable signal lines.
NT9X85AA	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	Ethernet AUI paddle board Provides an interface between the motherboard, the Ethernet interface card (EIC) and the attachment unit interface (AUI) cable.

NT9X72AD parts (Sheet 3 of 4)

PEC	Slot	Description
NTEX20AA	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	Intra F-bus 0 termination paddle board Terminates the F-bus A (FBUS A) and the channel support bus A (CBUS A).
NTEX20BA	10R	Intra F-bus 1 termination paddle board Terminates the F-bus B (FBUS B) and the C-bus B (CBUS B).
NTEX22AA	10F, 13F, 16F, 19F, 22F, 25F, 28F, 31F	STP integrated processor & F-bus interface card (IPF) Provides a LIU7 link general processor. Provides dual F-bus interface ability. The LIU7 of the STP switch uses this part. Replaces the NT9X13CA link general processor and the NT9X75AA F-bus to P-bus interface.
NTEX30AA	9R, 10R, 12R, 15R, 18R, 21R, 24R, 27R, 30R, 31R	Frame relay T1 paddle board Provides basic T1 framing and synchronization functions. Provides alarm monitor and generation facilities. Provides signaling bit insertion and extraction (A/B bits). Generates loss of signal (yellow alarm) and blue alarm signals. Provides jitter control. Allows clock recovery. Provides analog loop backs for hardware diagnostics. Provides T1 analog drivers and receivers for alternative mark inversion (AMI) transmission.

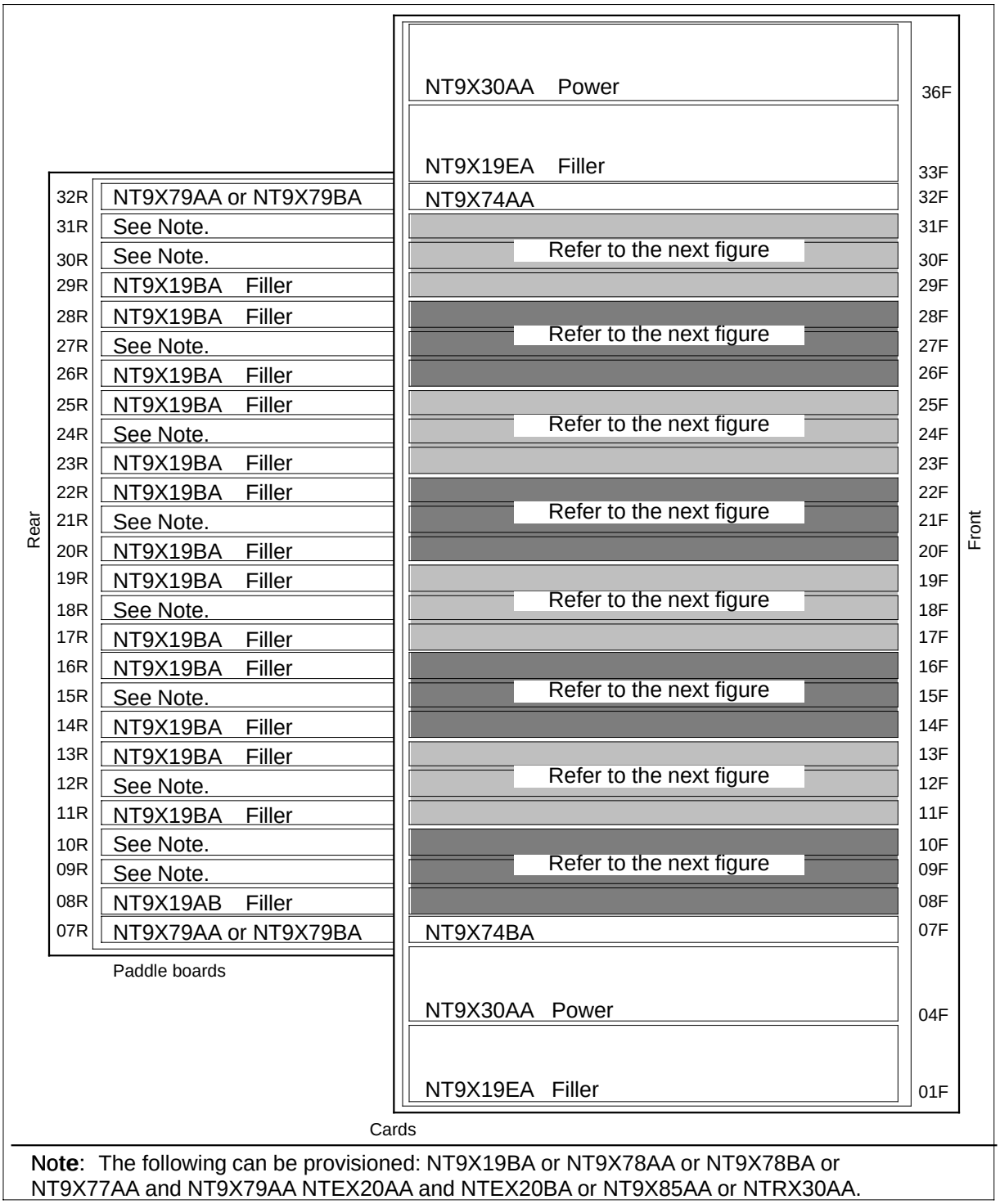
NT9X72AD (continued)

NT9X72AD parts (Sheet 4 of 4)

PEC	Slot	Description
NTEX31AA	9F, 12F, 15F, 18F, 21F, 24F, 27F, 30F	Frame relay access processor (FRAP) The NTEX31AA is the main processor for the frame relay interface unit (FRIU). The NTEX31AA provides: • an interface to the frame relay T1 access PB to transmit and receive pulse code modulated (PCM) data in the shape of frames. • an integrated system digital network and direct memory interface link layer controller. This network and controller provides concurrent access of a maximum of 32 channels. The network and controller provides access to channels in high-level data link control (HDLC) or non-HDLC modes. The network and controller transfer the data in 8-bit parallel format to and from an external buffer. The network and controller share this buffer with the host IPF. The NTEX31AA provides four register types that perform the following functions: • a configuration register to configure the FRAP in the correct mode • control registers to control static and dynamic operational features and maintenance features • status registers to report the T1 alarms • error registers to capture T1 error conditions • A/B bit signaling registers for use during the transmit and receive cycle • shared RAM to control FRAP operations and report frame status • a clock to provide timing for the FRAP • loop back operations to verify the FRIU

The design of an equipped NT9X72AC appears in the figure that follows.

NT9X72AD design

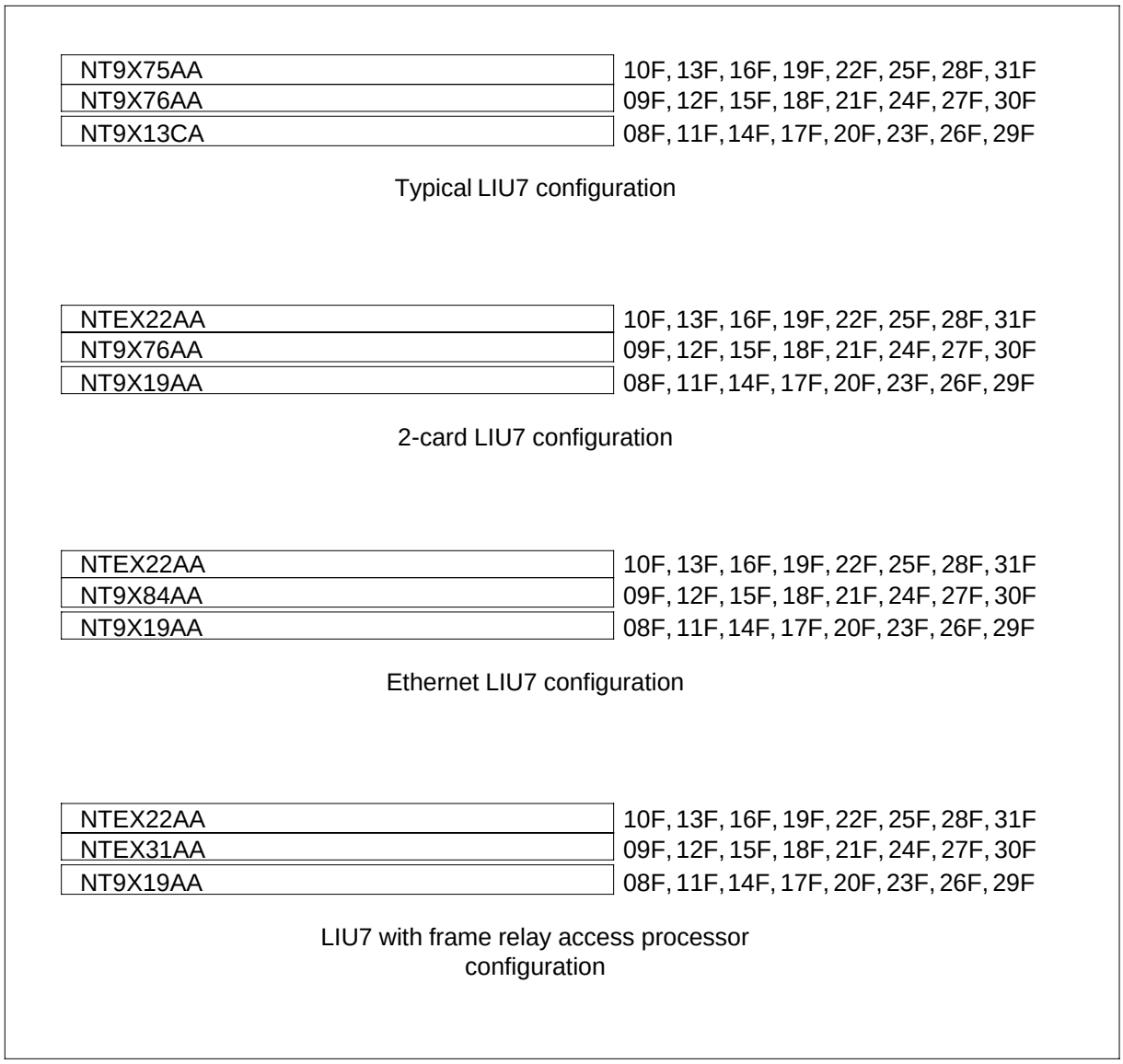


Note: The following can be provisioned: NT9X19BA or NT9X78AA or NT9X78BA or NT9X77AA and NT9X79AA NTEX20AA and NTEX20BA or NT9X85AA or NTRX30AA.

NT9X72AD (end)

The different configurations for the LIU7s appear in the following figure.

NT9X72AD LIU7 configuration options



NT9X73AA

Product description

The NT9X73AA is a local message switch (LMS) to frame transport bus (F-bus) rate adapter (RA). A link interface module (LIM) uses the NT9X73AA to transfer packets. The NT9X73AA transfers packets from the 32 bit LMS transaction bus (T-Bus) to the 8-bit F-bus. The NT9X73AA transfers packets from the 8-bit F-bus to the 32-bit LMS T-bus. Link interface units (LIU7) are on the F-bus. F-bus is duplication is present for reliability.

Location

The LMS shelf of the link peripheral processor (LPP) frame contains the NT9X73AA.

Functional description

The RA performs four functions:

- receives messages from the T-bus.
- transmits messages on the T-bus.
- receives messages from the F-bus.
- transmits messages from the F-bus.

Functional blocks

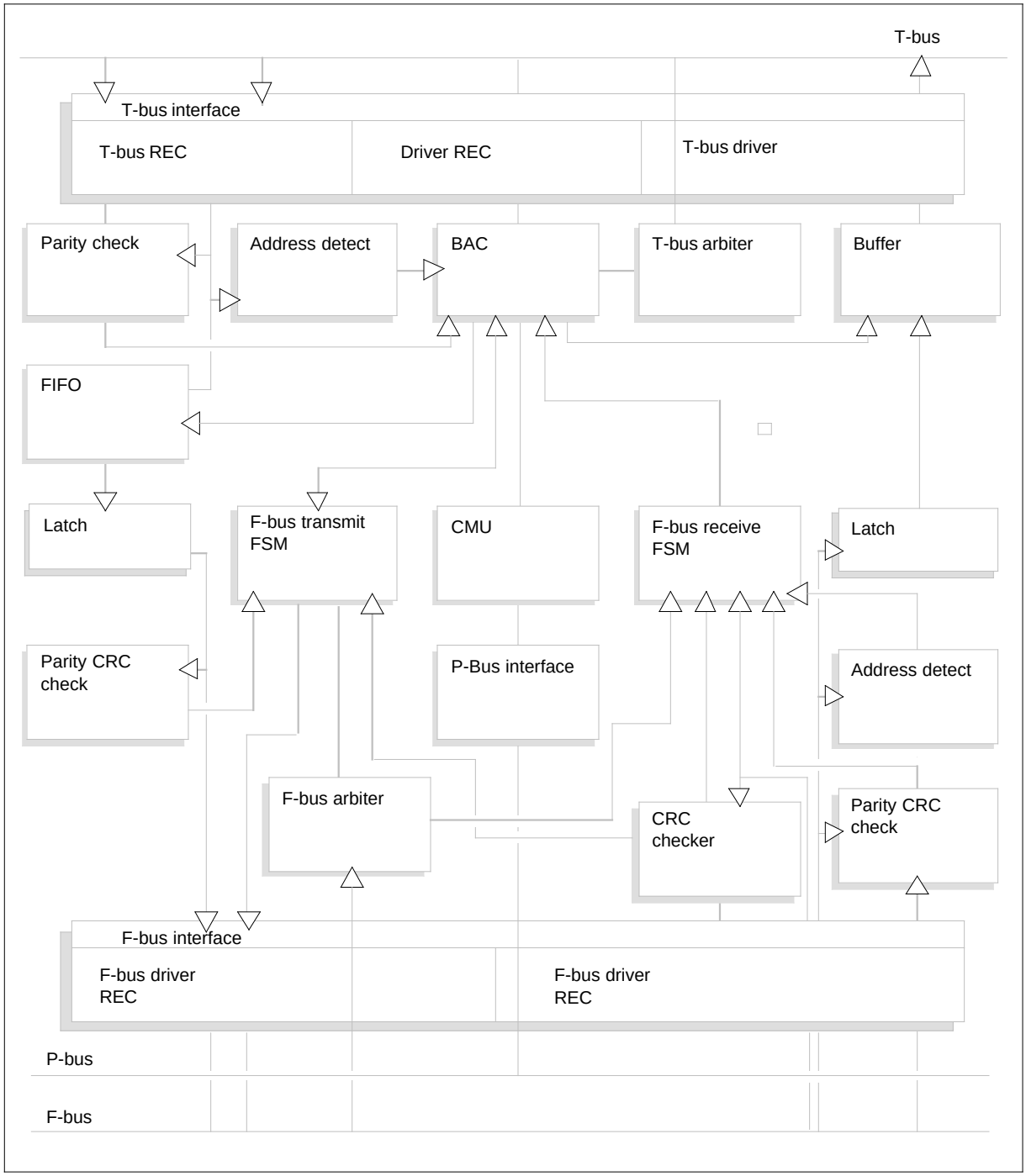
The NT9X73AA has the following functional blocks:

- bus access circuit (BAC)
- T-bus interface (T-bus rec/driver rec/T-bus driver)
- F-bus interface (F-bus driver/rec)
- buffer RAM
- first in, first out (FIFO) RAM
- F-bus transmit finite state machine (FSM)
- F-bus arbiter
- parity/cyclic redundancy check (CRC)
- F-bus receive FSM
- T-bus arbiter
- processor-bus (P-bus) interface
- card maintenance unit (CMU)

The functional relationship between blocks appears in the following figure.

NT9X73AA (continued)

NT9X73AA functional blocks



Bus access circuit

The BAC stores and retrieves messages when the T-bus or F-bus interfaces request an operation. The BAC keeps pointers to the buffer RAM to store messages from the F-bus. The BAC keeps pointers to the buffer RAM to transmit messages on the T-bus. The BAC keeps pointers to the FIFO RAM to store messages from the T-bus. The BAC keeps pointers to the FIFO RAM to transmit messages on the F-bus.

Transaction bus interface

The T-bus interface receives and transmits messages.

Frame transport bus interface

The F-bus interface receives and transmits messages.

Buffer RAM

The buffer RAM stores messages.

First in, first out RAM

The FIFO RAM stores messages.

Frame transport bus transmit finite state machine

The F-bus transmit finite state machine (FSM) controls message transmission on the F-bus. The F-bus transmit FSM communicates with the BAC to retrieve data bytes from the FIFO. The F-bus transmit FSM performs the protocol on the F-bus. When a message is present in the FIFO, the state machine requests a bus from the F-bus arbiter.

Frame transport bus arbiter

The F-bus arbiter performs a round-robin arbitration between the F-bus transmit FSM and the LIU7s. The LIU7s and the RA have the same priority.

Parity/cyclic redundancy check checker

This functional block checks parity and CRC on data from the FIFO. The system sends parity on the F-bus. The F-bus requires parity to protect the address cycles on the bus. The CRC does not protect address cycles.

Frame transport bus receive finite state machine

The F-bus receive FSM receives notification when the F-bus arbiter grants an LIU7 a bus and receives the next bus message.

Transaction bus arbiter

The T-bus arbiter uses a distributed arbitration design.

NT9X73AA (continued)

Processor-bus interface

The P-bus interface allows the CPU and the 8031 to communicate. The RA is an 8-bit slave on the P-bus. The P-bus interface contains registers that allow the CPU to control the RA. Controls include reset of the 8031 and deactivation of parity generation, and read of the identification (ID) PROM.

Card maintenance unit

The CMU communicates with the repeater to read the ID PROM of the following:

- NT9X74AA (F-bus repeater card)
- NT9X79BA (F-bus termination paddle board)
- NT9X79AA (F-bus extension paddle board)
- NT9X30AA (+5V 86A power converter card)

This communication occurs through the serial communication controller (SCC) of the 8031. The system places the serial interface in mode 2 and the link speed is set at 375 Kbps. This speed is 0.03125 of the processor clock (12 MHz).

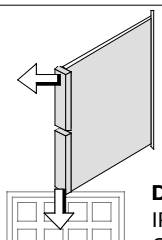
The CMU provides loopback modes. The RA receives messages at the RA physical address on the T-bus. These messages are sent on the F-bus. The F-bus receive FSM receives the messages. The messages transmit back on the T-bus. Loopback can be internal or external to the RA. External mode is the normal mode of operation. The loopback can use internal mode when the RA is out of service.

Signaling

Pin numbers

The pin numbers for NT9X73AA appear in the following figures.

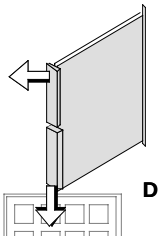
NT9X73AA pin numbers (Part 1 of 2)



	D	C	B	A
1	IP0	AD37	AD00	Gnd
2	OP0	ADP3	AD01	Gnd
3	IP1	ADREN–	AD02	Gnd
4	OP1	DATEN–	AD03	Gnd
5	IP2	EOS–	AD04	Gnd
6	OP2	NVB0	AD05	Gnd
7	IP3	NVB1	AD06	Gnd
8	OP3	POK–	AD07	Gnd
9	SEG0	BNF-	ADP0	Gnd
10	SEG1	SRCEN–	AD10	Gnd
11	SEG2	DSTEN–	AD11	Gnd
12	SEG3	REQ–	AD12	Gnd
13	SEG4	GRT-	AD13	FCLK+
14		INH–	AD14	FCLK–
15	PLN0–		AD15	FAD0+
16			AD16	FAD0–
17		BUSGRI–	AD17	FAD1+
18		BUSGRO–	ADP1	FAD1–
19			AD20	FAD2+
20			AD21	FAD2–
21		PERINT4–	AD22	FAD3+
22			AD23	FAD3–
23	RSTOUT-	AD24	FAD4+	
24		AD25	FAD4–	
25	BEN1–	BEN0–	AD26	FAD5+
26	BEN3–	BEN2–	AD27	FAD5–
27	GND		ADP2	FAD6+
28	WRT-	GND	AD30	FAD6–
29	EDTACK–		AD31	HW4
30	PARITY+		AD32	
31	PRTYEN–		AD33	
32		Gnd	AD34	SH0
33	DAS32–		AD35	SH1
34			AD36	FP61–
35				C61
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06		Gnd
41		ADDR07		Gnd
42		ADDR08		Gnd
43		ADDR09		Gnd
44		ADDR10		+5V
45		ADDR11		+5V

NT9X73AA (continued)

NT9X73AA pin numbers (Part 2 of 2)

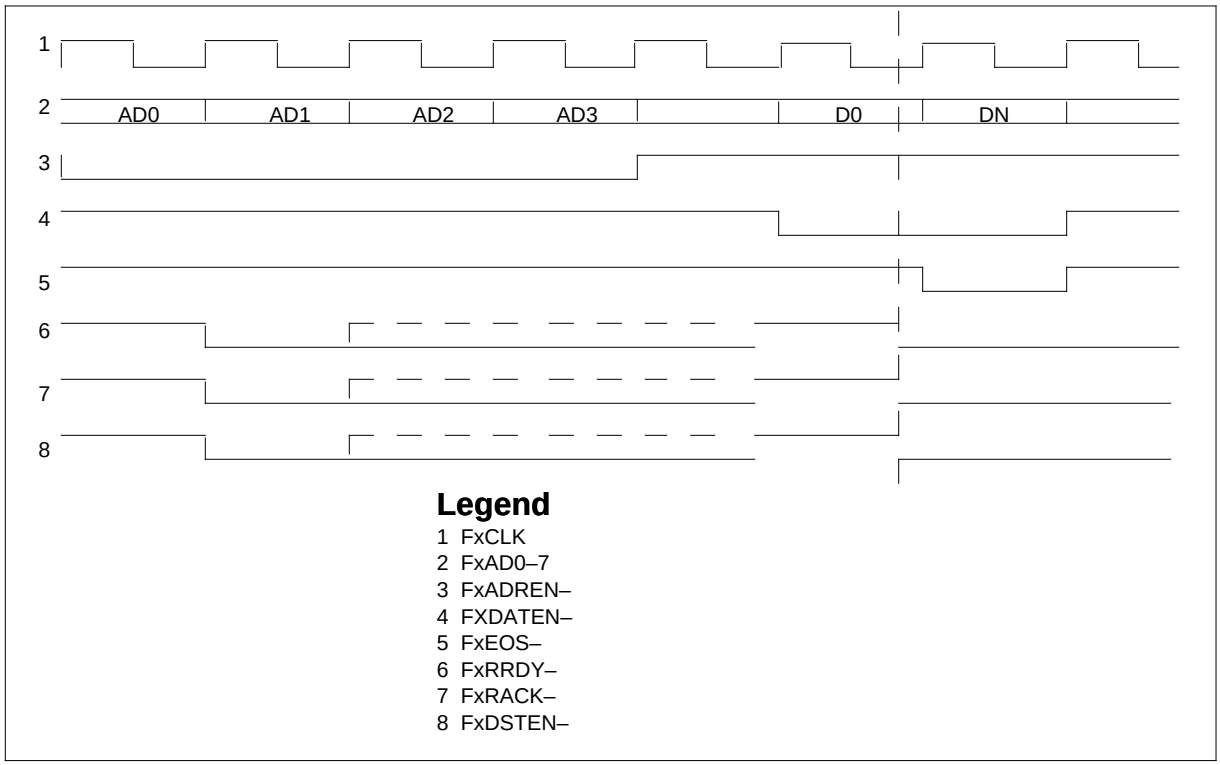


	D	C	B	A
46		ADDR12		+5V
47		ADDR13		+5V
48		ADDR14		+5V
49		ADDR15		+5V
50		ADDR16		+5V
51		ADDR17		+5V
52		ADDR18		+5V
53		ADDR19		+5V
54		ADDR20		+5V
55		ADDR21		+5V
56		ADDR22		
57		ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70				
71	IDTX+			
72	IDTX–			
73	IDRX+			
74	IDRX–			
75	D0	FPOLL+		
76	D2	FPOLL–		
77	D4	FREQ+		
78	D6	FREQ–		
79		FPACK+	FAD7+	Gnd
80	A2	FPACK–	FAD7–	Gnd
81	A0	FRRDY+	FPAR+	Gnd
82		FRRDY–	FPAR–	Gnd
83		FRACK+	FADREN+	Gnd
84	D7	FRACK–	FADREN–	Gnd
85	A1	FWAIT+	FDAEN+	Gnd
86	A3	FWAIT-	FDAEN–	Gnd
87		FCLR+	FEOS+	Gnd
88	D5	FCLR–	FEOS–	Gnd
89	D3		FRST+	Gnd
90	D1	CS79	FRST-	Gnd

Timing

The RA to LIU7 F-bus protocol timing for the NT9X73AA appears in the following figure.

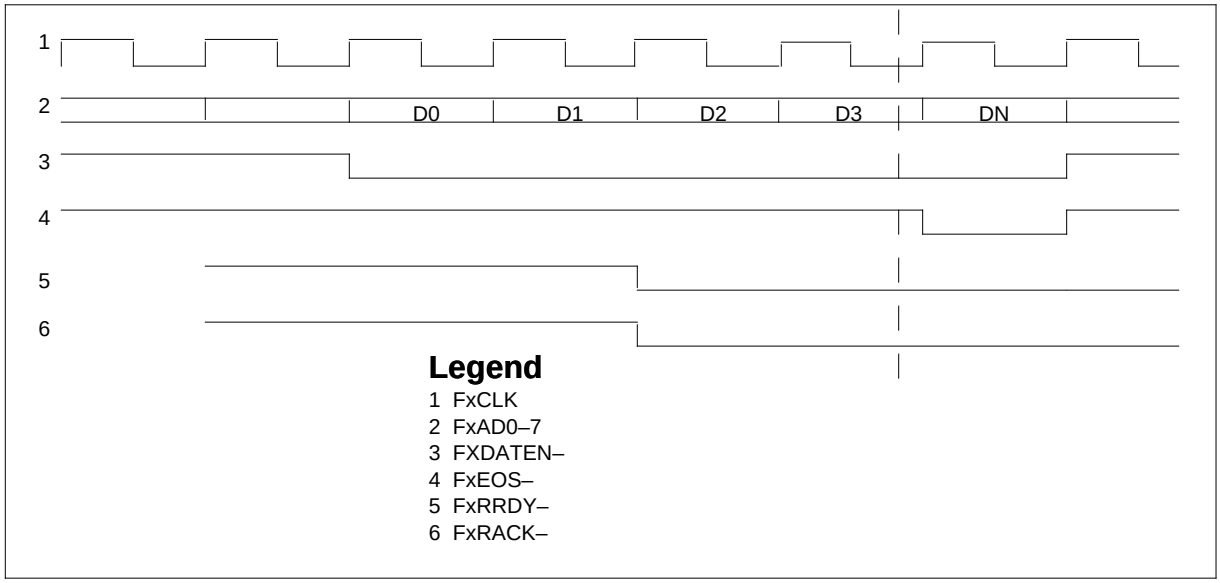
NT9X73AA RA to LIU7 F-bus protocol timing



The LIU7 to RA F-bus protocol timing for the NT9X73AA appears in the following figure.

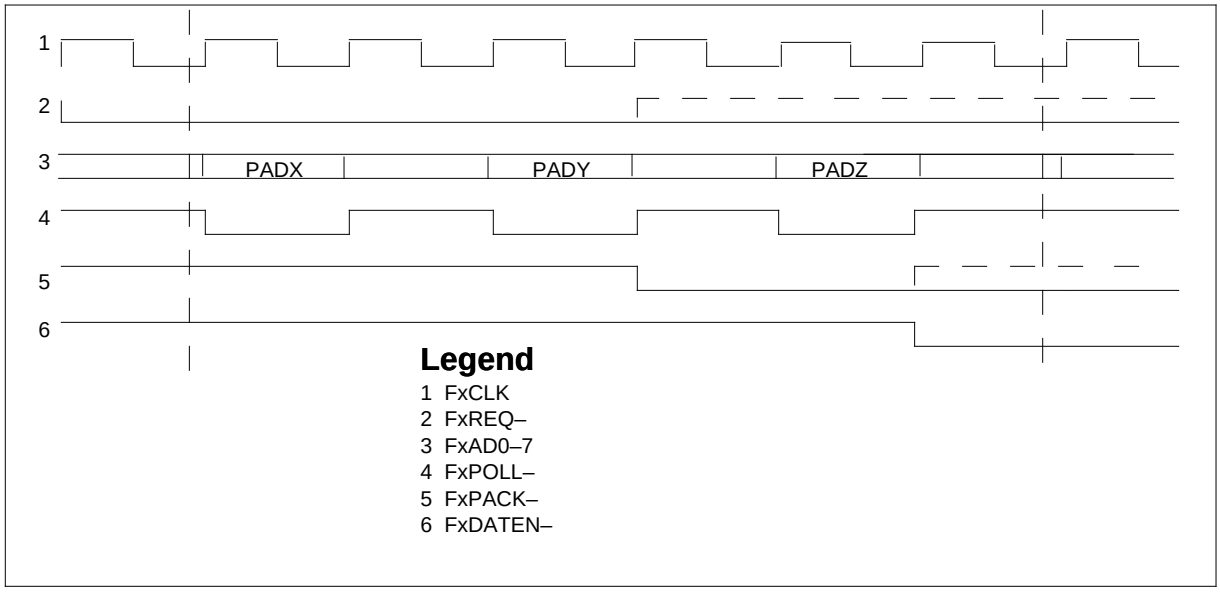
NT9X73AA (end)

NT9X73AA LIU7 to RA F-bus protocol timing



The F-bus arbitration timing for the NT9X73AA appears in the figure that follows.

NT9X73AA F-bus arbitration timing



NT9X73BA

Product description

The NT9X73BA is rate adapter (RA). A link interface module (LIM) uses the NT9X73BA to perform rate translation for the transfer of data packets. The transfer of data packets occurs between the local message switch (LMS) transaction bus (T-bus) and the frame transport bus (F-bus). The transfer of data packets occurs in both directions. Rate translation is necessary between the 32-Mbps T-bus and the 4-Mbps F-bus.

Each LIM in the message switch has two rate adaptors. The 73BA version of the rate adaptor supports both 2-slot and 3-slot configured LIU7 shelves.

Functional description

The NT9X73BA rate adaptor provides an interface between the LMS and the LIU7s. The NT9X73BA rate adaptor moves messages from the 32-bit T-bus of the LMS to the 8-bit F-bus to the LIU7s. The NT9X73BA rate adaptor also sends messages in the reverse direction.

The LMS and LIU7s require the rate adapter because of the pin limit on the other shelves. This limit prohibits the use of two T-buses. The use of an 8-bit bus simplifies the F-bus interface with the LIU7s.

Functional blocks

The relationship between the functional blocks appears in the following diagram.

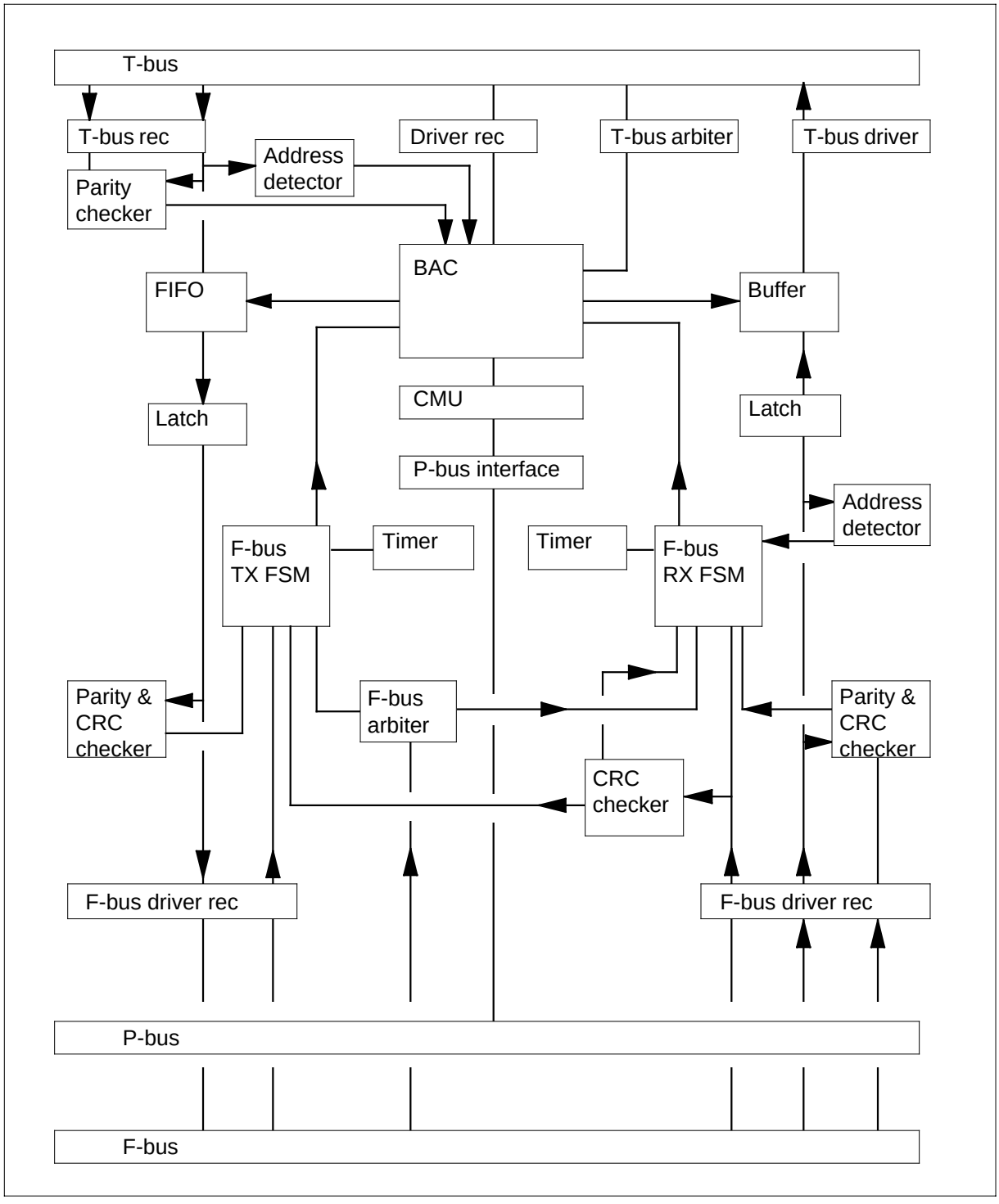
Signaling

Pin numbers

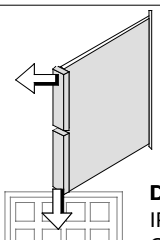
The pin numbers for the NT9X73BA appear in the diagram that follows the functional block diagram.

NT9X73BA (continued)

NT9X73BA functional blocks



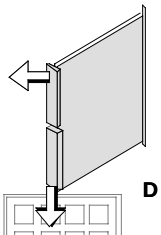
NT9X73BA pin numbers (Part 1 of 2)



	D	C	B	A
1	IP 0	AD 37	AD 00	GND
2	OP 0	ADP 3	AD 01	GND
3	IP 1	ADREN–	AD 02	GND
4	OP 1	DATEN–	AD 03	GND
5	IP 2	EOS–	AD 04	GND
6	OP 2	NVB 0	AD 05	GND
7	IP 3	NVB 1	AD 06	GND
8	OP 3	POK–	AD 07	GND
9	SEG 0	BNF–	ADP 0	GND
10	SEG 1	SRCEN–	AD 10	GND
11	SEG 2	DSTEN–	AD 11	GND
12	SEG 3	REQ–	AD 12	GND
13	SEG 4	GRT–	AD 13	FCLK+ I01
14		INH–	AD 14	FCLK– I02
15	PLN0–		AD 15	FAD0+ I03
16			AD 16	FAD0– I04
17		BUSGRI–	AD 17	FAD1+ I05
18		BUSGRO–	ADP 1	FAD1– I06
19			AD 20	FAD2+ I07
20			AD 21	FAD2– I08
21		PERINT4–	AD 22	FAD3+ I09
22			AD 23	FAD3– I010
23	RSTOUT–		AD 24	FAD4+ I011
24			AD 25	FAD4– I012
25	BEN1–	BEN0–	AD 26	FAD5+ I013
26	BEN3–	BEN2–	AD 27	FAD5– I014
27	GND		ADP 2	FAD6+ I015
28	WRT–	GND	AD 30	FAD6– I016
29	EDTACK–		AD 31	HW4
30	PARITY+		AD 32	
31	PRTYEN–		AD 33	
32		GND	AD 34	SH0
33	DAS32–		AD 35	SH1
34			AD 36	FP61–
35				C61
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5V
45		ADDR11		+5V

NT9X73BA (end)

NT9X73BA pin numbers (Part 2 of 2)



	D	C	B	A
46		ADDR12		+5V
47		ADDR13		+5V
48		ADDR14		+5V
49		ADDR15		+5V
50		ADDR16		+5V
51		ADDR17		+5V
52		ADDR18		+5V
53		ADDR19		+5V
54		ADDR20		+5V
55		ADDR21		+5V
56		ADDR22		
57		ADDR23		
58	DATA24	ADDR24		
59	DATA25	ADDR25		
60	DATA26	ADDR26		
61	DATA27	ADDR27		
62	DATA28	ADDR28		
63	DATA29	ADDR29		
64	DATA30	ADDR30		
65	DATA31	ADDR31		
66				
67				
68				
69				
70				
71	IDTX+ IO61			
72	IDTX– IO62			
73	IDRX+ IO63			
74	IDRX– IO64			
75	D0 IO45	FPOLL+ IO29		
76	D2 IO46	FPOLL– IO30		
77	D4 IO47	FREQ+ IO31		
78	D6 IO48	FREQ– IO32		
79		FPACK+ IO33	FAD7+ I017	GND
80	A2 IO50	FPACK– IO34	FAD7– I018	GND
81	A0 IO51	FRRDY+ IO35	FPAR+ I019	GND
82		FRRDY– IO36	FPAR– I020	GND
83		FRACK+ IO37	FADREN+ I021	GND
84	D7 IO54	FRACK– IO38	FADREN– I022	GND
85	A1 IO55	FWAIT+ IO39	FDAEN+ I023	GND
86	A3 IO56	FWAIT– IO40	FDAEN– I024	GND
87		FCLR+ IO41	FEOS+ I025	GND
88	D5 IO58	FCLR– IO42	FEOS– I026	GND
89	D3 IO59		FRST+ I027	GND
90	D1 IO60	CS79	FRST– I028	GND

NT9X73BB

Product description

The NT9X73BB triple rate adapter (RA) card is used in a link interface module (LIM) to transfer data packets from the local message switch (LMS) transaction bus (T-bus) to the frame transport bus (F-bus) and from the F-bus to the T-bus. The card provides rate translation between the 32-bit T-bus and 8-bit F-bus.

Location

The NT9X73BB is located in the LMS shelf of the enhanced link peripheral processor (ELPP) cabinet. Each LIM has six rate adapter cards, three for each LMS.

Functional description

In an ELPP cabinet, the NT9X73BB card provides an interface between the LMS and the dual-link link interface units (DLIU) located in the link interface shelves (LIS).

A DLIU is a set of high-speed link (HSL) termination hardware. Each set consists of:

- a high-speed link interface unit (HLIU)
- a high-speed link router (HSLR)

Functional blocks

NT9X73BB has the following functional blocks:

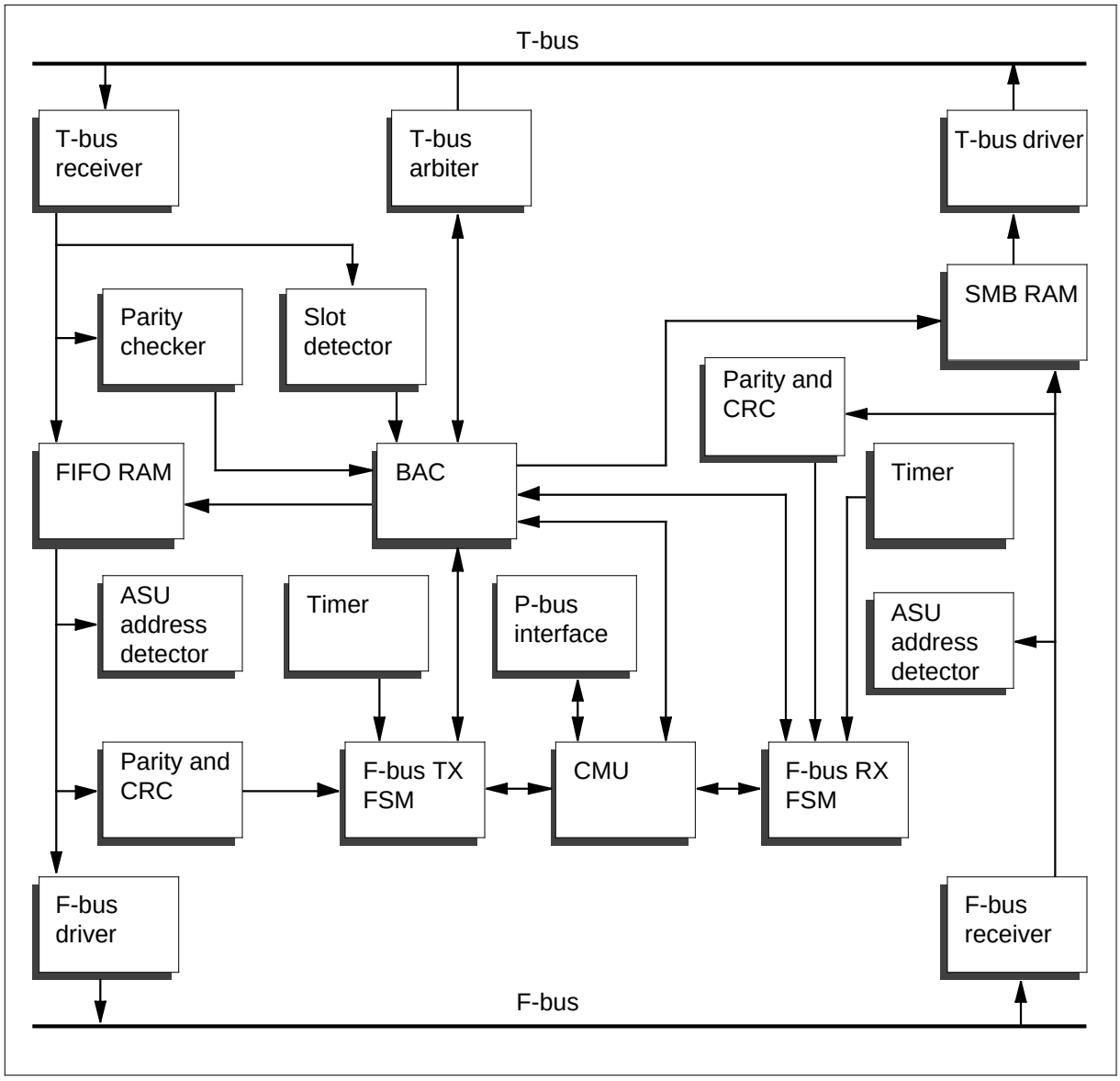
- bus access circuit (BAC)
- T-bus interface (T-bus receiver and driver)
- F-bus interface (F-bus receiver and driver)
- single message buffer (SMB) random access memory (RAM)
- first-in first-out (FIFO) RAM
- F-bus transmit finite state machine (TX FSM)
- F-bus receive FSM (RX FSM)
- F-bus arbiter
- T-bus arbiter
- parity and cyclic redundancy checker (CRC)
- processor bus (P-bus) interface
- card maintenance unit (CMU)

NT9X73BB (continued)

- ASU address detector
- slot detector

The following figure shows the relationship of the functional blocks.

NT9X73BB functional blocks



The BAC stores and retrieves messages when either the F-bus or the T-bus interface requests an operation. The BAC connects to the SMB RAM in order to store messages from the F-bus and to transmit messages on the T-bus. It also

connects to FIFO RAM in order to store messages from the T-bus and to transmit messages on the F-bus.

The F-bus TX FSM controls message transmission on the F-bus. It communicates with the BAC to retrieve data from the FIFO and performs protocol translation on the F-bus. If there is a message in the FIFO, the FSM requests bus access from the F-bus arbiter. The arbiter gives the access to the FSM if the bus is not being used by ASU. The parity and CRC block checks the parity and cyclic redundancy of the data from FIFO.

When an ASU requires the bus, it sends the request to the F-bus arbiter, which checks if the bus is not being used by the F-bus TX FSM or by one of the ASUs. The first requesting ASU found in the polling scheme gets access to the bus. The F-bus RX FSM is informed and it receives the next message on the bus. The RX FSM sends the information to the BAC, which stores the message in the buffer. A parity and cyclic redundancy check is performed on the received message.

In the LIM, the LMS mapper translates the logical address of the incoming messages to an ASU physical address. The triple RA receives all messages on the T-bus addressed to any of the ASUs. The slot detector in the triple RA detects the physical address of the corresponding LIS and these messages are sent to the correct ASU. Messages from ASUs being sent outside the LIM follow the reverse path. Messages sent between ASUs go through the RA to the T-bus and return to the RA, which transmits them to the F-bus.

Loopback features are also provided with the NT9X73BB card. The triple RA receives messages with its physical address on the T-bus. These messages are sent on the F-bus and received by the F-bus RX FSM. The messages are then transmitted back on the T-bus. Loopback can be internal or external to the triple RA. External mode is the normal mode of operation while the internal mode can be used when the triple RA is out of service.

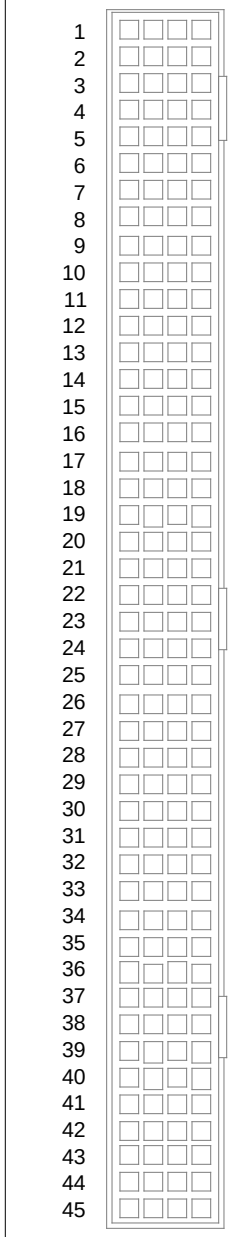
Signaling

Pin outs

The following figure shows the pin outs for NT9X73BB.

NT9X73BB (continued)

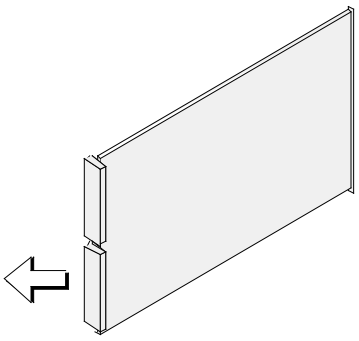
NT9X73BB pin outs (part 1 of 2)



	D	C	B	A
1	IP 0	AD 37	AD 00	GND
2	OP 0	ADP 3	AD 01	GND
3	IP 1	ADREN–	AD 02	GND
4	OP 1	DATEN–	AD 03	GND
5	IP 2	EOS–	AD 04	GND
6	OP 2	NVB 0	AD 05	GND
7	IP 3	NVB 1	AD 06	GND
8	OP 3	POK–	AD 07	GND
9	SEG 0	BNF–	ADP 0	GND
10	SEG 1	SRCEN–	AD 10	GND
11	SEG 2	DSTEN–	AD 11	GND
12	SEG 3	REQ–	AD 12	GND
13	SEG 4	GRT–	AD 13	FCLK+ IO1
14		INH–	AD 14	FCLK– IO2
15	PLN0–		AD 15	FAD0+ IO3
16			AD 16	FAD0– IO4
17		BUSGRI–	AD 17	FAD1+ IO5
18		BUSGRO–	ADP 1	FAD1– IO6
19			AD 20	FAD2+ IO7
20			AD 21	FAD2– IO8
21		PERINT4–	AD 22	FAD3+ IO9
22			AD 23	FAD3– IO10
23	RSTOUT		AD 24	FAD4+ IO11
24			AD 25	FAD4– IO12
25	BEN1–	BEN0–	AD 26	FAD5+ IO13
26	BEN3–	BEN2–	AD 27	FAD5– IO14
27	GND		ADP 2	FAD6+ IO15
28	WRT–	GND	AD 30	FAD6– IO16
29	EDTACK–		AD 31	HW4
30	PARITY+		AD 32	
31	PRTYEN–		AD 33	
32		GND	AD 34	SH0
33	DAS32–		AD 35	SH1
34			AD 36	FP61–
35				C61
36		ADDR02	HW0	
37		ADDR03	HW1	
38		ADDR04	HW2	
39		ADDR05	HW3	
40		ADDR06		GND
41		ADDR07		GND
42		ADDR08		GND
43		ADDR09		GND
44		ADDR10		+5 V
45		ADDR11		+5 V

NT9X73BB pin outs (part 2 of 2)

	D		C		B		A
46			ADDR12				+5 V
47			ADDR13				+5 V
48			ADDR14				+5 V
49			ADDR15				+5 V
50			ADDR16				+5 V
51			ADDR17				+5 V
52			ADDR18				+5 V
53			ADDR19				+5 V
54			ADDR20				+5 V
55			ADDR21				+5 V
56			ADDR22				
57			ADDR23				
58	DATA24		ADDR24				
59	DATA25		ADDR25				
60	DATA26		ADDR26				
61	DATA27		ADDR27				
62	DATA28		ADDR28				
63	DATA29		ADDR29				
64	DATA30		ADDR30				
65	DATA31		ADDR31				
66							
67							
68							
69							
70							
71	IDTX+	IO61					
72	IDTX–	IO62					
73	IDRX+	IO63					
74	IDRX–	IO64					
75	D0	IO45	FPOLL+	IO29			
76	D2	IO46	FPOLL–	IO30			
77	D4	IO47	FREQ+	IO31			
78	D6	IO48	FREQ–	IO32			
79			FPACK+	IO33	FAD7+	IO17	GND
80	A2	IO50	FPACK–	IO34	FAD7–	IO18	GND
81	A0	IO51	FRRDY+	IO35	FPAR+	IO19	GND
82			FRRDY–	IO36	FPAR–	IO20	GND
83			FRACK+	IO37	FADREN+	IO21	GND
84	D7	IO54	FRACK–	IO38	FADREN–	IO22	GND
85	A1	IO55	FWAIT+	IO39	FDAEN+	IO23	GND
86	A3	IO56	FWAIT–	IO40	FDAEN–	IO24	GND
87			FCLR+	IO41	FEOS+	IO25	GND
88	D5	IO58	FCLR–	IO42	FEOS–	IO26	GND
89	D3	IO59			FRST+	IO27	GND
90	D1	IO60	CS79	IO44	FRST–	IO28	GND



NT9X73BB (end)

Technical data

Power requirements

The following table shows the power requirements for the NT9X73BB.

NT9X73BB power requirements

Parameter	Minimum	Nominal	Maximum
Supply voltage	4.75 V	5.0 V	5.25 V
Supply current		4.29 A	
Power		21.45 W	

NT9X74AA

Product description

The Frame transport bus (F-bus) repeater card repeats and reclocks all F-bus communications. This communication occurs between the intershelf F-bus and the intrashelf F-bus. Each repeater card contains the circuits required to drive one of the two separate F-buses.

The F-bus repeater also contains loopback circuits that allow the following functions:

- the isolation of faults.
- a microcontroller to read pack IDs.
- the transfer of pack IDs to the NT9X73 card (rate adapter (RA)) over a serial link.

Location

Each LIU7 shelf at card locations 07 and 32 contains the card. These card locations correspond to card slots 1 and 26.

Functional description

The F-bus repeater card provides the following separate functions:

- buffer and reclock of the F-bus signals.
- loopback capabilities.
- access to card IDs.

Functional blocks

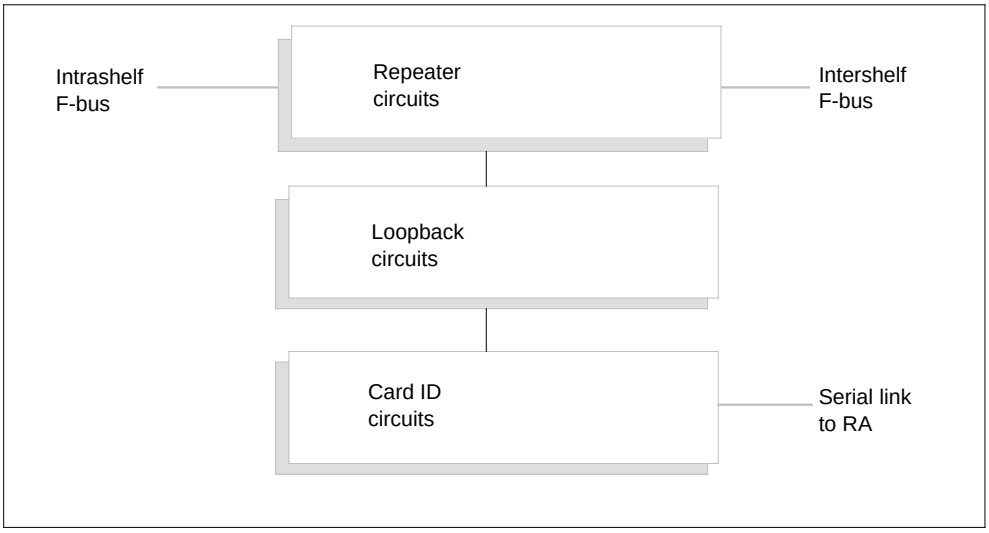
The NT9X74AA has the following functional blocks:

- repeater circuits
- loopback circuits
- card ID circuits

The functional relationship between these blocks appears in the following figure.

NT9X74AA (continued)

NT9X74AA functional blocks



Repeater circuits

The repeater circuits buffers and reclocks the signals between the intershelf F-bus and the intrashelf F-bus. The intershelf F-bus is the NT9X73 RA. The intrashelf F-bus is the NT9X75. The NT9X75 is the processor frame bus interface (PFI). The PFIs control two signals that select the direction of the buffers.

Loopback circuits

The loopback circuits allows the repeater to receive messages from the RA and transmit the messages back to the RA. Loopback can occur on the intershelf side or the intrashelf side. This capability allows F-bus tests that do not rely on the PFIs.

Card ID circuits

The card ID circuits allow the repeater to read the card IDs of the following:

- NT9X74 (F-bus repeater)
- NT9X79 (F-bus extension paddle board)
- NT9X30 (5-V power converter)

A microcontroller reads the card IDs. The microcontroller uses a serial link to communicate with the RA.

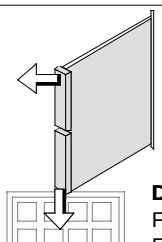
Signaling

Pin numbers

The pin numbers for NT9X74AA at card locations 7 and 32 appear in the following figures.

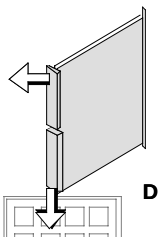
NT9X74AA (continued)

NT9X74AA pin numbers for card location 7 (Part 1 of 2)



	D	C	B	A
1	FBWAIT–	FAWAIT–	FAAD0	Gnd
2	FBCLR–	FACLR–	FAAD1	Gnd
3	FBREQ–	FAREQ–	FAAD2	Gnd
4	FBPOLL–	FAPOLL–	FAAD3	Gnd
5	FBRST–	FARST–	FAAD4	Gnd
6	FBPACK–	FAPACK–	FAAD5	Gnd
7	Gnd	Gnd	FAAD6	Gnd
8	FBADREN–	FAADREN–	FAAD7	Gnd
9	FBDATEN–	FADATEN–	FAPAR	Gnd
10	FBEOS–	FAEOS–	Gnd	Gnd
11	FBRACK–	FARACK–	FBAD0	Gnd
12	FBRRDY–	FARRDY–	FBAD1	Gnd
13	FBSRCEN–	FASRCEN–	FBAD2	FCLK+
14	FBDSTEN–	FADSTEN–	FBAD3	FCLK–
15	Gnd	Gnd	FBAD4	FAD0+
16	Gnd	Gnd	FBAD5	FAD0–
17			FBAD6	FAD1+
18			FBAD7	FAD1–
19			FBPAR	FAD2+
20	Gnd		Gnd	FAD2–
21	Gnd			FAD3+
22				FAD3–
23				FAD4+
24				FAD4–
25				FAD5+
26				FAD5–
27	Gnd			FAD6+
28		Gnd		FAD6–
29				HW4
30		FB+5TERM		Gnd
31		FB+5TERM		FACLK
32		Gnd		SH0
33				SH1
34				Gnd
35				FBCLK
36			HW0	
37			HW1	
38			HW2	
39			HW3	
40				Gnd
41				Gnd
42				Gnd
43				Gnd
44				+5V
45				+5V

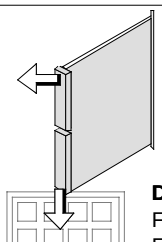
NT9X74AA pin numbers for card location 7 (Part 2 of 2)



	D	C	B	A
46				+5V
47		Gnd		+5V
48				+5V
49				+5V
50			Gnd	+5V
51				+5V
52				+5V
53			Gnd	+5V
54				+5V
55				+5V
56			Gnd	
57				
58				
59				
60				
61				
62				
63				
64				
65				
66	Gnd			
67				
68				
69		Gnd		
70				
71	IDTX+			
72	IDTX–			
73	IDRX+			
74	IDRX–			
75	D0	FPOLL+		
76	D2	FPOLL–		
77	D4	FREQ+		
78	D6	FREQ–		
79	CS5–	FPACK+	FAD7+	Gnd
80	A2	FPACK–	FAD7–	Gnd
81	A0	FRRDY+	FPAR+	Gnd
82		FRRDY–	FPAR–	Gnd
83	PLOCK	FRACK+	FADREN+	Gnd
84	D7	FRACK–	FADREN–	Gnd
85	A1	FWAIT+	FDAEN+	Gnd
86	A3	FWAOT–	FDAEN–	Gnd
87	CS5+	FCLR+	FEOS+	Gnd
88	D5	FCLR–	FEOS–	Gnd
89	D3		FRST+	Gnd
90	D1	CS79	FRST–	Gnd

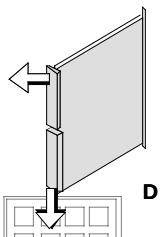
NT9X74AA (continued)

NT9X74AA pin numbers for card location 32 (Part 1 of 2)



	D	C	B	A
1	FAWAIT–	FBWAIT–	FBAD0	Gnd
2	FACLR–	FBCLR–	FBAD1	Gnd
3	FAREQ–	FBREQ–	FBAD2	Gnd
4	FAPOLL–	FBPOLL–	FBAD3	Gnd
5	FARST–	FBRST–	FBAD4	Gnd
6	FAPACK–	FBPACK–	FBAD5	Gnd
7	Gnd	Gnd	FBAD6	Gnd
8	FAADREN–	FBADREN–	FBAD7	Gnd
9	FADATEN–	FBDATEN–	FAPAR	Gnd
10	FAEOS–	FBEOS–	Gnd	Gnd
11	FARACK–	FBRACK–	FAAD0	Gnd
12	FARRDY–	FBRRDY–	FAAD1	FCLK+
13	FASRCEN–	FBSRCEN–	FAAD2	FCLK–
14	FADSTEN–	FBDSTEN–	FAAD3	Gnd
15	Gnd	Gnd	FAAD4	FAD0+
16	Gnd	Gnd	FAAD5	FAD0–
17			FAAD6	FAD1+
18			FAAD7	FAD1–
19			FAPAR	FAD2+
20	Gnd		Gnd	FAD2–
21	Gnd			FAD3+
22				FAD3–
23				FAD4+
24				FAD4–
25				FAD5+
26				FAD5–
27	Gnd			FAD6+
28		Gnd		FAD6–
29				HW4
30		FA+5TERM		Gnd
31		FA5+TERM		BCLK
32		Gnd		SH0
33				SH1
34				Gnd
35				FACLK
36			HW0	
37			HW1	
38			HW2	
39			HW3	
40				Gnd
41				Gnd
42				Gnd
43				Gnd
44				+5V
45				+5V

NT9X74AA pin numbers for card location 32 (Part 2 of 2)



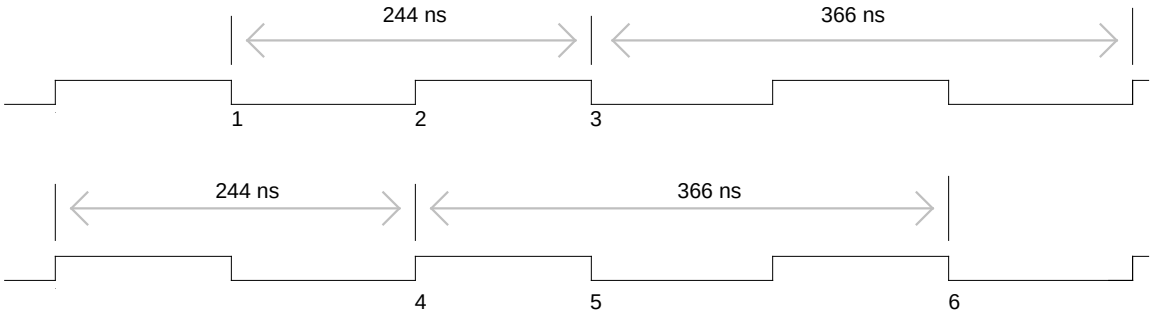
	D	C	B	A
46				+5V
47		Gnd		+5V
48				+5V
49				+5V
50			Gnd	+5V
51				+5V
52				+5V
53			Gnd	+5V
54				+5V
55				+5V
56			Gnd	
57				
58				
59				
60				
61				
62				
63				
64				
65				
66	Gnd			
67				
68				
69		Gnd		
70				
71	IDTX+			
72	IDTX–			
73	IDRX+			
74	IDRX–			
75	D0	FPOLL+		
76	D2	FPOLL–		
77	D4	FREQ+		
78	D6	FREQ–		
79	CS5–	FPACK+	FAD7+	Gnd
80	A2	FPACK–	FAD7–	Gnd
81	A0	FRRDY+	FPAR+	Gnd
82		FRRDY–	FPAR–	Gnd
83	PLOCK	FRACK+	FADREN+	Gnd
84	D7	FRACK–	FADREN–	Gnd
85	A1	FWAIT+	FDAEN+	Gnd
86	A3	FWAIT–	FDAEN–	Gnd
87	CS5+	FCLR+	FEOS+	Gnd
88	D5	FCLR–	FEOS–	Gnd
89	D3		FRST+	Gnd
90	D1	CS79	FRST–	Gnd

NT9X74AA (end)

Timing

The timing for NT9X74AA appears in the following figure.

NT9X74AA timing



Legend

1 RA transmits to repeater on falling clock edge
2 Repeater latches data on rising clock edge
3 LIU7 latches data from repeater on falling clock edge
4 LIU7 transmits data to repeater on clock rising edge
5 Repeater latches data on clock falling edge
6 RA latches data from repeater on falling clock edge

NT9X74BA

Product description

The NT9X74BA F-bus repeater circuit pack buffers and reclocks signals between the intershelf frame transport bus (F-bus) and the intrashelf F-bus.

The BA version of the repeater card is like the AA version. The far end F-bus terminations of the AA version are removed and placed on the NTEX20AA and the BA.

Location

Each link interface shelf (LIS) contains the NT9X74BA at card locations 07 and 32. These card locations correspond to card slots 1 and 26.

Functional description

The NT9X74BA provides the following functions:

- buffer and reclock the F-bus signals.
- loopback capabilities.
- access to card IDs.

The system requires only one version of the repeater board. This requirement occurs because of the way the two independent F-buses run across the link interface shelf backplane (9X72AA). The repeater board in slot 07 drives the F-bus 0. The same repeater board in slot 32 drives the F-bus 1. The far end terminations for each F-bus are available on the EX20AA and the BA paddle boards.

Functional blocks

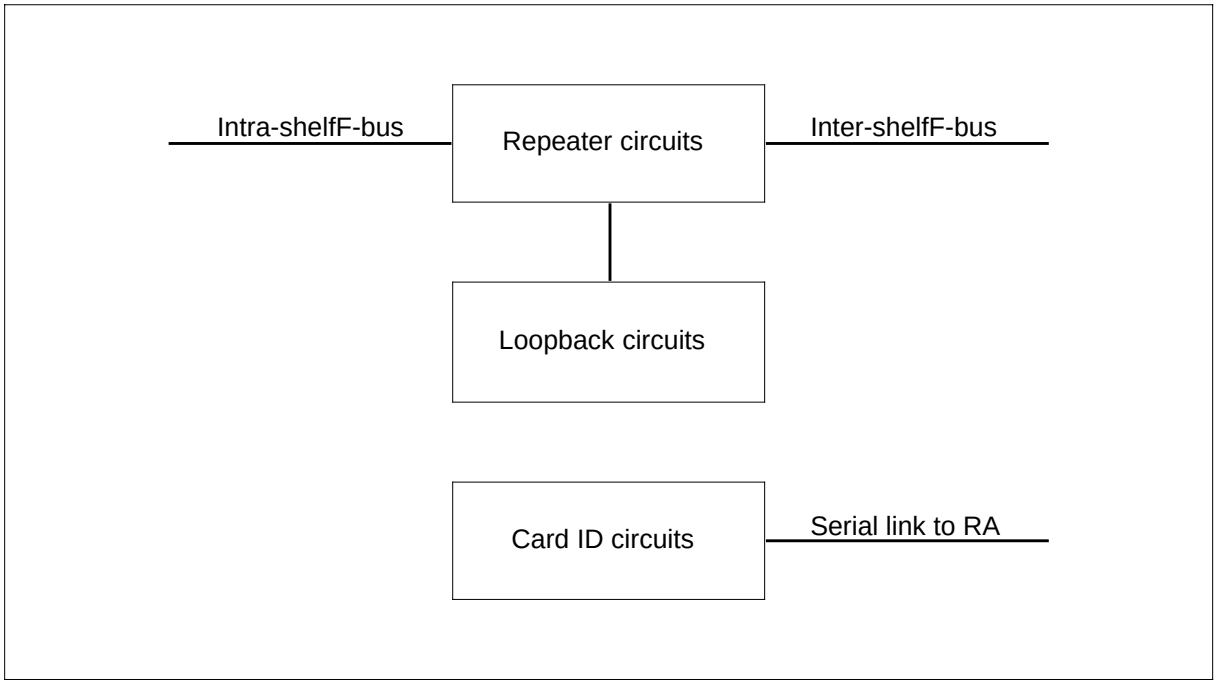
The NT9X74BA has the following functional blocks:

- repeater circuits
- loopback circuits
- card ID circuits

The relationship between the functional blocks appears in the following figure.

NT9X74BA (continued)

NT9X74BA functional blocks



Repeater circuits

The repeater circuits buffers and reclocks signals between the intershelf F-bus and the intrashelf F-bus. The application specific units (ASU) (FxDSTEN and FxSRCEN) controls two signals to select the direction of the buffers.

Loopback circuits

The loopback circuits receive messages from the RA and transmits the messages back to the RA. A loopback can occur on the intershelf or the intrashelf side. This capability allows tests of the F-bus which do not rely on the ASUs. Use of the two types of loopback allows the system to isolate intra-faults or inter-faults.

Card ID circuits

The card ID circuits reads the card IDs of the following:

- 9X74 (repeater)
- 9X79 (F-bus extension paddle board)
- 9X30 (5-V power converter)

The card ID circuits use a microcontroller to communicate with the RA over a serial link.

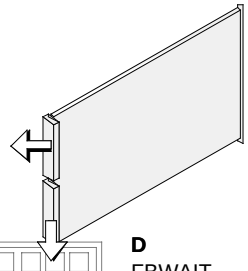
Signaling

Pin numbers

The pin numbers for the NT9X74BA at card locations 07 and 32 appear in the following figures.

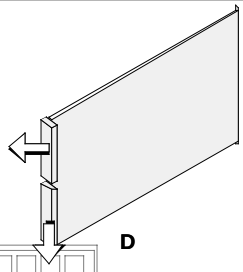
NT9X74BA (continued)

NT9X74BA pin numbers (in location 07) (Part 1 of 2)



	D	C	B	A
1	FBWAIT—	FAWAIT–	FAAD0	GND
2	FBCLR–	FACLR–	FAAD1	GND
3	FBREQ–	FAREQ–	FAAD2	GND
4	FBPOLL–	FAPOLL–	FAAD3	GND
5	FBRST–	FARST–	FAAD4	GND
6	FBPACK–	FAPACK–	FAAD5	GND
7	GNDGND	FAAD6	GND	
8	FBADREN–	FAADREN–	FAAD7	GND
9	FBDATEN–	FADATEN–	FAPAR	GND
10	FBEOS–	FAEOS–	GND	GND
11	FBRACK–	FARACK–	FBAD0	GND
12	FBRRDY–	FARRDY–	FBAD1	GND
13	FBSRCEN–	FASRCEN–	FBAD2	FCLK+ IO1
14	FBDSTEN–	FADSTEN–	FBAD3	FCLK– IO2
15	GND	GND	FBAD4	FAD0+ IO3
16	GND	GND	FBAD5	FAD0– IO4
17			FBAD6	FAD1+ IO5
18			FBAD7	FAD1– IO6
19			FBPAR	FAD2+ IO7
20	GND		GND	FAD2– IO8
21	GND			FAD3+ IO9
22				FAD3– IO10
23				FAD4+ IO11
24				FAD4– IO12
25				FAD5+ IO13
26				FAD5– IO14
27	GND			FAD6+ IO15
28		GND		FAD6– IO16
29				HW4
30			FB+5TERM	GND
31			FB+5TERM	FACLK
32		GND		SH0
33				SH1
34				GND
35				FBCLK
36			HW0	
37			HW1	
38			HW2	
39			HW3	
40				GND
41				GND
42				GND
43				GND
44				+5V
45				+5V

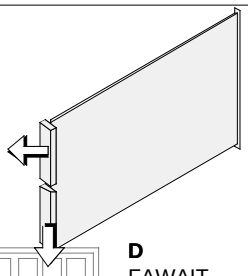
NT9X74BA pin numbers (in location 07) (Part 2 of 2)



	D		C		B		A	
46							+5V	
47			GND				+5V	
48							+5V	
49							+5V	
50					GND		+5V	
51							+5V	
52							+5V	
53					GND		+5V	
54							+5V	
55							+5V	
56					GND			
57								
58								
59								
60								
61								
62								
63								
64								
65								
66	GND							
67								
68								
69			GND					
70								
71	IDTX+	IO61						
72	IDTX–	IO62						
73	IDRX+	IO63						
74	IDRX–	IO64						
75	D0	O45	FPOLL+	IO29				
76	D2	IO46	FPOLL–	IO30				
77	D4	IO47	FREQ+	IO31				
78	D6	IO48	FREQ –	IO32				
79	CS5–	IO49	FPACK+	IO33	FAD7+	IO17	GND	
80	A2	IO50	FPACK–	IO34	FAD7–	IO18	GND	
81	A0	IO51	FRRDY+1	1O35	FPAR+	IO19	GND	
82			FRRDY–	IO36	FPAR–	IO20	GND	
83	PLOCK	IO53	FRACK–	IO37	FADREN+	IO21	GND	
84	D7	IO54	FRACK–	IO38	FADREN–	IO22	GND	
85	A1	IO55	FWAIT+	IO39	FDAEN+	IO23	GND	
86	A3	IO56	FWAIT–	IO40	FDAEN–	IO24	GND	
87	CS5+	IO57	FCLR+	IO41	FEOS+	IO25	GND	
88	D5	IO58	FCLR–	IO42	FEOS–	IO26	GND	
89	D3	IO59			FRST+	IO27	GND	
90	D1	IO60	CS79	IO44	FRST–	IO28	GND	

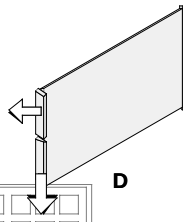
NT9X74BA (continued)

NT9X74BA pin numbers (in location 32) (Part 1 of 2)



	D	C	B	A
1	FAWAIT–	FBWAIT–	FBAD0	GND
2	FACLR–	FBCLR–	FBAD1	GND
3	FAREQ–	FBREQ–	FBAD2	GND
4	FAPOLL–	FBPOLL–	FBAD3	GND
5	FARST–	FBRST–	FBAD4	GND
6	FAPACK–	FBPACK–	FBAD5	GND
7	GNDGND	FBAD6	GND	
8	FAADREN–	FBADREN–	FBAD7	GND
9	FADATEN–	FBDATEN–	FBPAR	GND
10	FAEOS–	FBEOS–	GND	GND
11	FARACK–	FBRACK–	FAAD0	GND
12	FARRDY–	FBRRDY–	FAAD1	GND
13	FASRCEN–	FBSRCEN–	FAAD2	FCLK+ IO1
14	FADSTEN–	FBDSTEN–	FAAD3	FCLK– IO2
15	GND	GND	FAAD4	FAD0+ IO3
16	GND	GND	FAAD5	FAD0– IO4
17			FAAD6	FAD1+ IO5
18			FAAD7	FAD1– IO6
19			FAPAR	FAD2+ IO7
20	GND		GND	FAD2– IO8
21	GND			FAD3+ IO9
22				FAD3– IO10
23				FAD4+ IO11
24				FAD4– IO12
25				FAD5+ IO13
26				FAD5– IO14
27	GND			FAD6+ IO15
28		GND		FAD6– IO16
29				HW4
30			FA+5TERM	GND
31			FA+5TERM	FBCLK
32		GND		SH0
33				SH1
34				GND
35				FACLK
36			HW0	
37			HW1	
38			HW2	
39			HW3	
40				GND
41				GND
42				GND
43				GND
44				+5V
45				+5V

NT9X74BA pin numbers (in location 32) (Part 2 of 2)



	D	C		B		A
46						+5V
47		GND				+5V
48						+5V
49						+5V
50				GND		+5V
51						+5V
52						+5V
53				GND		+5V
54						+5V
55						+5V
56				GND		
57						
58						
59						
60						
61						
62						
63						
64						
65						
66	GND					
67						
68						
69		GND				
70						
71	IDTX+ IO61					
72	IDTX– IO62					
73	IDRX+ IO63					
74	IDRX– IO64					
75	D0 IO45	FPOLL+	IO29			
76	D2 IO46	FPOLL–	IO30			
77	D4 IO47	FREQ+	IO31			
78	D6 IO48	FREQ–	IO32			
79	CS5– IO49	FPACK+	IO33	FAD7+	IO17	GND
80	A2 IO50	FPACK–	IO34	FAD7–	IO18	GND
81	A0 IO51	FRRDY+	IO35	FPAR+	IO19	GND
82		FRRDY–	IO36	FPAR–	IO20	GND
83	PLOCK IO53	FRACK+	IO37	FADREN+	IO21	GND
84	D7 IO54	FRACK–	IO38	FADREN–	IO22	GND
85	A1 IO55	FWAIT+	IO39	FDAEN+	IO23	GND
86	A3 IO56	FWAIT–	IO40	FDAEN–	IO24	GND
87	CS5+ IO57	FCLR+	IO41	FEOS+	IO25	GND
88	D5 IO58	FCLR–	IO42	FEOS–	IO26	GND
89	D3 IO59			FRST+	IO27	GND
90	D1 IO60	CS79	IO44	FRST–	IO28	GND

DMS-100 Family

Hardware Description Manual

Volume 4 of 5

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