# Critical Release Notice

**Publication number: 297-8991-805**
**Publication release: Standard 11.03**

## The content of this customer NTP supports the SN06 (DMS) software release.

Bookmarks used in this NTP highlight the changes between the LEC0015 baseline and the current release. The bookmarks provided are color-coded to identify release-specific content changes. NTP volumes that do not contain bookmarks indicate that the LEC0015 baseline remains unchanged and is valid for the current release.

### Bookmark Color Legend

**Black: Applies to new or modified content for LEC0015 that is valid through the current release.**

**Red: Applies to new or modified content for SN04 (DMS) that is valid through the current release.**

**Blue: Applies to new or modified content for SN05 (DMS) that is valid through the current release.**

**Green: Applies to new or modified content for SN06 (DMS) that is valid through the current release.**

*Attention!*
*Adobe® Acrobat® Reader™ 5.0 or higher is required to view bookmarks in color.*

# Publication History

**June 2005**

Standard release 11.03 for software release SN06 (DMS). Updates made for this release are shown below:

**Volume 5**

Added NTDX16AA (Q00946403)

**March 2004**

Standard release 11.02 for software release SN06 (DMS). Updates made for this release are shown below:

**Volumes 1 – 3**

No changes

**Volume 4**

Card NT9X30AB is Manufacture Discontinued and is replaced by new card NT9X30AC.

**Volume 5**

No changes

**September 2003**

Standard release 11.01 for software release SN06 (DMS). Updates made for this release are shown below:

**Volumes 1 – 4**

No changes

**Volume 5**

Updates were made to NT9X76AA according to CR Q00177945.

297-8991-805

DMS-100 Family

# Hardware Description Manual

Volume 5 of 5

2001Q1 Standard 09.01 March 2001

NORTEL NETWORKS

How the world shares ideas.

DMS-100 Family

# Hardware Description Manual

Volume 5 of 5

Publication number: 297-8991-805
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# 1 NT9Xnnaa (continued)

## NT9X74CA through NT9X98AA (continued from Vol. 4)

# NT9X74CA

## Product description

The NT9X74CA frame transport bus (F–bus) repeater card buffers and reclocks signals between the intershelf F–bus and the intrashelf F–bus.

The CA version of the repeater card is like the BA version. The BA version has added firmware function to query the identification (ID) PROM of the NTEX20AA and BA.

### Location

The NT9X74CA is on each link interface shelf (LIS) at card locations 07 and 32. These card locations correspond to card slots 1 and 26.

## Functional description

The NT9X74CA provides the following functions:

- buffer and reclock the F–bus signals
- loopback capabilities
- access to card IDs

The system requires only one version of the repeater board. This requirement occurs because of the way the two independent F–buses are run across the link interface shelf backplane (9X72AA). The repeater board in slot 07 drives the F–bus 0. The same repeater board in slot 32 drives the F–bus 1. The far–end terminations for each F–bus are available on the EX20AA and the BA paddle boards.

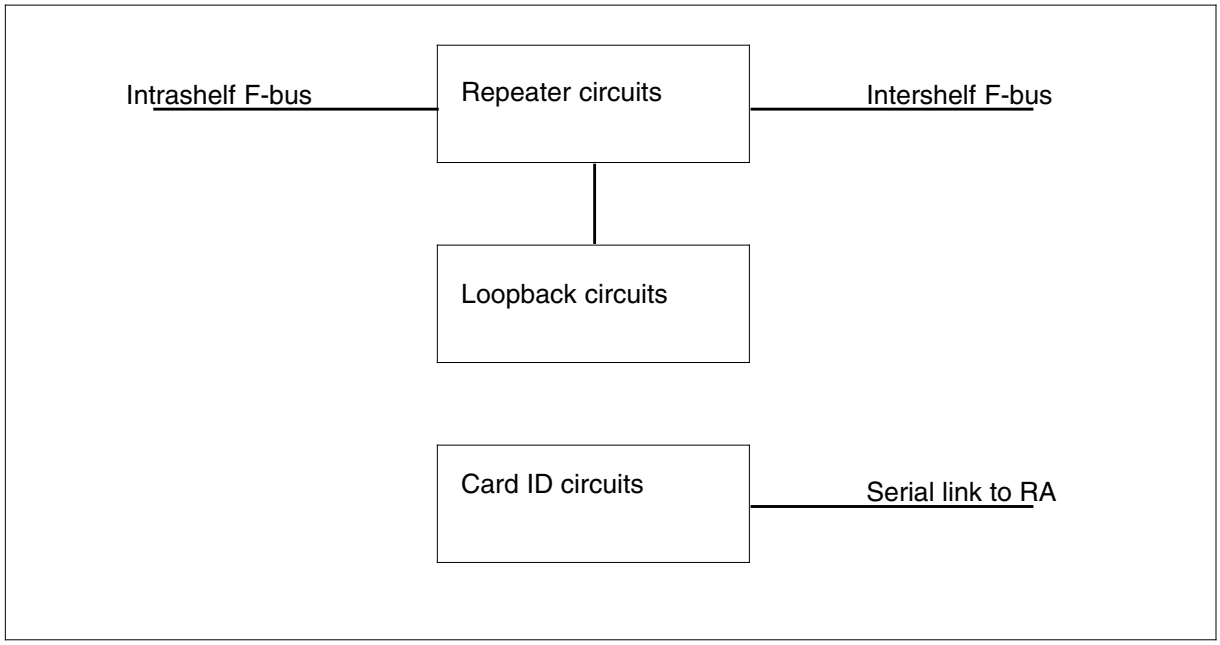
### Functional blocks

The NT9X74CA has the following functional blocks:

- repeater circuits
- loopback circuits
- card ID circuits

The relationship between the functional blocks appears in the following figure.

**NT9X74CA functional blocks**




### Repeater circuits

The repeater circuits buffers and reclocks signals between the intershelf F–bus and the intrashelf F–bus. The application specific unit (ASU) (FxDSTEN and FxSRCEN) controls two signals that select the direction of the buffers.

### Loopback circuits

The loopback circuits receives messages from the RA and transmits them back to the RA. A loopback can occur on the intershelf or the intrashelf side. This capability allows tests of the F–bus that do not rely on the ASUs. Use of the two types of loopback allows the system to isolate intrafaults or interfaults.

### Card ID circuits

The card ID circuits reads the card IDs of the following:

- the 9X74 (repeater),
- the 9X79 (F–bus extension paddle board)
- the 9X30 (5–V power converter)
- the EX20 (F–bus to C–bus termination paddle board).

The card ID circuits use a microcontroller to communicate with the RA over a serial link.

## **NT9X74CA** (continued)

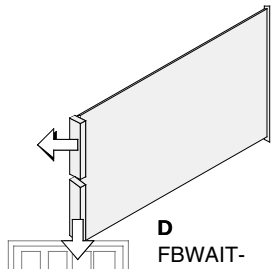
# Signaling

### Pin numbers

The pin numbers for the NT9X at card locations 07 and 32 appear in the following figures.

# **NT9X74CA** (continued)

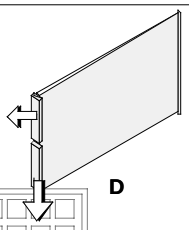
**NT9X pin numbers (in location 07) (Part 1 of 2)**



| | D | C | B | A | |
|---|---|---|---|---|---|
| 1 | FBWAIT- | FAWAIT- | FAAD0 | GND | |
| 2 | FBCLR- | FACLR- | FAAD1 | GND | |
| 3 | FBREQ- | FAREQ- | FAAD2 | GND | |
| 4 | FBPOLL- | FAPOLL- | FAAD3 | GND | |
| 5 | FBRST- | FARST- | FAAD4 | GND | |
| 6 | FBPACK- | FAPACK- | FAAD5 | GND | |
| 7 | GNDGND | FAAD6 | GND | | |
| 8 | FBADREN- | FAADREN- | FAAD7 | GND | |
| 9 | FBDATEN- | FADATEN- | FAPAR | GND | |
| 10 | FBEOS- | FAEOS- | GND GND | | |
| 11 | FBRACK- | FARACK- | FBAD0 | GND | |
| 12 | FBRRDY- | FARRDY- | FBAD1 | GND | |
| 13 | FBSRCEN- | FASRCEN- | FBAD2 | FCLK+ | IO1 |
| 14 | FBDSTEN- | FADSTEN- | FBAD3 | FCLK- | IO2 |
| 15 | GND | GND | FBAD4 | FAD0+ | IO3 |
| 16 | GND | GND | FBAD5 | FAD0- | IO4 |
| 17 | | | FBAD6 | FAD1+ | IO5 |
| 18 | | | FBAD7 | FAD1- | IO6 |
| 19 | | | FBPAR | FAD2+ | IO7 |
| 20 | GND | | GND | FAD2- | IO8 |
| 21 | GND | | | FAD3+ | IO9 |
| 22 | | | | FAD3- | IO10 |
| 23 | | | | FAD4+ | IO11 |
| 24 | | | | FAD4- | IO12 |
| 25 | | | | FAD5+ | IO13 |
| 26 | | | | FAD5- | IO14 |
| 27 | GND | | | FAD6+ | IO15 |
| 28 | | GND | | FAD6- | IO16 |
| 29 | | | | HW4 | |
| 30 | | | FB+5TERM | GND | |
| 31 | | | FB+5TERM | FACLK | |
| 32 | | GND | | SH0 | |
| 33 | | | | SH1 | |
| 34 | | | | GND | |
| 35 | | | | FBCLK | |
| 36 | | | HW0 | | |
| 37 | | | HW1 | | |
| 38 | | | HW2 | | |
| 39 | | | HW3 | | |
| 40 | | | | GND | |
| 41 | | | | GND | |
| 42 | | | | GND | |
| 43 | | | | GND | |
| 44 | | | | +5 V | |
| 45 | | | | +5 V | |

# **NT9X74CA** (continued)

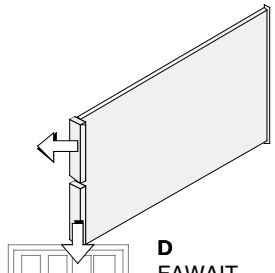
### NT9X pin numbers (in location 07) (Part 2 of 2)



| | D | C | | B | | A |
|---|---|---|---|---|---|---|
| 46 | | | | | | +5V |
| 47 | | GND | | | | +5V |
| 48 | | | | | | +5V |
| 49 | | | | | | +5V |
| 50 | | | | GND | | +5V |
| 51 | | | | | | +5V |
| 52 | | | | | | +5V |
| 53 | | | | GND | | +5V |
| 54 | | | | | | +5V |
| 55 | | | | | | +5V |
| 56 | | | | GND | | |
| 57 | | | | | | |
| 58 | | | | | | |
| 59 | | | | | | |
| 60 | | | | | | |
| 61 | | | | | | |
| 62 | | | | | | |
| 63 | | | | | | |
| 64 | | | | | | |
| 65 | | | | | | |
| 66 | GND | | | | | |
| 67 | | | | | | |
| 68 | | | | | | |
| 69 | | GND | | | | |
| 70 | | CSSFT | | | | |
| 71 | IDTX+ IO61 | | | | | |
| 72 | IDTX- IO62 | | | | | |
| 73 | IDRX+ IO63 | | | | | |
| 74 | IDRX- IO64 | | | | | |
| 75 | D0 IO45 | FPOLL+ | IO29 | | | |
| 76 | D2 IO46 | FPOLL- | IO30 | | | |
| 77 | D4 IO47 | FREQ+ | IO31 | | | |
| 78 | D6 IO48 | FREQ- | IO32 | | | |
| 79 | CS5- IO49 | FPACK+ | IO33 | FAD7+ | IO17 | GND |
| 80 | A2 IO50 | FPACK- | IO34 | FAD7- | IO18 | GND |
| 81 | A0 IO51 | FRRDY+ | IO35 | FPAR+ | IO19 | GND |
| 82 | | FRRDY- | IO36 | FPAR- | IO20 | GND |
| 83 | PLOCK IO53 | FRACK+ | IO37 | FADREN+ | IO21 | GND |
| 84 | D7 IO54 | FRACK- | IO38 | FADREN- | IO22 | GND |
| 85 | A1 IO55 | FWAIT+ | IO39 | FDAEN+ | IO23 | GND |
| 86 | A3 IO56 | FWAIT- | IO40 | FDAEN- | IO24 | GND |
| 87 | CS5+ IO57 | FCLR+ | IO41 | FEOS+ | IO25 | GND |
| 88 | D5 IO58 | FCLR- | IO42 | FEOS- | IO26 | GND |
| 89 | D3 IO59 | | | FRST+ | IO27 | GND |
| 90 | D1 IO60 | CS79 | IO44 | FRST- | IO28 | GND |

# **NT9X74CA** (continued)

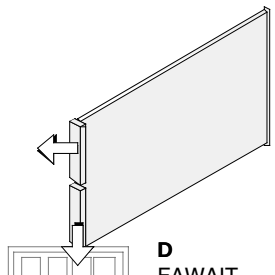
**NT9X pin numbers (in location 32) (Part 1 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 1 | FAWAIT- | FBWAIT- | FBAD0 | GND |
| 2 | FACLR- | FBCLR- | FBAD1 | GND |
| 3 | FAREQ- | FBREQ- | FBAD2 | GND |
| 4 | FAPOLL- | FBPOLL- | FBAD3 | GND |
| 5 | FARST- | FBRST- | FBAD4 | GND |
| 6 | FAPACK- | FBPACK- | FBAD5 | GND |
| 7 | GND | GND | FBAD6 | GND |
| 8 | FAADREN- | FBADREN- | FBAD7 | GND |
| 9 | FADATEN- | FBDATEN- | FBPAR | GND |
| 10 | FAEOS- | FBEOS- | GND | GND |
| 11 | FARACK- | FBRACK- | FAAD0 | GND |
| 12 | FARRDY- | FBRRDY- | FAAD1 | GND |
| 13 | FASRCEN- | FBSRCEN- | FAAD2 | FCLK+ IO1 |
| 14 | FADSTEN- | FBDSTEN- | FAAD3 | FCLK- IO2 |
| 15 | GND | GND | FAAD4 | FAD0+ IO3 |
| 16 | GND | GND | FAAD5 | FAD0- IO4 |
| 17 | | | FAAD6 | FAD1+ IO5 |
| 18 | | | FAAD7 | FAD1- IO6 |
| 19 | | | FAPAR | FAD2+ IO7 |
| 20 | GND | | GND | FAD2- IO8 |
| 21 | GND | | | FAD3+ IO9 |
| 22 | | | | FAD3- IO10 |
| 23 | | | | FAD4+ IO11 |
| 24 | | | | FAD4- IO12 |
| 25 | | | | FAD5+ IO13 |
| 26 | | | | FAD5- IO14 |
| 27 | GND | | | FAD6+ IO15 |
| 28 | | | GND | FAD6- IO16 |
| 29 | | | | HW4 |
| 30 | | | FA+5TERM | GND |
| 31 | | | FA+5TERM | FBCLK |
| 32 | | GND | | SH0 |
| 33 | | | | SH1 |
| 34 | | | | GND |
| 35 | | | | FACLK |
| 36 | | | HW0 | |
| 37 | | | HW1 | |
| 38 | | | HW2 | |
| 39 | | | HW3 | |
| 40 | | | | GND |
| 41 | | | | GND |
| 42 | | | | GND |
| 43 | | | | GND |
| 44 | | | | +5 V |
| 45 | | | | +5 V |

# **NT9X74CA** (end)

### NT9X pin numbers (in location 32) (Part 2 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 1 | FAWAIT- | FBWAIT- | FBAD0 | GND |
| 2 | FACLR- | FBCLR- | FBAD1 | GND |
| 3 | FAREQ- | FBREQ- | FBAD2 | GND |
| 4 | FAPOLL- | FBPOLL- | FBAD3 | GND |
| 5 | FARST- | FBRST- | FBAD4 | GND |
| 6 | FAPACK- | FBPACK- | FBAD5 | GND |
| 7 | GND | GND | FBAD6 | GND |
| 8 | FAADREN- | FBADREN- | FBAD7 | GND |
| 9 | FADATEN- | FBDATEN- | FBPAR | GND |
| 10 | FAEOS- | FBEOS- | GND | GND |
| 11 | FARACK- | FBRACK- | FAAD0 | GND |
| 12 | FARRDY- | FBRRDY- | FAAD1 | GND |
| 13 | FASRCEN- | FBSRCEN- | FAAD2 | FCLK+ IO1 |
| 14 | FADSTEN- | FBDSTEN- | FAAD3 | FCLK- IO2 |
| 15 | GND | GND | FAAD4 | FAD0+ IO3 |
| 16 | GND | GND | FAAD5 | FAD0- IO4 |
| 17 | | | FAAD6 | FAD1+ IO5 |
| 18 | | | FAAD7 | FAD1- IO6 |
| 19 | | | FAPAR | FAD2+ IO7 |
| 20 | GND | | GND | FAD2- IO8 |
| 21 | GND | | | FAD3+ IO9 |
| 22 | | | | FAD3- IO10 |
| 23 | | | | FAD4+ IO11 |
| 24 | | | | FAD4- IO12 |
| 25 | | | | FAD5+ IO13 |
| 26 | | | | FAD5- IO14 |
| 27 | GND | | | FAD6+ IO15 |
| 28 | | | GND | FAD6- IO16 |
| 29 | | | | HW4 |
| 30 | | | FA+5TERM | GND |
| 31 | | | FA+5TERM | FBCLK |
| 32 | | GND | | SH0 |
| 33 | | | | SH1 |
| 34 | | | | GND |
| 35 | | | | FACLK |
| 36 | | | HW0 | |
| 37 | | | HW1 | |
| 38 | | | HW2 | |
| 39 | | | HW3 | |
| 40 | | | | GND |
| 41 | | | | GND |
| 42 | | | | GND |
| 43 | | | | GND |
| 44 | | | | +5 V |
| 45 | | | | +5 V |

# NT9X74DA

## Product description

The NT9X74DA reclocks and repeats all frame bus (F–bus) communication between the intershelf F–bus and the intrashelf F–bus. Each NT9X74DA contains the circuits to drive one of the two separate F–buses.

The NT9X74DA supercedes the NT9X74CA. The NT9X74DA has channel bus (C–bus) terminations for link peripheral processor (LPP) channel access.

### Location

The NT9X74DA is in the CCS7 link interface unit 7 (LIU7) shelf in card slot 07 or 32.

## Functional description

### Functional blocks

The NT9X74DA has the following functional blocks:

- repeater circuits
- loopback circuits
- card ID circuits

### Repeater circuits

The repeater circuits buffers and reclocks signals between the intershelf F–bus (RA) and the intrashelf F–bus (PFI). The PFIs, FxDSTEN and FxSRCEN control two signals to select the direction of the buffers.

### Loopback circuits

The loopback circuits permits the repeater to communicate with the RA. Loopback can occur on the intershelf side or on the intrashelf side. This capability allows testing of the F–bus which do not rely on the application–specific units (ASU). Use of the two types of loopback allows the system to isolate intrashelf faults or intershelf faults.

### Card ID circuits

The card ID circuits allows the repeater to read the card IDs of the following:

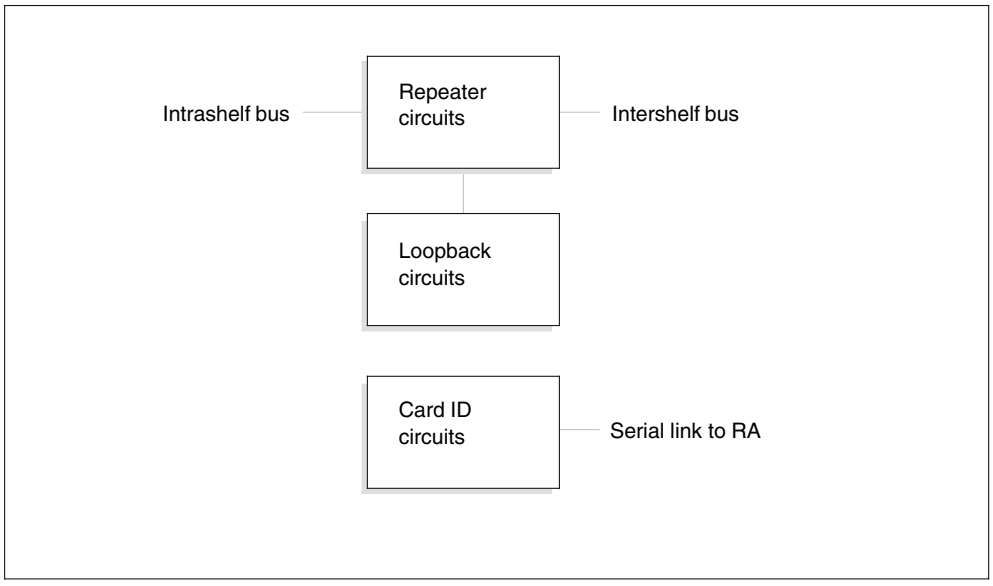
- NT9X74
- NT9X79
- NT9X30
- NTEX20

The card ID circuits use a microcontroller to communicates with the RA over a serial link.

## **NT9X74DA** (continued)

The relationship between the functional blocks appears in the following figure.

**NT9X74DA functional blocks**



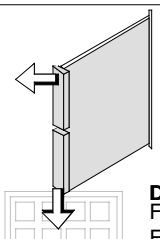

# Signaling

## Pin numbers

The pin numbers for the NT9X74DA at card locations 07 and 32 appear in the following figure.

# **NT9X74DA** (continued)

**NT9X74DA pin numbers for location 7 (Part 1 of 2)**

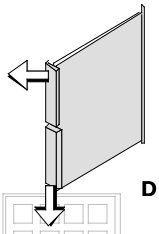


**Legend:** FB=5TM = FB=5TERM

| | D | C | B | A |
|---|---|---|---|---|
| 1 | FBWAITX- | FAWAITX- | FAA- | GND |
| 2 | FBCLRX- | FACLRX- | FAAD1 | GND |
| 3 | FBREQX- | FAREQX- | FAAD2 | GND |
| 4 | FBPOLLX- | FAPOLLX- | FAAD3 | GND |
| 5 | FBRSTX- | FARSTX- | FAAD4 | GND |
| 6 | FBPACKX- | FAPACKX- | FAAD5 | GND |
| 7 | GND | GND | FAAD6 | GND |
| 8 | FBADRENX- | FADDRENX- | FADD7 | GND |
| 9 | FBDATENX- | FADATENX- | FAPAR | GND |
| 10 | FBEOSX- | FAEOSX- | GND | GND |
| 11 | FBRACKX- | FARACKX- | FBA- | GND |
| 12 | FBRRDYX- | FARRDYX- | FBAD1 | GND |
| 13 | FBSRCENX- | FASRCENX- | FBAD2 | FCLK+ |
| 14 | FBDSTENX- | FADSTENX- | FBAD3 | FCLKX- |
| 15 | GND | GND | FBAD4 | FA-+ |
| 16 | GND | GND | FBAD5 | FA-X- |
| 17 | | | FBAD6 | FAD+ |
| 18 | | | FBAD7 | FAD1X- |
| 19 | | | FBPAR | FAD2+ |
| 20 | GND | | GND | FAD2X- |
| 21 | GND | | CLK8A | FAD3+ |
| 22 | | | CLK56A | FAD3X- |
| 23 | | | | FAD4+ |
| 24 | | | | FAD4X- |
| 25 | | | | FAD5+ |
| 26 | | | | FAD5X- |
| 27 | GND | | | FAD3X-<br>FAD6+ |
| 28 | | GND | FB+5TM | FAD6X- |
| 29 | | | FB+5TM | HW4 |
| 30 | | | FB+5TM | GND |
| 31 | | | FB+5TM | FACLK |
| 32 | | GND | | SH0 |
| 33 | | | | SH1 |
| 34 | | | | GND |
| 35 | | | | FBCLK |
| 36 | | | HW0 | |
| 37 | | | HW1 | |
| 38 | | | HW2 | |
| 39 | | | HW3 | |
| 40 | | | | GND |
| 41 | | | | GND |
| 42 | | | | GND |
| 43 | | | FB+5SEC | GND |
| 44 | | | FB+5SEC | +5V |
| 45 | | | | +5V |

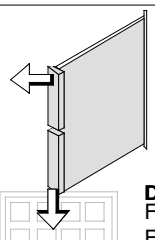
# **NT9X74DA** (continued)

### NT9X74DA pin numbers for location 7 (Part 2 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 46 | | | | +5V |
| 47 | | GND | | +5V |
| 48 | | | | +5V |
| 49 | | | | +5V |
| 50 | | | GND | +5V |
| 51 | | | | +5V |
| 52 | | | | +5V |
| 53 | | | GND | +5V |
| 54 | | | C0TFPN | +5V |
| 55 | | | C0TCLK | +5V |
| 56 | | | GND | |
| 57 | | | C0CBIDRN | |
| 58 | | | C0CBILPN | |
| 59 | | | C0T-N | |
| 60 | | | COTD1N | |
| 61 | | | COTD2N | |
| 62 | | | COTD3N | |
| 63 | | | COTD4N | |
| 64 | | | COTD5N | |
| 65 | | | COTD6N | |
| 66 | GND | | COTD7N | |
| 67 | | | C0TACTN | |
| 68 | | | C0TPAR | |
| 69 | C0CBIDSN | GND | C0R-N | |
| 70 | C0 SPARE | CSCFT | C0RD1N | |
| 71 | IDTX+ | CLK8A | C0RD2N | |
| 72 | IDTXX- | CLK56A | C0RD3N | |
| 73 | IDRX+ | | C0RD4N | |
| 74 | IDRXX- | | C0RD5N | |
| 75 | - | FPOLL+ | C0RD6N | |
| 76 | D2 | FPOLLX- | C0RD7N | |
| 77 | D4 | FREQ+ | C0RINDN | |
| 78 | D6 | FREQX- | C0RPAR | |
| 79 | CS5X- | FPACK+ | FAD7+ | GND |
| 80 | A2 | FPACKX- | FAD7X- | GND |
| 81 | A0 | FRRDY+ | FPAR+ | GND |
| 82 | | FRRDYX- | FPARX- | GND |
| 83 | PLOCK | FRACK+ | FADREN+ | GND |
| 84 | D7 | FRACKX- | FADRENX- | GND |
| 85 | A1 | FWAIT+ | FDAEN+ | GND |
| 86 | A3 | FWAITX- | FDAENX- | GND |
| 87 | CS5+ | FCLR+ | FEOS+ | GND |
| 88 | D5 | FCLRX- | FEOSX- | GND |
| 89 | D3 | | FRST+ | GND |
| 90 | D1 | CS79 | FRSTX- | GND |

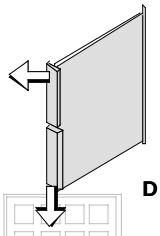
**NT9X74DA pin numbers for location 32 (Part 1 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 1 | FAWAITX- | FBWAITX- | FBA- | GND |
| 2 | FACLRX- | FBCLRX- | FBAD1 | GND |
| 3 | FAREQX- | FBREQX- | FBAD2 | GND |
| 4 | FAPOLLX- | FBPOLLX- | FBAD3 | GND |
| 5 | FARSTX- | FBRSTX- | FBAD4 | GND |
| 6 | FAPACKX- | FBPACKX- | FBAD5 | GND |
| 7 | GND | GND | FBAD6 | GND |
| 8 | FAADRENX- | FBDDRENX- | FBDD7 | GND |
| 9 | FADATENX- | FBDATENX- | FBPAR | GND |
| 10 | FAEOSX- | FBEOSX- | GND | GND |
| 11 | FARACKX- | FBRACKX- | FAA- | GND |
| 12 | FARRDYX- | FBRRDYX- | FAAD1 | GND |
| 13 | FASRCENX- | FBSRCENX- | FAAD2 | FCLK+ |
| 14 | FADSTENX- | FBDSTENX- | FAAD3 | FCLKX- |
| 15 | GND | GND | FAAD4 | FA-+ |
| 16 | GND | GND | FAAD5 | FA-X- |
| 17 | | | FAAD6 | FAD+ |
| 18 | | | FAAD7 | FAD1X- |
| 19 | | | FAPAR | FAD2+ |
| 20 | GND | | GND | FAD2X- |
| 21 | GND | | CLK8A | FAD3+ |
| 22 | | | CLK56A | FAD3X- |
| 23 | | | | FAD4+ |
| 24 | | | | FAD4X- |
| 25 | | | | FAD5+ |
| 26 | | | | FAD5X- |
| 27 | GND | | | FAD3X- |
| 28 | | GND | FB+5TM | FAD6+ |
| 29 | | | FB+5TM | FAD6X- |
| 30 | | | FB+5TM | HW4 |
| 31 | | | FB+5TM | GND |
| 32 | | GND | | FACLK |
| 33 | | | | SH0 |
| 34 | | | | SH1 |
| 35 | | | | GND |
| 36 | | | HW0 | FBCLK |
| 37 | | | HW1 | |
| 38 | | | HW2 | |
| 39 | | | HW3 | |
| 40 | | | | GND |
| 41 | | | | GND |
| 42 | | | | GND |
| 43 | | | FB+5SEC | GND |
| 44 | | | FB+5SEC | +5V |
| 45 | | | | +5V |

# **NT9X74DA** (end)

### NT9X74DA pin numbers for location 32 (Part 2 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 46 | | | | +5V |
| 47 | | GND | | +5V |
| 48 | | | | +5V |
| 49 | | | | +5V |
| 50 | | | GND | +5V |
| 51 | | | | +5V |
| 52 | | | | +5V |
| 53 | | | GND | +5V |
| 54 | | | C1TFPN | +5V |
| 55 | | | C1TCLK | +5V |
| 56 | | | GND | |
| 57 | | | C1CBIDRN | |
| 58 | | | C1CBILPN | |
| 59 | | | C1T-N | |
| 60 | | | C1TD1N | |
| 61 | | | C1TD2N | |
| 62 | | | C1TD3N | |
| 63 | | | C1TD4N | |
| 64 | | | C1TD5N | |
| 65 | | | C1TD6N | |
| 66 | GND | | C1TD7N | |
| 67 | | | C1TACTN | |
| 68 | | | C1TPAR | |
| 69 | C1CBIDSN | GND | C1R-N | |
| 70 | C1 SPARE | CSCFT | C1RD1N | |
| 71 | IDTX+ | CLK8A | C1RD2N | |
| 72 | IDTXX- | CLK56A | C1RD3N | |
| 73 | IDRX+ | | C1RD4N | |
| 74 | IDRXX- | | C1RD5N | |
| 75 | - | FPOLL+ | C1RD6N | |
| 76 | D2 | FPOLLX- | C1RD7N | |
| 77 | D4 | FREQ+ | C1RINDN | |
| 78 | D6 | FREQX- | C1RPAR | |
| 79 | CS5X- | FPACK+ | FAD7+ | GND |
| 80 | A2 | FPACKX- | FAD7X- | GND |
| 81 | A0 | FRRDY+ | FPAR+ | GND |
| 82 | | FRRDYX- | FPARX- | GND |
| 83 | PLOCK | FRACK+ | FADREN+ | GND |
| 84 | D7 | FRACKX- | FADRENX- | GND |
| 85 | A1 | FWAIT+ | FDAEN+ | GND |
| 86 | A3 | FWAITX- | FDAENX- | GND |
| 87 | CS5+ | FCLR+ | FEOS+ | GND |
| 88 | D5 | FCLRX- | FEOSX- | GND |
| 89 | D3 | | FRST+ | GND |
| 90 | D1 | CS79 | FRSTX- | GND |

# NT9X75AA

## Product description

The NT9X75AA is a processor bus (P-bus) to frame transport bus (F-bus) interface (PFI) card. This card is a part of the signal transfer point (STP) link interface unit (LIU7). The NT9X75AA card provides an interface between a P-bus and the two instances of the F-bus. The two instances of the F-bus are F-bus A and F-bus B.

The system duplicates the F-bus interfaces, which are fully independent. This condition allows the P-bus to access one of the F-bus interfaces. This action continues when other F-bus or the hardware associated with the other F-bus do not operate. The card provides a path to allow the F-bus master to reset an LIU7. The F-bus master is the rate adaptor (RA).

## Functional description

The PFI consists of a P-bus interface and duplicated F-bus interfaces. Each F-bus interface has a transmit block and a receive block. The P-bus interface provides access from the P-bus to the two F-bus interfaces. The P-bus provides two different sets of ports. Each set associates with one of the F-bus interfaces. The PFI appears in the P-bus as a 16-bit slave.

### Functional blocks

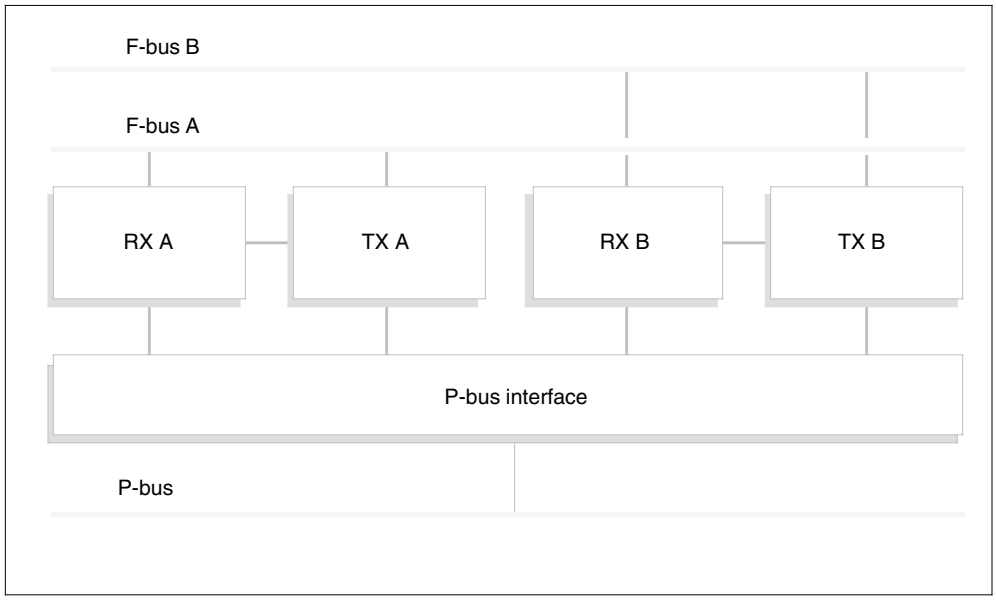
The NT9X75AA has the following functional blocks:

- F-bus transmit blocks A and B
- F-bus transmit block B
- F-bus receive block A and B
- F-bus receive block B
- P-bus interface

The functional relationship between the blocks appears in the following figure.

## **NT9X75AA** (continued)

**NT9X75AA functional blocks**




### Transmit blocks

Transmit blocks A and B relate to logic functions that send messages to the F-bus. Transmit blocks contain the following elements:

- buffer space
- buffer space protection logic, which protects with parity the data stored in the first-in first-out (FIFO) queue
- bus request logic, which generates a request for the use of the F-bus
- poll monitor logic, which allows an LIU7 to use the F-bus
- cyclic redundancy check (CRC) generator/checker, which acts as a CRC generator for the transmit block. The check acts as a CRC checker for the receive block. This check computes the CRC over the data as the data read occurs from the FIFO.
- transmit finite state machine. This machine controls the FIFO read and drive of data, CRC, parity. This machine controls F-bus control signals after the system grants the F-bus.
- bus monitor/error logger logic, which monitors F-bus and internal signals from the time the F-bus request occurs until the end of transmission

### Receive blocks

The receive blocks include logic functions that receive messages from the F-bus. The F-bus reset logic and grant logic are in the receive block. The grant

logic is in the receive block even while the grant logic function normally belongs to the transmit block.

The receive blocks contain the following elements:

- buffer space
- buffer space protection logic protects the data in the FIFO with an 8-bit CRC code (CRC8)
- CRC generator/checker is in the transmit block and shared with the receive block
- receive finite state machine controls data writing from the F-bus to the receive FIFO, CRC and CRC8 calculation. This machine drives F-bus response signals RACK and PACK. This machine also routes receive message status register contents and calculates CRC8 to the FIFO.
- receive message status register. The register constructs a message-by-message record of errors. The system routes the register to the receive FIFO after the last byte of the message.
- F-bus command logic, which monitors the F-bus control lines ADEN, POLL, and RESET

### P-bus interface

The PFI appears as a 16-bit P-bus slave on the P-bus. The P-bus interface generates parity. Parity is an optional feature of the P-bus. The P-bus signal DAS32- derives the timing of the P-bus interface through the delay lines. The design provides a high degree of immunity against noise glitches in the P-bus signals.

### Data flow control

Data travel between the PFI and the P-bus occurs through transceivers. The system enables the transceivers when the system addresses card and signal and asserts the CARD-. The latched version of P-bus signal WRT- completes the direction control.

### Interrupt logic

The system generates interrupts in the receive and transmit blocks. Similar interrupts from the A and B side are ORed together. The system can mask interrupts on each F-bus basis with the use of the control port.

### Reset logic

Reset logic meets the timing requirements to reset the FIFOs. Resets are classified into global reset and selective resets. Power up and P-bus Signal RSTOUT- causes global resets. The voltage monitor initiates the global reset.

## **NT9X75AA** (continued)

Selective resets require that the important enable bit in the control register be set.

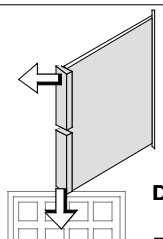
# Signaling

### Pin numbers

The pin numbers for NT9X75AA. appear in the following figures.

# **NT9X75AA** (continued)

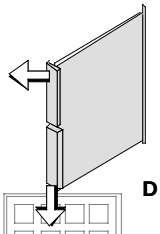
### NT9X75AA pin numbers (Part 1 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | FAAD0 | Gnd |
| 2 | FBCLR– | FACLR– | FAAD1 | Gnd |
| 3 | FBREQ– | FAREQ– | FAAD2 | Gnd |
| 4 | FBPOLL– | FAPOLL– | FAAD3 | Gnd |
| 5 | FBRST– | FARST– | FAAD4 | Gnd |
| 6 | FBPACK– | FAPACK– | FAAD5 | Gnd |
| 7 | Gnd | Gnd | FAAD6 | Gnd |
| 8 | FBADREN– | FAADREN– | FADD7 | Gnd |
| 9 | FBDATEN– | FADATEN– | FAPAR | Gnd |
| 10 | FBEOS– | FAEOS– | Gnd | Gnd |
| 11 | FBRACK– | FARACK– | FBAD0 | Gnd |
| 12 | FBRRDY– | FARRDY– | FBAD1 | Gnd |
| 13 | FBSCREN– | FASRCEN– | FBAD2 | RXNON0A |
| 14 | FBDSTEN– | FADSTEN– | FBAD3 | RXMONIA |
| 15 | Gnd | Gnd | FBAD4 | RXMON2A |
| 16 | Gnd | Gnd | FBAD5 | RXMON3A |
| 17 | PERINT6– | BUSGRI– | FBAD6 | TXMSB0A |
| 18 | | BUSGRO– | FBAD7 | TXFFRA– |
| 19 | | | FBPAR | TXCRCA– |
| 20 | Gnd | PERINT3– | Gnd | TXCRC1A |
| 21 | Gnd | | | TXCRC2A– |
| 22 | | PERINT5– | | TXINTA– |
| 23 | RSTOUT– | | | |
| 24 | | | | |
| 25 | BEN1– | BEN0– | | |
| 26 | BEN3– | BEN2– | | |
| 27 | Gnd | | | |
| 28 | WRT– | Gnd | | |
| 29 | | DTACK– | | HW4 |
| 30 | PARITY– | | | Gnd |
| 31 | PRTYEN– | | | FACLK |
| 32 | | Gnd | | SH0 |
| 33 | DAS32– | | | SH1 |
| 34 | | | | Gnd |
| 35 | | | | FBCLK |
| 36 | | ADDR02 | HW0 | |
| 37 | | ADDR03 | HW1 | |
| 38 | | ADDR04 | HW2 | |
| 39 | | ADDR05 | HW3 | |
| 40 | | ADDR06 | | Gnd |
| 41 | | ADDR07 | | Gnd |
| 42 | | ADDR08 | | Gnd |
| 43 | | ADDR09 | | Gnd |
| 44 | | ADDR10 | PBRST– | +5V |
| 45 | | ADDR11 | | +5V |

# **NT9X75AA** (continued)

### NT9X75AA pin numbers (Part 2 of 2)



| | D | C | B | | A |
|---|---|---|---|---|---|
| 46 | | ADDR12 | | +5V | |
| 47 | | ADDR13 | Gnd | +5V | |
| 48 | | ADDR14 | | +5V | |
| 49 | | ADDR15 | | +5V | |
| 50 | DATA16 | ADDR16 | Gnd | +5V | |
| 51 | DATA17 | ADDR17 | | +5V | |
| 52 | DATA18 | ADDR18 | | +5V | |
| 53 | DATA19 | ADDR19 | Gnd | +5V | |
| 54 | DATA20 | ADDR20 | | +5V | |
| 55 | DATA21 | ADDR21 | | +5V | |
| 56 | DATA22 | ADDR22 | Gnd | | |
| 57 | DATA23 | ADDR23 | | | |
| 58 | DATA24 | ADDR24 | | | |
| 59 | DATA25 | ADDR25 | | | |
| 60 | DATA26 | ADDR26 | | | |
| 61 | DATA27 | ADDR27 | | | |
| 62 | DATA28 | ADDR28 | | | |
| 63 | DATA29 | ADDR29 | | | |
| 64 | DATA30 | ADDR30 | | | |
| 65 | DATA31 | ADDR31 | | | |
| 66 | Gnd | | | | |
| 67 | | | | | |
| 68 | | | | | |
| 69 | | Gnd | | | |
| 70 | | | | | |
| 71 | | | | | |
| 72 | | | | | |
| 73 | | | | | |
| 74 | | | | | |
| 75 | | | | | |
| 76 | | | | | |
| 77 | | | | | |
| 78 | | | | | |
| 79 | | | RXMON0B | Gnd | |
| 80 | | | RXMON1B | Gnd | |
| 81 | | | RXMON2B | Gnd | |
| 82 | | | RXMON3B | Gnd | |
| 83 | | | TXMSB0B | Gnd | |
| 84 | | | TXFFRB– | Gnd | |
| 85 | | | TXCRCB– | Gnd | |
| 86 | | | TXCRC1B– | Gnd | |
| 87 | | | TXCRC2B– | Gnd | |
| 88 | | | TXINTB– | Gnd | |
| 89 | | | | | |
| 90 | | | | | |

# Technical data

## Power requirements

The normal power requirements for the NT9X75AA are 6.5 A from a +5V supply, with a maximum of 10 A.

# NT9X76AA

## Product description

The signaling transfer point (STP) connects to each CCS7 link through an NT9X76AA signaling terminal (ST) card. This card is a single board with two processors that handle the data link level functions of the CCS7 protocol. The link general processor (LGP) performs higher level servicing. The LGP is an external processor. The LGP communicates with the ST through a two-ported RAM accessible through the processor bus (P-bus).

## Functional description

The ST sends and receives messages to and from an associated link paddle board (PB). The two processors move the data. The two processors perform the data link level functions of the CCS7 protocol.

Incoming data passes through the PB from a link. The PB performs the electrical conversion. This conversion passes the data to the serial communications controller (SCC) of the ST. The SCC handles the following functions:

- converts serial/parallel data
- detects flags
- generates and checks CRC
- inserts and deletes zero bits

The data link processor (DLP) services the SCC. The DLP sends the data through the DLP/master processor (MP) first-in first-out (FIFO) device to the MP. The MP can pass the data to the LGP through the MP/LGP interface RAM. Data that goes to the link flows in the opposite direction. This DLP services the SCC. The DLP sends the data through the DLP/master processor (MP) first-in first-out (FIFO) device to the MP. The MP can pass the data to the LGP through the MP/LGP interface RAM. Data that goes to the link flows in the opposite direction. Data passes through the MP/DLP interface RAM, and does not pass through the FIFO.

### Functional blocks

The NT9X76AA has the following functional blocks:

- P-bus interface
- LGP/MP interface RAM
- MP
- MP/DLP interface RAM
- DLP

## NT9X76AA (continued)

- SCC
- test card

### Processor bus interface

The NT9X76AA has an 8-bit slave-only P-bus interface that returns the parity. The interface decodes three separate address spaces. The three address spaces follow:

- the interface port address space
- the dual-port memory address space (for the MP/LGP interface RAM)
- the PB port address space

### Link general processor/master processor interface RAM

The LGP/MP interface RAM is a 64 Kbyte array composed of two 32 Kbyte × 8 bit static RAM chips. The system switches access to the memory by a bank of 74ALS257 quad two-to-one multiplexers. The EXTG- controls these multiplexers. The multiplexers select the correct source of address bits. The multiplexers select read/write and chip select strobes. During a P-bus access, the system takes 16 bits of address directly from the P-bus. During MP access, the address forms when 13 bits of MP address merge with three bits of the page register occurs.

### Master processor

The MP is designed around an 8085 processor. A 63S841 1Kbyte × 4-bit PROM decodes the top 8 bits of the 16-bit address bus. This action occurs in the MP system, and provides active-low strobes for the following:

- the MP static RAM
- the MP input/output (IO) space
- the MP/DLP interface memory
- the MP/EXT interface memory

The system uses 4.915 MHz MP system clock as the clock for the 8530 SCC. Each MP cycle can incur wait states based on the address of the device. The MP watchdog timer checks the sanity of the processor. A 74HC4040 12-stage ripple counter implements this check. The MP has access to three Intel 82C54 programmable interval timers. Each timer has three channels, for a total of nine timers.

The center of the MP reset is a TL7705 supply voltage supervisor. The supervisor monitors the 5V supply and generates a reset pulse after power-up and after any transients below 4.6V.

### MP/DLP interface RAM

The 4Kbyte × 8-bit MP/DLP interface RAM is an array of two 1423-35 4Kx4 static RAMs. A bank of 74ALS257 quad two-to-one multiplexers switches the address bus of the RAMs. A 74F257 quad two-to-one multiplexer switches the chip select and writes enable signals.

### Data link processor

A 74F139 two-to-four decoder decodes the top three bits of the 16-bit address bus. This action occurs in the DLP system. The 74F139 decodes the bits to provide four active-low strobes for the following:

- the EPROM
- the SCC
- the MP/DLP interface memory
- the test card interface

The system uses a high level on address bit 15 to enable the DLP/MP FIFO. The DLP system uses a single 12.000 MHz clock. The processor does not support wait states. The SCC, with a 4.915 MHz clock, has a 1.35 ms recovery time after each access. The DLP has two hardware interrupt lines. The two hardware interrupt lines are not in use.

### Serial communications controller

The 8530 SCC is a dual-channel device. Channel A receives communications. Channel B transmits communications. This process makes the receiver and transmitter seaparate. In addition to the normal mode of operation, three types of loopback are supported. These loopbacks are: ST loopback, PB loopback and line loopback. In all modes of operation, the SCC requires a clock from the PB.

### Test card

The test card contains two common synchronous asynchronous receiver transmitters (USART) and the RS232 interfaces. These elements provide terminal and host computer access to the MP or DLP firmware. Connections occur through two 16-pin sockets. Add a test card strap to the ST card when the test card is present.

There is a bank of 8 DIP switches with the Test Card to control baud rates and terminal breaks. Details on setting these switches may be found in the tables below. The baud rates for the two ports, as determined by the switches, are independently selected by two 74ALS151 eight-to-one multiplexers (U106

## **NT9X76AA** (continued)

and U111). Note that for firmware performance reasons, the baud rates should be set to 9600 or 19200 baud if the Test Card is not used.

**DIP switch functions for switches 1-6**

| TERMINAL<br>HOST | 1<br>4 | 2<br>5 | 3<br>6 | RATE |
|---|---|---|---|---|
| | ON | ON | ON | 19200 |
| | ON | ON | OFF | 9600 |
| | ON | OFF | OFF | 4800 |
| | ON | ON | OFF | 2400 |
| | OFF | ON | ON | 1200 |
| | OFF | ON | OFF | 600 |
| | OFF | OFF | ON | 300 |
| | OFF | OFF | OFF | 0 |

**DIP switch functions for switches 7 and 8**

| SWITCH | FUNCTION |
|---|---|
| SWITCH 7 | UNUSED |
| SWITCH 8 ON | TERMINAL BREAK RESETS ST |
| SWITCH 8 OFF | TERMINAL BREAK HAS NO EFFECT |

The terminal port is configured as a DCE device. Since the 8251 USART is designed for DTE use, the link DTR and DSR circuits are connected to DSR and DTR, respectively, on the 8251. The link DTR line is pulled up so as to be asserted if the terminal does not drive it. Note that no support is offered for RTS/CTS handshaking (also because the 8251 is designed for DTEs). The CTS line may simply be tied to DSR to accomodate terminals needing a CTS signal. Note that with most terminals, only circuits BA (TxD), BB (RxD), and

AB (GND) need be connected to EIA pins 2, 3, and 7, respectively. The table below shows the signals used in each port.

**RS-232C signals used in Test Card ports**

| DIP16 PIN | TERM PORT U131 | HOST PORT U138 | EIA PIN |
|---|---|---|---|
| 1, 9 | AB (GND) | AB (GND) | 7 |
| 2, 10 | CC (DSR) (see note below) | CB (CTS) | 5 |
| 3, 11 | CC (DSR) | CC (DSR) | 6 |
| 4, 12 | BB (RXD) | BB (RXD) | 3 |
| 5, 13 | AB (GND) | AB (GND) | 7 |
| 6, 14 | BA (TXD) | BA (TXD) | 2 |
| 7, 15 | CD (DTR) | CD (DTR) | 20 |
| 8, 16 | --NC-- | CA (RTS) | 4 |

***Note:*** Connect DSR to EIA pin 5 to emulate CTS and to EIA pin 8 to emulate RLSD.

## Technical data

### Power requirements

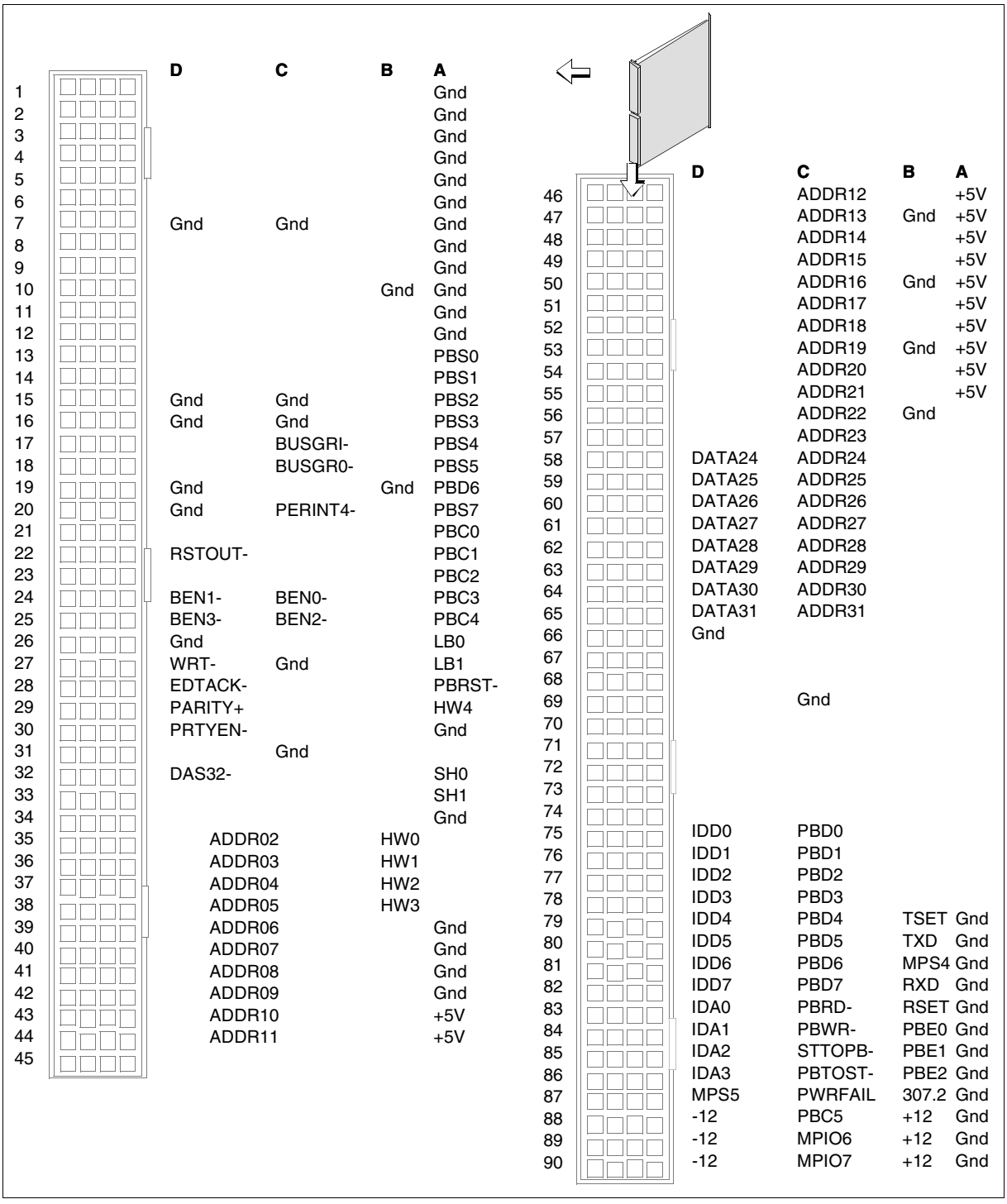
The power use of the NT9X76AA is 19W standard, and 37W maximum.

## Signaling

### Pin numbers

The pin numbers for NT9X76AA appear in the following figure.

### NT9X76AA pin numbers



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | Gnd |
| 2 | | | | Gnd |
| 3 | | | | Gnd |
| 4 | | | | Gnd |
| 5 | | | | Gnd |
| 6 | | | | Gnd |
| 7 | Gnd | Gnd | | Gnd |
| 8 | | | | Gnd |
| 9 | | | | Gnd |
| 10 | | | Gnd | Gnd |
| 11 | | | | Gnd |
| 12 | | | | Gnd |
| 13 | | | | PBS0 |
| 14 | | | | PBS1 |
| 15 | Gnd | Gnd | | PBS2 |
| 16 | Gnd | Gnd | | PBS3 |
| 17 | | BUSGRI- | | PBS4 |
| 18 | | BUSGR0- | | PBS5 |
| 19 | Gnd | | Gnd | PBD6 |
| 20 | Gnd | PERINT4- | | PBS7 |
| 21 | | | | PBC0 |
| 22 | RSTOUT- | | | PBC1 |
| 23 | | | | PBC2 |
| 24 | BEN1- | BEN0- | | PBC3 |
| 25 | BEN3- | BEN2- | | PBC4 |
| 26 | Gnd | | | LB0 |
| 27 | WRT- | Gnd | | LB1 |
| 28 | EDTACK- | | | PBRST- |
| 29 | PARITY+ | | | HW4 |
| 30 | PRTYEN- | | | Gnd |
| 31 | | Gnd | | |
| 32 | DAS32- | | | SH0 |
| 33 | | | | SH1 |
| 34 | | | | Gnd |
| 35 | ADDR02 | | HW0 | |
| 36 | ADDR03 | | HW1 | |
| 37 | ADDR04 | | HW2 | |
| 38 | ADDR05 | | HW3 | |
| 39 | ADDR06 | | | Gnd |
| 40 | ADDR07 | | | Gnd |
| 41 | ADDR08 | | | Gnd |
| 42 | ADDR09 | | | Gnd |
| 43 | ADDR10 | | | +5V |
| 44 | ADDR11 | | | +5V |
| 45 | | | | |

| | D | C | B | A |
|---|---|---|---|---|
| 46 | | ADDR12 | | +5V |
| 47 | | ADDR13 | Gnd | +5V |
| 48 | | ADDR14 | | +5V |
| 49 | | ADDR15 | | +5V |
| 50 | | ADDR16 | Gnd | +5V |
| 51 | | ADDR17 | | +5V |
| 52 | | ADDR18 | | +5V |
| 53 | | ADDR19 | Gnd | +5V |
| 54 | | ADDR20 | | +5V |
| 55 | | ADDR21 | | +5V |
| 56 | | ADDR22 | Gnd | |
| 57 | | ADDR23 | | |
| 58 | DATA24 | ADDR24 | | |
| 59 | DATA25 | ADDR25 | | |
| 60 | DATA26 | ADDR26 | | |
| 61 | DATA27 | ADDR27 | | |
| 62 | DATA28 | ADDR28 | | |
| 63 | DATA29 | ADDR29 | | |
| 64 | DATA30 | ADDR30 | | |
| 65 | DATA31 | ADDR31 | | |
| 66 | Gnd | | | |
| 67 | | | | |
| 68 | | | | |
| 69 | | Gnd | | |
| 70 | | | | |
| 71 | | | | |
| 72 | | | | |
| 73 | | | | |
| 74 | | | | |
| 75 | IDD0 | PBD0 | | |
| 76 | IDD1 | PBD1 | | |
| 77 | IDD2 | PBD2 | | |
| 78 | IDD3 | PBD3 | | |
| 79 | IDD4 | PBD4 | TSET | Gnd |
| 80 | IDD5 | PBD5 | TXD | Gnd |
| 81 | IDD6 | PBD6 | MPS4 | Gnd |
| 82 | IDD7 | PBD7 | RXD | Gnd |
| 83 | IDA0 | PBRD- | RSET | Gnd |
| 84 | IDA1 | PBWR- | PBE0 | Gnd |
| 85 | IDA2 | STTOPB- | PBE1 | Gnd |
| 86 | IDA3 | PBTOST- | PBE2 | Gnd |
| 87 | MPS5 | PWRFAIL | 307.2 | Gnd |
| 88 | -12 | PBC5 | +12 | Gnd |
| 89 | -12 | MPIO6 | +12 | Gnd |
| 90 | -12 | MPIO7 | +12 | Gnd |

# NT9X76BA

## Product description

The signaling transfer point (STP) connects to each Common Channel Signaling 7 (CCS7) link through an NT9X76BA signaling terminal (ST) card. The NT9X76BA is a single card with two processors that handles the data link level functions of the CCS7 protocol. The link general processor (LGP) performs higher level service. The LGP is an external processor that communicates with the ST through a dual–port RAM. Access is available through the processor bus (P–bus).

The NT9X76BA is backwards compatible.

### Location

The NT9X76BA fits into slots 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, and 29. These slots are in the NT9X72AA link interface shelf (LIS).

## Functional description

The NT9X76BA transmits messages to and from an associated link paddle board (PB). The two processors transmit the data, and perform the data link level functions of the CCS7 protocol. Data that comes from a link passes through the PB enroute to the ST serial communications controller (SCC). The SCC handles the following:

- serial–to–parallel data conversion
- flag detection
- cyclic redundancy check (CRC) generation
- zero bit insertion and deletion

The data link processor (DLP) services the SCC. The DLP sends the data through the DLP master processor (MP) first in, first out (FIFO) device to the MP. The MP passes the data to the LGP through the MP–LGP interface RAM. Data that goes to the link moves in the opposite direction. This data passes through the DLP-MP interface RAM instead of the FIFO.

### Functional blocks

The NT9X76BA has the following functional blocks:

- P–bus interface
- MP
- DLP
- DLP-MP interface RAM
- MP-LGP interface RAM

## **NT9X76BA** (continued)

- SCC
- test card

### Processor bus interface

The NT9X76BA has an 8–bit slave–only P–bus interface that returns parity. The interface decodes three address spaces:

- the interface port address space
- the PB port address space
- the dual–port memory address space (for the MP–LGP interface RAM)

### Master processor

The MP includes an 8085 processor. In the MP system, a 63S841 1 kbyte by 4–bit PROM decodes the top 8 bits of the 16–bit address bus.

This decoding provides active–low strobes for the following:

- MP static RAM
- MP input and output (IO) space
- DLP-MP interface memory
- MP-EXT interface memory

The 4.915 MHz MP clock system is the clock for the 8530 SCC. Wait states can occur in MP cycles. The occurrence of wait states depends on the device that the MP cycle addresses. The 74HC4040 12–stage ripple counter implements the MP watchdog timer to check the processor sanity. The MP has access to three Intel 82C54 programmable interval timers each with three channels for a total of nine timers.

The central feature of the MP reset is a TL7705 supply voltage supervisor. The TL7705 supply voltage supervisor monitors the 5V supply. The TL7705 supply voltage supervisor generates a reset pulse. The supervisor generates the reset pulse after you turn the power on, and after any transient power supply changes below 4.6V.

### Data link processor

In the DLP system, a 74F139 two–to–four decoder decodes the top 3 bits of the 16–bit address bus.

The signal that the decoder decodes provides active–low strobes for the following:

- EPROM
- SCC
- DLP-MP interface memory
- test card interface

The DLP system uses a single 12 MHz clock. The processor does not support wait states. The SCC, with a 4.915 MHz clock, has a 1.35 µs recovery time after every access. The DLP has two hardware interrupt lines. The system does not use the two hardware interrupt lines.

### Master processor-link general processor interface RAM

The MP-LGP interface RAM is a 64–kbyte array that consists of two 32–Kbyte by 8–bit static RAM chips. A bank of 74ALS257 quad two–to–one multiplexers switches access to the memory. The multiplexers select the appropriate source of address bits, and read–write and chip–select strobes. When the multiplexers access the P–bus, the multiplexers take the 16 bits of address from the P–bus. When the multiplexers access an MP, 13 bits of the MP address merge with three bits of the page register. This process forms the address.

### Data link processor-master processor interface RAM

The 4–kbyte by 8–bit DLP–MP interface RAM is an array of two 1423–35 4–Kbyte by 4–bit static RAMs. A bank of 74ALS257 quad two–to–one multiplexers switches the address bus of the RAM. A 74F257 quad two–to–one multiplexer switches the chip–select and write–enable signals.

### Serial communications controller

The 8530 SCC is a dual–channel device in which channel A receives and channel B transmits. The receiver and transmitter are separate. The SCC requires a clock from the PB in all modes of operation.

The SCC also supports the following types of loopback:

- ST
- PB
- line

### Test card

The test card consists of two USARTs and the RS232 interfaces. The USARTs and interfaces provide terminal and host computer access to the MP or DLP

## **NT9X76BA** (continued)

firmware. Two 16–pin sockets allow connections. A test card strap must be added to the ST card when the test card is present. The DLP switches on the test card control baud rates and terminal breaks.

# Technical data

### Power requirements

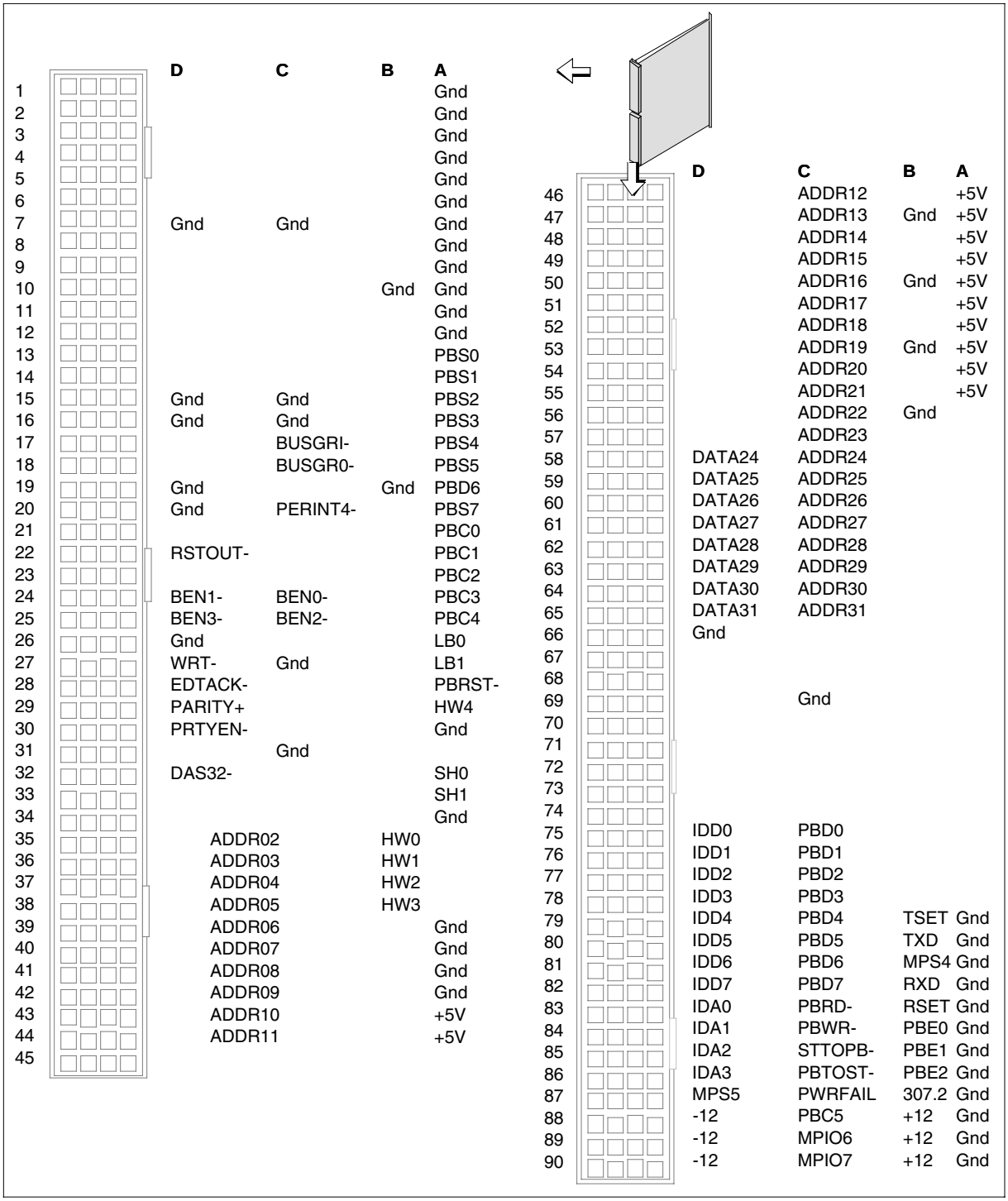
The power use of the NT9X76BA is normally 19W, and a maximum of 37W.

# Signaling

### Pin numbers

The pin numbers for NT9X76BA appear in the figure that follows.

### NT9X76BA pin numbers



| Pin | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | Gnd |
| 2 | | | | Gnd |
| 3 | | | | Gnd |
| 4 | | | | Gnd |
| 5 | | | | Gnd |
| 6 | | | | Gnd |
| 7 | Gnd | Gnd | | Gnd |
| 8 | | | | Gnd |
| 9 | | | | Gnd |
| 10 | | | Gnd | Gnd |
| 11 | | | | Gnd |
| 12 | | | | Gnd |
| 13 | | | | PBS0 |
| 14 | | | | PBS1 |
| 15 | Gnd | Gnd | | PBS2 |
| 16 | Gnd | Gnd | | PBS3 |
| 17 | | BUSGRI- | | PBS4 |
| 18 | | BUSGR0- | | PBS5 |
| 19 | Gnd | | Gnd | PBD6 |
| 20 | Gnd | PERINT4- | | PBS7 |
| 21 | | | | PBC0 |
| 22 | RSTOUT- | | | PBC1 |
| 23 | | | | PBC2 |
| 24 | BEN1- | BEN0- | | PBC3 |
| 25 | BEN3- | BEN2- | | PBC4 |
| 26 | Gnd | | | LB0 |
| 27 | WRT- | Gnd | | LB1 |
| 28 | EDTACK- | | | PBRST- |
| 29 | PARITY+ | | | HW4 |
| 30 | PRTYEN- | | | Gnd |
| 31 | | Gnd | | |
| 32 | DAS32- | | | SH0 |
| 33 | | | | SH1 |
| 34 | | | | Gnd |
| 35 | ADDR02 | | HW0 | |
| 36 | ADDR03 | | HW1 | |
| 37 | ADDR04 | | HW2 | |
| 38 | ADDR05 | | HW3 | |
| 39 | ADDR06 | | | Gnd |
| 40 | ADDR07 | | | Gnd |
| 41 | ADDR08 | | | Gnd |
| 42 | ADDR09 | | | Gnd |
| 43 | ADDR10 | | | +5V |
| 44 | ADDR11 | | | +5V |
| 45 | | | | |

| Pin | D | C | B | A |
|---|---|---|---|---|
| 46 | | ADDR12 | | +5V |
| 47 | | ADDR13 | Gnd | +5V |
| 48 | | ADDR14 | | +5V |
| 49 | | ADDR15 | | +5V |
| 50 | | ADDR16 | Gnd | +5V |
| 51 | | ADDR17 | | +5V |
| 52 | | ADDR18 | | +5V |
| 53 | | ADDR19 | Gnd | +5V |
| 54 | | ADDR20 | | +5V |
| 55 | | ADDR21 | | +5V |
| 56 | | ADDR22 | Gnd | |
| 57 | | ADDR23 | | |
| 58 | DATA24 | ADDR24 | | |
| 59 | DATA25 | ADDR25 | | |
| 60 | DATA26 | ADDR26 | | |
| 61 | DATA27 | ADDR27 | | |
| 62 | DATA28 | ADDR28 | | |
| 63 | DATA29 | ADDR29 | | |
| 64 | DATA30 | ADDR30 | | |
| 65 | DATA31 | ADDR31 | | |
| 66 | Gnd | | | |
| 67 | | | | |
| 68 | | | | |
| 69 | | Gnd | | |
| 70 | | | | |
| 71 | | | | |
| 72 | | | | |
| 73 | | | | |
| 74 | | | | |
| 75 | IDD0 | PBD0 | | |
| 76 | IDD1 | PBD1 | | |
| 77 | IDD2 | PBD2 | | |
| 78 | IDD3 | PBD3 | | |
| 79 | IDD4 | PBD4 | TSET | Gnd |
| 80 | IDD5 | PBD5 | TXD | Gnd |
| 81 | IDD6 | PBD6 | MPS4 | Gnd |
| 82 | IDD7 | PBD7 | RXD | Gnd |
| 83 | IDA0 | PBRD- | RSET | Gnd |
| 84 | IDA1 | PBWR- | PBE0 | Gnd |
| 85 | IDA2 | STTOPB- | PBE1 | Gnd |
| 86 | IDA3 | PBTOST- | PBE2 | Gnd |
| 87 | MPS5 | PWRFAIL | 307.2 | Gnd |
| 88 | -12 | PBC5 | +12 | Gnd |
| 89 | -12 | MPIO6 | +12 | Gnd |
| 90 | -12 | MPIO7 | +12 | Gnd |

## Product description

The signaling transfer point (STP) connects to each CCS7 link through an NT9X76CA signaling terminal (ST) card. The ST is a single card with two processors that handle the data link level functions of the CCS7 protocol. The data link processor (DLP) firmware of the NT9X76CA is set for a different intersignaling unit delay than the NT9X76AA. This change accommodates equipment that the Japanese market uses. The link general processor (LGP) performs higher level service. The LGP is an external processor that communicates with the ST through a two-port RAM. Access is available through the processor bus (P-bus).

### Location

Slots 9, 11, 13, 15, 17, 23, 25, 27, 29, and 31 in a channelized access link interface shelf contain the NT9X76CA. The NT9X76CA occupies slot 19 and 21 in access link interface shelves that are not channelized.

## Functional description

The ST sends and receives messages to and from an associated link paddle board (PB). Two processors exchange data and perform the data link level functions of the CCS7 protocol.

Data that comes from a link passes through the PB. The PB performs electrical conversion to send the data to the ST serial communications controller (SCC). The SCC handles serial and parallel data conversion, flag detection, CRC generation and checking, and zero bit insertion or deletion. The data link processor (DLP) services the SCC. The DLP sends the data through the DLP-master processor (MP) first in, first out (FIFO) device to the MP. The MP can send the data to the LGP through the MP-LGP interface RAM. Data that goes to the link flows in the opposite direction. This data goes through the MP-DLP interface RAM instead of the FIFO.

### Functional blocks

The NT9X76CA has the following functional blocks:

- P-bus interface
- LGP-MP interface RAM
- MP
- MP-DLP interface RAM
- DLP
- SCC
- test card

### Processor bus interface

The NT9X76CA has an 8-bit slave-only P-bus interface that returns the parity. The interface decodes the following separate address spaces:

- the interface port address space.
- dual-port memory address space (for the MP-LGP interface RAM).
- PB port address space.

### Link general processor-master processor interface RAM

The LGP-MP interface RAM is a 64 KB array that consists of two 32 KB×8-bit static RAM chips. A bank of 74ALS257 quad two-to-one multiplexers switch access to the memory. The EXTG- controls the multiplexers. The multiplexers select the appropriate source of address bits, and read/write and chip select strobes. During a P-bus access, the multiplexers take the 16 bits of address directly from the P-bus. During an MP access, 13 bits of MP address merge with 3 bits of the page register to form the address.

### Master processor

The MP is designed around an 8085 processor. In the MP system, a 63S841 1 KB×4 bit PROM decodes the top 8 bits of the 16-bit address bus. This process provides active-low strobes for the following:

- MP static RAM
- MP input/output (IO) space
- MP-DLP interface memory
- MP-EXT interface memory

The 4.915 MHz MP system clock is the clock for the 8530 SCC. Each MP cycle can incur some wait states. The occurrence of wait states depends on the device that the MP cycle addresses. The MP watchdog timer checks processor sanity. A 74HC4040 12-stage ripple counter implements the MP watchdog timer. The MP has access to three Intel 82C54 programmable interval timers. Each timer has three channels, for a total of nine timers.

The central feature of the MP reset is a TL7705 supply voltage supervisor. The supervisor monitors the 5V supply and generates a reset pulse after power-up and after any transients below 4.6V.

### MP-DLP interface RAM

The 4 KB×8-bit MP-DLP interface RAM is an array of two 1423-35 4 KB×4 static RAMs. A bank of 74ALS257 quad two-to-one multiplexers switches the address bus of the MP-DLP interface RAM. A 74F257 quad two-to-one multiplexer switches the chip select and writes enable signals.

## NT9X76CA (continued)

### Data link processor

In the DLP system, a 74F139 two-to-four decoder decodes the top 3 bits of the 16-bit address bus. This process provides four active-low strobes for the EPROM, SCC, MP-DLP interface memory, and test card interface. A high level on address bit 15 activates the DLP-MP FIFO. The DLP system uses a single 12 MHz clock. The processor does not support wait states. The SCC, with a 4.915 MHz clock, has a 1.35 ms recovery time after each access. The DLP has two hardware interrupt lines. The system does not use these two hardware lines.

### Serial communications controller

The 8530 SCC is a dual-channel device. The 8530 SCC contains channel A receives and channel B transmits. The receiver and transmitter are separate. In addition to the normal mode of operation, the serial communications controller supports three types of loopback:

- ST
- PB
- line

In all modes of operation, the SCC requires a clock from the PB.

### Test card

The test card consists of two universal synchronous asynchronous receiver transmitters (USART) and the RS232 interfaces. The USARTs and interfaces provide terminal and host computer access to the MP or DLP firmware. Two 16-pin sockets allow connections. A test card strap must be added to the ST card only when the test card is present. Dual inline package (DIP) switches on the test card control baud rates and terminal breaks.

# Technical data

### Power requirements

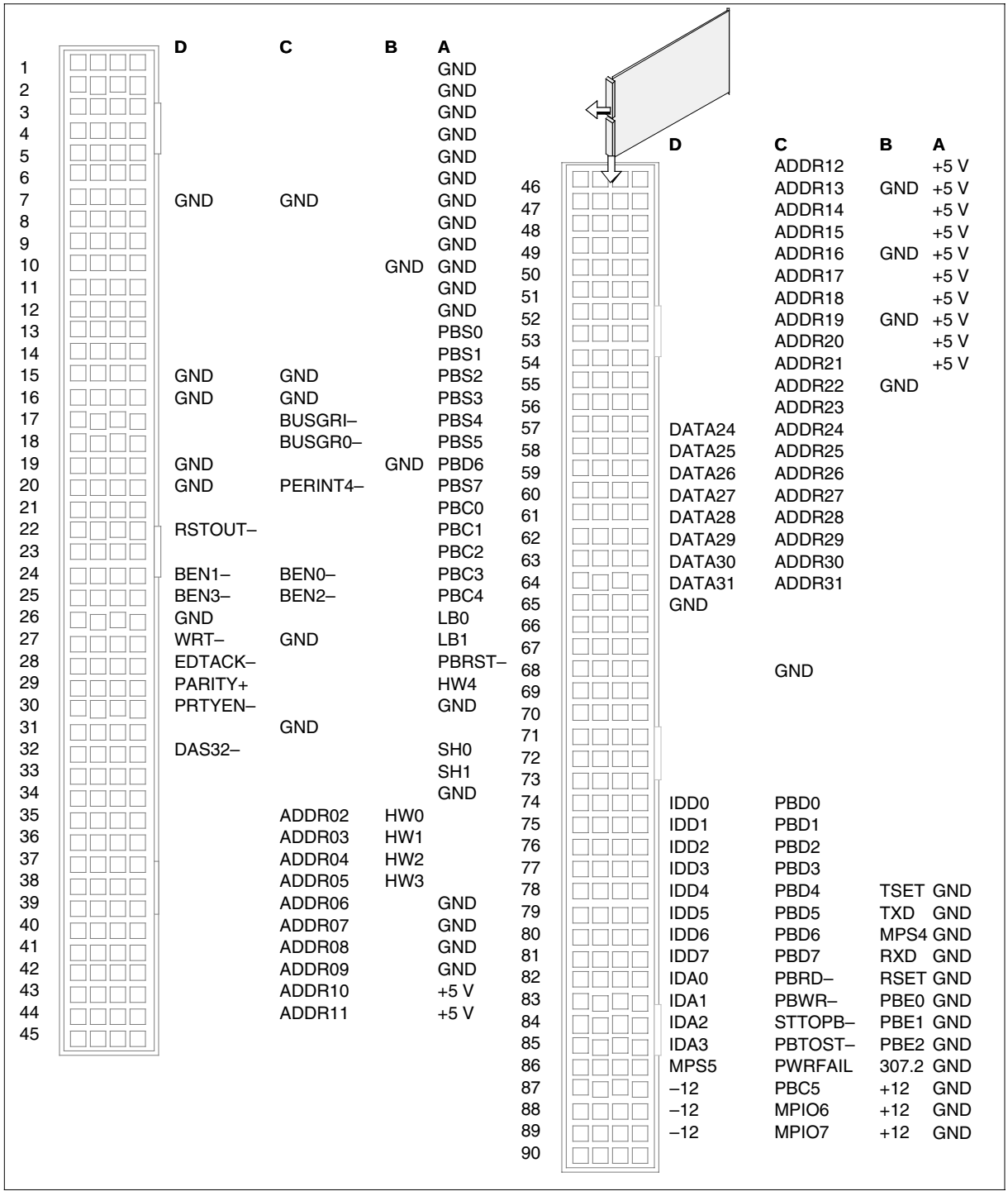
The power use of the NT9X76CA is normally 19W, and a maximum of 37W.

# Signaling

### Pin numbers

The pin numbers for the NT9X76CA appear in the figure that follows.

### NT9X76CA pin numbers



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | GND |
| 2 | | | | GND |
| 3 | | | | GND |
| 4 | | | | GND |
| 5 | | | | GND |
| 6 | | | | GND |
| 7 | GND | GND | | GND |
| 8 | | | | GND |
| 9 | | | | GND |
| 10 | | | GND | GND |
| 11 | | | | GND |
| 12 | | | | GND |
| 13 | | | | PBS0 |
| 14 | | | | PBS1 |
| 15 | GND | GND | | PBS2 |
| 16 | GND | GND | | PBS3 |
| 17 | | BUSGRI– | | PBS4 |
| 18 | | BUSGR0– | | PBS5 |
| 19 | GND | | GND | PBD6 |
| 20 | GND | PERINT4– | | PBS7 |
| 21 | | | | PBC0 |
| 22 | RSTOUT– | | | PBC1 |
| 23 | | | | PBC2 |
| 24 | BEN1– | BEN0– | | PBC3 |
| 25 | BEN3– | BEN2– | | PBC4 |
| 26 | GND | | | LB0 |
| 27 | WRT– | GND | | LB1 |
| 28 | EDTACK– | | | PBRST– |
| 29 | PARITY+ | | | HW4 |
| 30 | PRTYEN– | | | GND |
| 31 | | GND | | |
| 32 | DAS32– | | | SH0 |
| 33 | | | | SH1 |
| 34 | | | | GND |
| 35 | | ADDR02 | HW0 | |
| 36 | | ADDR03 | HW1 | |
| 37 | | ADDR04 | HW2 | |
| 38 | | ADDR05 | HW3 | |
| 39 | | ADDR06 | | GND |
| 40 | | ADDR07 | | GND |
| 41 | | ADDR08 | | GND |
| 42 | | ADDR09 | | GND |
| 43 | | ADDR10 | | +5 V |
| 44 | | ADDR11 | | +5 V |
| 45 | | | | |

| | D | C | B | A |
|---|---|---|---|---|
| | | ADDR12 | | +5 V |
| 46 | | ADDR13 | GND | +5 V |
| 47 | | ADDR14 | | +5 V |
| 48 | | ADDR15 | | +5 V |
| 49 | | ADDR16 | GND | +5 V |
| 50 | | ADDR17 | | +5 V |
| 51 | | ADDR18 | | +5 V |
| 52 | | ADDR19 | GND | +5 V |
| 53 | | ADDR20 | | +5 V |
| 54 | | ADDR21 | | +5 V |
| 55 | | ADDR22 | GND | |
| 56 | | ADDR23 | | |
| 57 | DATA24 | ADDR24 | | |
| 58 | DATA25 | ADDR25 | | |
| 59 | DATA26 | ADDR26 | | |
| 60 | DATA27 | ADDR27 | | |
| 61 | DATA28 | ADDR28 | | |
| 62 | DATA29 | ADDR29 | | |
| 63 | DATA30 | ADDR30 | | |
| 64 | DATA31 | ADDR31 | | |
| 65 | GND | | | |
| 66 | | | | |
| 67 | | | | |
| 68 | | GND | | |
| 69 | | | | |
| 70 | | | | |
| 71 | | | | |
| 72 | | | | |
| 73 | | | | |
| 74 | IDD0 | PBD0 | | |
| 75 | IDD1 | PBD1 | | |
| 76 | IDD2 | PBD2 | | |
| 77 | IDD3 | PBD3 | | |
| 78 | IDD4 | PBD4 | TSET | GND |
| 79 | IDD5 | PBD5 | TXD | GND |
| 80 | IDD6 | PBD6 | MPS4 | GND |
| 81 | IDD7 | PBD7 | RXD | GND |
| 82 | IDA0 | PBRD– | RSET | GND |
| 83 | IDA1 | PBWR– | PBE0 | GND |
| 84 | IDA2 | STTOPB– | PBE1 | GND |
| 85 | IDA3 | PBTOST– | PBE2 | GND |
| 86 | MPS5 | PWRFAIL | 307.2 | GND |
| 87 | –12 | PBC5 | +12 | GND |
| 88 | –12 | MPIO6 | +12 | GND |
| 89 | –12 | MPIO7 | +12 | GND |
| 90 | | | | |

# NT9X77AA

## Product description

The link paddle board (PB) provides the electrical interface between the link interface unit (LIU) and the Common Channel Signaling System 7 (CCS7) link. Two versions of the link PB are present: V.35 and DS-0A. The NT9X77AA is the V.35 version.

## Functional description

The V.35 version of the link PB provides standard layer-1 functions like level shifting drivers/receivers, and control of status lines. The link PB is between the signaling terminal (ST) and a data unit.

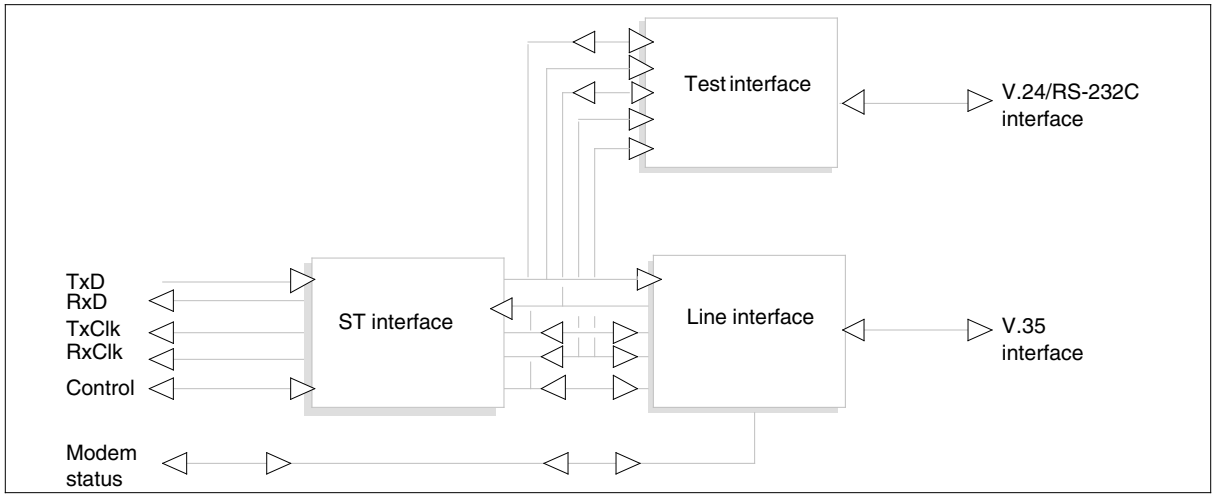
### Functional blocks

The NT9X77AA consists of the following functional blocks:

- ST interface
- line interface
- test set interface

The functional relationship between these blocks appears in the following figure.

**NT9X77AA functional blocks**



### Signaling terminal interface

The ST interface provides the following functions:

- internal clock generation
- clock loss monitoring for the transmit clock (TxClk) and the receive clock (RxClk)
- looparound buffer for loopbacks
- internal/external clock selection

### Line interface

The line interface provides the following functions:

- differential line drivers and receivers for data and clocks
- single-ended line drivers and receivers for status lines
- relay for paddle board loopback on data lines
- three 5PDT switches for DTE/DCE selection. Each switch has a ganged actuator.

### Test set interface

The test set interface provides the following functions:

- in monitor mode, the test set interface monitors the four status lines, and transmit data (TxD) and receive data (RxD) timed to TSET and RSET.
- in test mode, the test set interface monitors TxD and the four status lines timed to TSET. The interface transmits on RxD timed to RSET, and generates two clocks. The paddle board uses these clocks to generate the TxClk and RxClk for the ST.

## Signaling

### Pin numbers

The pin numbers for the V.35 line appear in the following table. The V.35 line uses a 25-pin D-type connector.

**V.35 line pin numbers (Sheet 1 of 2)**

| Signal | Pin | DTE mode | DCE mode |
|---|---|---|---|
| TxD-A | 1 | Output | Input |
| TxD-A | 2 | Output | Input |
| RxD-A | 7 | Input | Output |
| RxD-B | 8 | Input | Output |

## **NT9X77AA** (continued)

**V.35 line pin numbers (Sheet 2 of 2)**

| Signal | Pin | DTE mode | DCE mode |
|---|---|---|---|
| TSET-A | 3 | Input | Output |
| TSET-B | 4 | Input | Output |
| RSET-A | 9 | Input | Output |
| RSET-B | 10 | Input | Output |
| RTS | 13 | Output | Input |
| RFS | 14 | Input | Output |
| DSR | 15 | Input | Output |
| DCD | 16 | Input | Output |
| SGND | 21 | | |
| FMGND | 22 | | |
| DCETS-A | 20 | Output | Output |

The pin numbers for the V.24 test set interface appear in the following table. The V.24 test set interface uses a 25-pin D-type connector.

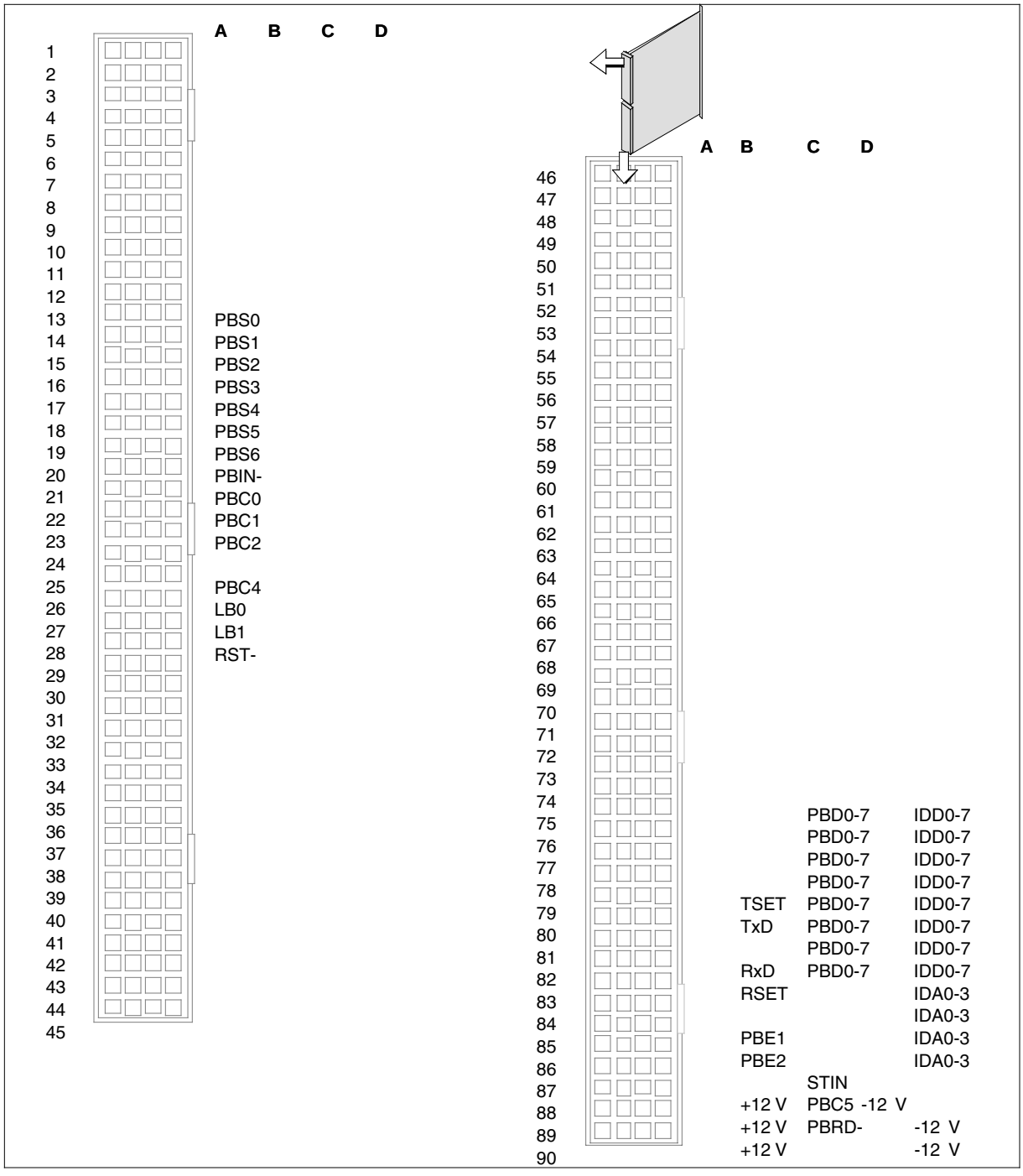
**V.24 test set pin numbers**

| Signal | Pin | Test set |
|---|---|---|
| V24RXD | 19 | Output |
| V24TSET | 23 | Output |
| V24RSET | 21 | Output |
| VRXD | 3 | Input |
| RS-V24 | 25 | Input |
| VSCT | 15 | Input |
| VSCR | 17 | Input |
| FRMGND | 1 | Ground |
| SIGND | 7 | Ground |

# **NT9X77AA** (end)

The NT9X77AA pin numbers for appear in the figure that follows.

**NT9X77AA pin numbers**



# NT9X77AB

## Product description

The link paddle board (PB) provides the electrical interface between the link interface unit (LIU) and the Common Channel Signaling System 7 (CCS7) link. Two versions of the link PB are available. The NT9X77AB versions are V.35 and DS-0A. The is the V.35 version.

## Functional description

The V.35 version of the link PB provides the following functions:

- normal layer-1 functions.
- level shifting drivers/receivers.
- input/output isolation.
- control of status lines.

This link PB resides between the signaling terminal (ST) and a data unit.

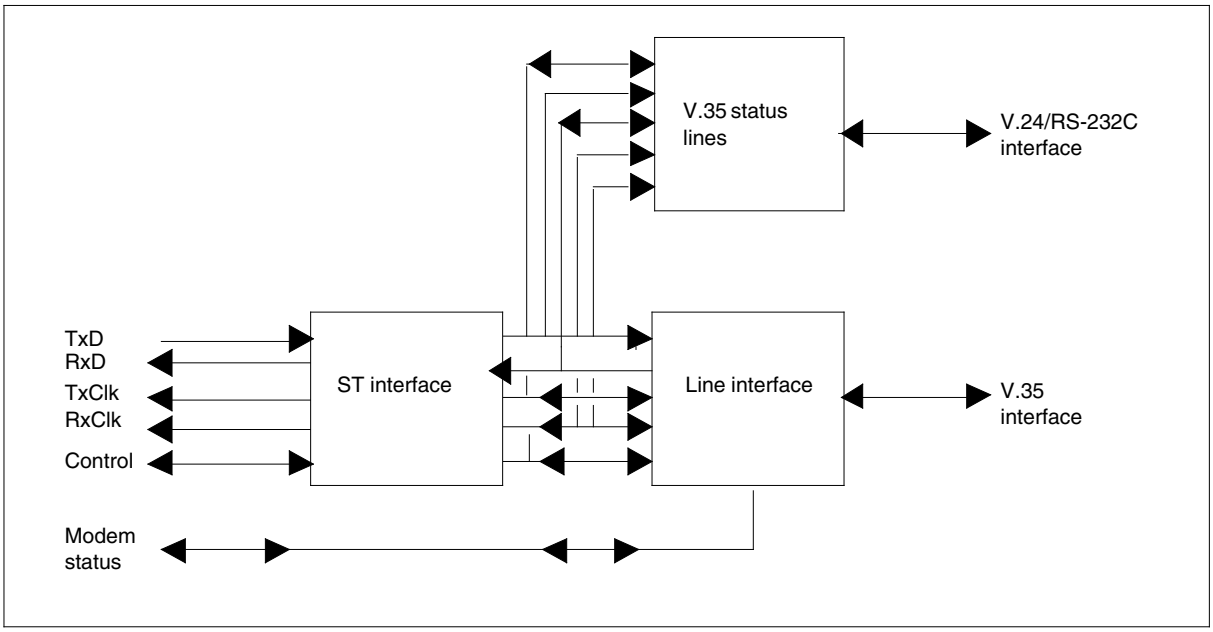
### Functional blocks

The NT9X77AB contains the following functional blocks:

- ST interface
- line interface

The functional relationship between these blocks appears in the following figure.

**NT9X77AB functional blocks**




## Signaling terminal interface

The ST interface provides the following functions:

- internal clock generation
- clock loss monitoring for both the transmit clock (TxClk) and the receive clock (RxClk)
- looparound buffer for loopbacks
- internal/external clock selection

## Line interface

The line interface provides the following functions:

- isolated differential line drivers and receivers for data and clocks
- isolated single-ended line drivers and receivers for status lines
- relay for paddle board loopback on data lines
- three 5PDT switches for DTE/DCE selection. Each switch has a ganged actuator.

## **NT9X77AB** (continued)

# Signaling

### Pin numbers

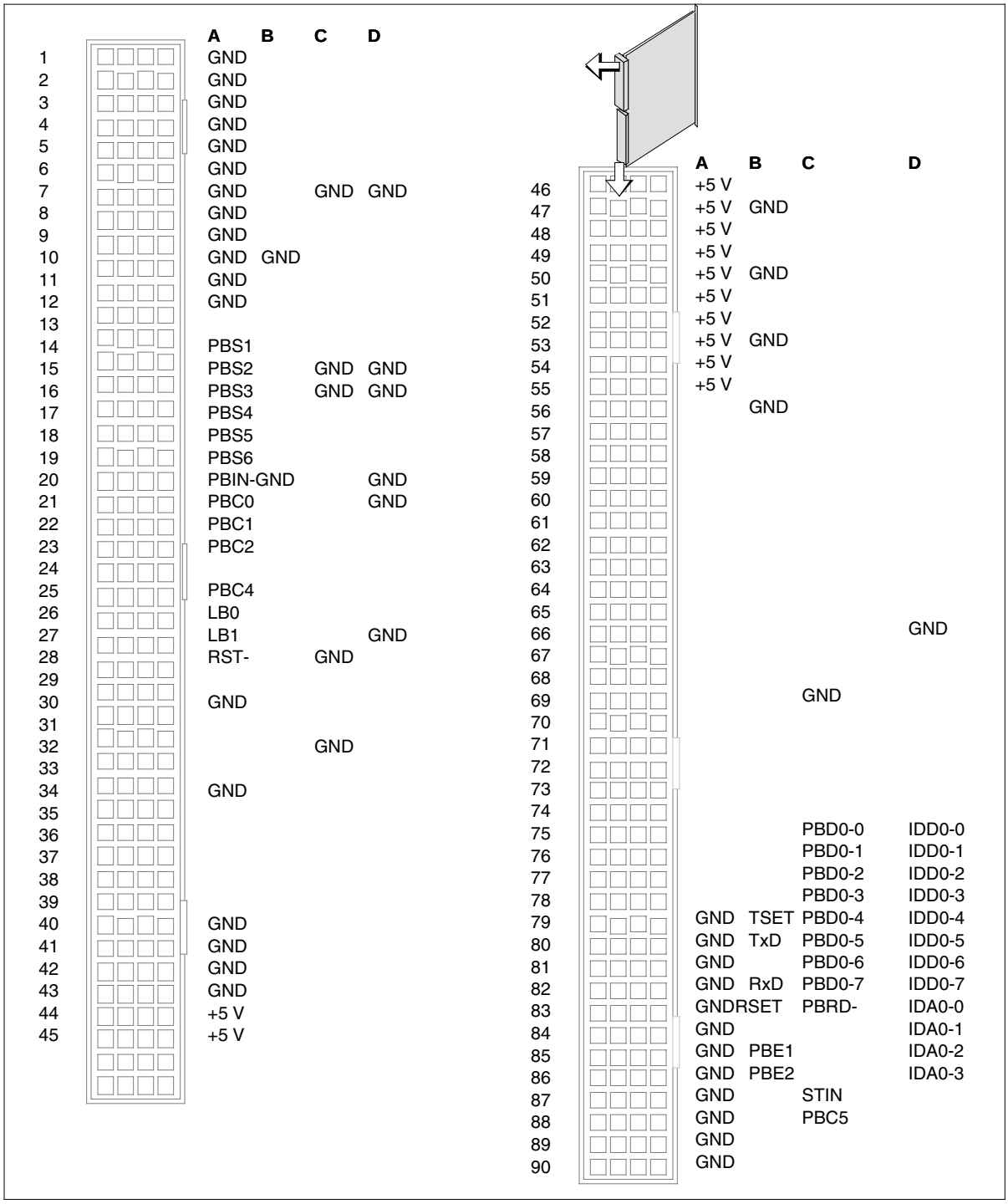
The pin numbers for the V.35 line appear in the following table. The V.35 line uses a 25-pin D-type connector.

**V.35 line pin numbers**

| Signal | Pin | DTE mode | DCE mode |
|---|---|---|---|
| TxD-A | 1 | Output | Input |
| TxD-B | 2 | Output | Input |
| RxD-A | 7 | Input | Output |
| RxD-B | 8 | Input | Output |
| TSET-A | 3 | Input | Output |
| TSET-B | 4 | Input | Output |
| RSET-A | 9 | Input | Output |
| RSET-B | 10 | Input | Output |
| RTS | 13 | Output | Input |
| RFS | 14 | Input | Output |
| DSR | 15 | Input | Output |
| DCD | 16 | Input | Output |
| ISOGND | 21 | | |
| DCETS-B | 19 | Output | Output |
| DCETS-A | 20 | Output | Output |

The pin numbers for NT9X77AB appear in the following figure.

### NT9X77AB pin numbers



# NT9X77BA

## Product description

The NT9X77BA is an asynchronous and synchronous interface paddle board. The NT9X77BA provides access for the V.35 and RS232 interfaces to the link interface unit data communications (LIUCOM) signaling terminal (ST) card (NT9X76BA).

One main difference is present between the NT9X77AA V.35 paddle board and the NT9X77BA V.35 paddle board. This difference is the addition of the RS232 synchronous and asynchronous interface.

The NT9X77BA can operate as data communications equipment (DTE) or data terminal equipment (DCE). The setting of a bank of switches on the card determines this function. The switches reflect the options that apply to the datafill of the LIUCOM ST CP. The V.35 interface can operate as a DTE or a DCE. The RS232 port can operate in DTE mode synchronous or asynchronous or DCE mode synchronous or asynchronous.

### Location

The NT9X77BA resides in the link interface shelf (LIS), in the slots behind the NT9X76BA.

## Functional description

### Functional blocks

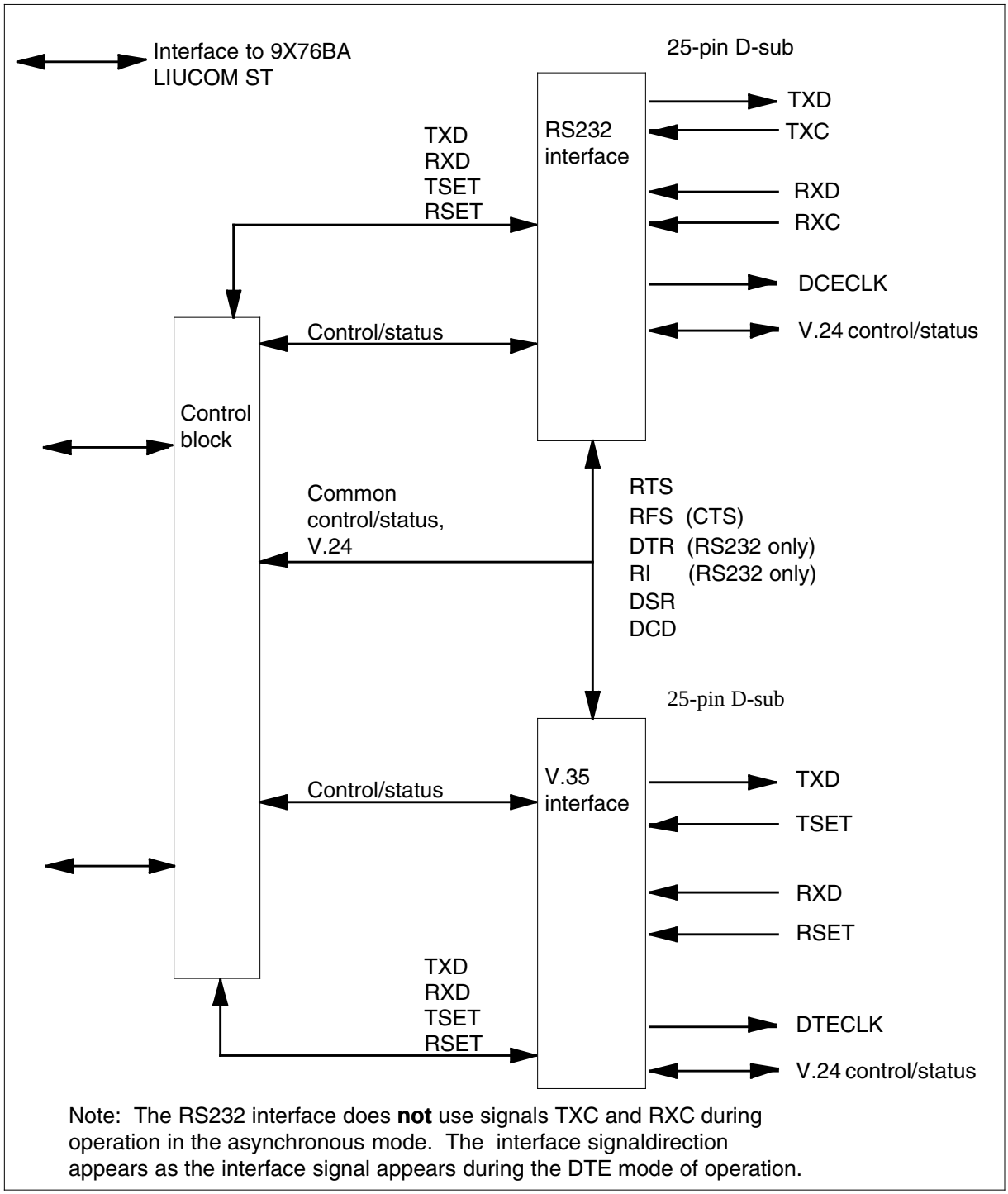
The NT9X77BA has the following functional blocks:

- RS232 interface
- V.35 interface
- interface control

The RS232 interface, and the V.35 interface perform signal translation. The control block monitors the status and configuration of the paddle board and implements a selection of modes of operation and tests.

The relationship between the functional blocks appears in the following figure.

**NT9X77BA functional blocks**




Note: The RS232 interface does **not** use signals TXC and RXC during operation in the asynchronous mode. The interface signaldirection appears as the interface signal appears during the DTE mode of operation.

## **NT9X77BA** (continued)

### RS232 interface

The RS232 interface converts transistor-transistor-logic (TTL) signals from the LIUCOM ST and the serial communications controller (SCC) to RS232 levels. The RS232 converts the signals for transmission to an external modem. The interface converts incoming signals from RS232 format to TTL levels for the SCC.

### V.35 interface

The V.35 interface converts TTL signals from the LIUCOM ST and the SCC into V.35 levels. The V.35 converts the signals for transmission to an external modem. The interface converts incoming signals from V.35 format to TTL levels for the SCC.

### Interface control

The interface control block controls and monitors the state of the RS232 and the V.35 interfaces. The control block has the following functions:

- generates a 56-kHz clock when the paddle board is in the DCE mode of operation
- selects DTE or DCE operation mode
- notifies the LIUCOM ST of the operation mode status
- establishes a looparound buffer to hold incoming data for the SCC
- monitors loss of signal element timing, and large differences in frequency
- provides clocking signals for the DTE and DCE configurations, and the ST loopback, paddle board loopback, and line loopback
- identifies the type of paddle board installed behind the LIUCOM ST CP

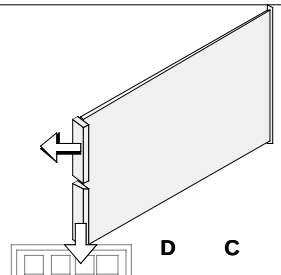
## Signaling

### Pin numbers

The pin numbers for the NT9X77BA appear in the following figures.

# **NT9X77BA** (continued)

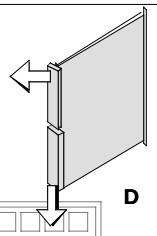
**NT9X77BA pin numbers (Part 1 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | GND |
| 2 | | | | GND |
| 3 | | | | GND |
| 4 | | | | GND |
| 5 | | | | GND |
| 6 | | | | GND |
| 7 | GND | GND | | GND |
| 8 | | | | GND |
| 9 | | | | GND |
| 10 | | | GND | GND |
| 11 | | | | GND |
| 12 | | | | GND |
| 13 | | | | RI/DTR |
| 14 | | | | RELAY- |
| 15 | GND | GND | | DCE- |
| 16 | GND | GND | | RFS/RTS |
| 17 | | | | DTE-DSR |
| 18 | | | | DTE-DCD |
| 19 | | | | SWERR- |
| 20 | GND | | GND | PBIN- |
| 21 | GND | | | RTS/RFS |
| 22 | | | | DCE-DSR |
| 23 | | | | DCE-DCD |
| 24 | | | | DTR/RI |
| 25 | | | | CLKSEL |
| 26 | | | | LB0 |
| 27 | GND | | | LB1 |
| 28 | | GND | | PBRST- |
| 29 | | | | |
| 30 | | | | GND |
| 31 | | | | |
| 32 | | GND | | |
| 33 | | | | |
| 34 | | | | GND |
| 35 | | | | |
| 36 | | | | |
| 37 | | | | |
| 38 | | | | |
| 39 | | | | |
| 40 | | | | GND |
| 41 | | | | GND |
| 42 | | | | GND |
| 43 | | | | GND |
| 44 | | | | +5V |
| 45 | | | | +5V |

# **NT9X77BA** (end)

### NT9X77BA pin numbers (Part 2 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 46 | | | | +5V |
| 47 | | | GND | +5V |
| 48 | | | | +5V |
| 49 | | | | +5V |
| 50 | | | GND | +5V |
| 51 | | | | +5V |
| 52 | | | | +5V |
| 53 | | | GND | +5V |
| 54 | | | | +5V |
| 55 | | | | +5V |
| 56 | | | GND | |
| 57 | | | | |
| 58 | | | | |
| 59 | | | | |
| 60 | | | | |
| 61 | | | | |
| 62 | | | | |
| 63 | | | | |
| 64 | | | | |
| 65 | | | | |
| 66 | GND | | | |
| 67 | | | | |
| 68 | | | | |
| 69 | | GND | | |
| 70 | | | | |
| 71 | | | | |
| 72 | | | | |
| 73 | | | | |
| 74 | | | | |
| 75 | IDD0 | PPP0 | | |
| 76 | IDD1 | PPP1 | | |
| 77 | IDD2 | PPP2 | | |
| 78 | IDD3 | PPP3 | | |
| 79 | IDD4 | PPP4 | TSET | GND |
| 80 | IDD5 | PPP5 | TXD | GND |
| 81 | IDD6 | PPP6 | | GND |
| 82 | IDD7 | PPP7 | RXD | GND |
| 83 | IDA0 | PBRD- | RSET | GND |
| 84 | IDA1 | | | GND |
| 85 | IDA2 | | TCKL- | GND |
| 86 | IDA3 | | RCKL- | GND |
| 87 | | PWRFAIL | 307.2 | GND |
| 88 | -12V | TSTCKL- | | GND |
| 89 | -12V | V35EN | | GND |
| 90 | -12V | ASYNC | | GND |

# NT9X78AA

## Product description

The link interface unit (LIU7) of the link interface modules of the signaling transfer point (STP) switch contains the DS-0A interface paddle board. The DS-0 interface provides layer-1 functions like level shifting drivers/receivers between the signaling terminal (ST) and a digital line.

## Functional description

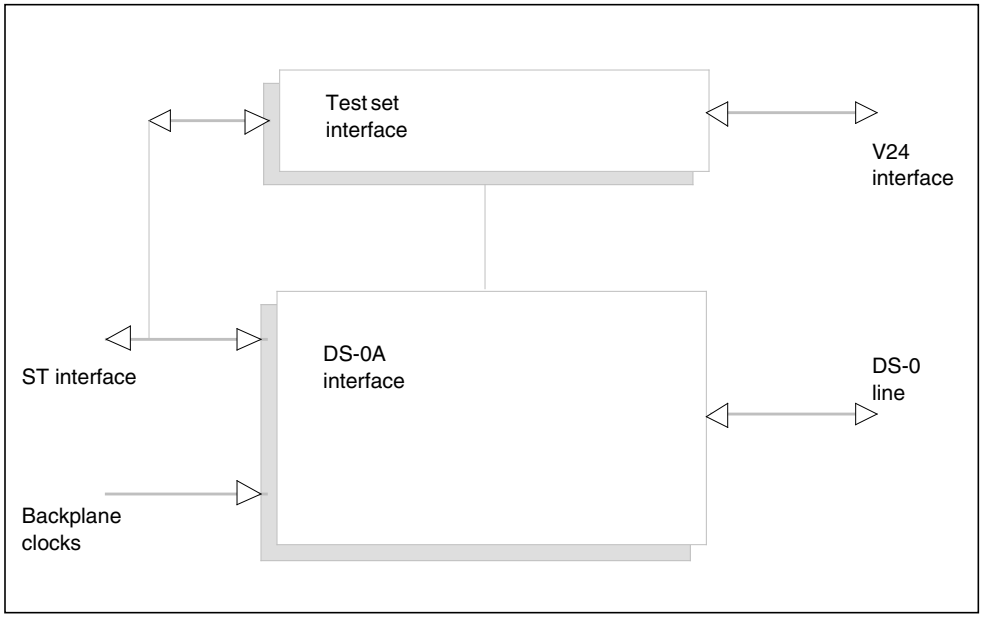
### Functional blocks

The NT9X78AA consists of the following major functional blocks:

- DS-0A interface
- test set interface

The functional relationship between these blocks appears in the following figure.

**NT9X78AA functional blocks**




### DS-0A interface

The DS-0A interface contains the clock section and the data section.

## **NT9X78AA** (continued)

The clock section performs the following functions on the DS-0A paddle board:

- internal clock generation
- external clock decoding
- clock selection and switching
- backup and primary clock loss detection
- clock error detection

The data section transmits and receives data. The data section transmits data from the SCC and the control-code bit to the DS-0 transmit line. The data section terminates the receive data line with a transformer and comparator circuit. The two outputs of the comparators are ORed together to produce the unipolar transitor-transitor logic (TTL) receive-data stream. The TTL receive-data stream is buffered for a period of a time in a one-byte shift register. The paddle board loopback loops data back from the output of the transmit DS-0 line transformer. The paddle board loopback loops the data to the input of the receive DS-0 line transformer. This process allows a complete test of the transmit and receive data paths.

### Test set interface

In monitor mode, the test set interface contains the following V.24 drivers:

- transmit data
- transmit clock
- receive data
- receive clock

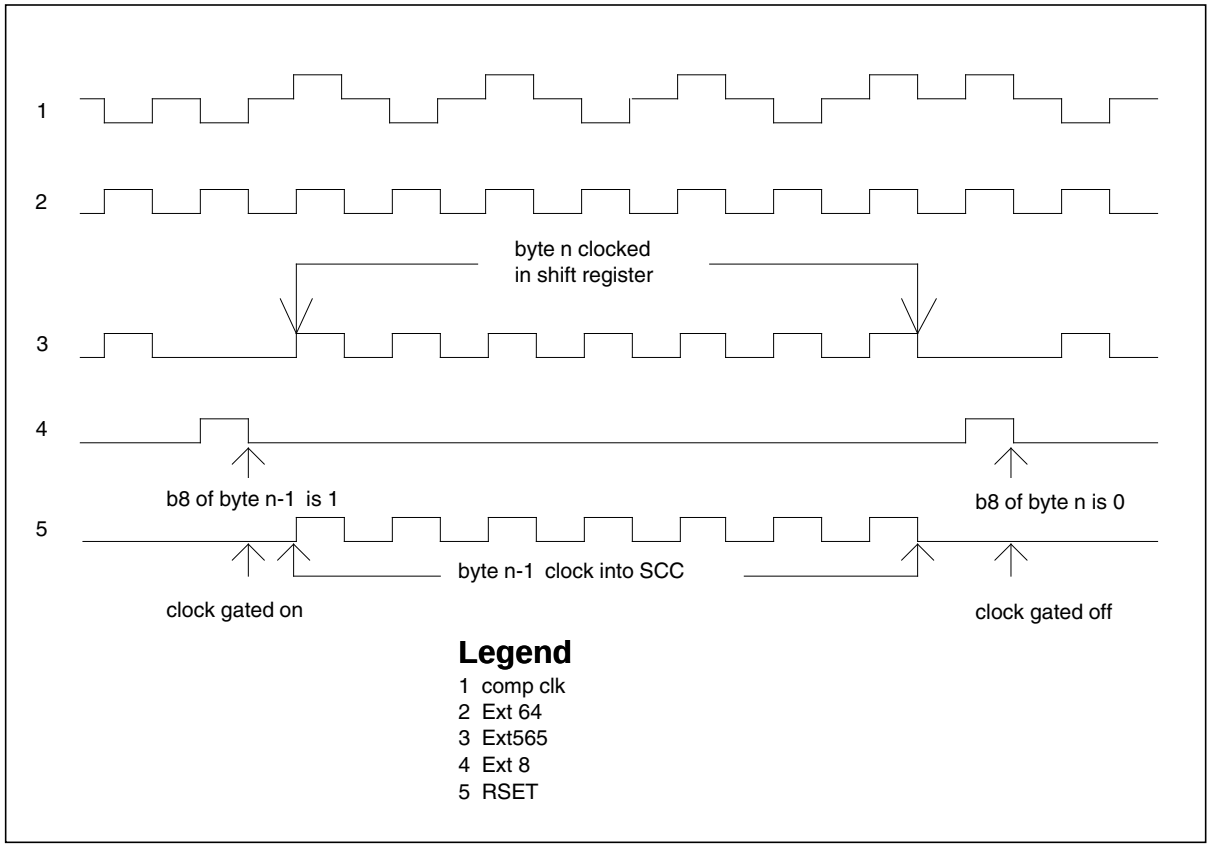
When the paddle board is in ST loopback, the test set interface only monitors the transmit data line.

# Signaling

### Timing

Timing for NT9X78AA appears in the following figure.

**NT9X78AA timing**




## Pin numbers

The DS-0 line interface pin numbers appear in the following table. The DS-0 line interface uses a 25-pin D-type connector with eight connected lines.

**NT9X78AA DS-0 line interface pin numbers (Sheet 1 of 2)**

| Signal | Pin | Type | |
|---|---|---|---|
| RXR | 1 | Input | DS0A |
| RXT | 2 | Input | DS0A |
| TXR | 3 | Output | DS0A |
| TXT | 4 | Output | DS0A |
| Gnd | 7 | | |
| Gnd | 8 | | |

## **NT9X78AA** (continued)

**NT9X78AA DS-0 line interface pin numbers (Sheet 2 of 2)**

| Signal | Pin | Type |
|---|---|---|
| CCLKR | 9 | |
| CCLKT | 10 | |

The board test interface pin numbers appear in the following table. The board test interface uses a 25-pin D-type connector.

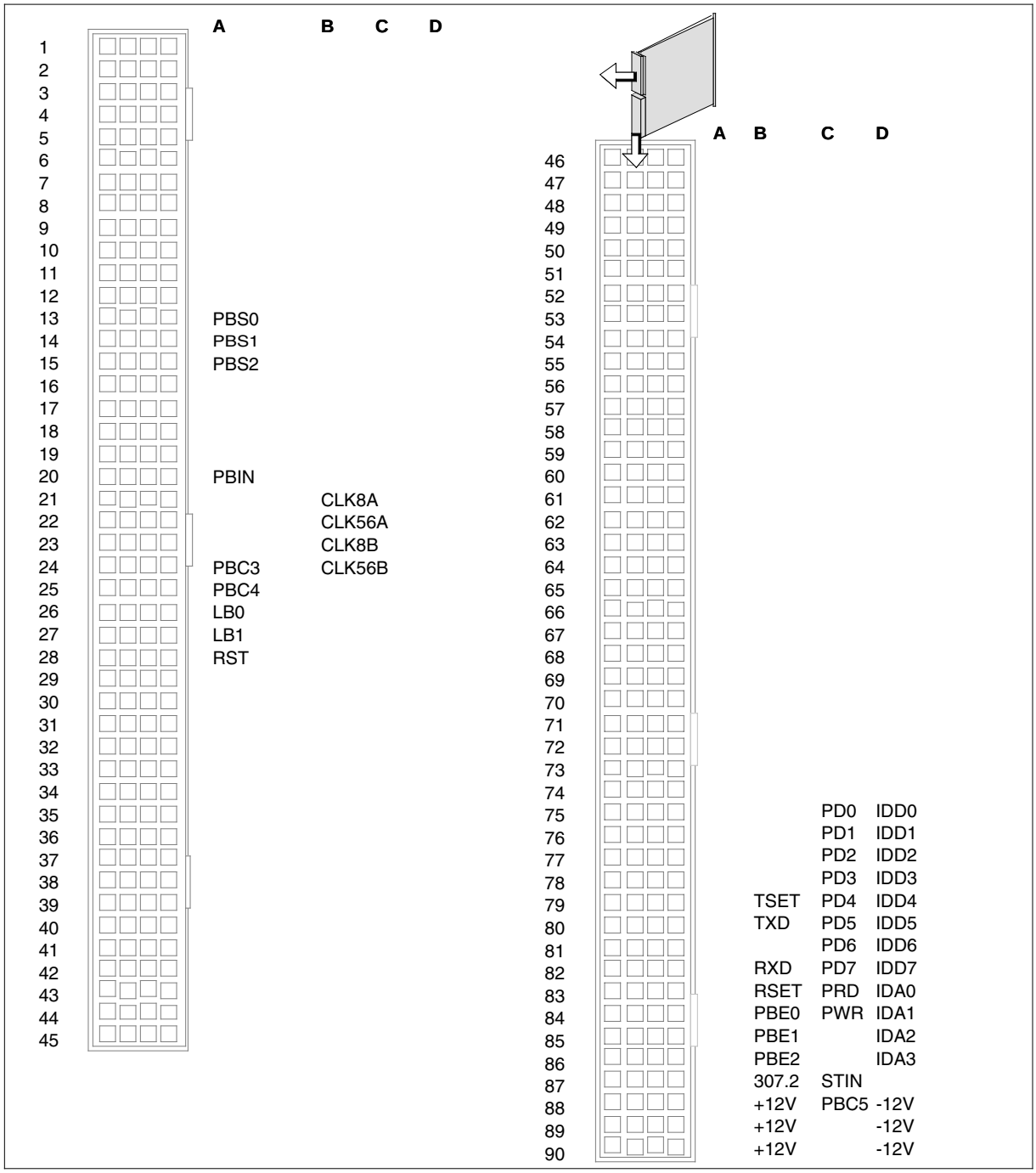
**NT9X78AA board test interface pin numbers**

| Signal | Pin | Type | |
|---|---|---|---|
| Gnd | 1 | Input | PWR |
| TD | 2 | Output | RS232 |
| RD | 3 | Input | RS232 |
| Gnd | 7 | Input | PWR |
| V24VLK | 12 | Input | RS232 |
| SCT | 15 | Output | RS232 |
| SCR | 17 | Output | RS232 |
| RDI | 10 | Input | RS232 |
| EM | 25 | Input | RS232 |

The pin numbers for the ST interface of the appear in the following figure.

# **NT9X78AA** (continued)

### NT9X78AA pin numbers



## **NT9X78AA** (end)

# Technical data

### Power requirements

The currents that NT9X78AA uses appear in the following table.

**Power requirements for NT9X78AA**

| Supply voltage | Standard current (mA) | Maximum current (mA) |
|---|---|---|
| +5 | 975 | 1307 |
| +12 | 79 | 106.8 |
| -12 | 54 | 75 |

# NT9X78BA

## Product description

The NT9X78BA enhanced DS-0A interface paddle board provides an electrical interface. This electrical interface is between the link interface unit (LIU7) and the Common Channel Signaling System No. 7 (CCS7) link.

The NT9X78BA responds to digital data system (DDS) control signals in the DS-0 input stream. The card is the signaling link front end for the signaling transfer point (STP).

### Location

The NT9X78BA is in the LIU7 of the link interface module (LIM) of the STP switch.

### Compatibility

The NT9X78BA is normally backward compatible with the NT9X78AA. When the system does not support the external composite clock recovery, the NT9X78BA is not backward compatible with the NT9X78AA.

## Functional description

The NT9X78BA performs the following functions:

- provides an interface between the LIU7 and the CCS7 link at a data rate of 56 Kbaud
- provides bipolar violation monitoring of the incoming line
- provides digital trunk equipment (DTE) configuration to DS-0 interface
- originates and responds to latching loopback control codes on DS-0 lines
- provides an RS-232 test terminal interface
- performs functional self-test on power-up, or in response to a request from the signaling terminal (ST)

### Functional blocks

The NT9X78BA card contains four functional blocks:

- DS-0A interface
- microcontroller
- test interface
- clock generation and selection

## NT9X78BA (continued)

### DS-0A interface

The DS-0A interface provides standard layer-1 functions, like level-shifting drivers and receivers between the ST and a digital line.

### Microcontroller

The microcontroller provides the software to perform the following functions:

- full self test
- manufacture test
- receives and generates DS-0 line control code
- communication with the ST

### Test interface

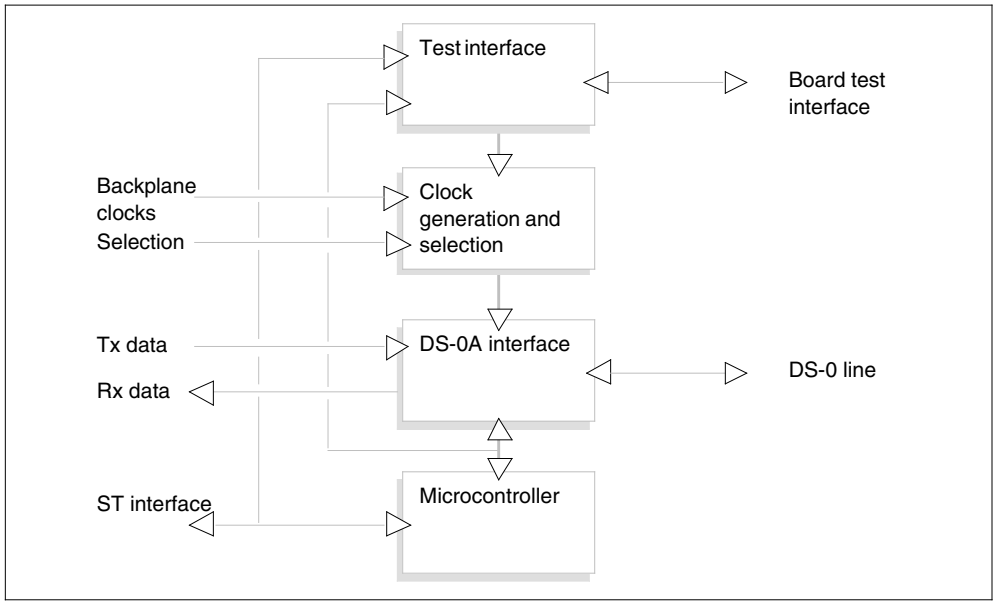
The test interface provides the RS-232 level interface for connection to standard terminals.

### Clock generation and selection

The clock generation and selection block generates the internal clocks that the NT9X78BA requires. The clock generation and selection block selects one of the three possible clock sources for the DS-0 line.

The functional relationship between these blocks appears in the following figure.

**NT9X78BA functional blocks**

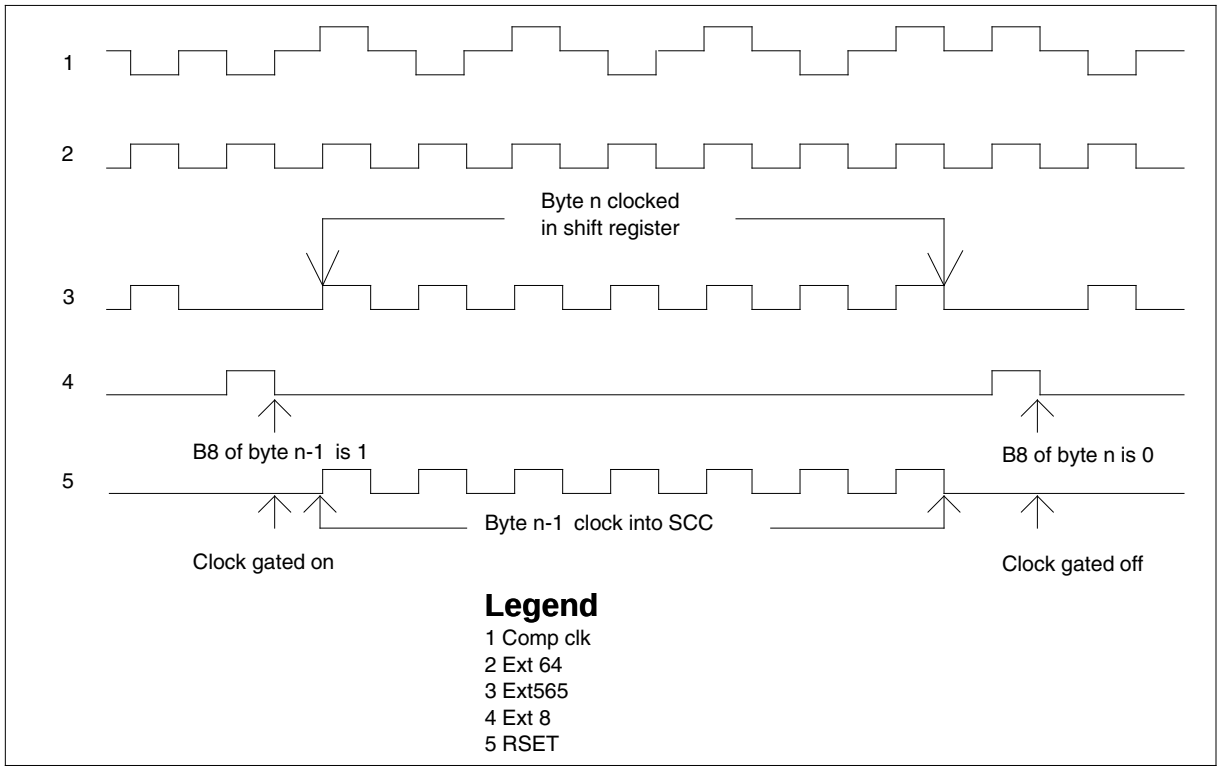


# Signaling

## Timing

The timing for the NT9X78BA appears in the following figure.

**NT9X78BA timing**




## Pin numbers

The table that follows lists the DS-0 line interface pin numbers. The DS-0 line interface uses a 25-pin D-type connector, with eight connected lines.

**NT9X78BA DS-0 line interface pin numbers (Sheet 1 of 2)**

| Signal | Pin | Type | |
|---|---|---|---|
| RXR | 1 | Input | DS0 |
| RXT | 2 | Input | DS0 |
| TXR | 3 | Output | DS0 |
| TXT | 4 | Output | DS0 |
| Gnd | 7 | Input | PWR |

## **NT9X78BA** (continued)

**NT9X78BA DS-0 line interface pin numbers (Sheet 2 of 2)**

| Signal | Pin | Type | |
|---|---|---|---|
| Gnd | 8 | Input | PWR |
| CCLKR | 9 | | DS0 |
| CCLKT | 10 | | DS0 |

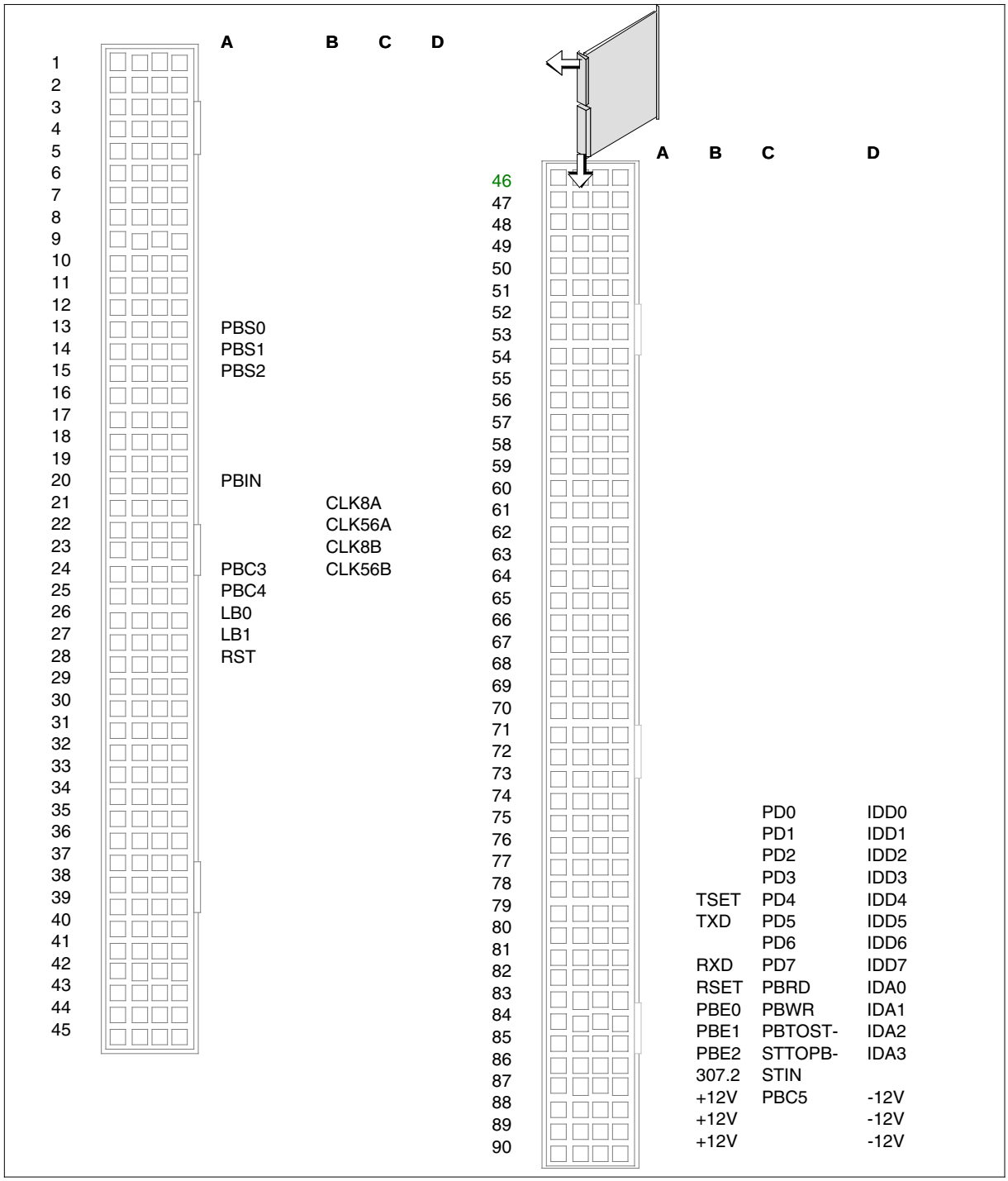
The board test interface pin numbers appear in the following table. The board test interface uses a 25-pin D-type connector.

**NT9X78BA board test interface pin numbers**

| Signal | Pin | Type | |
|---|---|---|---|
| Gnd | 1 | Input | PWR |
| TD | 2 | Output | RS232 |
| RD | 3 | Input | RS232 |
| Gnd | 7 | Input | PWR |
| V24VLK | 12 | Input | RS232 |
| SCT | 15 | Output | RS232 |
| SCR | 17 | Output | RS232 |
| RDI | 10 | Input | RS232 |
| TEST | 24 | Input | RS232 |
| EM | 25 | Input | RS232 |

The pin numbers for the ST interface of the NT9X78BA appear in the following figure.

### NT9X78BA pin numbers



# NT9X78CA

## Product description

The NT9X78CA enhanced DS-0A interface paddle board provides an electrical interface. This electrical interface occurs between the link interface unit (LIU7) and the Common Channel Signaling System No. 7 (CCS7) link.

The NT9X78CA responds to digital data system (DDS) control signals in the DS-0 input stream. This card is the signaling link front end for the signaling transfer point (STP).

### Location

The NT9X78CA is in the LIU7 of the link interface module (LIM) of the STP switch.

### Compatibility

The NT9X78CA is normally backward compatible with the NT9X78AA. When the system does not support external composite clock recovery, the NT9X78CA is not backward compatible with the NT9X78AA.

## Functional description

The NT9X78CA performs the following functions:

- provides an interface between the LIU7 and the CCS7 link at a data rate of 56 Kbaud or 64 Kbaud
- provides bipolar violation monitoring of the incoming line
- provides digital trunk equipment (DTE) configuration to DS-0 interface
- originates and responds to latching loopback control codes on DS-0 lines
- provides an RS-232 test terminal interface
- performs functional self-test on power-up, or in response to a request from the signaling terminal (ST)

### Functional blocks

The NT9X78CA card contains four functional blocks:

- DS-0A interface
- microcontroller
- test interface
- clock generation and selection

### DS-0A interface

The DS-0A interface provides standars layer-1 functions, like level-shifting drivers and receivers between the ST and a digital line.

### Microcontroller

The microcontroller performs the following functions:

- full self test
- manufacture test
- receives and generates DS-0 line control code
- communication with the ST

### Test interface

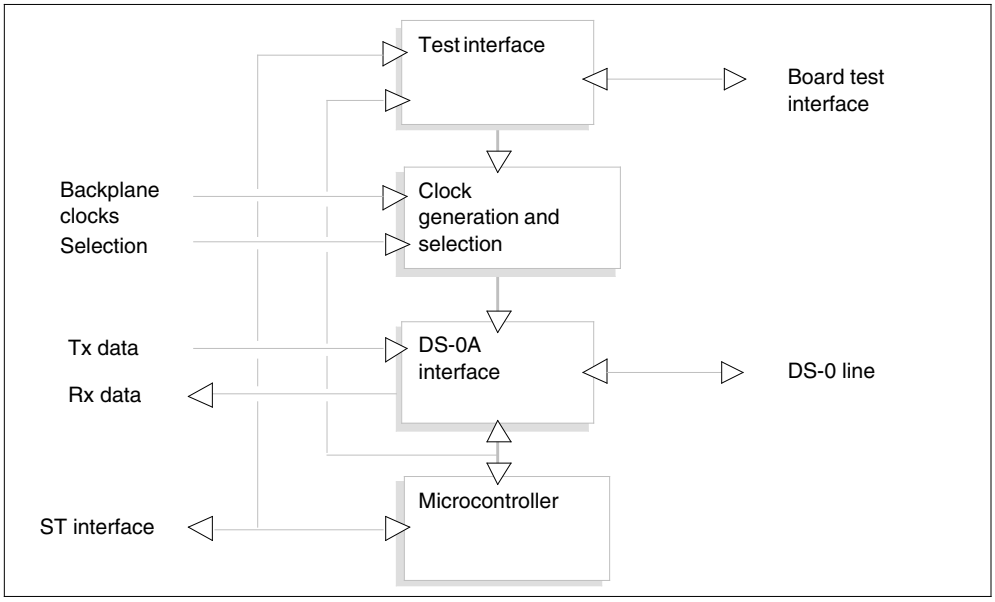
The test interface provides the RS-232 level interface for connection to standard terminals.

### Clock generation and selection

The clock generation and selection block generates the internal clocks that the NT9X78CA requires. The clock generation and selection block selects one of the three possible clock sources for the DS-0 line.

The functional relationship between these blocks appears in the following figure.

**NT9X78CA functional blocks**



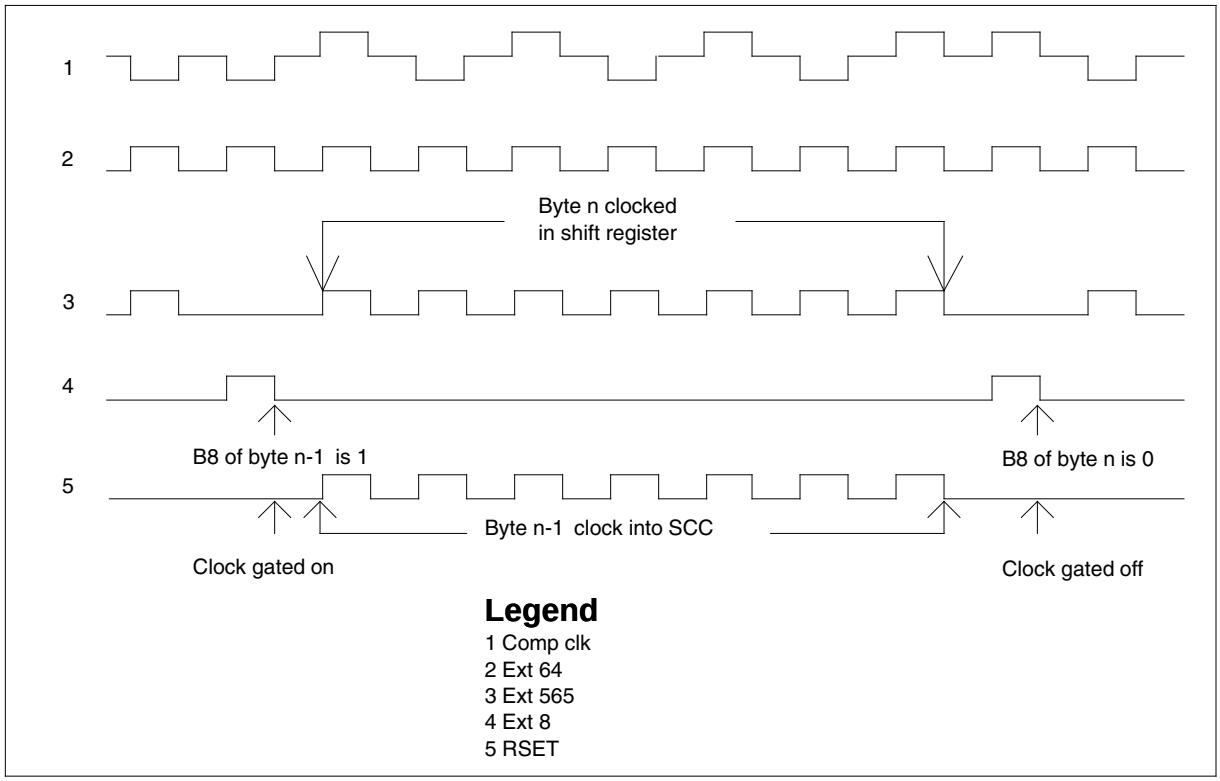
## NT9X78CA (continued)

# Signaling

### Timing

The timing for the NT9X78CA appears in the following figure.

**NT9X78CA timing**




### Pin numbers

The DS-0 line interface pin numbers appear in the following table. The DS-0 line interface uses a 25-pin D-type connector, with eight connected lines.

**NT9X78CA DS-0 line interface pin numbers (Sheet 1 of 2)**

| Signal | Pin | Type | |
|---|---|---|---|
| RXR | 1 | Input | DS0 |
| RXT | 2 | Input | DS0 |
| TXR | 3 | Output | DS0 |
| TXT | 4 | Output | DS0 |
| Gnd | 7 | Input | PWR |

**NT9X78CA DS-0 line interface pin numbers (Sheet 2 of 2)**

| Signal | Pin | Type | |
|---|---|---|---|
| Gnd | 8 | Input | PWR |
| CCLKR | 9 | | DS0 |
| CCLKT | 10 | | DS0 |

The board test interface pin numbers appear in the following table. The board test interface uses a 25-pin D-type connector.

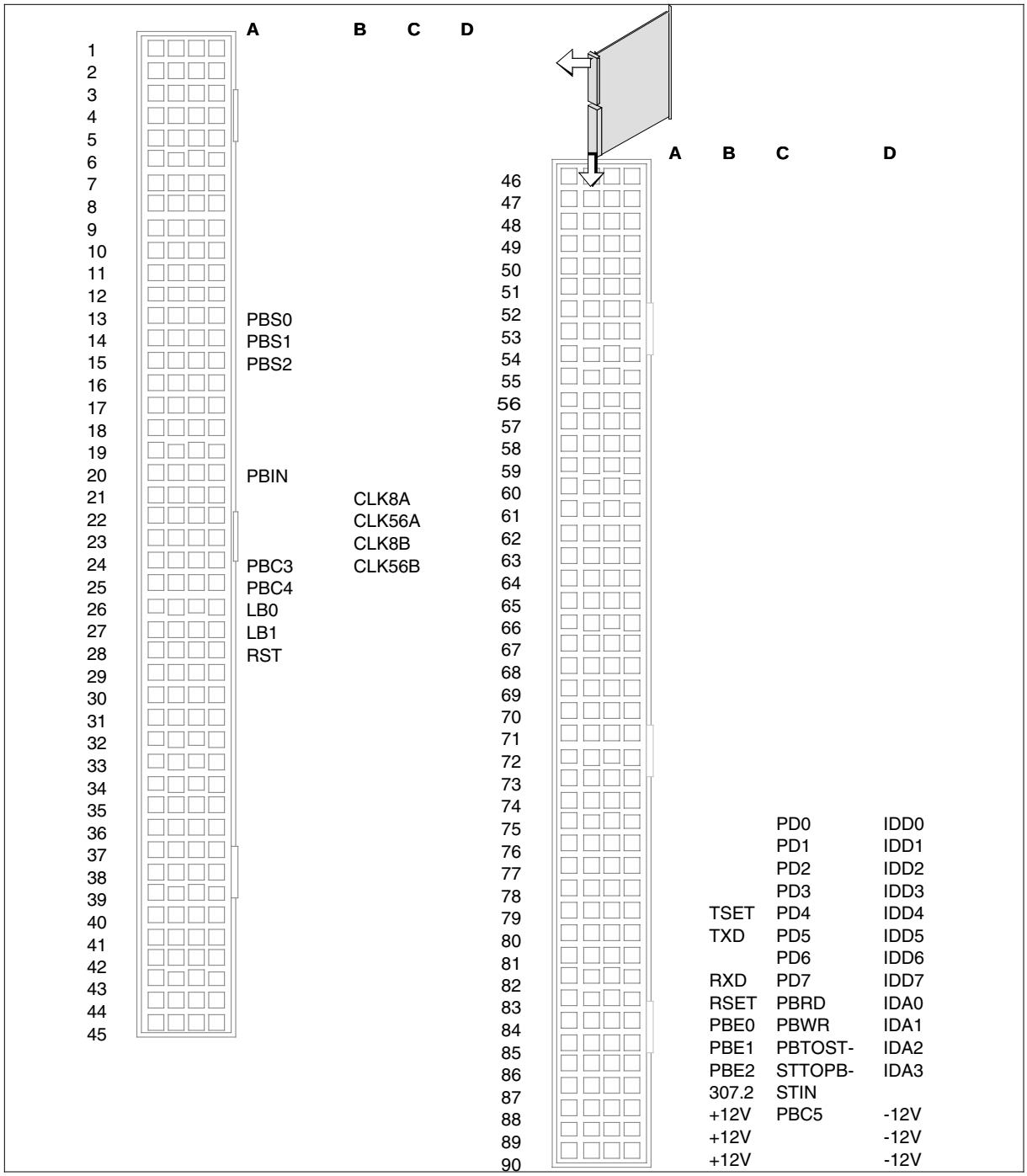
**NT9X78CA board test interface pin numbers**

| Signal | Pin | Type | |
|---|---|---|---|
| Gnd | 1 | Input | PWR |
| TD | 2 | Output | RS232 |
| RD | 3 | Input | RS232 |
| Gnd | 7 | Input | PWR |
| V24VLK | 12 | Input | RS232 |
| SCT | 15 | Output | RS232 |
| SCR | 17 | Output | RS232 |
| RDI | 10 | Input | RS232 |
| TEST | 24 | Input | RS232 |
| EM | 25 | Input | RS232 |

The pin numbers for the ST interface of the NT9X78CA appear in the following figure.

# **NT9X78CA** (end)

### NT9X78CA pin numbers



# NT9X79AA

## Product description

The NT9X79AA is a frame transport bus (F–bus) extension paddle board.

### Location

The NT9X79AA is behind the NT9X74 in the top and middle link interface shelves (LIS). The NT9X74 is the F–bus repeater card. These LIS are in the link interface module (LIM).

## Functional description

The NT9X79AA performs the following main functions:

- to terminate and distribute the differential intershelf F–bus
- to provide the termination and distribution for the DS–0 Composite Clock input to the link peripheral processor (LPP) frame

On the middle two shelves, the NT9X79AA provides a connection between the F–bus cables and the rate adaptor (RA). This connection is for the F–bus signals. The NT9X79AA receives the DS–0 clock signals from the F–bus cable as differential signals. The signals are converted to single–ended levels, and sent to the NT9X74. The NT9X74 routes the signals to the correct backplane pin. The differential signals on the NT9X79AA do not have termination resistors.

### Functional blocks

The NT9X79AA has the following functional blocks:

- F–bus
- composite clock

### Frame transport bus

The F–bus must meet requirements for the NT9X79AA to work. The F–bus must:

- provide a connection on each shelf for intershelf F–bus cables
- terminate intershelf F–bus cable signals to minimize unwanted reflections. The F–bus and DS–0 clock signals are F–bus cable signals
- guarantee that the receiver views a high level on the bus when the bus is idle, for F–bus signals

The F–bus signals originate on the local message switch (LMS) T–bus. The RA differentially drives the F–bus signals to the bottom three shelves. The Repeater converts these differential signals to single–ended levels, and drives the single–ended levels across the LIS backplane.

## **NT9X79AA** (continued)

### Composite clock

The composite clock must meet certain requirements for the NT9X79AA to work. The composite clock must:

- provide a connection to the LIM for composite clock input
- convert the composite clock to differential signal levels for distribution to the bottom three LIS shelves
- convert differential DS–0 clock signal levels to single–ended levels for distribution on the LIS backplane
- terminate single–ended DS–0 clock signals at both ends of the LIS backplane

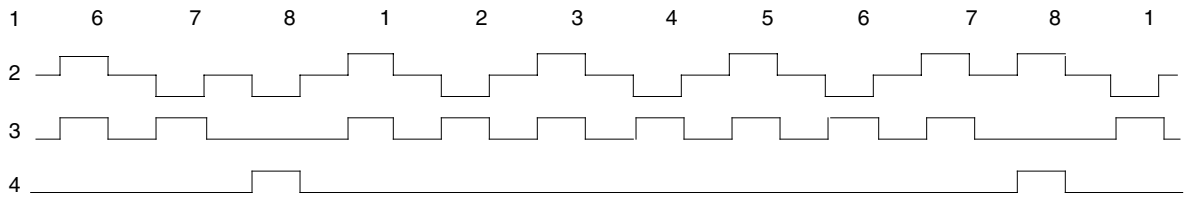
The composite clock input to the LIM provides the timing source for all DS–0 links to the LIM. The composite clock input to the LIM terminates on the NT9X79. The system must convert the bipolar, balanced composite clock input to differential. The system must drive the bipolar, balanced composite clock input across the F–bus cable through the NT9X79. The three bottom shelves must receive the input. The system drives the composite clock as a single–ended signal to the DS–0 paddle boards on each shelf.

# Signaling

### Timing

The timing for the NT9X79AA appears in the following figure.

**NT9X79AA timing**




**Legend**

1 Bit timer
2 Composite clock
3 56 clock
4 8 clock

**Note**: The composite clock input has a 5/8 duty cycle (high 5 to low 3).

## Pin numbers

The pin numbers for the F–bus connectors appears in the following table.

**NT9X79AA F–bus connector pin numbers**

| Pin A | Name | Pin B | Name |
|---|---|---|---|
| 1 | FRGND | 20 | FCLK+ |
| 2 | FCLK- | 21 | Gnd |
| 3 | FAD0+ | 22 | FAD0- |
| 4 | FAD1+ | 23 | FAD1- |
| 5 | FAD2+ | 24 | FAD2- |
| 6 | FAD3+ | 25 | FAD3- |
| 7 | Gnd | 26 | FAD4+ |
| 8 | FAD4- | 27 | FAD5+ |
| 9 | FAD5- | 28 | FAD6+ |
| 10 | FAD6- | 29 | FAD7+ |
| 11 | FAD7- | 30 | Gnd |
| 12 | FPAR+ | 31 | FPAR- |
| 13 | FADREN+ | 32 | FADREN- |
| 14 | FDAEN+ | 33 | FDAEN- |
| 15 | FEOS+ | 34 | FEOS- |
| 16 | Gnd | 35 | FRST+ |
| 17 | FRST- | 36 | FPOLL+ |
| 18 | FPOLL- | 37 | |
| 19 | FRGND | | |

## **NT9X79AA** (continued)

The connector B (J3) pin numbers appears in the following table.

**NT9X79AA connector B pin numbers**

| Pin A | Name | Pin B | Name |
|---|---|---|---|
| 1 | FRGND | 20 | FRACK+ |
| 2 | FRACK- | 21 | FRRDY+ |
| 3 | FRRDY- | 22 | FWAIT+ |
| 4 | FWAIT- | 23 | Gnd |
| 5 | FPACK+ | 24 | FPACK- |
| 6 | FCLR+ | 25 | FCLR- |
| 7 | Gnd | 26 | IDTX+ |
| 8 | IDTX- | 27 | IDRX+ |
| 9 | IDRX- | 28 | Gnd |
| 10 | FREQ+ | 29 | FREQ- |
| 11 | — | 30 | — |
| 12 | — | 31 | — |
| 13 | — | 32 | — |
| 14 | — | 33 | — |
| 15 | — | 34 | — |
| 16 | Gnd | 35 | CLK8+ |
| 17 | CLK8- | 36 | Gnd |
| 18 | CLK56+ | 37 | CLK56- |
| 19 | FRGND | | |

The composite clock connector pin numbers appear in the following table.

**NT9X79AA composite clock pin numbers**

| Pin | Name |
|---|---|
| 1 | Shield |
| 2 | CCLKT |
| 6 | CCLKR |
| 7 | Shield |

The backplane connections pin numbers for the appear in the figure that follows section Technical data.

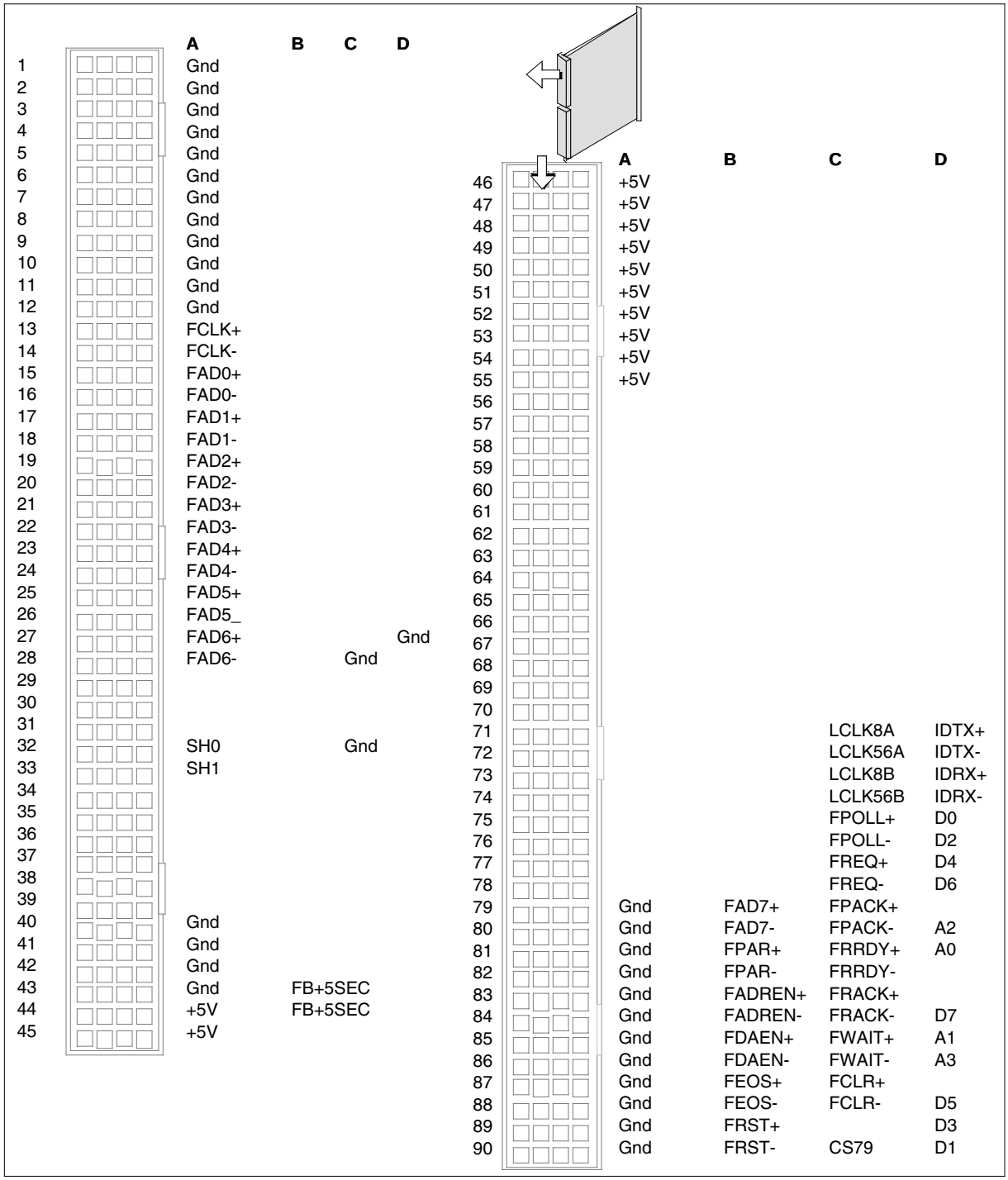
## Technical data

### Power requirements

The normal power requirements for the NT9X79AA from a +5V supply are 2.25W, to a maximum of 3.0W.

# **NT9X79AA** (end)

### NT9X79AA pin numbers



# NT9X79BA

## Product description

The NT9X79BA is a frame transport bus (F-bus) termination paddle board.

### Location

The NT9X79BA has two locations:

- behind the NT9X73AA card [rate adaptor (RA)] in the local message switch shelf (LMS)
- behind the NT9X74 card (F-bus repeater) in the bottom link interface shelf (LIS) of the link interface module (LIM)

## Functional description

The NT9X79BA has the following main functions:

- to terminate and distribute the differential intershelf F-bus
- to provide the termination and distribution for the DS-0 Composite Clock input to the link peripheral processor (LPP) frame

On the top shelf, the NT9X79BA provides the driving-end resistive termination for F-bus signals. The RA drives or receives these F-bus signals across the intershelf cables. The F-bus cables terminate on the NT9X79BA. All F-bus signals pass directly through these cables and the rate adaptor card through the NT9X79.

On the bottom shelf, the NT9X79BA provides the same function as the middle two shelves, with one exception. On the bottom shelf, termination resistors for the differential signals are present. The termination resistors are present because this version is the same as the version the top shelf uses.

### Functional blocks

The NT9X79BA has the following functional blocks:

- F-bus
- composite clock

## **NT9X79BA** (continued)

### Frame transport bus

In order for the NT9X79BA to work, the F-bus must perform the following tasks:

- provide a connection on each shelf for intershelf F-bus cables
- terminate intershelf F-bus cable signals (F-bus and DS-0 clock) to minimize reflections that the system does not require
- guarantee that the receiver views a high level on the bus when the bus is idle, for F-bus signals

The F-bus signals originate on the LMS transaction bus (T-bus). The RA differentially drives the F-bus signals across the bottom three shelves. The repeater converts these differential signals to single-ended levels, and drives the single-ended levels across the LIS backplane.

### Composite clock

For the NT9X79BA to work, the composite clock must perform the following tasks:

- provide a connection to the LIM for composite clock input
- convert the composite clock to differential signal levels for distribution to the bottom three LIS shelves
- convert differential DS-0 clock signal levels to single-ended levels for distribution on the LIS backplane
- terminate single-ended DS-0 clock signals at both ends of the LIS backplane

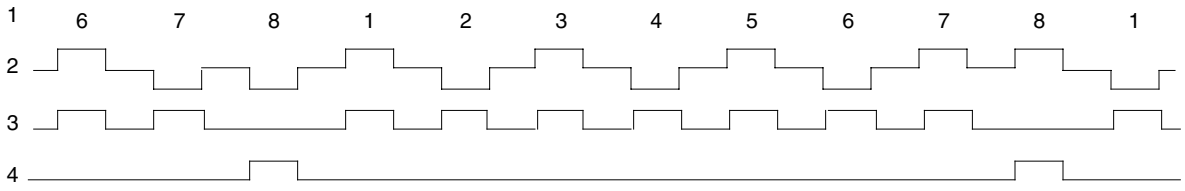
The composite clock input to the LIM provides the timing source for all DS-0 links to the LIM. The composite clock input to the LIM terminates on the NT9X79. The system converts the bipolar, balanced composite clock to differential. The system drives the bipolar, balanced composite clock across the F-bus cable through the NT9X79 to the three bottom shelves. The system drives the composite clock as a single-ended signal to the DS-0 paddle boards on each shelf.

## Signaling

### Timing

The timing for the NT9X79BA appears in the following figure.

**NT9X79BA timing**




**Legend**

1 Bit timer
2 Composite clock
3 56 clock
4 8 clock

**Note**: The composite clock input has a 5/8 duty cycle (high 5 to low 3).

## Pin numbers

The pin numbers for the F-bus connectors appear in the following table.

**NT9X79BA F-bus connector pin numbers (Sheet 1 of 2)**

| Pin A | Name | Pin B | Name |
|---|---|---|---|
| 1 | FRGND | 20 | FCLK+ |
| 2 | FCLK- | 21 | Gnd |
| 3 | FAD0+ | 22 | FAD0- |
| 4 | FAD1+ | 23 | FAD1- |
| 5 | FAD2+ | 24 | FAD2- |
| 6 | FAD3+ | 25 | FAD3- |
| 7 | Gnd | 26 | FAD4+ |
| 8 | FAD4- | 27 | FAD5+ |
| 9 | FAD5- | 28 | FAD6+ |
| 10 | FAD6- | 29 | FAD7+ |
| 11 | FAD7- | 30 | Gnd |
| 12 | FPAR+ | 31 | FPAR- |
| 13 | FADREN+ | 32 | FADREN- |

## **NT9X79BA** (continued)

**NT9X79BA F-bus connector pin numbers (Sheet 2 of 2)**

| Pin A | Name | Pin B | Name |
|---|---|---|---|
| 14 | FDAEN+ | 33 | FDAEN- |
| 15 | FEOS+ | 34 | FEOS- |
| 16 | Gnd | 35 | FRST+ |
| 17 | FRST- | 36 | FPOLL+ |
| 18 | FPOLL- | 37 | — |
| 19 | FRGND | | |

The following table lists the connector B (J3) pin number.

**NT9X79BA F-bus B pin numbers (Sheet 1 of 2)**

| Pin A | Name | Pin B | Name |
|---|---|---|---|
| 1 | FRGND | 20 | FRACK+ |
| 2 | FRACK- | 21 | FRRDY+ |
| 3 | FRRDY- | 22 | FWAIT+ |
| 4 | FWAIT- | 23 | Gnd |
| 5 | FPACK+ | 24 | FPACK- |
| 6 | FCLR+ | 25 | FCLR- |
| 7 | Gnd | 26 | IDTX+ |
| 8 | IDTX- | 27 | IDRX+ |
| 9 | IDRX- | 28 | Gnd |
| 10 | FREQ+ | 29 | FREQ- |
| 11 | — | —30 | — |
| 12 | — | —31 | — |
| 13 | — | —32 | — |
| 14 | — | —33 | — |
| 15 | — | —34 | — |

**NT9X79BA F-bus B pin numbers (Sheet 2 of 2)**

| Pin A | Name | Pin B | Name |
|---|---|---|---|
| 16 | Gnd | 35 | CLK8+ |
| 17 | CLK8- | 36 | Gnd |
| 18 | CLK56+ | 37 | CLK56- |
| 19 | FRGND | | |

The composite clock connector pin numbers appear in the following table.

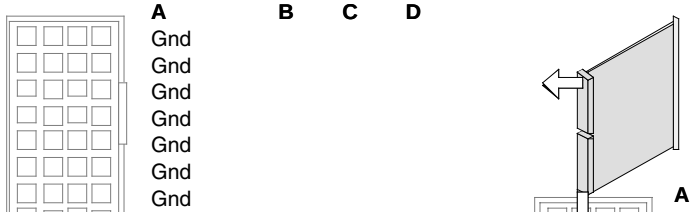
**NT9X79BA composite clock pin numbers**

| Pin | Name |
|---|---|
| 1 | Shield |
| 2 | CCLKT |
| 6 | CCLKR |
| 7 | Shield |

The backplane connection pin numbers for the NT9X79BA appear in the following figure.

# **NT9X79BA** (continued)

### NT9X79BA pin numbers



| | A | B | C | D |
|---|---|---|---|---|
| 1 | Gnd | | | |
| 2 | Gnd | | | |
| 3 | Gnd | | | |
| 4 | Gnd | | | |
| 5 | Gnd | | | |
| 6 | Gnd | | | |
| 7 | Gnd | | | |
| 8 | Gnd | | | |
| 9 | Gnd | | | |
| 10 | Gnd | | | |
| 11 | Gnd | | | |
| 12 | Gnd | | | |
| 13 | FCLK+ | | | |
| 14 | FCLK- | | | |
| 15 | FAD0+ | | | |
| 16 | FAD0- | | | |
| 17 | FAD1+ | | | |
| 18 | FAD1- | | | |
| 19 | FAD2+ | | | |
| 20 | FAD2- | | | |
| 21 | FAD3+ | | | |
| 22 | FAD3- | | | |
| 23 | FAD4+ | | | |
| 24 | FAD4- | | | |
| 25 | FAD5+ | | | |
| 26 | FAD5_ | | | |
| 27 | FAD6+ | | | Gnd |
| 28 | FAD6- | | Gnd | |
| 29 | | | | |
| 30 | | | | |
| 31 | | | | |
| 32 | SH0 | | Gnd | |
| 33 | SH1 | | | |
| 34 | | | | |
| 35 | | | | |
| 36 | | | | |
| 37 | | | | |
| 38 | | | | |
| 39 | | | | |
| 40 | Gnd | | | |
| 41 | Gnd | | | |
| 42 | Gnd | | | |
| 43 | Gnd | FB+5SEC | | |
| 44 | +5V | FB+5SEC | | |
| 45 | +5V | | | |

| | A | B | C | D |
|---|---|---|---|---|
| 46 | +5V | | | |
| 47 | +5V | | | |
| 48 | +5V | | | |
| 49 | +5V | | | |
| 50 | +5V | | | |
| 51 | +5V | | | |
| 52 | +5V | | | |
| 53 | +5V | | | |
| 54 | +5V | | | |
| 55 | +5V | | | |
| 56 | | | | |
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| 62 | | | | |
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| 65 | | | | |
| 66 | | | | |
| 67 | | | | |
| 68 | | | | |
| 69 | | | | |
| 70 | | | | |
| 71 | | | LCLK8A | IDTX+ |
| 72 | | | LCLK56A | IDTX- |
| 73 | | | LCLK8B | IDRX+ |
| 74 | | | LCLK56B | IDRX- |
| 75 | | | FPOLL+ | D0 |
| 76 | | | FPOLL- | D2 |
| 77 | | | FREQ+ | D4 |
| 78 | | | FREQ- | D6 |
| 79 | Gnd | FAD7+ | FPACK+ | |
| 80 | Gnd | FAD7- | FPACK- | A2 |
| 81 | Gnd | FPAR+ | FRRDY+ | A0 |
| 82 | Gnd | FPAR- | FRRDY- | |
| 83 | Gnd | FADREN+ | FRACK+ | |
| 84 | Gnd | FADREN- | FRACK- | D7 |
| 85 | Gnd | FDAEN+ | FWAIT+ | A1 |
| 86 | Gnd | FDAEN- | FWAIT- | A3 |
| 87 | Gnd | FEOS+ | FCLR+ | |
| 88 | Gnd | FEOS- | FCLR- | D5 |
| 89 | Gnd | FRST+ | | D3 |
| 90 | Gnd | FRST- | CS79 | D1 |

# Technical data

## Power requirements

The normal power requirements for the NT9X79BA from a +5V supply are 6.25W, to a maximum of 8.75W.

# NT9X79BB

## Product description

The NT9X79BB is the frame transport bus (F-bus) termination and extension paddle board. It serves as a physical interface to the intershelf F-bus cables, which provide communication between the local message switch (LMS) shelf and the link interface shelves (LIS) in the enhanced link peripheral processor (ELPP) cabinet.

### Location

The NT9X79BB paddle board is located behind the NT9X73BB (triple rate adapter) card in the LMS of the link interface module (LIM) shelf in the ELPP cabinet.

## Functional description

The NT9X79BB paddle board has the following main functions:

- to terminate and distribute the intershelf frame transport bus (F-bus) signaling
- to provide the termination and distribution for the DS-0 composite clock input to the ELPP frame

The NT9X79BB paddle board provides the same functionality as the BA version, with one minor difference. The quarter key location in the NT9X79BB paddle board (field H8) is changed because the paddle board occupies a different slot in the ELPP cabinet than in other cabinets.

### Functional blocks

NT9X79BB has the following functional blocks:

- F-bus
- composite clock

#### Frame transport bus

The NT9X79BB paddle board provides connection for intershelf F-bus cables on the LIM shelf. Intershelf F-bus cable signals terminate on the NT9X79BB paddle board. The F-bus signals originate on the LMS transaction bus (T-bus) and are differentially driven by the NT9X73BB (triple rate adapter) card to three LISs. The NT9X74DA (F-bus repeater) card converts these signals to single-ended levels and drives them across the LIS backplane.

#### Composite clock

The NT9X79BB paddle board terminates the composite clock input to the LIM. This bipolar, balanced composite clock input is converted to a differential and driven across the F-bus cable through the NT9X79BB paddle

board to three LISs. On each LIS, the composite clock is driven as a single-ended signal to the DS-1 paddle board.

## Signaling

There are four connectors on the NT9X79BB card. The face plate has three windows where connectors are placed, and the backplane connector provides the LIS backplane connection.

### Pin outs

The intershelf F-bus uses two 37-pin connectors: connector A and connector B. Connector C is provided for termination of the composite clock input. The pin outs for these three connectors are listed in the following tables.

The following table lists the F-bus connector A pin outs.

**NT9X79BB F-bus connector A pin outs (Sheet 1 of 2)**

| Pin A | Name | Pin B | Name |
|---|---|---|---|
| 1 | FRGND | 20 | FCLK+ |
| 2 | FCLK- | 21 | GND |
| 3 | FAD0+ | 22 | FAD0- |
| 4 | FAD1+ | 23 | FAD1- |
| 5 | FAD2+ | 24 | FAD2- |
| 6 | FAD3+ | 25 | FAD3- |
| 7 | GND | 26 | FAD4+ |
| 8 | FAD4- | 27 | FAD5+ |
| 9 | FAD5- | 28 | FAD6+ |
| 10 | FAD6- | 29 | FAD7+ |
| 11 | FAD7- | 30 | GND |
| 12 | FPAR+ | 31 | FPAR- |
| 13 | FADREN+ | 32 | FADREN- |
| 14 | FDAEN+ | 33 | FDAEN- |
| 15 | FEOS+ | 34 | FEOS- |

## **NT9X79BB** (continued)

**NT9X79BB F-bus connector A pin outs (Sheet 2 of 2)**

| Pin A | Name | Pin B | Name |
|---|---|---|---|
| 16 | GND | 35 | FRST+ |
| 17 | FRST- | 36 | FPOLL+ |
| 18 | FPOLL- | 37 | - |
| 19 | FRGND | | |

The following table lists the F-bus connector B pin outs.

**NT9X79BB F-bus connector B pin outs (Sheet 1 of 2)**

| Pin A | Name | Pin B | Name |
|---|---|---|---|
| 1 | FRGND | 20 | FRACK+ |
| 2 | FRACK- | 21 | FRRDY+ |
| 3 | FRRDY- | 22 | FWAIT+ |
| 4 | FWAIT- | 23 | GND |
| 5 | FPACK+ | 24 | FPACK- |
| 6 | FCLR+ | 25 | FCLR_ |
| 7 | GND | 26 | IDTX+ |
| 8 | IDTX- | 27 | IDRX+ |
| 9 | IDRX- | 28 | GND |
| 10 | FREQ+ | 29 | FREQ- |
| 11 | - | 30 | - |
| 12 | - | 31 | - |
| 13 | - | 32 | - |
| 14 | - | 33 | - |
| 15 | - | 34 | - |
| 16 | GND | 35 | CLK8+ |
| 17 | CLK8- | 36 | GND |

**NT9X79BB F-bus connector B pin outs (Sheet 2 of 2)**

| Pin A | Name | Pin B | Name |
|---|---|---|---|
| 18 | CLK56+ | 37 | CLK56- |
| 19 | FRGND | | |

The following table lists the composite clock connector pin outs.

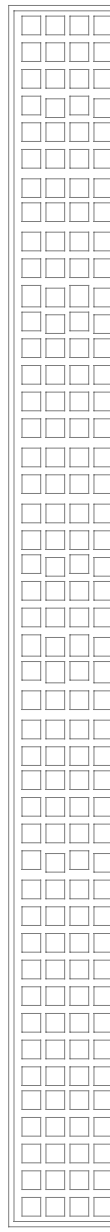
**NT9X79BB composite clock connector pin outs**

| Pin | Name |
|---|---|
| 1 | Shield |
| 2 | CCLKT |
| 6 | CCLKR |
| 7 | Shield |

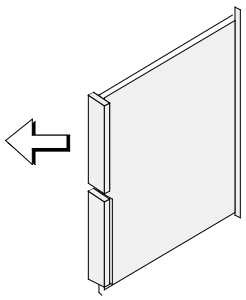
The following figure shows the backplane pin outs for NT9X79BB.

# **NT9X79BB** (continued)

### NT9X79BB pin outs (part 1 of 2)



| | A | | B | C | D |
|---|---|---|---|---|---|
| 1 | GND | | | | |
| 2 | GND | | | | |
| 3 | GND | | | | |
| 4 | GND | | | | |
| 5 | GND | | | | |
| 6 | GND | | | | |
| 7 | GND | | | | |
| 8 | GND | | | | |
| 9 | GND | | | | |
| 10 | GND | | | | |
| 11 | GND | | | | |
| 12 | GND | | | | |
| 13 | FCLK+ | IO1 | | | |
| 14 | FCLK- | IO2 | | | |
| 15 | FAD0+ | IO3 | | | |
| 16 | FAD0- | IO4 | | | |
| 17 | FAD1+ | IO5 | | | |
| 18 | FAD1- | IO6 | | | |
| 19 | FAD2+ | IO7 | | | |
| 20 | FAD2- | IO8 | | | |
| 21 | FAD3+ | IO9 | | | |
| 22 | FAD3- | IO10 | | | |
| 23 | FAD4+ | IO11 | | | |
| 24 | FAD4- | IO12 | | | |
| 25 | FAD5+ | IO13 | | | |
| 26 | FAD5- | IO14 | | | |
| 27 | FAD6+ | IO15 | | | GND |
| 28 | FAD6- | IO16 | | GND | |
| 29 | | | | | |
| 30 | | | | | |
| 31 | | | | | |
| 32 | SH0 | | | GND | |
| 33 | SH1 | | | | |
| 34 | | | | | |
| 35 | | | | | |
| 36 | | | | | |
| 37 | | | | | |
| 38 | | | | | |
| 39 | | | | | |
| 40 | GND | | | | |
| 41 | GND | | | | |
| 42 | GND | | | | |
| 43 | GND | | FB+5SEC | | |
| 44 | +5 V | | FB+5SEC | | |
| 45 | +5 V | | | | |



**NT9X79BB pin outs (part 2 of 2)**

| | A | B | | C | | D | |
|---|---|---|---|---|---|---|---|
| 46 | +5 V | | | | | | |
| 47 | +5 V | | | | | | |
| 48 | +5 V | | | | | | |
| 49 | +5 V | | | | | | |
| 50 | +5 V | | | | | | |
| 51 | +5 V | | | | | | |
| 52 | +5 V | | | | | | |
| 53 | +5 V | | | | | | |
| 54 | +5 V | | | | | | |
| 55 | +5 V | | | | | | |
| 56 | | | | | | | |
| 57 | | | | | | | |
| 58 | | | | | | | |
| 59 | | | | | | | |
| 60 | | | | | | | |
| 61 | | | | | | | |
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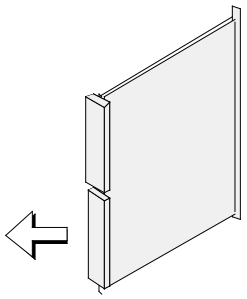
| 64 | | | | | | | |
| 65 | | | | | | | |
| 66 | | | | | | | |
| 67 | | | | | | | |
| 68 | | | | | | | |
| 69 | | | | | | | |
| 70 | | | | | | | |
| 71 | | | | LCLK8A | IO65 | IDTX+ | IO61 |
| 72 | | | | LCLK56A | IO66 | IDTX- | IO62 |
| 73 | | | | LCLK8B | IO67 | IDRX+ | IO63 |
| 74 | | | | LCLK56B | IO68 | IDRX- | IO64 |
| 75 | | | | FPOLL+ | E01 | D0 | IO45 |
| 76 | | | | FPOLL- | E02 | D2 | IO46 |
| 77 | | | | FREQ+ | E03 | D4 | IO47 |
| 78 | | | | FREQ- | E04 | D6 | IO48 |
| 79 | GND | FAD7+ | IO17 | FPACK+ | E05 | | |
| 80 | GND | FAD7- | IO18 | FPACK- | E06 | A2 | IO50 |
| 81 | GND | FPAR+ | IO19 | FRRDY+ | E07 | A0 | IO51 |
| 82 | GND | FPAR- | IO20 | FRRDY- | E08 | | |
| 83 | GND | FADREN+ | IO21 | FRACK+ | E09 | | |
| 84 | GND | FADREN- | IO22 | FRACK- | E10 | D7 | IO54 |
| 85 | GND | FDAEN+ | IO23 | FWAIT+ | E11 | A1 | IO55 |
| 86 | GND | FDAEN- | IO24 | FWAIT- | E12 | A3 | IO56 |
| 87 | GND | FEOS+ | IO25 | FCLR+ | E13 | | |
| 88 | GND | FEOS- | IO26 | FCLR- | E14 | D5 | IO58 |
| 89 | GND | FRST+ | IO27 | | | D3 | IO59 |
| 90 | GND | FRST- | IO28 | CS79 | IO44 | D1 | IO60 |



# Technical data

## Power requirements

The NT9X79BB requires 6.25 W of power up to maximum of 8.75 W.

# NT9X80CA

## Product description

The NT9X80CA application processor cabinet (APC) is an improved version of the current NT9X01 1.07 m (42 in.) cabinet. The NT9X80CA meets global regulatory and customer specifications. These specifications include compliance with electromagnetic interference (EMI) standards and alignment with FiberWorld.

The DMS SuperNode core handles call processing and switch-based application software. The APC is designed for the functions of the DMS SuperNode. The APC provides additional processing and storage capacity. This capacity allows applications like DMS service control point (SCP) II and billing server.

Components in the APC communicate over fiber links through the DMS-bus message switch. An Ethernet interface in the link interface shelf provides input/output (I/O) functions. The APC has computing resources and mass storage devices.

The NT9X80CA cabinet contains three types of APC shelves that can be provisioned. The following sections describe the APC shelves.

### Application processor

The application processor (AP) is a general purpose, dual-plane computing device with provisionable central processing unit (CPU) and memory.

### File processor

The file processor (FP) is an AP. A small computer system interface (SCSI) port replaces one of the memory slots. The SCSI provides an interface to the storage devices.

### Storage device

Many of SCSI-compatible storage devices (SD) can be provisioned. Currently, a 600-Mbyte hard disk drive and a 1.3-Gbyte digital audio tape (DAT) drive is available.

The three shelf positions in the APC can be provisioned. The APC always includes the AP and FP shelf in shelf position 39. On an AP shelf, each half-shelf supports one dual plane AP or FP. On an SD shelf, each quarter-shelf (quadrant) supports a single storage device. The AP and SD shelves do not always require use. In a half-shelf, each AP and FP plane or SD receives power from a different feed (A or B).

### SCSI bus configuration

Each FP connects to one or more SDs through a daisy chain SCSI bus arrangement. In this arrangement, a cable runs from the SCSI port on a paddle board (PB) at the rear of the FP to the PB of the first SD in the chain. Cabling or backplane connections, or both, chain together paddle boards on subsequent SDs. The last SD in the chain is cabled back to back to the FP. This SD terminates on the same PB from which the chain began. This method allows several FPs with separate SD chains of different sizes to be configured in a single cabinet.

## Parts

The NT9X80CA cabinet contains the following parts:

- A0382101—frame supervisory panel, -48V (dc)
- A0382102—core cooling unit, -60V (dc)
- NT0X24BD—blank shelf
- NT9X03BA—SuperNode frame supervisory panel, -60V (dc)
- NT9X8101—application processor shelf
- NT9X8301—storage device shelf
- NT9X01FB—filler faceplate

### SuperNode frame supervisory panel

The A0382101 -48V (dc) or NT9X03BA -60V (dc) SuperNode frame supervisory panel (FSP) provides alarm, maintenance, and additional supervisory functions. The FSP is in the top shelf in the NT9X80CA. You must open cabinet doors to access or view the front and rear faces of the A0382101 or NT9X03BA. The frame alarm light in the cabinet is visible when you close the doors.

Power from the power distribution center frame enters the FSP. The system distributes this power to different power supply modules in the cabinet. These power supply modules include the NTDX15AB and NT9X91AB power converters. The power supply modules contain all power control. The power control is separate from the FSP.

### Core cooling unit

The core cooling unit (CU) provides mechanical ventilation for equipment that the APC contains. The CU is provisioned for dc voltages of -48V (A0382101) or -60V (A0382102). The voltage amount depends on the power requirement.

## NT9X80CA (continued)

### Blank shelf

The NT0X24BD blank shelf fills in any shelf position when a shelf is not in use.

### Application processor shelf

The NT9X8101 shelf assembly contains the following cards:

- NTDX15AB—APC power converter
- NT9X13LA—AP/FP 68030 HPM-based CPU card
- NT9X14DB—memory 24-Mbyte card (handshake override)
- NT9X21AB—bus terminator PB
- NT9X26AB—remote terminal interface PB
- NT9X62AA—two-port subrate DS512 PB
- NT9X86AA—dual-port message controller card
- NT9X87AA—dual-access buffer memory card
- NT9X88AA—SCSI interface processor PB

### Storage device shelf

The NT9X8301 shelf assembly contains the following cards:

- NT9X89AA—SCSI device interface PB
- NT9X89BA—SCSI device interface PB
- NT9X90AA—600-Mbyte disk storage unit card
- NT9X90BA—1.3-Gbyte DAT storage unit card
- NT9X91AB—SD power converter card

### Filler faceplate

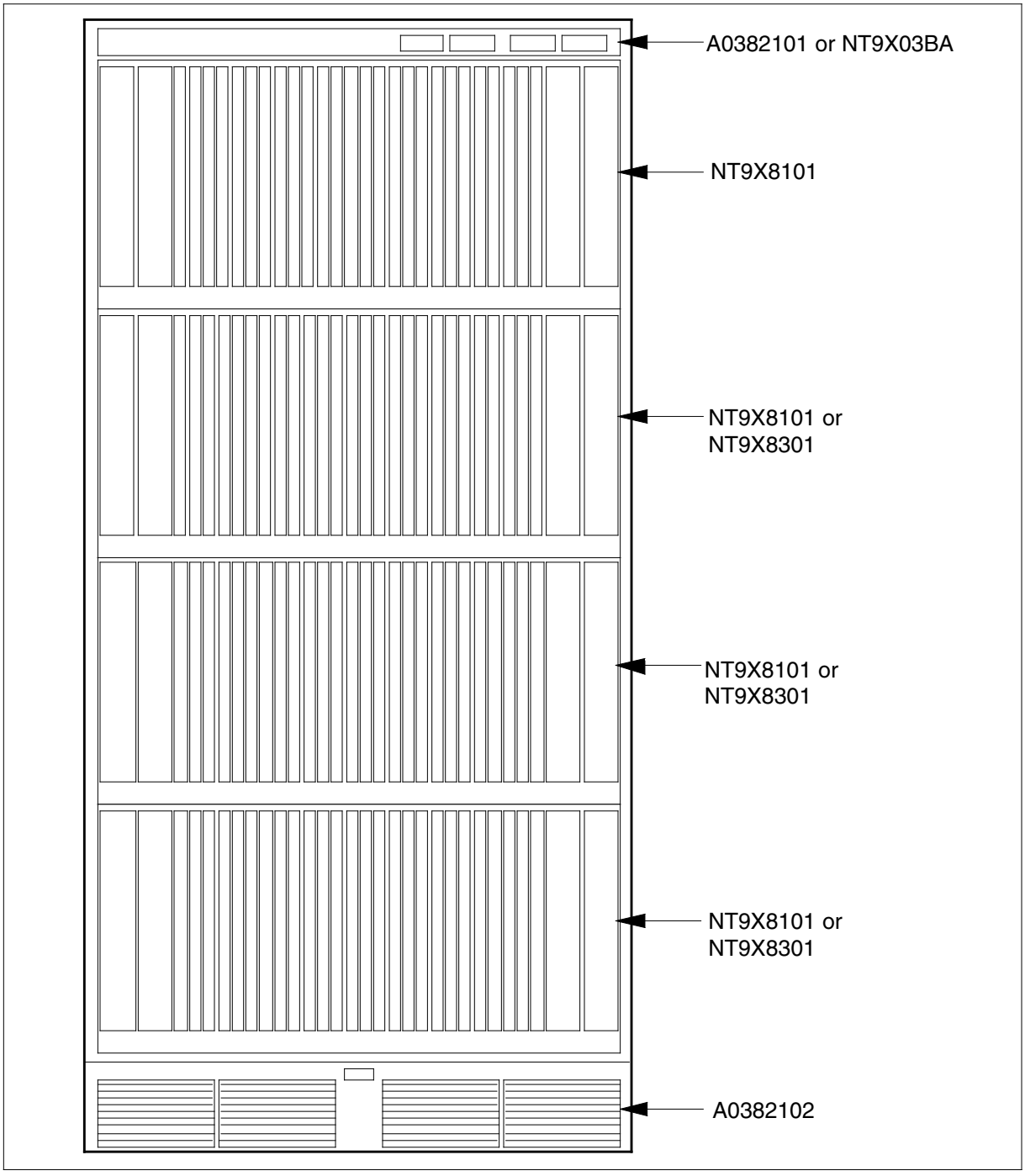
The NT9X01FB filler faceplate is in a shelf. This shelf does not contain application processors, file processors, or storage devices. This condition satisfies the forced-air cooling requirements of the cabinet.

## Design

The design of the application processor cabinet appears in the following diagram.

# **NT9X80CA** (end)

**NT9X80CA parts**



# NT9X84AA

## Product description

The NT9X84AA forms the technological base and architecture to provide the flexible access structure products in the SuperNode group.

### Location

The NT9X84AA occupies a slot in an application-specific unit shelf of a link peripheral processor (LPP) cabinet. The LPP is part of the data communications processor.

## Functional description

The main functions of the NT9X84AA are as follows:

- temporary storage of incoming/outgoing link messages
- protocol management and handshaking for Ethernet carrier sense multiple access/collision detect (CSMA/CD)
- generation of correct voltage and impedance levels to drive standard twisted-pair drop cable signal lines

### Functional blocks

The NT9X84AA contains the following functional blocks:

- processor bus (P-bus) decode/control
- software (S/W) timer
- card registers
- identification (ID) PROM
- P-bus interface
- P-bus/shared bus latch/state machine
- RAM
- local area network controller (LANCE) bus (L-bus)/shared bus latch/state machine
- P-bus/L-bus latch/state machine
- arbiter
- allocator
- LANCE chip
- SIA chip
- clock distribution

### Processor bus decode/control

This block performs the following functions:

- decodes addresses
- latches address and data
- times asynchronous bus transactions to local clock again
- controls P-bus and internal control signals to permit byte, aligned word and aligned longword accesses to compatible locations

### Software timer

The S/W timer provides higher resolution process monitoring.

### Card registers

Card registers control different card operation and maintenance characteristics.

### Identification PROM

The identification PROM block allows the card to conform to the standard SuperNode ID PROM definition. Identification and vintage information is carried to the processor to allow correct initialization and ease of maintenance.

### Processor bus interface

The P-bus interface provides a path to the paddleboard for future enhancements.

### Processor bus/shared bus latch/state machine

This block provides the following:

- a gateway for the processor to read/write into high-speed RAM over the shared bus
- rate conversion between buses and single-state buffering
- control of internal card control signals to coordinate transfers
- generation and checks of processor-side RAM parity

### RAM

The RAM provides temporary storage of incoming and outgoing link messages, LANCE chip initialization parameters and individual message descriptor rings.

## NT9X84AA (continued)

### LANCE bus/shared bus latch/state machine

This block provides the following:

- a gateway for LANCE chip DMA accesses to and from high-speed RAM over the shared bus
- multiplexed and demultiplexed combined address and data buses of the LANCE chip
- rate conversion between the two buses
- single-state buffering
- control of the internal card control signals to coordinate transfers
- generation and checks of LANCE-side RAM parity

### Processor bus/LANCE bus latch/state machine

This block provides the following:

- a gateway to allow processor access to LANCE chip internal registers
- multiplexed and demultiplexed LANCE chip combined address and data buses
- control of internal card control signals to coordinate transfers

### Arbiter

The artiber performs the arbitration control function for the LANCE bus.

### Allocator

The allocator distributes the available bandwidth of the shared bus between users. A time multiplexed shared bus and the allocation of known time slots is an alternative to arbitration.

### LANCE chip

The LANCE chip provides link and data control functions like data buffer management and support of the CSMA/CD link protocol.

### SIA chip

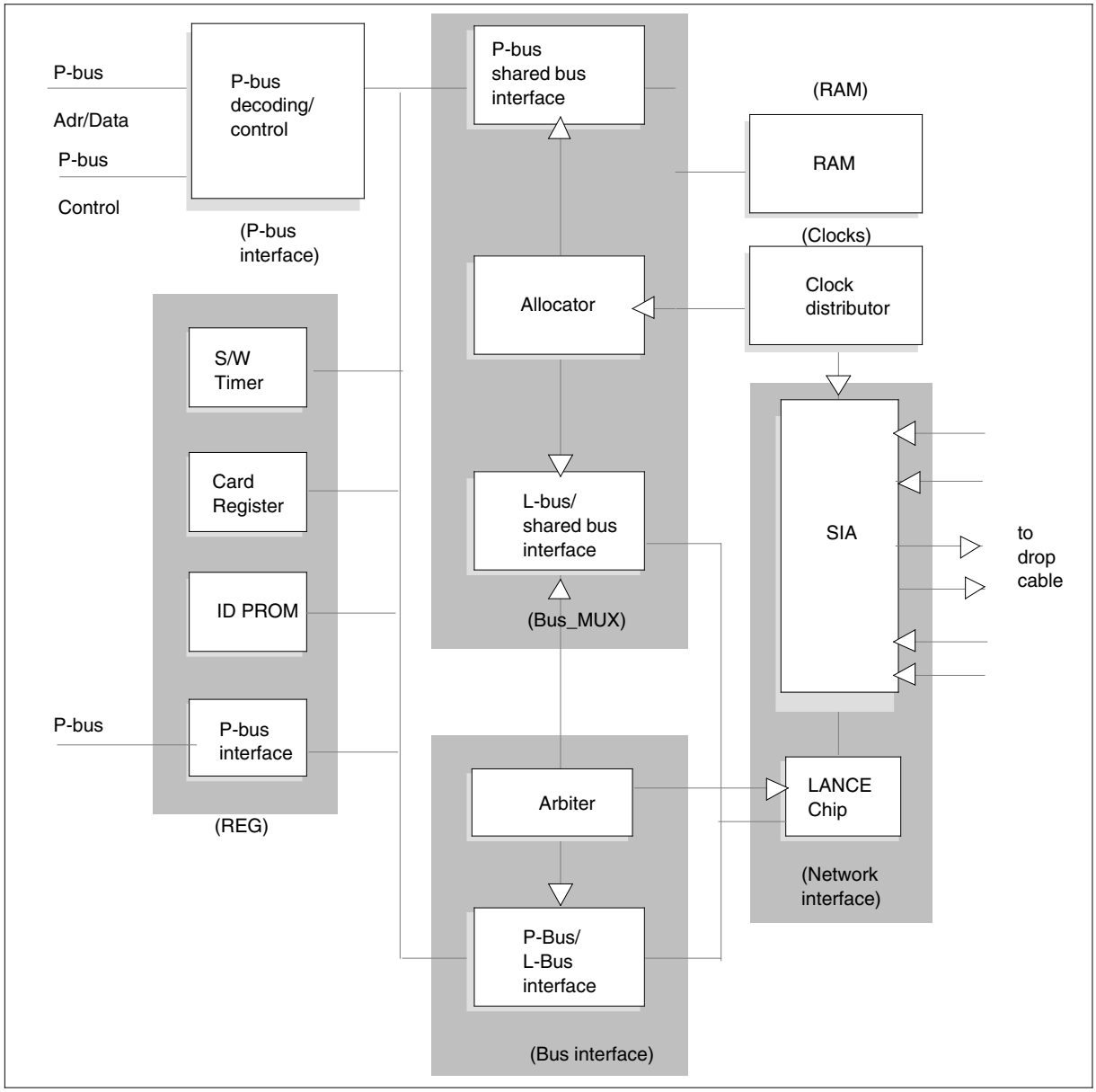
The SIA chip is the companion device to the LANCE chip.

### Clock distribution

Clock distribution is a transmit source for SIA. Clock distribution is a common time reference. All data control state machines use clock distribution.

The relationship between the functional blocks appears in the following figure.

**NT9X84AA functional blocks**



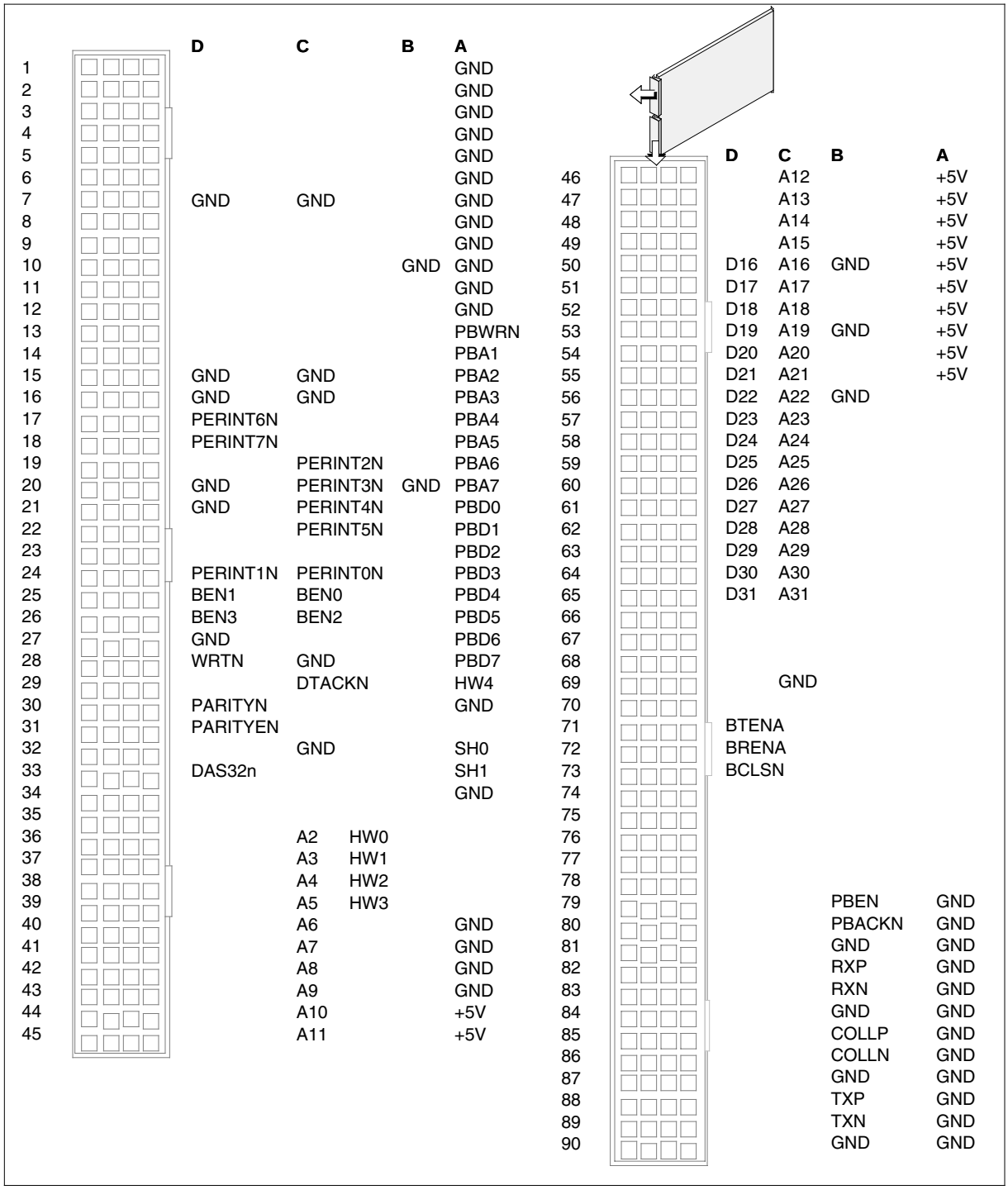

# Signaling

## Pin numbers

The pin numbers for NT9X84AA appear in the following figure.

# **NT9X84AA** (end)

### NT9X84AA pin numbers



# NT9X85AA

## Product description

The NT9X85AA Ethernet attachment unit interface (AUI) paddle board (EIP) provides an interface between the NT9X85AA mother board, the Ethernet interface card (EIC) and the AUI cable. All transactions between the EIC and EIP are directed through a 31-pin bus. This bus is dedicated to communications between the mother board and the paddle board. Access the local area network (LAN) through standard Ethernet connector hardware and appropriate AUI cabling. Standard media attachment units (MAU) provide an interface to the Ethernet network which allows AUI interface to coaxial or twisted-pair LANs.

## Functional description

The NT9X85AA provides a physical interface between the Ethernet MAU and the EIC. The NT9X85AA provides power to the MAU.

### Functional blocks

The NT9X85AA contains the following functional blocks:

- 5V-to-12V converter
- MAU power-failure detect
- power-up detect
- status register
- configuration (config) register
- EIC-to-EIP interface
- line interface connector
- loopback point
- decoder
- identification (ID) PROM
- acknowledgment generator (ACK GEN)
- light-emitting diodes (LED)

### 5V-to-12V converter

This block receives 5V as input and outputs 12V as ground for all currents from 0 to 500 mA. The 5V ground to the converter is separate from on-board logic component ground.

## **NT9X85AA** (continued)

### Media attachment units power-failure detect

This block asserts a signal when the converter voltage output falls below 1.2V or when power to the MAU is shorted.

### Power-up detect

This block asserts a power-up bit after the detection of on-board powering. Power hits or a card inserted in the card designation slot cause a power-up.

### Status register

The status register stores on-board characteristics. Relay error bits can be read. The power-up detect bit and converter failure detect bit can be read and cleared.

### Configuration register

When the configuration register is set, the board can be configured into loopback or non-loopback mode. Read/write operations are possible.

### EIC-to-EIP interface

This block contains a 31-pin bus dedicated to input/output operations between the mother board and paddle board. All signal buffering is implemented on the EIC.

### Line interface connector

This block is a 25-pin receptacle shell plated with conductive material. This block makes sure the current path from the cable shield to the chassis has integrity. Ethernet shielded cable links the MAU to the EIP through the line interface connector.

### Loopback point

The LAN controller (LANCE) chip used on the EIC features an external loopback option. This option allows full duplex mode operation to perform data path integrity tests. A software accessible register permits loopback or non-loopback EIP configurations. The loopback point links DATA IN signals to DATA OUT signals when the EIP is configured in loopback mode. For non-loopback operations, the DATA IN and DATA OUT signals link to the MAU. The COLLISION IN signals open to indicate collision-free status.

### Decoder

Element block decoding uses standard decoding schemes. Elements that can be decoded are the status register, ID PROM and config register.

### Acknowledgment generator

An acknowledge is generated when data is valid during read cycles or when data has been properly stored during write cycles. The EIC receives this

acknowledge. The EIC transmits the acknowledge again as a DTACK to the processor.

### Light-emitting diodes

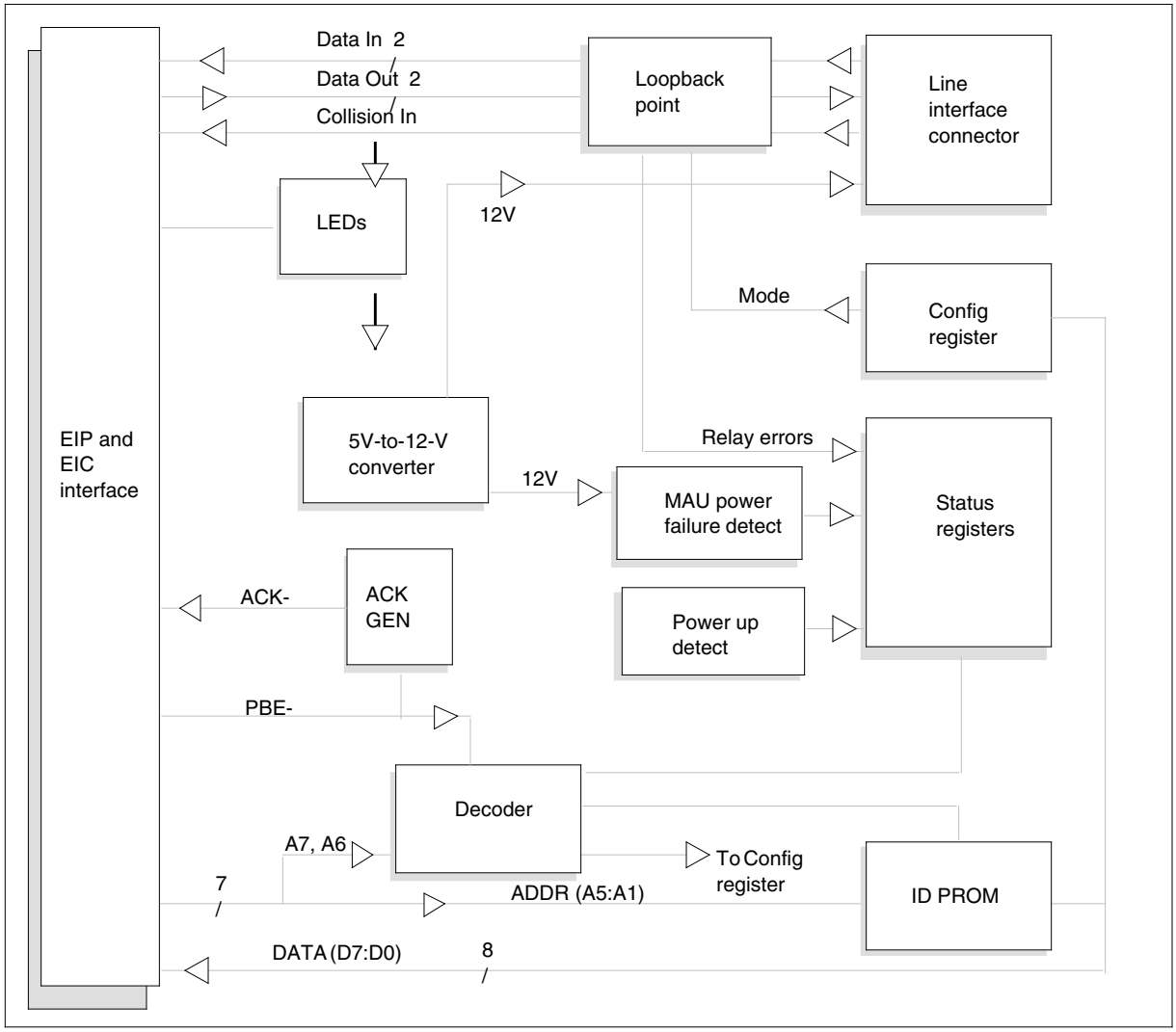
Four LEDs use signals that originate at the LANCE chip of the EIC to monitor Ethernet activity. The LEDs perform the following functions:

- transmit - green LED glows when the EIC LANCE chip asserts the Transmit Enable
- receive - yellow LED glows when the EIC LANCE chip asserts the Receive Enable
- collision presence - red LED glows when the EIC LANCE chip asserts Collision. This action occurs if Transmit Enable or Receive Enable is currently active.
- signal quality error - green LED glows when the EIC LANCE chip asserts Collision. This action occurs if Transmit Enable and Receive Enable are currently active.

The relationship between the functional blocks appears in the following figure.

## **NT9X85AA** (continued)

**NT9X85AA functional blocks**



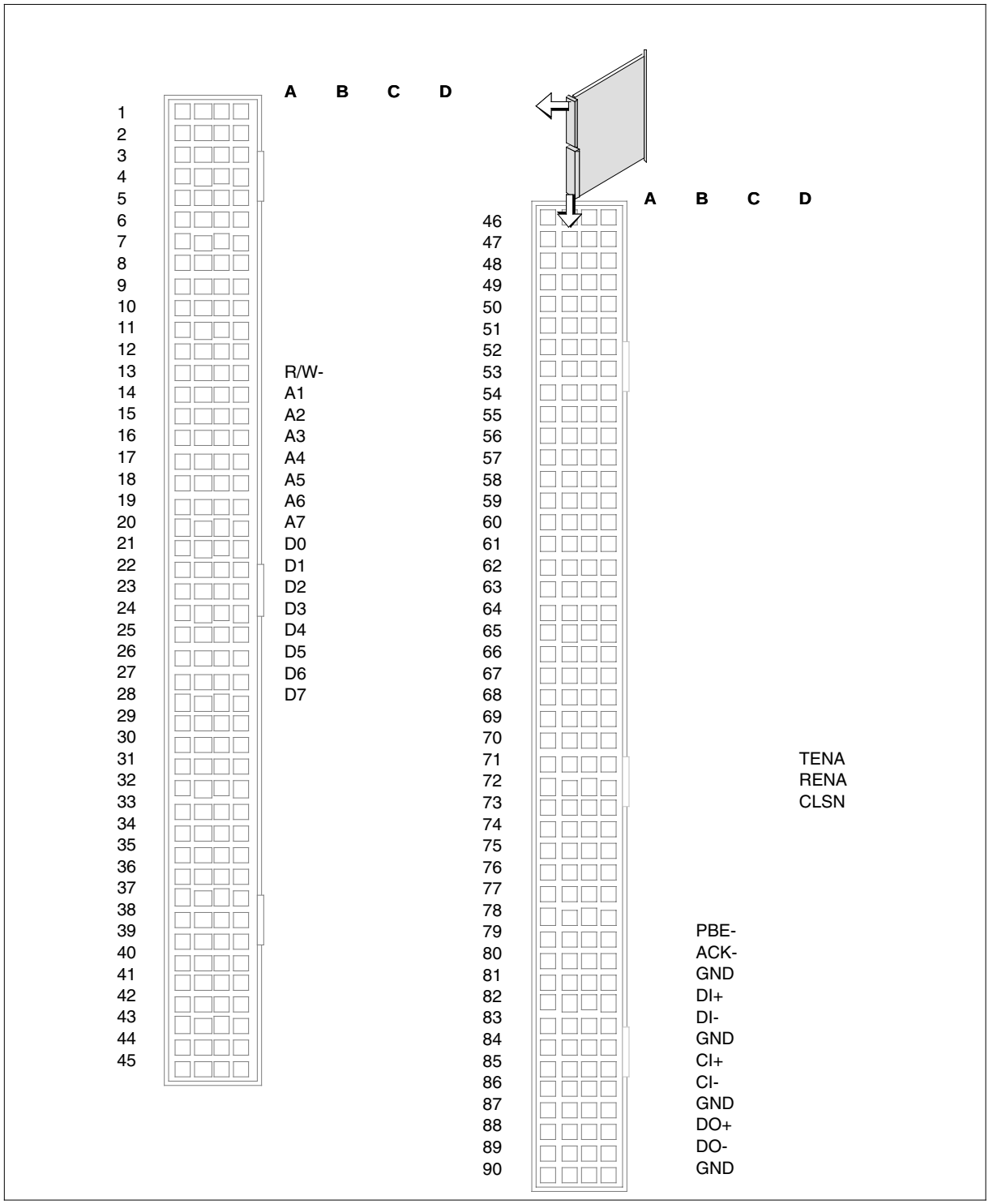

# Signaling

### Pin numbers

The pin numbers for the EIC-to-EIP interface appear in the following figure.

# **NT9X85AA** (continued)

### NT9X85AA EIC-to-EIP interface pin numbers



## **NT9X85AA** (continued)

The pin numbers for the EIC-to-MAU interface appear in the following table.

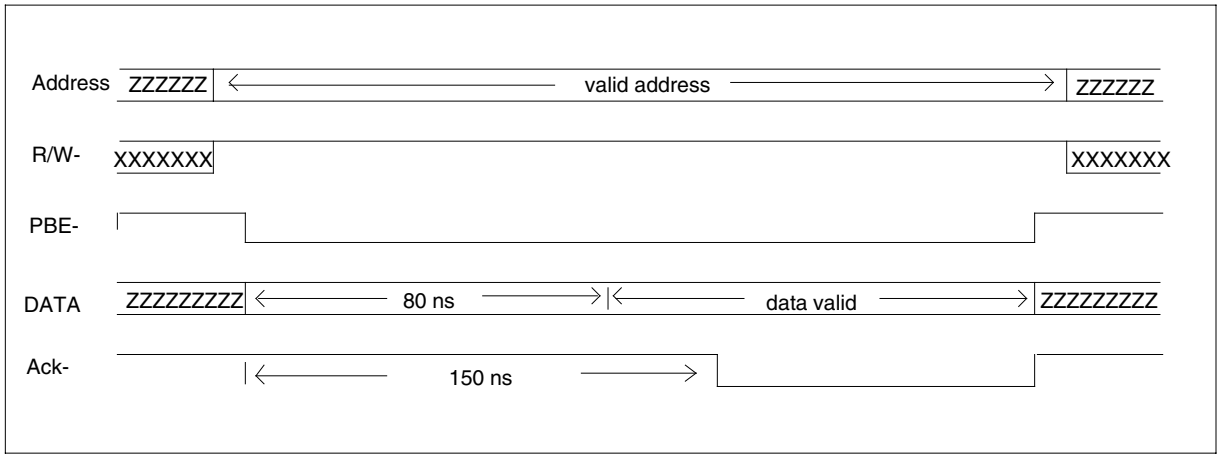
**NT9X85AA EIC-to-MAU interface pin numbers**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 3 | DO+ | 8 | CO Sh |
| 15 | DO | -2 | CI+ |
| 16 | DO Sh | 14 | CI |
| 5 | DI+ | 1 | CI Sh |
| 12 | DI | -6 | Vc |
| 4 | DI Sh | 18 | VP |
| 7 | CO+ | 19 | VS |
| 20 | C0 | -shell | PG |

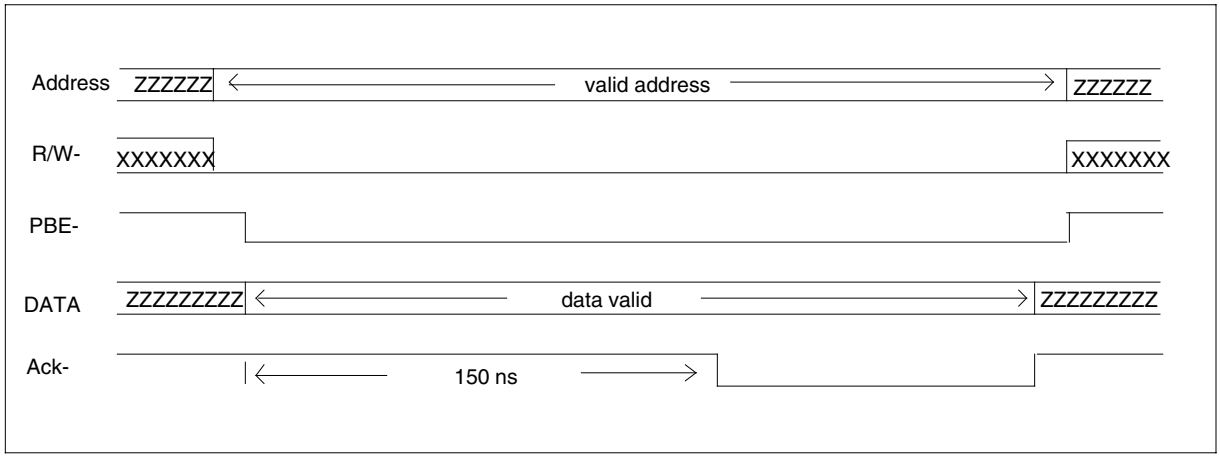
### Timing

The timing requirements for the NT9X85AA appear in the following figures.

**NT9X85AA read cycle timing**



**NT9X85AA write cycle timing**




# Technical data

## Electrical specifications

The address and data lines on the EIP are buffered on the EIC. When the EIP is not accessed, these buffers are set to high-impedance state. The address and data lines on the EIP are pulled high to minimize electrical activity that is not necessary.

# NT9X86AA

## Product description

The NT9X86AA has a link paddle board. The NT9X86AA provides two serial message communications links to the DMS–bus from:

- a computing module
- an applications processor module
- a file processor module

## Functional description

The main functions of the NT9X86AA are as follows:

- provides a maximum of two high–bandwidth communications links to the DMS–bus through the message switch
- provides a local time–of–day (TOD) clock for applications that run in a computing module environment, a file processor or an applications processor

### Functional blocks

The NT9X86AA contains the following functional blocks:

- message control
- split mode register (SMR)
- command and status registers
- TOD clock
- paddle board interface
- identification (ID) PROM
- reset
- subsystem clock (SSC) diagnostics
- parity
- interrupt
- bus interface

### Message control

The message control block provides two virtual message ports that interface to two subrate DS512 communication links.

### Split mode register

The SMR block provides the following:

- generation of the path control signals required to split off the ports on a dual–port message controller (DPMC) on the inactive plane
- physical address to insert in header field of outgoing DMSY messages to the link on both ports in a split–mode CPU

### Command and status registers

The command and status registers block controls the operation of the message hardware.

### Time–of–day clock

The TOD clock block provides a real–time clock. Applications that require an accurate timing element can reference this clock.

### Paddle board interface

The paddle board interface block provides buffered processor access to the addressable paddle board functions.

### Identification PROM

The ID PROM block provides circuit element identification information for the dual–port message control card.

### Reset

The reset block provides a reset function for the card hardware. The block provides a power–up reset and a software reset.

### Subsystem clock diagnostics

The subsystem clock (SSC) diagnostics block provides a diagnostics interface to the 9X22 clock card.

### Parity

The parity block calculates parity on all processor bus (P–bus) transactions. This block calculates parity on transactions originated by the dual–port message control mate card originates over the crossover bus.

### Interrupt

The interrupt block provides interrupt capability for data input and output and for message controller errors.

## **NT9X86AA** (continued)

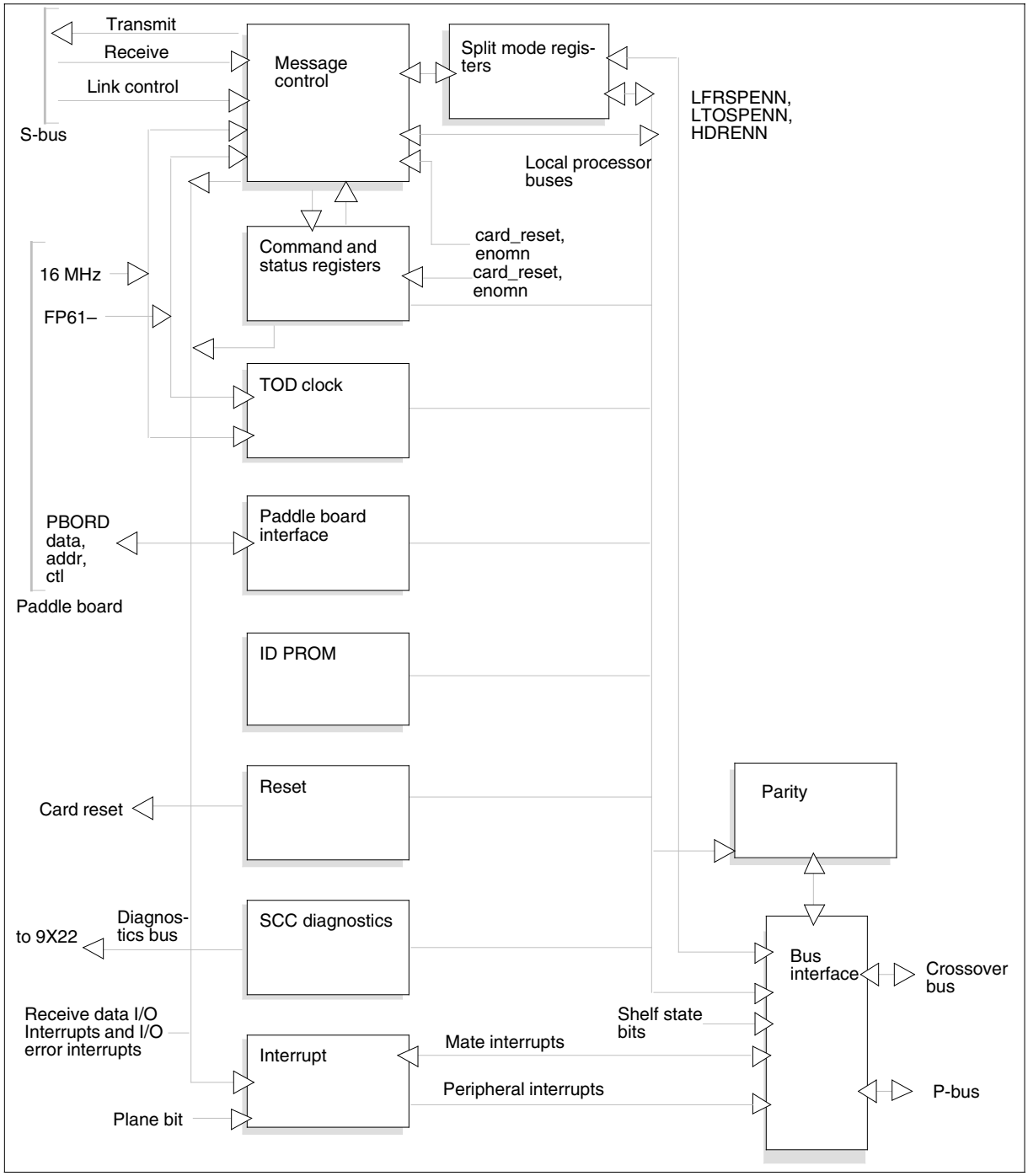
### Bus interface

The bus interface block provides an interface between the P–bus and the local processor buses. The bus interface provides an interface between the crossover bus and the local processor buses. This block also decodes addresses.

The relationship between these functional blocks appears in the following figure.

# **NT9X86AA** (continued)

### NT9X86AA functional blocks



## **NT9X86AA** (continued)

# Signaling

### Pin numbers

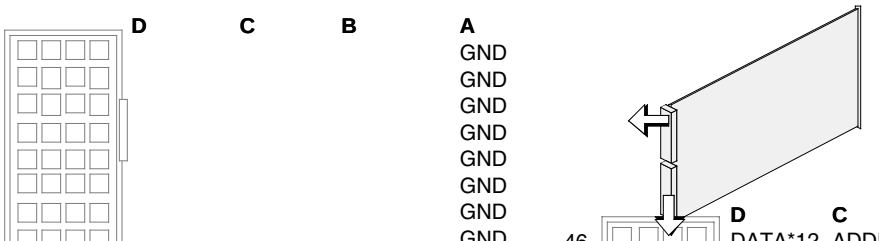
The pin numbers for the NT9X86AA appear in the following figure.

### Timing

The timing figures for the NT9X86AA follow the pin number figure.

# **NT9X86AA** (continued)

### NT9X86AA pin numbers



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | GND |
| 2 | | | | GND |
| 3 | | | | GND |
| 4 | | | | GND |
| 5 | | | | GND |
| 6 | | | | GND |
| 7 | | | | GND |
| 8 | | | | GND |
| 9 | | | | GND |
| 10 | | | | GND |
| 11 | | INT*4– | | GND |
| 12 | | | | GND |
| 13 | | | | PENB– |
| 14 | | | | PWRT– |
| 15 | PLN*– | | CLK*1 | PDTACK– |
| 16 | | | CLK*2 | C244 |
| 17 | | | CLK*3 | PADDR0 |
| 18 | PEINT*7– | | CLK*4 | PADDR1 |
| 19 | | | CLK*5 | PADDR2 |
| 20 | | PEINT*3– | CLK*6 | PADDR3 |
| 21 | | | CLK*7 | DREN |
| 22 | | PEINT*5– | CLK*8 | PADDR4 |
| 23 | | | TMTINT–* | PADDR5 |
| 24 | PEINT*1– | | FMTINT–* | |
| 25 | BEN*1– | BEN*0– | TMRINT–* | |
| 26 | BEN*3– | BEN*2– | FMRINT–* | |
| 27 | GND | | TSPLEN–* | |
| 28 | WRT*– | GND | FSPLEN–* | |
| 29 | EDTACK*– | DTACK*– | ENOMN*– | HW4 |
| 30 | PARITY*+ | | FRMSP–* | |
| 31 | PRTYEN*– | | | |
| 32 | | GND | CMACT*– | SH*0 |
| 33 | DAS32*– | | | SH*1 |
| 34 | DATA*00 | | CMSYNC*– | FP61*– |
| 35 | DATA*01 | | | C61* |
| 36 | DATA*02 | ADDR*02 | HW0 | |
| 37 | DATA*03 | ADDR*03 | HW1 | |
| 38 | DATA*04 | ADDR*04 | HW2 | |
| 39 | DATA*05 | ADDR*05 | HW3 | |
| 40 | DATA*06 | ADDR*06 | | GND |
| 41 | DATA*07 | ADDR*07 | | GND |
| 42 | DATA*08 | ADDR*08 | TMHERE–* | GND |
| 43 | DATA*09 | ADDR*09 | FHERE–* | GND |
| 44 | DATA*10 | ADDR*10 | TOMWRT–* | +5V* |
| 45 | DATA*11 | ADDR*11 | FRMWRT–* | +5V* |

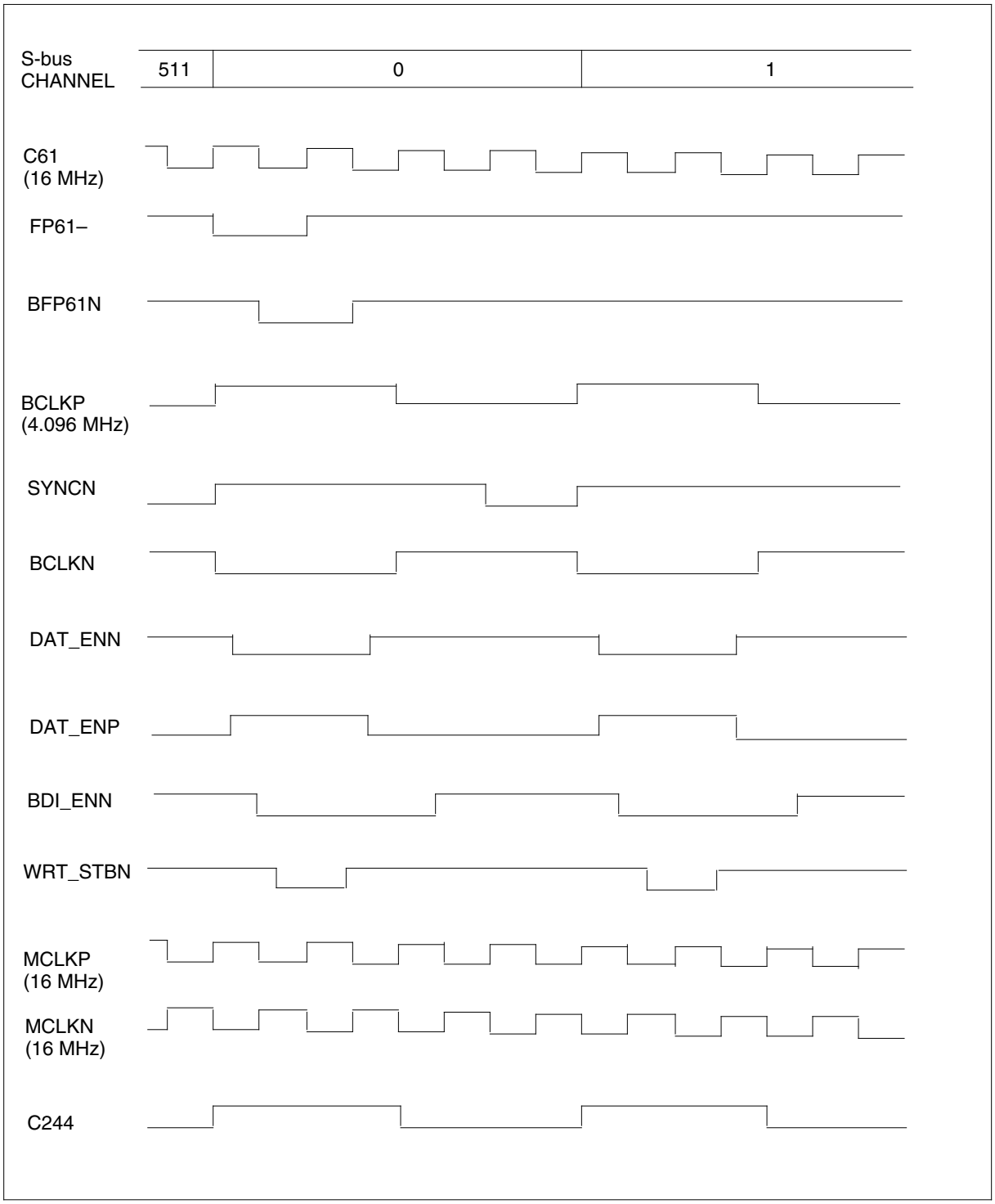
**Legend**

MADDR = MDR
MDATA = MDTA

| | D | C | B | A |
|---|---|---|---|---|
| 46 | DATA*12 | ADDR*12 | TOMAS–* | +5V* |
| 47 | DATA*13 | ADDR*13 | FRMAS–* | +5V* |
| 48 | DATA*14 | ADDR*14 | TOMACK–* | +5V* |
| 49 | DATA*15 | ADDR*15 | FRMACK–* | +5V* |
| 50 | DATA*16 | ADDR*16 | TBSDEC–* | +5V* |
| 51 | DATA*17 | ADDR*17 | FBSDEC–* | +5V* |
| 52 | DATA*18 | ADDR*18 | TMIOINT* | +5V* |
| 53 | DATA*19 | ADDR*19 | FMIOINT* | +5V* |
| 54 | DATA*20 | ADDR*20 | MDR00* | +5V* |
| 55 | DATA*21 | ADDR*21 | | +5V* |
| 56 | DATA*22 | ADDR*22 | | |
| 57 | DATA*23 | ADDR*23 | | TXFP**0 |
| 58 | DATA*24 | ADDR*24 | | RXFP**0 |
| 59 | DATA*25 | ADDR*25 | | STDA**0 |
| 60 | DATA*26 | ADDR*26 | | STDA**1 |
| 61 | DATA*27 | ADDR*27 | | STDA**2 |
| 62 | DATA*28 | ADDR*28 | | STDA**3 |
| 63 | DATA*29 | ADDR*29 | | STDA**4 |
| 64 | DATA*30 | ADDR*30 | | STDA**5 |
| 65 | DATA*31 | ADDR*31 | | STDA**6 |
| 66 | MDTA07* | MDR02* | | STDA**7 |
| 67 | MDTA08* | MDR03* | | |
| 68 | MDTA09* | MDR04* | | |
| 69 | MDTA10* | MDR05* | | SRDA**0 |
| 70 | MDTA11* | MDR06* | | SRDA**1 |
| 71 | MDTA12* | MDR07* | | SRDA**2 |
| 72 | MDTA13* | MDR08* | | SRDA**3 |
| 73 | MDTA14* | MDR09* | | SRDA**4 |
| 74 | MDTA15* | MDR10* | | SRDA**5 |
| 75 | MDTA16* | MDR11* | | SRDA**6 |
| 76 | MDTA17* | MDR12* | | SRDA**7 |
| 77 | MDTA18* | MDR13* | | |
| 78 | MDTA19* | MDR14* | | |
| 79 | MDTA20* | MDR15* | PDATA0 | GND |
| 80 | MDTA21* | MDR16* | PDATA1 | GND |
| 81 | MDTA22* | MDR17* | PDATA2 | GND |
| 82 | MDTA23* | MDR18* | PDATA3 | GND |
| 83 | MDTA24* | | PDATA4 | GND |
| 84 | MDTA25* | MDTA00* | PDATA5 | GND |
| 85 | MDTA26* | MDTA01* | PDATA6 | GND |
| 86 | MDTA27* | MDTA02* | PDATA7 | GND |
| 87 | MDTA28* | MDTA03* | PDATA8 | GND |
| 88 | MDTA29* | MDTA04* | PDATA9 | GND |
| 89 | MDTA30* | MDTA05* | PDATA10 | GND |
| 90 | MDTA31* | MDTA06* | PDATA11 | GND |

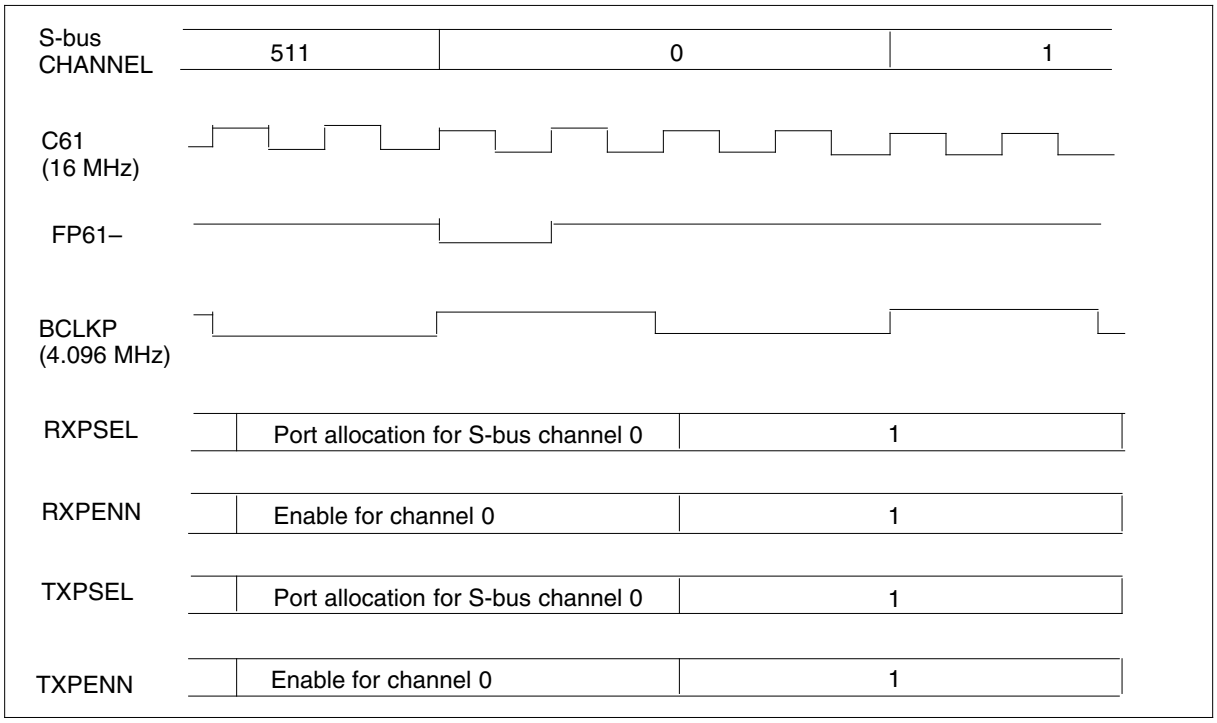
## **NT9X86AA** (continued)

**NT9X86AA clock relationship timing**



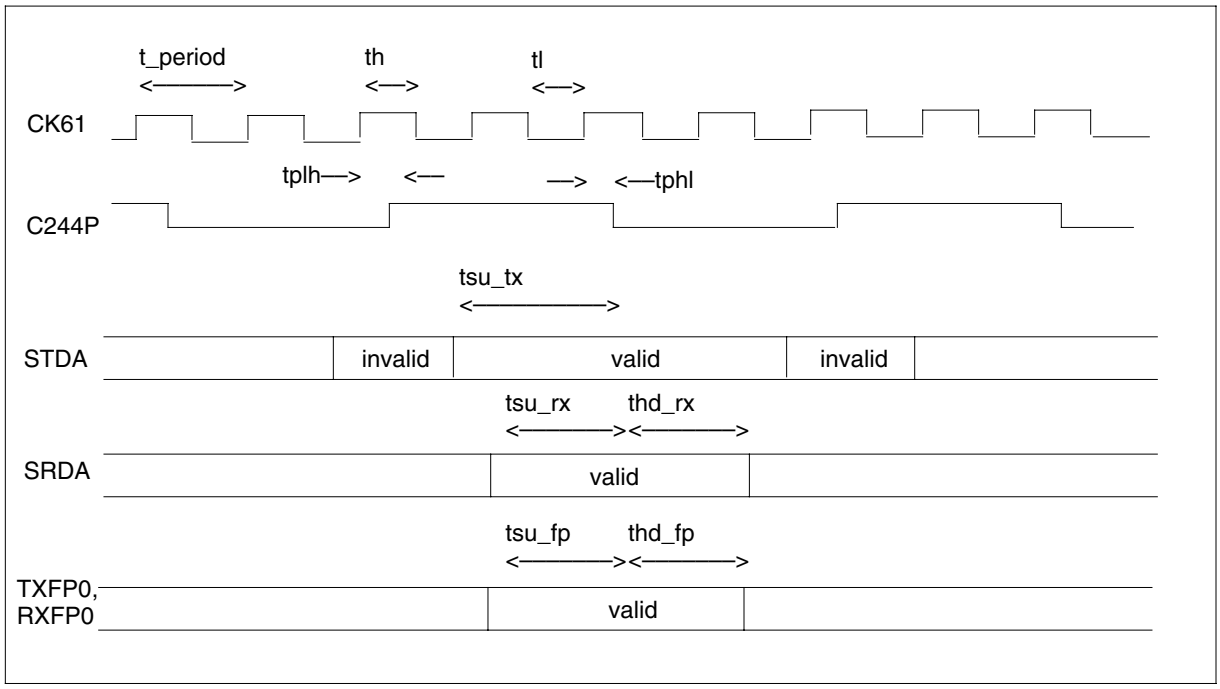
# **NT9X86AA** (continued)

**NT9X86AA port select and port enable signal timing**



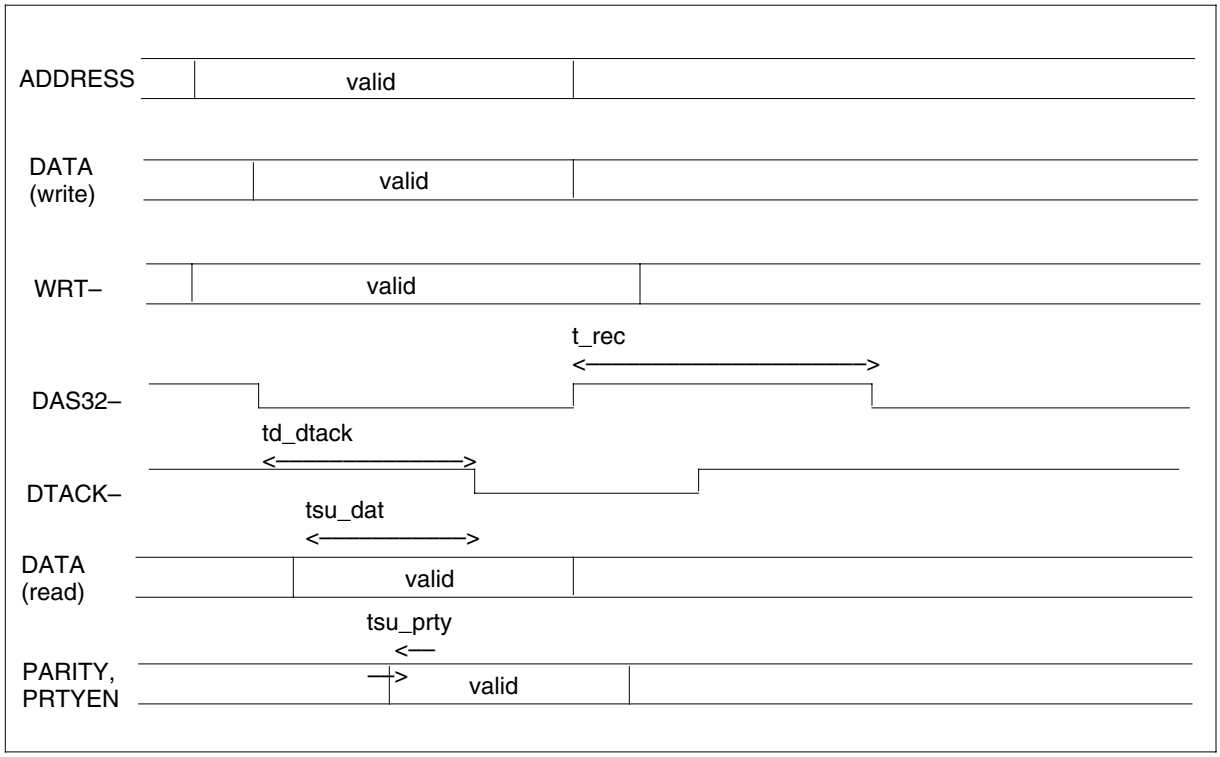
## **NT9X86AA** (continued)

### NT9X86AA Shorting–bus timing




| S–bus timing | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Nominal** | **Maximum** |
| t_period | C61 clock period | 61 ns | | |
| th/tl | C61 duty cycle | 40/60 | 50/50 | 60/40 |
| tplh | C244 lh prop delay | 9.4 ns | 14.0 ns | 25.4 ns |
| tphl | C244 hl prop delay | 10.4 ns | 15.5 ns | 28.5 ns |
| tsu_tx | STDA setup to C244 | 20.5 ns | | |
| tsu_rx | SRDA setup to C244 | 26.0 ns | | |
| thd_rx | SRDA hold from C244 | 15.5 ns | | |
| tsu_fp | FP setup to C244 | 27.0 ns | | |
| thd_fp | FP hold from C244 | 15.5 ns | | |

**NT9X86AA Processor–bus timing**




**(Sheet 1 of 2)**

| **Processor–bus timing** | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Nominal** | **Maximum** |
| t_rec | DAS32- recovery time: | | | |
| | ID PROM read | 115 ns | | |
| | All other IO | 85 ns | | |
| td_dtack | DAS 32- to DTACK- dly: | | | |
| | Maintenance page | 91 ns | 125 ns | 213 ns |
| | IO page | 135 ns | 196 ns | 465 ns |
| | Data ports | 247 ns | 335 ns | 395 ns |
| | TOD | | | |

## **NT9X86AA** (end)

**(Sheet 2 of 2)**

| **Processor–bus timing** | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Nominal** | **Maximum** |
| tsu_prty | Parity valid to DTACK:<br>Write cycle<br>Read cycle | 19.5 ns | | –58 ns |
| tsu_dat | Data valid to DTACK | | | –58 ns |

# Technical data

### Power requirements

The following table shows the power requirements for the NT9X86AA.

| **Power requirements** | | | |
|---|---|---|---|
| **Parameter** | **Minimum** | **Nominal** | **Maximum** |
| Supply voltage | 4.8 V | 5.0 V | 5.2 V |
| Supply ripple | | 0.1 V | |
| Supply current | | 6.5 A | |
| Supply voltage | 4.8 V | 5.0 V | 5.2 V |

# NT9X87AA

## Product description

The NT9X87AA is an important part of the SuperNode file processor (FP) disk and tape drive interface. The NT9X87AA provides a large random-access dual-ported buffer memory. The system uses this memory when the system passes commands to the controllers. The memory holds the data that goes to and from the disk. The memory allows scatter and gather operations. In these operations, the system spreads disk sectors with a common border or messages through the buffers.

The FP CPU, the mass storage disk, and the tape drive controller use this memory. The speed and size of the memory makes sure this event does not congest data transferred to and from the mass storage devices.

## Functional description

The main function of the NT9X87AA is to buffer data and control information. This information moves between the mass storage devices and the FP processor.

### Functional blocks

The NT9X87AA has the following functional blocks:

- memory array
- dual arbiter
- element decode
- crossover bus (C-bus) interface

### Memory array

The memory array is a read and write buffer storage. The processor bus (P-bus) and the small computer system interface (SCSI) storage device controllers use the memory array. The FP processor stores SCSI instructions and data in this buffer. The SCSI controller reads and writes data and status.

The buffer memory array has 8 Mbytes of longword-organized static RAM (SRAM). The memory array, with byte parity, is separated in X and Y blocks. Each block has 4 Mbytes of memory. The memory is 36 bits wide, with 32 bits of data and 4 bits of parity.

The buffer memory array supports all types of memory accesses. The system uses synchronous memory bus accesses to access this memory and control registers.

## **NT9X87AA** (continued)

### Dual arbiter

The dual arbiter controls access of the buffer memory array on the NT9X87AA. One to four dual access buffer memories (DABM) have this control. A maximum of four NT9X88AAs and two FP duplex 9X13s compete for access to the RAM blocks.

### Element decode

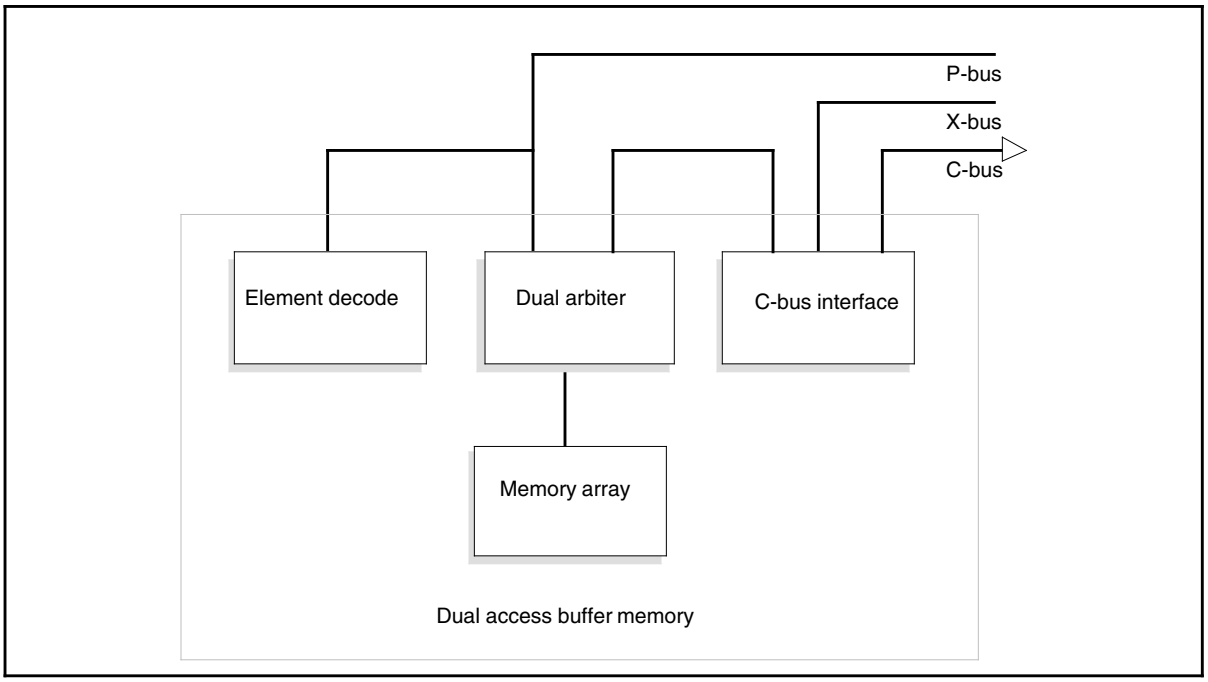
The element decode decodes addresses received from the P-bus to enable the parent card element block components. This block generates allowances for identification (ID) PROM and register block accesses. This block generates data transfer acknowledges. The element decode block contains interrupt controls, out-of-synchronization switch activity detector and zero page protection.

### Crossover bus interface

The C-bus interface controls the data and control signal flow between the active and inactive sides of the duplex FP.

The relationship between the functional blocks appears in the following figure.

**NT9X87AA functional blocks**

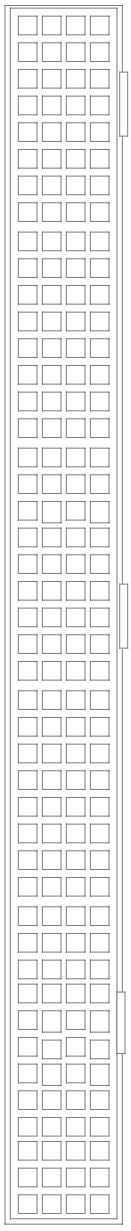


# Signaling

## Pin numbers

The pin numbers for the NT9X87AA appear in the following figures.

**NT9X87AA pin numbers (Part 1 of 2)**



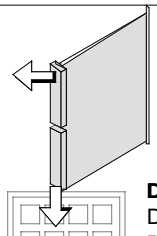
| | D | C | B | A |
|---|---|---|---|---|
| 1 | XDATA02 | XDATA01 | XDATA00 | GND |
| 2 | XDATA05 | XDATA04 | XDATA03 | GND |
| 3 | XDATA08 | XDATA07 | XDATA06 | GND |
| 4 | XDATA11 | XDATA10 | XDATA09 | GND |
| 5 | XDATA14 | XDATA13 | XDATA12 | GND |
| 6 | XDATA17 | XDATA16 | XDATA15 | GND |
| 7 | XDATA20 | XDATA19 | XDATA18 | GND |
| 8 | XDATA23 | XDATA22 | XDATA21 | GND |
| 9 | XDATA26 | XDATA25 | XDATA24 | GND |
| 10 | XDATA29 | XDATA28 | XDATA27 | GND |
| 11 | XDATA31 | INT4– | XDATA30 | GND |
| 12 | | | | GND |
| 13 | | | | |
| 14 | | | | |
| 15 | PLANE | | | |
| 16 | | IMATCH– | | |
| 17 | PEINT6– | | CFNT0 | |
| 18 | PEINT7– | | CFNT1 | |
| 19 | | PEINT2– | CSER10– | |
| 20 | | PEINT3– | CEXP10– | |
| 21 | | PEINT4– | CSER11– | |
| 22 | | PEINT5– | CEXP11– | |
| 23 | RSTOUT– | BUSLOCK– | CCTLB0– | |
| 24 | PEINT1– | PEINT0– | CENX0– | |
| 25 | BEN1– | BEN0– | CCTLB1– | |
| 26 | BEN3– | BEN2– | CENX1– | |
| 27 | GND | | CCTLA0– | |
| 28 | WRT– | GND | CCTLA1– | |
| 29 | | DTACK– | ENOMB– | QUAD1 |
| 30 | PARITY+ | SSR– | CREQP– | |
| 31 | PREN– | MEMERR– | CREQ1– | CREQ0– |
| 32 | FAS– | GND | CSER00– | 9.SH0 |
| 33 | DAS32– | CPUCLK+ | CENBP– | SH1 |
| 34 | DATA00 | | CSER01– | |
| 35 | DATA01 | ADDR01 | TYPE1 | |
| 36 | DATA02 | ADDR02 | HW0 | |
| 37 | DATA03 | ADDR03 | HW1 | |
| 38 | DATA04 | ADDR04 | HW2 | |
| 39 | DATA05 | ADDR05 | QUAD0 | |
| 40 | DATA06 | ADDR06 | CMACT– | GND |
| 41 | DATA07 | ADDR07 | CEXP00– | GND |
| 42 | DATA08 | ADDR08 | CMSYNC– | GND |
| 43 | DATA09 | ADDR09 | CEXP01– | GND |
| 44 | DATA10 | ADDR10 | CPARITY | +5V |
| 45 | DATA11 | ADDR11 | CACK– | +5V |

**Legend**

XAD = XADDR
CADR = CADDR

# **NT9X87AA** (continued)

### NT9X87AA pin numbers (Part 2 of 2)

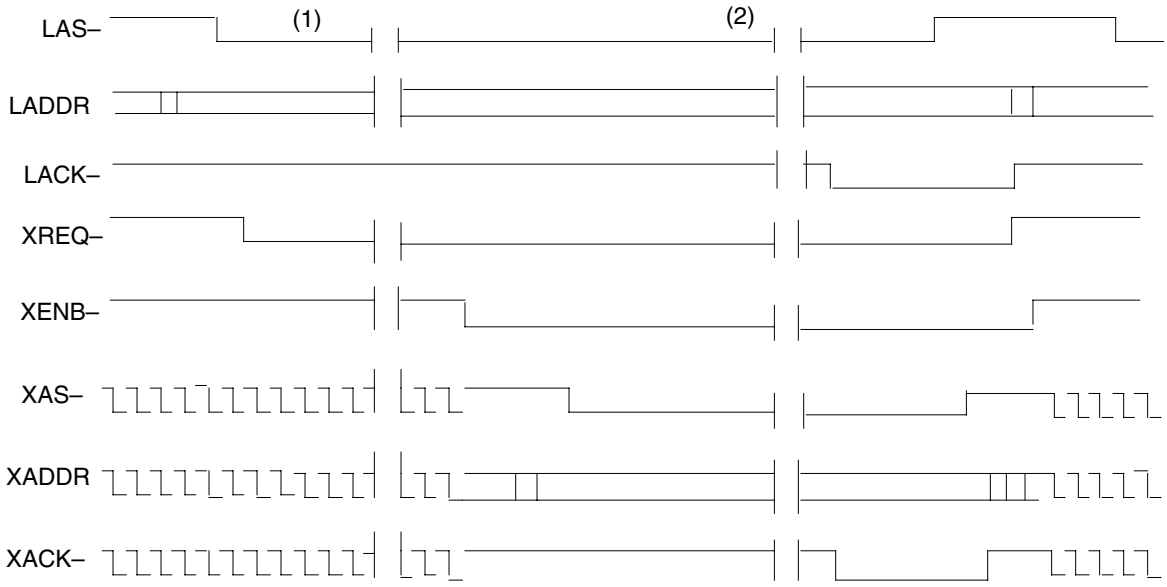


| | D | C | B | A |
|---|---|---|---|---|
| 46 | DATA12 | ADDR12 | CAS– | +5V |
| 47 | DATA13 | ADDR13 | CWRT– | +5V |
| 48 | DATA14 | ADDR14 | FACK– | +5V |
| 49 | DATA15 | ADDR15 | CBSDEC– | +5V |
| 50 | DATA16 | ADDR16 | CADR02 | +5V |
| 51 | DATA17 | ADDR17 | CADR03 | +5V |
| 52 | DATA18 | ADDR18 | CADR04 | +5V |
| 53 | DATA19 | ADDR19 | CADR05 | +5V |
| 54 | DATA20 | ADDR20 | CADR06 | +5V |
| 55 | DATA21 | ADDR21 | CADR07 | +5V |
| 56 | DATA22 | ADDR22 | FAULT– | TYPE0 |
| 57 | DATA23 | ADDR23 | XCTLB0– | XAD02 |
| 58 | DATA24 | ADDR24 | XENX0– | XAD03 |
| 59 | DATA25 | ADDR25 | XCTLB1– | XAD04 |
| 60 | DATA26 | ADDR26 | XENX1– | XAD05 |
| 61 | DATA27 | ADDR27 | XCTLA0– | XAD06 |
| 62 | DATA28 | ADDR28 | XCTLA1– | XAD07 |
| 63 | DATA29 | ADDR29 | XPARITY | XAD08 |
| 64 | DATA30 | ADDR30 | XSERV0– | XAD09 |
| 65 | DATA31 | ADDR31 | XEXCP0– | XAD10 |
| 66 | CDATA07 | CADR08 | XSERV1– | XAD11 |
| 67 | CDATA08 | CADR09 | XEXCP1 | XAD12 |
| 68 | CDATA09 | CADR10 | XENBS– | XAD13 |
| 69 | CDATA10 | CADR11 | | XAD14 |
| 70 | CDATA11 | CADR12 | XREQ0– | XAD15 |
| 71 | CDATA12 | CADR13 | XREQ1– | XAD16 |
| 72 | CDATA13 | CADR14 | PENBS– | XAD17 |
| 73 | CDATA14 | CADR15 | XACK– | XAD18 |
| 74 | CDATA15 | CADR16 | XAS– | XAD19 |
| 75 | CDATA16 | CADR17 | XWRT– | XAD20 |
| 76 | CDATA17 | CADR18 | XBSDEC– | XAD21 |
| 77 | CDATA18 | CADR19 | XAD24 | XAD22 |
| 78 | CDATA19 | CADR20 | XAD25 | XAD23 |
| 79 | CDATA20 | CADR21 | | GND |
| 80 | CDATA21 | CADR22 | | GND |
| 81 | CDATA22 | CADR23 | | GND |
| 82 | CDATA23 | CADR24 | | GND |
| 83 | CDATA24 | CADR25 | | GND |
| 84 | CDATA25 | CDATA00 | | GND |
| 85 | CDATA26 | CDATA01 | | GND |
| 86 | CDATA27 | CDATA02 | | GND |
| 87 | CDATA28 | CDATA03 | | GND |
| 88 | CDATA29 | CDATA04 | | GND |
| 89 | CDATA30 | CDATA05 | | GND |
| 90 | CDATA31 | CDATA06 | | GND |

### Timing

The timing for the NT9X87AA appears in the following figure.

**NT9X87AA X-bus timing with arbitration**




**Legend**

(1) waiting for X-bus grant (XENB–)
(2) waiting for DABM acknowledge (XACK–)
LADDR includes LWRT– and LBSDEC.
XADDR includes XWRT– and XBSDEC.

X-bus may be driven by another SCSI interface paddle board (SIP)

indeterminate address

SIP 68020 wait cycle insertion

## Technical data

### Power requirements

The required voltage for the NT9X87AA is 5V. The required current is 7A.

# NT9X88AA

## Product description

The SCSI interface processor (SIP) paddle board is an important part of the SuperNode change file processor (FP) disk and tape drive interface. The NT9X88AA provides a standard small computer system interface (SCSI) port to connect to disk and tape mass storage devices.

### Location

The NT9X88AA is behind the dual access buffer memory, NT9X87AA, in the file processor shelf.

## Functional description

The function of the NT9X88AA is to provide low-level control of an independent SCSI bus. The controller takes commands from the dual access buffer memory (DABM). The controller executes the commands with limited interruption from the FP 9X13 CPU card. The system processes interrupts and faults to remove the main shelf processor.

### Functional blocks

The NT9X88AA has the following functional blocks:

- SCSI interface
- serial interface
- microcontroller unit (MCU)
- X-bus interface
- element

### Small computer system interface

The SCSI interface contains a commercial SCSI controller chip. The interface contains differential transceivers and termination resistors. The SCSI requires these transceivers and resistors to operate the SCSI bus at the maximum speed. The SCSI controller integrated circuit (IC) can arbitrate for the SCSI bus. The IC performs this function through a standard 8-bit peripheral interface. The IC can select an objective, and send a first message with two commands.

### Serial interface

The serial interface is the FP end of a low-speed serial bus that follows the same route as the SCSI bus. At each SCSI device, a small controller interprets commands and issues replies over the serial interface. The system uses this link to collect identification (ID) PROM data from remote devices. This link issues specialized control commands like single device resets.

### Microcontroller unit

The MCU accesses the DABM to read instructions that the FP 9X13 issues. The MCU interprets the instructions and initiates SCSI transactions. The MCU handles most SCSI bus anomalies without intervention from the 9X13. The MC68020 has 128 kbytes of EPROM program storage and 128K by 32 bits of RAM program and data storage. For power-up and basic operations, the EPROM contains enough software to run the system.

### X-bus interface

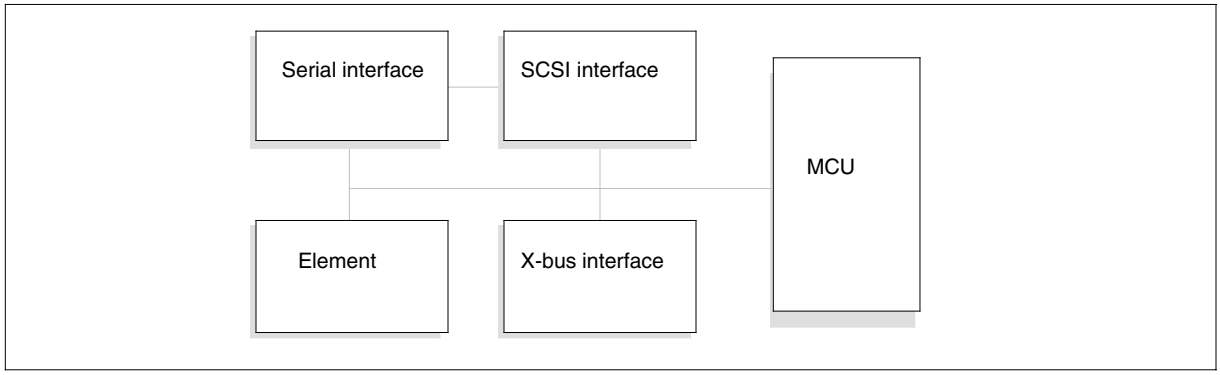
The X-bus interface buffers 32 bits of data and 24 bits of address. The 24 bits of address are A2 to A25. The interface buffers the data and addresses from the SIP internal bus to the AP shelf X-bus. The logic is responsible for the correct generation and acceptance of X-bus arbitration and parity checks. The X-bus parity calculates X-bus arbitration and parity checks for reads and for writes.

### Element

The element provides 9X13 access to an SIP status scan register and the internal MC68020 local bus (L-bus). The status scan register provides status bits for power-up, service and exception requests, sanity timeout and card fail.

The relationship between the functional blocks appears in the following figure.

**NT9X88AA functional blocks**



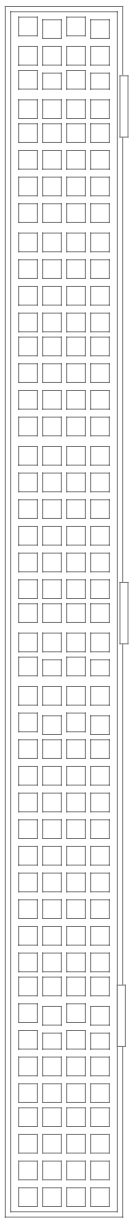

## Signaling

### Pin numbers

The pin numbers for the NT9X88AA appear in the following figure. The SCSI start connectors and the SCSI end connectors appear in the following tables.

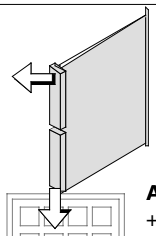
# **NT9X88AA** (continued)

### NT9X88AA pin numbers (Part 1 of 2)



| | A | B | C | D |
|---|---|---|---|---|
| 1 | GND | XDATA00 | XDATA01 | XDATA02 |
| 2 | GND | XDATA03 | XDATA04 | XDATA05 |
| 3 | GND | XDATA06 | XDATA07 | XDATA08 |
| 4 | GND | XDATA09 | XDATA10 | XDATA11 |
| 5 | GND | XDATA12 | XDATA13 | XDATA14 |
| 6 | GND | XDATA15 | XDATA16 | XDATA17 |
| 7 | GND | XDATA18 | XDATA19 | XDATA20 |
| 8 | GND | XDATA21 | XDATA22 | XDATA23 |
| 9 | GND | XDATA24 | XDATA25 | XDATA26 |
| 10 | GND | XDATA27 | XDATA28 | XDATA29 |
| 11 | GND | XDATA30 | | XDATA31 |
| 12 | GND | | | |
| 13 | | | | |
| 14 | | | | |
| 15 | | | | PLANE |
| 16 | | | | |
| 17 | | | | |
| 18 | | | | |
| 19 | | | | |
| 20 | | | | |
| 21 | | | | |
| 22 | | | | |
| 23 | | | BUSLCK– | |
| 24 | | | | |
| 25 | | | | |
| 26 | | | | |
| 27 | | | | GND |
| 28 | | | GND | WRT– |
| 29 | QUAD1 | ENOMB– | DTACK– | EDTACK– |
| 30 | | | | |
| 31 | | | | |
| 32 | SH0 | | GND | |
| 33 | SH1 | | CPUCLK+ | DAS32– |
| 34 | | | | DATA00 |
| 35 | | TYPE1 | | DATA01 |
| 36 | | HW0 | ADDR02 | DATA02 |
| 37 | | HW1 | ADDR03 | DATA03 |
| 38 | | HW2 | ADDR04 | DATA04 |
| 39 | | QUAD0 | ADDR05 | DATA05 |
| 40 | GND | CMACT– | ADDR06 | DATA06 |
| 41 | GND | | ADDR07 | DATA07 |
| 42 | GND | | AADR08 | DATA08 |
| 43 | GND | | ADDR09 | DATA09 |
| 44 | +5V | | ADDR10 | DATA10 |
| 45 | +5V | | ADDR11 | DATA11 |

**NT9X88AA pin numbers (Part 2 of 2)**



| | A | B | C | D |
|---|---|---|---|---|
| 46 | +5V | | ADDR12 | DATA12 |
| 47 | +5V | | ADDR13 | DATA13 |
| 48 | +5V | | ADDR14 | DATA14 |
| 49 | +5V | | ADDR15 | DATA15 |
| 50 | +5V | | ADDR16 | DATA16 |
| 51 | +5V | | ADDR17 | DATA17 |
| 52 | +5V | | ADDR18 | DATA18 |
| 53 | +5V | | ADDR19 | DATA19 |
| 54 | +5V | | ADDR20 | DATA20 |
| 55 | +5V | | ADDR21 | DATA21 |
| 56 | TYPE0 | | ADDR22 | DATA22 |
| 57 | XADDR02 | XCTLB | ADDR23 | DATA23 |
| 58 | XADDR03 | XENX– | ADDR24 | DATA24 |
| 59 | XADDR04 | | ADDR25 | DATA25 |
| 60 | XADDR05 | | ADDR26 | DATA26 |
| 61 | XADDR06 | XCTLA | ADDR27 | DATA27 |
| 62 | XADDR07 | | ADDR28 | DATA28 |
| 63 | XADDR08 | XPARITY | ADDR29 | DATA29 |
| 64 | XADDR09 | XSERV– | ADDR30 | DATA30 |
| 65 | XADDR10 | XEXCP– | ADDR31 | DATA31 |
| 66 | XADDR11 | | | |
| 67 | XADDR12 | | | |
| 68 | XADDR13 | | | |
| 69 | XADDR14 | | | |
| 70 | XADDR15 | XREQ– | | |
| 71 | XADDR16 | | | |
| 72 | XADDR17 | | | |
| 73 | XADDR18 | XACK– | | |
| 74 | XADDR19 | XAS– | | |
| 75 | XADDR20 | XWRT– | | |
| 76 | XADDR21 | XBSDEC– | | |
| 77 | XADDR22 | XADDR24 | | |
| 78 | XADDR23 | XADDR25 | | |
| 79 | GND | | | |
| 80 | GND | | | |
| 81 | GND | | | |
| 82 | GND | | | |
| 83 | GND | | | |
| 84 | GND | | | |
| 85 | GND | | | |
| 86 | GND | | | |
| 87 | GND | | | |
| 88 | GND | | | |
| 89 | GND | | | |
| 90 | GND | | | |

## **NT9X88AA** (continued)

**SCSI bus start connectors (P2) (Sheet 1 of 2)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +TXDATA | 32 | SP11 |
| 2 | -TXDATA | 33 | +BSY |
| 3 | +DB0 | 34 | -BSY |
| 4 | -DB0 | 35 | +ACK |
| 5 | +DB1 | 36 | -ACK |
| 6 | -DB1 | 37 | +RST |
| 7 | +DB2 | 38 | -RST |
| 8 | -DB2 | 39 | +MSG |
| 9 | +DB3 | 40 | -MSG |
| 10 | -DB3 | 41 | +SEL |
| 11 | +DB4 | 42 | -SEL |
| 12 | -DB4 | 43 | +C_D |
| 13 | +DB5 | 44 | -C_D |
| 14 | -DB5 | 45 | +REQ |
| 15 | +DB6 | 46 | -REQ |
| 16 | -DB6 | 47 | +I_O |
| 17 | +DB7 | 48 | -I_O |
| 18 | -DB7 | 49 | SP12 |
| 19 | +DBP | 50 | SP13 |
| 20 | -DPB | 51 | SP14 |
| 21 | SP2 | 52 | SP15 |
| 22 | SP3 | 53 | SP16 |
| 23 | SP4 | 54 | SP17 |
| 24 | SP5 | 55 | SP18 |

**SCSI bus start connectors (P2) (Sheet 2 of 2)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 25 | SP6 | 56 | SP19 |
| 26 | SP7 | 57 | CBLCAR |
| 27 | SP8 | 58 | BCBLPWR |
| 28 | SP9 | 59 | +ENOMB |
| 29 | +ATN | 60 | -ENOMB |
| 30 | -ATN | 61 | +RXDATA |
| 31 | SP10 | 62 | -RXDATA |

**SCSI bus end connectors (P3) (Sheet 1 of 2)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +ZTXDATA | 32 | |
| 2 | -ZTXDATA | 33 | +ZBSY |
| 3 | +ZDB0 | 34 | Busy |
| 4 | -ZDB0 | 35 | +ZACK |
| 5 | +ZDB1 | 36 | Acknowledge |
| 6 | -ZDB1 | 37 | +ZRST |
| 7 | +ZDB2 | 38 | Reset |
| 8 | -ZDB2 | 39 | +ZMSG |
| 9 | +ZDB3 | 40 | Message |
| 10 | -ZDB3 | 41 | +ZSEL |
| 11 | +ZDB4 | 42 | Selection |
| 12 | -ZDB4 | 43 | ZC_D |
| 13 | +ZDB5 | 44 | -ZC_D |
| 14 | -ZDB5 | 45 | +ZREQ |
| 15 | +ZDB6 | 46 | -ZREQ |

## **NT9X88AA** (continued)

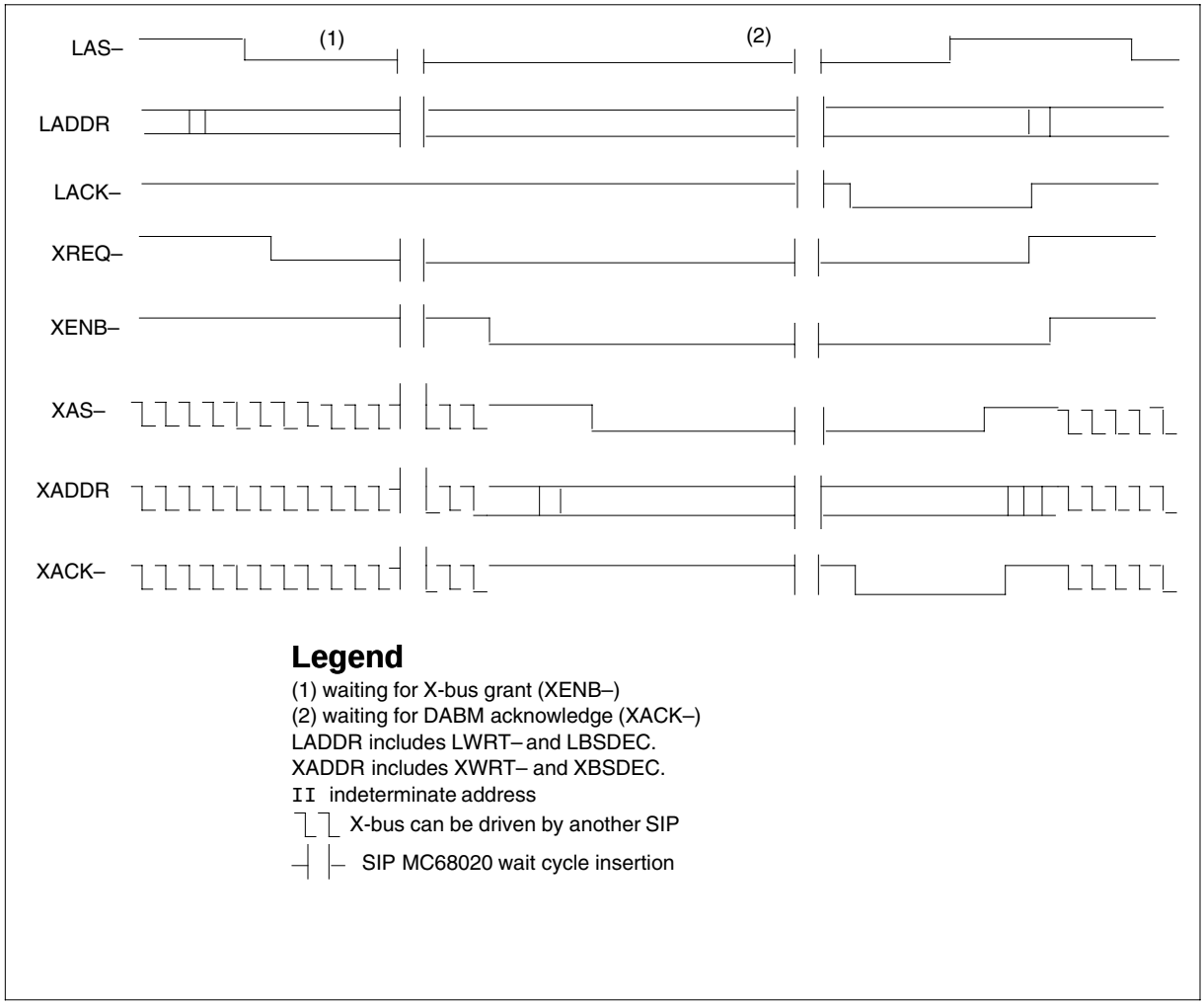
**SCSI bus end connectors (P3) (Sheet 2 of 2)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 16 | -ZDB6 | 47 | +ZI_O |
| 17 | +ZDB7 | 48 | -ZI_O |
| 18 | -ZDB7 | 49 | ZSP12 |
| 19 | +ZDBP | 50 | ZSP13 |
| 20 | -ZDBP | 51 | ZSP14 |
| 21 | ZSP2 | 52 | ZSP15 |
| 22 | | 53 | ZSP16 |
| 23 | ZSP4 | 54 | ZSP17 |
| 24 | | 55 | ZSP18 |
| 25 | ZSP6 | 56 | ZSP19 |
| 26 | | 57 | ZCBLCAR |
| 27 | ZSP8 | 58 | ZBCBLPWR |
| 28 | | 59 | ZSP22 |
| 29 | +ZATN | 60 | ZSP23 |
| 30 | Attention | 61 | +ZRXDATA |
| 31 | ZSP10 | 62 | -ZRXDATA |

### Timing

The X-bus timing with arbitration appears in the following figure.

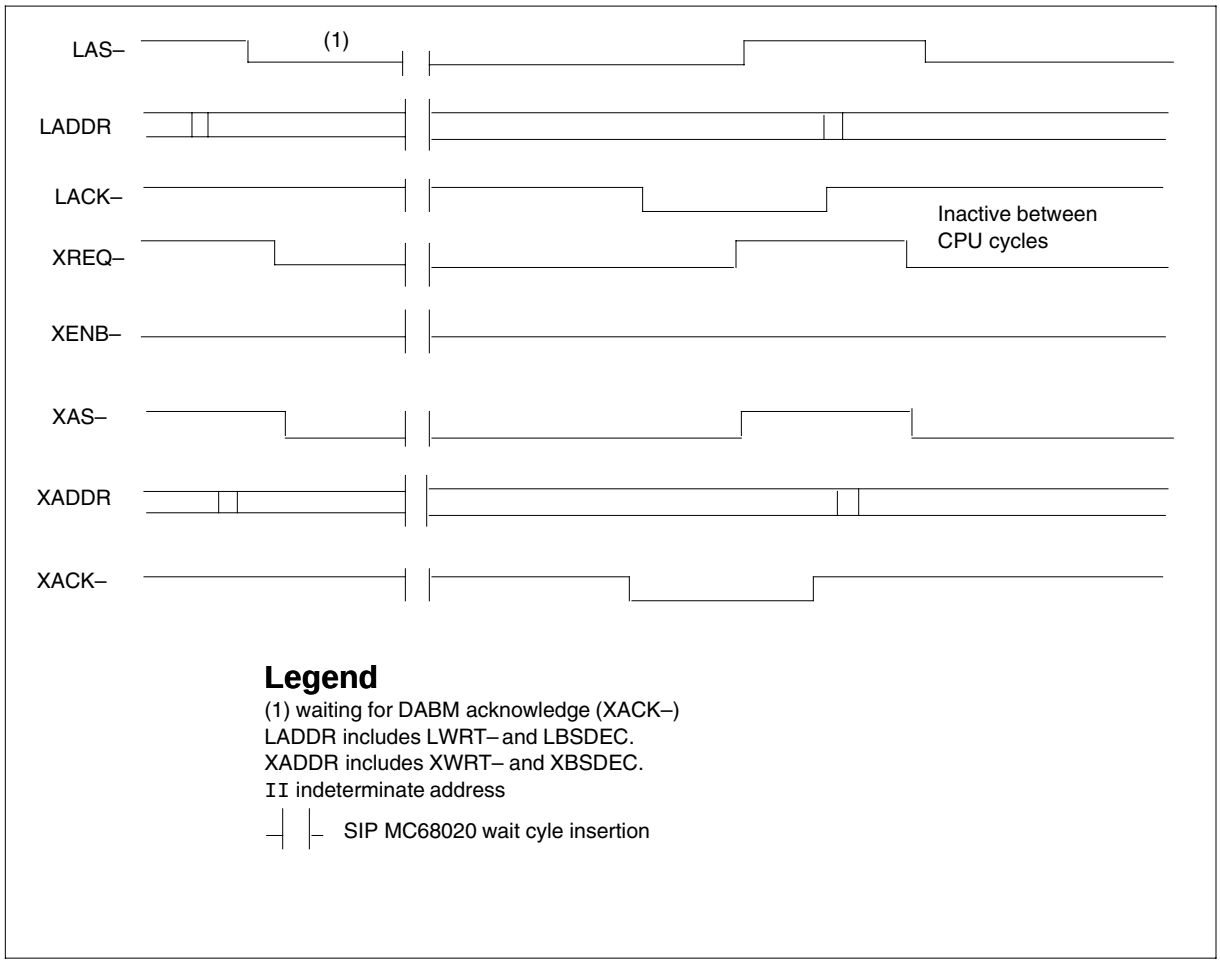
**NT9X88AA X-bus timing with arbitration**




The X-bus timing without arbitration appears in the following figure.

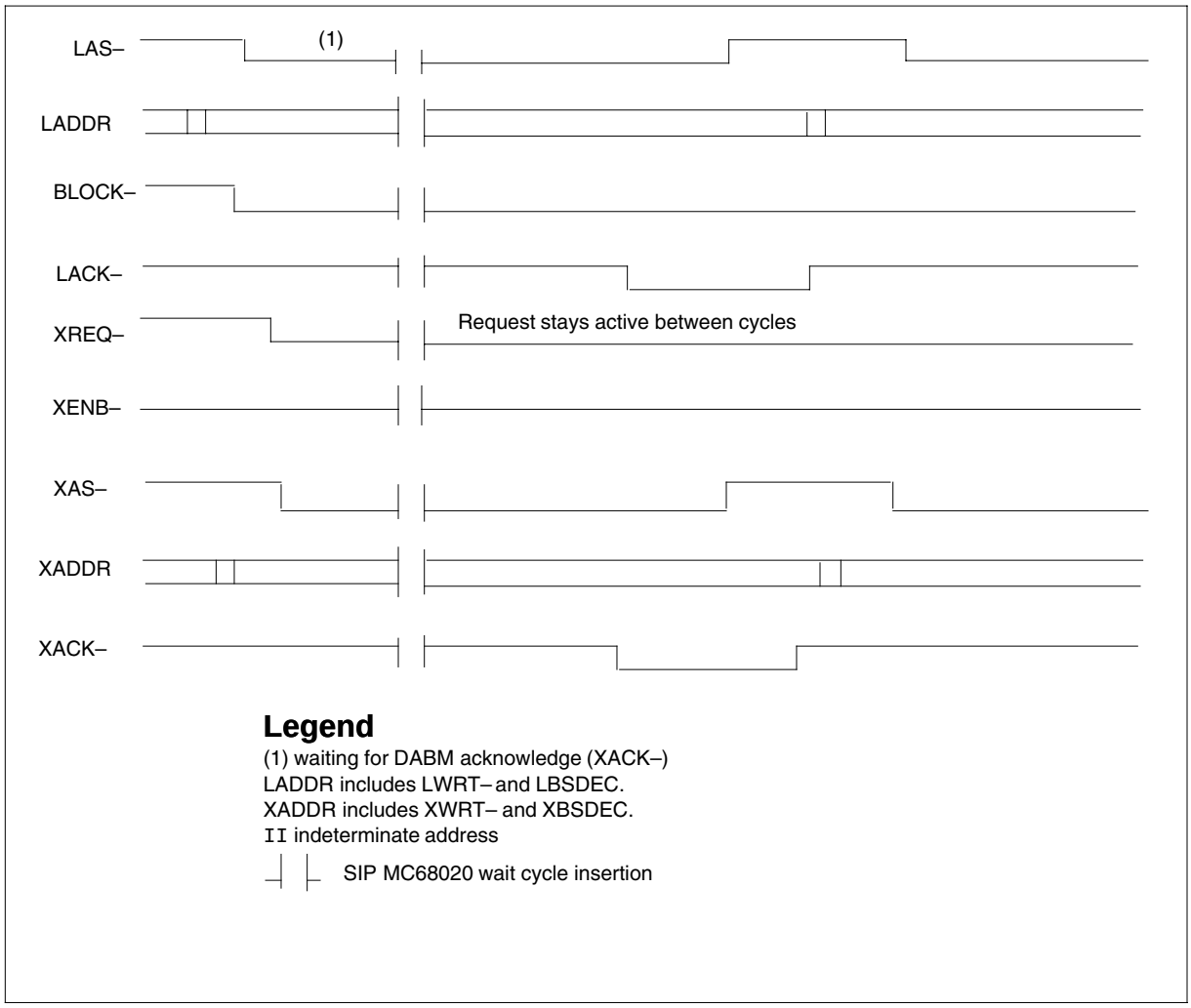
## **NT9X88AA** (continued)

**NT9X88AA X-bus timing without arbitration**




The X-bus timing without arbitration and with bus lock active appears in the following figure.

**NT9X88AA X-bus timing without arbitration, bus lock active**




# Technical data

## Power requirements

The required voltage is 5V. The required current is 3.6A.

# NT9X89AA

## Product description

The system uses the NT9X89AA in SuperNode evolution. In the Super Node evolution, the application processor (AP), the file processor (FP) and the data communication processor (DCP) form the computing structure. The FP accesses mass storage devices with a small computer systems interface (SCSI) bus. The NT9X89AA provides an interface between these storage devices and the SCSI bus.

### Location

The SCSI device interface paddle boards (SDIP) is in the first two paddleboard slots of the SCSI device shelf.

## Functional description

The NT9X89AA performs the following functions:

- communicates with the FP, through a differential serial link, for the transfer of control and status information
- allows the FP to control the attachment and removal of a differential SCSI bus to and from the SCSI mass storage devices
- monitors different status conditions of the boards in the shelf where the board resides
- allows SDIP micro control access to the identification (ID) PROM in each quadrant of the shelf, and scan and control registers on other cards

### Functional blocks

The NT9X89AA has the following functional blocks:

- priority
- sanity timer
- microcontroller
- terminal interface
- differential drivers and receivers
- SCSI repeater
- element interface
- ID PROM
- ROM/RAM
- shelf status
- local SCSI controller

### Priority

The priority block controls which SDIP has priority in the quadrant. The priority SDIP controls which of the two SDIPs is active. The active SDIP reads data from and writes data to the mass storage device of the quadrant. The active SDIP sends SCSI signals back to the SCSI interface paddle boards (SIP).

### Sanity timer

The sanity timer resets the microcontroller when the microcontroller counts down to zero to check the sanity of the microcontroller.

### Microcontroller

The microcontroller controls all functions of the SDIP. The microcontroller performs the following functions:

- reads and writes data
- communicates with the FP SIP to transmit data and receive commands
- provides a soft universal asynchronous receiver--transmitter (UART) for terminal serial link
- controls the local SCSI interface

### Terminal interface

The terminal interface is an RS232 interface for a debug terminal to communicate with a soft UART on the microcontroller.

### Differential drivers and receivers

The differential drivers and receivers convert differential serial signals on the differential serial link. The differential drivers and receivers convert single--ended serial signals that go to and from the microcontroller.

### Small computer systems interface repeater

The SCSI repeater converts differential SCSI signals to and from single--ended SCSI signals.

### Identification PROM

The processor reads the hardware and software information that the ID PROM contains for initialization and maintenance.

### ROM/RAM

The ROM contains the firmware for the microcontroller. The RAM stores data.

### Shelf status

The shelf status block monitors different status conditions of the cards in the shelf in which the NT9X89AA resides.

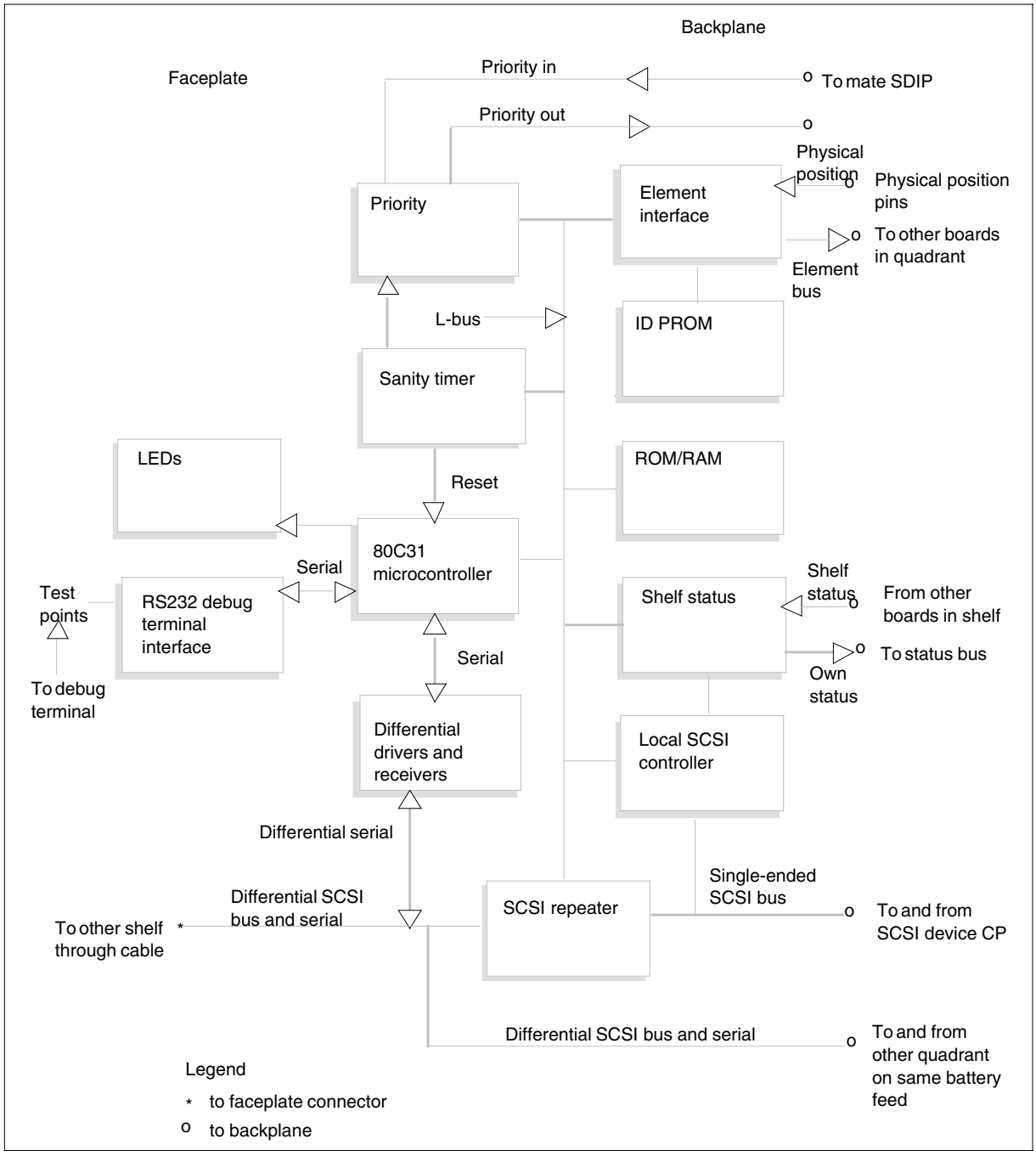
## **NT9X89AA** (continued)

### Local small computer systems interface controller

The local SCSI controller contributes to the FP maintenance in SCSI bus fault isolation.

The relationships between the functional blocks appears in the following figure.

### NT9X89AA functional blocks



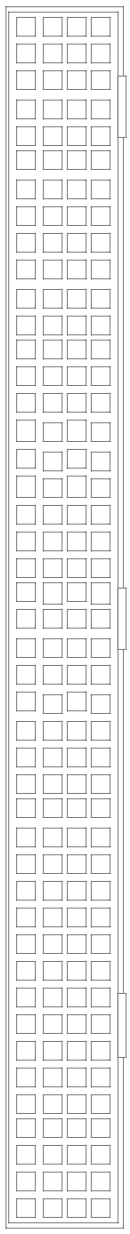

# Signaling

## Pin numbers

The pin numbers for the NT9X89AA appear in the following figures.

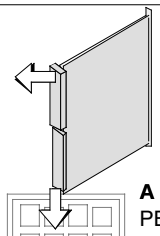
# **NT9X89AA** (continued)

### NT9X89AA pin numbers (Part 1 of 2)



| | A | B | C | D |
|---|---|---|---|---|
| 1 | | | D0 | D1 |
| 2 | | | D2 | D3 |
| 3 | | | D4 | D5 |
| 4 | | D6 | | |
| 5 | | | | A3 |
| 6 | | | A2 | A1 |
| 7 | | | A0 | D7 |
| 8 | | | | |
| 9 | | | A4 | RD |
| 10 | | WR | CS | |
| 11 | | PRIORIN | | PRIORO |
| 12 | | | | SDIPSEL |
| 13 | | | | |
| 14 | | | | |
| 15 | | | | |
| 16 | | | | |
| 17 | | | | |
| 18 | | | | |
| 19 | | | | |
| 20 | | | | SPARE |
| 21 | | | CPPR0 | |
| 22 | | PWPR0 | PB2PR0 | |
| 23 | TXDH | PB1PR0 | | |
| 24 | TXDL | | DB2H | |
| 25 | | DB1H | DB2L | |
| 26 | DB0H | DB1L | CAB1PR0 | CAB2PR0 |
| 27 | DB0L | PB2SAN0 | DB5H | RPTR1EN0 |
| 28 | PB1SAN0 | DB4H | DB5L | |
| 29 | DB3H | DB4L | | PRTR2EN0 |
| 30 | DB3L | | DBPH | |
| 31 | | DB7H | DBPL | |
| 32 | DB6H | DB7L | SPARE | |
| 33 | DB6L | SPARE | REQH | SPARE |
| 34 | SPARE | | REQL | |
| 35 | ACKH | | RSTH | |
| 36 | ACKL | | RSTL | |
| 37 | | BSYH | | |
| 38 | ATNH | BSYL | PB1PR1 | |
| 39 | ATNL | CPPR1 | SELH | |
| 40 | PWPR1 | FCBLPWR | SELL | |
| 41 | MSGH | | BCBLPWR | PB2PR1 |
| 42 | MSGL | | SPARE1 | |
| 43 | | I_OH | SPARE2 | |
| 44 | C_DH | I_OL | CAB1PR1 | |
| 45 | C_DL | PB2SAN1 | SPARE5 | |

**NT9X89AA pin numbers (Part 1 of 2)**



| | A | B | C | D |
|---|---|---|---|---|
| 46 | PB1SAN1 | SPARE21 | SPARE6 | |
| 47 | SPARE3 | SPARE22 | CAB2PR1 | |
| 48 | SPARE4 | | SPARE11 | |
| 49 | | SPARE9 | SPARE12 | |
| 50 | SPARE7 | SPARE10 | SPARE | |
| 51 | SPARE8 | PRTR2EN1 | SPARE17 | |
| 52 | RPTR1EN1 | SPARE15 | SPARE18 | |
| 53 | SPARE13 | SPARE16 | SPARE | |
| 54 | SPARE14 | | RXDH | |
| 55 | | ENOMBNH | RXDL | |
| 56 | SPARE19 | ENOMBNL | SPARE | SPARE |
| 57 | SPARE20 | SPARE | | |
| 58 | SPARE | | | |
| 59 | | | | |
| 60 | | | | |
| 61 | | CPPR2 | PB1PR2 | QUAD0 |
| 62 | | TYPE0 | PB2PR2 | QUAD1 |
| 63 | PWPR2 | TYPE1 | CAB1PR2 | SPARE |
| 64 | SH1 | PB2SAN2 | PRTR2EN2 | |
| 65 | PB1SAN2 | RPTR1EN2 | | |
| 66 | CAB2PR2 | | SPARE | |
| 67 | | SPARE | SPARE | |
| 68 | SPARE | SPARE | PLN | |
| 69 | | PWPR3 | PB2PR3 | |
| 70 | CAB1 | PB1PR3 | CAB1PR3 | |
| 71 | CPPR3 | PB2SAN3 | | |
| 72 | PB1SAN3 | | PRTR2EN3 | |
| 73 | | RPTR1EN3 | SPARE | |
| 74 | CAB2PR3 | SPARE | HW2 | |
| 75 | SPARE | HW1 SPARE | | |
| 76 | HW0 | SPARE | SPARE | |
| 77 | | | | |
| 78 | | | | |
| 79 | | | | |
| 80 | | | | |
| 81 | SEDBPL | | SEDB3L | |
| 82 | | SEDB2L | | |
| 83 | | SEDB1L | SEDB7L | |
| 84 | SEDB0L | SEDB6L | | |
| 85 | SEDB5L | | | |
| 86 | | SEDB4L | | |
| 87 | | SEMSGL | | SEREQL |
| 88 | SEC_DL | | SEACKL | |
| 89 | | SEBSYL | | |
| 90 | SESELL | | | SEI_OL |

# NT9X89BA

## Product description

The NT9X89BA small computer system interface (SCSI) device interface paddle board (SDIP) provides file processing with the use of mass storage devices. The SDIP communicates with the NT9X88AA SCSI interface processor (SIP) over a differential serial link for transfers of control and status information.

File processors (FP) provide access to mass storage devices over an SCSI bus. The SDIP acts as an interface between these storage devices and the SCSI bus.

The NT9X89BA has the following features:

- SCSI device identification (ID) the microcontroller assigns
- SCSI access control is transparent to the SCSI bus operation
- interconnection of single mass–storage devices to the SCSI bus without the use of a spare quadrant to continue the SCSI bus
- supports data transfer rates of up to 3.0 Mbps asynchronous, and 4.0 Mbps synchronous
- 9.6 Kbps serial link to the SIP for communication and control
- flexible SCSI device provisioning
- complete status monitoring
- local diagnostics, scan function and control
- software control of +12V for the SCSI device
- status light–emitting diodes (LED)
- reads and transmits ID PROM data to provide electronic inventory capability
- SCSI interface chip for use in loop testing and buffer testing of the SCSI bus
- a debugging terminal interface dedicated to hardware testing

The NT9X89BA is the first issue of this card. Backward compatibility is not an issue.

### Location

The NT9X89BA can be in slots 8, 9, 14, 15, 20, 21, 26, or 27 of the NT9X83 SCSI device shelf. The configuration of the FP determines the position of the card.

## Functional description

File processor hardware consists of two sets of mass storage devices. The associated hardware and software to access the storage devices also makes up the the hardware. The design has two independent sides. Each side can access the sets of mass storage devices over SCSI buses.

The SCSI buses originate at SIP paddle boards on each FP side. The buses connect to SDIPs in the device shelves and return to the SIP where the buses begin. When the correct SDIP is active, any storage device can attach to an FP side. Each FP can support several configurations for each set of devices. Both FP sides can possess two SIPs.

The maximum number of attached storage devices on a bus at one time is six. This condition occurs because only eight SCSI device IDs are available and one device is for tests. A larger number of storage devices can connect to the SCSI bus through SDIPs. When the FP must access a device, a command sent to the SDIP must assign that device a SCSI ID.

The NT9X89BA has the following functions:

- communicates with the FP over a differential serial link for the transfers of control and status information
- gives the FP control to attach and detach the differential SCSI bus to and from the SCSI mass–storage devices
- monitors the status conditions of the boards in the shelves
- provides the SDIP with read and write access to the ID PROMs. The NT9X89BA provides the status and control registers on all the other boards in the quadrant, except for the other SDIP.

### Functional blocks

The NT9X89BA has the following functional blocks:

- SCSI repeater
- shelf status interface
- LEDs
- location block
- ID PROM
- single–chip microcontroller
- universal asynchronous receiver/transmitter (UART)
- local SCSI interface

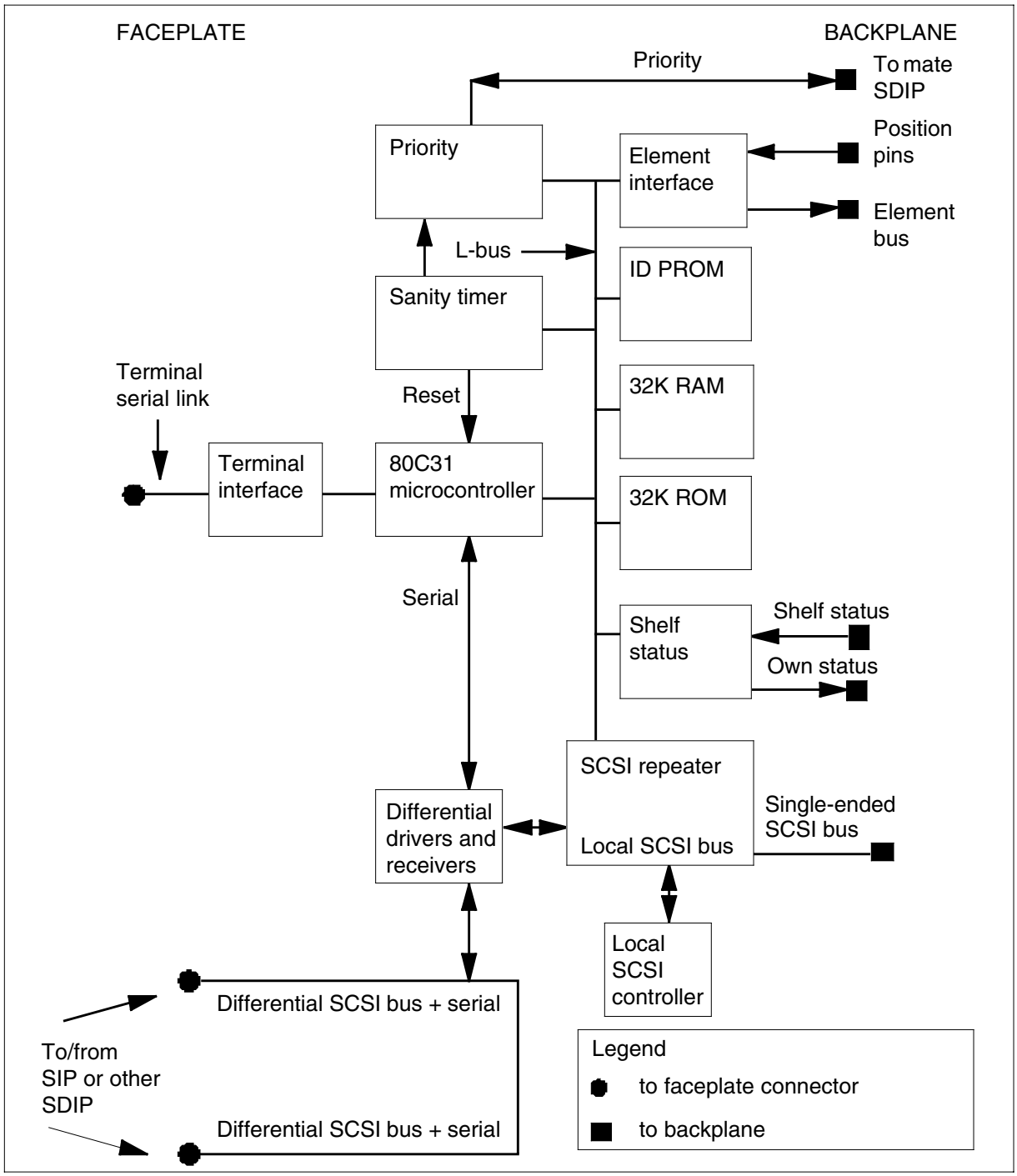
## **NT9X89BA** (continued)

- ROM
- RAM
- differential drivers and receivers
- RS232 terminal interface
- sanity timer
- priority

The relationship between the functional blocks appears in the following figure.

# **NT9X89BA** (continued)

**NT9X89BA functional blocks**



## NT9X89BA (continued)

### Small computer system interface repeater

The SCSI repeater performs two–way conversions between differential SCSI signals and single–ended SCSI signals. The microcontroller activates the repeater.

### Shelf status interface

The shelf status interface transmits shelf status data from the storage–device circuit pack and the SDIPs to the status registers.

### Light–emitting diodes

Two LEDs are present on the SDIP faceplate. One LED has a label IN USE and one LED has a label FAULT. A reset of the microcontroller lights the two LEDs. The initialization firmware extinguishes the two LEDs. A sanity error also lights the FAULT LED. Software controls the LEDs at all other times.

### Location block

The location block interprets information the device shelf provides. The SDIP uses the information to determine the location in the device shelf. The information contains slot, quadrant, shelf and cabinet location.

### Identification PROM

The ID PROM contains hardware and software vintage data that the processor reads for initialization and maintenance.

### Single–chip microcontroller

The single–chip microcontroller controls the functions of the SDIP. One of the functions is to read data from and write data to different blocks. The single chip microcontroller performs this function with the local bus (L–bus). The UART performs the serial data communication with the SIP, under control of the microcontroller.

### Universal asynchronous receiver/transmitter

The microcontroller uses the UART for serial communication with other devices. The UART has two independent channels. One channel provides a serial link to the SIP for the transfer of status and control information. This function is the main function of this channel. The RS232 debug terminal interface uses the second channel.

### Local SCSI interface

The local SCSI interface helps the FP maintenance process in SCSI bus fault isolation. The interface can read from and write to the local SCSI bus under control of the microcontroller, with the exception of the RST- line. The RST- line is not tracked to this chip.

### ROM

The ROM contains the firmware for the microcontroller.

### RAM

The system uses RAM for data storage.

### Differential drivers and receivers

The differential drivers and receivers perform conversion between differential serial signals and single–ended serial signals. A differential serial link that connects to the SIP travels with the differential SCSI bus through the cabinet. The signal conversion is required for communication between UART and the SIP of the SDIP. This requirement occurs because the UART can only provide only single–ended serial capability.

### RS232 terminal interface

The RS232 terminal interface provides a connection between the SDIP UART and an external terminal at RS232 levels. The UART is under the control of the microcontroller. This connection is for hardware debugging.

### Sanity timer

The sanity timer block checks the sanity of the microcontroller. The sanity timer does not always receive a reset from the microcontroller with a specified duration. When this condition occurs, the microcontroller is not considered sane and the sanity timer circuit attempts to reset the microcontroller.

### Priority

The priority block controls which SDIP has priority in the quadrant and which SDIP is active. An active SDIP can read from and write to the mass storage device of the quadrant. The priority blocks on the two SDIPs in a quadrant operate together. The blocks make sure that only one SDIP has priority at any one time.

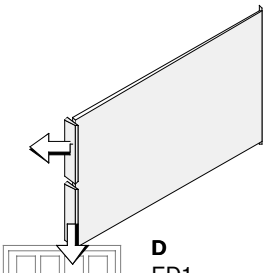
## Signaling

### Pin numbers

The pin numbers for the NT9X89BA appear in the following figures.

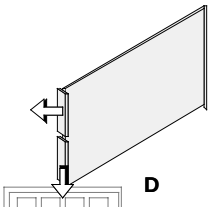
# **NT9X89BA** (continued)

### NT9X89BA pin numbers (Part 1 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 1 | ED1 | ED0 | | |
| 2 | ED3 | ED2 | | |
| 3 | ED5 | ED4 | | |
| 4 | | PCEN– | ED6 | |
| 5 | EA3 | | | |
| 6 | EA1 | EA2 | | |
| 7 | ED7 | EA0 | | |
| 8 | | | | |
| 9 | ERD– | EA4 | | |
| 10 | | MBEN– | EWR– | |
| 11 | PRIROUT– | | PRIRIN– | |
| 12 | ENABLE– | | | |
| 13 | | | | |
| 14 | | | | |
| 15 | | | | SH0 |
| 16 | | | | SH1 |
| 17 | | | | |
| 18 | | | | |
| 19 | | | | |
| 20 | | | | |
| 21 | | CPPR0 | | |
| 22 | | PB2PR0 | PWPR0 | |
| 23 | | | PB1PR0 | |
| 24 | | | | |
| 25 | | | | |
| 26 | CAB2PR0 | CAB1PR0 | | |
| 27 | RPTR1EN0 | | PB2SAN0 | |
| 28 | | | | PB1SAN0 |
| 29 | RPTR2EN0 | | | |
| 30 | SPARE | | | |
| 31 | | | | |
| 32 | | SPARE | | |
| 33 | SPARE | | SPARE | |
| 34 | | | | SPARE |
| 35 | | SPARE | | |
| 36 | | | | |
| 37 | | | | |
| 38 | | PB1PR1 | | |
| 39 | | | CPPR1 | |
| 40 | | | | PWPR1 |
| 41 | | PB2PR1 | | |
| 42 | | | | |
| 43 | | | | |
| 44 | | CAB1PR1 | | |
| 45 | | | PB2SAN1 | |

**NT9X89BA pin numbers (Part 2 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 46 | | | | PB1SAN1 |
| 47 | | CAB2PRI | | |
| 48 | | | | |
| 49 | | | | |
| 50 | | SPARE | | |
| 51 | | | RPTR2EN1 | |
| 52 | | | | RPTR1EN1 |
| 53 | | SPARE | | |
| 54 | | | | |
| 55 | | | | |
| 56 | SPARE | SPARE | | |
| 57 | | | SPARE | |
| 58 | | | | SPARE |
| 59 | | | | CAB0 |
| 60 | | | | CAB1 |
| 61 | QUAD0 | PB1PR2 | CPPR2 | |
| 62 | QUAD1 | PB2PR2 | TYPE0 | PWPR2 |
| 63 | SPARE | CAB1PR2 | TYPE1 | |
| 64 | | RPTR2EN2 | PB2SAN2 | |
| 65 | | | RPTR1EN2 | PB1SAN2 |
| 66 | | SPARE | | CAB2PR2 |
| 67 | | SPARE | SPARE | |
| 68 | | PLN | SPARE | SPARE |
| 69 | | PB2PR3 | PWPR3 | |
| 70 | | CAB1PR3 | PB1PR3 | |
| 71 | | | PB2SAN3 | CPPR3 |
| 72 | | RPTR2EN3 | | PB1SAN3 |
| 73 | | SPARE | RPTR1EN3 | |
| 74 | | HW2 | SPARE | CAB2PR3 |
| 75 | | SPARE | HW1 | SPARE |
| 76 | | SPARE | SPARE | HW0 |
| 77 | | | | |
| 78 | | BSNTY | | |
| 79 | PBPRES | BCBLP | | |
| 80 | | BRPTR | | |
| 81 | SDB3– | | | SDBP– |
| 82 | | SDB2– | | |
| 83 | SDB7– | | SDB1– | |
| 84 | | SDB6– | | SDB0– |
| 85 | | | SDB5– | |
| 86 | SATN– | SRST– | | SDB4– |
| 87 | SREQ– | | SMSG– | |
| 88 | | SACK– | | SC_D– |
| 89 | | | SBSY– | |
| 90 | SI_O– | | | SSEL– |

# NT9X91AA

## Product description

The NT9X91AA power converter provides regulated and protected output of +5V and +12V to the DMS-100 SuperNode storage devices. Each NT9X91AA interfaces with DMS-100 office alarm circuits with the use of the frame supervisory panel (FSP) NT9X03AA.

## Functional description

The NT9X91AA provides outputs of +12V at a maximum current of 10A, and 5.1V at a maximum current of 30A. The input to the converter is a nominal battery voltage of -48V.

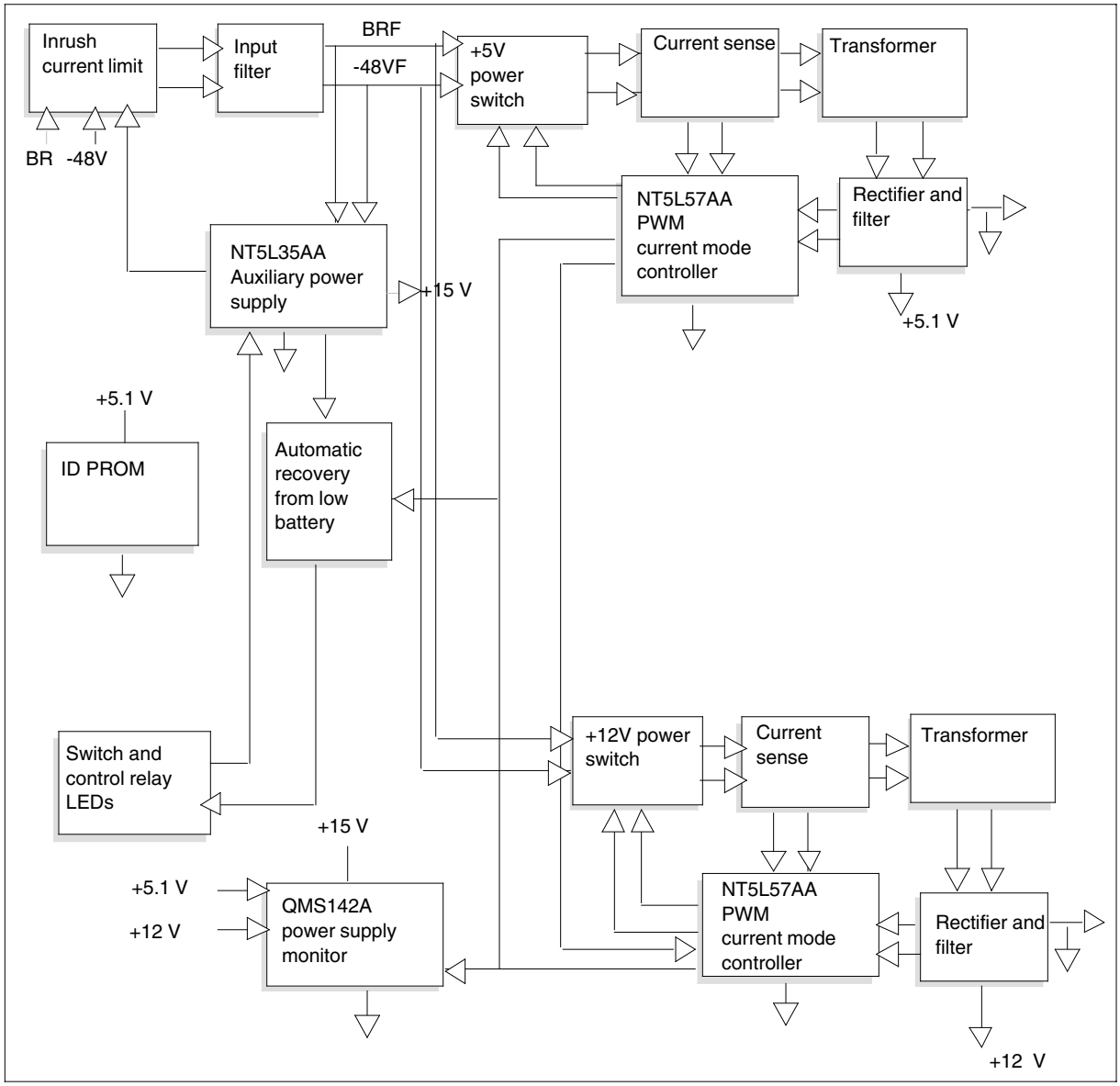
### Functional blocks

The NT9X91AA has the following functional blocks:

- inrush current limit
- input filter
- auxiliary power supply and automatic recovery from low battery (ARLB)
- power processing
- power switch, current sense, and control
- power transformer, rectifier, and filter
- output monitoring
- identification PROM
- switch, control relays and light-emitting diode (LED)

The relationship between the functional blocks appears in the following figure.

**NT9X91AA functional blocks**




## Inrush current limit

The maximum inrush current limit is 3.75A at converter startup. This maximum limit also occurs when the system removes power and applies power again.

## Input filter

The input filter provides common and differential mode filtering for the switching power train.

## **NT9X91AA** (continued)

### Auxiliary power supply and automatic recovery from low battery

An NT5L35AA hybrid provides the auxiliary power for the control circuits. This hybrid provides an isolated and regulated output of +15V. This hybrid controls the automatic recovery from low battery (ARLB). The ARLB is a feature of the power supply that allows the converter to recover from loss of input power. This condition occurs when the converter is in operation when the loss of power occurs.

### Power processing

The NT9X91AA generates two outputs +5.1V and +12V with two semi-independent push-pull dc-dc converter circuits. The 5.1-V pulse width modulator (PWM) controller circuit provides a master clock and a sawtooth waveform to the 12V PWM.

### Power switch, current sense and control

This entire block is duplicated. One block is for the +5V output and one block is for the +12V output. The power switches are two switching field-effect transistors (FET) configured for push-pull operation. These switches step down the output of the input filter. An NT5L57AA current-mode controller controls the two switching FETs. This hybrid controller regulates the output voltage. The controller uses voltage feedback and current information that the current-sense transformer provides to control the output voltage.

### Power transformer, rectifier and filter

This block is duplicated. One block is for the +5V output and one block is for the +12V output. The power transformer processes the ac waveform the that the switching action of the FETs generates. The system rectifies and filters output.

### Output monitoring

The QMS142A power supply monitor checks for undervoltage and overvoltage on the two outputs of the supply. When the monitor detects an undervoltage or an overvoltage condition, the monitor shuts down the converter and disables ARLB.

### Identification PROM

The ID PROM allows the system software to determine the type and release of the power supply.

### Switch and control relay and light-emitting diodes

The NT9X91AA has a faceplate ON/OFF switch and a faceplate power converter fail LED. The NT9X91AA has a provision through backplane connectors for a remote switch and a remote fail LED. The system provides relays for remote start, remote stop and remote alarm signaling.

# Signaling

## Pin numbers

The pin numbers for the NT9X91AA appear in the following tables.

Explanations of the abbreviations that appear in the tables appear below:

- address (A)
- data (D)
- chip select (CS)
- ring alarm sense (RAS)
- There is no converter (NOCON)
- There is no connection on the backplane. The converter has a signal on this pin (N/C)
- shutdown (SD)
- power lock on converter (PLOCK)
- remote start converter (REM.START)
- remote shutdown converter (REM.SHDN)

**Connector P1 (Sheet 1 of 2)**

| Row | Column Z | Column B | Column D | Column F |
|---|---|---|---|---|
| 2 | | SD | CS-5 | EXT.SW.OFF |
| 4 | A2-5 | A1-5 | A0-5 | A3-5 |
| 6 | D6-5 | D5-5 | D4-5 | D7-5 |
| 8 | D2-5 | D1-5 | D0-5 | D3-5 |
| 10 | EXT.SW.ON | RAS-NC | RAS-C | EXT.SW |
| 12 | BR.ABS | -48VABS | EXT.LED | RAS/NO |
| 14 | NOCONA | +12SENSE | SLM | NOCONB |
| 16 | +12V | +12V | +12V | +12V |
| 18 | GND | GND | GND | GND |
| 20 | +12V | +12V | +12V | +12V |
| 22 | GND | GND | GND | GND |
| 24 | +5V | +5V | +5V | +5V |

## **NT9X91AA** (continued)

**Connector P1 (Sheet 2 of 2)**

| Row | Column Z | Column B | Column D | Column F |
|---|---|---|---|---|
| 26 | GND | GND | GND | GND |
| 28 | +5V | +5V | +5V | +5V |
| 30 | GND | GND | GND | GND |
| 32 | +5V | +5V | +5V | +5V |

**Connector P2**

| Row | Column Z | Column B | Column D | Column F |
|---|---|---|---|---|
| 2 | GNDSENSE | GNDSENSE | GND | GND |
| 4 | +5V | +5V | +5V | +5V |
| 6 | GND | GND | GND | GND |
| 8 | +5V | +5V | +5V | +5V |
| 10 | GND | GND | GND | GND |
| 12 | +5V | +5V | +5V | +5V |
| 14 | GND | GND | GND | GND |
| 16 | +5V | +5V | +5V | +5V |
| 18 | GND | GND | GND | GND |
| 20 | +5V | +5V | +5V | +5V |
| 22 | -48V | -48V | -48V | +5SENSE |
| 24 | -48V | -48V | -48V | -48V |
| 26 | BR | BR | BR | N/C |
| 28 | BR | BR | BR | BR |
| 30 | +12VTEST | +5VTEST | N/C | +15V |
| 32 | REM.START | REM.SHDN | -48T | PLOCK |

# Technical data

## Power requirementsInput specifications

The nominal voltage is -48V, and ranges between a minimum of -42V and a maximum of -56V. The maximum current is 9A. The converter operates at the low-battery shutdown voltage of -41.5 ± .5V. The converter must start at the low-battery recovery voltage of -43.5 ± 0.5V.

## Output specifications

The output specifications for +12V appear in the following table.

**+12 V output**

| Parameter | Value |
|---|---|
| Voltage (0-2 A) | +12 V ±2% |
| Voltage (2-10 A) | +12 V ±7% |
| High voltage shutdown | +14 V ±1 V |
| Low voltage shutdown | +10 V ±1 V |
| Steady state ripple | 50 mV rms |
| Maximum current | 10 A |
| Minimum current | 0.5 A |
| Current limit | 13 A ±1 A |
| Transient response (±7 A step, 0.5 A minimum load) | 90 mV peak to peak |

The output specifications for +5.1V appear in the following table.

**+5.15 V output (Sheet 1 of 2)**

| Parameter | Value |
|---|---|
| Voltage | +5.1 V ±2% |
| High voltage shutdown | +6.5 V ±0.5 V |
| Low voltage shutdown | +4.3 V ±0.3 V |
| Steady state ripple | 50 mV rms |
| Maximum current | 30 A |

## **NT9X91AA** (end)

**+5.15 V output (Sheet 2 of 2)**

| Parameter | Value |
|---|---|
| Minimum current | 1 A |
| Current limit | 35A ±2 A |

# NT9X91AB

## Product description

The NT9X91AB power converter. The NT9X91AB provides regulated and protected output of +5V and +12V to the DMS–100 SuperNode storage device shelf and the Meridian mail shelves. The NT9X91AB uses input battery voltage of –48V or –60V to operate. The card is provisioned with the frame supervisory panel (FSP) NT9X03AA.

## Functional description

The NT9X91AB provides outputs of +12V at a maximum current of 18A and +5V at a maximum current of 55A.

### Functional blocks

The NT9X91AB contains the following functional blocks:

- inrush current limit
- input filter
- auxiliary power supply and automatic recovery from low battery (ARLB)
- power processing
- power switch, current sense and control
- power transformer, rectifier, and filter
- output monitoring
- identification PROM
- load sharing
- redundancy
- switch, control relays, and light–emitting diode (LED)

### Inrush current limit

The maximum inrush current limit is 3.75A at converter startup. The maximum inrush current limit is also 3.75A when you remove and apply power again.

### Input filter

The input filter provides common and differential mode filtering for the switching power train.

### Auxiliary power supply and automatic recovery from low battery

An NT6L38AA hybrid provides the auxiliary power for the control circuits. This hybrid provides an isolated and regulated output of +15.5V and controls the automatic recovery from low battery (ARLB). The ARLB is a feature of

## **NT9X91AB** (continued)

the power supply. The ARLB allows the converter to recover from loss of input power, if the converter is operating when the power is lost.

### Power processing

The NT9X91AB uses two semi–independent push–pull dc–to–dc converter circuits to generate two outputs +5.15V and +12.0V. The 5.15V pulse width modulator (PWM) controller circuit provides a master clock and a sawtooth waveform to the 12.0V PWM.

### Power switch, current sense and control

The system duplicates the complete block, one for the +5V output and one for the +12V output. The power switches contain two switching field–effect transistors (FET) configured for push–pull operation. The power switches step down the output of the input filter. An NT5L57AA current–mode controller controls the two switching FETs. The NT5L57AA is a hybrid controller. The NT5L57AA regulates the output voltage by direct voltage feedback and by current information the current–sense transformer provides.

### Power transformer, rectifier and filter

The system duplicates the block, one for the +5V output and one for the +12V output. The power transformer processes the ac waveform that the switching action of the FETs generates. The power transformer rectifies and filters the output.

### Output monitoring

The QMS142A power supply monitor determines undervoltage and overvoltage on both outputs of the supply. If the monitor detects an undervoltage or an overvoltage condition, the monitor turn off the converter off and disables the ARLB.

### Identification PROM

The ID PROM allows the system software to determine the type and release of the power supply.

### Load sharing

The system duplicates the block, one for the +5V output and one for the +12V output. The PWM hybrid produces a voltage signal proportional to the output current. In load–sharing applications, the signal ties to a common node between the converters that share the load. The signal ties to a common node through a resistance.

### Redundancy

In load–sharing applications, one converter can supply the complete load requirement of the half–shelf when the mate converter shuts down.

### Switch and control relay and light–emitting diodes

The NT9X91AB contains the following parts:

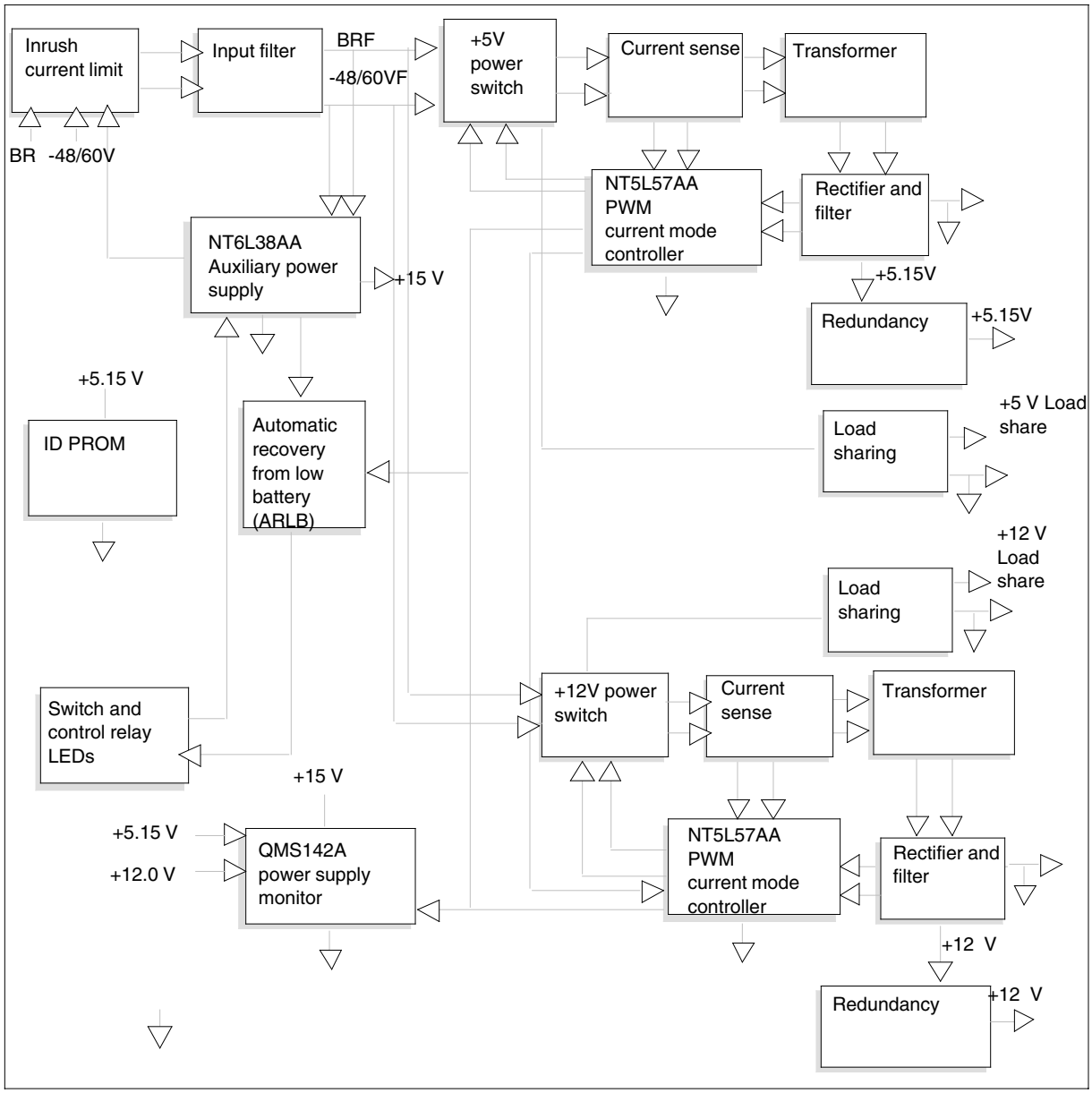
- a faceplate ON/OFF switch
- a faceplate power converter fail LED
- provision through backplane connectors for both a remote switch and remote fail LED

The NT9X91AB provides relays for remote start, remote stop, and remote alarm signaling.

The relationship between the functional blocks appears in the following figure.

## **NT9X91AB** (continued)

### NT9X91AB functional blocks




# Signaling

## Pin numbers

The pin numbers for the NT9X91AB appear in the following tables. The following list describes the abbreviations that the table uses:

- address (A)
- data (D)

- chip select (CS)
- remote alarm sense (RAS)
- no converter (NOCON)
- no connection on the backplane but the converter has a signal on this pin (N/C)
- shutdown (SD)
- power lock–on converter (PLOCK)
- remote start converter (REM.START)
- remote shutdown converter (REM.SHDN)

**Connector P1**

| Pin | Z | B | D | F |
|---|---|---|---|---|
| 2 | 12ISHARE | SD | CS–5 | EXT.SW.OFF |
| 4 | A2–5 | A1–5 | A0–5 | A3–5 |
| 6 | D6–5 | D5–5 | D4–5 | D7–5 |
| 8 | D2–5 | D1–5 | D0–5 | D3–5 |
| 10 | EXT.SW.ON | RAS/NC | RAS/C | EXT.SW |
| 12 | BR.ABS | –ABS | EXT.LED | RAS/NO |
| 14 | NOCON–A | +12SENSE | SLM | NOCON-B |
| 16 | +12V | +12V | +12V | +12V |
| 18 | LR | LR | LR | LR |
| 20 | +12V | +12V | +12V | +12V |
| 22 | LR | LR | LR | LR |
| 24 | +5V | +5V | +5V | +5V |
| 26 | LR | LR | LR | LR |
| 28 | +5V | +5V | +5V | +5V |
| 30 | LR | LR | LR | LR |
| 32 | +5V | +5V | +5V | +5V |

## **NT9X91AB** (continued)

**Connector P2**

| Pin | Z | B | D | F |
|---|---|---|---|---|
| 2 | GNDSENSE | GNDSENSE | LR | LR |
| 4 | +5V | +5V | +5V | +5V |
| 6 | LR | LR | LR | LR |
| 8 | +5V | +5V | +5V | +5V |
| 10 | LR | LR | LR | LR |
| 12 | +5V | +5V | +5V | +5V |
| 14 | LR | LR | LR | LR |
| 16 | +5V | +5V | +5V | +5V |
| 18 | LR | LR | LR | LR |
| 20 | +5V | +5V | +5V | +5V |
| 22 | –BAT | –BAT | –BAT | +5SENSE |
| 24 | –BAT | –BAT | –BAT | –BAT |
| 26 | BR | BR | BR | N/C |
| 28 | BR | BR | BR | BR |
| 30 | +12VTEST | +5VTEST | +5ISHARE | +15V |
| 32 | REM.START | REM.SHDN | –BT | PLOCK |

# Technical data

### Power requirements

The nominal voltage is –48V or –60V. The nominal voltage ranges from a minimum of –42.0V to a maximum of –75V. The maximum current is 13A. The converter operates at the low–battery shutdown voltage. The converter must start at the low–battery recovery voltage. The low–battery shut down voltage is –38.2 ±1.0V. The low–battery recovery voltage is –40.7 ±1.14V.

### Output specifications

The output specifications for the +12V output appear in the following table.

**+12 V output**

| Parameter | Value |
|---|---|
| Voltage | +12.0V ±2% |
| High voltage shutdown | +14.0V ±1V |
| Low voltage shutdown | +10.0V ±1V |
| Ripple | 50mV rms |
| Maximum current | 18A |
| Minimum current | 2A |
| Current limit | 20A ±1A |

The output specifications for the +5.15V output appear in the following table.

**+5.15 V output**

| Parameter | Value |
|---|---|
| Voltage | +5.15V ±2% |
| High voltage shutdown | +6.5V ±0.5V |
| Low voltage shutdown | +4.3V ±0.5V |
| Ripple | 50mV rms |
| Maximum current | 55A |
| Minimum current | 2.0A |
| Current limit | 62A ±2A |

## NT9X95AA

## Product description

The NT9X95AA 42 in. (1.067 m) cabinet is an improved version of the current NT9X01 42 in. cabinet. The NT9X95AA meets global regulatory and customer specifications, like compliance with electromagnetic interference (EMI) standards. The NT9X95AA provides additional FiberWorld improvement.

The development of the NT9X95AA cabinet is similar to improvements and changes to products, like cabinets for standard frames. Examples of cabinets for standard frames are the cabinetized power distribution center (CPDC), NTRX31AA and the cabinetized input/output equipment frame (CIOE), NTRX33AA.

The NT9X95AA contains the following improvements:

- modified framework based on need for EMI-compliance and commitment to FiberWorld
- modular cooling unit
- incorporation of horizontal through lineup cabling
- enhanced design for facilitating hot slide insertions
- introduction of an enhanced cabling cabinet (NT0X35CC)

The NT9X95AA cabinet accommodates different functional sets of 42 in. shelves. The functional sets of 42 in. shelves are cabinet products.

The NT9X95AA cabinet is backward compatible with SuperNode shelf based products in the following areas:

- software (including alarming)
- electrical hardware (shelf and bulkhead Printed circuit packs (PCP))
- shelf level mechanical hardware
- frame supervisory panel (sheetmetal or wireform)
- signal cables

The NT9X95AA cabinet does not affect the electrical signal or software architecture of current products. The NT9X95AA provides power to the shelves in a different way than the current NT9X01 provides power. The cabinet and the fans are inside the EMI (Faraday) cage.

## Parts

The NT9X95AA 42 in. cabinet contains the following types of parts:

- framework
- shielding
- cabling
- power control
- cooling system
- contents

Shielding includes doors, panels, and the bulkheads. Power control refers to the frame supervisory panel (FSP). Contents refers to the shelves. The shelves define the function of the cabinet unit or product. The following pages describe the different parts of the NT9X95AA.

### Framework

The framework is a welded steel structure that has a base, vertical uprights and a top assembly.

### Doors

Two steel cabinet doors attach to the front and rear of the framework. The doors are larger than the doors on previous cabinets. The doors provide the following:

- access to internal equipment and cabling
- protection against accidental electrostatic discharge (ESD) damage
- aesthetic features
- areas on door caps for product identification labels

### Endpanels

Endpanels complete the electromagnetic compatibility (EMC) enclosure for cabinets at the ends of a lineup or in a standalone installation.

### Cooling unit and air filter

The cooling unit is a steel enclosure that contains three blower assemblies. The blower assemblies can cool the contents of the cabinet. The cooling unit is modular. You can replace the cooling unit. The cooling unit is easy to install and maintain.

## NT9X95AA (continued)

The cooling unit has an air filter at the air inlet. You can replace the air filter. The air filter provides easy access and eliminates the need for a pre-filter. You must replace this filter in intervals of six weeks.

### Cabling

The NT9X95AA cabinet allows cables to run from inside the cabinet down to the base of the cabinet. The cables run through a hole in the side of the cabinet to the next cabinet(s) in the lineup. The cabling design horizontal cabling. The lineup form the EMC cage. The EMC cage allows the cables to run from cabinet to cabinet without EMC filtering.

The holes in the side of the cabinets are approximately 26 $in.^2$. Horizontal cabling allows battery or alarm cables to run without a filter in the EMI cage.

The new cabinet supports overhead and under floor cabling. The cables that exit the EMI cage run through a bulkhead in the left rear or right rear of the cabinet. The signals on the cables are filtered at the bulkheads. This cabling follows current cabling practice. This cabling does not cause important changes to the office cabling method.

You must seal the hole in the side of the cabinet to the next cabinet for horizontal cabling. If you do not seal the hole, you must close the cabinet. The provisionable cabling cabinet adds two additional setup possibilities. You can set up cabinets in a line of cabinets or standalone. The following section describes cabling and no cabling cabinet solutions.

### NT0X35CC cabling cabinet

Operating company personnel can provision the NT0X35CC cabling cabinet for the NT9X95AA cabinet. The NT0X35CC cabinet provides additional cabling space for ABAM cabling in high-speed interface (HSI) and enhanced network (ENET) applications. This cabinet provides additional cabling space when heavy input/output (I/O) requirements occur.

To set up cabinets in a line with a cabling cabinet, provision an EMI tunnel. The tunnel seals one end of the horizontal cable-way in the NT9X95AA cabinet to the hole that corresponds. The hole that corresponds is in the cabinet next to the cabling cabinet. The tunnel continues the EMI cage along the lineup.

To set up a stand-alone cabinet, provision cable tunnel covers to plug the horizontal cable holes.

Refer to section NT0X35CC, Cabling cabinet in this document.

If you do not use a cabling cabinet, cabinet joining kits provide a continuous EMI cage along a lineup. The horizontal cable tunnel is not completely sealed between cabinets. The cabinet joining kits seal the edge of the cabinets together.

### Bulkheads

The bulkheads form part of the EMI cage around the equipment. The bulkheads provide a place to mount filter Process control blocks (PCB) and optional power filters. Each bulkhead has section near the bottom that you can remove. This section facilitates hot slide installation of equipment in a lineup that uses horizontal cabling.

### Frame supervisory panel

The NT9X95AA cabinet uses the NT9X03AA SuperNode FSP. The new wireform FSP provides a jack for an ESD wrist strap grounding at the front and rear. The current sheetmetal FSP provides one ESD ground point in the front.

The FSP cables to an alarm lamp above the center of the front doors. The FSP can indicate problems in the cabinet with the doors open or closed. The FSP bulkhead panel provides improved access to the alarm connectors.

### NT9X95AA cabinet products

The NT9X95AA cabinet contains the following products:

- SuperNode core (NT9X01JB) - Refer to the figure.
- Link interface module (LIM) (NT9X70BB) - Refer to the figure.
- Enhanced network (ENET) (NT9X05AC) - Refer to the figure.

### SuperNode - NT9X01JB

The SuperNode cabinet contains the following parts:

- DMS-bus
  - — message switch shelf
- DMS-core
  - — active processor
  - — inactive processor
- system load module (SLM)
  - — magnetic tape cartridge drive
  - — hard disk controller and drive

## **NT9X95AA** (continued)

### DMS-bus

The DMS-bus is a message switch. The DMS-bus transports messages from port to port across the transaction bus (TBUS). The TBUS data width is 32 bits with a clock of 4.096 MHz. The TBUS can handle approximately 250 000 64-byte messages each second. Port buffers can handle messages to a maximum of 2 Kbytes in length. Messages are load-shared across both planes of the DMS-bus. If one plane fails, the other plane can handle all the load.

### DMS-core

The DMS-core handles the less real-time-intensive call processing tasks of digit translation, billing, and network routing. The DMS-core also performs the central administrative tasks. The DMS-core distributes software to the switch processors and monitors the sanity of the switch processors. The DMS-core performs these functions for all of the processors on the switch.

The DMS-core contains two synchronously matched processors. Both processors receive the same inputs and perform the same calculations. One processor is active. The active processor is the source of output. The other processor is not active. The outputs of the processor that is not active are inhibited. Comparison logic circuits compare the output of the two processors. If the comparison logic circuits detect a problem, comparison logic circuits select one of the units to activate.

### System load module

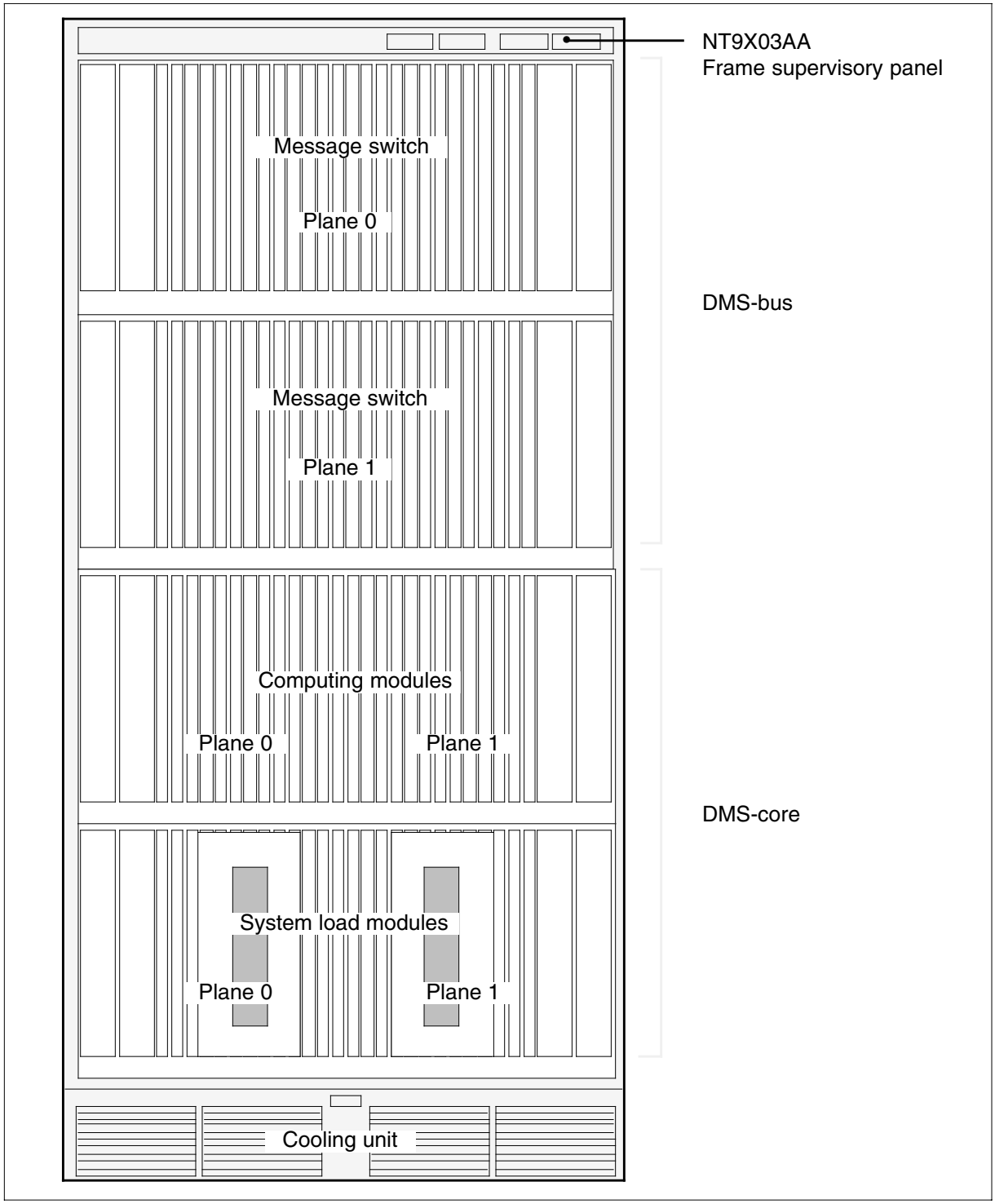
The SLM contains a tape cartridge and hard disk drive. The SLM connects to the DMS-core with an extension of the DMS-core processor bus. The SLM loads software in the office and records the software in the switch according to a schedule.

## Design

The design of the SuperNode cabinet appears in the following figure.

## **NT9X95AA** (continued)

**SuperNode cabinet**



## **NT9X95AA** (continued)

### Link interface module (LIM) - NT9X70BB

The LIM contains the following parts:

- local message switch (LMS) shelf
- three link interface shelves (LIS)
  - — three LISs hold a maximum of 36 link interface units (LIU)

The LMS shelf contains the frame bus (F-bus) hardware and two LMS units.

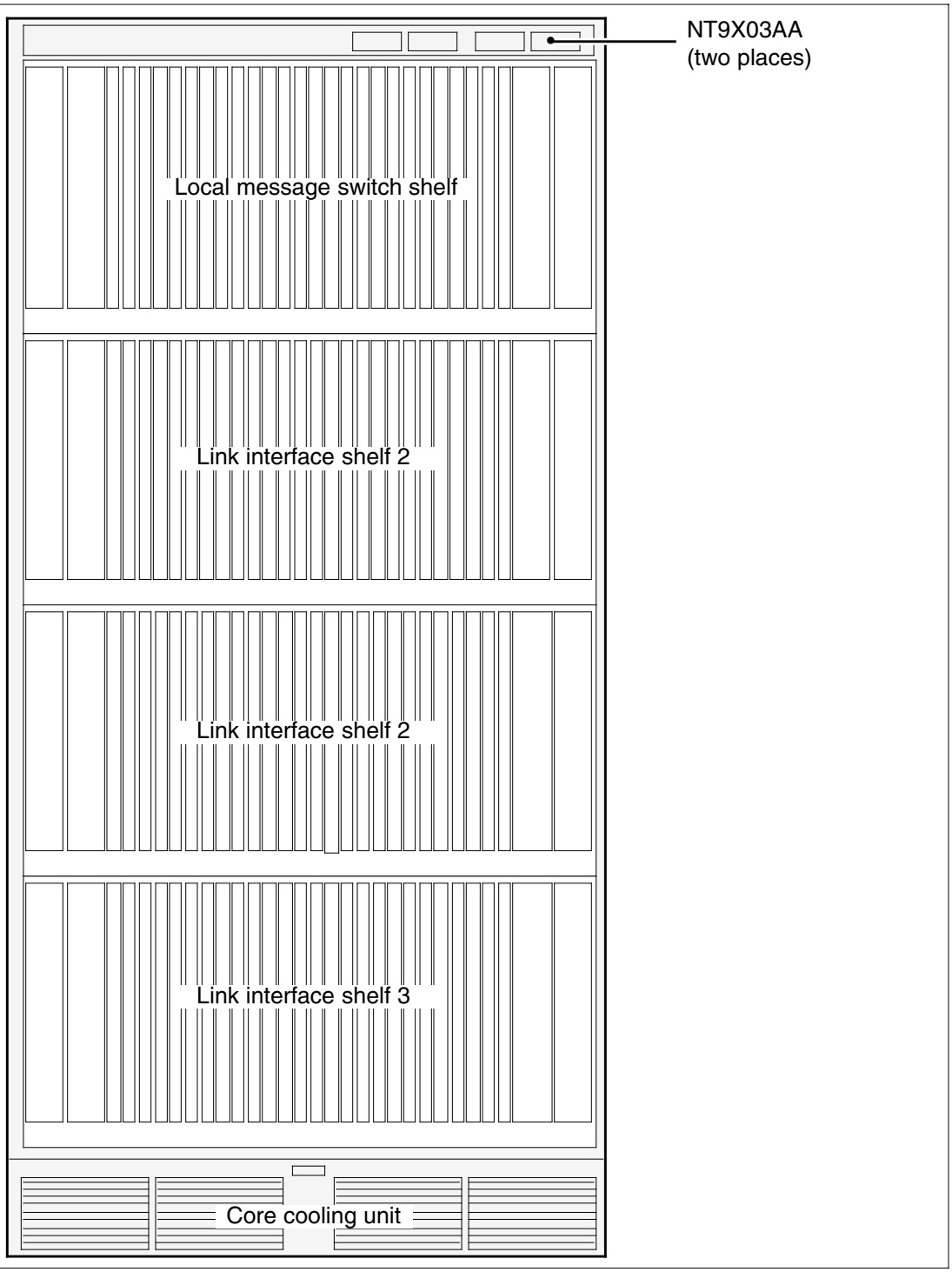
The link interface shelf contains the F-bus hardware and a maximum of twelve LIUs. An F-bus connects each LIU to each LMS.

## Design

The design of the LIM cabinet appears in the following figure.

## **NT9X95AA** (continued)

**LIM cabinet**



## **NT9X95AA** (continued)

### Enhanced network (ENET) - NT9X05AC

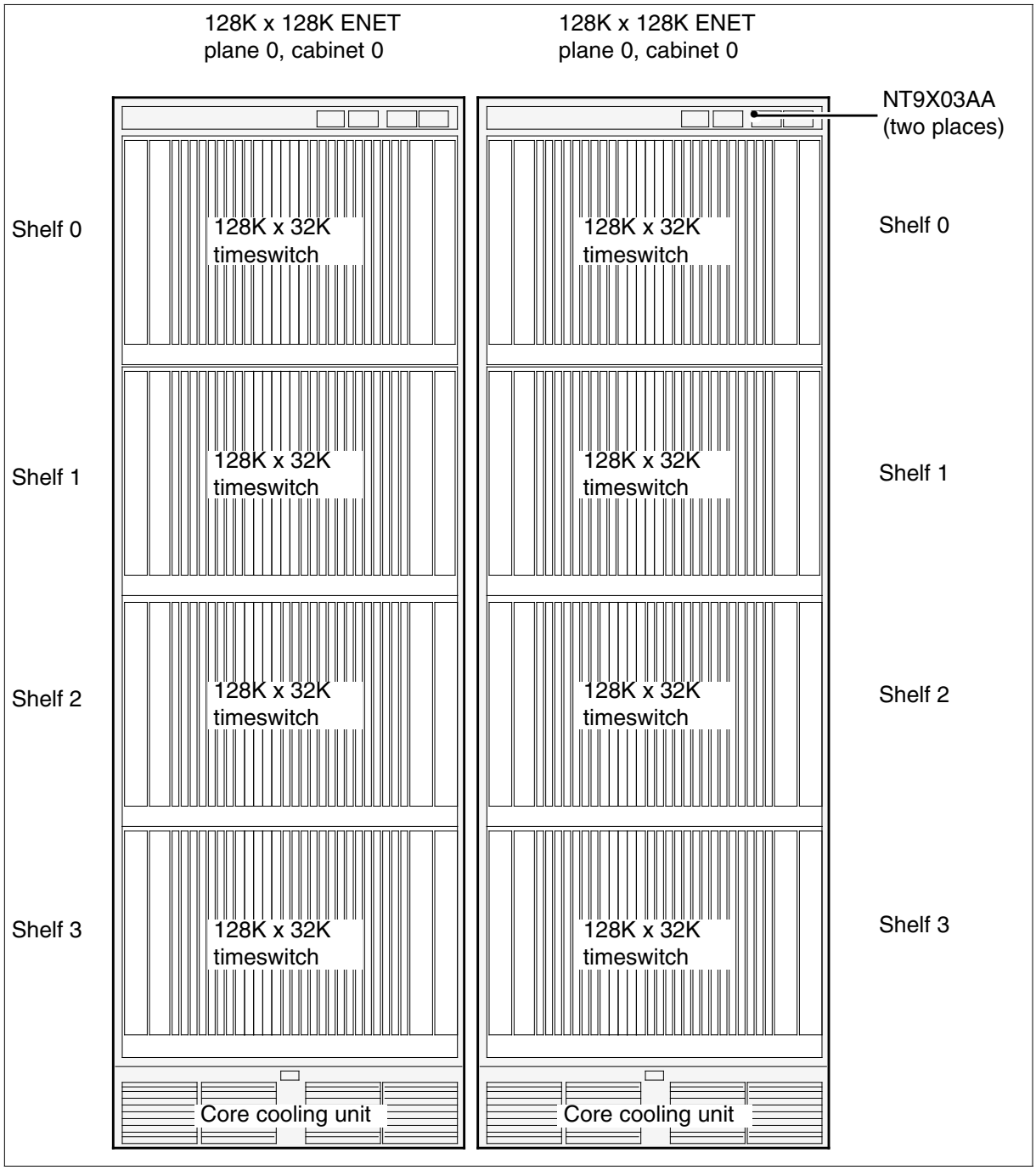
Two cabinets contain the 128K x 128K dual plane ENET. Plane 0 is in one cabinet and plane 1 is in the other cabinet. Each cabinet has four shelves and terminates 64 DS512 fibers. Each shelf receives 32K (64 x 512) channels from external sources. Each shelf transmits 32K channels to external sources.

The 128K x 32K timeswitch has 128K inputs and 32K outputs. The 128K inputs are the inputs from all of the DS512 fibers that terminate on the cabinet. The 32K outputs are the outputs to the 32K channels on the DS512 fibers that terminate on the shelf. Vertical buses are present between the shelves to distribute the DS512 inputs from each shelf to all the other shelves.

## Design

The design of the ENET cabinets appear in the following figure.

**ENET cabinets**



# NT9X95SA

## Product description

The NT9X95SA provides surge protection and alarm circuits for the C42 cooling unit.

### Location

The C42 cooling unit subassembly contains the NT9X95SA.

## Functional description

The NT9X95SA controls current surges in two 33,000-uF noise-filter capacitors in the cooling unit. The noise-filter capacitors are mounted off the NT9X95SA. This card functions as an alarm interface for the blower alarms in the cooling unit. This card functions as an interconnection point for the four blower assemblies and the filter wiring.

### Functional blocks

The NT9X95SA has the following functional blocks:

- capacitor surge current control
- alarm interface

### Capacitor surge current control

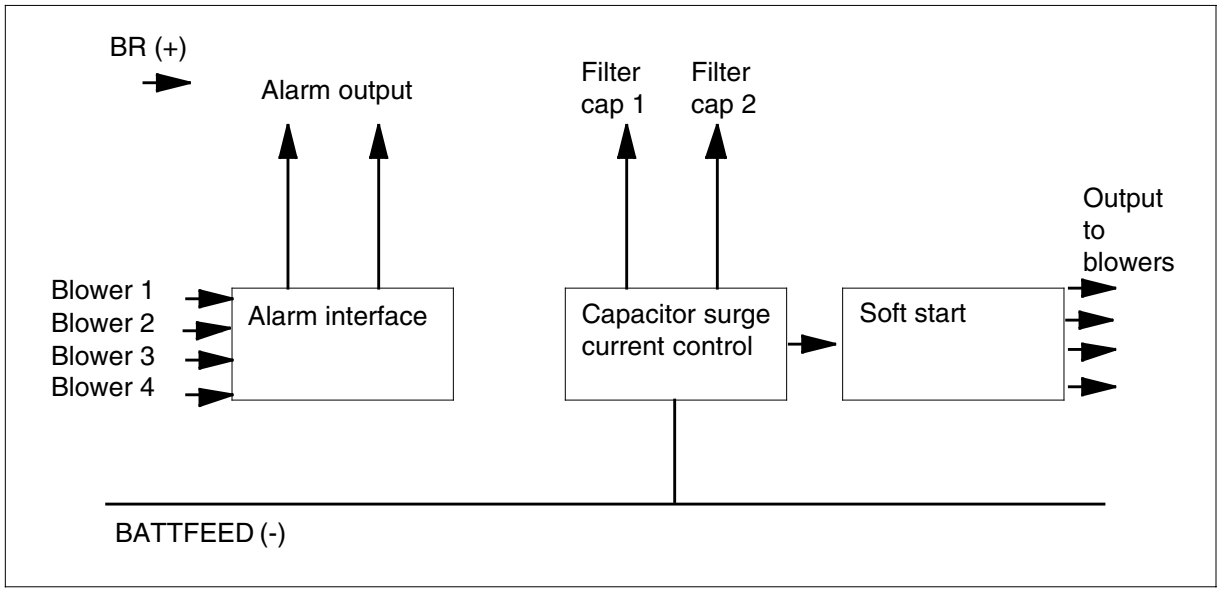
This block contains a field effective transistor (FET) in series with each of the two external filter capacitors. The FETs connect the capacitors to the circuit under normal operation. If the input voltage increases suddenly, the FETs limit the capacitor charging currents to a safe value. When the capacitors are charged, the FETs resume normal operation.

### Alarm interface

This block monitors the alarm outputs from the blowers. If a blower assembly produces an alarm output, an LED that corresponds on the NT9X95SA glows. A relay is deactivated to sound the external alarm.

The relationship of the functional blocks appears in the following figure.

**NT9X95SA functional blocks**




## Signaling

### Pin numbers

The connections for connector P1 appear in the following table.

**Connector P1 to power (filtered)**

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | Capacitor C6 + | 6 | Alarm (open) |
| 2 | Battery return | 7 | Battery feed B |
| 3 | Capacitor C6- | 8 | Alarm (closed) |
| 4 | Battery feed A | 9 | Alarm (closed) |
| 5 | Alarm (common) | | |

## **NT9X95SA** (end)

The connections for connectors P2, P3, P4, and P5 appear in the following table.

**Connectors P2, P3, P4, and P5 to blowers 1, 2, 3, and 4**

| Pin | Function |
|---|---|
| 1 | Alarm (emitter) |
| 2 | Alarm (collector) |
| 3 | Battery feed (-) |
| 4 | Battery return (+) |

The connections for connector P6 appear in the following table.

**Connector P6 to power (unfiltered)**

| Pin | Function |
|---|---|
| 1 | no connection |
| 2 | Fan- |
| 3 | Capacitor C7- |
| 4 | BR filter |

# Technical data

### Power requirements

The nominal input voltage is -48V or -60V. A range from -36V to -72V is normal. The maximum input current is 20A.

### Output

The output specifications for the NT9X95SA appear in the following table.

**Output specifications**

| | |
|---|---|
| Nominal voltage drop @ 8 A | input + 1.25 V |
| Max voltage drop @ 8 A | input +1.75 V |
| Maximum current limit | 40 A |
| Minimum current limit | 20 A |

# NT9X96AA

## Product description

The NT9X96AA is the link interface shelf (LIS) frame transport bus (F-bus) controller card. The NT9X96AA functions with an NT9X98AA paddle board (LIS fiber interface). The NT9X96AA and the NT9X98AA operate together to allow the LIS to connect to the DMS-bus. The LIS connects to the DMS-bus with a fiber cable.

## Functional description

The NT9X96AA contains the F-bus interface, the link interface to the DMS-bus, and the card maintenance unit (CMU). The NT9X96AA has the following ports:

- an interface between a paddle board and an onboard messaging bus. The interface is common to the three ports.
- an interface between the CMU and the common messaging bus
- an interface between the F-bus and the common messaging bus

A logical message path on a fiber link allows messaging to the NT9X96AA. The fiber link terminates at paddle board NT9X98AA. A 4.096 MHz 8-bit bus provides the interface between the paddle board and the NT9X96AA. A logical message path communicates to the CMU and the application-specific units (ASU) through the F-bus from the DMS-bus.

The F-bus is an 8-bit transaction bus that interfaces between the ASUs and the NT9X96AA. The NT9X96AA controls access to the transaction bus. When an ASU uses the F-bus, the ASU asserts a request line. The NT9X96AA polls the available ASUs to determine which ASU requested the F-bus. When an ASU confirms the poll number, the ASU asserts a poll acknowledge signal. The NT9X96AA grants the F-bus to the ASU that sent the poll acknowledge signal.

The NT9X96AA is an interface between two synchronous buses. The H39 controls the interface to the paddle board. The FSMs control the interface to the F-bus. Two FIFOs or buffers on the link side are present. An application-specific integrated circuit (ASIC) controls the buffers on the link side. The ASIC is the bus access circuit.

The CMU controls the NT9X96AA. The CMU responds to commands from the DMS-bus that allow software control of the configuration of the NT9X96AA board. The CMU handles initialization, configuration, and maintenance.

## NT9X96AA (continued)

### Functional blocks

The NT9X96AA contains the following functional blocks:

- F-bus data path access
- link
- CMU data path access
- CMU
- router
- F-bus poller
- data path arbiter

### Frame transport bus data path access

The F-bus data path access block interfaces to and controls the F-bus. The F-bus communicates with the ASUs.

### Link

The link block interfaces to the messaging bus that the paddle board uses.

### Card maintenance unit data path access

The CMU data path access block contains the interface to the CMU. The CMU controls message transfers to and from the CMU and the F-bus or paddle board messaging bus.

### Card maintenance unit

The CMU block performs initialization and maintenance for the NT9X96AA.

### Router

The router block contains the logic that the address translations require.

### Frame transport bus poller

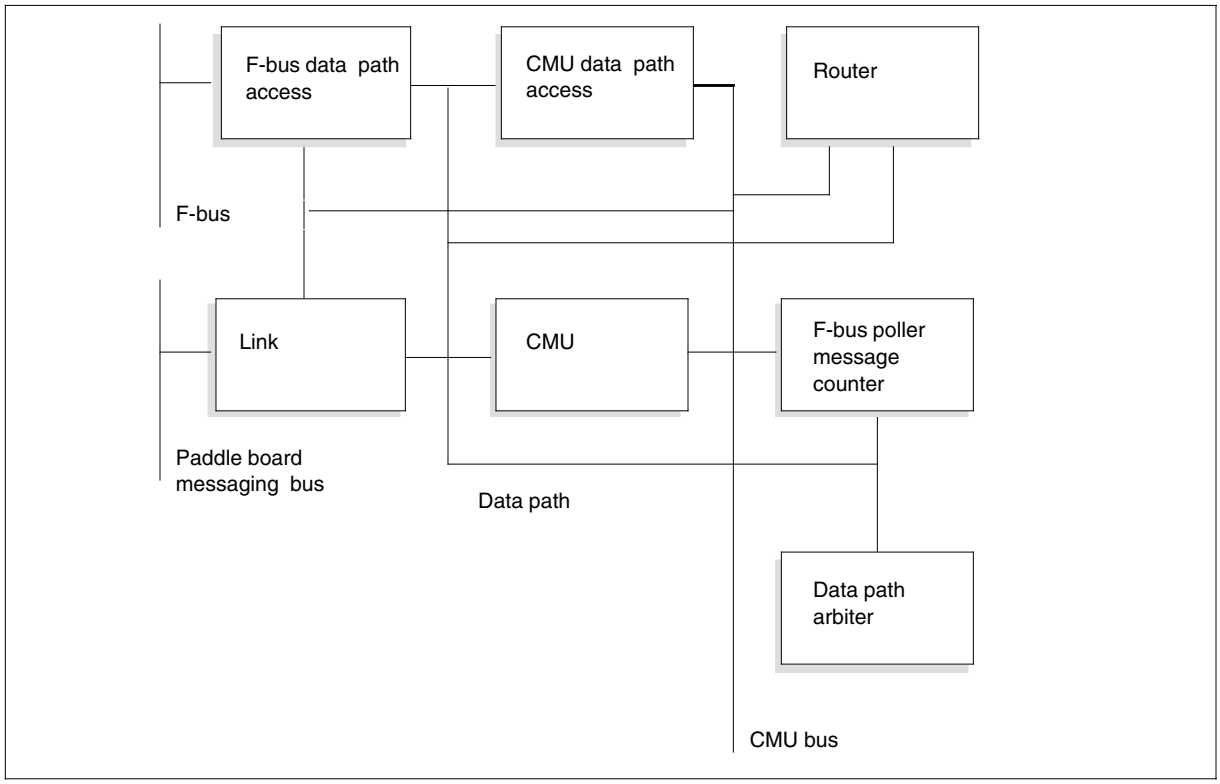
The F-bus block contains the F-bus poller and the message counter logic.

### Data path arbiter

The data path arbiter block controls the data flow in the data path system.

The relationship between the functional blocks appears in the following figure.

**NT9X96AA functional blocks**




# Signaling

## Pin numbers

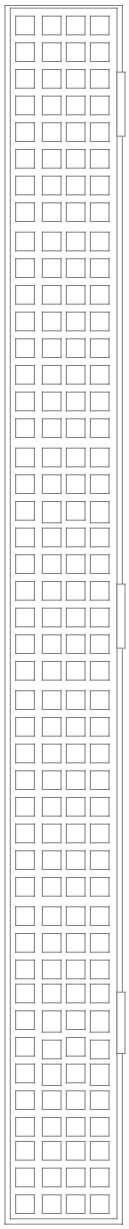
The pin numbers for the NT9X96AA appear in the following figure.

## Timing

The timing for the NT9X96AA appears in the timing figures. The timing figures follow the pin number figure.

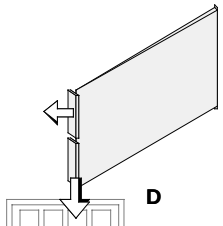
# **NT9X96AA** (continued)

### NT9X96AA pin numbers (Part 1 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | FWAITN | FAD0 | GND |
| 2 | | FCLRN | FAD1 | GND |
| 3 | | FREQN | FAD2 | GND |
| 4 | | FPOLLN | FAD3 | GND |
| 5 | | FRSTN | FAD4 | GND |
| 6 | | FPACKN | FAD5 | GND |
| 7 | GND | GND | FAD6 | GND |
| 8 | | FADRENN | FAD7 | GND |
| 9 | | FDATENN | FPAR | GND |
| 10 | | FEOSN | GND | GND |
| 11 | | FRACKN | | GND |
| 12 | | FRRDYN | | GND |
| 13 | | FSRCENN | | PBDASN |
| 14 | | FDSTENN | | PWRTN |
| 15 | GND | | GND | PDTACKN |
| 16 | GND | GND | | SRESN |
| 17 | | | | PADDR1 |
| 18 | | | | PADDR2 |
| 19 | | | | PADDR3 |
| 20 | GND | | GND | PADDR4 |
| 21 | GND | | | PADDR5 |
| 22 | | | | PADDR6 |
| 23 | | | | PADDR7 |
| 24 | | | | |
| 25 | | | FSPARE | |
| 26 | | | | |
| 27 | GND | | | PBHN |
| 28 | | GND | | RESET |
| 29 | | | | HW4 |
| 30 | | | | GND |
| 31 | | | | FCLK |
| 32 | | GND | | SH0 |
| 33 | | | | SH1 |
| 34 | | | | GND |
| 35 | | | | |
| 36 | | | HW0 | |
| 37 | | | HW1 | |
| 38 | | | HW2 | |
| 39 | | | HW3 | |
| 40 | | | | GND |
| 41 | | | | GND |
| 42 | | | | GND |
| 43 | | | FP61N | GND |
| 44 | | | C61 | +5 |
| 45 | | | | +5 |

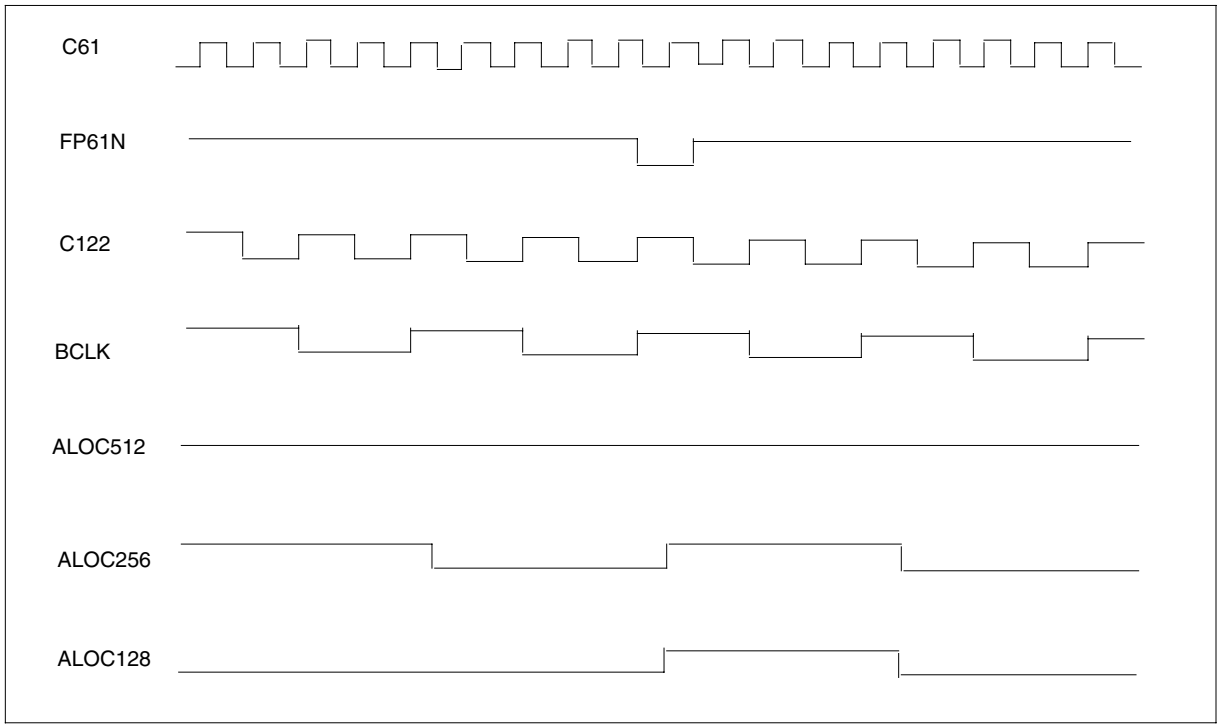
**NT9X96AA pin numbers (Part 2 of 2)**



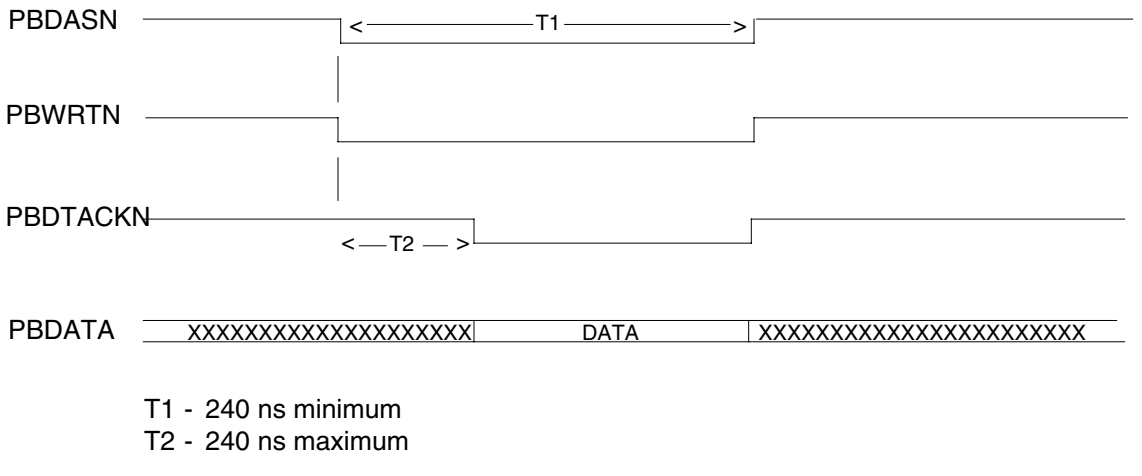
| | D | C | B | A |
|---|---|---|---|---|
| 46 | | | | 5+ |
| 47 | | | GND | 5+ |
| 48 | | | | 5+ |
| 49 | | | | 5+ |
| 50 | | | GND | 5+ |
| 51 | | | | 5+ |
| 52 | | | | 5+ |
| 53 | | | GND | 5+ |
| 54 | | | | 5+ |
| 55 | | | | 5+ |
| 56 | | | GND | |
| 57 | | | | |
| 58 | | | | |
| 59 | | | | |
| 60 | | | | |
| 61 | | | | |
| 62 | | | | |
| 63 | | | | |
| 64 | | | | |
| 65 | | | | |
| 66 | GND | | | |
| 67 | | | | |
| 68 | | | | |
| 69 | | GND | | |
| 70 | | CS20N | | |
| 71 | VCPU | MTDA0 | | |
| 72 | LRVL | MTDA1 | | |
| 73 | GND1 | MTDA2 | | |
| 74 | PRS0 | MTDA3 | | |
| 75 | DAT0 | MTDA4 | | |
| 76 | DAT2 | MTDA5 | | |
| 77 | DAT4 | MTDA6 | | |
| 78 | DAT6 | MTDA7 | | |
| 79 | CS-5N | | TXD1 | GND |
| 80 | ADD2 | TXD0 | RXD0 | GND |
| 81 | ADD0 | MRDA0 | RXD1 | GND |
| 82 | PRS1 | MRDA1 | GND0 | GND |
| 83 | PLOCK, | MRDA2 | PDAT0 | GND |
| 84 | DAT7 | MRDA3 | PDAT1 | GND |
| 85 | ADD1 | MRDA4 | PDAT2 | GND |
| 86 | ADD3 | MRDA5 | PDAT3 | GND |
| 87 | CS+5N | ,MRDA6 | PDAT4 | GND |
| 88 | DAT5 | MRDA7 | PDAT5 | GND |
| 89 | DAT3 | LTVL | PDAT6 | GND |
| 90 | DAT1 | MTDA8 | PDAT7 | GND |

## **NT9X96AA** (continued)

### NT9X96AA clock relationships

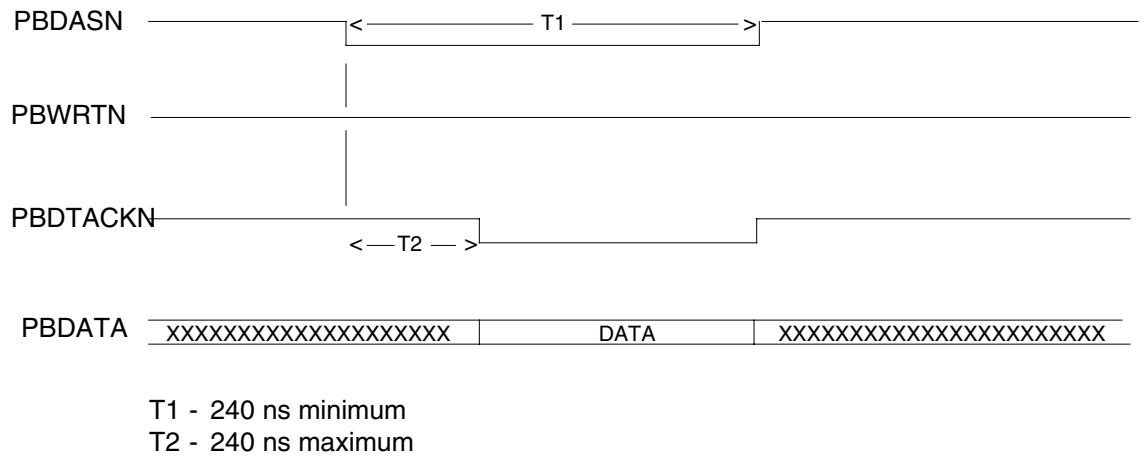


**NT9X96AA CMU paddle board read and write timing**




T1 - 240 ns minimum
T2 - 240 ns maximum

CMU write paddle board cycle

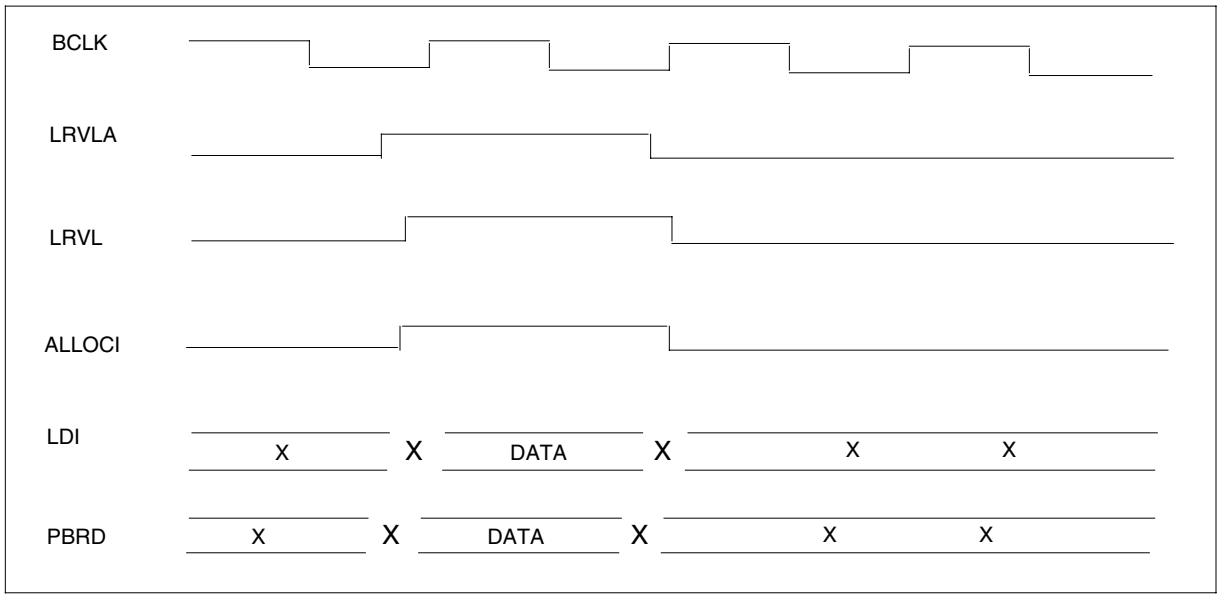



T1 - 240 ns minimum
T2 - 240 ns maximum

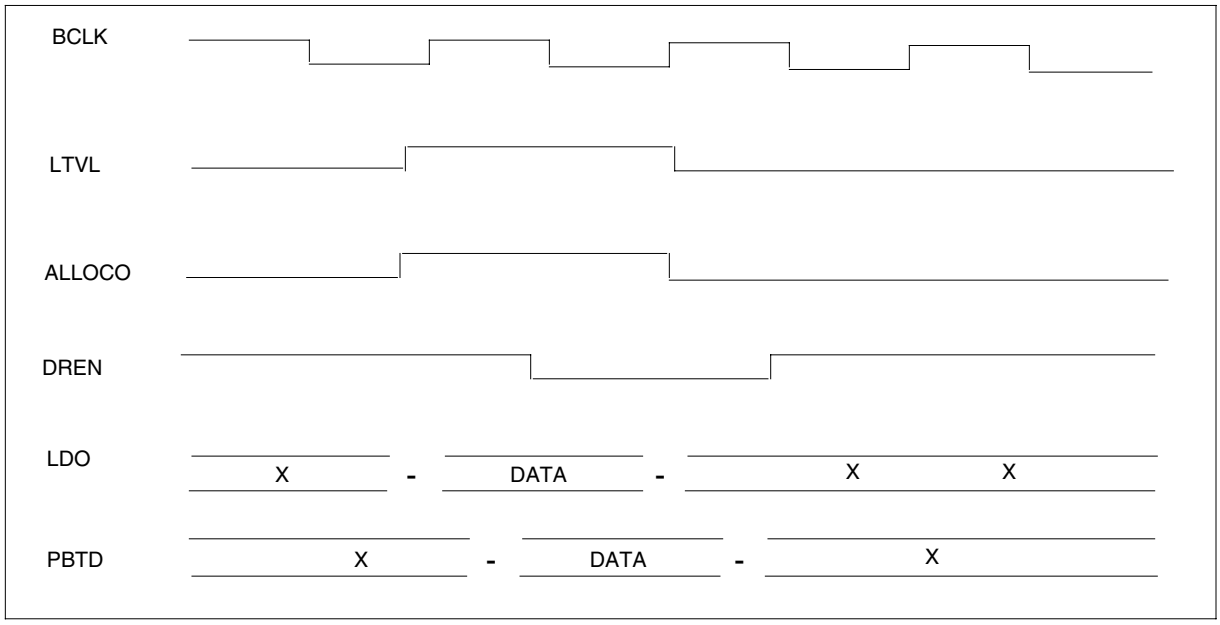
CMU read paddle board cycle

## **NT9X96AA** (continued)

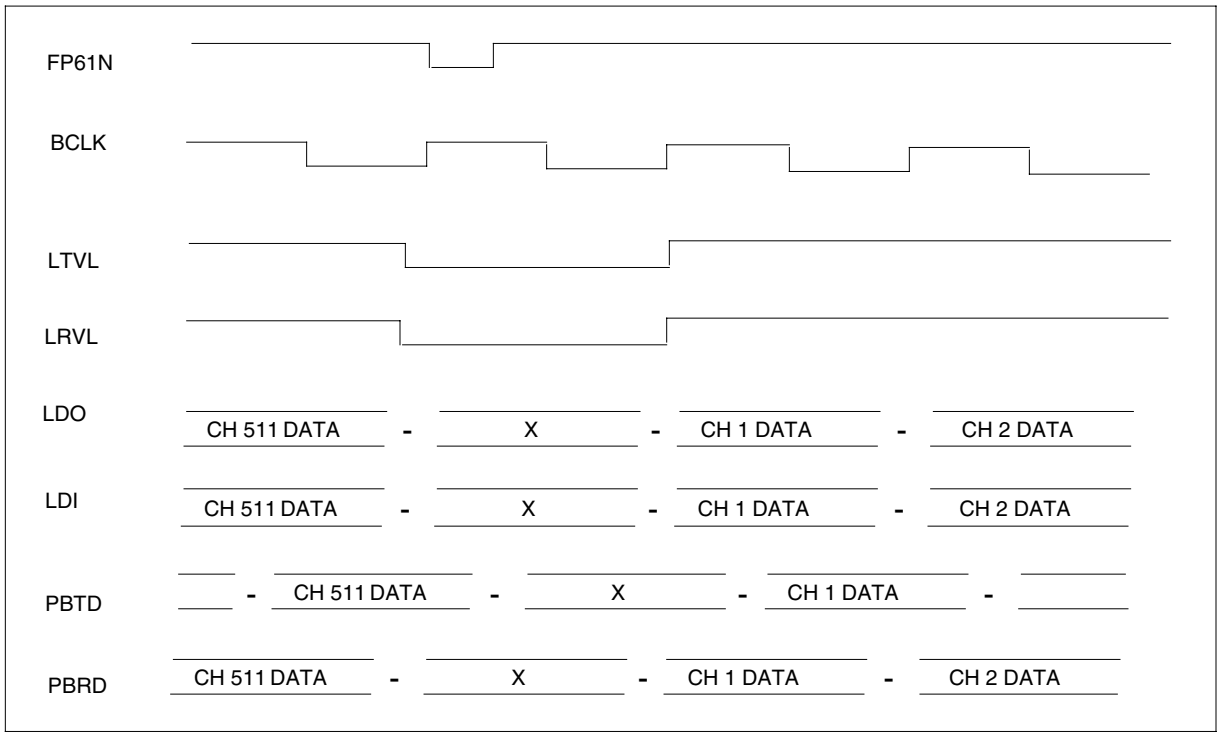
**NT9X96AA paddle board messaging interface timing (PBRD to LH)**




**NT9X96AA paddle board messaging interface timing (PBTD to LH)**



**NT9X96AA link channel relationships**



# NT9X98AA

## Product description

The link interface shelf (LIS) fiber interface paddle board provides a direct link with a fiber cable between the link interface shelf and the DMS-bus.

## Functional description

The NT9X98AA performs the following functions:

- provides a fiber link interface between the DMS bus and the NT9X96AA card (LIS frame transport bus (F-bus) controller)
- provides the subsystem clock from which the paddle board clock and the F-bus clock are derived
- detects out-of-band (OOB) resets
- receives a DS0A composite clock and derives an 8-kHz and a 56-kHz clock from the composite clock

### Functional blocks

The NT9X98AA has the following functional blocks:

- optical interface
- quad fiber link interface chip (QFLIC)
- data transmitter receiver chip (DTRC)
- message bus (M-bus) interface
- OOB reset detection
- phase-locked loop (PLL)
- PLL management unit (PMU)
- power supply monitor (PMON)
- subrate controller (SRC) application-specific integrated circuit (ASIC)
- DS-0 interface
- universal asynchronous receiver transmitter (UART) interface

### Optical interface

The optical interface block performs optical to emitter-coupled logic (ECL) to transistor-transistor logic (TTL) conversion. The optical interface block performs optical to ECL to TTL conversion in the receive direction. The optical interface block also performs TTL to ECL to optical conversion in the transmit direction. The transmit and receive interfaces to the optical interface block are serial TTL.

### Quad fiber link interface chip

The QFLIC block receives serial data from the optical interface block. The QFLIC converts the serial data to 6 bit parallel data. The QFLIC recovers a 4.096-MHz clock and an 8-kHz frame pulse from the received data stream. The QFLIC block receives 6-bit parallel data from the DTRC block. The QFLIC converts the parallel data to serial data. The QFLIC sends the converted data to the optical interface block.

### Data transmitter receiver chip

The DTRC block receives 6-bit words from the QFLIC block. The DTRC demultiplexes the 6-bit words to form 12 bit words. The DTRC block samples 9-bit data from the M-bus interface block.

### Message bus interface

The M-bus interface block provides a bidirectional interface between the link and the NT9X96AA.

### Out-of-band reset detection

The OOB block receives data from the link. The OOB monitors the data and detects the OOB reset sequence. When the OOB block detects the OOB reset sequence, the OOB block asserts a reset pulse on the backplane.

### Phase-locked loop

The PLL block generates the subsystem clocks C61 (16.384 MHz) and FP61 (8 kHz). The PLL synchronizes the subsystem clocks to the recovered clock from the QFLIC block.

### Phase-locked loop management unit

The main part of the PMU block is the microcontroller. The PMU block performs the synchronization routine. The synchronization routine allows the PLL block to lock to the recovered clock from the QFLIC block.

### Power supply monitor

The PMON block detects the following:

- loss of electro/optical (E/O) signal intensity
- loss of the -5V supply
- loss of the +12V supply
- loss of the -12V supply

### Subrate controller

The main part of the SRC block is the subrate controller ASIC, S28. The SRC block allows the subset processor bus (P-bus) to communicate with blocks

## **NT9X98AA** (continued)

PMON, PMU, and PLL. The SRC contains the registers and counters that the PMU block requires to perform the synchronization routine.

### DS-0 interface

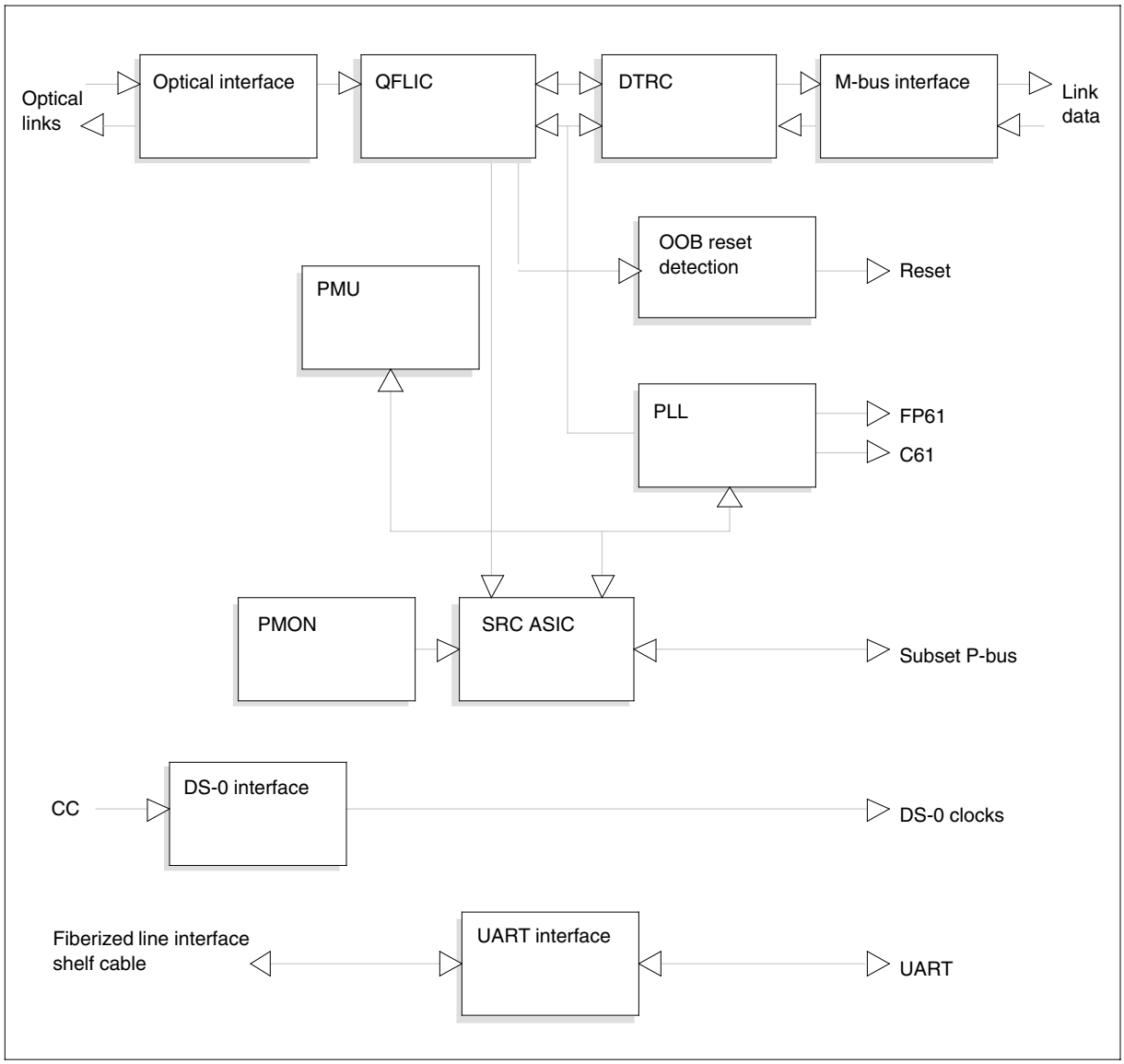
The DS-0 interface block accepts the office DS-0A composite clock. The DS-0 generates and buffers the DS-0 derivative clocks.

### Universal synchronous receiver transmitter interface

The UART interface block allows external communication with the NT9X96AA.

The relationship between the functional blocks appears in the following figure.

**NT9X98AA functional blocks**



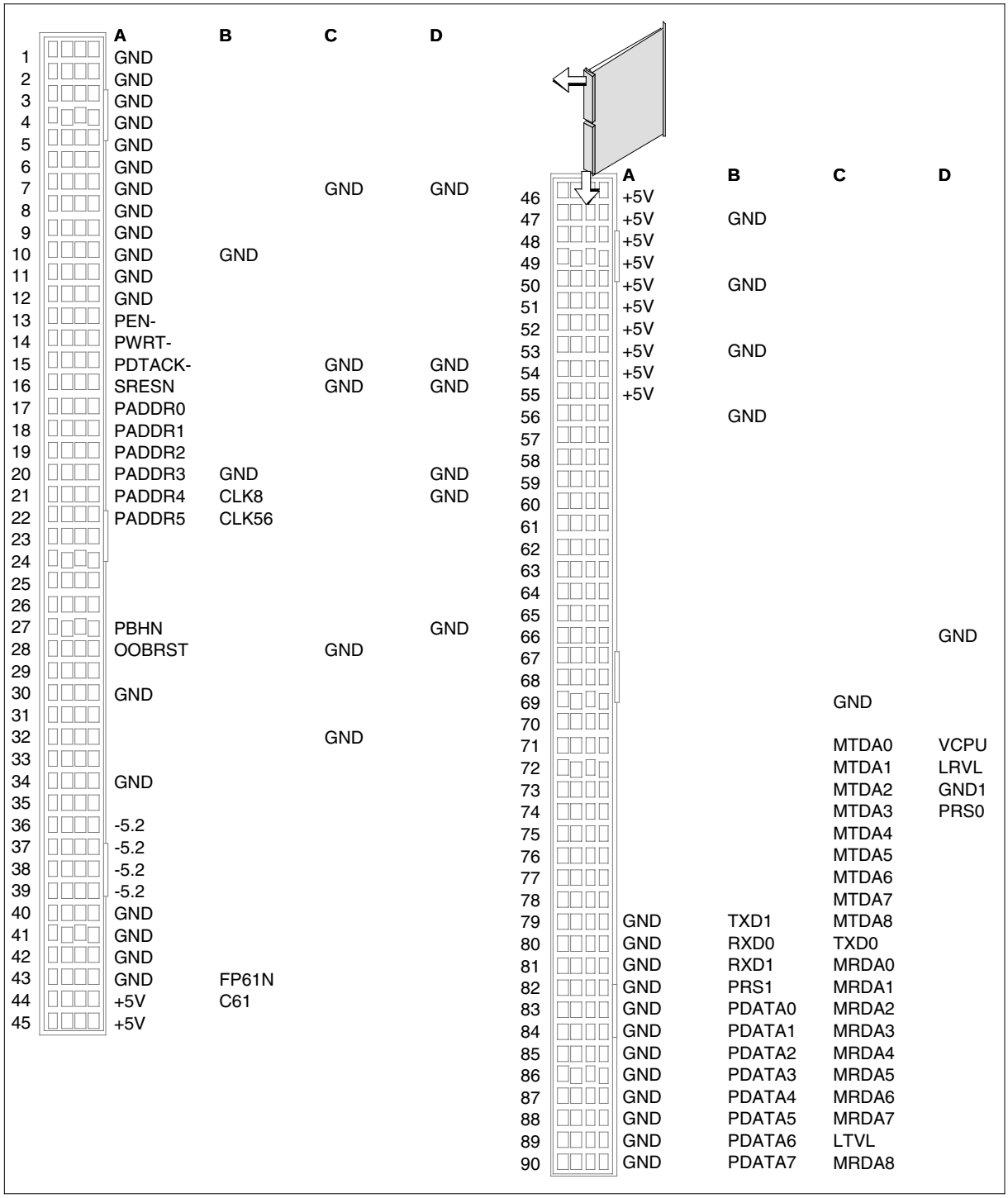

# Signaling

## Pin numbers

The pin numbers for NT9X98AA appear in the following table.

# **NT9X98AA** (continued)

### NT9X98AA pin numbers



| | A | B | C | D |
|---|---|---|---|---|
| 1 | GND | | | |
| 2 | GND | | | |
| 3 | GND | | | |
| 4 | GND | | | |
| 5 | GND | | | |
| 6 | GND | | | |
| 7 | GND | | GND | GND |
| 8 | GND | | | |
| 9 | GND | | | |
| 10 | GND | GND | | |
| 11 | GND | | | |
| 12 | GND | | | |
| 13 | PEN- | | | |
| 14 | PWRT- | | | |
| 15 | PDTACK- | | GND | GND |
| 16 | SRESN | | GND | GND |
| 17 | PADDR0 | | | |
| 18 | PADDR1 | | | |
| 19 | PADDR2 | | | |
| 20 | PADDR3 | GND | | GND |
| 21 | PADDR4 | CLK8 | | GND |
| 22 | PADDR5 | CLK56 | | |
| 23 | | | | |
| 24 | | | | |
| 25 | | | | |
| 26 | | | | |
| 27 | PBHN | | | GND |
| 28 | OOBRST | | GND | |
| 29 | | | | |
| 30 | GND | | | |
| 31 | | | | |
| 32 | | | GND | |
| 33 | | | | |
| 34 | GND | | | |
| 35 | | | | |
| 36 | -5.2 | | | |
| 37 | -5.2 | | | |
| 38 | -5.2 | | | |
| 39 | -5.2 | | | |
| 40 | GND | | | |
| 41 | GND | | | |
| 42 | GND | | | |
| 43 | GND | FP61N | | |
| 44 | +5V | C61 | | |
| 45 | +5V | | | |

| | A | B | C | D |
|---|---|---|---|---|
| 46 | +5V | | | |
| 47 | +5V | GND | | |
| 48 | +5V | | | |
| 49 | +5V | | | |
| 50 | +5V | GND | | |
| 51 | +5V | | | |
| 52 | +5V | | | |
| 53 | +5V | GND | | |
| 54 | +5V | | | |
| 55 | +5V | | | |
| 56 | | GND | | |
| 57 | | | | |
| 58 | | | | |
| 59 | | | | |
| 60 | | | | |
| 61 | | | | |
| 62 | | | | |
| 63 | | | | |
| 64 | | | | |
| 65 | | | | |
| 66 | | | | GND |
| 67 | | | | |
| 68 | | | | |
| 69 | | | GND | |
| 70 | | | | |
| 71 | | | MTDA0 | VCPU |
| 72 | | | MTDA1 | LRVL |
| 73 | | | MTDA2 | GND1 |
| 74 | | | MTDA3 | PRS0 |
| 75 | | | MTDA4 | |
| 76 | | | MTDA5 | |
| 77 | | | MTDA6 | |
| 78 | | | MTDA7 | |
| 79 | GND | TXD1 | MTDA8 | |
| 80 | GND | RXD0 | TXD0 | |
| 81 | GND | RXD1 | MRDA0 | |
| 82 | GND | PRS1 | MRDA1 | |
| 83 | GND | PDATA0 | MRDA2 | |
| 84 | GND | PDATA1 | MRDA3 | |
| 85 | GND | PDATA2 | MRDA4 | |
| 86 | GND | PDATA3 | MRDA5 | |
| 87 | GND | PDATA4 | MRDA6 | |
| 88 | GND | PDATA5 | MRDA7 | |
| 89 | GND | PDATA6 | LTVL | |
| 90 | GND | PDATA7 | MRDA8 | |

The signals for connector J1 appear in the following table.

**NT9X98AA J1 signals**

| Pin | Name |
|---|---|
| 1 | VCPU |
| 2 | GND1 |
| 3 | TXD1 |
| 4 | RXD1 |
| 5 | PRS1 |
| 6 | TXD0 |
| 7 | PRS0 |
| 8 | RXD0 |
| 9 | GND0 |

**NT9X98AA J2 signals**

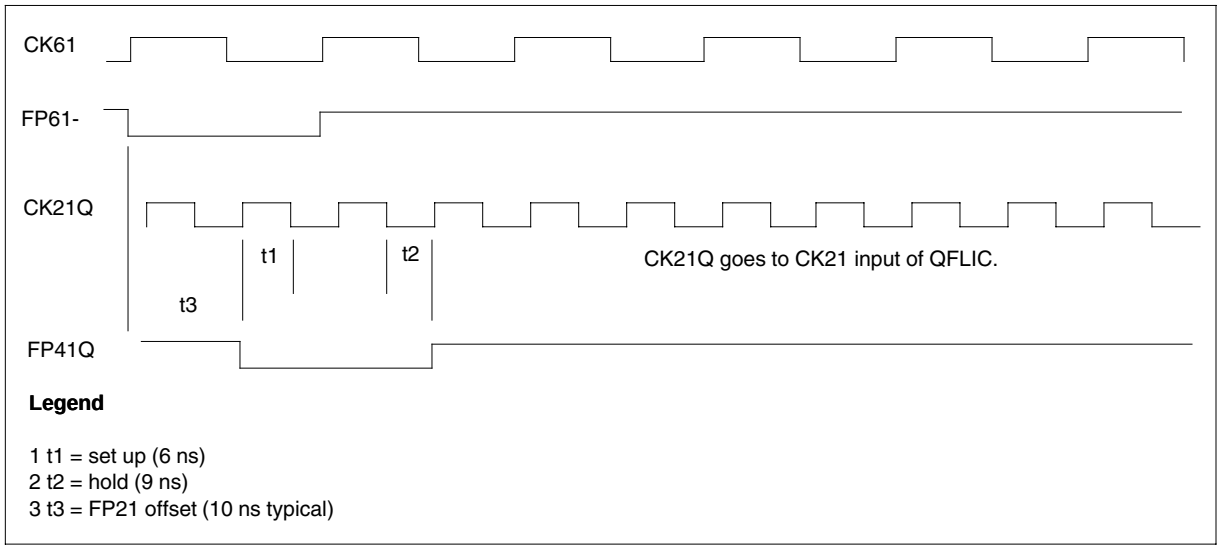
| Pin | Name |
|---|---|
| 1 | Shield |
| 2 | CCLKT |
| 3 | |
| 4 | |
| 5 | FFP |
| 6 | CCLKR |
| 7 | Shield |
| 8 | |
| 9 | PLLFP |

## Timing

The timing diagrams for the NT9X98AA appear in the following figures and tables.

# **NT9X98AA** (continued)

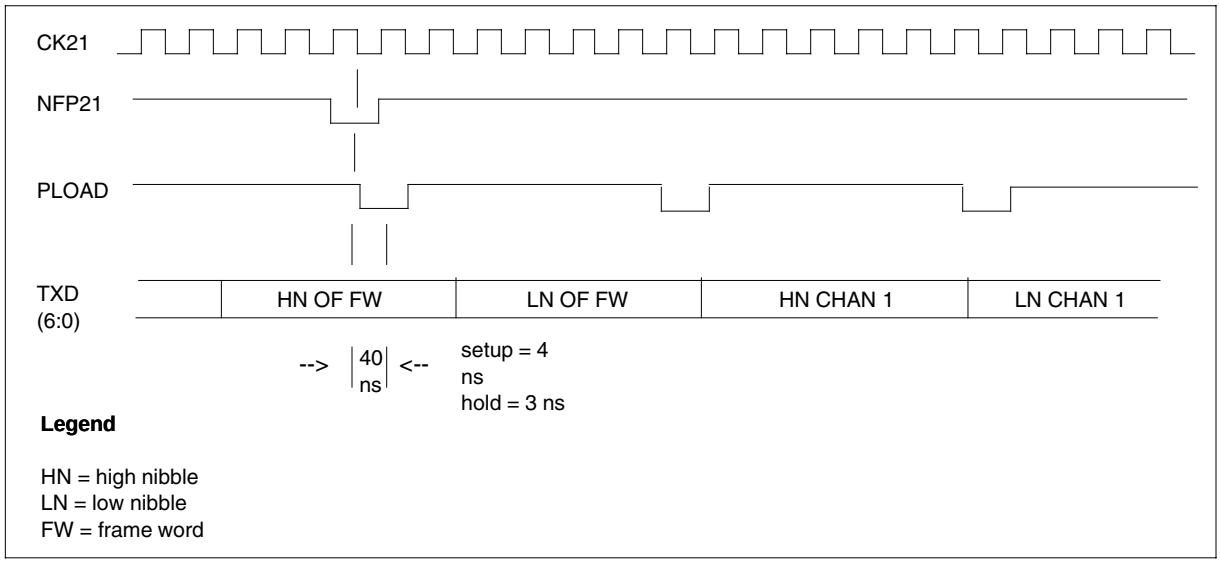
### NT9X98AA CK21 and FP41 synchronization timing




**Legend**

1 t1 = set up (6 ns)
2 t2 = hold (9 ns)
3 t3 = FP21 offset (10 ns typical)

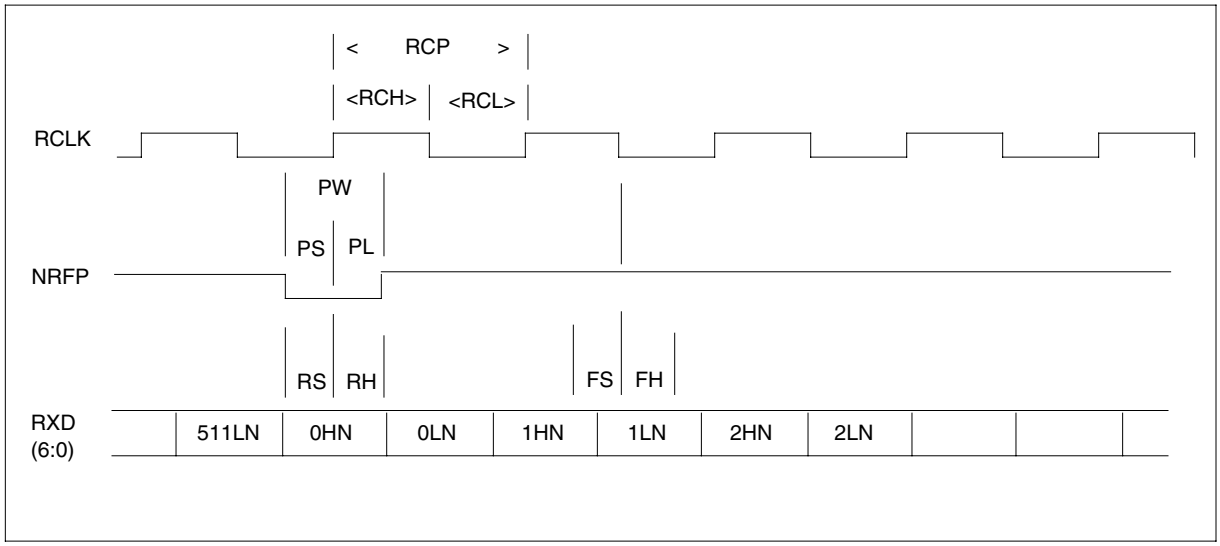
### NT9X98AA R94 transmitter timing




**Legend**

HN = high nibble
LN = low nibble
FW = frame word

### NT9X98AA RXD timing

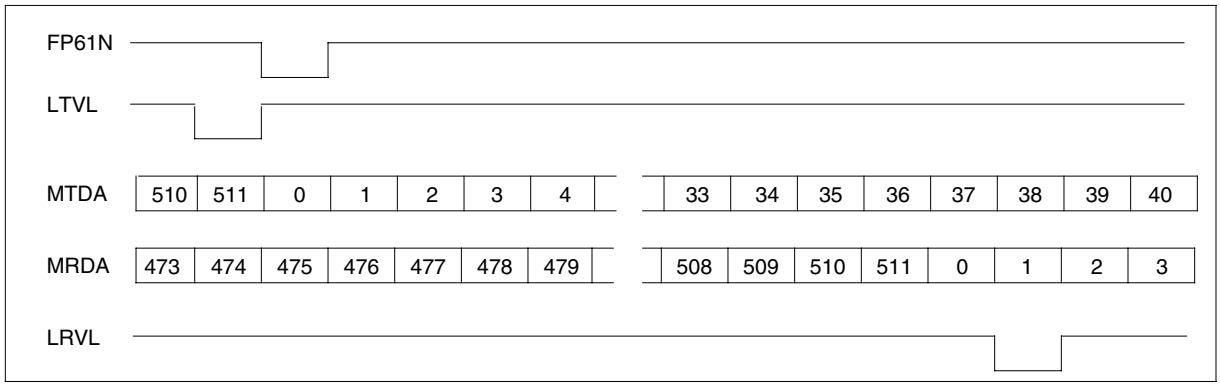



### RXD timing

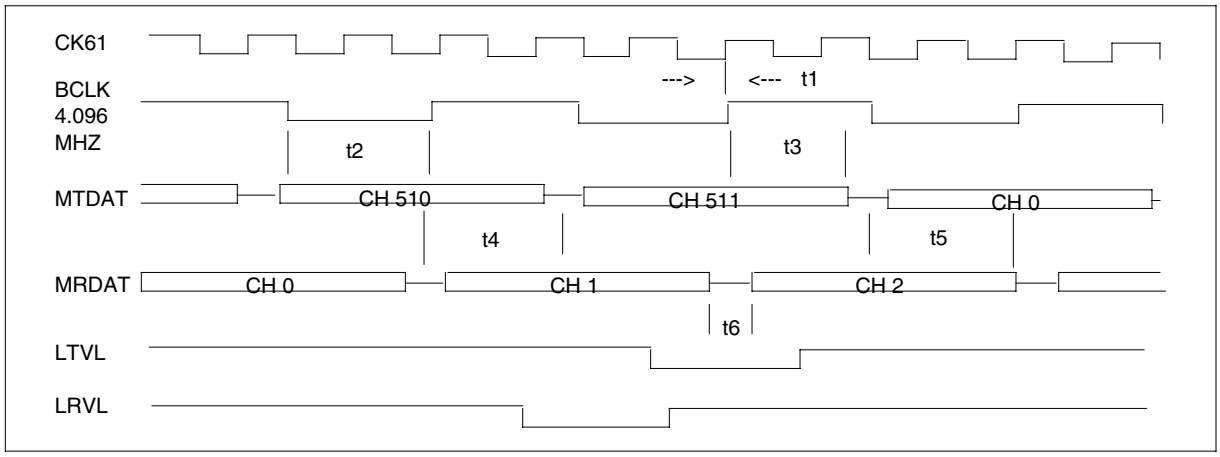
| Symbol | Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|---|
| RCP | RCLK period | | 244 ns | |
| RCH | RCLK high | 100 ns | 122 ns | |
| RCL | RCLK low | 100 ns | 122 ns | |
| PS | FP setup | 10 ns | | 120 ns |
| PH | FP hold | 10 ns | | 150 ns |
| RS | High nibble setup | 10 ns | | |
| RH | High nibble hold | 10 ns | | |
| FS | Low nibble setup | 10 ns | | |
| FH | Low nibble hold | 10 ns | | |

## **NT9X98AA** (continued)

### NT9X98AA M-bus backplane timing



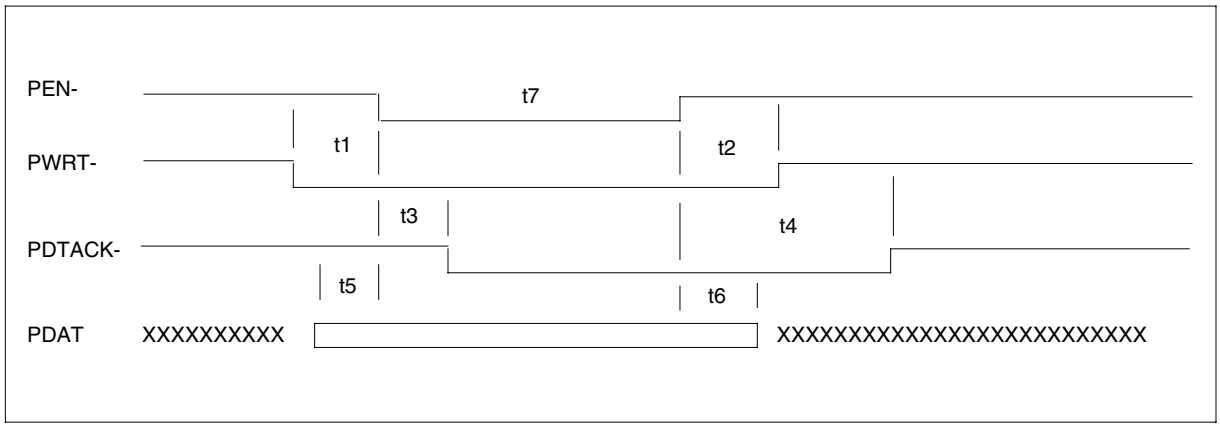

### NT9X98AA M-bus timing specification at backplane




### P-bus interface timing (write cycle)

| Symbol | Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|---|
| t1 | Difference between C61 and BCLK | 0 ns | | ±30 ns |
| t2 | Required setup | | | |
| t3 | Required hold | | | |
| t4 | Setup | | | |
| t5 | Hold | | | |
| t6 | Guard time | | | |

**NT9X98AA P-bus interface timing (write cycle)**

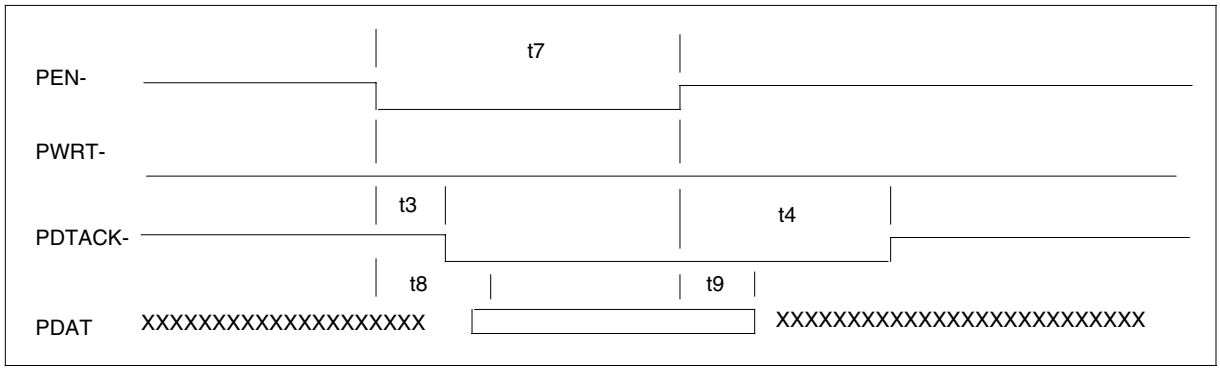



**P-bus interface timing (write cycle)**

| Symbol | Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|---|
| t1 | PWRT- valid to PEN- | 0 ns | | |
| t2 | PEN- released to PWRT- released | 0 ns | | |
| t3 | PEN- valid to PDTACK- asserted | 180 ns | | 240 ns |
| t4 | PEN- released to PDTACK- released | | | 40 ns |
| t5 | DATA valid to PEN- | -60 ns | | |
| t6 | PEN- released to DATA valid | 0 ns | | |
| t7 | PEN- pulse width | 240 ns | | |

## **NT9X98AA** (continued)

**NT9X98AA P-bus interface timing (read cycle)**




**P-bus interface timing (read cycle)**

| Symbol | Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|---|
| t3 | PEN- valid to PDTACK- asserted | 180 ns | | 240 ns |
| t4 | PEN- released to PDTACK- released | | | 40 ns |
| t7 | PEN- pulse width | 240 ns | | |
| t8 | PEN- asserted to PDAT valid | 120 ns | | 180 ns |
| t9 | PEN- released to PDAT released | | | 10 ns |

# Technical data

### Power requirements

The power requirements for the NT9X98AA appear in the following table.

**Power requirements (Sheet 1 of 2)**

| Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|
| Supply voltage | 4.75V | 5.0V | 5.25V |

**Power requirements (Sheet 2 of 2)**

| Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|
| Supply ripple | | | 1.0V |
| Supply current | | | 1.85A |

# 2 NTAXnnaa

## NTAX78AA through NTAX87AA

# NTAX78AA

## Product description

The NTAX78AA digital cellular time switch (DCTS) circuit card is for the digital integrated cellular peripheral (DICP). The DICP is an XPM base peripheral for digital cellular applications. The ISDN digital trunk controller (DTCI) shelf can use this card without software modification. The NTAX78AA is backward compatible with the NT6X44AB. The DTCI can use this card for ISDN applications where a switch of wideband channels is necessary.

## Functional description

The main functions of the NTAX78AA are:

- time switching of DS0 samples between three ports
- parallel-to-serial and serial-to-parallel formatting of DS0 samples
- provides logic for transmission and reception of DS1 signaling information to and from the signaling processor (SP)
- provides looparound ability for diagnostic purposes

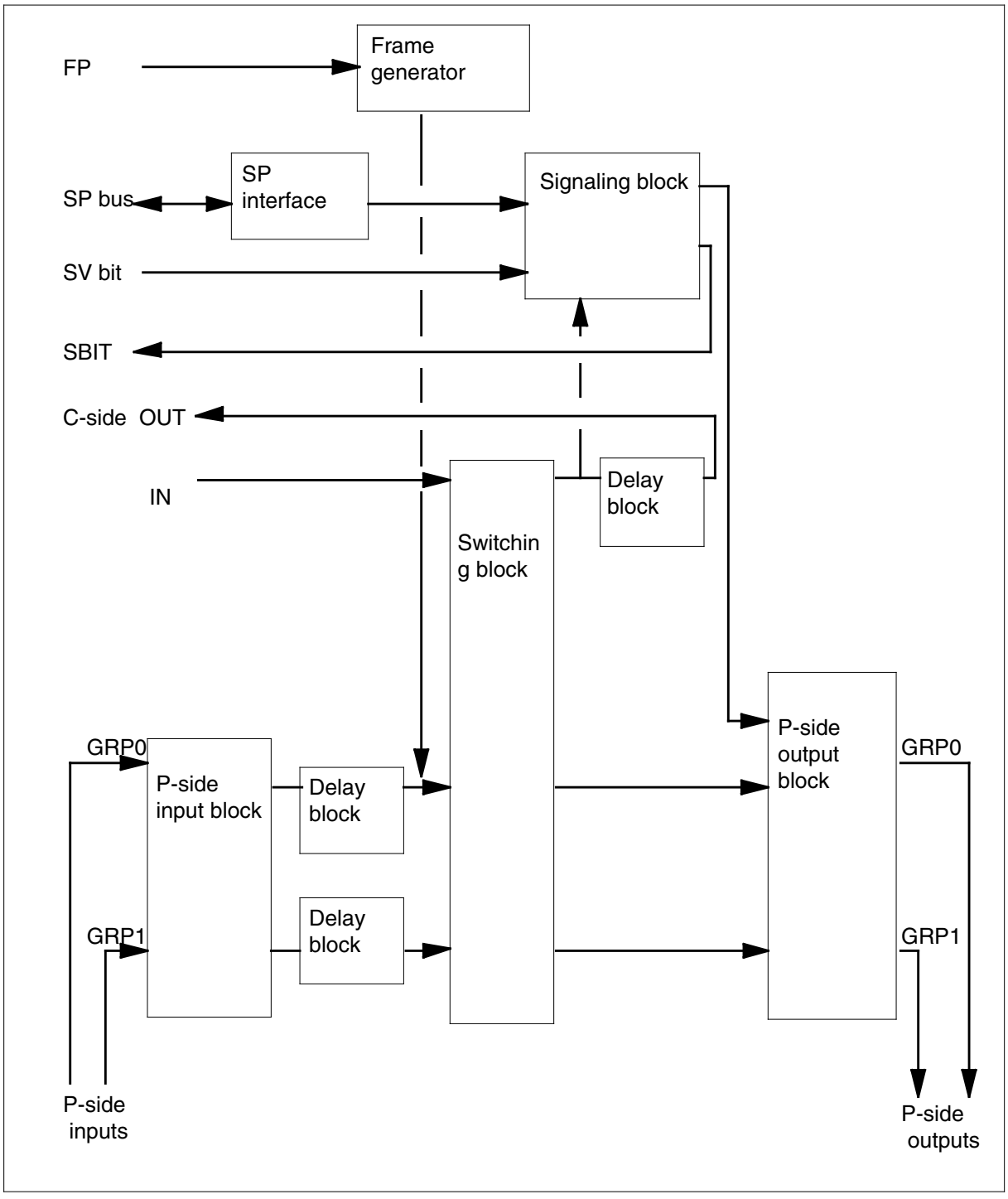
### Functional blocks

The NTAX78AA has the following functional blocks:

- microprocessor interface
- switching block
- signaling block
- processor (P-side) input block
- P-side output block
- three delay blocks
- frame generation block

The relationship between these functional blocks appears in the following figure.

**NTAX78AA functional blocks**



## NTAX78AA (continued)

### Microprocessor interface

The microprocessor interface provides access to the card from the signaling processor address bus (A-bus) on the backplane of the peripheral. The A-bus is a data bus and a conduit for control signals.

### Switching block

The switching block performs the time switch function for three input groups and three output groups. Each group is a frame of 640 channels. The inputs to the switching blocks from the central-side (C-side) and P-side ports must be channel-assigned.

### Signaling block

The signaling block provides signaling access to the P-side group 0 input/output from the signaling processor. The signaling block provides loop-backs in the signaling path for diagnostic purposes.

### Peripheral-side input block

The P-side input block converts incoming P-side data from bit-interleaved serial DS60 format to parallel format for input. Conversion occurs for input to the P-side delay memory.

### Peripheral-side output block

The P-side output block converts parallel output from the switching block to bit-interleaved DS60 serial output.

### Delay blocks

The NTAX78AA performs switching with a constant frame delay. This feature requires alignment in time between the P-side and C-side interfaces. Delay blocks that use memories configured as circular buffers accomplish alignment

### Frame generation block

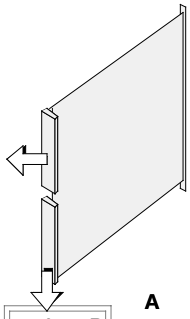
The function of this block is to generate a 40 ms time-division multiple access (TDMA) frame pulse. The frame pulse is for use on the digital signal processor (DSP) shelf for system synchronization.

## Signaling

### Pin numbers

The pin numbers for the NTAX78AA appear in the following figure.

### NTAX78AA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | +5V | +5V |
| 4A 4B | +5V | +5V |
| 5A 5B | GND | GND |
| 6A 6B | FP- | C97+ |
| 7A 7B | GND | GND |
| 8A 8B | ACT- | |
| 9A 9B | ETS- | ETS-M |
| 10A 10B | FP48- | SBIT |
| 11A 11B | GND | GND |
| 12A 12B | DAS- | TWR |
| 13A 13B | LDS- | TST1 |
| 14A 14B | DTACK- | TST0- |
| 15A 15B | UDS- | ABOUT |
| 16A 16B | WRT- | ABIN |
| 17A 17B | | 3MSIRQ- |
| 18A 18B | SASTOUTN | GND |
| 19A 19B | | |
| 20A 20B | | MB |
| 21A 21B | PIN0 | POUT0 |
| 22A 22B | PIN1 | POUT1 |
| 23A 23B | PIN2 | POUT2 |
| 24A 24B | PIN3 | POUT3 |
| 25A 25B | PIN4 | POUT4 |
| 26A 26B | PIN5 | POUT5 |
| 27A 27B | PIN6 | POUT6 |
| 28A 28B | PIN7 | POUT7 |
| 29A 29B | ADDR01 | T1OUT0 |
| 30A 30B | ADDR02 | T1OUT2 |
| 31A 31B | ADDR03 | T1OUT4 |
| 32A 32B | ADDR04 | T1OUT6 |
| 33A 33B | ADDR05 | T1OUT8 |
| 34A 34B | GND | GND |
| 35A 35B | ADDR06 | T1OUT10 |
| 36A 36B | ADDR07 | T1OUT12 |
| 37A 37B | ADDR08 | T1OUT14 |
| 38A 38B | ADDR09 | T1OUT16 |
| 39A 39B | ADDR10 | SV |
| 40A 40B | ADDR11 | T1OUT18 |

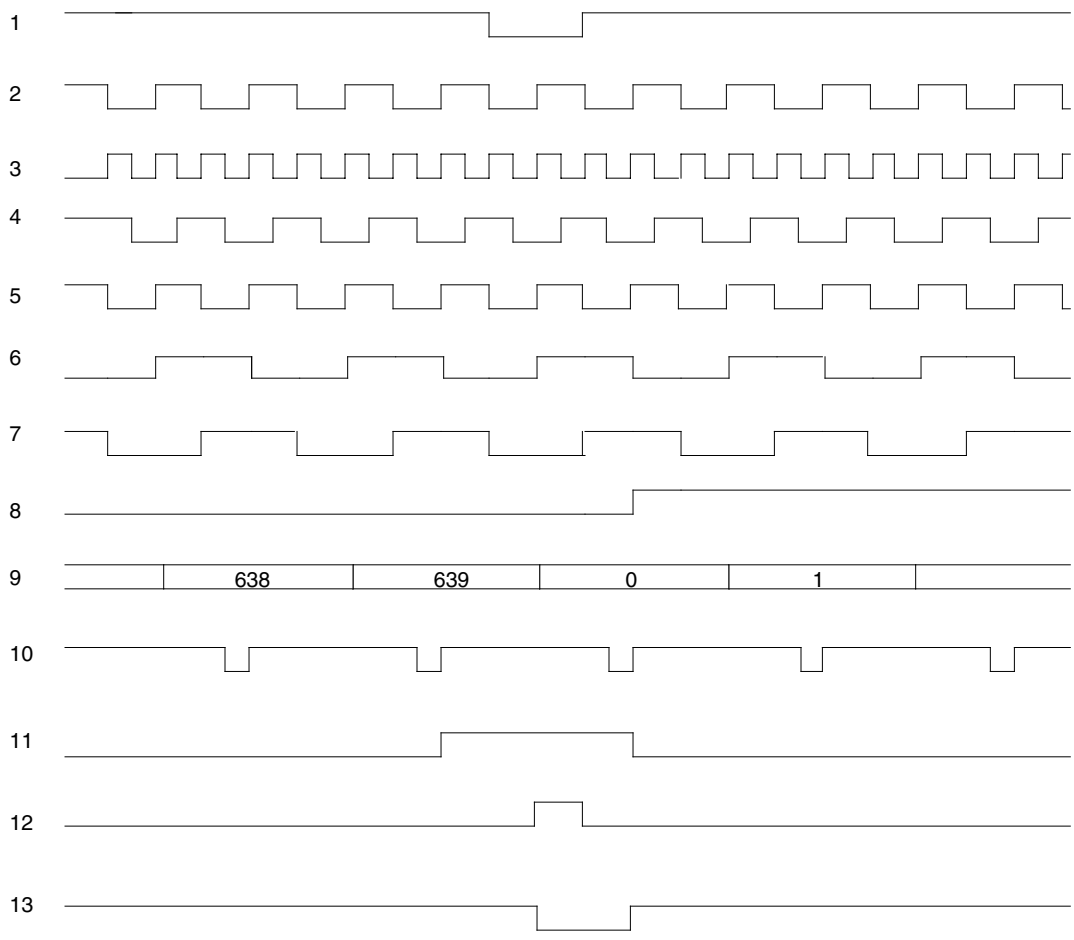
| | A | B |
|---|---|---|
| 41A 41B | GND | DSOUT0 |
| 42A 42B | ADDR12 | DSOUT2 |
| 43A 43B | ADDR13 | DSOUT4 |
| 44A 44B | ADDR14 | DSOUT6 |
| 45A 45B | ADDR15 | DSOUT8 |
| 46A 46B | ADDR16 | DSOUT10 |
| 47A 47B | ADDR17 | DSOUT12 |
| 48A 48B | ADDR18 | DSOUT14 |
| 49A 49B | ADDR19 | DSOUT16 |
| 50A 50B | ADDR20 | DSOUT18 |
| 51A 51B | ADDR21 | GND |
| 52A 52B | | T1IN0 |
| 53A 53B | | T1IN2 |
| 54A 54B | | T1IN4 |
| 55A 55B | PSPEN- | T1IN6 |
| 56A 56B | | T1IN8 |
| 57A 57B | GND | T1IN10 |
| 58A 58B | DATA00 | T1IN12 |
| 59A 59B | DATA01 | T1IN14 |
| 60A 60B | DATA02 | T1IN16 |
| 61A 61B | DATA03 | T1IN18 |
| 62A 62B | DATA04 | GND |
| 63A 63B | DATA05 | DSIN0,DSIN1 |
| 64A 64B | GND | DSIN2,DSIN3 |
| 65A 65B | DATA06 | DSIN4,DSIN5 |
| 66A 66B | DATA07 | DSIN6,DSIN7 |
| 67A 67B | DATA08 | DSIN8,DSIN9 |
| 68A 68B | DATA09 | DSIN10,DSIN11 |
| 69A 69B | DATA10 | DSIN12,DSIN13 |
| 70A 70B | DATA11 | DSIN14,DSIN15 |
| 71A 71B | DATA12 | DSIN16,DSIN17 |
| 72A 72B | DATA13 | DSIN18 |
| 73A 73B | DATA14 | GND |
| 74A 74B | DATA15 | RECFP0 |
| 75A 75B | TDMASYNC | RECFP1 |
| 76A 76B | GND | GND |
| 77A 77B | | |
| 78A 78B | GND | GND |
| 79A 79B | | |
| 80A 80B | GND | GND |

## **NTAX78AA** (continued)

### Timing

The timing for the NTAX78AA appears in the following figure.

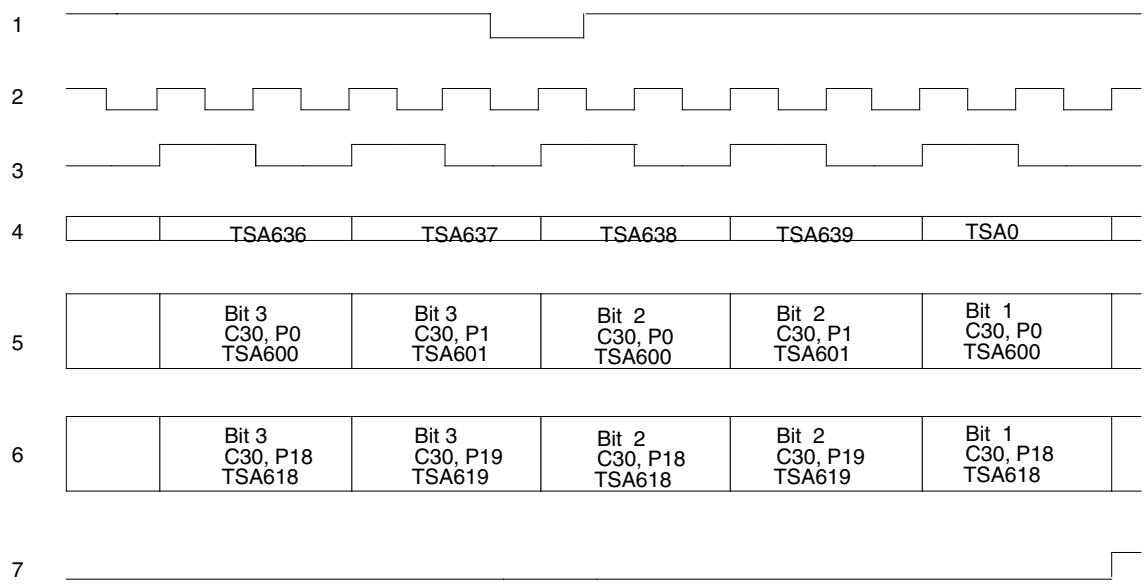
**NTAX78AA Clock signals and channel counter timing**




**Legend**

1 FP input
2. C97 input
3. CK48 output
4. CK97FB
5. CK97
6. CK195
7. A11
8. FC
9. Count (9:0)
10. CDMWE-
11. PROCYC
12. CMWE+/CMRD+ (PAD (14:12)= 000)
13. STATCK (PAD (14:10) = 00111)

**NTAX78AA Timing for block POUTPUT**

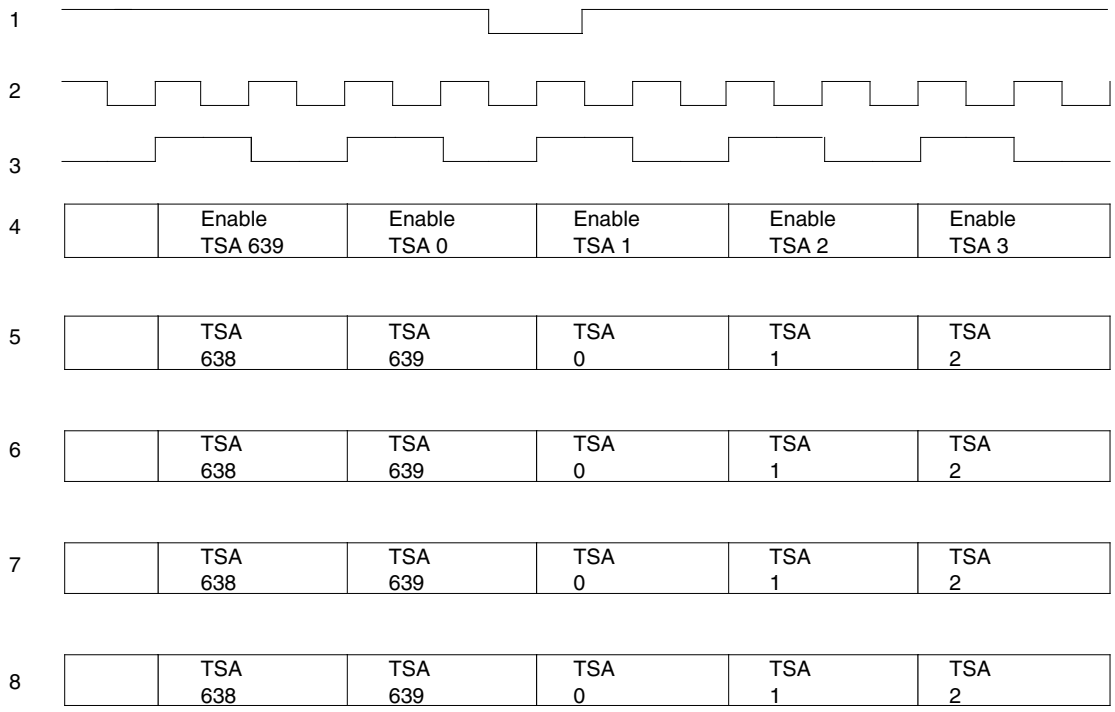



**Legend**

1. FP input
2. C97 input
3. CK195
4. Formatter input (7:0)
5. T1OUT00 or DSOUT00 . . .
6. T1OUT18 or DSOUT18
7. SYNCHO

## **NTAX78AA** (continued)

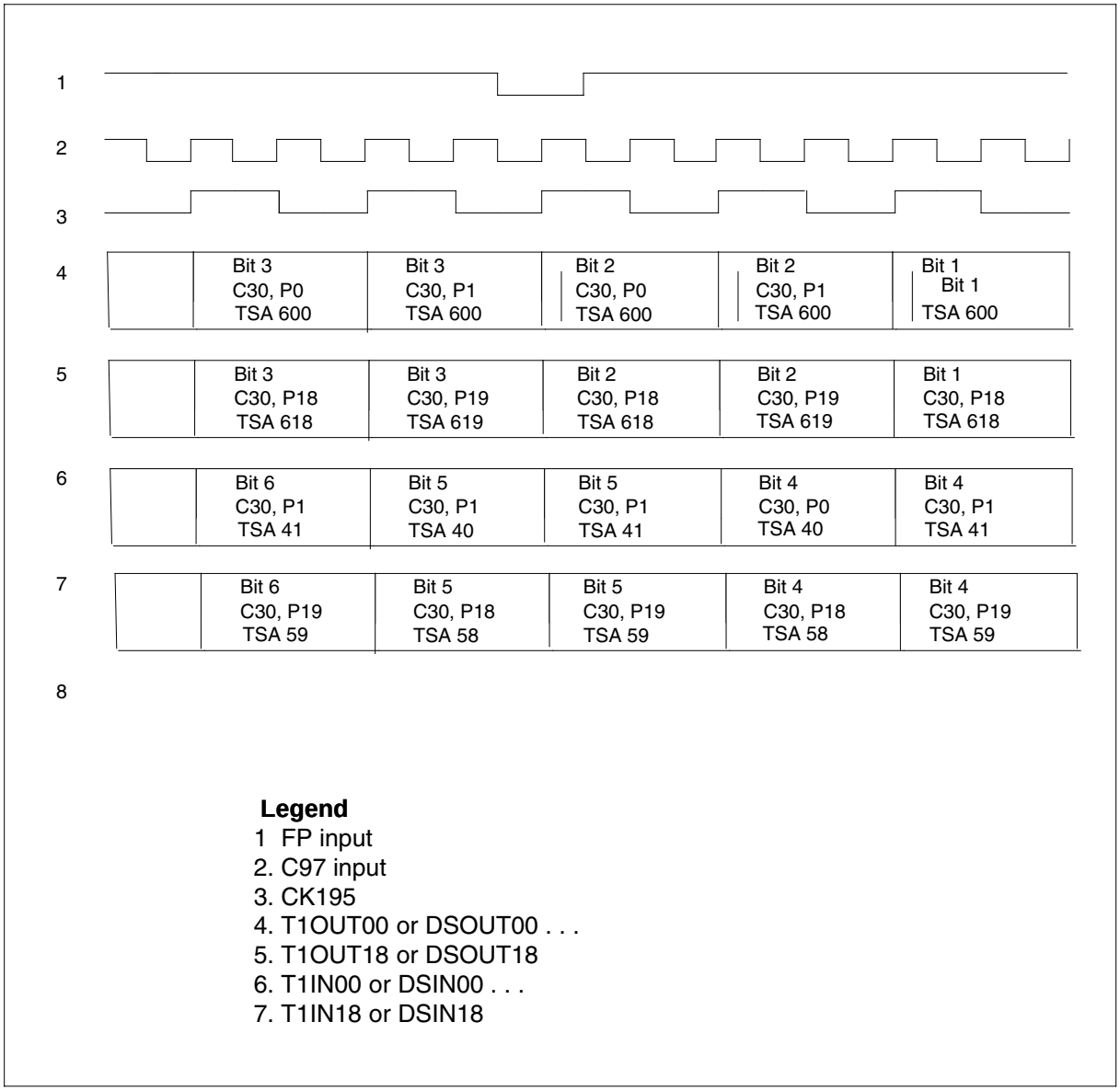
### NTAX78AA Speech bus data timing




**Legend**

1 FP input
2. C97 input
3. CK195
4. T1OUT00 or DSOUT00 . . .
5. T1OUT18 or DSOUT18
6. T1IN00 or DSIN00 . . .
7. T1IN18 or DSIN18

**NTAX78AA P-side DS60 timing**




**Legend**

1 FP input
2. C97 input
3. CK195
4. T1OUT00 or DSOUT00 . . .
5. T1OUT18 or DSOUT18
6. T1IN00 or DSIN00 . . .
7. T1IN18 or DSIN18

# NTAX78BA

## Product description

The NTAX78BA enhanced time switch circuit card is backwards compatible with NT6X44 and NTAX78 time switches. This card obsoletes the signaling bit handler (H77) and time switch (H78) ASICs. There are five modes of operation for the NTAX78BA:

- NT6X44AA—has 20 P-side ports of 32 channels (640 total timeslots) which are selected as DS1 or DS30A interfaces on a per-port basis. It also has 20 C-side ports from the parallel speech bus on the XPM backplane. The time switch is separated into an incoming and outgoing time switch. Therefore, only C-to-P-side or P-to-C-side connections are possible. Signaling bits are extracted from the incoming P-side PCM on the C-side of the time switch. It does not support PCM conversions. Switching delay through the time switch depends on the connection (there is no constant delay).
- NT6X44CA—this version is used for remotes. Incoming signaling is extracted on the P-side of incoming P-side PCM before it is time switched. The inversion of signaling bits is selected on this card.
- NT6X44EA—this is the international version of the time switch. The NT6X44EA supports PCM conversions, including U-law to A-law and bit inversion, on a per-timeslot basis which is configured in the connection memory.
- NTAX78AB—this card supports 40 P-side ports, 20 for DS1 interface and 20 for DS30A interface. There are two banks of data memory, allowing a constant switching delay through the time switch. It does not partition the time switch into an incoming and an outgoing direction, allowing P-to-P-side and C-to-C-side connections. It is backwards compatible with NT6X44AA only if there is a DS1 P-side interface—it does not support the DS30A interface in the NT6X44AA mode. There is a mode switch which is backwards compatible with NT6X44CA with only the DS1 P-side interface. There is no support for P-side selection of DS1 versus DS30A on a per-port basis. The NTAX78AB mode uses all 40 ports, so no selection is necessary. The 6X44 mode uses only 20 ports from the DS1 interface.
- NTAX78BA—the subject of this hardware description.

One selects the mode of operation of the NTAX78BA by software, or one configures the mode of operation on power-up by populating a resistor on the motherboard.

The NTAX78BA interfaces to 640 incoming and 640 outgoing C-side speech bus channels. It interfaces to 1280 incoming and 1280 outgoing P-side channels arranged on serial DS60 links. Each group of 1280 channels consists

of 640 channels to or from DS1 interface and 640 channels to or from DS30A interface.

It provides time switching and PCM conversions on a per-channel basis.

The AX78 modes of operation allow any of the 1920 input channels to be connected to any of the 1920 output channels.

It provides selection of DS1 versus DS30A P-side interface on a per-port basis for the 20 available P-side ports in 6X44 mode, and it extends this selection over all 40 available P-side ports in AX78BA mode.

ABCD signaling bits are extracted from the incoming P-side PCM on the P-side of the time switch (6X44CA mode) or on the C-side of the time switch (all other modes). Insertion of outgoing ABCD signaling bits is controlled on a per-channel basis.

Following is a summary of the modes of operation listed above:

- NT6X44AA—the default mode on power-up; the original version of the XPM time switch.
- NT6X44CA—selectable by software or resistor configuration on power-up; the version of the XPM time switch used in remotes; it extracts signaling information on the P-side of the time switch.
- NT6X44EA—selectable by software or resistor configuration on power-up; the international version of the time switch; performs PCM conversions including A-law to Mu-law and bit inversion.
- NTAX78AB—selectable by software; an enhanced version of the time switch which provides 40 P-side ports.
- NTAX78BA—selectable by software; a universal enhanced version of the time switch which provides 40 P-side ports, a hiway mux to select DS1 versus DS30A, and PCM conversions.

## Functional description

The main functions of the NTAX78BA are:

- time switches outgoing and incoming PCM-based on connections configured in connection memory. 6X44 modes of operation have logically separate connection memories for the incoming and outgoing direction. They handle 640 channels in each direction. AX78 modes of operation

## **NTAX78BA** (continued)

support one connection memory for all connections, allowing all connections regardless of input or output.

- interfaces to 640 C-side channels on the parallel speech bus, and 1280 P-side channels on 20 serial DS60 links. In 6X44 mode, only 640 P-side channels are available for switching. All 1280 P-side channels are available in AX78 mode.
- provides selection of DS1 or DS30A P-side interface on a per-port basis (6X44 modes and AX78BA mode).
- provides parallel-to-serial and serial-to-parallel formatting of P-side PCM data.
- provides ABCD signaling bit transmit and receive interfaces for digital trunk applications.
- provides 3 ms interrupt for processor ABCD bit scanning synchronization.
- provides phase comparators that allow the central office to synchronize off a carrier (T1) connected to another office.
- provides global P-side loopback (all modes) and various other loopbacks (AX78 modes) for diagnostic purposes.
- performs PCM conversions of a per-channel basis (A-law, Mu-law, bit inversion) (6X44EA and AX78BA modes only).
- generates TDMA synch signal used in cellular applications (AX78 modes).

### Functional blocks

The NTAX78BA has the following functional blocks:

- clock generation block
- processor interface block
- TDMA synch block
- time switch block
- AB signaling block

### Clock generation block

This block generates clocks needed for the NTAX78BA card. A phase-locked loop (PLL) generates a 40.96 MHz clock synchronized to C97, the 10.24 MHz backplane system clock. This block generates various clocks, ranging from 40.96 down to 2.56 MHz. There are various delayed and inverted versions of these clocks.

This block creates the timeslot counter, which sequences from 0 to 639 based on the C195 clock. It is aligned with the frame pulse signal. This timeslot counter aligns time-division multiplexed PCM data throughout the design.

### Processor interface block

This block contains the circuitry that interfaces the time switch circuit pack to the processor for read/write access to registers and memory. This block handles the reception and generation of control signals for processor access. It also performs address decoding, latches address and data lines, and contains several internal registers. It latches data from the processor bus on writes. It latches data from other blocks (or from registers internal to this block) onto the processor bus on read operations. It latches address lines used to index into memory blocks for memory accesses in other design blocks.

The processor interface block contains three registers:

- 3 ms Interrupt Clear
- Status/Control
- Synch Phase

This block generates the 3 ms interrupt signal. This signal synchronizes AB signaling. It contains the register which clears the interrupt. This block generates the Enhanced Time Switch (ETS) signal, based on the mode of operation set by external straps or by the Status/Control register settings.

In addition, this block generates a global reset signal for the board. Two sources of this reset are the reset signal from the backplane and a reset from the power supervisor circuit. This indicates the power supply voltage drop below an acceptable level.

This block also generates a 3.3 V supply voltage for the ASIC from the 5V backplane power supply.

### TDMA synch block

This block is active in the AX78 modes of operation; its functions are not available in the 6X44 mode. This block contains five registers:

- Link Select Register
- Channel Select Register
- AX78 Version Control Register
- TDMA Synch Register
- Hardware Diagnostic Monitor Register

## NTAX78BA (continued)

The Link Select and Channel Select Registers control selection of a link and/or channel for monitoring or loopback functions. This block also performs the selected monitoring function, in which the selected channel is viewed by the Hardware Diagnostic Monitor Register. This block generates the TDMA synch signal if the unit is active.

### Time switch block

This block contains the basic PCM data path through the card. It switches PCM data from any input timeslot to any output timeslot. The C-side of the time switch contains the interface to 640 timeslots of parallel speech bus PCM data. There is one bus for the outgoing direction (POUT) and one for the incoming direction (PIN). On the C-side interface, incoming data is an output of the time switch, and outgoing data is an input to the time switch. The P-side of the time switch contains one interface to the DS1 interface cards (also used by DCH cards) and one interface to DS30A interface cards. Each of these P-side interfaces consists of 640 timeslots of PCM data, arranged as ten DS60 serial links for input and ten for output. In the 6X44 modes of operation, both of the P-side interfaces are muxed together into a single group of 640 timeslots. These P-side interfaces are selectable on a per-port basis, a port being 32 PCM channels. In AX78 mode, both groups of 640 timeslots are available for switching.

As the incoming P-side data comes into the card, it is muxed based on the hiway mux registers. These registers convert from serial to parallel, and they pass through a delay RAM to align its timing with the C-side input data. Both P-side and C-side data is stored into the data memory. Two banks of data memory ensure a constant switching delay for all channels. The system writes to one bank, while it reads from the other bank. The processor configures connection memory, which determines the order that the system reads data out of the PCM memory. PCM conversions are then performed as configured. P-side data is then converted to serial DS60 data streams and demuxed onto the correct physical interface. The C-side output data passes through a delay RAM to properly align its output before transmission.

Most variations between different modes of operation respond to an address and data translation memory. This memory exists between the processor interface and the connection memory. Translations are performed to make the interface look backward-compatible to the software. This also ensures that data in the connection memory has the same meaning in all modes of operation. No translations are required in the AX78 modes of operation.

This block allows extraction and insertion of signaling information. It is the AB Signaling Block that actually captures the signaling information and determines bit insertion. This block also contains global PCM loopback.

### AB signaling block

This block inserts and extracts AB signaling information into the PCM data stream. It extracts signaling information from incoming P-side PCM. This information passes through the time switch, and stores in RAM on the C-side of the data path. The exception is 6X44CA mode, in which it extracts and stores signaling on the P-side of the time switch (before PCM data is time switched). Select regular or superframe format so that it extracts either only A and B signaling bits, or it extracts A, B, C, and D signaling bits. It stores extracted signaling bits in memory, indexed by channel number and port. There is a separate block of memory for each type of signaling bit (ABCD). For 6X44CA mode, it indexes the incoming signaling memory by P-side timeslot address. For all other modes of operation, they index the incoming signaling memory by C-side timeslot address.

In the outgoing direction, the system inserts signaling bits into the PCM data stream based on the per-timeslot configuration set in the outgoing signaling memory. There is a memory location for each P-side timeslot. The system inserts AB or ABCD signaling bits based on the selected format. Several options exist to specify which data to put onto a particular signaling system. This includes taking information from various backplane signals. AB signaling information occurs only on DS1 P-side interfaces; none occurs on the DS30A interface.

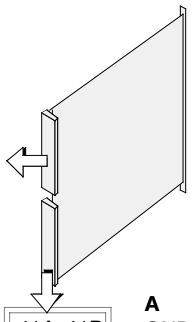
## Signaling

### Pin numbers

The pin numbers for the NTAX78BA appear in the following figure.

# NTAX78BA (continued)

### NTAX78BA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | +5V | +5V |
| 4A 4B | +5V | +5V |
| 5A 5B | GND | GND |
| 6A 6B | FPN | C97 |
| 7A 7B | GND | GND |
| 8A 8B | ACTN | |
| 9A 9B | ETSN | ETSMN |
| 10A 10B | FP48N | SBIT |
| 11A 11B | GND | GND |
| 12A 12B | DASN | TWR |
| 13A 13B | LDSN | TST1 |
| 14A 14B | DTACKN | TST0- |
| 15A 15B | UDSN | ABOUT |
| 16A 16B | WRTN | ABIN |
| 17A 17B | | 3MSIRQN |
| 18A 18B | SRSTOUTN | GND |
| 19A 19B | PINA | POUTA |
| 20A 20B | PINB | POUTB/MB |
| 21A 21B | PIN0 | POUT0 |
| 22A 22B | PIN1 | POUT1 |
| 23A 23B | PIN2 | POUT2 |
| 24A 24B | PIN3 | POUT3 |
| 25A 25B | PIN4 | POUT4 |
| 26A 26B | PIN5 | POUT5 |
| 27A 27B | PIN6 | POUT6 |
| 28A 28B | PIN7 | POUT7 |
| 29A 29B | ADDR01 | T1OUT0/C0 |
| 30A 30B | ADDR02 | T1OUT2/C2 |
| 31A 31B | ADDR03 | T1OUT4/C4 |
| 32A 32B | ADDR04 | T1OUT6/C6 |
| 33A 33B | ADDR05 | T1OUT8/C8 |
| 34A 34B | GND | GND |
| 35A 35B | ADDR06 | T1OUT10/C10 |
| 36A 36B | ADDR07 | T1OUT12/C12 |
| 37A 37B | ADDR08 | T1OUT14/C14 |
| 38A 38B | ADDR09 | T1OUT16/C16 |
| 39A 39B | ADDR10 | SV |
| 40A 40B | ADDR11 | T1OUT18/C18 |

| | A | B |
|---|---|---|
| 41A 41B | GND | DSOUT0 |
| 42A 42B | ADDR12 | DSOUT2 |
| 43A 43B | ADDR13 | DSOUT4 |
| 44A 44B | ADDR14 | DSOUT6 |
| 45A 45B | ADDR15 | DSOUT8 |
| 46A 46B | ADDR16 | DSOUT10 |
| 47A 47B | ADDR17 | DSOUT12 |
| 48A 48B | ADDR18 | DSOUT14 |
| 49A 49B | ADDR19 | DSOUT16 |
| 50A 50B | ADDR20 | DSOUT18 |
| 51A 51B | ADDR21 | GND |
| 52A 52B | | T1IN0 |
| 53A 53B | | T1IN2 |
| 54A 54B | | T1IN4 |
| 55A 55B | PSPEN | T1IN6 |
| 56A 56B | | T1IN8 |
| 57A 57B | GND | T1IN10 |
| 58A 58B | DATA00 | T1IN12 |
| 59A 59B | DATA01 | T1IN14 |
| 60A 60B | DATA02 | T1IN16 |
| 61A 61B | DATA03 | T1IN18 |
| 62A 62B | DATA04 | GND |
| 63A 63B | DATA05 | DSIN0 |
| 64A 64B | GND | DSIN2 |
| 65A 65B | DATA06 | DSIN4 |
| 66A 66B | DATA07 | DSIN6 |
| 67A 67B | DATA08 | DSIN8 |
| 68A 68B | DATA09 | DSIN10 |
| 69A 69B | DATA10 | DSIN12 |
| 70A 70B | DATA11 | DSIN14 |
| 71A 71B | DATA12 | DSIN16 |
| 72A 72B | DATA13 | DSIN18 |
| 73A 73B | DATA14 | GND |
| 74A 74B | DATA15 | RECFP0 |
| 75A 75B | | RECFP1 |
| 76A 76B | GND | GND |
| 77A 77B | | |
| 78A 78B | GND | GND |
| 79A 79B | | |
| 80A 80B | GND | GND |

# Technical data

## Electrical specifications

The electrical specifications for the NTAX78BA appear in the following table. The table identifies both the electrical drive and the load requirements for each external connector pin, including input and output characteristics.

**Backplane interface (example)**

| Parameters | Minimum | Nominal | Maximum | Units | Comments |
|---|---|---|---|---|---|
| Vil | | | 1.75 | Volts | Recognized as LOW |
| Vih | 2.25 | | | Volts | Recognized as HIGH |
| Vol | | | 0.8 | Volts | Vi=0.5V |
| Voh | NA | | | Volts | See note |

***Note:*** Since drivers are open-collector, Voh depends on backplane termination resistors.

## Power requirements

The power specifications for the NTAX78BA appear in the following table.

**Power specifications**

| Parameter | Minimum | Nominal | Maximum | Units | Comments |
|---|---|---|---|---|---|
| Supply voltage | | 5.0 | | Volts | |
| Supply ripple | | 50.0 | | mV | rms |
| Supply current | | | 0.95 | Amps | 1W measurement |

# NTAX87AA

## Product description

The remote module radio port (RMRP) card provides an interface of eight pulse code modulation voice frequency (PCM/VF) ports. The RMRP card provides an interface between the integrated cellular remote module (ICRM) and analog radio units (ARU). The RMRP provides eight RS232 serial ports that control the ARUs.

The NTAX87AA has the following features:

- eight 4-wire analog voice interfaces
- eight 9600-baud RS232 asynchronous interfaces
- program store of 128 Kbytes
- data store of 128 Kbytes

A ground loop between the ARU and the ICRM is not present. Redundant +24V and +5V sources power the NTAX87AA.

### Location

The RMRP fits in the ICRM, or the ICRM expansion shelf, of the digital cellular common equipment (DCCE).

## Functional description

The RMRP performs the following functions:

- conversion of Q.921 protocol messages in the link access procedure on the D channel (LAPD) to message length qualifier (MLQ) protocol messages
- conversion of one DS30X data channel to a RS232 serial port
- conversion of DS30X PCM channels to 4-wire VF ports
- self-diagnostics
- maintenance

### Functional blocks

The NTAX87AA has the following functional blocks:

- DS30X buffer
- DS30X interface
- CPU support block
- serial communications controller
- timer chip

- quad coder/decoder (CODEC)
- four-wire interface
- CPU
- RAM
- EPROM
- octal universal asynchronous receiver transmitter (UART)
- optically isolated RS232 interfaces
- RS232 debug interface
- power converter block

### DS30X buffer

The DS30X buffer selects one of two DS30X data streams for the RMRP to use. The DS30X buffer loops the other stream back to the inactive NTAX88 remote module time switch (RMTS) of the ICRM. The DS30X buffer passes the clock and frame pulse receive and transmit data streams in both directions to the DS30X interface. If an RMTS is not active, the DS30X buffer does not allow the clock pulse to reach the DS30X interface.

### DS30X interface

The DS30X interface block performs the following functions:

- extracts a 64 Kbps serial data stream from the DS30X data stream
- multiplexes the DS30X data streams from the two quad CODECs with the serial data streams from the serial communications controller
- assists the CPU to multiplex and demultiplex the DS30X data streams for the ICRM and the ICRM expansion shelf

### CPU support block

The CPU support block performs the following functions for the 68020 microprocessor:

- address decoding, data strobe and data strobe acknowledge (DSAK) generation, and wait-state generation
- general purpose control register
- address and data bus multiplexing for the quad CODECs
- error timing for the bus and CPU

## NTAX87AA (continued)

### Serial communications controller

The serial communications controller chip (85C30) provides the following resources:

- two serial channels
- two baud-rate generators
- two control line blocks
- two control register blocks
- interrupt control logic
- internal control block
- CPU bus interface

One serial channels communicates with the LAPD in the remote module control processor (RMCP). The other channel communicates with the debug terminal that can connect to the RMRP.

### Timer chip

The 82C54 timer chip consists of three timers, a control register and a CPU bus interface. The timer chip provides two timer interrupts to the CPU.

### Quad CODEC

The two quad CODEC blocks perform the following functions:

- ac-to-dc conversion
- dc-to-ac conversion
- transmit and receive filtering
- limited gain padding
- loopback
- DS30X-bit stream insertion and extraction for each four voice channels each

### Four-wire interface

The four-wire interface provides the following:

- level shifting
- buffering
- unipolar to balanced interface conversion
- surge protection for the audio path between the RMRP and the ARU

This block provides a precision 2.5 V and 4 V reference to the quad CODEC and loopback ability for the RMRP.

### CPU

The CPU is a 20 MHz 32-bit Motorola 68020 microprocessor operated at 16 MHz to improve the timing margins. The CPU provides the control and protocol conversion logic that the RMRP requires.

### RAM

The RAM provides the following:

- temporary data and program storage for the RMRP card
- buffers for the transmit and receive messages for the eight RS232 ports

This static RAM is 128 Kbytes by 8 bits in size.

### EPROM

The EPROM provides permanent data and program storage for the RMRP card. The ultraviolet-erasable PROM is 128 Kbytes by 8 bits in size.

### Octal UART

The octal UART is a TCM78808 chip with eight independent RS232 links. The RS232 links support the transmission and reception of asynchronous messages.

### Optically isolated RS232 interface

The optically isolated RS232 interface connects command and control messages to the ARU for call processing and maintenance functions. This interface consists of eight optically isolated RS232 links that connect the ARUs to the octal UART.

### RS232 debug interface

The RS232 debug interface block handles data transfers between a debug terminal and the RS232 debug link. The debug terminal can connect to the RMRP.

### Power converter block

The power converter block receives the following power supply:

- +24 V from the ICRM shelf power supply
- +5 V from the two power converters in the ICRM shelf (NT2X70CA)

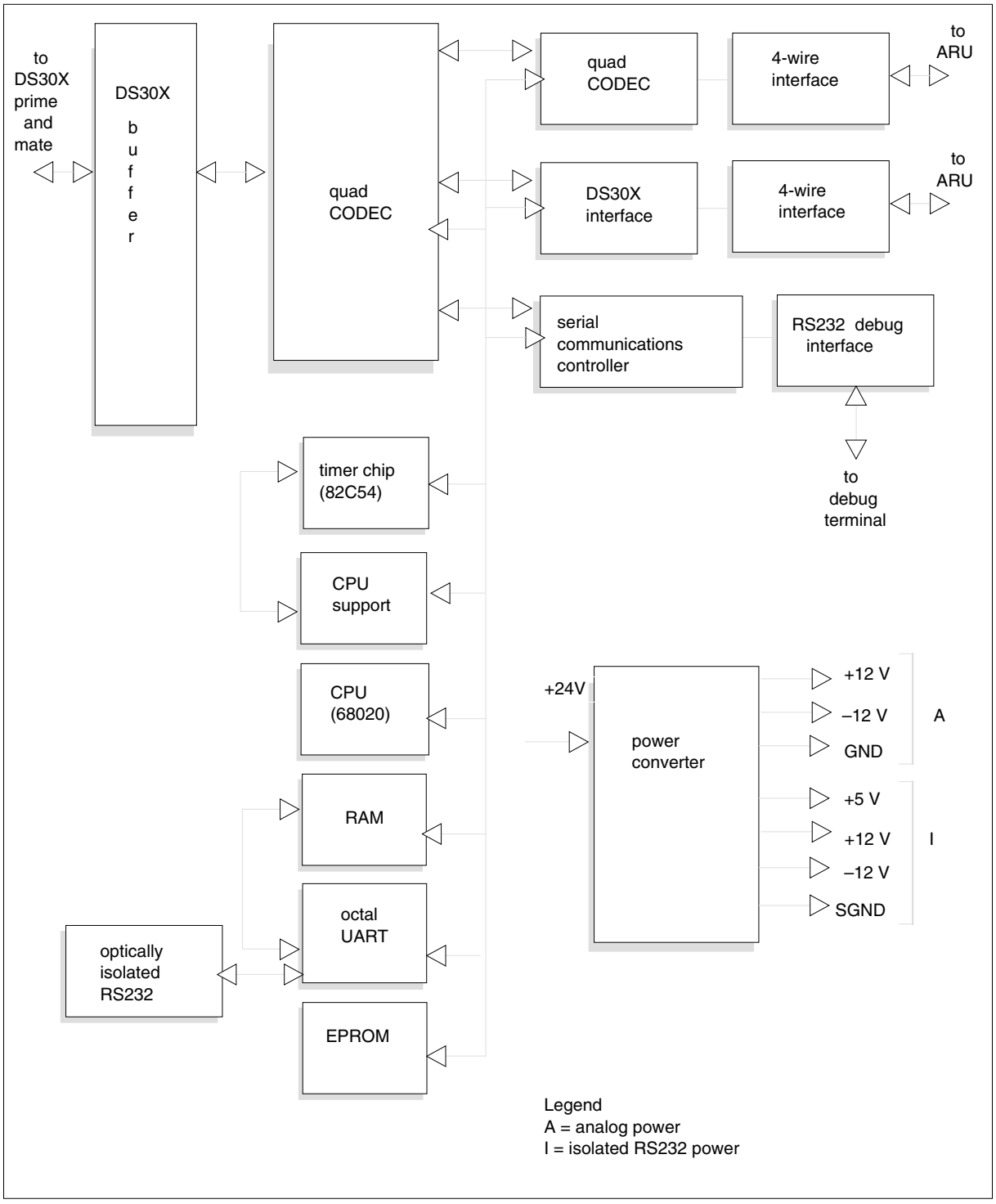
## **NTAX87AA** (continued)

The power converter block provides the following supply voltages from the +24 V power supply:

- isolated +5 V for the RS232 interfaces
- isolated +/-12 V for the RS232 interfaces
- +/-12 V for the analog interfaces

The relationship of the functional blocks appears in the following figure.

### NTAX87AA functional blocks



## **NTAX87AA** (continued)

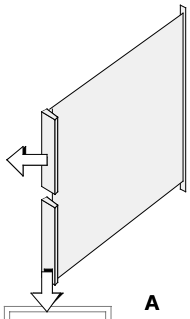
# Signaling

### Pin numbers

The pin numbers for the NTAX87AA appear in the following figure.

### NTAX87AA pin numbers

| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | RREV00 | TREV00 |
| 3A 3B | RREV01 | TREV01 |
| 4A 4B | RREV02 | TREV02 |
| 5A 5B | RREV03 | TREV03 |
| 6A 6B | RREV04 | TREV04 |
| 7A 7B | GND | GND |
| 8A 8B | GND | GND |
| 9A 9B | RREV05 | TREV05 |
| 10A 10B | RREV06 | TREV06 |
| 11A 11B | RREV07 | TREV07 |
| 12A 12B | RREV08 | TREV08 |
| 13A 13B | RREV09 | TREV09 |
| 14A 14B | RREV10 | TREV10 |
| 15A 15B | RREV11 | TREV11 |
| 16A 16B | RREV12 | TREV12 |
| 17A 17B | RREV13 | TREV13 |
| 18A 18B | RREV14 | TREV14 |
| 19A 19B | RREV15 | TREV15 |
| 20A 20B | +5V–0 | +5V–0 |
| 21A 21B | RING00 | TIP00 |
| 22A 22B | RING01 | TIP01 |
| 23A 23B | RING02 | TIP02 |
| 24A 24B | RING03 | TIP03 |
| 25A 25B | RING04 | TIP04 |
| 26A 26B | RING05 | TIP05 |
| 27A 27B | RING06 | TIP06 |
| 28A 28B | RING07 | TIP07 |
| 29A 29B | RING08 | TIP08 |
| 30A 30B | RING09 | TIP09 |
| 31A 31B | RING10 | TIP10 |
| 32A 32B | RING11 | TIP11 |
| 33A 33B | RING12 | TIP12 |
| 34A 34B | RING13 | TIP13 |
| 35A 35B | RING14 | TIP14 |
| 36A 36B | RING15 | TIP15 |
| 37A 37B | +15V | +15V |
| 38A 38B | +15V | +15V |
| 39A 39B | +5V–1 | +5V–1 |
| 40A 40B | AGND | AGND |



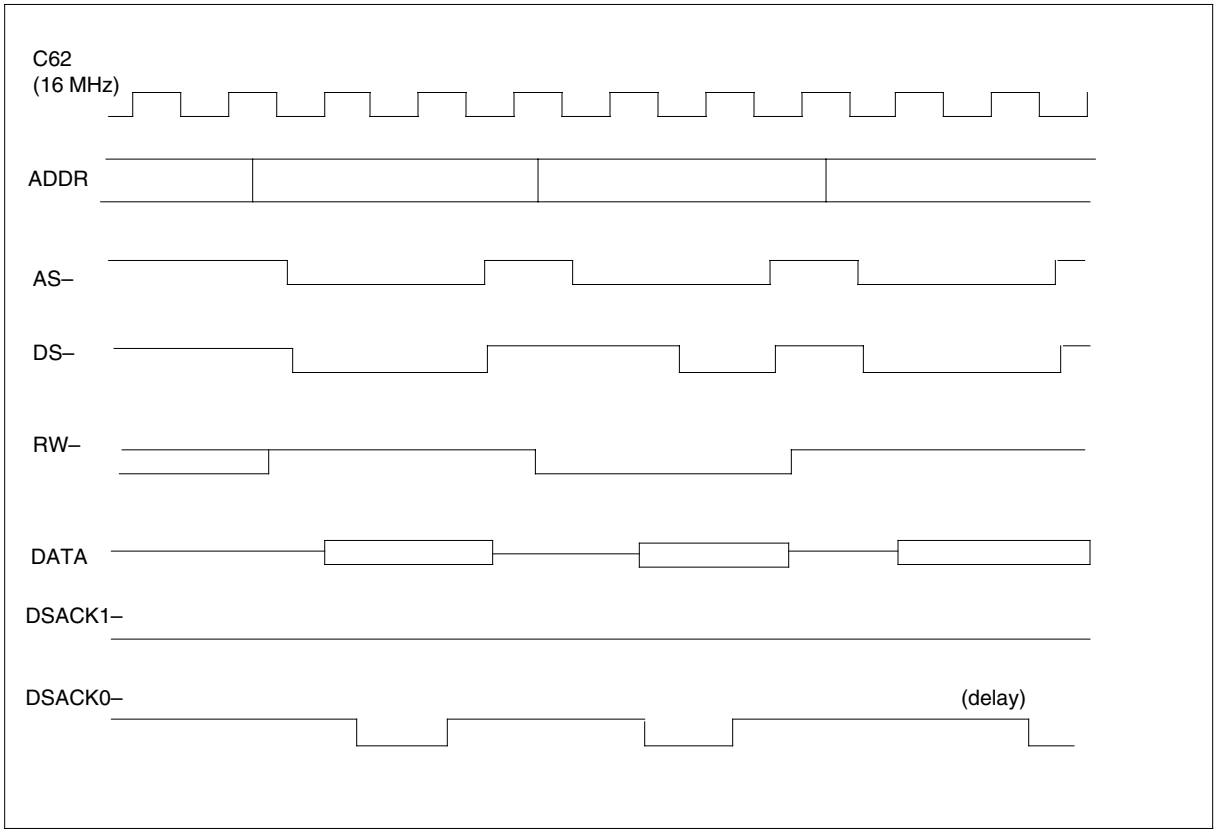
| | A | B |
|---|---|---|
| 41A 41B | GND | GND |
| 42A 42B | RDAT00 | TDAT00 |
| 43A 43B | RDAT01 | TDAT01 |
| 44A 44B | RDAT02 | TDAT02 |
| 45A 45B | RDAT03 | TDAT03 |
| 46A 46B | RDAT04 | TDAT04 |
| 47A 47B | RDAT05 | TDAT05 |
| 48A 48B | RDAT06 | TDAT06 |
| 49A 49B | RDAT07 | TDAT07 |
| 50A 50B | DGND | DGND |
| 51A 51B | DGND | DGND |
| 52A 52B | DGND | DGND |
| 53A 53B | DGND | DGND |
| 54A 54B | | |
| 55A 55B | | |
| 56A 56B | | |
| 57A 57B | | |
| 58A 58B | C195–0 | C195–1 |
| 59A 59B | SFRM–0 | SFRM–1 |
| 60A 60B | DGND | DGND |
| 61A 61B | DGND | DGND |
| 62A 62B | RDS30–0 | RDS30–1 |
| 63A 63B | SHELF | DGND |
| 64A 64B | LTD | LRD |
| 65A 65B | | |
| 66A 66B | | |
| 67A 67B | BR–0 | BR–0 |
| 68A 68B | BR–1 | BR–1 |
| 69A 69B | | |
| 70A 70B | STATUS | |
| 71A 71B | XDS30–0 | XDS30–1 |
| 72A 72B | ACT–0 | ACT–1 |
| 73A 73B | | |
| 74A 74B | +24V–0 | +24V–0 |
| 75A 75B | +24V–1 | +24V–1 |
| 76A 76B | | |
| 77A 77B | | |
| 78A 78B | | |
| 79A 79B | | |
| 80A 80B | GND | GND |

## **NTAX87AA** (continued)

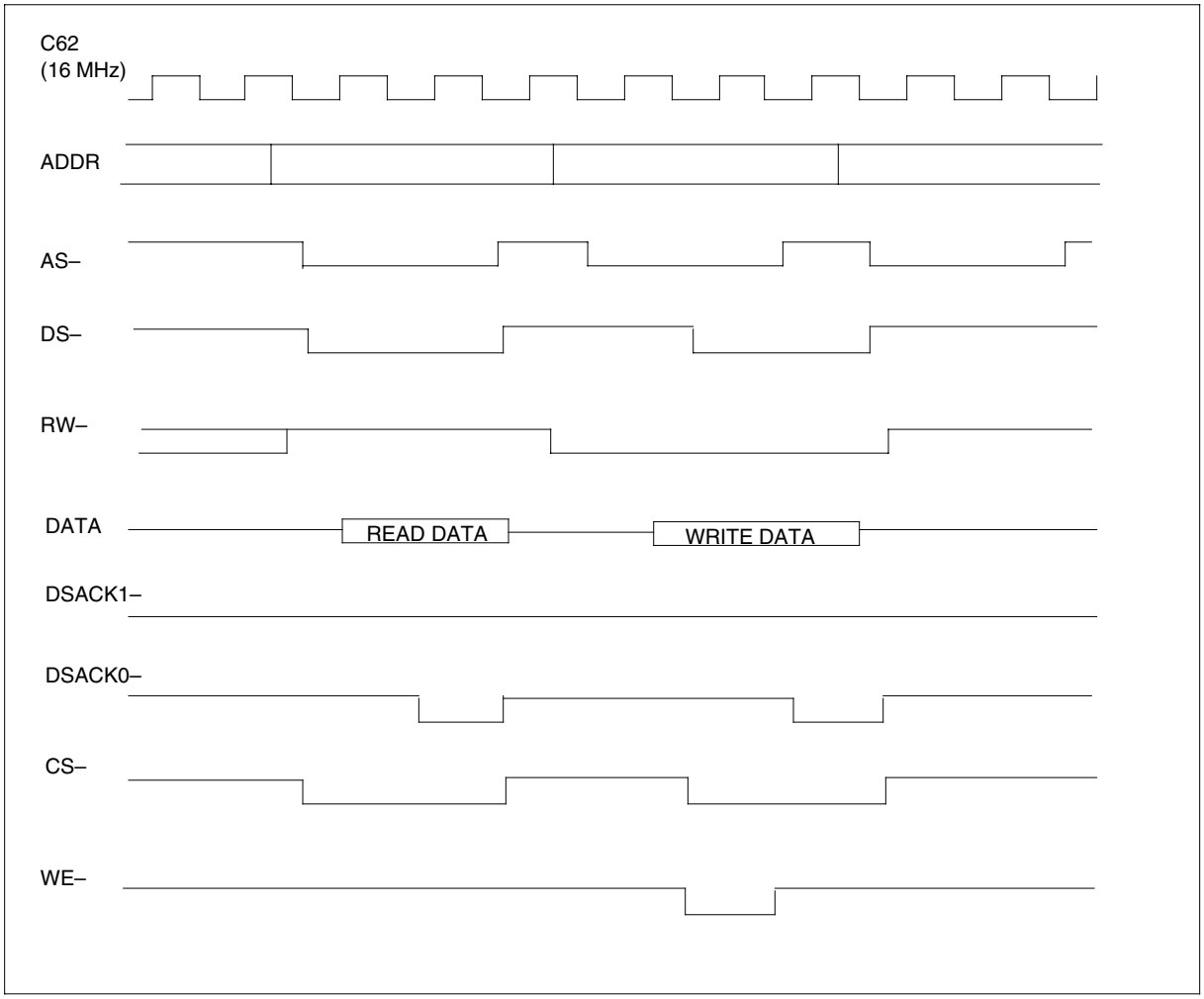
### Timing

The CPU support timing for the NTAX87AA appears in the following figure.

**NTAX87AA CPU overall timing**

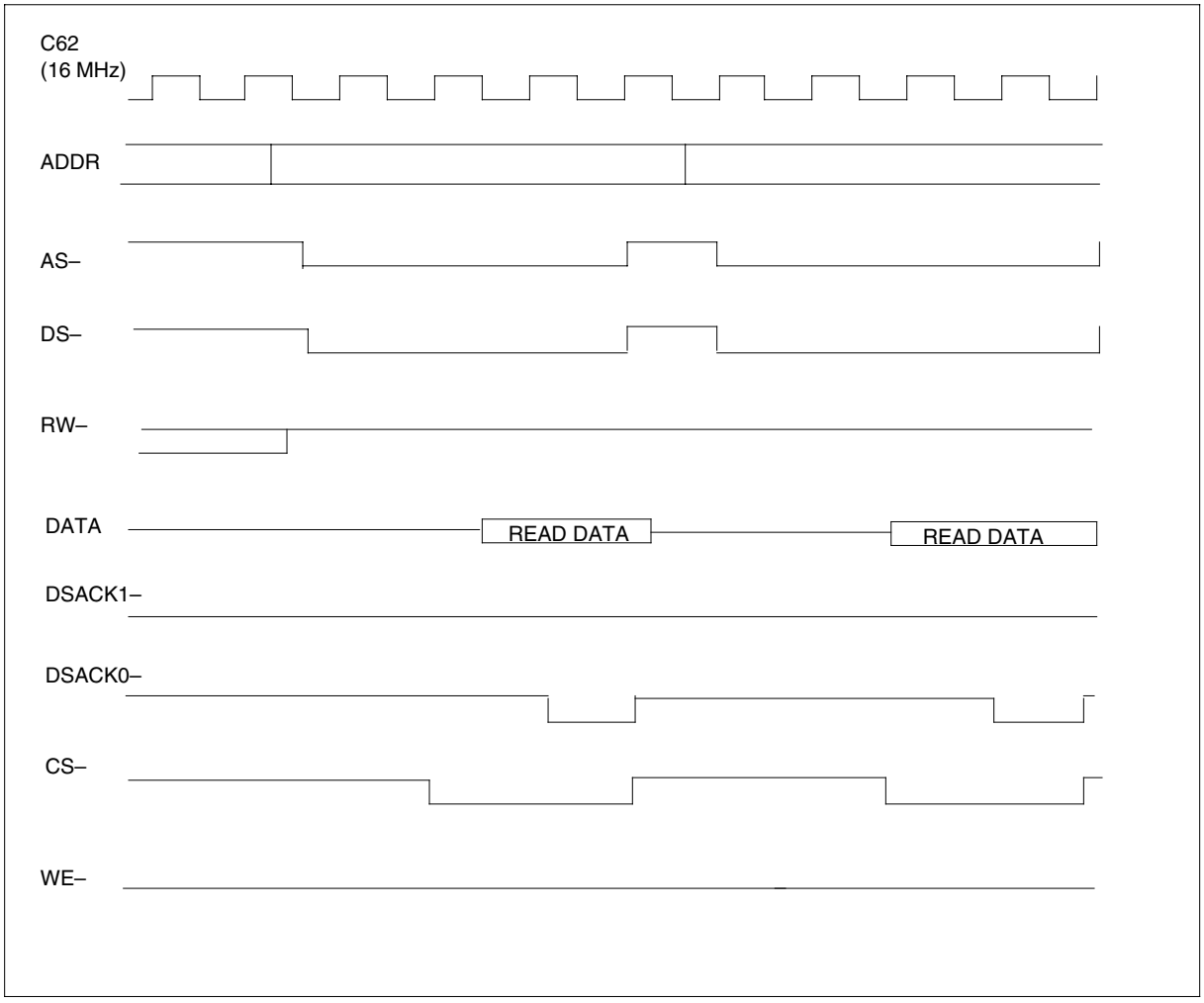


**NTAX87AA CPU-RAM timing**

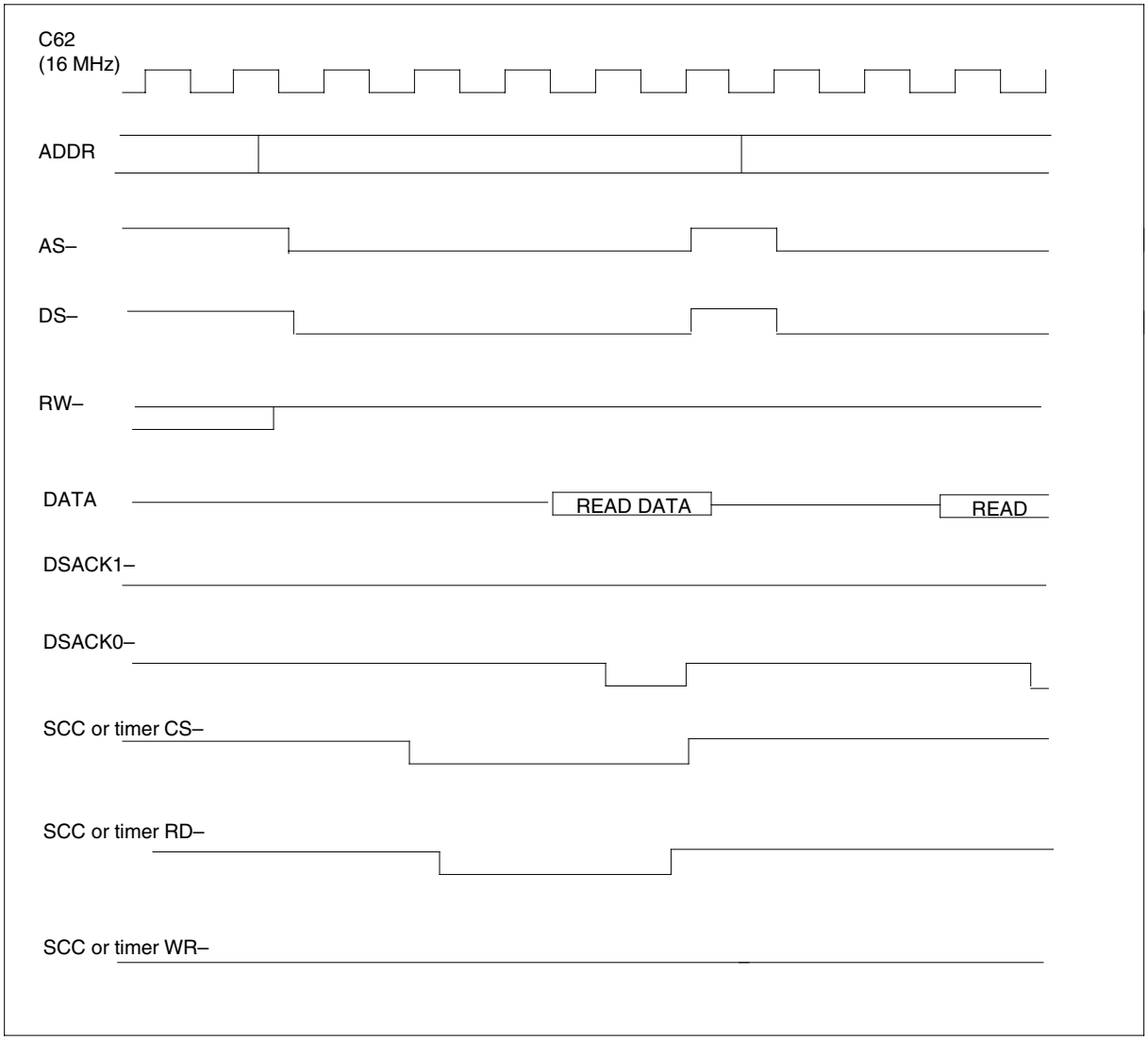


# **NTAX87AA** (continued)

### NTAX87AA CPU-EPROM timing

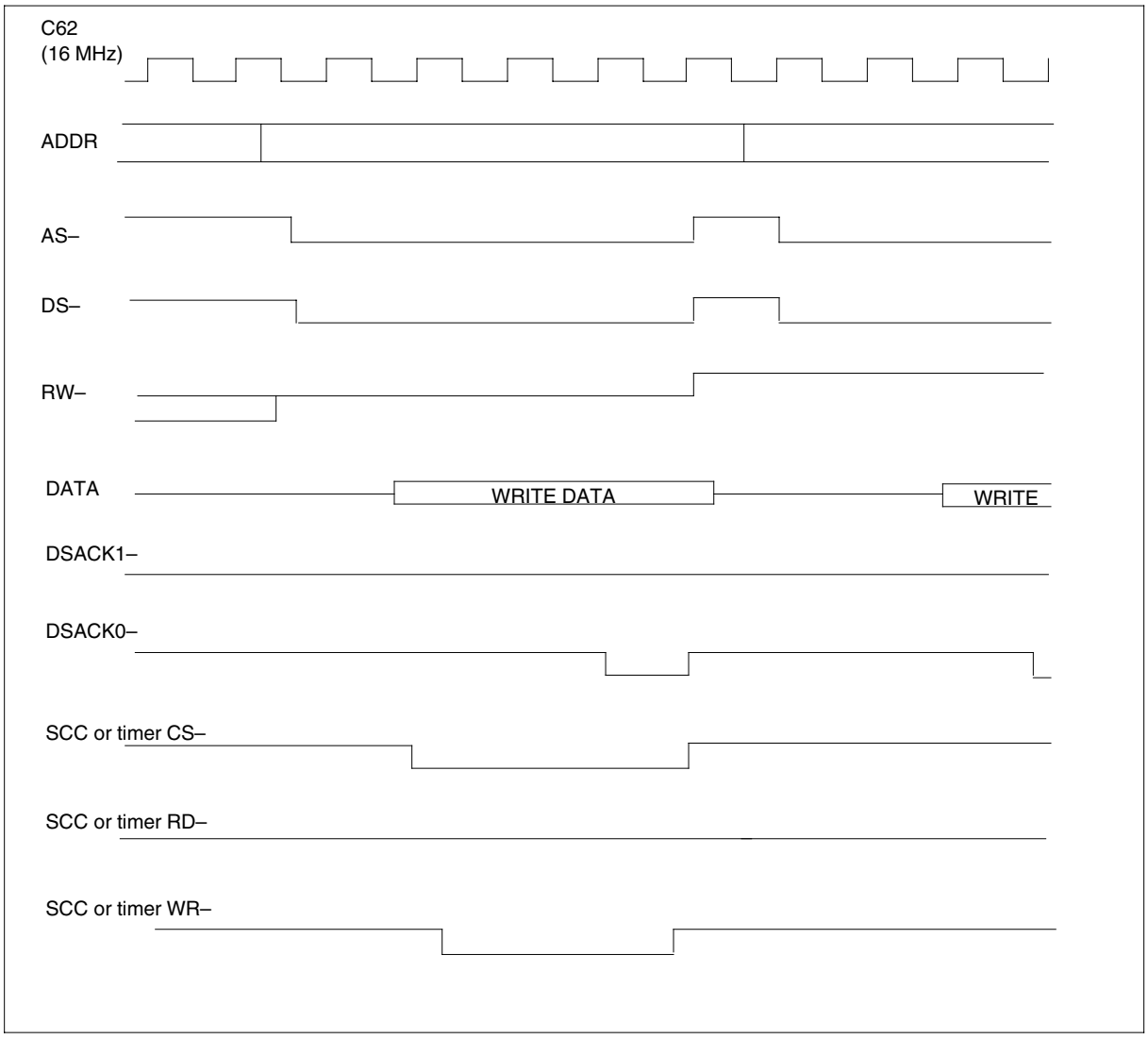


**NTAX87AA CPU-SCC or timer read timing**



## **NTAX87AA** (continued)

**NTAX87AA CPU-SCC or timer write timing**




# Technical data

### NTAX87AA Power requirements

**NTAX87AA power requirements (Sheet 1 of 2)**

| Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|
| Supply voltage | 20V | 25V | 30V |
| Supply current | 130 mA | | 200 mA |

**NTAX87AA power requirements (Sheet 2 of 2)**

| Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|
| Supply voltage | 4.75V | 5V | 5.25V |
| Supply current | 1.2A | | 2A |
| Supply voltage | 12V | 15V | 18V |
| Supply current | 80 mA | | 100 mA |

# 3 NTBXnnaa

## NTBX01AA through NTBX72AA

# NTBX01AA

## Product description

The NTBX01AA is the integrated services digital network (ISDN) pre-processor (ISP) card. The NTBX01AA provides interfaces to both the signaling processor (SP) and the speech bus.

The NTBX01AA terminates a single messaging link for each D-channel handler (DCH). The NTBX01AA processes layer-3 information. The DCH extracts the signaling information. The information goes to the master processor (MP) through the ISP.

The NTBX01AA provides the following features:

- interface to both the signaling processor (SP) and the speech bus
- processor based on the 68020 with a 16-bit data bus
- program space of 1 Mbyte
- read-only memory (ROM) space of 128 Kbyte
- access to SP and MP memories through an address bus (A-bus) interface
- parity support for each byte
- bus error on bus timeout
- extension to an external card
- interrupts

This card is part of the ISDN line trunk controller (LTCI) and is fully duplicated.

### Location

The NTBX01AA is in slot 16 of the LTCI. In this location, the card has access to the SP memory card and the speech bus.

## Functional description

The NTBX01AA performs the following functions:

- reception and transmission on 32 of 640 speech bus timeslots
- termination of DCH-originated 64 Kbit high-level data link control (HDLC) links
- window access to the following:
  - — the SP memory through the speech bus
  - — the MP memory through the SP direct memory access (DMA) with an A-bus interface

### Functional blocks

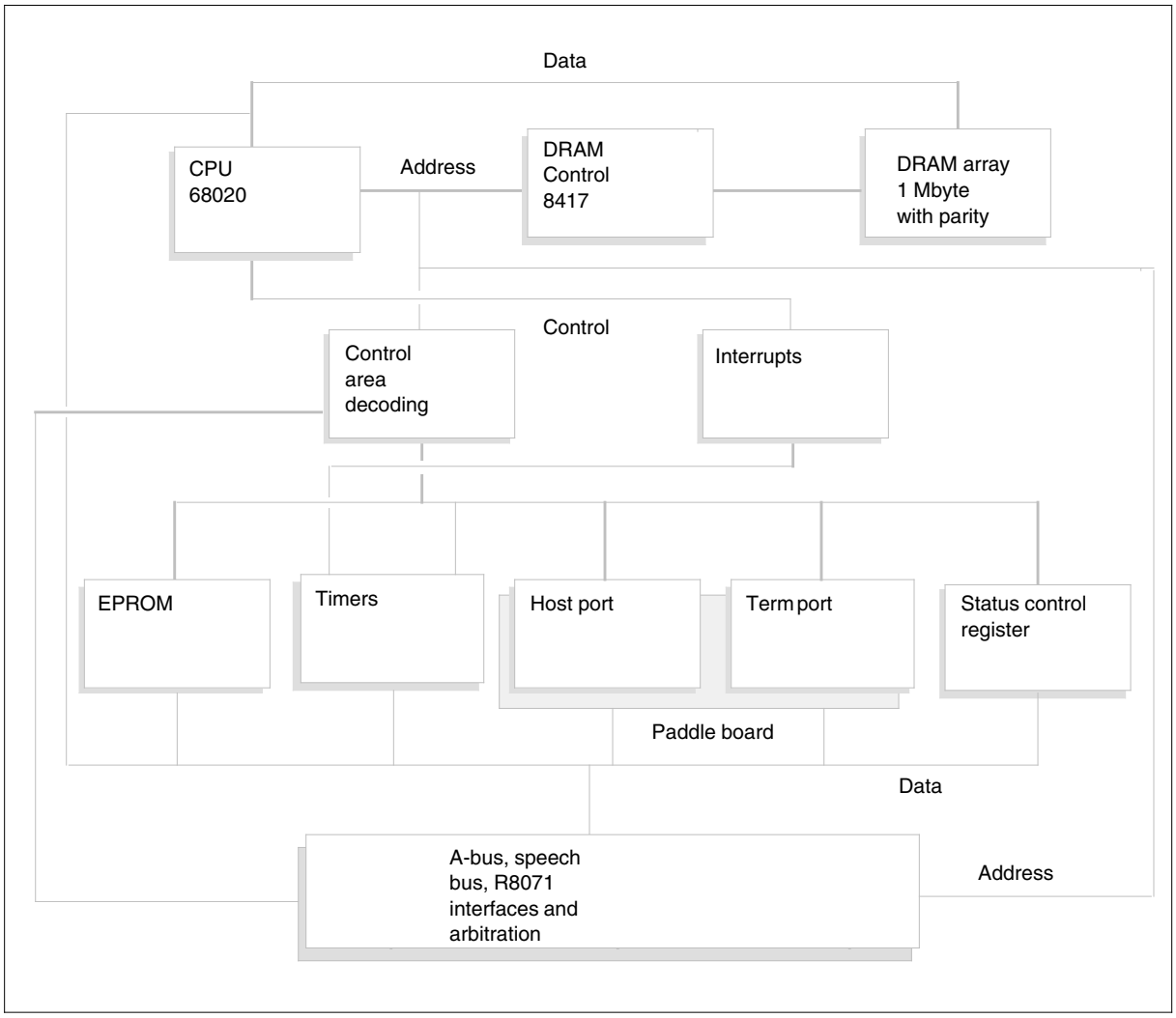
The NTBX01AA consists of the following functional blocks:

- central processing unit (CPU)
- erasable programmable read-only memory (EPROM)
- sanity timer
- bus response timer
- programmable timers
- paddle board extension
- interrupts
- an A-bus interface
- speech bus interface

The following diagram shows the functional relationship between the blocks.

## **NTBX01AA** (continued)

### NTBX01AA functional blocks




### CPU

The CPU operates at a frequency of 16 MHz. The processor supports both 8-bit and 16-bit ports.

On power-up, the system initializes ISP main blocks to a known state. A power-on reset affects the CPU, all state machines, and the programmable timers. A power-on reset also disables the sanity timer.

The program space for the processor consists of 1 Mbyte of dynamic random-access memory (DRAM). An expansion block brings the available RAM space to 16 Mbyte.

A parity bit protects each byte of memory.

### EPROM

The on-board EPROM is one 128 Kbyte device. This device appears as an 8-bit port to the CPU.

### Sanity timer

The sanity timer checks the CPU sanity in steps.

### Bus response timer

The bus response timer monitors the bus response during bus access. The timer makes sure that the bus remains active if the addressed agent does not respond.

### Programmable timers

Two programmable timers are available on the NTBX01AA:

- a scheduling timer that serves as a time base for scheduling tasks
- a general timer for event and periodic counting

### Paddle board extension

A paddle board (PB) extension provides communication with an external PB. The PB connects on the ISDN line trunk controller (LTCI) backplane.

### Address bus interface

The A-bus interface of the NTBX01AA contains a 16-bit bus interface (master only). The interface is compatible with the A-bus requirements for 16-bit masters.

The A-bus interface operates asynchronous to the CPU at the SP rate of 16 MHz.

The NTBX01AA arbitrates for the SP bus to support DMA operations When the NTBX01AA does not request access on the bus, the SP is the prime bus master.

### Speech bus interface

The speech bus interface contains:

- timeslot counter and control circuit
- receive and transmit connection memories
- receive and transmit data memories
- the R8071 serial channel counter and control circuit
- the 68020 interface

## **NTBX01AA** (end)

### Interrupts

The NTBX01AB provides seven interrupts. The seven interrupts follow in descending order of priority:

1. The sanity timer generates the sanity timeout when the sanity program does not receive service.
2. The system generates memory parity error when the system detects a parity error during a read cycle to the program space.
3. The system does not use this interrupt.
4. The general purpose timer generates general purpose timeout.
5. The scheduling timer generates clock tick interrupt. The timer uses a time base for O/S scheduling.
6. The PB0 serial ports interrupt can originate from status and control ports, host data ports, or terminal data ports.
7. The peripheral input/output interrupt register identifies level-1 interrupts.

# Technical data

### Power requirements

The NTBX01AA uses +5 V, +12 V, and -12 V supply voltages.

# NTBX01AB

## Product description

The NTBX01AB is an adjustment of the ISDN signaling pre-processor (ISP) card. An increase in the size of memory and speed of processor meets system requirements. The NTBX01AB provides interfaces to the signaling processor (SP) and to the speech bus.

The NTBX01AB terminates a single messaging link for each D-channel handler (DCH) and processes layer-3 information. The DCH extracts signaling information. The information goes to the master processor (MP) through the enhanced ISDN signaling pre-processor (EISP).

The NTBX01AB provides the following elements:

- interfaces to both the SP and the speech bus
- processor based on a 68020 with a 20-bit data bus
- program space of 4 Mbytes
- read-only memory (ROM) of 128 Kbytes
- access to SP and MP memories through an address bus (A-bus) interface
- parity support for each byte
- bus error on a bus timeout
- extension to an external card
- interrupts

The NTBX01AB card enhances the NTBX01AA card (ISDN signaling pre-processor) as follows:

- increased processor speed from 16 MHz to 20 MHz
- increased memory from 1 Mbyte to 4 Mbytes
- change of the random-access memory (RAM) interface from a 16-bit wide interface to a 32-bit wide interface
- addition of write protection

The NTBX01AB is part of the ISDN line trunk controller (LTCI) and is fully duplicated. The EISP is compatible with any equipment that uses the ISP Code. Modify any equipment that responds to processor timing to work at the faster clock speed.

### Location

The NTBX01AB resides in slot 16 of the LTCI. In this location, the card has access to the SP memory card and the speech bus.

## **NTBX01AB** (continued)

# Functional description

The NTBX01AB performs the following functions:

- reception and transmission on 32 of 640 speech bus timeslots
- termination of DCH-originated 64-Kbit high-level data link control (HDLC) links
- window access to the following:
  - — the SP memory through the speech bus
  - — the MP memory through the SP direct memory access (DMA) with an A-bus interface

### Functional blocks

The NTBX01AB consists of the following functional blocks:

- processor complex
- speech bus interface (SBIF)
- Rockwell 8071 (R8071) HDLC interface

### Processor complex

The processor complex includes the following parts:

- central processing unit (CPU)
- erasable programmable read-only memory (EPROM)
- sanity timer
- bus error timer
- programmable timers
- paddle board (PB) extension
- write protection for random-access memory (RAM)
- interrupts
- address bus (A-bus) interface

### CPU

The CPU operates at a frequency of 20 MHz. The pre-processor data bus is 32 bits wide. The pre-processor supports both 8-bit and 16-bit ports.

On power-up, the system initializes EISP main blocks to a known state. A power-on reset affects the CPU, all state machines, and the programmable timers. A power-on reset also disables the sanity timer. Two other types of

resets can occur: a system reset from the SP and a software-generated reset from the EISP.

Program space for the pre-processor consists of 4 Mbytes of dynamic RAM (DRAM). An expansion block increases available RAM to 16 Mbytes.

A parity bit protects each byte of memory.

### EPROM

On-board EPROM contains one 128 Kbyte block. The system reserves an expansion block in the memory map for future expansion. These two blocks together provide a maximum of 2 Mbytes of EPROM. On-board EPROM is an 8-bit port to the CPU.

### Sanity timer

The sanity timer checks CPU sanity in steps.

### Bus error timer

The bus error timer monitors bus response during bus access. The timer makes sure that the bus remains active if the addressed agent does not respond.

### Programmable timers

The following programmable timers are available on the NTBX01AB:

- scheduling timer that serves as a time base for scheduling tasks
- general timer for event and periodic counting

### Paddle board extension

A PB extension provides communication with an external PB. The PB connects on the LTCI backplane

### Write protection for RAM

The system write-protects memory in 1-Kbyte blocks. The system writes the correct locations in write-protected RAM.

### Interrupts

The system provides seven interrupts. The seven interrupts are listed as follows, in descending order of priority:

1. The sanity timer generates the sanity timeout when the sanity program does not receive service.
2. The system generates memory parity error when the system detects a parity error during a read cycle to the program space.
3. The system does not use this interrupt.

## **NTBX01AB** (continued)

4. The general purpose timer generates general purpose timeout.
5. The scheduling timer generates the clock tick interrupt. The timer uses the interrupt as a time base for scheduling
6. The PB0 serial ports interrupt can originate from status and control ports, host data ports, or terminal data ports.
7. The peripheral input/output interrupt register identifies level-1 interrupts

### Address bus interface

The A-bus interface consists of a 16-bit bus interface (master only). The interface is compatible with A-bus requirements for 16-bit masters. The A-bus interface operates asynchronous to the CPU at the SP rate of 16 MHz. The NTBX01AB arbitrates for the SP bus to support DMA operations. When the card does not request access on the bus, the SP is the prime bus master.

### Speech bus interface

The SBIF contains the following:

- timeslot counter and control circuit
- receive and transmit connection memories
- receive and transmit data memories
- receive and transmit buffers
- an R8071 serial channel counter and control circuit
- a 68020 interface

### Timeslot counter and control circuit

This section of the circuit generates the 640 timeslot count and other necessary control signals.

### Receive and transmit connection memories

The receive and transmit connection memories are 1 Kbyte. The output of each RAM controls the operation of the receive and transmit buffers. The output maps speech bus data on the R8071 bus.

### Receive and transmit data memories

Only the R8071 or the speech bus can access the 32-byte receive and transmit data memories. Receive data memory contains data read from the speech bus for transmission to the R8071 chip. Transmit data memory contains data that the R8071 writes for transmission to the speech bus.

### Receive and transmit buffers

The system controls receive buffers so that only one of the buffers can read in data from the speech bus. Transmit buffers can drive both sides of the speech bus.

### R8071 serial channel counter and control circuit

This circuit block generates the 32-channel count and other control signals that the Rockwell circuit block requires.

### 68020 interface

The 68020 interface allows the 68020 to program the SBIF block.

### R8071 high level data link control interface

The EISP contains one R8071 chip. The chip and support circuits are called the R8071 cell. Each cell contains the following parts:

- an R8071 multichannel HDLC chip
- static buffer memory
- first-in, first-out (FIFO)
- control register
- status register

### R8071 multichannel high-level link control chip

The chip terminates 32 full duplex HDLC channels with rates from 8 Kbps to 64 Kbps.

### Static buffer memory

Each cell contains 64 Kbytes of static RAM organized as 64-Kbyte 8-bit words. The R8071 and the CPU shares this memory. The R8071 has memory priority.

### First-in first-out

When the R8071 returns a buffer to the CPU, the R8071 asserts the interrupt pin. The R8071 updates the status byte of buffer. The channel number that directs the buffer is latched to prevent the software access to each buffer. The software access determines the buffer that needs processing. The system releases buffers faster than the software can process them. The system requires a queue to schedule the processing. The system implements a queue with a 1 Kbyte by 9 bit FIFO.

There are two modes in the FIFO: normal operation mode and test mode. In normal operation mode, the R8071 writes data to the FIFO. The CPU reads the data out. In test mode, the CPU clocks data to the FIFO.

## **NTBX01AB** (continued)

### Control register

Each R8071 cell has the following control bits:

- R8071 reset
- FIFO reset
- R8071 ATTN
- FIFO test mode
- R8071 interrupt enable
- transmit disable
- DCH reset

### Status register

The 8-bit read has 4 bits of data that are important. These bits follow:

- FIFO empty, when the bit is 0
- FIFO half full
- FIFO full, possible loss of additional entries
- R8071 ATACK, confirmation that the R8071 recognizes the ATTN signal

A pack reset clears or sets each bit.

# Technical data

### Power requirements

The NTBX01AB uses +5 V, +12 V, and -12 V supply voltages.

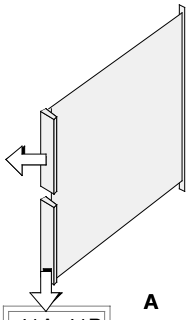
The EISP draws approximately 3.5 A from the +5V supply.

# Signaling

### Pin numbers

The following figure shows the pin numbers for the NTBX01AB.

### NTBX01AB pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | +5V | +5V |
| 4A 4B | +5V | +5V |
| 5A 5B | GND | GND |
| 6A 6B | FP– | C97+ |
| 7A 7B | GND | GND |
| 8A 8B | | |
| 9A 9B | BUSBSY | BREQ |
| 10A 10B | 8.192M+ | M8.192M+ |
| 11A 11B | GND | GND |
| 12A 12B | DAS | BGOUT |
| 13A 13B | LDS | BUSGRI |
| 14A 14B | DTACK | DCHRIST– |
| 15A 15B | UDS | MDCHRST– |
| 16A 16B | WRT | SBOV– |
| 17A 17B | CK125+ | |
| 18A 18B | RSTIN | |
| 19A 19B | | |
| 20A 20B | | |
| 21A 21B | PSIN0 | PSOUT0 |
| 22A 22B | PSIN1 | PSOUT1 |
| 23A 23B | PSIN2 | PSOUT2 |
| 24A 24B | PSIN3 | PSOUT3 |
| 25A 25B | PSIN4 | PSOUT4 |
| 26A 26B | PSIN5 | PSOUT5 |
| 27A 27B | PSIN6 | PSOUT6 |
| 28A 28B | PSIN7 | PSOUT7 |
| 29A 29B | ADD1 | |
| 30A 30B | ADD2 | |
| 31A 31B | ADD3 | |
| 32A 32B | ADD4 | |
| 33A 33B | ADD5 | |
| 34A 34B | GND | GND |
| 35A 35B | ADD6 | |
| 36A 36B | ADD7 | |
| 37A 37B | ADD8 | |
| 38A 38B | ADD9 | PB0 |
| 39A 39B | ADD10 | PB1 |
| 40A 40B | ADD11 | PB2 |

| | A | B |
|---|---|---|
| 41A 41B | | PB3 |
| 42A 42B | ADD12 | PB4 |
| 43A 43B | ADD13 | PB5 |
| 44A 44B | ADD14 | PB6 |
| 45A 45B | ADD15 | PB7 |
| 46A 46B | ADD16 | PBRW– |
| 47A 47B | ADD17 | C400 |
| 48A 48B | ADD18 | SADM17+ |
| 49A 49B | ADD19 | SADM18+ |
| 50A 50B | ADD20 | SADM19+ |
| 51A 51B | ADD21 | HX– |
| 52A 52B | SEN0 | SCC– |
| 53A 53B | SEN1 | |
| 54A 54B | SEN2 | |
| 55A 55B | | |
| 56A 56B | | PBA2 |
| 57A 57B | | PBA3 |
| 58A 58B | D0 | PBA4 |
| 59A 59B | D1 | PBA5 |
| 60A 60B | D2 | |
| 61A 61B | D3 | |
| 62A 62B | D4 | PBSCCD0– |
| 63A 63B | D5 | PBDS– |
| 64A 64B | GND | GND |
| 65A 65B | D6 | DWR– |
| 66A 66B | D7 | SCCINT |
| 67A 67B | D8 | PBORST– |
| 68A 68B | D9 | ENDP |
| 69A 69B | D10 | CK62+ |
| 70A 70B | D11 | DPCK |
| 71A 71B | D12 | |
| 72A 72B | D13 | |
| 73A 73B | D14 | |
| 74A 74B | D15 | |
| 75A 75B | | |
| 76A 76B | GND | GND |
| 77A 77B | | |
| 78A 78B | GND | |
| 79A 79B | | |
| 80A 80B | GND | GND |

# NTBX01AC

## Product description

The NTBX01AC is the integrated services digital network (ISDN) pre-processor (ISP) card. The NTBX01AC replaces the NTBX01AB in the SMA and in the cellular XPMs that use the NTAX74AA cellular access processor (CAP). The NTBX01AC also works with the NTMX77AA unified processor (UP).

The NTBX01AC terminates a single messaging link for each D-channel handler (DCH) and processes layer-3 information. The DCH extracts signaling information.

The NTBX01AC provides the following elements:

- interfaces to the speech bus
- processor based on a 68020 with a 20-bit data bus
- program space of 4 Mbytes
- read-only memory (ROM) of 128 Kbytes
- access to UP and CAP memories through an address bus (A-bus) interface
- parity support for each byte
- bus error on a bus timeout
- extension to an external card
- interrupts

The NTBX01AC is backward compatible with the NTBX01AB with the following exception. The NTBX01AC does not work with the XPM processors, MP and SP.

The NTBX01AC is part of the ISDN line trunk controller (LTCI) and is fully duplicated.

### Location

The NTBX01AC resides in slot 16 of the LTCI.

## Functional description

The NTBX01AC performs the following functions:

- reception and transmission on 32 of 640 speech bus timeslots
- termination of DCH-originated 64-Kbit high-level data link control (HDLC) links
- window access to the following:
  - — the SP memory through the speech bus
  - — the MP memory through the SP direct memory access (DMA) with an A-bus interface

### Functional blocks

The NTBX01AC consists of the following functional blocks:

- processor complex
- speech bus interface (SBIF)
- Rockwell 8071 (R8071) HDLC interface

### Processor complex

The processor complex includes the following parts:

- central processing unit (CPU)
- erasable programmable read-only memory (EPROM)
- sanity timer
- bus error timer
- programmable timers
- paddle board (PB) extension
- write protection for random-access memory (RAM)
- interrupts
- address bus (A-bus) interface

### CPU

The CPU operates at a frequency of 20 MHz. The pre-processor data bus is 32 bits wide. The pre-processor supports both 8-bit and 16-bit ports.

On power-up, the system initializes EISP main blocks to a known state. A power-on reset affects the CPU, all state machines, and the programmable timers. A power-on reset also disables the sanity timer. Two other types of

## NTBX01AC (continued)

resets can occur: a system reset from the SP and a software-generated reset from the EISP.

Program space for the pre-processor consists of 4 Mbytes of dynamic RAM (DRAM). An expansion block increases available RAM to 16 Mbytes.

A parity bit protects each byte of memory.

### EPROM

On-board EPROM contains one 128 Kbyte block. The system reserves an expansion block in the memory map for future expansion. These two blocks together provide a maximum of 2 Mbytes of EPROM. On-board EPROM is an 8-bit port to the CPU.

### Sanity timer

The sanity timer checks CPU sanity in steps.

### Bus error timer

The bus error timer monitors bus response during bus access. The timer makes sure that the bus remains active if the addressed agent does not respond.

### Programmable timers

The following programmable timers are available on the NTBX01AC:

- scheduling timer that serves as a time base for scheduling tasks
- general timer for event and periodic counting

### Paddle board extension

A PB extension provides communication with an external PB. The PB connects on the LTCI backplane

### Write protection for RAM

The system write-protects memory in 1-Kbyte blocks. The system writes the correct locations in write-protected RAM.

### Interrupts

The system provides seven interrupts. The seven interrupts are listed as follows, in descending order of priority:

1. The sanity timer generates the sanity time-out when the sanity program does not receive service.
2. The system generates memory parity error when the system detects a parity error during a read cycle to the program space.
3. The system does not use this interrupt.

4. The general purpose timer generates general purpose time-out.
5. The scheduling timer generates the clock tick interrupt. The timer uses the interrupt as a time base for scheduling
6. The PB0 serial ports interrupt can originate from status and control ports, host data ports, or terminal data ports.
7. The peripheral input/output interrupt register identifies level-1 interrupts

### Address bus interface

The A-bus interface consists of a 16-bit bus interface (master only). The interface is compatible with A-bus requirements for 16-bit masters. The A-bus interface operates asynchronous to the CPU.

### Speech bus interface

The SBIF contains the following:

- timeslot counter and control circuit
- receive and transmit connection memories
- receive and transmit data memories
- receive and transmit buffers
- an R8071 serial channel counter and control circuit
- a 68020 interface

### Timeslot counter and control circuit

This section of the circuit generates the 640 timeslot count and other necessary control signals.

### Receive and transmit connection memories

The receive and transmit connection memories are 1 Kbyte. The output of each RAM controls the operation of the receive and transmit buffers. The output maps speech bus data on the R8071 bus.

### Receive and transmit data memories

Only the R8071 or the speech bus can access the 32-byte receive and transmit data memories. Receive data memory contains data read from the speech bus for transmission to the R8071 chip. Transmit data memory contains data that the R8071 writes for transmission to the speech bus.

### Receive and transmit buffers

The system controls receive buffers so that only one of the buffers can read in data from the speech bus. Transmit buffers can drive both sides of the speech bus.

## NTBX01AC (continued)

### R8071 serial channel counter and control circuit

This circuit block generates the 32-channel count and other control signals that the Rockwell circuit block requires.

### 68020 interface

The 68020 interface allows the 68020 to program the SBIF block.

### R8071 high level data link control interface

The EISP contains one R8071 chip. The chip and support circuits are called the R8071 cell. Each cell contains the following parts:

- an R8071 multichannel HDLC chip
- static buffer memory
- first-in, first-out (FIFO)
- control register
- status register

### R8071 multichannel high-level link control chip

The chip terminates 32 full duplex HDLC channels with rates from 8 Kbps to 64 Kbps.

### Static buffer memory

Each cell contains 64 Kbytes of static RAM organized as 64-Kbyte 8-bit words. The R8071 and the CPU shares this memory. The R8071 has memory priority.

### First-in first-out

When the R8071 returns a buffer to the CPU, the R8071 asserts the interrupt pin. The R8071 updates the status byte of buffer. The channel number that directs the buffer is latched to prevent the software access to each buffer. The software access determines the buffer that needs processing. The system releases buffers faster than the software can process them. The system requires a queue to schedule the processing. The system implements a queue with a 1 Kbyte by 9 bit FIFO.

There are two modes in the FIFO: normal operation mode and test mode. In normal operation mode, the R8071 writes data to the FIFO. The CPU reads the data out. In test mode, the CPU clocks data to the FIFO.

### Control register

Each R8071 cell has the following control bits:

- R8071 reset
- FIFO reset
- R8071 ATTN
- FIFO test mode
- R8071 interrupt enable
- transmit disable
- DCH reset

### Status register

The 8-bit read has 4 bits of data that are important. These bits follow:

- FIFO empty, when the bit is 0
- FIFO half full
- FIFO full, possible loss of additional entries
- R8071 ATACK, confirmation that the R8071 recognizes the ATTN signal

A pack reset clears or sets each bit.

## Technical data

### Power requirements

The NTBX01AC uses +5 V, +12 V, and -12 V supply voltages.

The EISP draws approximately 3.5 A from the +5 V supply.

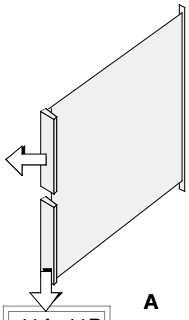
## Signaling

### Pin numbers

The following figure shows the pin numbers for the NTBX01AC.

# **NTBX01AC** (end)

### NTBX01AC pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | +5V | +5V |
| 4A 4B | +5V | +5V |
| 5A 5B | GND | GND |
| 6A 6B | FP– | C97+ |
| 7A 7B | GND | GND |
| 8A 8B | | |
| 9A 9B | BUSBSY | BREQ |
| 10A 10B | 8.192M+ | M8.192M+ |
| 11A 11B | GND | GND |
| 12A 12B | DAS | BGOUT |
| 13A 13B | LDS | BUSGRI |
| 14A 14B | DTACK | DCHRIST– |
| 15A 15B | UDS | MDCHRST– |
| 16A 16B | WRT | SBOV– |
| 17A 17B | CK125+ | |
| 18A 18B | RSTIN | |
| 19A 19B | | |
| 20A 20B | | |
| 21A 21B | PSIN0 | PSOUT0 |
| 22A 22B | PSIN1 | PSOUT1 |
| 23A 23B | PSIN2 | PSOUT2 |
| 24A 24B | PSIN3 | PSOUT3 |
| 25A 25B | PSIN4 | PSOUT4 |
| 26A 26B | PSIN5 | PSOUT5 |
| 27A 27B | PSIN6 | PSOUT6 |
| 28A 28B | PSIN7 | PSOUT7 |
| 29A 29B | ADD1 | |
| 30A 30B | ADD2 | |
| 31A 31B | ADD3 | |
| 32A 32B | ADD4 | |
| 33A 33B | ADD5 | |
| 34A 34B | GND | GND |
| 35A 35B | ADD6 | |
| 36A 36B | ADD7 | |
| 37A 37B | ADD8 | |
| 38A 38B | ADD9 | PB0 |
| 39A 39B | ADD10 | PB1 |
| 40A 40B | ADD11 | PB2 |

| | A | B |
|---|---|---|
| 41A 41B | | PB3 |
| 42A 42B | ADD12 | PB4 |
| 43A 43B | ADD13 | PB5 |
| 44A 44B | ADD14 | PB6 |
| 45A 45B | ADD15 | PB7 |
| 46A 46B | ADD16 | PBRW– |
| 47A 47B | ADD17 | C400 |
| 48A 48B | ADD18 | SADM17+ |
| 49A 49B | ADD19 | SADM18+ |
| 50A 50B | ADD20 | SADM19+ |
| 51A 51B | ADD21 | HX– |
| 52A 52B | SEN0 | SCC– |
| 53A 53B | SEN1 | |
| 54A 54B | SEN2 | |
| 55A 55B | | |
| 56A 56B | | PBA2 |
| 57A 57B | | PBA3 |
| 58A 58B | D0 | PBA4 |
| 59A 59B | D1 | PBA5 |
| 60A 60B | D2 | |
| 61A 61B | D3 | |
| 62A 62B | D4 | PBSCCD0– |
| 63A 63B | D5 | PBDS– |
| 64A 64B | GND | GND |
| 65A 65B | D6 | DWR– |
| 66A 66B | D7 | SCCINT |
| 67A 67B | D8 | PBORST– |
| 68A 68B | D9 | ENDP |
| 69A 69B | D10 | CK62+ |
| 70A 70B | D11 | DPCK |
| 71A 71B | D12 | |
| 72A 72B | D13 | |
| 73A 73B | D14 | |
| 74A 74B | D15 | |
| 75A 75B | | |
| 76A 76B | GND | GND |
| 77A 77B | | |
| 78A 78B | GND | |
| 79A 79B | | |
| 80A 80B | GND | GND |

# NTBX01BA

## Product description

The NTBX01BA is a redesign of the enhanced ISDN signaling pre-processor (EISP) card. The NTBX01BA improves the functionality and stability of the pack.

The NTBX01BA terminates a single messaging link for each D-channel handler (DCH) and processes layer-3 information. The DCH extracts signaling information.

The NTBX01BA provides the following elements:

- interfaces to the speech bus
- processor based on a 68020 with a 20-bit data bus
- program space of 4 Mbytes
- read-only memory (ROM) of 128 Kbytes
- access UP and CAP memories through an address bus (A-bus) interface
- parity support for each byte
- bus error on a bus timeout
- extension to an external card
- interrupts

The NTBX01BA card contains the following additions:

- processor access to the speech bus data rams
- configuration prom

The NTBX01BA is compatible with the NTMX77AA cellular access processor (CAP) and the NTAX74AA unified processor (UP). The NTBX01BA is not compatible with the master processor (MP) and signalling processor (SP) configuration.

The NTBX01BA is part of the ISDN line trunk controller (LTCI) and is fully duplicated. The EISP is compatible with any equipment that uses the ISP Code. Modify any equipment that responds to processor timing to work at the faster clock speed.

### Location

The NTBX01BA resides in slot 16 of the LTCI.

## **NTBX01BA** (continued)

# Functional description

The NTBX01BA performs the following functions:

- reception and transmission on 32 of 640 speech bus timeslots
- termination of DCH-originated 64-Kbit high-level data link control (HDLC) links
- window access to the UP and CAP memory via the A-bus interface

### Functional blocks

The NTBX01BA consists of the following functional blocks:

- processor complex
- speech bus interface (SBIF)
- Rockwell 8071 (R8071) HDLC interface

### Processor complex

The processor complex includes the following parts:

- central processing unit (CPU)
- erasable programmable read-only memory (EPROM)
- sanity timer
- bus error timer
- programmable timers
- paddle board (PB) extension
- write protection for random-access memory (RAM)
- interrupts
- address bus (A-bus) interface

### CPU

The CPU operates at a frequency of 20 MHz. The pre-processor data bus is 32 bits wide. The pre-processor supports both 8-bit and 16-bit ports.

On power-up, the system initializes EISP main blocks to a known state. A power-on reset affects the CPU, all state machines, and the programmable timers. A power-on reset also disables the sanity timer. Two other types of resets can occur: a system reset from the XPM and a software-generated reset from the EISP.

Program space for the pre-processor consists of 4 Mbytes of dynamic RAM (DRAM). An expansion block increases available RAM to 16 Mbytes.

A parity bit protects each byte of memory.

### EPROM

On-board EPROM contains one 128 Kbyte block. The system reserves an expansion block in the memory map for future expansion. These two blocks together provide a maximum of 2 Mbytes of EPROM. On-board EPROM is an 8-bit port to the CPU.

### Sanity timer

The sanity timer checks CPU sanity in steps.

### Bus error timer

The bus error timer monitors bus response during bus access. The timer makes sure that the bus remains active if the addressed agent does not respond.

### Programmable timers

The following programmable timers are available on the NTBX01BA:

- scheduling timer that serves as a time base for scheduling tasks
- general timer for event and periodic counting

### Paddle board extension

A PB extension provides communication with an external PB. The PB connects on the LTCI backplane

### Write protection for RAM

The system write-protects memory in 1-Kbyte blocks. The system writes the correct locations in write-protected RAM.

### Interrupts

The system provides seven interrupts. The seven interrupts are listed as follows, in descending order of priority:

1. The sanity timer generates the sanity timeout when the sanity program does not receive service.
2. The system generates memory parity error when the system detects a parity error during a read cycle to the program space.
3. The system does not use this interrupt.
4. The general purpose timer generates general purpose timeout.
5. The scheduling timer generates the clock tick interrupt. The timer uses the interrupt as a time base for scheduling

## NTBX01BA (continued)

6. The PB0 serial ports interrupt can originate from status and control ports, host data ports, or terminal data ports.
7. The peripheral input/output interrupt register identifies level-1 interrupts

### Address bus interface

The address bus (A-bus) interface has a 16-bit bus interface (master only). The interface is compatible with A-bus requirements for 16-bit masters. The A-bus interface operates asynchronous to the CPU at the rate of 20 MHz.

### Speech bus interface

The SBIF contains the following:

- timeslot counter and control circuit
- receive and transmit connection memories
- receive and transmit data memories
- receive and transmit buffers
- an R8071 serial channel counter and control circuit
- a 68020 interface

### Timeslot counter and control circuit

This section of the circuit generates the 640 timeslot count and other necessary control signals.

### Receive and transmit connection memories

The receive and transmit connection memories are 1 Kbyte. The output of each RAM controls the operation of the receive and transmit buffers. The output maps speech bus data on the R8071 bus.

### Receive and transmit data memories

Only the R8071 or the speech bus can access the 32-byte receive and transmit data memories. Receive data memory contains data read from the speech bus for transmission to the R8071 chip. Transmit data memory contains data that the R8071 writes for transmission to the speech bus.

### Receive and transmit buffers

The system controls receive buffers so that only one of the buffers can read in data from the speech bus. Transmit buffers can drive both sides of the speech bus.

### R8071 serial channel counter and control circuit

This circuit block generates the 32-channel count and other control signals that the Rockwell circuit block requires.

### 68020 interface

The 68020 interface allows the 68020 to program the SBIF block.

### R8071 high level data link control interface

The EISP contains one R8071 chip. The chip and support circuits are called the R8071 cell. Each cell contains the following parts:

- an R8071 multichannel HDLC chip
- static buffer memory
- first-in, first-out (FIFO)
- control register
- status register

### R8071 multichannel high-level link control chip

The chip terminates 32 full duplex HDLC channels with rates from 8 Kbps to 64 Kbps.

### Static buffer memory

Each cell contains 64 Kbytes of static RAM organized as 64-Kbyte 8-bit words. The R8071 and the CPU shares this memory. The R8071 has memory priority.

### First-in first-out

When the R8071 returns a buffer to the CPU, the R8071 asserts the interrupt pin. The R8071 updates the status byte of buffer. The channel number that directs the buffer is latched to prevent the software access to each buffer. The software access determines the buffer that needs processing. The system releases buffers faster than the software can process them. The system requires a queue to schedule the processing. The system implements a queue with a 1 Kbyte by 9 bit FIFO.

There are two modes in the FIFO: normal operation mode and test mode. In normal operation mode, the R8071 writes data to the FIFO. The CPU reads the data out. In test mode, the CPU clocks data to the FIFO.

### Control register

Each R8071 cell has the following control bits:

- R8071 reset
- FIFO reset
- R8071 ATTN
- FIFO test mode

## **NTBX01BA** (continued)

- R8071 interrupt enable
- transmit disable
- DCH reset

### Status register

The 8-bit read has 4 bits of data that are important. These bits follow:

- FIFO empty, when the bit is 0
- FIFO half full
- FIFO full, possible loss of additional entries
- R8071 ATACK, confirmation that the R8071 recognizes the ATTN signal

A pack reset clears or sets each bit.

# Technical data

### Power requirements

The NTBX01BA uses a +5 V supply voltage.

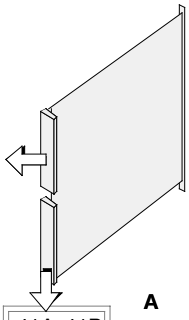
The EISP draws approximately 2.5 A from the +5 V supply

# Signaling

### Pin numbers

The following figure shows the pin numbers for the NTBX01BA.

### NTBX01BA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | +5V | +5V |
| 4A 4B | +5V | +5V |
| 5A 5B | GND | GND |
| 6A 6B | FP– | C97+ |
| 7A 7B | GND | GND |
| 8A 8B | | |
| 9A 9B | BUSBSY | BREQ |
| 10A 10B | 8.192M+ | M8.192M+ |
| 11A 11B | GND | GND |
| 12A 12B | DAS | BGOUT |
| 13A 13B | LDS | BUSGRI |
| 14A 14B | DTACK | DCHRIST– |
| 15A 15B | UDS | MDCHRST– |
| 16A 16B | WRT | SBOV– |
| 17A 17B | CK125+ | |
| 18A 18B | RSTIN | |
| 19A 19B | | |
| 20A 20B | | |
| 21A 21B | PSIN0 | PSOUT0 |
| 22A 22B | PSIN1 | PSOUT1 |
| 23A 23B | PSIN2 | PSOUT2 |
| 24A 24B | PSIN3 | PSOUT3 |
| 25A 25B | PSIN4 | PSOUT4 |
| 26A 26B | PSIN5 | PSOUT5 |
| 27A 27B | PSIN6 | PSOUT6 |
| 28A 28B | PSIN7 | PSOUT7 |
| 29A 29B | ADD1 | |
| 30A 30B | ADD2 | |
| 31A 31B | ADD3 | |
| 32A 32B | ADD4 | |
| 33A 33B | ADD5 | |
| 34A 34B | GND | GND |
| 35A 35B | ADD6 | |
| 36A 36B | ADD7 | |
| 37A 37B | ADD8 | |
| 38A 38B | ADD9 | PB0 |
| 39A 39B | ADD10 | PB1 |
| 40A 40B | ADD11 | PB2 |

| | A | B |
|---|---|---|
| 41A 41B | | PB3 |
| 42A 42B | ADD12 | PB4 |
| 43A 43B | ADD13 | PB5 |
| 44A 44B | ADD14 | PB6 |
| 45A 45B | ADD15 | PB7 |
| 46A 46B | ADD16 | PBRW– |
| 47A 47B | ADD17 | C400 |
| 48A 48B | ADD18 | SADM17+ |
| 49A 49B | ADD19 | SADM18+ |
| 50A 50B | ADD20 | SADM19+ |
| 51A 51B | ADD21 | HX– |
| 52A 52B | SEN0 | SCC– |
| 53A 53B | SEN1 | PBRST– |
| 54A 54B | SEN2 | |
| 55A 55B | | |
| 56A 56B | | PBA2 |
| 57A 57B | | PBA3 |
| 58A 58B | D0 | PBA4 |
| 59A 59B | D1 | PBA5 |
| 60A 60B | D2 | |
| 61A 61B | D3 | |
| 62A 62B | D4 | PBSCCD0– |
| 63A 63B | D5 | PBDS– |
| 64A 64B | GND | GND |
| 65A 65B | D6 | DWR– |
| 66A 66B | D7 | SCCINT |
| 67A 67B | D8 | PBORST– |
| 68A 68B | D9 | ENDP |
| 69A 69B | D10 | CK62+ |
| 70A 70B | D11 | DPCK |
| 71A 71B | D12 | |
| 72A 72B | D13 | |
| 73A 73B | D14 | |
| 74A 74B | D15 | |
| 75A 75B | | |
| 76A 76B | GND | GND |
| 77A 77B | | |
| 78A 78B | GND | GND |
| 79A 79B | | |
| 80A 80B | GND | GND |

# NTBX02AA

## Product description

The NTBX02AA is the D-channel handler card. The system uses the NTBX02AA in the ISDN line trunk controller (LTCI).

The NTBX02AA selects a unit of the LTCI for communication. The LTCI activity determines the selection. The card terminates one half of a DS60 interface. The card does not have other interfaces.

The NTBX02AA provides the following features:

- a 68020 processor with 16-bit data bus
- program space of 1 Mbyte
- read-only memory (ROM) space of128 Kbyte
- parity support for each byte
- bus error on bus timeout
- extension to an external card
- interrupts

### Location

The NTBX02AA is in one of ten DS-1 slots on the peripheral side (P-side) of the time switch.

## Functional description

The NTXB02AA performs the following functions:

- termination of ISDN D-channels
- communication with the ISDN signaling preprocessor (ISP) over a high-level data link control (HDLC) to transfer signaling and maintenance data
- exchange of packet data with the data networking system (DPN) through the HDLC links

### Functional blocks

The NTBX02AA has the following functional blocks:

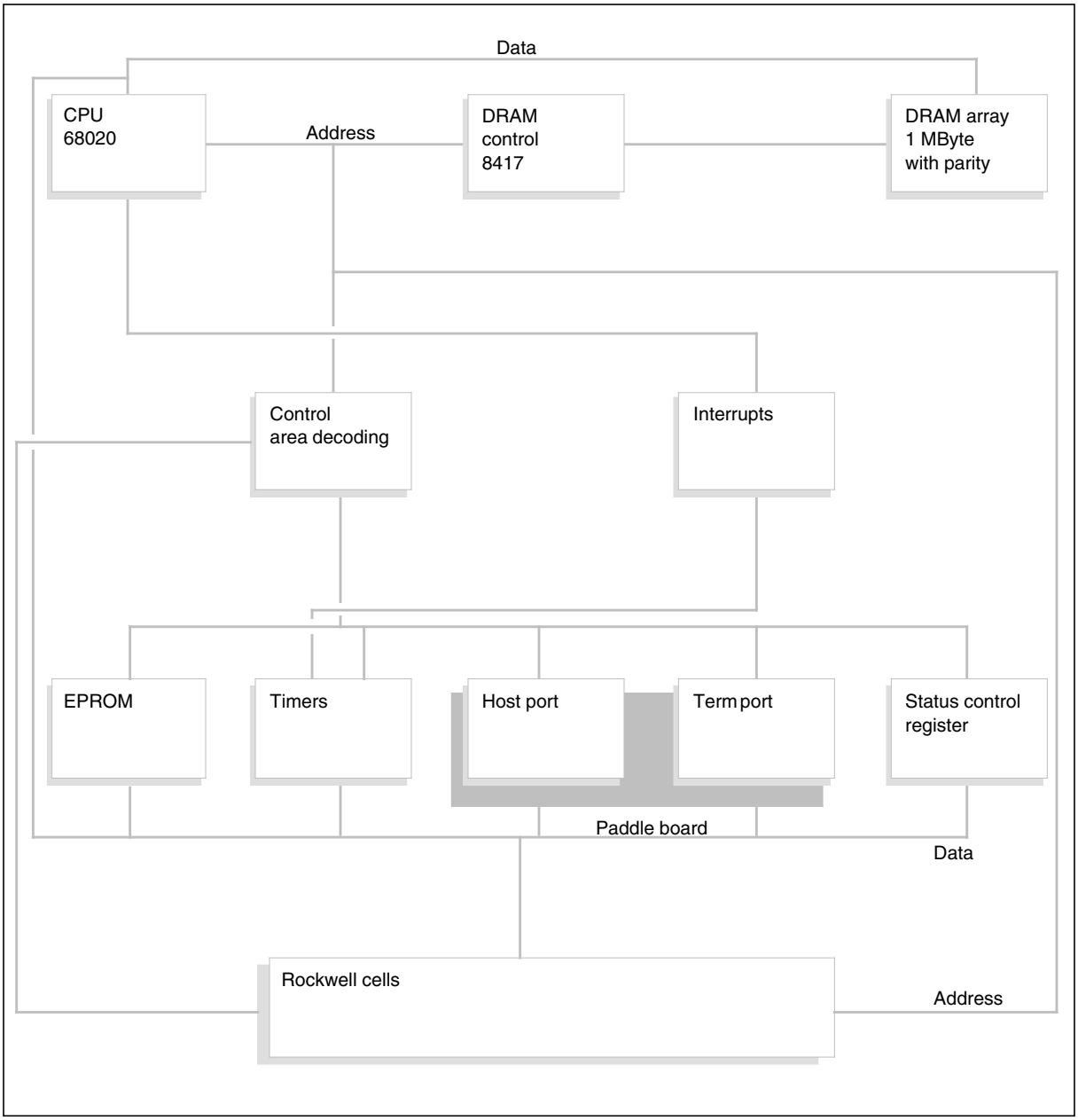
- central processing unit (CPU)
- erasable programmable read-only memory (EPROM)
- sanity timer
- bus response timer

- programmable timers
- paddle board extension
- the R8071 cells
- a DS60 interface
- interrupts

The following figure shows the relationship between the blocks.

## NTBX02AA (continued)

### NTBX02AA functional blocks




### CPU

The CPU operates at a frequency of 16 MHz. The processor supports 8-bit and 16-bit ports.

When power-up occurs, the system initializes D-channel handler (DCH) main blocks to a known state. A power-on reset affects the CPU, all state machines, and the programmable timers. A power-on reset disables the sanity timer.

The program and data space for the processor has 1 Mbyte of digital RAM (DRAM). The system provides an expansion block. The total available RAM space is 16 Mbyte.

A parity bit protects each byte of memory.

### EPROM

Combined EPROM capacity is 1 Mbyte. The on-board EPROM has a 128 Kbyte by 8 bit block. This block is an 8 bit port to the CPU.

### Sanity timer

The sanity timer checks the CPU sanity in steps.

### Bus response timer

The bus response timer monitors the bus response during bus access. The timer makes sure that the bus remains active if the addressed agent does not respond.

### Programmable timers

Two programmable timers are available on the DCH:

- a scheduling timer that is a time base for scheduling tasks
- a general timer for event and periodic counting

### Paddle board extension

A paddle board extension provides communication with an external paddle board (PB) that connects to the LTCI backplane.

### R8071 cells

The DCH has four RT8071 cells. Each cell consists of one R8071 chip. Each chip has a buffer memory and support hardware.

Each R8071 cell contains the following parts:

- an R8071 multichannel HDLC chip
- static buffer memory of 64 Kbyte that the system organizes for 8-bit access
- a 1 Kbyte by 9-bit buffer
- bus arbitration state machine

## NTBX02AA (continued)

### DS60 interface

The DS60 interface performs the following functions:

- reception of data from the odd-numbered port only. The DS60 interface drives both ports.
- exchange of data with the active unit only
- an inactive unit loopback. The data from the inactive unit uses the inactive clock and frame pulse to loop back.
- rate conversions in both directions between 2.048 MHz and 2.56 MHz

### Interrupts

The NTBX02AA has seven interrupts. The interrupts are as follows, in descending order of priority:

1. The sanity timer generates sanity timeout when the sanity program does not receive service.
2. The system generates memory parity error when the system detects a parity error during a read cycle to the program space.
3. The system does not use this interrupt.
4. The general purpose timer generates the general purpose timeout.
5. The scheduling timer generates the clock tick interrupt. The timer uses the clock tick interrupt as a time base for O/S scheduling.
6. Paddle board serial ports can generate from status and control ports, host data port, and the terminal data port.
7. peripheral input/output (I/O)

Peripheral input/output (I/O) has eight interrupts. Three interrupts are in use. The system reserves a peripheral interrupt register for these interrupts. When the processor acknowledges a level-1 interrupt, the system can poll this register to indicate the source of the interrupt. The following interrupts can occur:

- switch of activity (SWACT) detect
- frame pulse loss
- an R8071 interrupt

When the state of the activity lead on the backplane changes, the system generates the SWACT detect interrupt. This interrupt notifies the software that a SWACT occurred. Expect data errors for one frame time.

When the system misses a frame pulse, the system generates the frame pulse loss interrupt. This interrupt notifies the software that communication with the system is affected.

Any of the four R8071 cells can write information to the cell buffer. The system generates the R8071 interrupt to notify the software for traffic processing.

## Technical data

### Power requirements

The NTBX02AA has a power converter, which converts the -48V battery output to the +5V supply that the card requires.

# NTBX02BA

## Product description

The NTBX02BA is the enhanced D-channel handler card for use in the integrated services digital network (ISDN) line trunk controller (LTCI).

The NTBX02BA selects a unit of the LTCI for communication. The LTCI activity determines the selection. The card terminates one half of a DS60 interface. The card does not have other interfaces.

The NTBX02BA provides the following features:

- a 68020 processor with a 32 bit data bus
- program space of 4 Mbyte
- read-only memory (ROM) space of 128 kbyte
- parity support for each byte
- bus error on bus timeout
- extension to an external card
- interrupts
- write protect capability for RAM
- on-board C122 Rockwell clock

The NTBX02BA is compatible with any NTBX02AA application software. The processor speed increases from 16 MHz to 20 MHz. Clock-dependent software requires modification to work at the new clock speed.

### Location

The NTBX02BA is in one of ten DS-1 slots on the peripheral side (P-side) of the time switch.

## Functional description

The NTBX02BA performs the following functions:

- termination of ISDN D-channels
- handling of layer 2 signaling information frames
- communication with the ISDN signaling preprocessor (ISP) over a high-level data link control (HDLC) to transfer signaling and maintenance data
- bidirectional exchange of packet data with the data networking system (DPN) by way of the HDLC links

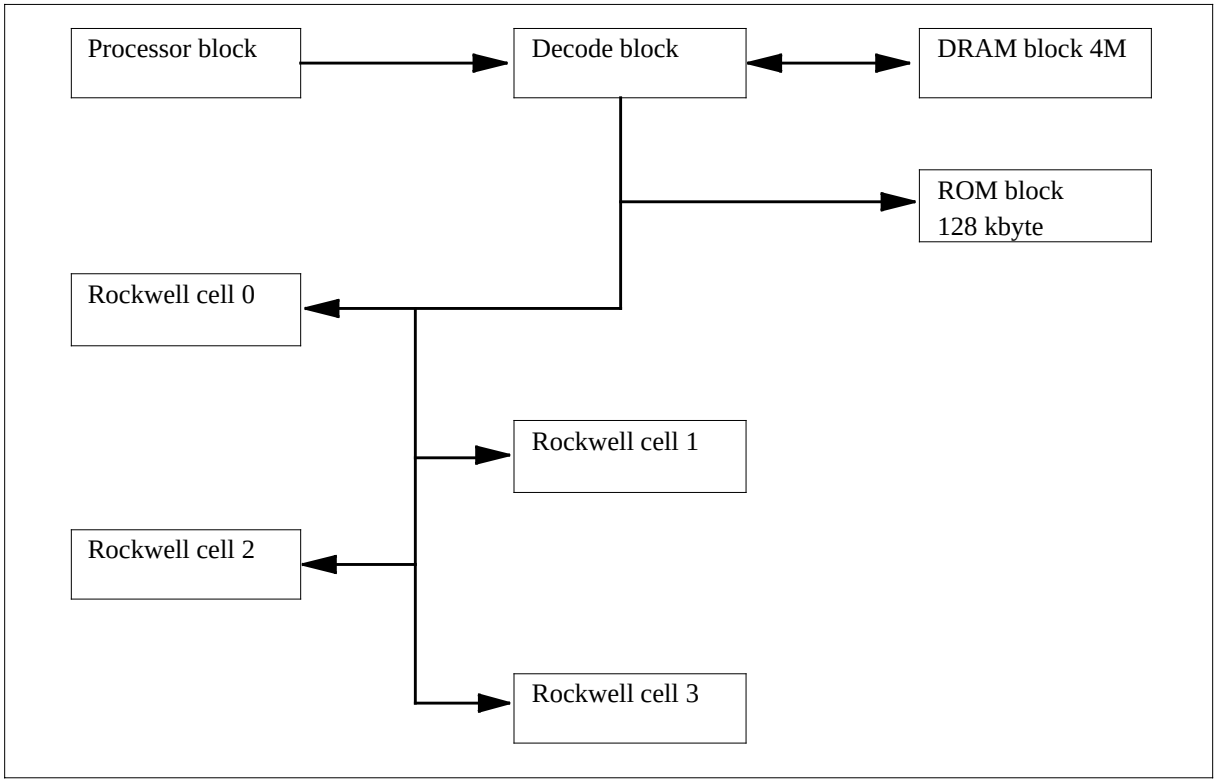
## Functional blocks

The NTBX02BA has the following functional blocks:

- central processing unit (CPU)
- dynamic random-access memory (DRAM)
- erasable programmable read-only memory (EPROM)
- sanity timer
- bus response timer
- programmable timers
- interrupts
- paddle board extension
- the R8071 cells
- a DS60 interface

The following figure shows the relationship between the blocks.

**NTBX02BA functional blocks**



## NTBX02BA (continued)

### CPU

The CPU operates at a frequency of 20 MHz. The processor has a 32-bit data bus. The CPU supports both 8-bit and 16-bit ports.

When power-on occurs, the system initializes the D-channel handler (DCH) main blocks to a known state. A power-on reset affects the CPU, all state machines, and the programmable timers. A power-on reset disables the sanity timer.

### DRAM

The program and data space for the processor has 4 Mbyte of dynamic RAM (DRAM). The system provides an expansion block. The total available RAM space is 16 Mbyte.

The NTBX02BA write-protects the on-board DRAM in 1 kbyte blocks.

A parity bit protects each byte of memory.

### EPROM

Combined EPROM capacity is 1 Mbyte. The on-board EPROM is a 128 kbyte by 8-bit block. This block is an 8-bit port to the CPU.

### Sanity timer

The sanity timer is a two-stage circuit that checks the CPU.

### Bus response timer

The bus response timer monitors the bus response during bus access. The timer makes sure that the bus remains active when the addressed agent does not respond.

### Programmable timers

Two programmable timers are available on the DCH:

- a scheduling timer that is a time base for scheduling tasks
- a general timer for event and periodic counting

### Paddle board extension

A paddle board extension provides communication with an external paddle board (PB) that connects to the LTCI backplane.

### R8071 cells

The DCH contains four RT8071 cells. Each cell has one R8071 chip. Each chip has a buffer memory and support hardware.

Each R8071 cell has the following parts:

- an R8071 multichannel HDLC chip
- static buffer memory of 64 kbytes organized for 8-bit access
- a 1 kbyte by 9 bit buffer
- bus arbitration state machine
- four status bits

### DS60 interface

The DS60 interface performs the following functions:

- reception of data from the odd-numbered port only. The DS60 drives both ports
- exchange of data with the active unit only
- an inactive unit loopback. The data back from the inactive unit uses the inactive clock and frame pulse to loop back
- rate conversions in both directions between 2.048 MHz and 2.56 MHz

### Interrupts

The NTBX02BA has seven interrupts. The seven interrupts are listed below in descending order of priority:

1. The sanity timer generates the sanity timeout interrupt when the sanity program does not receive service.
2. The system generates memory parity error interrupt when the system detects a parity error during a read cycle to the program space.
3. The system does not use this interrupt.
4. The general purpose timer generates the general purpose timeout interrupt.
5. The scheduling timer generates the clock tick interrupt. The system uses the timer as a time base for the operating system scheduling.
6. The PB serial ports interrupt can generate from status and control ports, host data port, and terminal data port.
7. The peripheral I/O interrupt consists of eight interrupts. Three interrupts are used. The system reserves a peripheral interrupt register for these interrupts. When the processor acknowledges a level-1 interrupt, a poll of

## **NTBX02BA** (continued)

this register indicates the source of the interrupt. The system uses the following interrupts:

- switch of activity (SWACT) detect
- frame pulse loss
- an R8071 interrupt

The state-of-the-activity lead on the backplane can change. The system generates SWACT detect interrupt. This interrupt notifies the software that a SWACT occurred. Expect data errors for one frame time.

The system can miss a frame pulse. The system generates frame-pulse-loss interrupt to notify the software. The software sends an acknowledgement to clear the register. The software continues to process information. The handler routines determine how the software processes information.

Any of the four R8071 cells can write information to the cell buffer. The R8071 interrupt notifies the software of the traffic to process.

# Technical data

### Power requirements

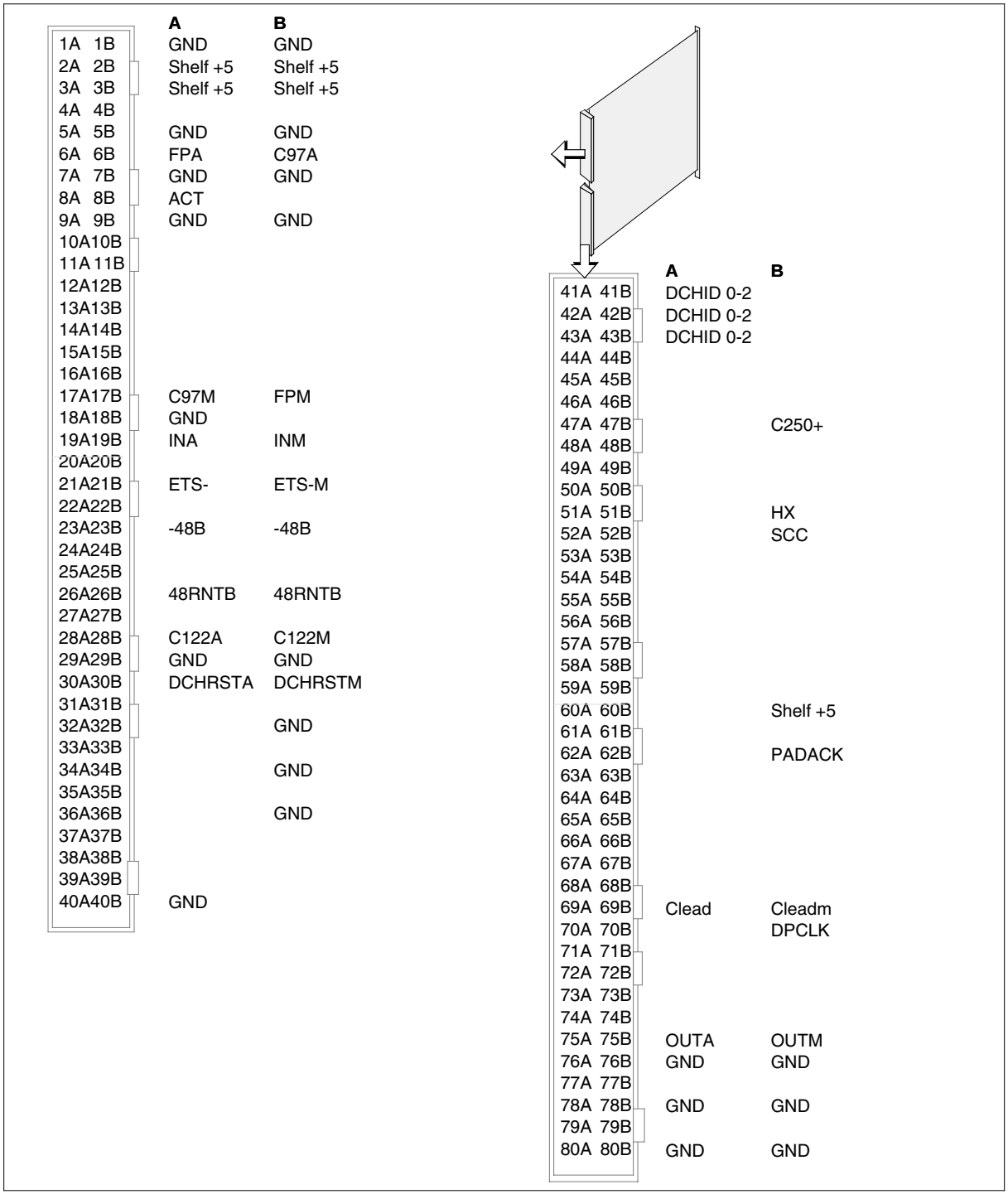
The NTBX02BA has a power converter, which converts the -48V battery output to the +5V supply that the card requires.

# Signaling

### Pin numbers

The pin numbers for the NTBX02BA appear in the following figure.

### NTBX02BA pin numbers



# NTBX25AB

## Product description

The NTBX25AB ISDN U-line card is a component that facilitates ISDN basic access to the subscriber. This card interfaces the the loop of the two-wire subscriber to the DMS/SL-100 switch.

### Location

The NTBX25AB occupies two slots in the line card drawer of the ISDN line concentrating module (ISLM).

## Functional description

### Functional blocks

The NTBX25AB contains the following functional blocks:

- line-bus (L-bus) interface subsystem
- U-interface subsystem

### L-bus interface subsystem

The L-bus interface subsystem connects to the bus interface card (BIC) in the line drawer. This subsystem contains the R34 large scale integration chip (LSI chip).

The L-bus interface subsystem provides the following features:

- interface to the X24 scan chips on the BIC
- inter-chip digital link (IDL) signals to the U-interface subsystem
- power-up reset input and reset output
- test access and cutoff relay control signals
- status inputs that the network can poll
- control outputs that the network can set

### U-interface subsystem

The U-interface subsystem accesses the IDL signals that the L-bus interface system provides. The U-interface subsystem interfaces to the two-wire subscriber loop. This subsystem contains a discreet analog front end, the X95 LSI chip, and the following thick film: NT5L04, NTL18CC, and NTL19CC.

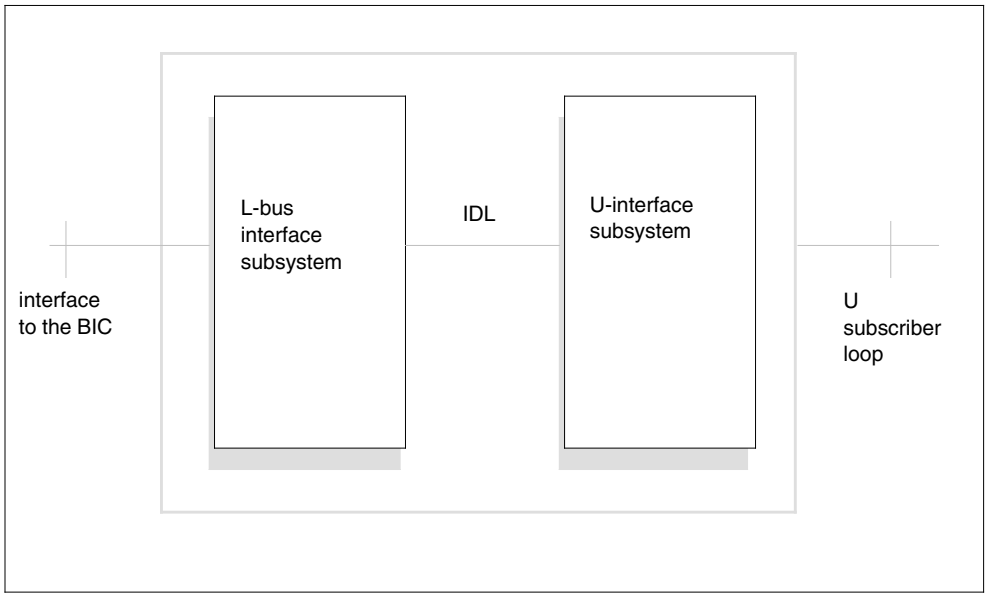
The U-interface subsystem provides the following features:

- sourcing of sealing current
- transmission line termination
- overvoltage protection

- loop isolation through the cutoff relay
- loop access through the test access bus
- two-wire to four-wire conversion through a hybrid transformer and a balance network
- alternate mark inversion (AMI) encoding and decoding
- local echo cancellation
- automatic equalization for line characteristics
- frame synchronization and clock recovery
- loop performance monitoring
- scrambling/descrambling of the transmit/receive data streams
- full-frame analog loopback at the subscriber loop terminals
- generation of reset signal

The relationship of the functional blocks appears in the following figure.

**NTBX25AB functional blocks**



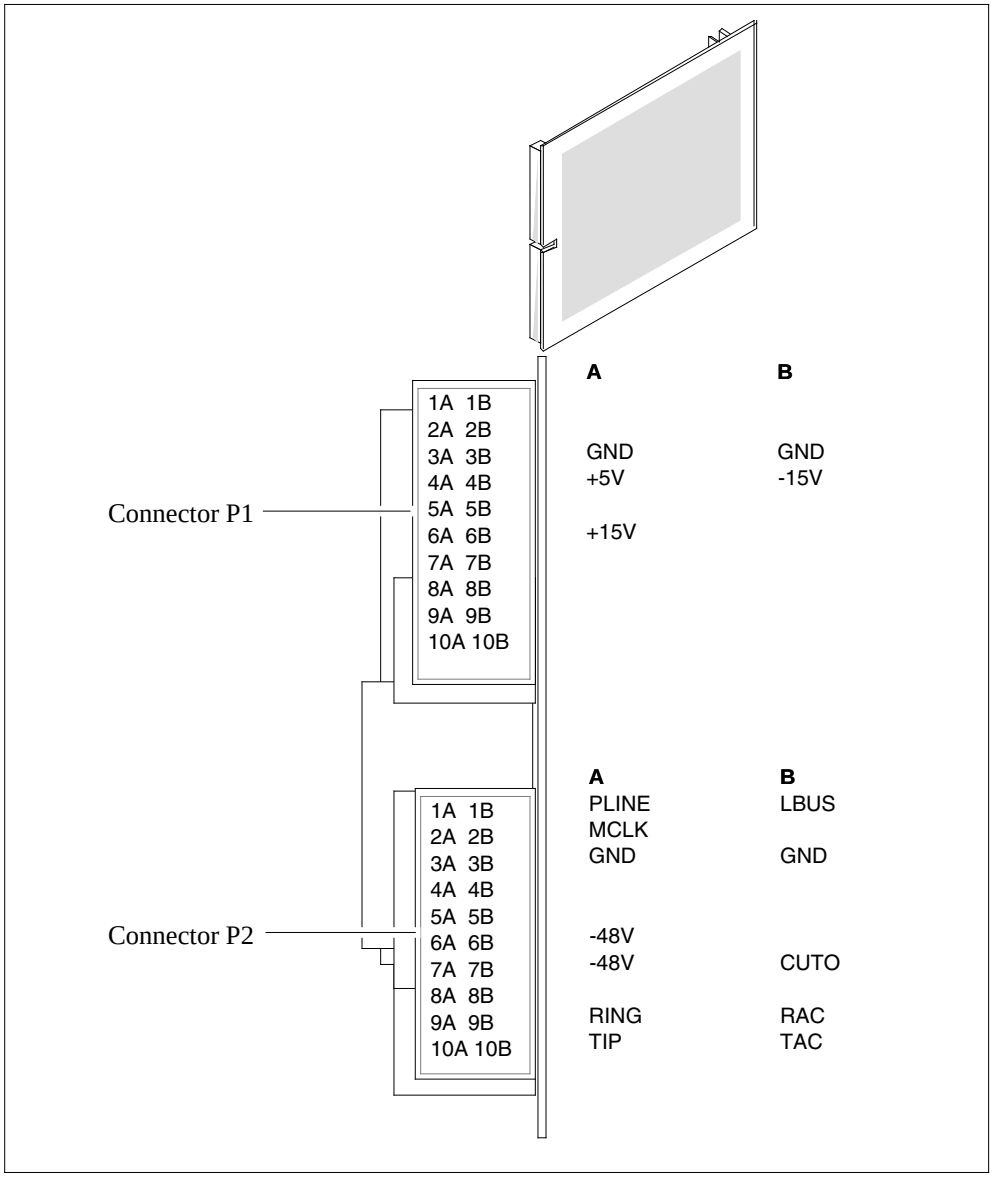

## Signaling

### Pin number

The pin numbers for the NTBX25AB appear in the following figure.

# **NTBX25AB** (continued)

**NTBX25AB pin numbers**



# Technical data

## Power requirements

The power requirements of the NTBX25AB appear in the following table.

**NTBX25AB power requirements**

| Parameter | Power supply 1 | Power supply 2 | Power supply 3 |
|---|---|---|---|
| Supply voltage | +5V | +15V | -15V |
| Supply current | 40 mA | 85 mA | 85 mA |

# NTBX26AA

## Product description

The ISDN S/T line card (S/T-ISLC) applies in the DMS-100 and Meridian SL-100 (MSL-100) systems. Applications of the S/T-ISLC are limited to ISDN remotes and customer premise equipment. The first delivery vehicle of the ISDN S/T line card is the ISDN line concentrating module (LCMI). The ISDN S/T line card can be of an MSL-100 private branch exchange (PBX) or a DMS-100 ISDN remote switching center (RSCI).

### Location

The S/T-ISLC inserts in a standard LCMI-type line drawer. The S/T-ISLC interfaces to the bus interface card (BIC) through the local bus (L-bus) in the line drawer. The S/T-ISLC interfaces the terminal equipment through the 4-wire S/T-bus.

## Functional description

The S/T-ISLC provides the DMS-100/MSL-100 access vehicle with an ISDN basic rate access (2B+D) network interface. An S/T-ISLC provides a S/T-bus interface. The switch functions as a network termination 2 (NT2).

### ISDN S/T standard features

A list of ISDN S/T standard features follows:

- compatible with I.430 (S/T-bus)
- supports all I.430 compatible terminals
- supports point-to-point and multipoint bus configurations
- provides enough power (2.5W) through the phantom power method to supply two I.430 terminals
- loop range a maximum of 6 dB
- supports Q/S-channel maintenance that the customer initiates
- activates S/T-bus according to Active Only NorTel procedures
- provides analog loopback at the S/T-bus
- provides protection against outside plant overvoltages on the S/T-bus

### DMS/MSL-100 maintenance features

A list of DMS/MSL-100 maintenance features follows:

- ISDN and plain ordinary telephone service (POTS) messages transfer maintenance and control information between the LCMI processor and the line card
- Full (2B+D) analog loopback toward the switch

- loop cutoff relay with cutover hold circuits
- separate B-channel loopbacks (transparent or not transparent) to the switch or the customer
- monitoring capability of customer-initiated maintenance
- error monitoring capability of errored frames the S/T bus sends
- software-initiated hardware reset
- monitoring capability of phantom powering source

### Hardware parts/features

A list of hardware parts and features follows:

- Motorola MC145475 S/T-bus transceiver (28-pin dual inline package (DIP))
- Motorola 68HC05 single chip microcontroller (40-pin DIP)
- R34 L-bus interface chip (28-pin DIP)
- overvoltage protection circuits
- terminal (phantom) power with short-circuit protection
- loop isolation transformers
- S/T-bus 100 Ω terminating resistors
- loopback/cutoff relay
- 90 mm by 150 mm standard 2-slot DMS line card

### Functional blocks

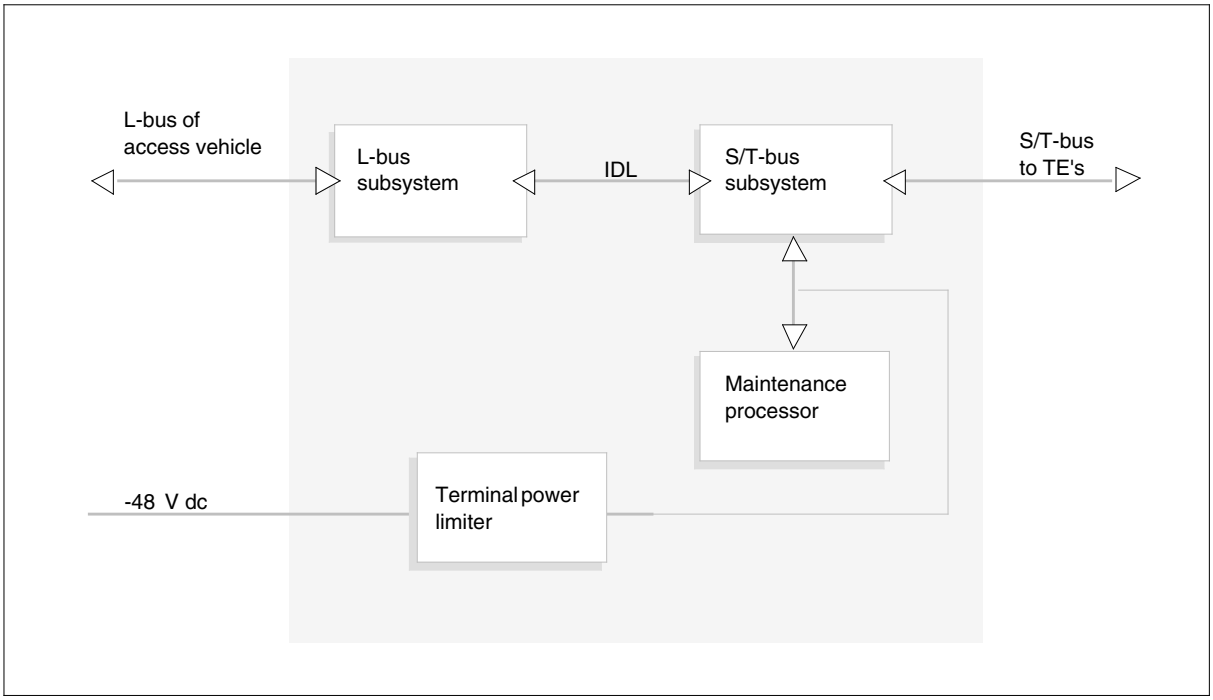
The NTBX26AA contains the following functional blocks:

- L-bus subsystem
- S/T-bus subsystem
- maintenance processor subsystem
- terminal power limiter subsystem

The functional relationship of the blocks appear in the following figure.

## NTBX26AA (continued)

**NTBX26AA functional blocks**




### Local-bus subsystem

The interface to the L-bus uses an L-chip provides the required timing and buffering. The L-chip decodes maintenance messages received on the L-bus. The L-chip can act on the messages. The L-chip can send the messages to the S/T-bus subsystem. The L-chip sends the messages through the C-channel on the serial data link, IDL. The S/T subsystem controls the loop cutoff relay.

### S/T-bus subsystem

The interface to the S/T-bus uses an S/T transceiver chip and a discrete analog front end. The S/T transceiver chip provides required timing and buffer. The S/T transceiver chip communicates over the S/T-bus with all the terminal equipment (TE). The chip also multiplexes and demultiplexes C-channel messages in and out of the control registers of the transceiver. The IDL receives C-channel messages from the L-chip.

The discrete front end contains the following:

- transformers for coupling to the line
- a passive low-pass filter for the receive signal
- components for overvoltage protection

- a relay that provides an analog loopback and cuts off the loop
- resistors for transmission line termination

This subsystem interfaces to the terminal power. This subsystem limits the subsystem through two signals. One signal connects to the center tap on the loop side of each transformer.

### Maintenance processor subsystem

The maintenance processor uses ROM to interface the S/T transceivers internal control registers. This interface occurs through the serial control port of the maintenance processor. The processor uses 3.84 MHz as the clock source. Divide the oscillator output of the S/T transceiver chip by two to obtain the value of the clock source. Programmable I/O pins are for any discrete signal control or monitoring.

### Terminal power limiter subsystem

The terminal power limiter subsystem uses discrete components to limit the current to the loop. This action protects the power supply of the switch from short circuits. The terminal power limiter subsystem interfaces to the line drawer through the -48V and -48VR pins. The terminal power limiter subsystem also interfaces to the S/T-bus subsystem. The terminal power limiter subsystem connects the positive terminal, -48VR, to the center tap of the receive transformer. The subsystem also connects the negative terminal that limits currents to the center tap of the transmit transformer.

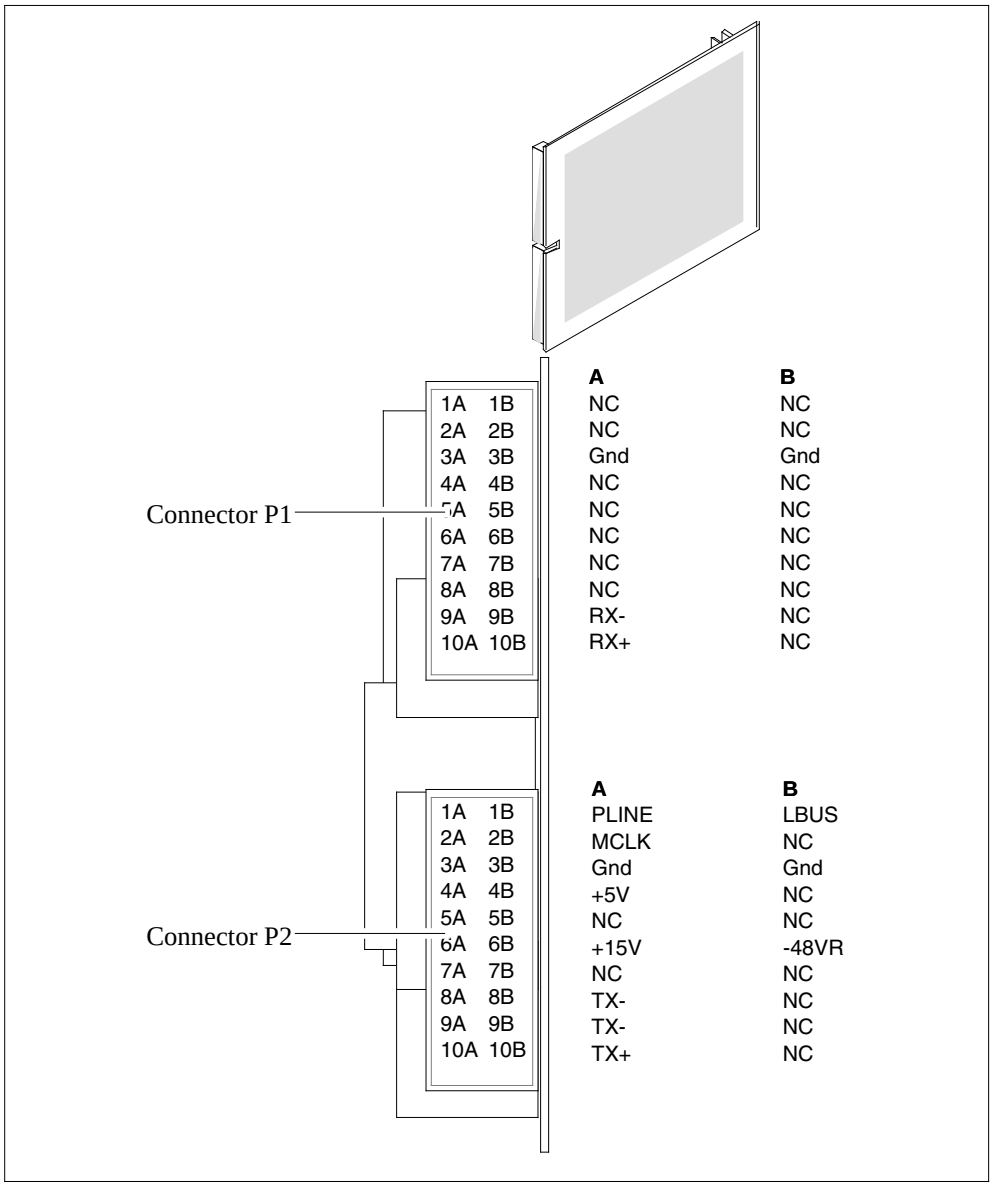
## Signaling

### Pin numbers

The pin numbers for NTBX26AA appear in the following figure.

## **NTBX26AA** (continued)

**NTBX26AA pin numbers**



# Technical data

## Electrical requirements

The connector pin drive or load requirements appear in the following table.

**Connector pin drive and load requirements**

| Group | Signal name | Drive or load requirement |
|---|---|---|
| Power | +5V | 35 mA dc |
| | +15V | 35 mA dc |
| | Gnd | N/A |
| | -48V | 70 mA dc |
| | -48VR | N/A |
| L-bus | L-Bus | Must be able to drive standard TTL load |
| | MCLK | |
| | PLINE | |
| S/T interface | TX+ | Transmit pair must be terminated to 100 ohms and. Drive the receive pair with signal |
| | TX- | |
| | RX+ | |
| | RX- | |

## Power requirements

The power requirements and thermal distribution for the S/T-ISLC appear in the following table.

**Power requirements and thermal distribution dissipation (Sheet 1 of 2)**

| Item | mA at 5V | mA at 15V | mA at 48V | Power (mW) |
|---|---|---|---|---|
| S/T receiver | 15 | | | 75 |
| R34 L-chip | 5 | | | 25 |

***Note 1:*** The relay requires current at +15V when operated.

***Note 2:*** The operation of the cutoff relay and power distributed in the power limiter circuits are separate.

***Note 3:*** During a short circuit on the S/T-bus, the total power distribution on the S/T-ISLC is 4W. The power rating of the drawer is over the limit. The rating is over the limit if all lines in the same line card drawer short at the same time. This event occurs on a rare basis.

## NTBX26AA (end)

**Power requirements and thermal distribution dissipation (Sheet 2 of 2)**

| Item | mA at 5V | mA at 15V | mA at 48V | Power (mW) |
|---|---|---|---|---|
| Microcomputer | 8 | | | 40 |
| S/T interface cut-off relay | | 35 (1) | | 525 (1) |
| Reset and glue | 6 | | | 30 |
| Power detector | 1 | | | 5 |
| Terminal | | | | 500 |
| Power limiter | | | | (2) |
| Power available at S/T interface | | | 70 (2) | |
| Total power required | 35 | 35 (1) | 70 (3) | |
| Total on-board thermal dissipation | | | | 675 (2) |

***Note 1:*** The relay requires current at +15V when operated.

***Note 2:*** The operation of the cutoff relay and power distributed in the power limiter circuits are separate.

***Note 3:*** During a short circuit on the S/T-bus, the total power distribution on the S/T-ISLC is 4W. The power rating of the drawer is over the limit. The rating is over the limit if all lines in the same line card drawer short at the same time. This event occurs on a rare basis.

# NTBX27AA

## Product description

The two-binary one-quaternary (2B1Q) U-interface ISDN line card provides the DMS-100 and MSL-100 with a subscriber interface. The interface is an ISDN basic rate access (BRA) subscriber interface. The U-interface ISDN line card (U-ISLC) subscriber interface meets the ANSI ISDN 2B1Q metallic loop (U-loop) standard specification.

### Location

The NTBX27AA can be in the ISDN line concentrating module (LCMI) high capacity line drawer. The NTBX27AA can be in the line remote unit (LRU) small remote line drawer.

## Functional description

### Functional blocks

The NTBX27AA contains the following functional blocks:

- L-bus subsystem
- U subsystem
- maintenance subsystem
- reset circuits

### L-bus subsystem

The L-bus subsystem interfaces to the line card drawer bus interface card (BIC). The L-bus subsystem provides signals that meet the inter-digital link (IDL) specification and serial control port (SCP) specifications. The R88 chip starts the L-bus subsystem.

### U subsystem

The U subsystem accesses the IDL and SCP signals. The L-bus and maintenance subsystems provide the signals. The U subsystem interfaces to the two-wire metallic U-loop.

### Maintenance subsystem

The maintenance subsystem is the master of the SCP interface between the L-bus subsystem and the U subsystem.

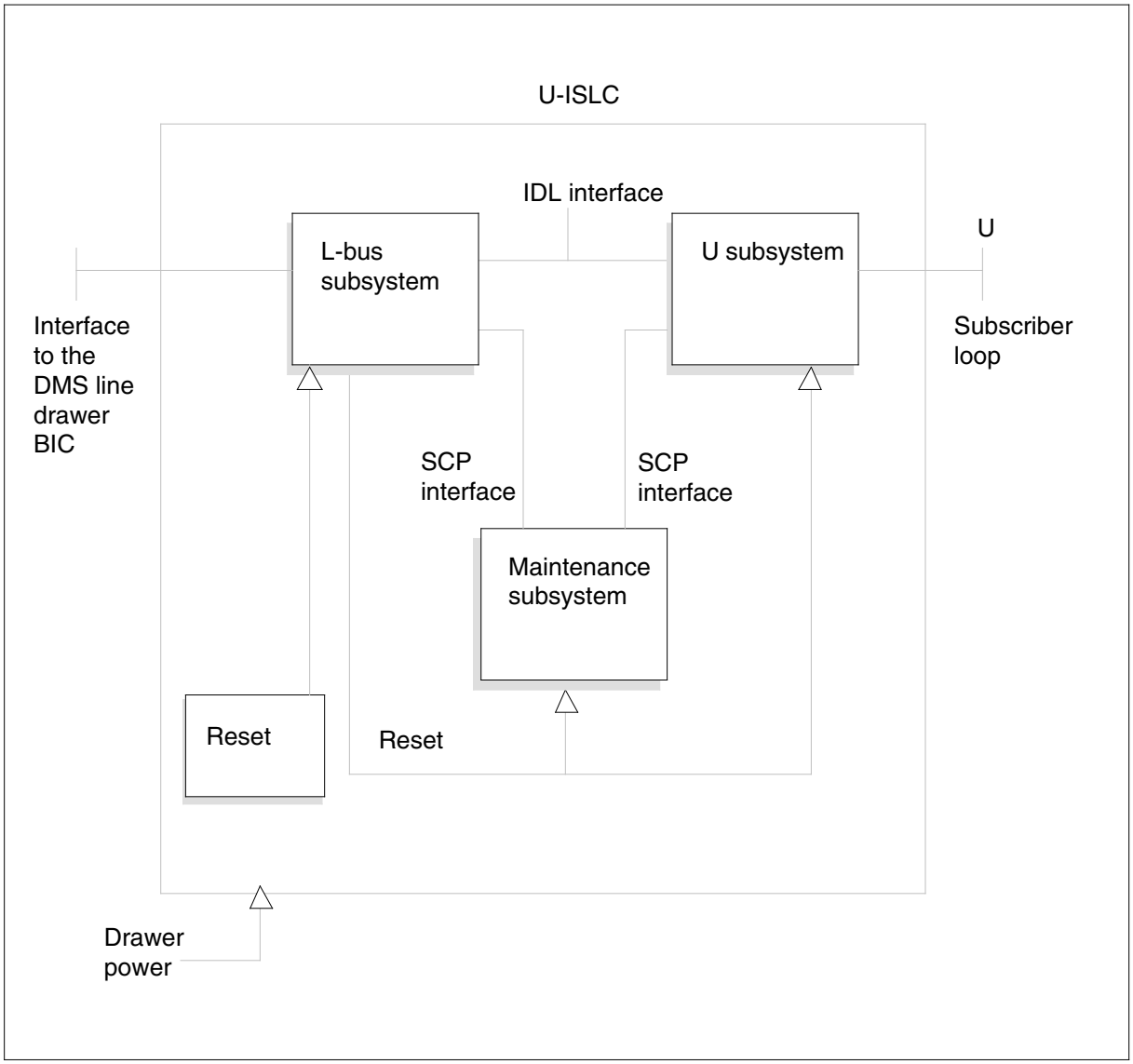
### Reset circuits

The reset circuits provides a hardware reset signal to the L-bus subsystem. The subsystem internally resets and generates a stretched reset output signal to the U subsystem and maintenance subsystem.

## NTBX27AA (continued)

The relationship between these functional blocks appears in the following figure.

**NTBX27AA functional blocks**

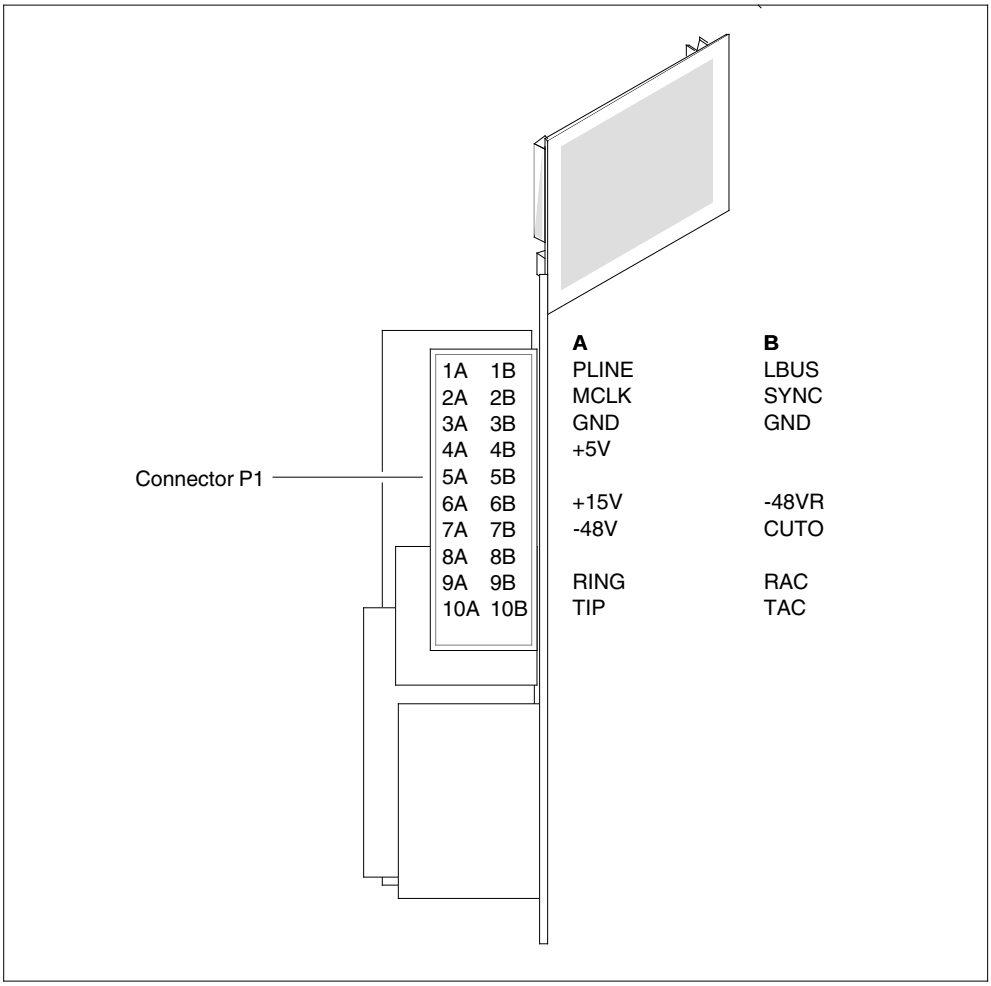



# Signaling

## Pin numbers

The pin numbers for the NTBX27AA appear in the following figure.

**NTBX27AA pin numbers**




## Technical data

### Power requirements

The NTBX27AA requires a supply voltage of +5V and +15V. The -48V talk battery supplies sealing current to the subscriber loop.

# NTBX30AB

## Product description

The ISDN line concentrating equipment (LCEI) frame has a single bay that contains one or two line concentrating modules. One module can be an ISDN line concentrating module (LCMI) or an enhanced ISDN line concentrating module (LCME). Each line concentrating module (LCM) houses eight line drawers. Each LCM contains two line concentrating arrays (LCA). Each array occupies a separate shelf in the frame.

The LCMI is for ISDN lines that use the alternate mark inversion line protocol. The LCME is for ISDN lines that use the 2B1Q line protocol.

An upgrade kit, NTBX30AB, is available to convert an LCMI to an LCME. During the upgrade, the LCMI is not in service. Replace all NTBX32AA line drawers in the LCMI with NTBX32BA line drawers.

The LCEI frame includes an NTBX63AA cooling fan and two NT6X30AA ringing generators. If analog ringing is required, use ringing generators.

## Parts

The NTBX30AB frame includes a minimum of two LCAs. Each LCA pair has eight line drawers and a common fill. Each NTBX30AB frame includes several of the following components. The correct mix reflects customer needs like the type of line protocols in use.

- an NTBX31AC—ISDN line concentrating module common fill
- an NTBX31BA—ISDN enhanced LCM common fill
- an NTBX32BA—ISDN enhanced line drawer
- an NTBX37AB—ISDN line concentrating equipment frame supervisory panel

### ISDN line concentrating module common fill

The NTBX31AC contains all cards in the LCMI. These cards are the following:

- the NT6X5BA ISDN converter 5.25V/15V
- the NT6X53EA ISDN LCMI power converter +5V/-15V
- the NTBX34AB ISDN line modular processor card
- two NTBX35AA ISDN LCM digroup control cards

### ISDN enhanced line concentrating module common fill

The NTBX31BA contains all cards in the LCME. The NTBX31BA is an enhancement in comparison to the NTBX31AC. Each NTBX31BA line drawer can contain a maximum of 12 additional line cards.

The cards in this common fill are the following:

- the NTBX72AA battery and ring router
- the NT6X53CA ISDN LCME power converter +5V/+15V card
- the NTBX34BA ISDN enhanced LCME processor card
- two NTBX35AA ISDN LCM digroup control cards

### ISDN enhanced line drawer

Each ISDN subscriber line terminates on a line card in the NTBX32BA enhanced line drawer. The NTBX32BA always contains a minimum of one line card, an NTBX36BA ISDN LCM enhanced line drawer BIC (bus interface card). The NTBX32BA always contains an NTBX71AA ISDN enhanced line drawer PUPS (point-of-use power supply) card. The ISDN enhanced line drawer houses a maximum of 60 line cards. The LCME supports many line card types. The specified group of subscriber lines determines the line card capacity.

The LCME provides flexible time division multiplexing (TDM) groups. The TDM groups allow the position of an ISDN line in any position in a drawer. Any four ISDN lines from the same drawer can belong to the same TDM group. The lines in a specified group must come from the same drawer.

### ISDN line concentrating equipment frame supervisory panel

The NTBX37AB ISDN line concentrating equipment (LCEI) FSP includes power supervisory equipment and two talk battery filters. The power supervisory equipment includes the frame fail lamp, fan fail lamp, and four frame jacks (DATA-A, DATA-B, TEL-A, and TEL-B). Other jacks provide:

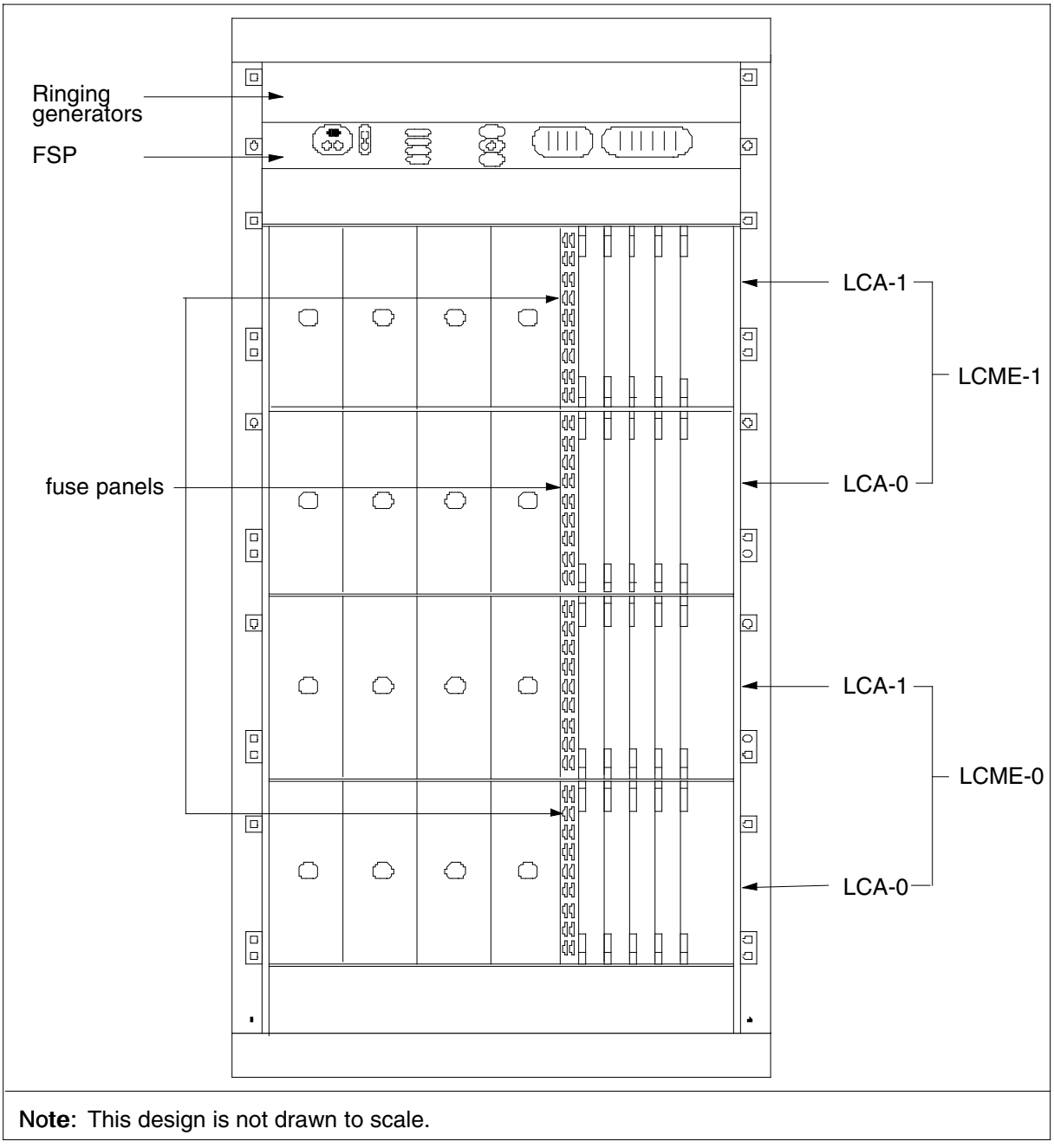
- front and rear fused access the alarm battery supply (ABS)
- two talk battery filter
- 10 circuit breakers
- four ABS fuses
- two NT6X36AA line concentrating module FSP alarm cards

## Design

The design of the ISDN line concentrating equipment (LCEI) frame appears in the next figure.

# **NTBX30AB** (end)

**LCEI frame**




**Note:** This design is not drawn to scale.

# NTBX31AA

## Product description

The NTBX31AA ISDN line concentrating module (LCMI) common fill contains all cards in the LCMI. This common fill is in each LCMI in offices with BCS27 or lower software release. A standard ISDN line concentrating equipment frame contains two LCMIs, with a cooling fan, a frame supervisory panel, and two ringing generators.

## Parts

The LCMI common fill shelf contains the following components:

- the NT6X53BA—power converter card
- the NT6X53EA—power converter card
- the NTBX34AA—ISDN LCM processor card
- the NTBX35AA—ISDN LCM digroup control card

## Design

The parts appear in the following table.

**NTBX31AA parts (Sheet 1 of 2)**

| PEC | Slot | Description |
|---|---|---|
| NT6X53BA | 25F | *Power converter card*<br>The NT6X53BA power converter card provides regulated +5V and +15V common-ground dc outputs from the nominal -48V office battery dc input. |
| NT6X53EA | 22F | *Power converter card*<br>The NT6X53EA power converter card provides +5V and -15V regulated dc outputs from the office battery -48V dc input. |

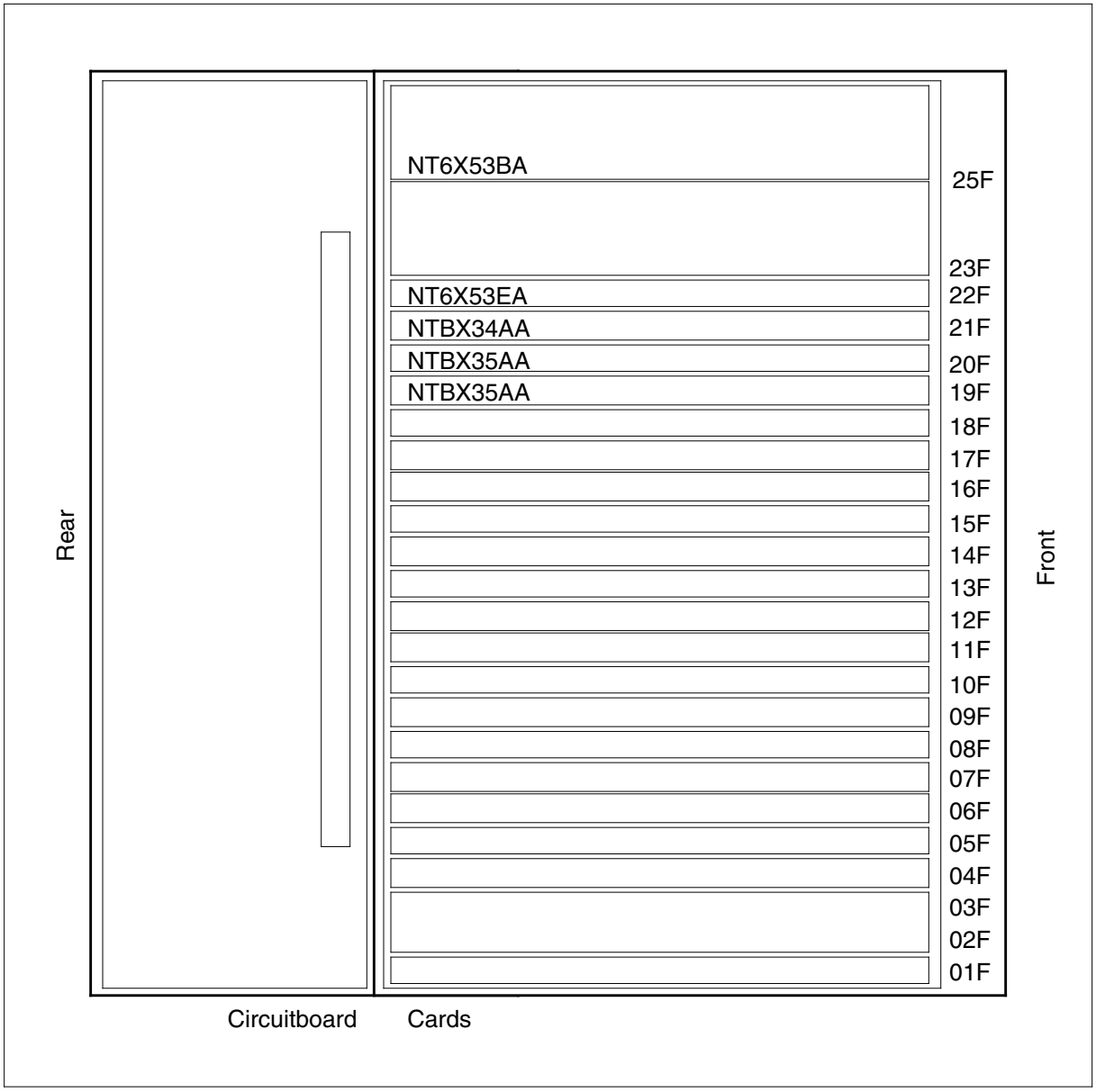
## **NTBX31AA** (continued)

**NTBX31AA parts (Sheet 2 of 2)**

| PEC | Slot | Description |
|---|---|---|
| NTBX34AA | 21F | *ISDN LCM processor card*<br><br>This card is in each ISDN LCM in offices with BCS27 or lower software release. The NTBX34AA processor card contains all the programs that control the operation of the LCMI. The processor generates control messages to and acts on control messages from the central control complex. The processor supervises the transfer of messages between the LCMI and the line trunk controller (LTC) or line group controller (LGC).<br><br>The processor connects to the bus interface card in each line drawer. This event allows exchange of line card and C-channel control, maintenance, and test messages. |
| NTBX35AA | 19F, 20F | *ISDN LCM digroup control card*<br><br>The digroup control cards allow the ISDN LCM to connect the LCM line drawers to the DS30 links. The links connect to an ISDN peripheral, like the LGC or LTC.<br><br>The digroup control cards separate B-channel and D-channel data. The cards time switch the data between a maximum of 18 DS30A ports (to the LGC or LTC) and 12 peripheral-side digroups.<br><br>The digroup control card multiplexes the 16 kbit/s D-channels in the line card-to-switch direction into 64 kbit/s channels. The digroup control card routes the channels through the DS30A links to the LGC or LTC. The digroup control card (DCC) demultiplexes the D-channels in the switch-to-line card direction.<br><br>From the DCC, the B-channels and D-channels pass through connections in the time switch of the LCMI to the LGC or LTC. The D-channels have permanent connections in the switch. The B-channel connections are assigned and removed for each call.<br><br>The DCC inserts pulse code modulation (PCM) codes in the PCM stream. With these codes, the DCC instructs a plain ordinary telephone service (POTS) line card to operate. The DCC also instructs a POTS line card to release the ringing relay of the card.<br><br>The DCC provides a clear connection between the processor card and the DS30A channel. The clear connection is the control channel between the LCMI and the LGC or LTC. The DCC applies loop-around tests to the digroup links between the DCC and the bus interface card. The DCC supports the setup of loop-arounds between D30A channels. This event allows the LGC or LTC to test the DS30A channels between the LGC or LTC and the LCMI. |

The design of the LCMI common fill shelf appears in the following figure.

**NTBX31AA parts**



# NTBX31AC

## Product description

The NTBX31AC ISDN line concentrating module common fill contains all cards always provided in the LCMI. A standard ISDN line concentrating equipment frame contains two LCMIs, a cooling fan, a frame supervisory panel and two ringing generators.

## Parts

The LCMI common fill shelf contains the following parts:

- the NT6X53BA—ISDN power converter 5.25 V/15 Vcard
- the NT6X53EA—ISDN LCM power converter +5 V/-15 V card
- the NTBX34AB—ISDN line module processor card upgrade
- the NTBX35AA—ISDN LCM digroup control card

## Design

The parts of the LCMI common fill shelf appear in the following table.

**NTBX31AC parts (Sheet 1 of 3)**

| PEC | Slot | Description |
|---|---|---|
| NT6X53BA | 25F | *ISDN power converter 5.25V/15V card*<br>The NT6X53BA power converter card provides regulated +5V and +15V common-ground dc outputs from the nominal -48V office battery dc input. |
| NT6X53EA | 22F | *ISDN LCM power converter +5V/-15V card*<br>The NT6X53EA power converter card provides 5V and 15V regulated dc outputs from the nominal -48V office battery dc input. The common-ground dc outputs are +5 and -15V. |

**NTBX31AC parts (Sheet 2 of 3)**

| PEC | Slot | Description |
|---|---|---|
| NTBX34AB | 21F | *ISDN line module processor card upgrade*<br><br>This card is part of each LCMI in offices with any application with a software release higher than BCS-27. The NTBX34AB processor card contains all the programs that control the operation of the LCMI. The processor generates control messages to the central control complex. The processor acts on control messages from the central control complex. The processor supervises the transfer of messages between the LCMI and the line trunk controller (LTC) or line group controller (LGC).<br><br>The processor connects to the bus interface card in each line drawer. This event allows exchange of line card and C-channel control, maintenance, and test messages. |

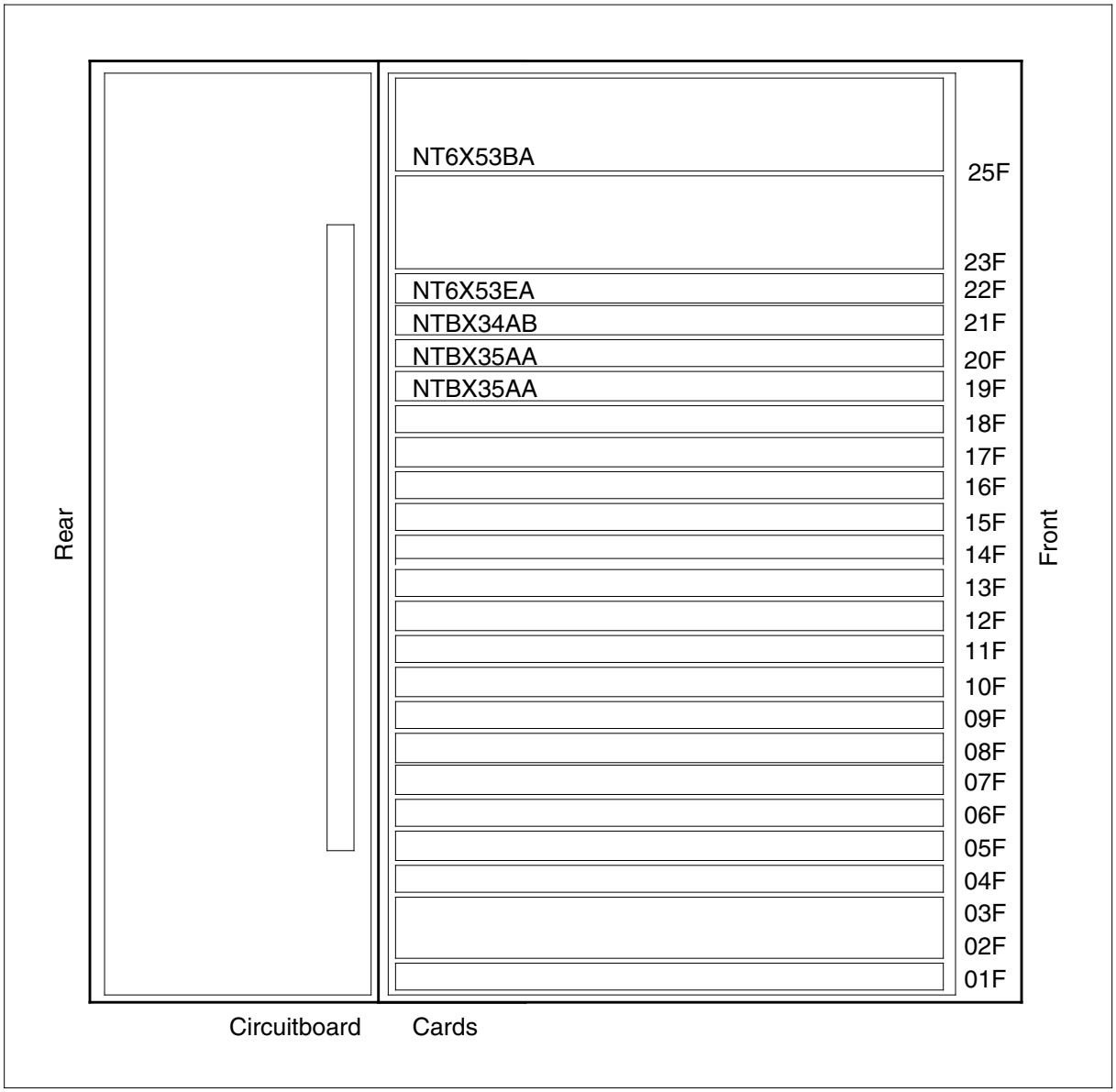
## **NTBX31AC** (continued)

**NTBX31AC parts (Sheet 3 of 3)**

| PEC | Slot | Description |
|---|---|---|
| NTBX35AA | 19F, 20F | *ISDN LCM digroup control card*<br><br>The digroup control cards (DCC) allow the LCMI to connect the line drawers of the LCMI to the DS30 links. The DS30 links connect to an ISDN peripheral like the LGC or LTC.<br><br>A digroup is a 32-channel, pulse code modulated path that allows the line drawers to communicate with the DCC. The DCCs separate B-channel and D-channel data. The DCCs timeswitch the data between a maximum of 18 DS30A ports (to the LGC or LTC) and 12 peripheral-side digroups.<br><br>The DCC multiplexes the 16 kbit/s D-channels in the line card-to-switch direction into 64 kbit/s channels. The DCC routes the channels through the DS30A links to the LGC or LTC. The DCC demultiplexes the D-channels in the switch-to-line card direction.<br><br>From the DCC, the B- and D-channels pass through connections in the time switch of the LCMI to the LGC or LTC. The D-channels have permanent connections in the switch. The B-channel connections are assigned and taken down for each call.<br><br>The DCC inserts pulse code modulation (PCM) codes into the PCM stream. The DCC uses this code to instruct a plain ordinary telephone service (POTS) line card. The DCC can instruct POTS to operate or release the ringing relay of the POTS line card.<br><br>The DCC provides a clear connection between the processor card and the DS30A channel. This channel is the control channel between the LCMI and the LGC or LTC. The DCC applies looparound tests to the digroup links between the DCC and the bus interface card. The DCC supports the setup of looparounds between DS30A channels. The setup of looparounds allows the LGC or LTC to test the DS30A channels between the LGC or LTC and the LCMI. |

The design of the LCMI common fill shelf appears in the following figure.

**NTBX31AC parts**



# NTBX31BA

## Product description

The NTBX31BA ISDN enhanced line concentrating module common fill contains all cards always provided in the LCME. A standard ISDN enhanced line concentrating equipment frame contains the following:

- two LCMEs
- a cooling fan
- a frame supervisory panel
- two ringing generators

This common fill is part of each LCME in offices with a BCS31 or higher software release.

The NTBX31BA is enhanced because the NTBX31BA line concentrating module accommodates a maximum of 480 line cards in eight line drawers. The NTBX31AA accommodates a maximum of 384 line cards.

## Parts

The ISDN enhanced line concentrating module common fill contains the following parts:

- the NT6X53CA—ISDN LCME power converter +5V/+15V card
- the NTBX34BA—ISDN enhanced LCME processor card
- the NTBX35AA—ISDN LCM digroup control card
- the NTBX72AA—ISDN LCME battery and ringing router card

## Design

The parts and design of the LCME common fill appears in the following table and figure.

**NTBX31BA parts (Sheet 1 of 2)**

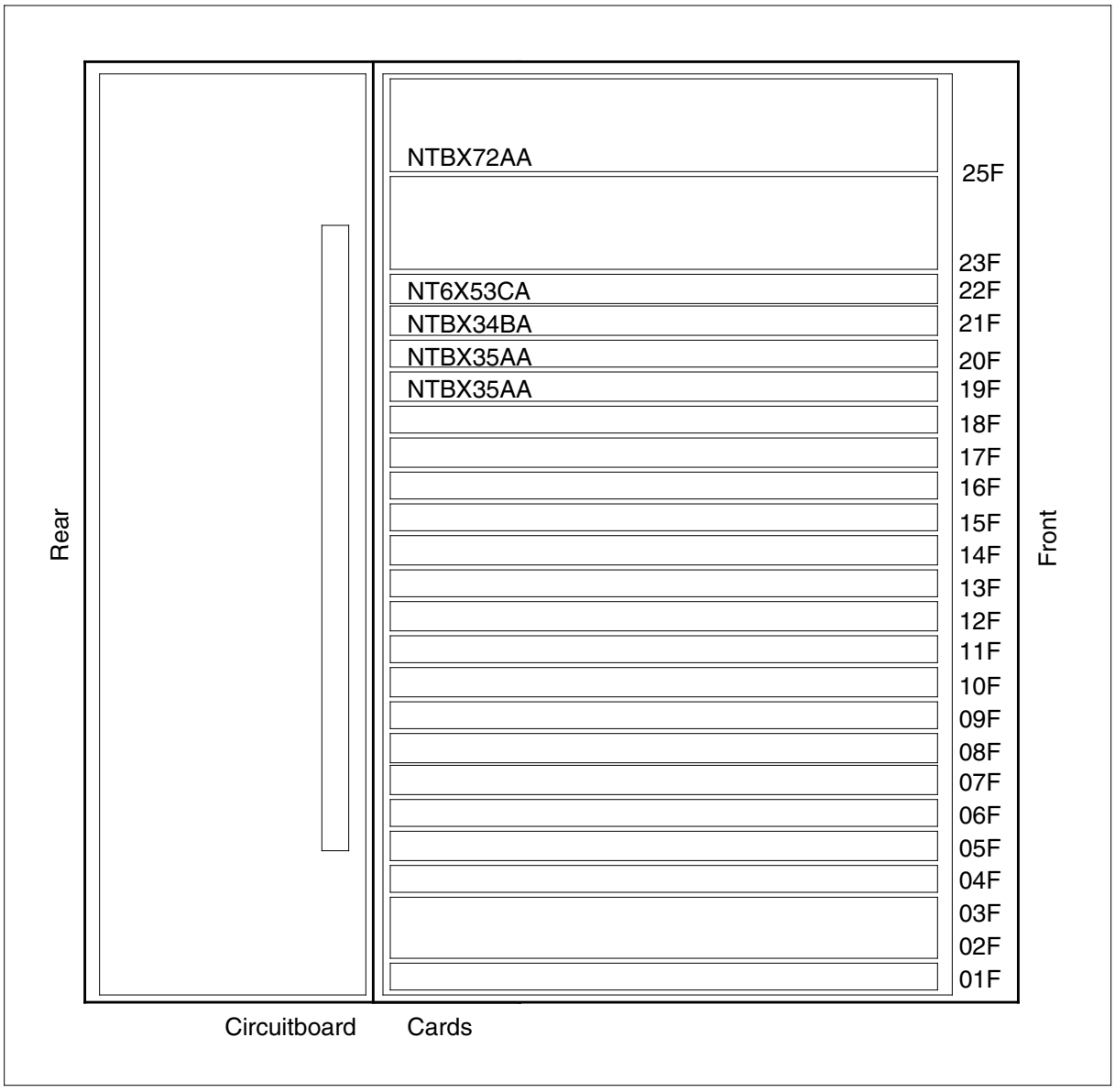
| PEC | Slot | Description |
|---|---|---|
| NT6X53CA | 22F | *ISDN LCME power converter +5V/+15V card*<br>The power converter supplies dc voltages of +5V for the shelf common control cards and +15V for the line drawers. |
| NTBX34BA | 21F | *ISDN enhanced LCME processor card*<br>The processor card contains all the programs that control the operation of the LCME. The processor generates control messages to the central control complex. The processor acts on control messages from the central control complex. The processor supervises the transfer of messages between the LCME and the line trunk controller (LTC) or line group controller (LGC). The processor connects to the bus interface card in each line drawer. The connection allows exchange of line card and M–channel control, maintenance, and test messages. |

## **NTBX31BA** (continued)

**NTBX31BA parts (Sheet 2 of 2)**

| PEC | Slot | Description |
|---|---|---|
| NTBX35AA | 19F, 20F | *ISDN LCM digroup control card*<br><br>The digroup control cards allow the LCME to connect the line drawers of the LCME to the DS30 links. The DS30 links connect to an ISDN peripheral like the LGC or LTC.<br><br>The digroup control cards separate B–channel and D–channel data. The cards time switch the data between a maximum of 18 DS30A ports (to the LGC or LTC) and 12 peripheral–side digroups.<br><br>The B– and D–channels pass from the digroup control card (DCC). The B– and D–channels pass through connections in the timeswitch of the LCME to the LGC or LTC. The D–channels have permanent connections in the switch. The B–channel connections are assigned and taken down for each call.<br><br>The DCC provides a clear connection between the processor card and the DS30A channel. The channel is the control channel between the LCME and the LGC or LTC. The DCC applies looparound tests to the digroup links between the DCC and the bus interface card. The DCC supports the setup of looparounds between DS30A channels. The setup of looparounds allows the LGC or LTC to test the DS30A channels between the LGC or LTC and the LCME. |
| NTBX72AA | 25F | *ISDN LCME battery and ringing router card*<br><br>The ISDN enhanced LCME battery and ringing router card monitors the current of ANI/COIN inputs that a multiplexer (MUX) circuit selects.<br><br>The card contains a relay network that acts like a MUX. The card contains a ring current detector that monitors the level of the current. The card also contains a +5V auxiliary switching supply that feeds the MUX logic and the ring detector. An alarm circuit indicates failure of the +5V or -48V power supply of the card. A high current Schottky rectifier functions like an isolator and power distributor for other cards. |

**NTBX31BA parts**



# NTBX32BA

## Product description

Each ISDN subscriber line stops on a line card in the line drawer of the ISDN enhanced line concentrating module (LCME). The line card transmits and receives messages and data between the ISDN line and the bus interface card (BIC).

The NTBX32BA ISDN enhanced line drawer houses a maximum of 60 line cards. A maximum of eight line drawers can be assigned to one LCME. An LCME that is fully configured can contain maximum of 240 ISDN T lines or maximum of 480 ISDN U lines. In an LCME that supports a group of line types, the group of installed lines determines the total number of lines.

## Parts

The NTBX32BA shelf contains the following parts:

- the NT6X17AA/AB/AC—Type–A world line card
- the NT6X18BA—Type–B world line card
- the NT6X19AA—Type–E standard line card
- the NT6X21AC—P-phone line card
- the NT6X71AA/AB—data line card
- the NT6X76AA—asynchronous interface line card
- the NT6X99AA—Datapath bit error rate tester (2–slot) card
- the NTBX26AA—ISDN S/T line card
- the NTBX27AA—2B1Q U–interface ISDN line card
- the NTBX36BA—ISDN LCM enhanced line drawer BIC
- the NTBX71AA—ISDN enhanced line drawer point–of–use power supply (PUPS) card

The NTBX32BA seldom contains all the different types of line cards described. Customer needs and preferences determine the type and quantity of line cards in the line drawer.

### Type–A world line card

The NT6X17AA type–A world line card operates with lines that connect to single–line analog telephone sets. The card provides an interface between a two–way analog subscriber line and one channel of the 4–wire, 32–channel, 2.56–Mbit/s data stream. The digital switch uses this data stream. The card, which includes a cutover control circuit, occupies one slot in the line drawer.

The NT6X17AB functions like the NT6X17AA. The U.S. offices require the NT6X17AB instead of the NT6X17AA.

The NT6X17AC is called an optimized line card. The NT6X17AC is like the NT6X17AA. The NT6X17AC uses higher density circuits and has a lower failure rate. The NT6X17AC is the only type–A world line card used in new manufactured products.

### Type–B world line card

The NT6X18BA type–B world line card is like the type–A line card. The type–B world line card can operate with analog pay telephone sets that need coin control . The type–B world line card can operate with analog single–, two–, and multi–party telephone sets. The type–B world line card occupies a single slot in the line drawer. The type–B world line provides a voice and signaling interface. The interface is between two–way analog subscriber lines and the 4–wire, 32–channel, 2.56 Mbit/s digital stream used by the switching system.

### Type–E standard line card

The NT6X19AA type–E standard line card contains circuits to flash the neon lamp in a message–waiting telephone set. This line card also provides features like line card type A features. The NT6X19AA provides a single–parity or two–party interface. The interface is between a 2–wire analog line of the subscriber and one channel of the 4–wire, 32–channel, 2.56 Mbit/s stream. The switching system uses this channel. The type–E standard line card works in conjunction with the NT6X20AA message waiting converter. This converter must be present.

### P–phone line card

The NT6X21AC p–phone line card provides voice and signaling interfaces. The interfaces are between 2–wire analog subscriber lines with business sets and the 4–wire, 32–channel, 2.56 Mbit/s digital bit stream of the switching system. Each NT6X21AC supports one business setup to three known add–on units. The voice path and the signaling path can be active at the same time.

### Data line card

The NT6X71AA or AB data line card provides an interface for lines equipped with DMS data units. The card occupies two LC slots in the line drawer. The card uses a bidirectional bus and an enable signal to transfer messages between the LCM and a data unit. Clock signals provide timing for data transmission. Clock signals also synchronize the time–compression–multiplexing (TCM) frames for all the data lines in the line drawer.

## NTBX32BA (continued)

### Asynchronous interface line card

The NT6X76AA asynchronous interface line card interconnects a 4–wire, RS–422 line and one channel of the 32–channel, 2.56 Mbit/s digital bit stream of the SL–100 PABX. The NT6X76AA card occupies two slots in the line drawer.

### Datapath bit error rate tester (2–slot) card

The NT6X99AA Datapath bit error rate tester line card generates and applies bit error rate tests to a Datapath data transmission link. This line card generates a 511–bit test pattern described in CCITT Recommendation V52. This test pattern is looped back to the tester line card from selected points in the data link. Outgoing and incoming test patterns are compared and errors are detected. Test registers store error statistics. These statistics are available for transmission to the maintenance system. Commands to initiate transmission of error statistics come from the line concentrating module. The NT6X99AA card checks the performance of any asynchronous interface that are part of any asynchronous interface. The parts include the line card, data line card, and data unit that are part of the Datapath link under test.

### ISDN S/T line card

The name of this line card follows a CCITT naming standard. The S/T–bus is the name CCITT assigns to the loop that connects customer terminals in an ISDN network. The S/T–bus is also known as the S/T–interface and S/T–loop and T–bus (for transaction bus).

The NTBX26AA ISDN T–line card stops and exchanges data between the L–bus. The L–bus connects the line card to the bus interface card. The NTBX26AA also exchanges data between the line card and the T–line bus.

***Note:*** More than eight T–line cards can be present in the same row as type–A line card. When this event occurs, the type–A line cards will **NOT** stay in service if the point–of–use power supply fails.

### 2BIQ U–interface ISDN line card

The NTBX27AA line card stops and exchanges data between the L–bus and the U loop. The L–bus connects the line card to the bus interface card. The U loop connects the line card and the 2B1Q network termination 1. This line card also provides registers, looparound points, and metallic test access points for maintenance activities.

The NTBX27AA contains an on–board maintenance processor. The functions of the processor include the following:

- message transaction processing
- U–subsystem maintenance
- interface control for the serial port
- line card self diagnostics

### ISDN LCM enhanced line drawer BIC

Each enhanced line drawer has a bus interface controller circuit card. The bus interface controller performs the following functions:

- provides connections between the line cards and the three digroups
- is a message transceiver between the LCME processor and the line cards and performs commands the LCME processor sends through the serial communications link
- scans line cards to detect a change in supervision bits
- receives control messages from the digroup control cards and passes on control messages from the digroup control cards to the line cards
- splits the M–channel off each ISDN line and stops the channel
- time switches the two B–channels and the D–channel between the digroup control card and the line card
- multiplexes four ISDN line card 16 kbit/s D–channel data streams. The direction of the dtat stream is from the line card to the LCME processor to one 64 kbit/s digroup channel. In the opposite direction, the line drawer demultiplexes the digroup channel into four D–channel data streams.
- monitors the status of the point–of–use power supply

A bus interface controller contains one scan chip. The scan chip supports both logical drawers. The scan chip passes maintenance and control messages between the LCME controller and the ISDN line card.

### ISDN enhanced line drawer PUPS card

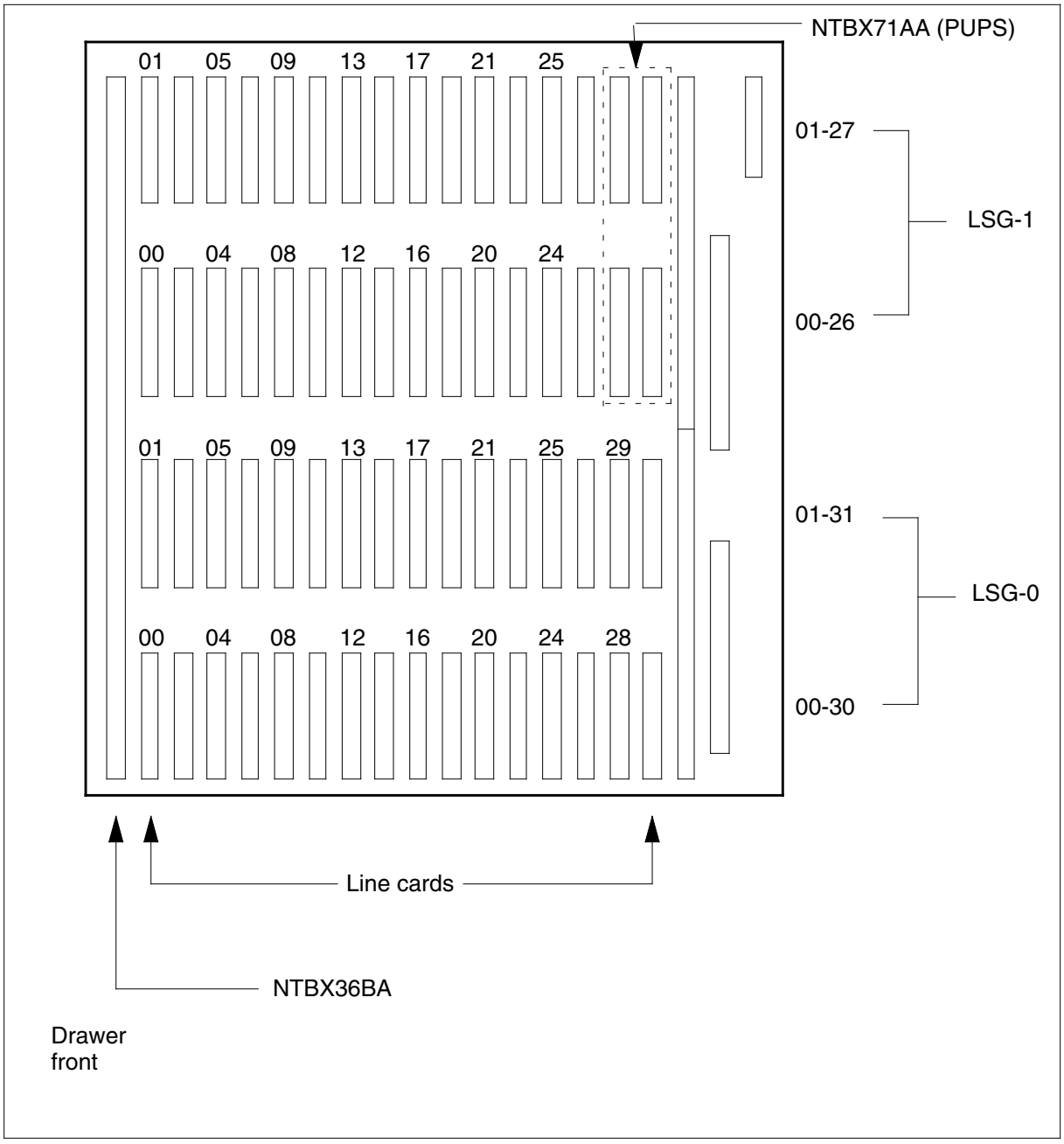
One NTBX71AA power supply is in each line drawer. This point–of–use power supply converts -48V dc input and provides +5V dc output to the line card slots.

## Design

The design of the NTBX32BA ISDN enhanced line drawer appears in the following figure.

# **NTBX32BA** (end)

**NTBX32BA parts**



## Product description

The ISDN line control module (LCMI) processor acts as an interface between the ISDN extended multiprocessor system (XMS)–based peripheral modules (XPM) and the line drawers. The NTBX34AA circuit card is responsible for the processing associated with

- scanning line cards with calls
- the set up call connections through the Digroup controller card (DCC)
- the care of DMS–X messages

The LCMI processor carries out background tasks for diagnostic purposes to make sure of the LCMI integrity.

## Functional description

### Functional blocks

The NTBX34AA contains the following functional blocks:

- CPU interface
- control and timing
- a 19.2 kbaud link to the mate processor
- message interface

### CPU interface

The CPU is an 8085 microprocessor. The system buffers the address and data buses of the CPU before distribution on the board. The system buffers the buses again before the buses go to the backplane.

The NTBX34AA has 8 kbytes of erasable programmable read only memory (EPROM). The NTBX34AA powers up with the 8 kbytes assigned to the EPROM. The system cannot read the RAM when selection of the EPROM occurs.

The NTBX34AA has 64 kbytes of dynamic memory.

### Control and timing

Two control signals control the CPU transactions. The system issues a read signal when the processor requests data from memory or a register. The system issues a write signal when the processor sends data to memory or to a register.

## **NTBX34AA** (end)

Ringing generators provide ringing control. Each generator provides the following:

- ac signals for ringing
- different dc voltage levels for automatic number identification (ANI)
- different dc voltage levels for pay telephones

The CPU uses four interrupts for timing purposes and error detection. The CPU uses four timers to schedule events or detect faults.

### 19.2 kbaud link

The serial data link for communication between processors uses an 8251 programmable universal synchronous/asynchronous receiver/transmitter (USART). The link shares the interrupt with the ringing zero crossover signal, the mate activity and the DCCFAIL pins. An interrupt generates on a byte transmit or receive. The microprocessor polls the state register to determine the cause of the interrupt.

### Message interface

The message interface provides processor access to the drawers through a serial data link. The serial data link has four parallel-to-serial and serial-to-parallel shift registers.

# NTBX34AB

## Product description

The ISDN line control module (LCMI) processor acts as an interface between the ISDN extended multiprocessor system (XMS)–based peripheral modules (XPM) and the line drawers. This processor associates with the following

- scanning line cards with calls
- setting up call connections through the Digroup controller card (DCC)
- DMS–X messages

The LCMI processor carries out background tasks for diagnostic purposes to make sure of the LCMI integrity.

The NTBX34AB is an upgraded version of NTBX34AA.

## Functional description

### Functional blocks

The NTBX34AB contains the following functional blocks:

- CPU interface
- control and timing
- a 19.2 Kbaud link to the mate processor
- message interface

### CPU interface

The CPU is an 8085 microprocessor. The system buffers the address and data buses of the CPU before distribution on the board. The system buffers the buses again before the buses go to the backplane.

The erasable, programmable read only memory (EPROM) of the NTBX34AB has 16 kbytes of memory. The NTBX34AA has 8 kbytes. The NTBX34AB powers up with the lower 8 kbytes assigned to the EPROM. The NTBX34AB also powers up with the upper 8 kbytes assigned to RAM. To assign 16 kbytes to EPROM, the software must set the BIGPROM bit in the BANK register. The NTBX34AB allows writes to RAM in the lower 8 kbytes or 16 kbytes when selection of the EPROM occurs. The system cannot read the RAM when selection of the EPROM occurs.

## **NTBX34AB** (end)

The NTBX34AB has 256 kbytes of dynamic memory. The card uses a bank switching scheme to map four 64–kbyte banks in to the 8085 64–kbyte address limit. The bank switching mechanism has the following functions:

- to expand the address range of the processor from 64 kbyte 256 kbyte
- to separate data memory from program memory

The NTBX34AB contains a common bank. This bank allows a common area of program store to be accessible from all code banks.

### Control and timing

Two main control signals control CPU transactions. The system issues a read signal when the processor requests data from memory or a register. The system issues a write signal when the processor sends data to memory or to a register.

Ringing generators provide ringing control. Each generator provides the following:

- ac signals for ringing
- different dc voltage levels for automatic number identification (ANI)
- different dc voltage levels for pay telephones

The CPU uses four interrupts for timing purposes and error detection. The CPU uses four timers to schedule events or detect faults.

### 19.2 Kbaud link

The serial data link for communication between processors uses an 8251 programmable universal synchronous/asynchronous receiver/transmitter (USART). The link shares the interrupt with the ringing zero crossover signal, the mate activity and the DCCFAIL pins. An interrupt generates on a byte transmit or receive. The microprocessor polls the state register to determine the cause of the interrupt.

### Message interface

The message interface provides processor access to the drawers through a serial data link. The serial data link has four parallel–to–serial/serial–to–parallel shift registers.

# NTBX34BA

## Product description

The NTBX34BA ISDN enhanced line concentrating module (LCME) processor card is the same as the NTBX34AB. The firmware is the only difference between cards.

## Functional description

The NTBX34BA provides an interface between the ISDN extended peripheral modules (XPM) and the line drawers. This card is responsible for the processing that associates with:

- scanning the line cards for calls
- setting up call connections through the digroup controller card (DCC)
- handling DMS–X messages

The NTBX34BA also performs diagnostic background tasks to make sure of the LCME integrity.

### Functional blocks

The NTBX34BA contains the following functional blocks:

- CPU interface
- timing and control
- 19.2 kbaud link to mate processor
- message interface

### CPU interface

The CPU is an 8085 microprocessor. The system buffers the address and data buses of the CPU before the distribution to the card occurs. The system buffers the buses again before the buses go to the backplane.

The erasable, programable read only memory (EPROM) has 16 kbytes of memory. The card powers up with the lower 8 kbytes assigned to the EPROM and the upper 8 kbytes assigned to RAM. The NTBX34BA allows writes to RAM in the lower 8 kbytes. Selection of the EPROM allows writes in the full 16 kbytes and does not allow reads of the RAM.

The NTBX34BA has 256 kbytes of dynamic memory. The NTBX34BA uses a bank switching scheme to map four banks in the 64 kbyte address limit of the 8085 microprocessor. The bank switching mechanism has two functions:

- to expand the address range of the processor from 64 kbyte to 256 kbyte
- to separate data memory from program memory

## **NTBX34BA** (end)

A common bank allows code banks to access a common area of program store.

### Control and timing

Two main control signals control CPU transactions. The system issues a read signal when the processor requests data from memory or a register. The system sends a write signal when the processor sends data to memory or to a register.

Ringing generators provide ringing control. Each generator provides the following:

- ac signals for ringing
- the different dc voltage levels for automatic number identification (ANI)
- the different dc voltage levels for pay telephones

The CPU uses four interrupts for timing purposes and error detection. The CPU uses four timers to schedule events or detect faults.

### 19.2 Kbaud link to mate processor

The serial data link for communication between the processors runs at 19 200 baud. The link is a programmable 8251 USART.

### Message interface

The message interface provides the processor with access to the drawers through a serial data link. The link contains four parallel–to–serial and serial–to–parallel shift registers.

## Product description

The ISDN enhanced LCME processor (NTBX34BC) circuit card functions as an interface between the integrated services digital network (ISDN) extended peripheral modules (XPM) and the line drawers. The NTBX34BC circuit card is responsible for the processing associated with

- scanning of line cards for calls
- the set up of call connections through the digroup controller card (DCC)
- the care of DMS-X messages

The NTBX34BC circuit card performs diagnostic background tasks that guarantee the integrity of the enhanced IDSN line concentrating module (LCME). The NTBX34BC circuit card contains modifications to the clock monitoring circuitry. These modifications create sanity time-outs, caused by the loss of clock, dependent on the mate processor's clock and activity. Sanity time-outs caused by loss of clock are suppressed, if the mate processor does not have a clock source or if the mate processor is not active.

## Functional description

This section contains the functional description of the NTBX34BC circuit card.

### Functional blocks

Functional blocks of the NTBX34BC circuit card are:

- central processing unit (CPU) interface
- control and timing
- 19.2 kbaud link to mate processor
- message interface

### CPU interface

The CPU is an 8085 microprocessor. The Digital Multiplex System (DMS) buffers address and data buses of the CPU. The address and data buses are buffered before being distributed on the circuit card and before going to the backplane.

The erasable programmable read only memory (EPROM) has 16 kbytes of memory. The NTBX34BC circuit card powers up with the lower 8 kbytes assigned to the EPROM and the upper 8 kbytes assigned to random access memory (RAM). When the EPROM is selected the NTBX34BC circuit card allows write access to the RAM in the lower 8 or 16 kbytes. When the EPROM is selected, the RAM can not be read.

## **NTBX34BC** (end)

The NTBX34BC has 256 kbytes of dynamic memory. The NTBX34BC circuit card uses a bank switching design to map four 64 kbyte banks in the 64 kbyte address limit of the 8085 microprocessor. The bank switching mechanism has two functions:

- to expand the address range of the processor from 64 kbyte to 256 kbyte
- to separate data memory from program memory

A common bank allows code banks to access a common area of program store.

### Control and timing

Two control signals control every CPU transaction. The system sends a read signal when the NTBX34BC circuit card requests data from memory or from a register. The system sends a write signal when the NTBX34BC circuit card sends data to memory or to a register.

Ringing generators provide ringing control. Each ringing generator provides the ac signals for ringing. Each ringing generator also provides the different dc voltage levels for automatic number identification (ANI) and for pay phones.

The CPU uses four interrupts for timing purposes and error detection. The CPU uses four timers to schedule events or detect faults.

### 19.2 kbaud link to mate processor

The serial data link for communication between the NTBX34BC circuit cards runs at 19.2 kbaud. The link is an 8251 programmable universal synchronous/asynchronous receiver/transmitter (USART).

### Message interface

The message interface provides the processor with access to the drawers through a serial data link. The link contains four parallel-to-serial and serial-to-parallel shift registers.

# NTBX34CA

## Product description

The NTBX34CA ISDN enhanced line concentrating module (LCME) is the same as NTBX34BA and NTBX34AB, except for differences in the firmware.

## Functional description

The NTBX34CA provides an interface between the ISDN extended peripheral modules (XPM) and the line drawers. This card is responsible for the processing that associates with:

- scans of the line cards for calls
- the set up of call connections through the digroup controller card (DCC)
- care of DMS–X messages

The NTBX34CA initializes the PCM30/DS1 links to the host on power up in the Small Remote Unit (SRU). Except for this firmware function, the NTBX34CA circuit card is identical to the NTBX34AB and interchangeable with the NTBX34AB.

The NTBX34CA also performs diagnostic background tasks to guarantee the integrity of the LCME.

### Functional blocks

The NTBX34CA consists of the following functional blocks:

- CPU interface
- control and timing
- 19.2 kbaud link to mate processor
- message interface

### CPU interface

The CPU is an 8085 microprocessor. The system buffers address and data buses of the CPU. The system buffers these buses before the system distributes the buses on the card. The system also buffers these buses before the cards go to the backplane.

The EPROM has 16 kbyte of memory. The card powers up with the lower 8 kbyte assigned to the EPROM and the upper 8 kbyte assigned to RAM. The NTBX34CA allows writes to RAM in the lower 8 kbyte. When the EPROM is selected, writes are allowed in the 16 kbyte. The system cannot read the RAM, when the system selects the EPROM.

## **NTBX34CA** (end)

The NTBX34CA has 256 kbyte of dynamic memory. This card uses a bank switching scheme to map four 64 kbyte banks in the 64 kbyte address limit of the 8085 microprocessor. The bank switching mechanism has two functions:

- to expand the address range of the processor from 64 kbyte to 256 kbyte
- to separate data memory from program memory

A common bank allows code banks to access a common area of program store.

### Control and timing

Two control signals control every CPU transaction. The system sends a read signal when the processor requests data from memory or from a register. The system sends a write signal when the processor sends data to memory or to a register.

Ringing generators provide ringing control. Each ringing generator provides the ac signals for ringing. Each ringing generator also provides the different dc voltage levels for automatic number identification (ANI) and for pay phones.

The CPU uses four interrupts for timing purposes and error detection. The CPU uses four timers to schedule events or detect faults.

### 19.2 kbaud link to mate processor

The serial data link for communication between the processors runs at 19 200 baud. The link is an 8251 programmable USART.

### Message interface

The message interface provides the processor with access to the drawers through a serial data link. The link consists of four parallel–to–serial and serial–to–parallel shift registers.

# NTBX34CB

## Product description

The ISDN enhanced LCME processor (NTBX34CB) circuit card functions as an interface between the integrated services digital network (ISDN) extended peripheral modules (XPM) and the line drawers. The NTBX34CB circuit card is responsible for the processing associated with

- scanning of line cards for calls
- the set up of call connections through the digroup controller card (DCC)
- the care of DMS-X messages

The NTBX34CB circuit card performs diagnostic background tasks that guarantee the integrity of the enhanced IDSN line concentrating module (LCME). The NTBX34CB circuit card contains modifications to the clock monitoring circuitry. These modifications create sanity time-outs, caused by the loss of clock, dependent on the mate processor's clock and activity. Sanity time-outs due to loss of clock are suppressed, if the mate processor does not have a clock source or if the mate processor is not active.

The NTBX34CB circuit card is used in the Small Remote Unit (SRU). The NTBC34CB circuit card initializes pulse code modulation 30 (PCM30) and digital signal level 1 (DS-1) links to the host on power-up.

## Functional description

This section contains the functional description of the NTBX34CB circuit card.

### Functional blocks

Functional blocks of the NTBX34CB circuit card are:

- central processing unit (CPU) interface
- control and timing
- 19.2 kbaud link to mate processor
- message interface

### Central processing unit interface

The CPU is an 8085 microprocessor. The Digital Multiplex System (DMS) buffers address and data buses of the CPU. The address and data buses are buffered before being distributed on the circuit card and before going to the backplane.

The erasable programmable read only memory (EPROM) has 16 kbytes of memory. The NTBX34CB circuit card powers up with the lower 8 kbytes

## NTBX34CB (end)

assigned to the EPROM and the upper 8 kbytes assigned to random access memory (RAM). When the EPROM is selected the NTBX34CB circuit card allows write access to the RAM in the lower 8 or 16 kbytes. When the EPROM is selected, the RAM can not be read

The NTBX34CB has 256 kbytes of dynamic memory. The NTBX34CB circuit card uses a bank switching design to map four 64 kbyte banks in the 64 kbyte address limit of the 8085 microprocessor. The bank switching mechanism has two functions:

- to expand the address range of the processor from 64 kbyte to 256 kbyte
- to separate data memory from program memory

A common bank allows code banks to access a common area of program store.

### Control and timing

Two control signals control every CPU transaction. The system sends a read signal when the NTBX34CB circuit card requests data from memory or from a register. The system sends a write signal when the NTBX34CB circuit card sends data to memory or to a register.

Ringing generators provide ringing control. Each ringing generator provides the ac signals for ringing. Each ringing generator also provides the different dc voltage levels for automatic number identification (ANI) and for pay phones.

The CPU uses four interrupts for timing purposes and error detection. The CPU uses four timers to schedule events or detect faults.

### 19.2 kbaud link to mate processor

The serial data link for communication between the NTBX34CB circuit card runs at 19.2 kbaud. The link is an 8251 programmable universal synchronous/asynchronous receiver/transmitter (USART).

### Message interface

The message interface provides the processor with access to the drawers through a serial data link. The link contains four parallel-to-serial and serial-to-parallel shift registers.

## Product description

The ISDN enhanced LCME processor (NTBX34DA) circuit card functions as an interface between the integrated services digital network (ISDN) extended peripheral modules (XPM) and the line drawers. The NTBX34DA circuit card is responsible for the processing associated with

- scanning of line cards for calls
- the set up of call connections through the digroup controller card (DCC)
- the care of DMS-X messages

The NTBX34DA circuit card performs diagnostic background tasks that guarantee the integrity of the enhanced IDSN line concentrating module (LCME). The NTBX34DA circuit card contains modifications to the clock monitoring circuitry. These modifications create sanity time-outs, caused by the loss of clock, dependent on the mate processor's clock and activity. Sanity time-outs due to loss of clock are suppressed, if the mate processor does not have a clock source or if the mate processor is not active.

The NTBX34DA circuit card is used in the Small Remote Unit (SRU). The NTBC34DA circuit card initializes pulse code modulation 30 (PCM30) and digital signal level 1 (DS-1) links to the host on power-up.

## Functional description

This section contains the functional description of the NTBX34DA circuit card.

### Functional blocks

Functional blocks of the NTBX34DA circuit card are:

- central processing unit (CPU) interface
- control and timing
- 19.2 kbaud link to mate processor
- message interface

### Central processing interface

The CPU is an 8085 microprocessor. The Digital Multiplex System (DMS) buffers address and data buses of the CPU. The address and data buses are buffered before being distributed on the circuit card and before going to the backplane.

The erasable programmable read only memory (EPROM) has 16 kbytes of memory. The NTBX34DA circuit card powers up with the lower 8 kbytes

## **NTBX34DA** (end)

assigned to the EPROM and the upper 8 kbytes assigned to random access memory (RAM). When the EPROM is selected the NTBX34DA circuit card allows write access to the RAM in the lower 8 or 16 kbytes. When the EPROM is selected, the RAM can not be read.

The NTBX34DA has 256 kbytes of dynamic memory. The NTBX34DA circuit card uses a bank switching scheme to map four 64 kbyte banks in the 64 kbyte address limit of the 8085 microprocessor. The bank switching mechanism has two functions:

- to expand the address range of the processor from 64 kbyte to 256 kbyte
- to separate data memory from program memory

A common bank allows code banks to access a common area of program store.

### Control and timing

Two control signals control every CPU transaction. The system sends a read signal when the NTBX34DA circuit card requests data from memory or from a register. The system sends a write signal when the NTBX34DA circuit card sends data to memory or to a register

Ringing generators provide ringing control. Each ringing generator provides the ac signals for ringing. Each ringing generator also provides the different dc voltage levels for automatic number identification (ANI) and for pay phones.

The CPU uses four interrupts for timing purposes and error detection. The CPU uses four timers to schedule events or detect faults.

### 19.2 kbaud link to mate processor

The serial data link for communication between the NTBX34DA circuit cards runs at 19.2 kbaud. The link is an 8251 programmable universal synchronous/asynchronous receiver/transmitter (USART).

### Message interface

The message interface provides the processor with access to the drawers through a serial data link. The link contains four parallel-to-serial and serial-to-parallel shift registers.

# NTBX35AA

## Product description

The ISDN line concentrating module (LCM) digroup control card (DCC) performs time switching functions. The ISDN LCCM DCC performs time switching functions between a maximum of ten DS30A lines and four ISDN or POTS line drawers. The DS30A lines connect to the line group controller (LGC)

### Location

Two NTBX35AA cards are in one shelf of the ISDN LCM.

## Functional description

The NTBX35AA functions like the NT6X52. The NT6X52 is the DCC for the POTS LCM. The LCM processor card establishes the time switch connections for the NTBX35AA cards and monitors the card functions. If one DCC fails, the LCM switches activity to the other LCM shelf. The inactive DCC continues to run. The inactive DCCs do not send data to the LGC.

### Functional blocks

The NTBX35AA contains the following functional blocks:

- timing generation
- message removal and insertion
- time switching
- data select multiplexing
- D–channel multiplexing and demultiplexing
- peripheral module side (P–side) looparound
- hardware data check

### Timing generation

The timing generation block handles the clock and frame pulse that both DCCs receive from the LGC through the DS30A links. This clock runs the other clocks on the NTBX35AA. The frame pulse generates the counting chains and the signal. The card uses the counting chain. The hardware check circuits use the signal.

### Message removal and insertion

The DCCs handle the removal and insertion of messages in each LCM shelf. The DCCs receive and transmit messages (channel 1, port 0) to and from the LGC. This process also occurs when the cards are not active.

## NTBX35AA (end)

### Time switching

The time switch block allows the incoming 384 P–side timeslots to switch to a 320 central–side (C–side) timeslot. The following time switch RAMs pass the data stream to the data select multiplexer:

- one for B–channel ports 0 to 5
- one for B–channel ports 6 to 11
- one for the time–division multiplexed D–channels

### Data select multiplexing

Data select multiplexing occurs in both directions. Incoming data arrives at the multiplexer. Control information in the C–side connection memory determines if the system selects the data. Selected data converts to serial transmission. Channel 1, port 0 does not convert to serial transmission. The selected data travels through the DS30A links to the LGC.

The multiplexer selects outgoing data based on the control information in the P–side connection memory. The processor demultiplexes and accesses the selected data.

### D–channel multiplexing and demultiplexing

The ISDN D–channel multiplexing and demultiplexing block groups and ungroups four D–channels in to one byte. This process saves space on the card and increases performance. Each channel uses two bits for each byte.

### P–side looparound

The data stream goes to the bus interface card (BIC). The P–side looparound copies the outgoing data stream to a RAM. This process delays the data by the same time the mate data stream transmits to and returns from the BIC. A control bit selects the looped data or the BIC data to continue to the time switches and the time division multiplexer.

### Hardware data check

The hardware check circuit verifies the data path of the looped data in the DCC. The data read in the check location can differ from that written to a exact timeslot address location in the DCC. When this condition occurs, the hardware check circuit sets the DCC failure pin to 1. This process causes the processor to switch activity to the other LCM shelf.

## Technical data

### Power requirements

The nominal supply voltage for the NTBX35AA is +5V and the supply current is less than 5A.

# NTBX36AA

## Product description

The NTBX36AA bus interface card (BIC) provides interfaces between the following:

- a maximum of 48 line cards in the line drawer
- the NTBX36AA digroup control card (DCC) and the NTBX34AA ISDN line concentrating module (LCMI) processor card

The BIC supports integrated services digital network (ISDN) and plain old telephone service (POTS) lines.

## Functional description

The BIC selects one LCMI shelf as the primary interface, at any time. The activity state of the line drawer controls the selection. The BIC monitors LCMI drawer activity and performs digital looparound on command from the LCMI processor card. The two processes allow the BIC to perform maintenance functions.

The NTBX36AA functions like the NT6X54AA BIC.

### Functional blocks

The NTBX36AA contains the following functional blocks:

- central processor–side (C–side) interfaces
- peripheral–side (P–side) interface

### C–side interfaces

The C–side interfaces contains the DCC–interfaces, the processor interface and the activity control.

The DCC–interfaces has three digroups (DS–30A links). The pulse code modulation (PCM) data passes through the digroups in both directions to the DCC. The system sends the DS–30A, clock and frame pulse signal to the BIC. The signals are completely duplicated with an identical set from the mate DCC. The receive signals from the DCCs go through tristate buffers in the DCC interface. One set of signals continues to the X24 scan chips in the line–bus (L–bus) interface.

The processor interface transfers control messages from the processor card (NTBX34AA) to the X24 scan chips in the L–bus interface.

The activity control selects which of the two processor cards (NTBX34AA) interfaces with the line cards.

# NTBX36AA (end)

## P–side interfaces

The C–side interfaces contains the L–bus interfaces, the X24 scan chips and the relay multiplexer.

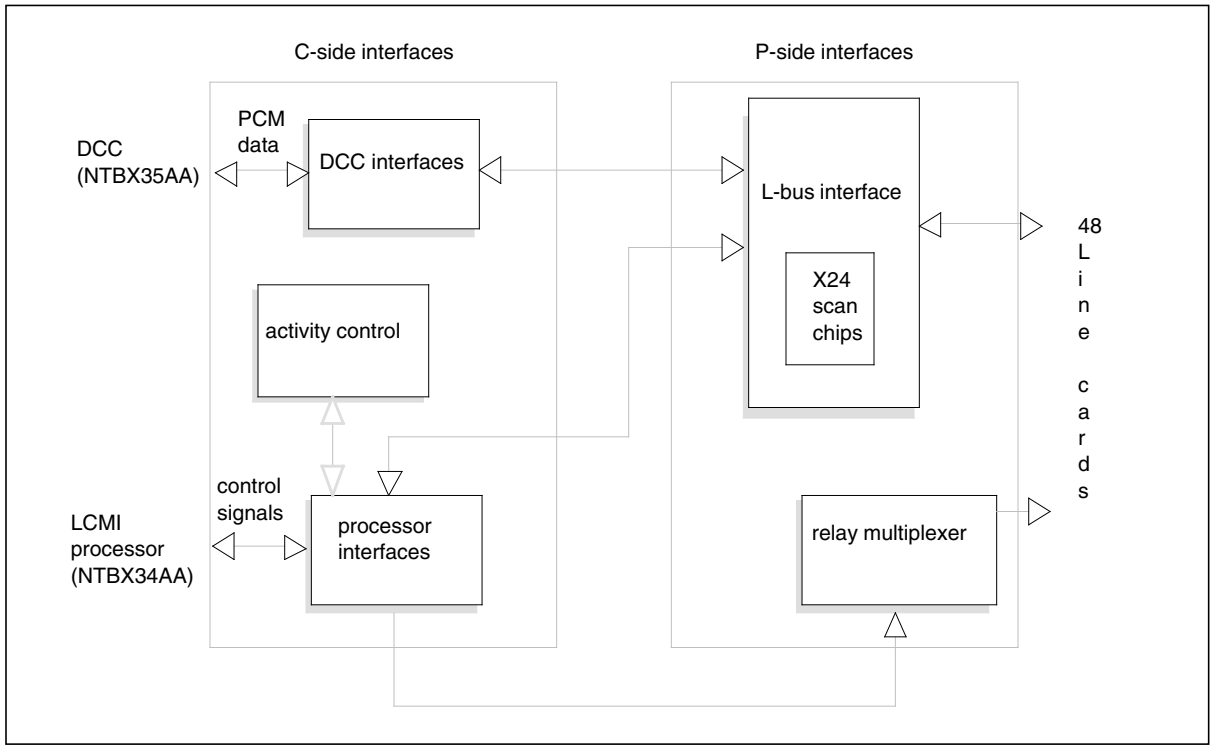
The L–bus is a bidirectional bus that interfaces the processor interface and the DCC interface to the line cards. The system designates each L–bus to one line card slot. There are 48 L–buses that carry two types of transactions. The transaction types are control messages from the processor card and PCM data from the DCC.

The X24 scan chips perform the L–bus interface functions between the line cards and the DCC. These chips generate timing signals for L–buses and control the relays. The scan chips handle 32 L–buses on the P–side and two complete sets of DCC signals on the C–side.

The relay multiplexer switches ringing voltages and automatic number identification and/or coin voltages. The relay multiplexer switches these features from the frame to the line cards that require them.

The relationship between the functional blocks appears in the following figure.

**NTBX36AA functional blocks**



# NTBX36BA

## Product description

The ISDN line concentrating module (LCM) enhanced line drawer bus interface card (BIC) is a component of the enhanced ISDN two–binary one–quaternary (2B1Q) access subsystem. This subsystem is the LCME.

## Functional description

The NTBX36BA provides an interface between the LCME common control and the 60 line cards that the line drawer accommodates.

The NTBX36BA provides the following functions:

- line card bus (L–bus) interface
- line card scanning
- control messaging
- pulse code modulation (PCM) data timeswitching
- D–channel multiplexing and demultiplexing timeswitching
- point–of–use power supply (PUPS) voltage supervision
- line card functions
- ringing relay control
- digroup selection and activity switching

### Functional blocks

The NTBX36BA consists of the following functional blocks:

- S14 enhanced line scan chip
- activity select
- phase–locked loop
- C195 delay circuit
- PUPS voltage supervision circuit
- ring multiplex relays
- 12.7V precision regulator
- +15V to +5V converter
- reset circuit

## NTBX36BA (continued)

### S14 enhanced line scan chip

The S14 enhanced line scan chip is the core of the NTBX36BA. This chip provides the following functions:

- terminates three digroups that originate from the host through the digroup control card
- maintains a direct connection to the LCME processor card
- generates four control signals that the system distributes to the line cards
- provides a control signal for the PUPS

### Activity select

The activity select line (ACT) selects the group of common control signals from the LCME units (active and mate), to input to the S14 chip. The ACT can determine which group of signals is disabled and which group is input. This process allows the BIC and the line drawer to operate during a common equipment failure.

### Phase–locked loop

The phase–locked loop allows the frequency and the phase of the 5.12 MHz clock to be synchronized with the incoming C195 clock. The S14 generates the 5.12 MHz clock on the card.

### C195 Delay circuit

The delay circuit receives two 5.12 MHz biphase inputs from the C195. These inputs enable the S14 to generate the 10.24 MHz clock.

### PUPS voltage supervision circuit

The card monitors the +5V output from the PUPS to the line cards to detect failure. When the card detects a long–term drop, the supervision circuit filters out short–duration glitches in the +5V rail. The circuit delivers a fail signal to the hardware monitor on the S14.

### Ring multiplex relays

Three ring multiplex relays are available. One relay holds line card relays open during cut–over and the other two relays control the ring bus.

### +12.7V precision regulator

The +15V input from common control generates a precise temperature–compensated +12.7V reference for distribution to the line drawer.

### +15V to +5V converter

The +15V to +5V converter is a high efficiency, 75% efficient, converter. This converter transforms the +15V from the common equipment supply to +5V

that the NTBX36BA requires. This process allows the NTBX36BA to detect and survive a PUPS failure.

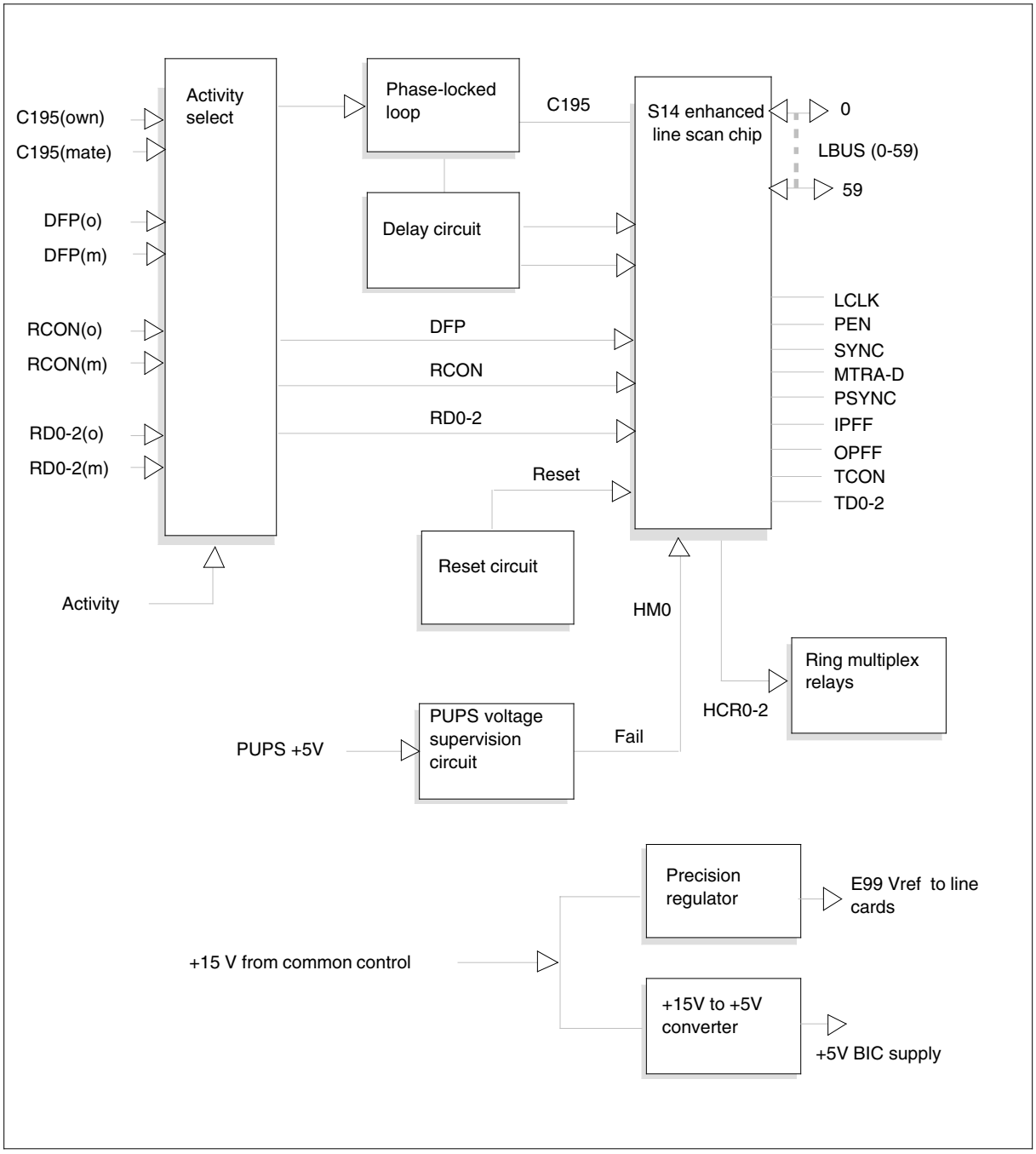
### Reset circuit

The reset circuit senses the output level of the +15V to +5V converter. The circuit resets the S14 chip when a voltage drop lasts longer than 0.2 ms. The reset circuit must hold the S14 chip in reset during insertion of the NTBX36BA in the backplane.

The relationship between the functional blocks appears in the following table.

# **NTBX36BA** (continued)

### NTBX36BA functional blocks



## Signaling

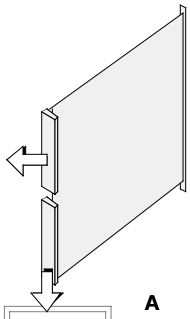
### Pin numbers

The pin numbers for the NTBX36BA appear in the following figure.

# **NTBX36BA** (continued)

### NTBX36BA pin numbers

| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +15V | +15V |
| 3A 3B | GND | GND |
| 4A 4B | +5VMON | PSYNC |
| 5A 5B | GND | ACT |
| 6A 6B | SYNC3 | PEN3 |
| 7A 7B | LCLK3 | CUTO |
| 8A 8B | MTRD | VREF |
| 9A 9B | GND | GND |
| 10A 10B | LB58 | LB59 |
| 11A 11B | LB56 | LB57 |
| 12A 12B | LB54 | LB55 |
| 13A 13B | LB52 | LB53 |
| 14A 14B | LB50 | LB51 |
| 15A 15B | LB48 | LB49 |
| 16A 16B | LB46 | LB47 |
| 17A 17B | GND | GND |
| 18A 18B | SYNC2 | PEN2 |
| 19A 19B | LCLK2 | CUTO |
| 20A 20B | MTRC | VREF |
| 21A 21B | GND | GND |
| 22A 22B | LB44 | LB45 |
| 23A 23B | LB42 | LB43 |
| 24A 24B | LB40 | LB41 |
| 25A 25B | LB38 | LB39 |
| 26A 26B | LB36 | LB37 |
| 27A 27B | LB34 | LB35 |
| 28A 28B | LB32 | LB33 |
| 29A 29B | GND | GND |
| 30A 30B | DFP+ | DFP- |
| 31A 31B | C195+ | C195- |
| 32A 32B | GND | GND |
| 33A 33B | DFP+M | DFP-M |
| 34A 34B | C195+M | C195-M |
| 35A 35B | GND | GND |
| 36A 36B | TCON0 | RCON0 |
| 37A 37B | TCON0M | RCON0M |
| 38A 38B | TCON1 | TCON1M |
| 39A 39B | TCON2 | TCON2M |
| 40A 40B | GND | GND |



| | A | B |
|---|---|---|
| 41A 41B | GND | GND |
| 42A 42B | TD0 | RD0 |
| 43A 43B | TD1 | RD1 |
| 44A 44B | TD2M | RD2M |
| 45A 45B | TD1M | RD1M |
| 46A 46B | TD0M | RD0M |
| 47A 47B | TD2 | RD2 |
| 48A 48B | GND | GND |
| 49A 49B | SYNC1 | PEN1 |
| 50A 50B | LCLK1 | CUTO |
| 51A 51B | MTRB | VREF |
| 52A 52B | GND | GND |
| 53A 53B | LB30 | LB31 |
| 54A 54B | LB28 | LB29 |
| 55A 55B | LB26 | LB27 |
| 56A 56B | LB24 | LB25 |
| 57A 57B | LB22 | LB23 |
| 58A 58B | LB20 | LB21 |
| 59A 59B | LB18 | LB19 |
| 60A 60B | LB16 | LB17 |
| 61A 61B | GND | GND |
| 62A 62B | SYNC0 | PEN0 |
| 63A 63B | LCLK0 | CUTO |
| 64A 64B | MTRA | VREF |
| 65A 65B | GND | GND |
| 66A 66B | LB14 | LB15 |
| 67A 67B | LB12 | LB13 |
| 68A 68B | LB10 | LB11 |
| 69A 69B | LB08 | LB09 |
| 70A 70B | LB06 | LB07 |
| 71A 71B | LB04 | LB05 |
| 72A 72B | LB02 | LB03 |
| 73A 73B | LB00 | LB01 |
| 74A 74B | GND | GND |
| 75A 75B | RINGBUST | RINGBUSR |
| 76A 76B | GND | GND |
| 77A 77B | RINGT | RINGR |
| 78A 78B | GND | GND |
| 79A 79B | A/CT | A/CR |
| 80A 80B | GND | GND |

# Technical data

## Power requirements

The minimum supply voltage is 14.25V. The small supply voltage is 15V. The maximum supply voltage is 15.75V. The maximum supply current is 307 mA.

# NTBX37AB

## Product description

The NTBX37AB ISDN line concentrating equipment (LCEI) frame supervisory panel includes power supervisory equipment and two talk battery filters. The power supervisory equipment includes the frame fail lamp, fan fail lamp, and four frame jacks DATA–A, DATA–B, TEL–A, and TEL–B. Other jacks give front and rear fused access to the alarm battery supply (ABS), two talk battery filters and ten circuit breakers. These jacks also provide four ABS fuses, and two NT6X36AA alarm cards.

Circuit breakers CB2, CB4, CB6, and CB8 feed a dc voltage of -48V to four NT6X53 power converters. The CB3, CB5, CB7, and CB9 feed a dc voltage of -48V to four NTBX72AA battery and ring routers. The CB1 powers ringing generator 0 and CB10 powers ringing generator 1. The circuit breakers operate with alarm relays in the power converters, and with ten breaker trip circuits in the alarm cards.

This frame supervisory panel (FSP) monitors the ABS fuses, the external distribution fuses (+15, -15, +5, and -48V), and the cooling unit. The FSP also monitors the four NT6X53 power converters, four battery and ring routers, and the two NT6X30 ringing generators. If one of these devices activates the alarm, the aisle alarm loop closes, and the frame fail lamp lights. The fan fail lamp lights if the cooling unit fails. The aisle alarm loop closes if the alarm battery supply fails. The FSP monitoring includes the activation of the alarm LED on the power converters.

The FSP includes points for the connection of the end aisle lamp.

## Parts

The NTBX37AB FSP includes two alarm cards (NT6X36AA) and the LCEI FSP assembly (NTBX3704).

### Alarm card

The NT6X36AA alarm card monitors operating conditions. The card activates visual indications of failures and dangerous operating conditions. The alarm loop can close because of a cooling fan failure, a tripped circuit breaker, or a T1 alarm. In this event, the alarm card lights the frame fail lamp. If a problem occurs in a power converter or ringing generator in the frame, the card lights the alarm LED.

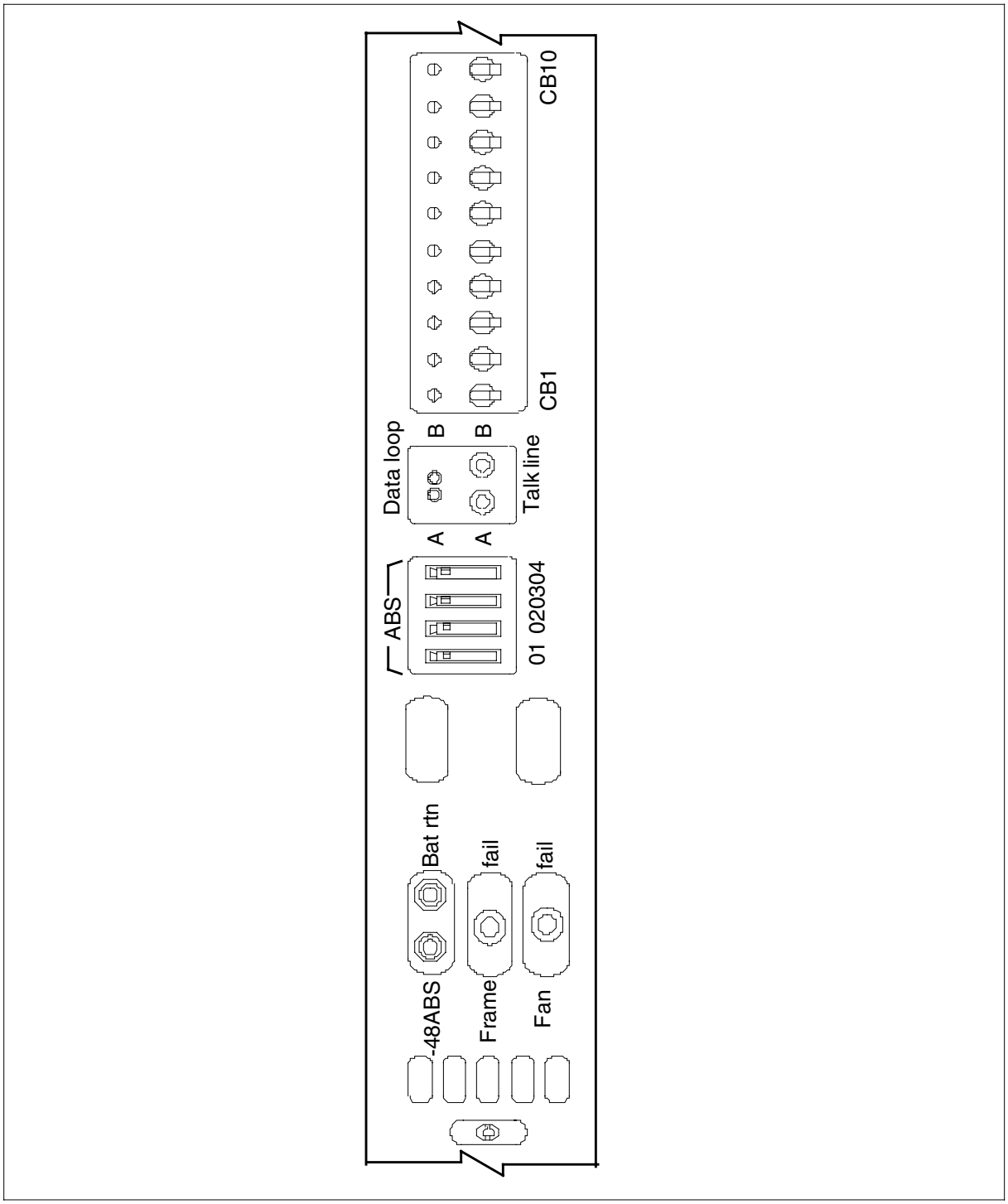
The alarm cards are in FSP locations CD1 and CD2.

## Design

The design of the NTBX37AB FSP appears in the following figure. The alarm cards and talk battery filter inside the FSP are not visible in this figure.

# **NTBX37AB** (end)

### NTBX37AB parts



# NTBX40AA

## Product description

The NTBX40AA integrated access equipment frame allows use of common channel signaling (CCS). The CCS is a signaling method that transmits information for a number of trunks over a separate trunk. The integrated access equipment (IAE) frame uses the Common Channel Signaling 7 (CCS7). This frame associates the signaling information that the CCS link carries with the voice and data that the CCS trunk carries.

The integrated access equipment frame combines technology from the line trunk controller and the message switch and buffer. The frame includes a central–side (C–side) interface, a duplicated processor complex, signaling terminals, and a peripheral–side (P–side) interface. The processor complex includes a master processor card, and a signaling processor card. The processor complex also includes cards that handle the reception, transmission, and temporary storage of data.

This frame supports the primary rate interface to ISDN and provides call control for functional signaling. For primary rate interface, the P–side uses DS–1 interface cards for links to digital private branch exchanges (PBX) or other switching offices. The C–side uses DS30 interface cards for links that carry information through the two planes of network modules to the central control complex. These links also carry information to other peripheral modules.

This frame requires a logic return but does not require a connection to the logic return busbar. A switchboard cable runs from the logic ground busbar assembly (NT0X9504) at each frame to the power distribution center battery return plate. The power distribution center battery return plate supplies the power.

## Parts

The NTBX40AA integrated access equipment frame consists of the following parts:

- NT0X28AP—frame supervisory panel (FSP)
- NT6X08AA—signaling terminal extension shelf
- NTBX40BC—integrated access controller CP fill
- NTBX45AA—signaling terminal card

### Frame supervisory panel

The NT0X28AP FSP contains power control and alarm circuits. These circuits provide interfaces between the power distribution center and the equipment

## **NTBX40AA** (continued)

frames of the DMS–100 switch. Six circuit breakers (CB), one NT0X91AA converter drive and alarm, and two NT0X91AE converter drive and protection cards provide power control to the IAE frame. One FSP is mounted on each IAE frame.

### Signaling terminal extension shelf

Two NT6X08AA signaling terminal extension shelves are on the NTBX40AA frame. Each signaling terminal extension shelf contains one or two groups. Each group is a signaling terminal controller modules and can contain a maximum of eight signaling terminal cards. A pair of signaling terminal interface cards associates with each signaling terminal controller module. The signaling terminal interface cards isolate a group of eight signaling terminals from the control bus. This action allows the signaling terminal controller modules to be added or repaired and does not affect the function of other signaling terminals. The signaling terminal interface communicates with the signaling terminals when the control bus is active. The signaling terminal interface includes a control bus buffer, a speech bus circuit, maintenance circuits and a signaling terminal bus buffer. This interface also includes address match and control circuitry.

Basic rate interface requires the NT6X68AC, NTBX44AC, and NTBX44AD signaling terminal interface cards. Primary rate interface requires the NT6X68AC and NT6X68AD signaling terminal interface cards.

### Integrated access controller card

The NTBX40BC integrated access controller card is used for the basic rate interface and the primary rate interface. This card replaces NTBX40BA and NTBX40BB. This card is required for applications BCS27 or later.

Each NTBX40AA frame has two integrated access controller (IAC) shelves. Each IAC shelf contains the set of cards required to operate the P–side and C–side interfaces and the IAC control complex. Each shelf also contains the internal interfaces with the signaling terminals.

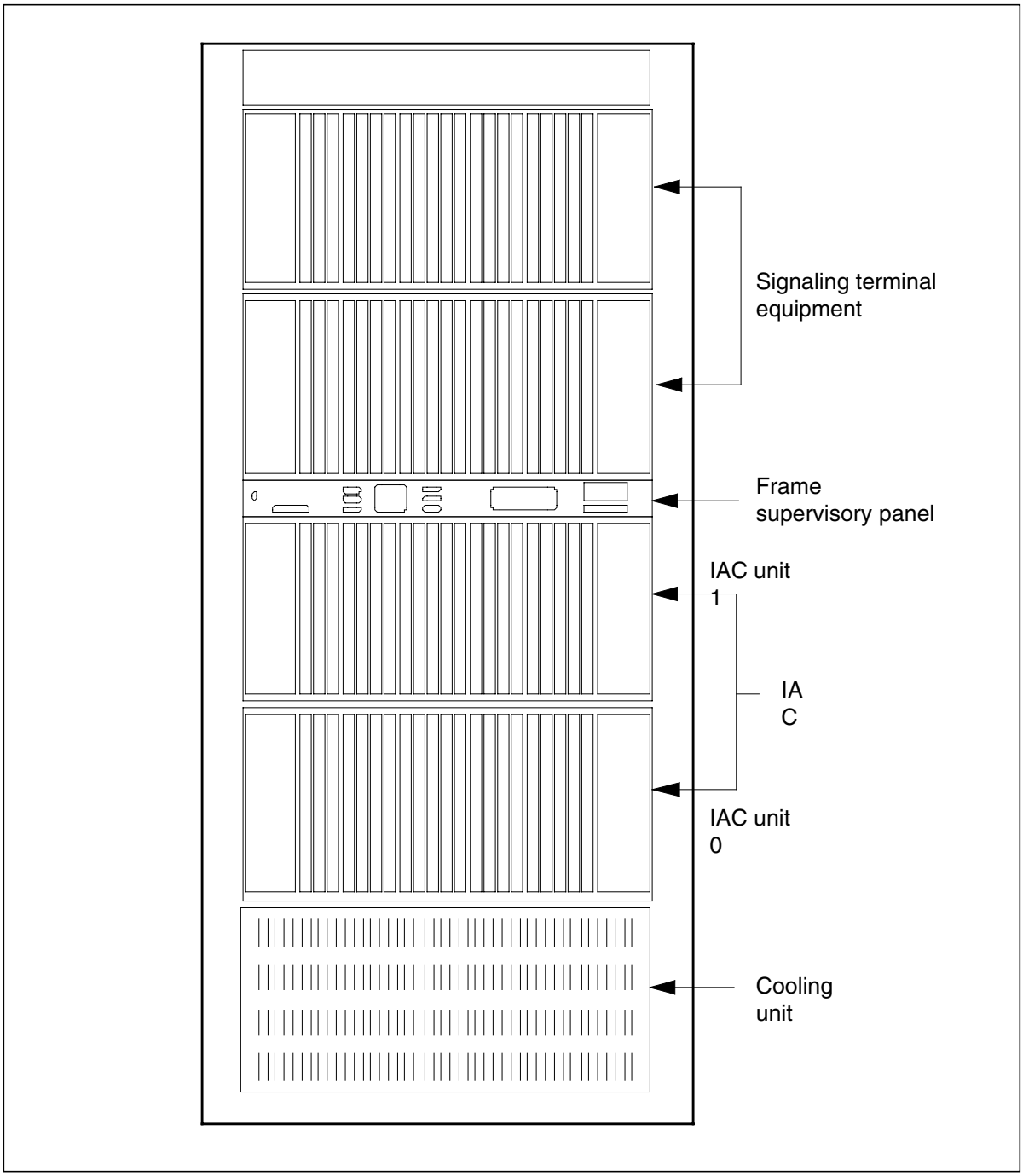
### Signaling terminal cards

Each of the two signaling terminal equipment shelves in the NTBX40AA frame contains two signaling terminal groups. Signaling terminal group 0 acts as the packet handler interface group. For basic rate interface, the NTBX45AA signaling terminal cards are assigned, one on each line, as D–channel handlers. For primary rate interface, the NTBX45AA signaling terminal cards are assigned, one on each D–channel, on the primary rate interface trunks.

## Design

The design of the NTBX40AA appears in the following figure.

**NTBX40AA parts**




***Note:*** Front panels are removed to illustrate NTBX40AA parts. This illustration is not drawn to scale.

# NTBX71AA

## Product description

The ISDN enhanced line drawer point–of–use power supply (PUPS) provides power to a drawer of ISDN line cards. The NTBX71AA is a power converter that operates from the normal -52V office battery and provides a +5V output.

## Functional description

The NTBX71AA provides a +5V power supply to the ISDN line cards in the drawer.

### Functional blocks

The NTBX71AA consists of the following functional blocks:

- input filter
- power conversion circuit
- minimum load
- current sense
- start–up supply
- pulse width modulator (PWM) and control circuit
- synchronization circuit
- output feedback
- output overvoltage shutdown

### Input filter

The input filter reduces switching noise fed back to the battery input. The input filter includes differential and common–mode filtering components.

### Power conversion circuit

The power conversion circuit pulses the input voltage. The circuit steps the voltage down through a transformer that provides input and output isolation. The circuit rectifies and filters this signal to produce a stable output.

### Minimum load

The minimum load samples the output current through a current sense transformer to determine the load current level. If the output load approaches the lower limit of an acceptable minimum load, a dummy load is switched in. The dummy load is switched in until the converter operates at a zero external load current.

### Current sense

The current sense block samples the input current through a current–sense transformer. The current sense block rectifies and filters the input current. The system feeds the signal back to the PWM for pulse–width control purposes.

### Start–up supply

The start–up supply provides a slow start feature that helps limit the surge of current when a PUPS is plugged in a line drawer. The start–up supply provides power to the chip until the feedback loop is in place.

### PWM and control circuit

The PWM and control circuit control the switching of the input FETs and provide features like current limiting and shutdown.

### Synchronization circuit

The synchronization circuit transmits the external synchronization signal to the PWM. An optocoupler provides isolation of the signal.

### Output feedback

The output feedback samples the output voltage and compares the voltage to a stable reference. The output feedback sends the difference signal to the PWM for pulse width control purposes. An optocoupler provides isolation between the primary (input) signal and secondary (output) signal.

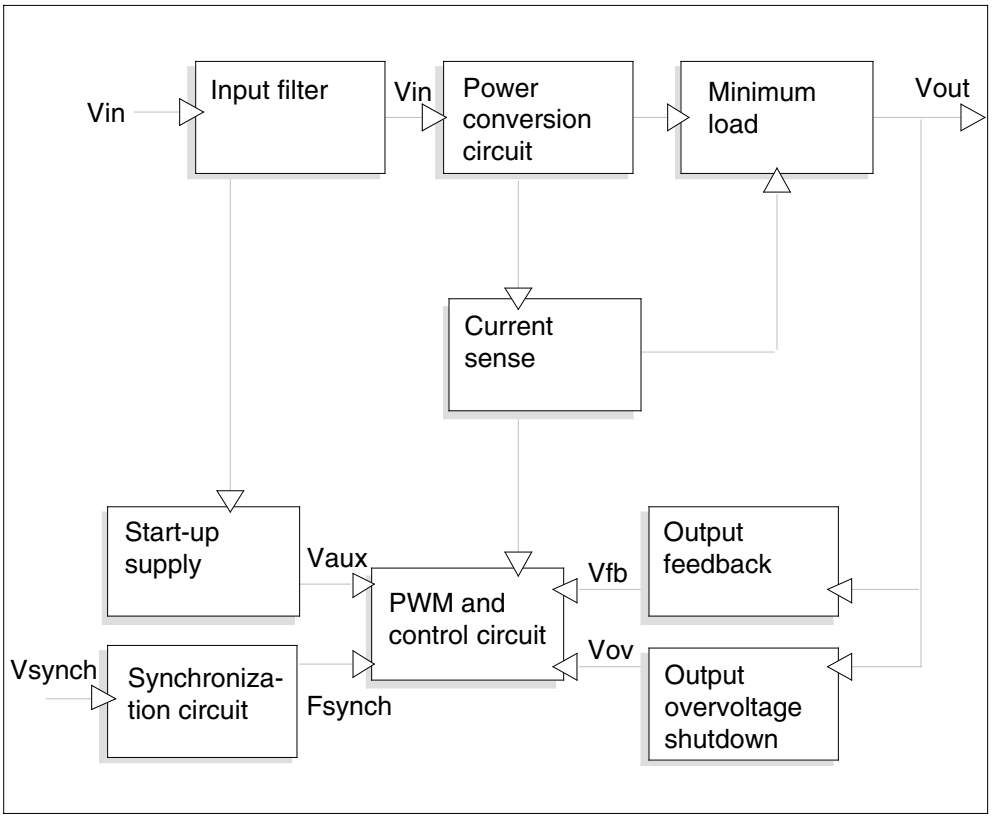
### Output overvoltage shutdown

The output overvoltage shutdown samples the output voltage and checks for an overvoltage condition. If the shutdown detects an overvoltage, the shutdown sends back a signal to the PWM to shut down the NTBX71AA. To reset the card, remove power and apply power again.

The relationships between these functional blocks appears in the following figure.

## **NTBX71AA** (continued)

**NTBX71AA functional blocks**




# Signaling

## Pin numbers

The pin numbers for the NTBX71AA appear in the following table.

**Top connector pin numbers (Sheet 1 of 2)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1A | NS | 1B | NC |
| 2A | GND | 2B | GND |
| 3A | +5V | 3B | +5V |
| 4A | GND | 4B | GND |
| 5A | +5V | 5B | +5V |
| 6A | GND | 6B | GND |

**Top connector pin numbers (Sheet 2 of 2)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 7A | +5V | 7B | +5V |
| 8A | GND | 8B | GND |
| 9A | +5V | 9B | +5V |
| 10A | GND | 10B | GND |
| 11A | +5V | 11B | +5V |

**Bottom connector pin numbers**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1A | MINLOAD | 1B | OVPTEST |
| 2A | GND | 2B | GND |
| 3A | +5V | 3B | +5V |
| 4A | GND | 4B | GND |
| 5A | SYNCHIN | 5B | GND |
| 6A | NS | 6B | NS |
| 7A | –48VBAT | 7B | –48VBAT |
| 8A | –48VADV | 8B | –48VBAT |
| 9A | NS | 9B | VAUX |
| 10A | –48VRET | 10B | –48VRET |
| 11A | –48VRET | 11B | –48VRET |

## **NTBX71AA** (end)

# Technical data

### Power requirementsInput

The input specifications for the NTBX71AA appear in the following table.

**Input specifications**

| Parameter | Value |
|---|---|
| Minimum voltage | 39.5 V |
| Nominal voltage | -52 V |
| Maximum voltage | -56V |
| Transient voltage | -60V |
| Maximum current | 2.5 A |

### Output

The output specifications for the NTBX71AA appear in the following table.

**Output specifications**

| Parameter | Value |
|---|---|
| Nominal voltage | 5.1 V |
| Minimum current | 25 mA |
| Maximum current | 10 A |
| Current limit | 13.4 A ±1.5 A |
| Regulation | ± 3% |
| Noise b/band (0-10 MHz) | 50 mVrms |
| Overvoltage shutdown | Threshold at 6 V ±0.5 V |

# NTBX72AA

## Product description

The ISDN enhanced line concentrating module (LCME) battery and ringing router card monitors the current of different ANI/COIN inputs that a multiplexer (MUX) circuit selects.

## Functional description

The NTBX72AA consists of a relay network that acts as a MUX, a ring current detector, and a +5V auxiliary switching supply. The ring current detector monitors the level of the current. The switching supply feeds the MUX logic and the ring detector. An alarm circuit indicates failure of the +5V or -48V power supply of the card. A high current Schottky rectifier functions as an isolater and power distributor for other cards.

### Functional blocks

The NTBX72AA consists of the following functional blocks:

- ring detector
- MUX
- auxiliary power supply
- alarm circuit

### Ring detector

The ring detector accepts a current from the ANI/COIN circuits. If this current reaches or exceeds 10 mA, the output pin 44A changes states.

### MUX

Incoming logic signals control ANI/COIN input. The MUX accepts and selects the ANI/COIN input and directs the input to the appropriate output.

### Auxiliary power supply

The auxiliary power supply provides low power (+5V) to the logic elements of the ring detector, the alarm relay circuit, and the MUX.

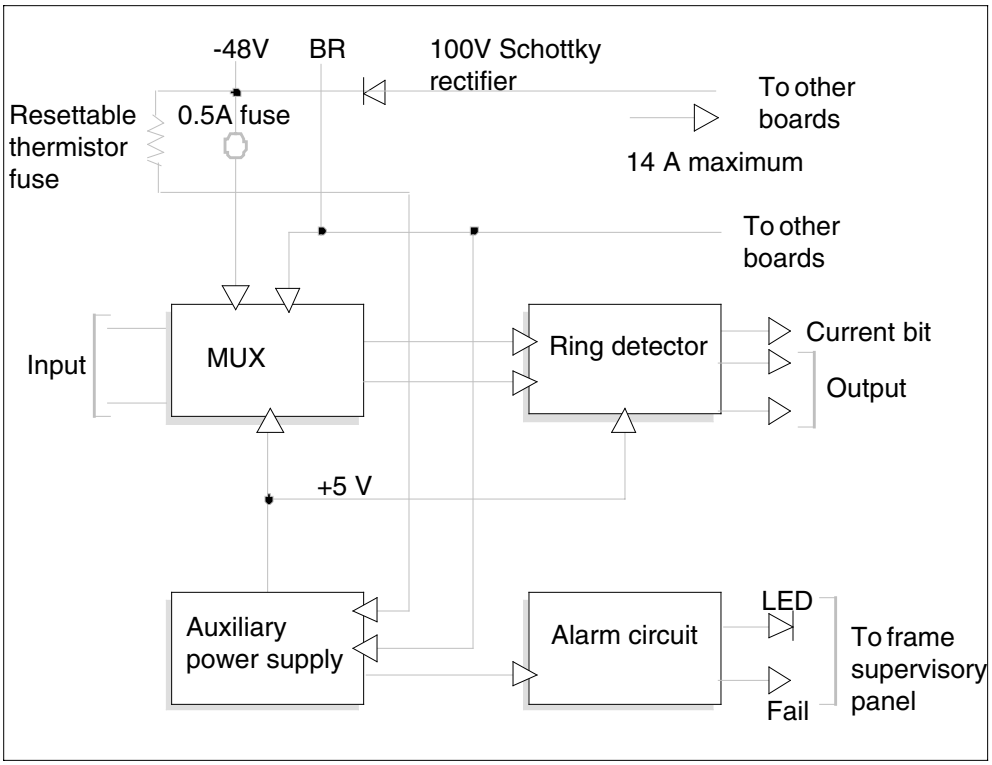
### Alarm circuit

The alarm relay circuit turns on an LED failure indicator and sends an alarm signal to the frame supervisory panel. The circuit sends the alarm when the +5V or the -48V power supply fails.

The relationship between the functional blocks appears in the following figure.

## **NTBX72AA** (continued)

**NTBX72AA functional blocks**

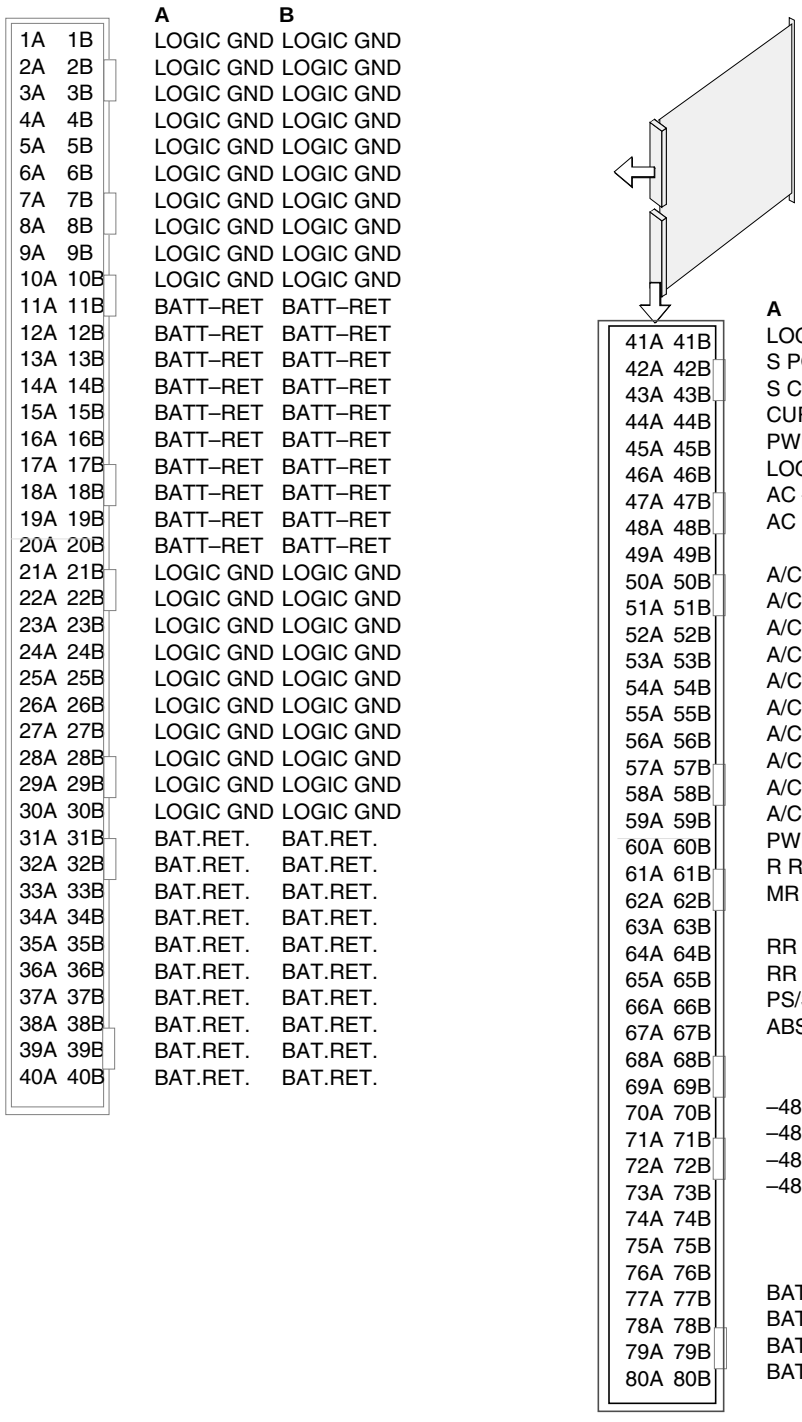



# Signaling

### Pin numbers

The pin numbers for the NTBX72AA appear in the following figure.

### NTBX72AA pin numbers



## **NTBX72AA** (end)

# Technical data

### Power requirements

The minimum supply voltage for the NTBX72AA is -38V. The maximum supply voltage is -60V. The maximum supply ripple is 120 mV peak–to–peak. The minimum supply current is 106 mA.

# 4 NTCXnnaa

## NTCX07AB through NTCX50BA

# NTCX07AB

## Product description

The coin and multiparty simulator paddle board works with the main card NTCX08AB to simulate eight telephone sets. The paddle board is based on the test access controller (TAC). These sets appear in the following table.

**Simulation possibilities**

| Set type | Set list |
|---|---|
| POTS | 500 (rotary dial) |
| | 2500 (Digitone) |
| | multiparty without ANI (up to 10 parties) |
| | multiparty with ANI (T1, T2, R1, R2) |
| | link set |
| PBX | ground start |
| CLASS | calling number delivery (CND) |
| COIN | coin first (CCF) |
| | dial tone first (CDF) |
| | semi post pay (CSP) |

The NTCX07AB paddle board and the NTCX08AB card replace the TAC plain ordinary telephone service (POTS) simulator card set. The TAC POTS card set includes the NTCX07AA and NTCX08AA. Cards are not interchangeable between the two sets.

### Location

The NTCX07AB paddle board is in the TAC. The TAC is a peripheral that can house a maximum of 48 simulator card sets in three extension shelves. The system can support 384 test head loops because each simulator card set (test head) can simulate eight telephone sets. A hardware restriction on the TAC limits the actual number of test head loops to 374.

## Functional description

The NTCX07AB card performs some of the line interface functions of the coin–simulator card set. For example, the NTCX07AB card allows the simulator to go onhook and offhook. The main card, NTCX08AB, provides the additional line interface functions.

### Functional blocks

The NTCX07AB has the following functional blocks:

- loop termination and hook switch
- audio buffer
- paddle board input/output (I/O)

### Loop termination and hook switch

The loop termination and hook switch allows the simulator to go onhook and offhook. This block provides analog termination for reception and transmission of tones.

### Audio buffer

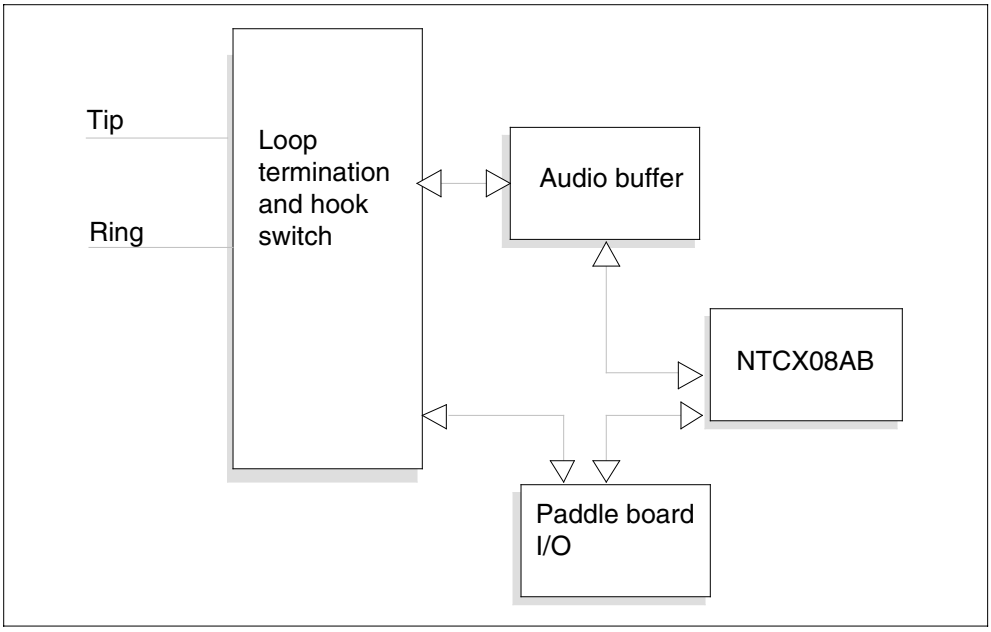
The audio buffer has two amplifiers. These amplifiers condition the speech signal in and out of the analog–to–digital coder/decoder (CODEC).

### Paddle board I/O

During a read operation, the paddle board I/O circuit returns a identification code on the data bus to the central processor. Each simulator set has one paddle board I/O circuit. This block contains the relay latches that control the line interfaces.

The relationship between the functional blocks appears in the following figure.

**NTCX07AB functional blocks**



## **NTCX07AB** (continued)

# Signaling

### Pin numbers

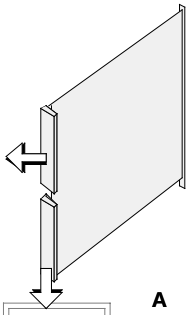
The pin numbers for the NTCX07AB paddle board appear in the following table and figure.

**NTCX07AB pin numbers connector P2**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | T0 | 9 | T4 |
| 2 | R0 | 10 | R4 |
| 3 | T1 | 11 | T5 |
| 4 | R1 | 12 | R5 |
| 5 | T2 | 13 | T6 |
| 6 | R2 | 14 | R6 |
| 7 | T3 | 15 | T7 |
| 8 | R3 | 16 | R7 |

***Note:*** T=Tip, R=Ring, associated number=circuit number

### NTCX07AB pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | +5V | +5V |
| 4A 4B | +5V | +5V |
| 5A 5B | GND | GND |
| 6A 6B | | |
| 7A 7B | GND | GND |
| 8A 8B | | |
| 9A 9B | | |
| 10A 10B | | |
| 11A 11B | | |
| 12A 12B | | |
| 13A 13B | | |
| 14A 14B | | |
| 15A 15B | GND | GND |
| 16A 16B | GND | GND |
| 17A 17B | | |
| 18A 18B | | |
| 19A 19B | | |
| 20A 20B | | |
| 21A 21B | | |
| 22A 22B | | |
| 23A 23B | GND | |
| 24A 24B | | PBDATA0 |
| 25A 25B | PBRD- | PBDATA1 |
| 26A 26B | PBEN- | PBDATA2 |
| 27A 27B | PBWR- | PBDATA3 |
| 28A 28B | GND | GND |
| 29A 29B | | PBDATA4 |
| 30A 30B | | PBDATA5 |
| 31A 31B | | PBDATA6 |
| 32A 32B | | PBDATA7 |
| 33A 33B | | GND |
| 34A 34B | | |
| 35A 35B | TIP0 | |
| 36A 36B | RING0 | |
| 37A 37B | AI0 | |
| 38A 38B | AO0 | |
| 39A 39E | | |
| 40A 40B | GND | GND |

| | A | B |
|---|---|---|
| 41A 41B | GND | GND |
| 42A 42B | +5V | +5V |
| 43A 43B | GND | GND |
| 44A 44B | TIP1 | |
| 45A 45B | RING1 | |
| 46A 46B | AI1 | |
| 47A 47B | AO1 | |
| 48A 48B | TIP2 | |
| 49A 49B | RING2 | |
| 50A 50B | AI2 | |
| 51A 51B | AO2 | OC+ |
| 52A 52B | TIP3 | |
| 53A 53B | RING3 | |
| 54A 54B | AI3 | |
| 55A 55B | AO3 | |
| 56A 56B | GND | GND |
| 57A 57B | +12V | +12V |
| 58A 58B | GND | GND |
| 59A 59B | | |
| 60A 60B | GND | GND |
| 61A 61B | TIP4 | |
| 62A 62B | RING4 | |
| 63A 63B | AI4 | |
| 64A 64B | AO4 | |
| 65A 65B | TIP5 | |
| 66A 66B | RING5 | |
| 67A 67B | AI5 | |
| 68A 68B | AO5 | |
| 69A 69B | TIP6 | |
| 70A 70B | RING6 | |
| 71A 71B | AI6 | |
| 72A 72B | AO6 | |
| 73A 73B | TIP7 | |
| 74A 74B | RING7 | |
| 75A 75B | AI7 | |
| 76A 76B | AO7 | |
| 77A 77B | AGND | |
| 78A 78B | AGND | |
| 79A 79B | | |
| 80A 80B | GND | GND |

## **NTCX07AB** (end)

# Technical data

### Power requirements

The supply voltage for the NTCX07AB is 5.0V. The minimum supply voltage is 4.75V and the maximum supply voltage is 5.25V.

# NTCX08AB

## Product description

The coin and multiparty simulator card operates with the NTCX07AB paddle board to simulate eight telephone sets. The simulator card is based on the test access controller (TAC). These sets appear in the following table.

**Simulation possibilities**

| Set type | Set list |
|---|---|
| POTS | 500 (rotary dial) |
| | 2500 (Digitone) |
| | multiparty without automatic number identification (ANI) (maximum of 10 parties) |
| | multiparty with ANI (T1, T2, R1, R2) |
| | link set |
| PBX | ground start |
| CLASS | calling number delivery (CND) |
| COIN | coin first (CCF) |
| | dial tone first (CDF) |
| | semi post pay (CSP) |

The NTCX08AB card and the NTCX07AB paddle board replace the TAC plain ordinary telephone service (POTS) simulator card set. The TAC POTS card set includes NTCX08AA and NTCX07AA. Cards are not interchangeable between the two sets.

### Location

The NTCX08AB card is in the TAC. The TAC is a peripheral that can have a maximum of 48 simulator card sets in three extension shelves. The system can support 384 test head loops because each card set (test head loop) can simulate eight telephone sets. A hardware restriction on the TAC limits the number of test head loops to 374.

## Functional description

The NTCX08AB and the NTCX07AB provides some of the line interface functions. The NTCX08AB provides the control functions required to simulate eight telephone sets.

## **NTCX08AB** (continued)

### Functional blocks

The NTCX08AB has the following functional blocks:

- ground start, automatic number identification (ANI), and coin ground block
- coder/decoder (CODEC) block
- loop voltage dividers
- ringing detector block
- microcontroller
- erasable programmable read-only memory (EPROM)
- dual-port random-access memory (RAM) (DPRAM)
- input and output (I/O) block
- analog-to-digital (A/D) converter
- the TAC pulse code modulation (PCM) interface
- the TAC digital interface

### Ground start, ANI, and coin ground block

The ground start, ANI, and coin ground block can simulate the following conditions:

- a coin in a coin phone hopper
- the identification of a party line that is offhook
- a ground start

These functions provide a connection to ground. The ground is applied on the tip (T) conductor or the ring (R) conductor. The type of simulated function determines the location of the ground.

### CODEC block

The CODEC block converts analog speech signals to digital pulse code modulation (PCM) signals in the receive direction. The CODEC block converts PCM signals to speech signals in the transmit direction. Disabling the transmit direction simulates semi-post-pay public telephone sets.

### Loop voltage dividers

The loop voltage dividers condition the voltage of the T or R for input to the analog to digital converter. The maximum voltage of the T or R is 250V. The digital converter has a maximum input of 5V. To divide the input voltage and calculate the output voltage requires a given formula.

### Ringing detector block

Each test head loop has one ringing detector. The eight ringing detectors when switched can monitor for ringing voltage across any of the following:

- the T and R
- the T and ground
- the R and ground

The ringing detector sends a signal to the microcontroller when ringing voltage is present on a monitored line.

### Microcontroller

The 8031 microcontroller processes and executes commands from the TAC. The microcontroller can determine the ringing frequency and loop voltage from the signal that the ringing detector sends. The microcontroller can operate in a diagnostic mode and perform tests on the test head hardware.

### EPROM

The 8-kbyte EPROM contains the firmware for the NTCX08AB microcontroller. The EPROM also contains tables for ringing detection, loop voltage detection, and configurations. Four kbytes are free for future code improvements.

### DPRAM

The 2-kbyte DPRAM functions as a messaging buffer between the microcontroller and the TAC. The microcontroller uses the DPRAM as a scratch-pad memory. The DPRAM allows the TAC and the microcontroller to read or write at the same time. The two controllers cannot access the same location in the device at the same time. The internal bus arbitration gives priority to the first controller to attempt to access the device.

### I/O block

The I/O block is the interface between the microcontroller and the rest of the test head loop hardware. The I/O block contains the multiplexers, latches, drivers, decoders, address and data buffering to the NTCX07AB paddle board.

### A/D converter

The A/D converter converts the test head loop voltage to a binary format. The input voltage is the T-to-ground or the R-to-ground voltage of the eight test loops. The microcontroller calculates the T-to-R voltage.

### TAC PCM interface

The TAC PCM interface converts the single 80-bit PCM enable signal (DLEN-) to eight 8-bit enable signals, one for each CODEC. The 16 bits that

## **NTCX08AB** (continued)

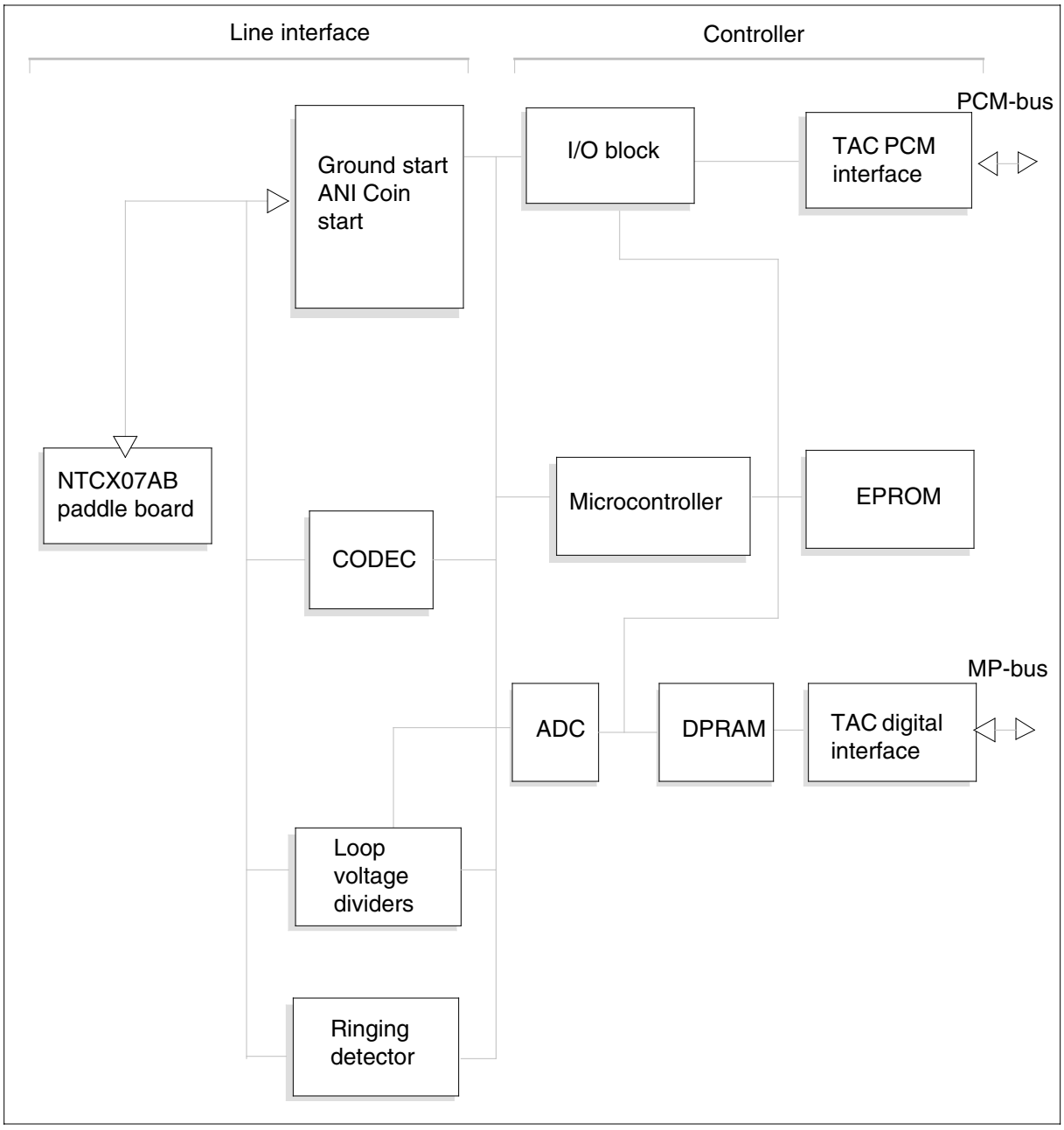
remain are discarded on the incoming PCM stream (DLRX). The system does not generate the bits on the outgoing stream. This interface also converts the 10-bit PCM stream to an 8-bit PCM stream. The 2 bits that remain are discarded.

### TAC digital interface

The TAC digital interface provides buffering for the address and data line signals of the TAC. The TAC digital interface manages the handshaking between the TAC and the DPRAM through the DUNIT signal.

The relationship between the functional blocks appears in the following figure.

**NTCX08AB functional blocks**



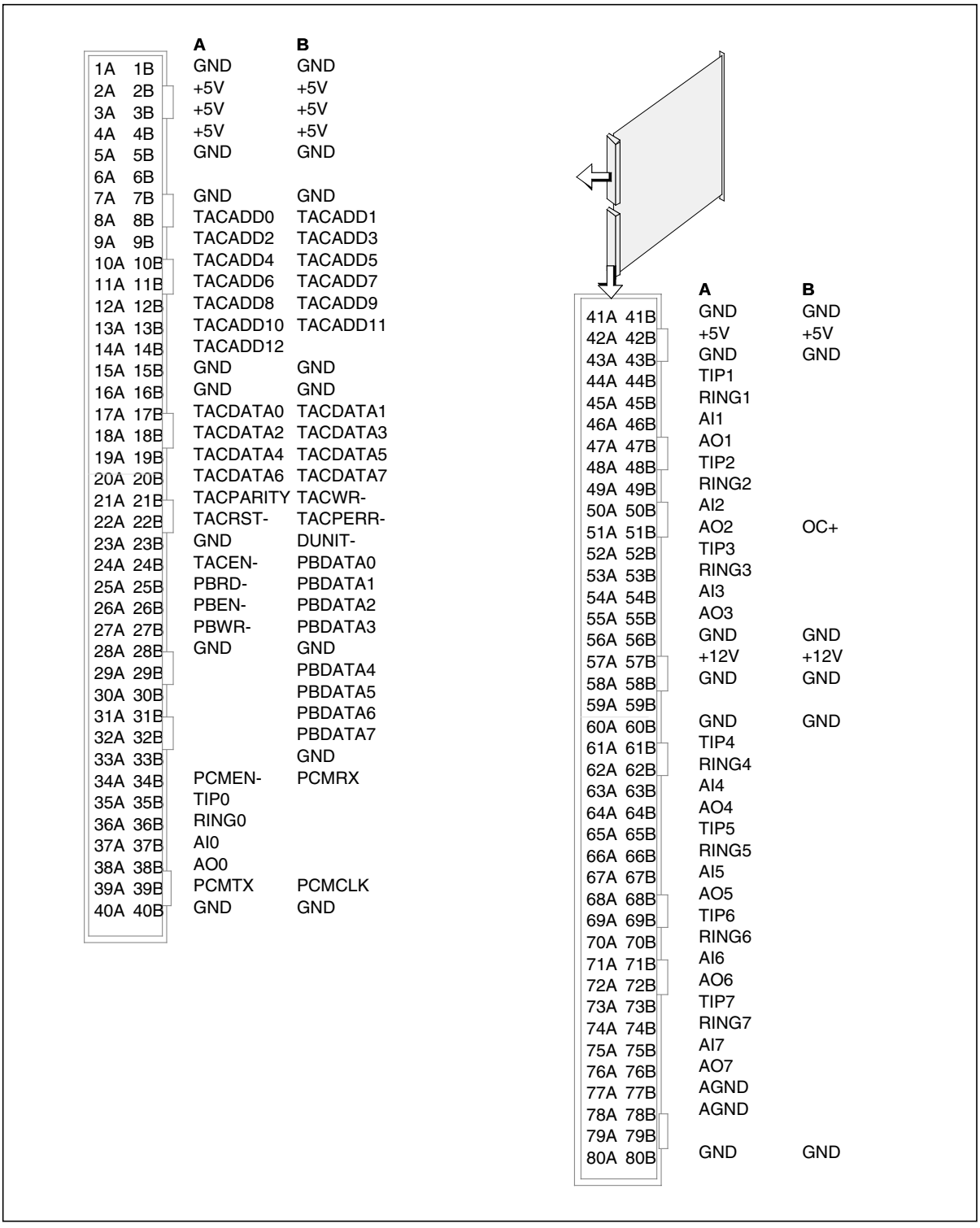

## Signaling

### Pin numbers

The pin numbers for NTCX08AB appear in the following figure.

# **NTCX08AB** (continued)

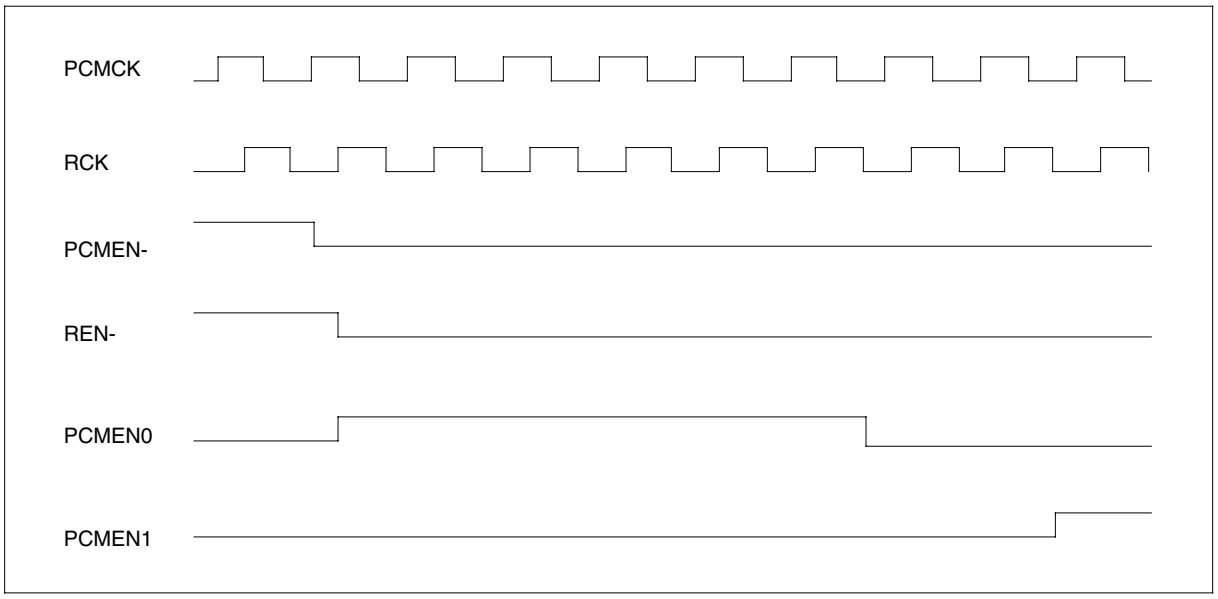
### NTCX08AB pin numbers



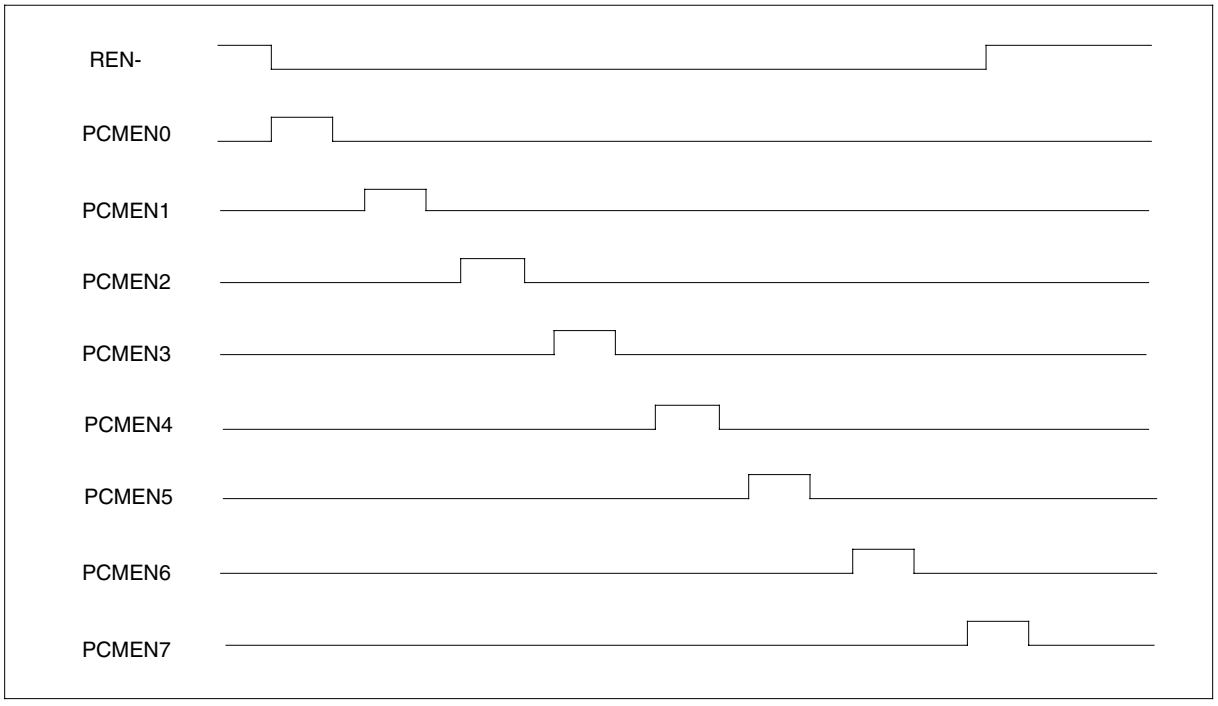
### Timing

The timing signals for NTCX08AB appear in the following figure.

**NTCX08AB recovered bit clock (DSCK) and DSEN- signal**

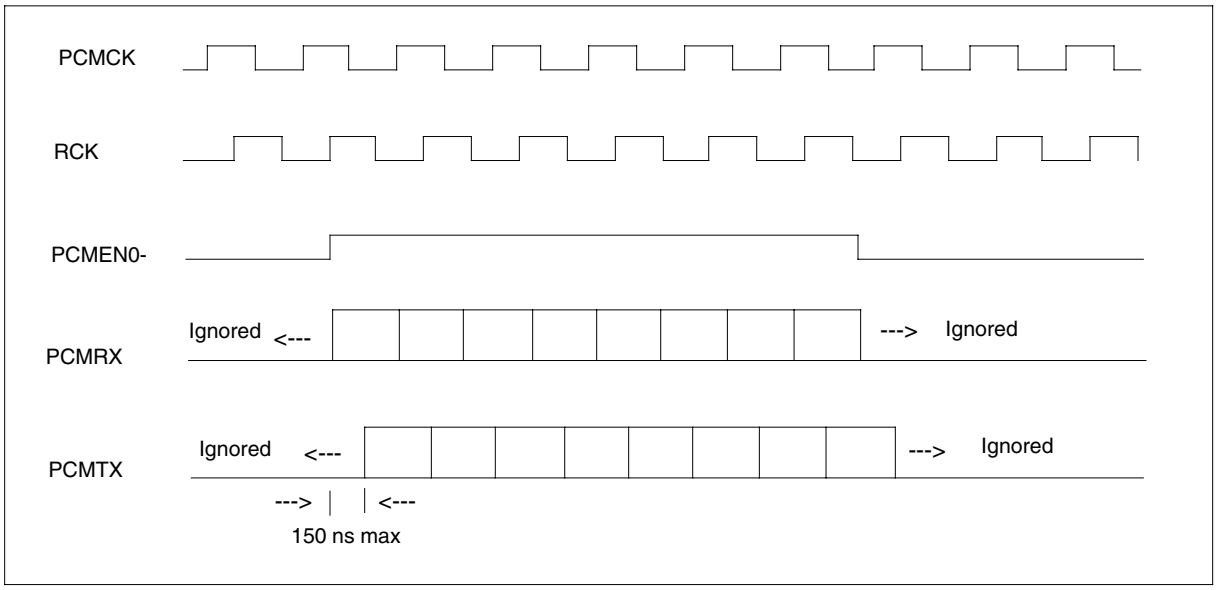



**NTCX08AB PCMENx signals**



# **NTCX08AB** (end)

**NTCX08AB PCM transmission**




## Technical data

### Power requirements

The supply voltage for the NTCX08AB is 5.0V. The minimum supply voltage is 4.75V and the maximum supply voltage is 5.25V.

# NTCX50AA

## Product description

The NTCX50AA echo canceller control (ECC) card is a paddle board for the NT6X28 signaling interface card. The NTCX50AA can control a maximum of 16 2 Mbps echo canceller modules.

The NTCX50AA has the following features:

- the RS232 or RS423 transmission protocol
- software control of card activity
- use in a polled or interrupt–driven environment
- on–board control and status registers
- variable board addressing
- hardware and software board reset
- a 64–character transmission and reception
- diagnostic capabilities

A duplicate of the NTCX50AA is on the PCM30 digital trunk controller (PDTC) in an active/standby configuration.

The NTCX50AA is compatible with current hardware. Backward compatibility is not a factor, because the NTCX50AA is the first issue of the paddle board.

### Location

The NTCX50AA is in slot 19, behind the NT6X28 signaling interface card, on the PDTC backplane.

## Functional description

The NTCX50AA allows the PDTC signaling processor (SP) to control echo canceller equipment from a distance. The SP uses an Electronic Industries Association (EIA) RS232 or RS423 transmission link. Software in the SP reads from and writes to the control and status registers on the ECC. A universal asynchronous receiver and transmitter (UART) defines and controls a handshake protocol with the echo cancellers. One ECC can control a maximum of 16 2–Mbps echo canceller modules.

### Functional blocks

The NTCX50AA has the following functional blocks:

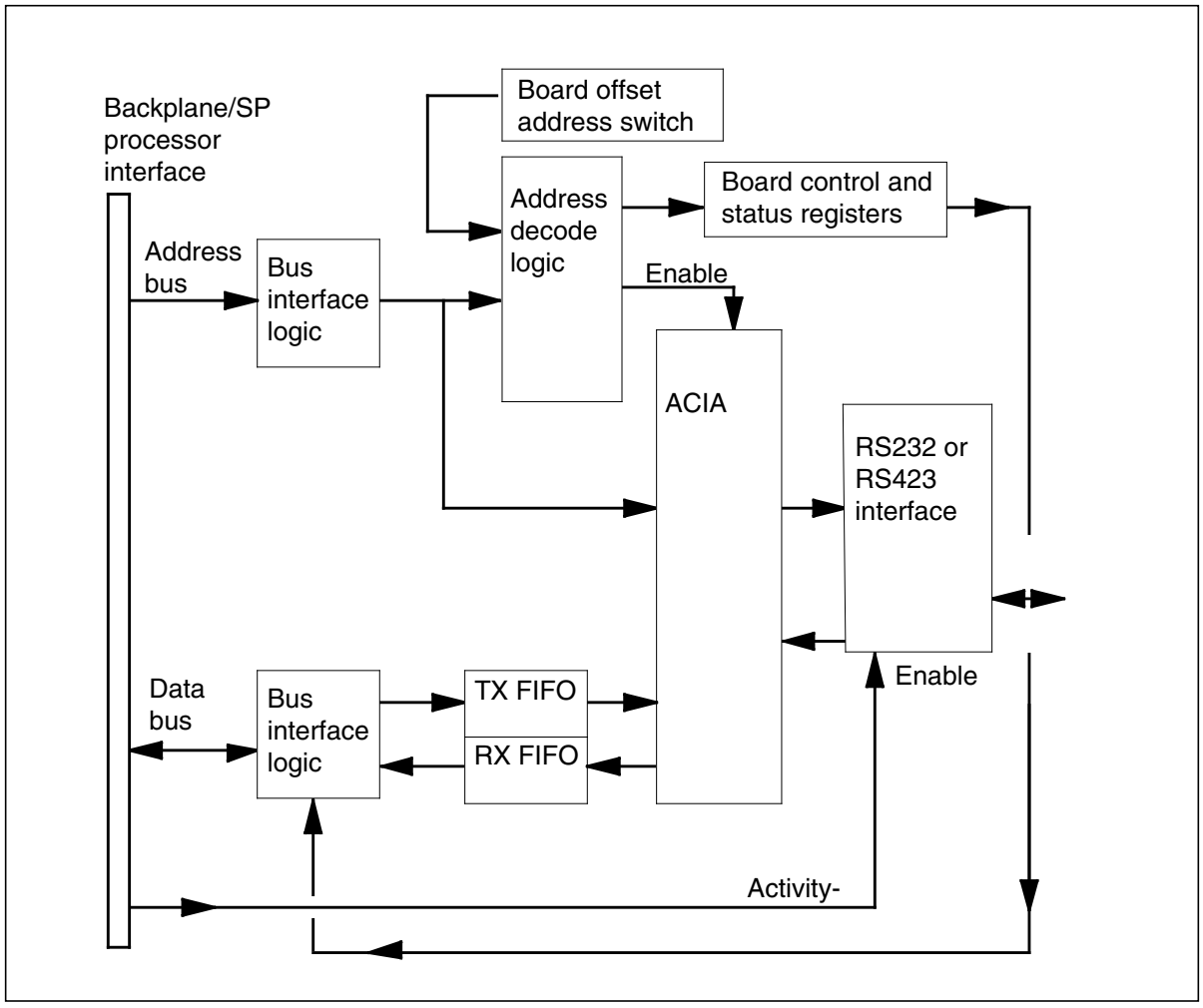
- bus interface logic
- transmit first–in–first–out (FIFO) memory

## **NTCX50AA** (continued)

- receive FIFO
- address decode logic
- board control and status registers
- asynchronous communications interface adapter (ACIA)
- the RS232 or RS423 interface

The relationship between the functional blocks appears in the following table.

**NTCX50AA functional blocks**



### Bus interface logic

The bus interface logic connects the PDTC backplane signals to the board signals. The bus interface logic uses tristate buffers on the processor address and data buses for the connection.

### Transmit FIFO memory

The transmit FIFO memory is a 64 byte memory that stores bytes. The NT6X45 SP generates the bytes that go to the ACIA.

### Receive FIFO memory

The receive FIFO memory is a 64 byte memory that stores bytes. The ACIA generates the bytes that go to the NT6X45 SP.

### Address decode logic

The address decode logic selects board registers or ACIA registers.

### Board control and status registers

The software uses board control register to control general board functions. The board status register sends the status of the different board functions to the software.

### Asynchronous communications interface adapter

The SP instructs the ACIA to perform a two–way conversion. The ACIA converts the 8–bit parallel data to a half–duplex modem transmission protocol.

### RS232 or RS423 interface

The RS232 or RS423 interface provides a connection between the ACIA transistor–transistor–logic (TTL) level signals and the EIA transmission protocol signals. The signals are for transmission and reception over remote lines.

The pin numbers for the NTCX50AA appear in the following figure.

## Technical data

### Power requirements

The NTCX50AA requires a voltage of +5V and current of 50 mA.

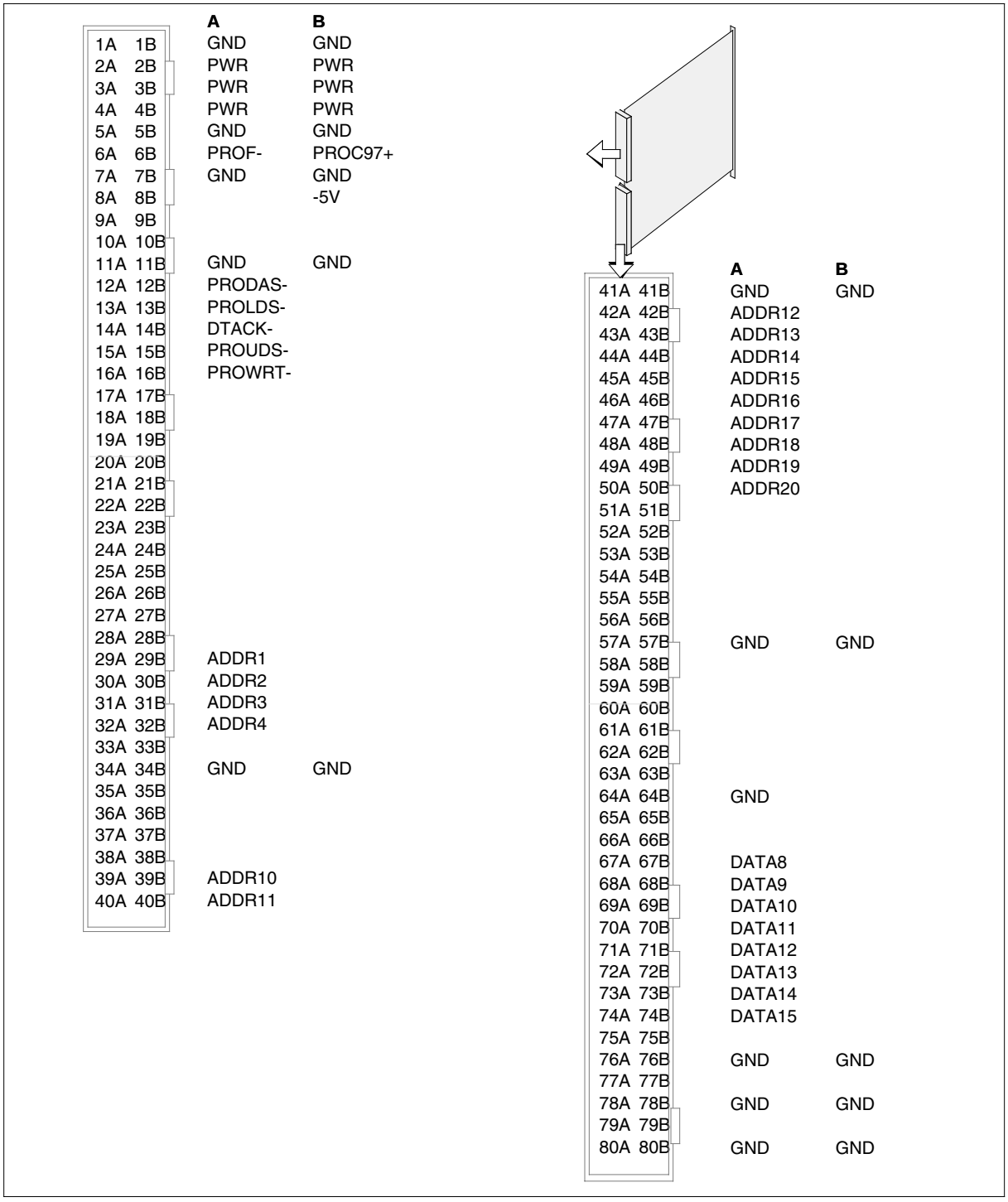
## Signaling

### Pin numbers

The NTCX50AA ECC derives the +5V supply from 6 backplane pins. Twenty–one separate pins provide grounding.

# **NTCX50AA** (end)

### NTCX50AA pin numbers



# NTCX50AB

## Product description

The NTCX50AB echo canceller control (ECC) card is an interface between the following:

- the extended multiprocessor system (XMS)-based peripheral module (PM) (XPM)
- external original equipment manufacturer (OEM) echo cancellers

The NTCX50AB can control a maximum of 16 2-Mbit/s echo canceller modules.

The NTCX50AB has the following features:

- the RS-232 transmission protocol without handshaking protocol
- software control of card operation
- use in a polled or interrupt-driven environment
- on-board control and status registers
- hardware and software board reset
- a 64-character transmission and reception
- diagnostic capabilities, like looparound of RS-232 data
- the RS-232 lines electrically isolated from card power and ground

A duplicate of the NTCX50AB is in each unit of the PCM30 digital trunk controller (PDTC) in an active-standby configuration.

The NTCX50AB is backwards compatible with the NTCX50AA.

### Location

The NTCX50AB is in slot 19, behind the NT6X28AC signaling interface card, on the backplane of the XPM plus peripheral module.

## Functional description

The NTCX50AB allows the XPM plus processor (unified processor) to control echo canceller equipment from a distance. The processor uses an Electronic Industries Association (EIA) RS-232C transmission link to control the equipment. Software in the XPM reads from and writes to the control and status registers on the ECC. A universal asynchronous receiver and transmitter (UART) communicates with the echo cancellers. One ECC can control a maximum of 16 2-Mbit/s echo canceller modules.

## **NTCX50AB** (continued)

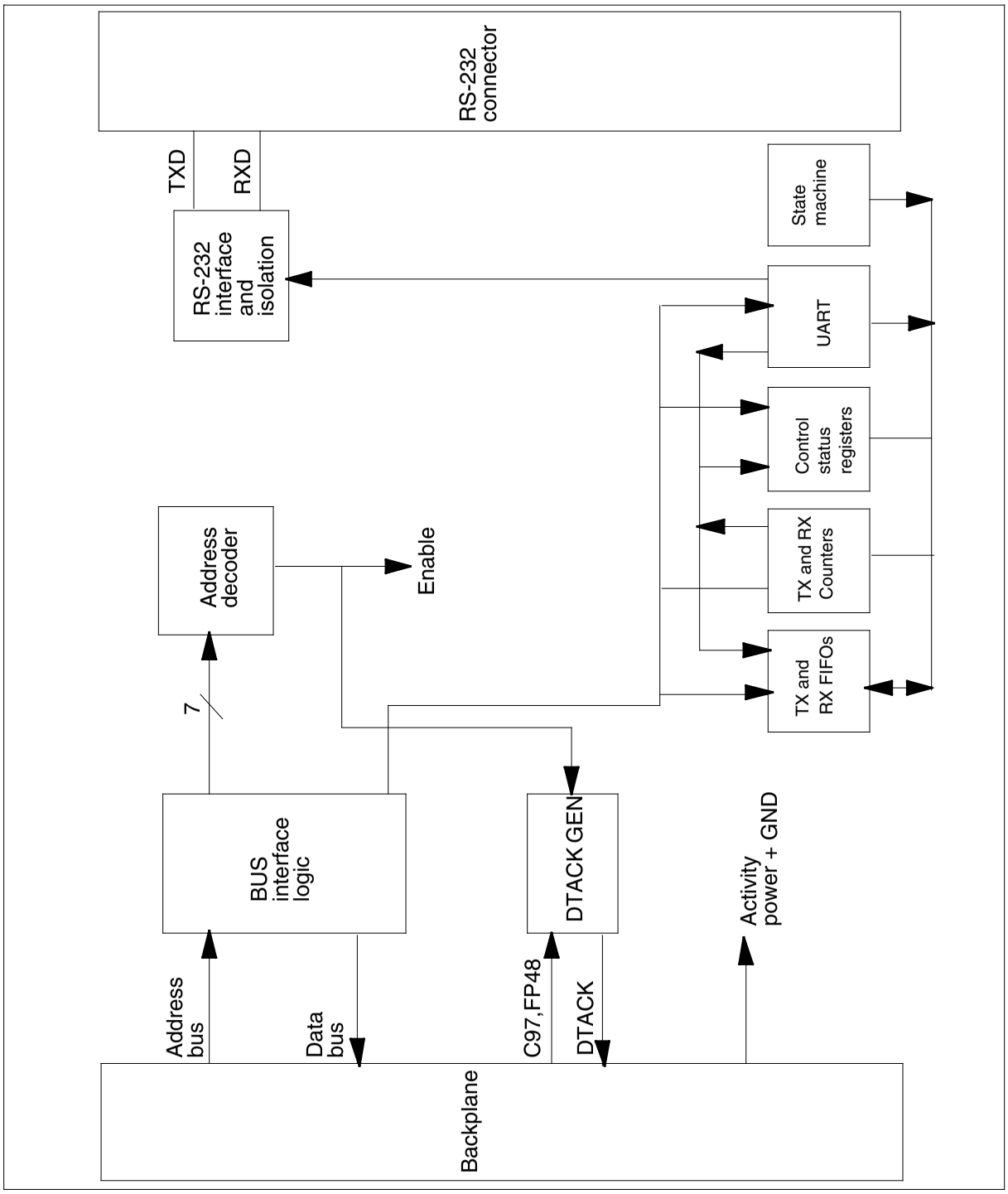
### Functional blocks

The NTCX50AB has the following functional blocks:

- bus interface logic
- transmit first-in-first-out (FIFO) memory
- receive FIFO
- address decode logic
- board control and status registers
- asynchronous communications interface adapter (ACIA)
- the RS232 interface

The relationship between the functional blocks appears in the following figure.

**NTCX50AB functional blocks**



## NTCX50AB (continued)

### Bus interface logic

The bus interface logic connects the PDTC backplane signals to the board signals. The bus interface logic uses tristate buffers on the processor address and data buses for the connection.

### Transmit FIFO memory

The transmit FIFO memory is a 64 byte memory that stores bytes. The MX77 processor generates the bytes that go to the ACIA.

### Receive FIFO memory

The receive FIFO memory is a 64 byte memory that stores bytes. The ACIA generates the bytes that go to the MX77 processor.

### Address decode logic

The address decode logic selects board registers or ACIA registers.

### Board control and status registers

The software uses the board control register to control general board functions. The board status register sends the status of the different board functions to the software.

### Asynchronous communications interface adapter

The MX77 processor instructs the ACIA to perform a two-way conversion. The ACIA converts the 8-bit parallel data to a half-duplex modem transmission protocol.

### RS232 interface

The RS232 interface provides a connection between the ACIA transistor-transistor-logic (TTL) level signals and the EIA transmission protocol signals. These signals are for transmission and reception over remote lines.

## Technical data

### Power requirements

The NTCX50AB requires a voltage of +5V and current of 700 mA.

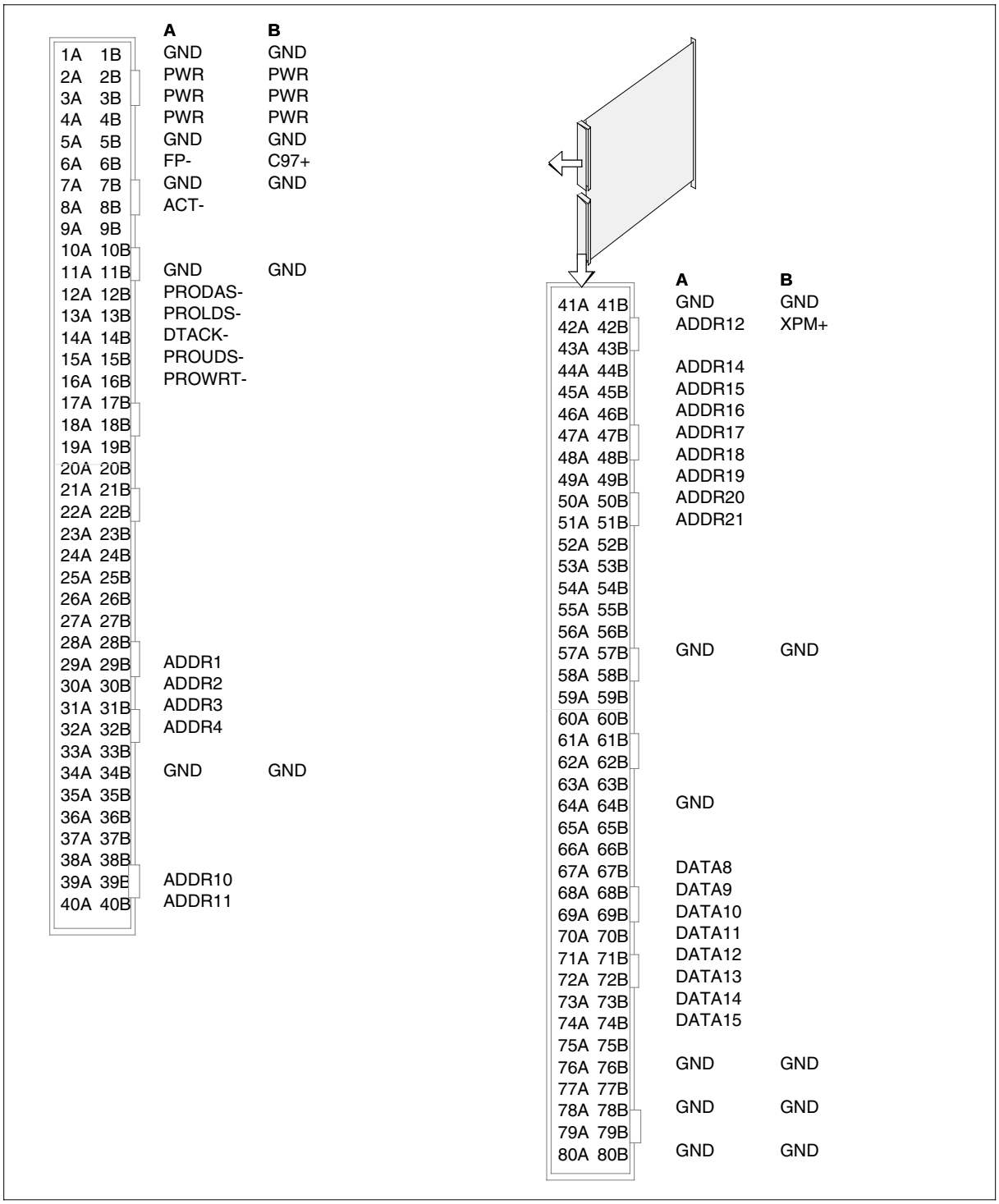
## Signaling

### Pin numbers

The NTCX50AB ECC derives the +5V supply from six backplane pins. Twenty-one separate pins provide the grounding.

The pin numbers for the NTCX50AB appear in the following figure.

### NTCX50AB pin numbers



# NTCX50BA

## Product description

The NTCX50BA echo canceller control (ECC) card is a paddleboard designed specifically for the CPM-based DTC02 platform used in GPP market applications. The primary function of the card is to enable the shelf processor (ie. the Unified MX77 Processor) to remotely control external echo cancellers via an EIA RS-232E transmission link. The design of the NTCX50BA is based on that of the NTCX50AB card, with a change to the addressing range to accommodatethe different GPP/CPM module requirements. This change effectively resolves an addressing conflict between the NTCX50AB and the NTMX76CA cards.

The NTCX50BA card has two added straps but is otherwise is identical to NTCX50AB. Consequently, NTCX50BA has the following features:

- the RS-232 transmission protocol without handshaking protocol
- software control of card operation
- use in a polled or interrupt-driven environment
- on-board control and status registers
- hardware and software board reset
- a 64-character transmission and reception
- diagnostic capabilities, like looparound of RS-232 data
- the RS-232 lines electrically isolated from card power and ground

### Location

The NTCX50BA paddleboard mounts on the rear of the Global Tone Receiver cards at positions 6R and 22R of the DTC02. This card may be used when slot 5/23 is filled by NT0X50AA or STR only.

## Functional description

The NTCX50BA meets the 150000-15FFFF address range in the CPM peripheral. This card does not recognise the XPM address range (1C0000-1CFFFF) and the XPM+ address range (1B0000-1BFFFF) and consequently cannot replace the NTCX50AA or NTCX50AB in the XPM/XPM+.

### Functional blocks

The NTCX50BA is identical to the NTCX50AB from a functional block diagram perspective. NTCX50BA has the following functional blocks:

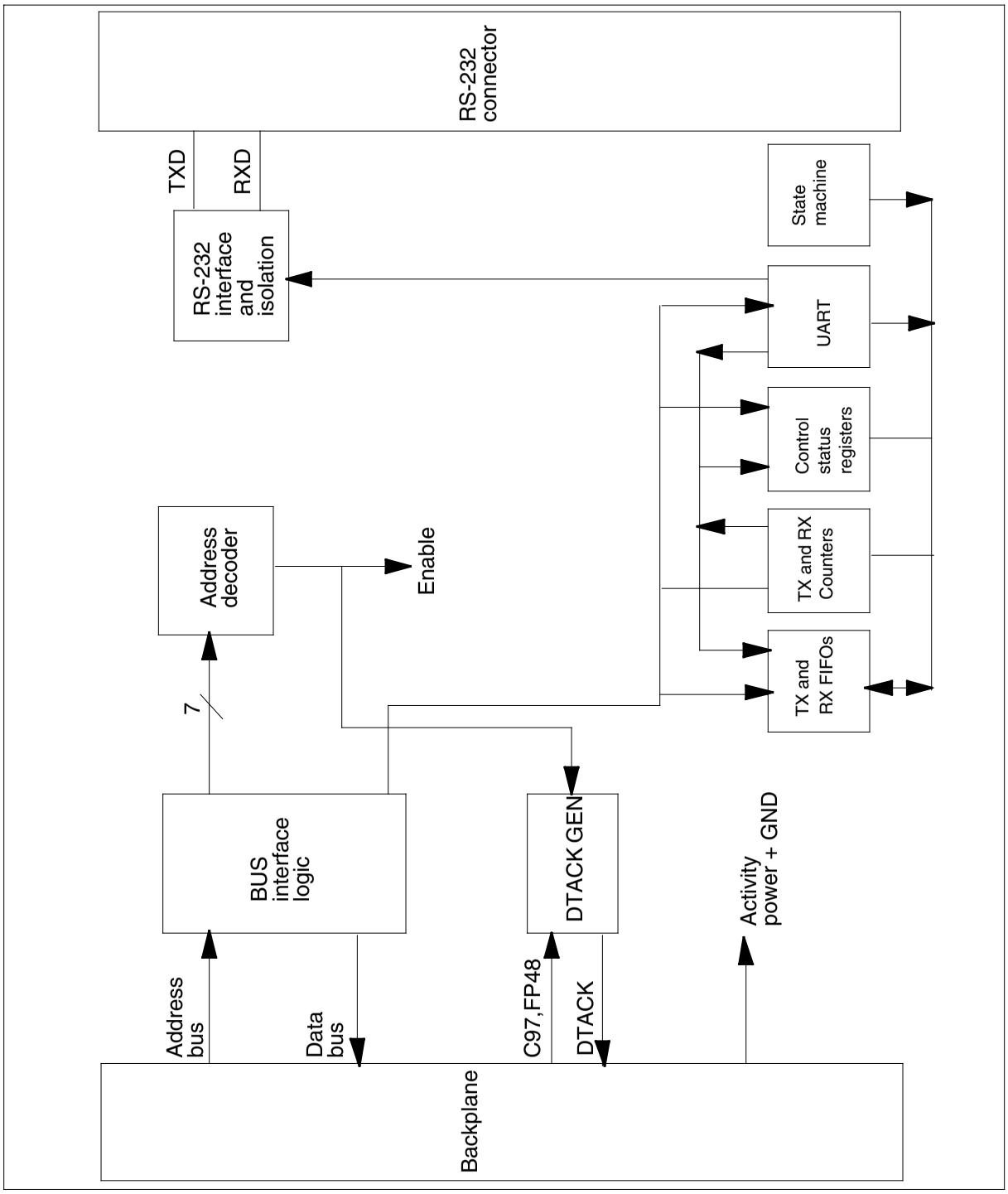
- bus interface logic
- transmit first-in-first-out (FIFO) memory

- receive FIFO
- address decode logic
- board control and status registers
- asynchronous communications interface adapter (ACIA)
- the RS232 interface

The relationship between the functional blocks appears in the following figure.

## NTCX50BA (continued)

### NTCX50BA functional blocks



### Bus interface logic

The bus interface logic connects the PDTC backplane signals to the board signals. The bus interface logic uses tristate buffers on the processor address and data buses for the connection.

### Transmit FIFO memory

The transmit FIFO memory is a 64 byte memory that stores bytes. The MX77 processor generates the bytes that go to the ACIA.

### Receive FIFO memory

The receive FIFO memory is a 64 byte memory that stores bytes. The ACIA generates the bytes that go to the MX77 processor.

### Address decode logic

The address decode logic selects board registers or ACIA registers.

### Board control and status registers

The software uses the board control register to control general board functions. The board status register sends the status of the different board functions to the software.

### Asynchronous communications interface adapter

The MX77 processor instructs the ACIA to perform a two-way conversion. The ACIA converts the 8-bit parallel data to a half-duplex modem transmission protocol.

### RS232 interface

The RS232 interface provides a connection between the ACIA transistor-transistor-logic (TTL) level signals and the EIA transmission protocol signals. These signals are for transmission and reception over remote lines.

## Technical data

### Power requirements

The NTCX50BA requires a voltage of +5V and current of 700 mA.

## Signaling

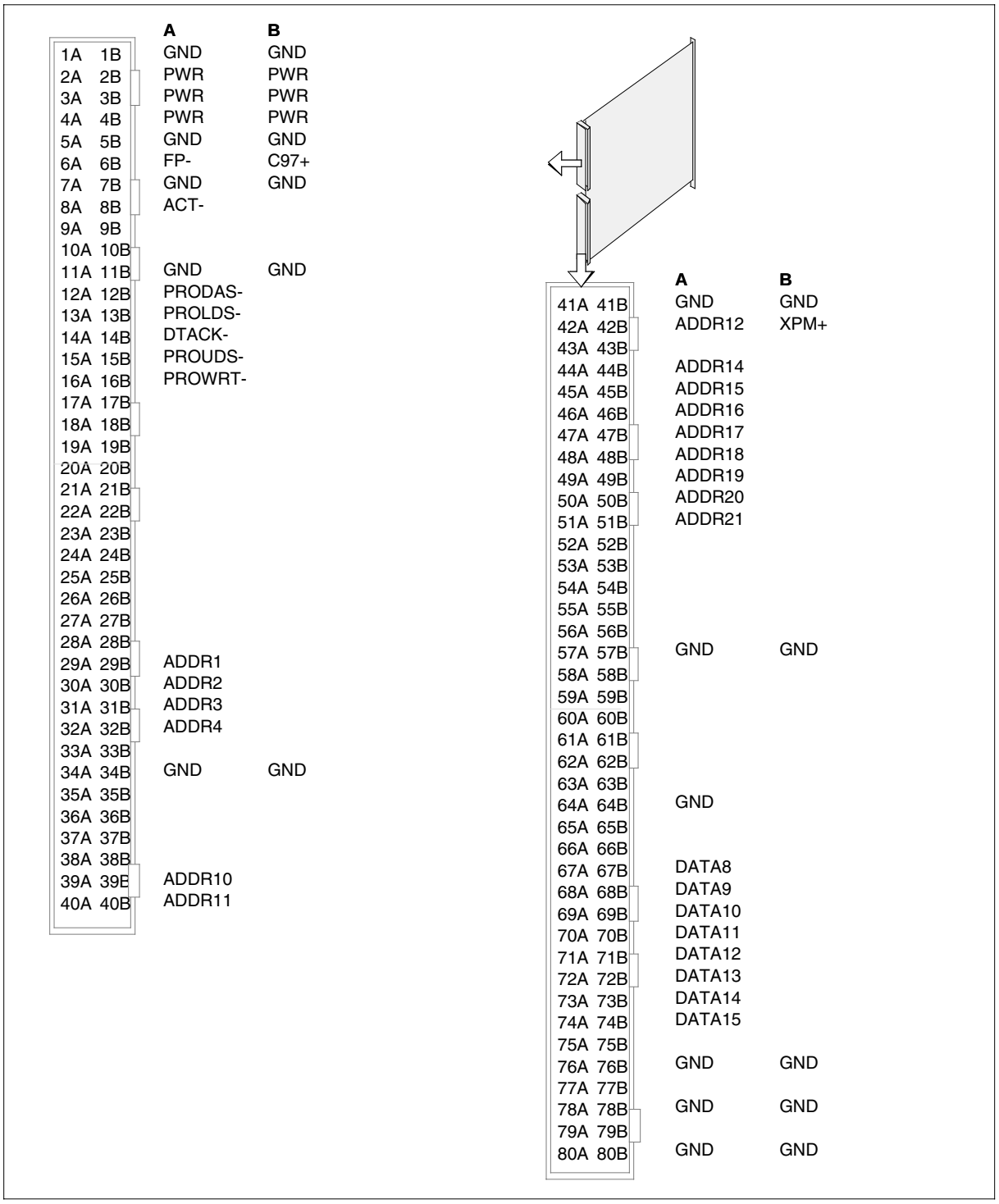
### Pin numbers

The NTCX50BA ECC derives the +5V supply from six backplane pins. Twenty-one separate pins provide the grounding.

The pin numbers for the NTCX50BA appear in the following figure.

# **NTCX50BA** (end)

### NTCX50BA pin numbers



# 5 NTDXnnaa

## NTDX15AA through NTDX15AB

# NTDX15AA

## Product description

The NTDX15AA provides a nominal ±5V to the following DMS–100 SuperNode products:

- high–speed interface (HSI)
- network programming platform (NPP)
- channel frame processor (CFP)

Each NTDX15AA uses a frame supervisory panel (FSP) to interface with DMS–100 office alarm circuits.

## Functional description

The NTDX15AA provides a regulated and protected nominal output of +5.15V and -5.2V.

The negative output load determines the maximum current available on the positive output. You cannot draw a maximum of 69A from the positive rail for a load. You can draw a maximum of 55A from the positive rail at -10A.

### Functional blocks

The NT9X91AA consists of the following functional blocks:

- inrush current limit
- input filter
- primary power switch
- current mode controller
- auxiliary power supply
- automatic recovery from low battery (ARLB)
- identification (ID) PROM
- switch and control relay light–emitting diodes (LED)
- QMS142A power supply monitor
- current sense transformer
- power transformer
- rectifier and filter

### Inrush current limit

The inrush current limit is approximately 3A when the converter is first plugged in, or power is removed and applied again.

### Input filter

The input filter provides common and differential mode filtering for the switching power train.

### Primary power switch

The power switch, that consists of two switching field–effect transistors (FET) configured for push–pull operation, chops the output of the input filter.

### Current mode controller

The NT5L57AA current mode controller controls the two switching FETs.

### Auxiliary power supply

An NT5L35AA hybrid provides the auxiliary power for the control circuits.

### Automatic recovery from low battery

The ARLB allows the converter to recover from a loss of input power if the converter operates when the power is lost.

### Identification PROM

The ID PROM allows the system software to determine the type and release of the power supply.

### Switch and control relay light–emitting diodes

The NT9X91AA has a faceplate on/off switch and a faceplate power converter fail LED. The NT9X91AA has a provision for a remote switch and remote fail LED. Relays are provided for remote start, remote stop, and remote alarm signaling.

### QMS142A power supply monitor

The QMS142A power supply monitor checks for low voltage and overvoltage on the two outputs of the supply. If the monitor detects a low voltage or an overvoltage, the monitor shuts down the converter.

### Current sense transformer

The current sense transformer provides current information to the hybrid, that regulates the output voltage.

### Power transformer

The power transformer steps down the ac waveform by a fixed ratio to provide the voltage for the regulated output. The switching action of the FETs generates the ac waveform.

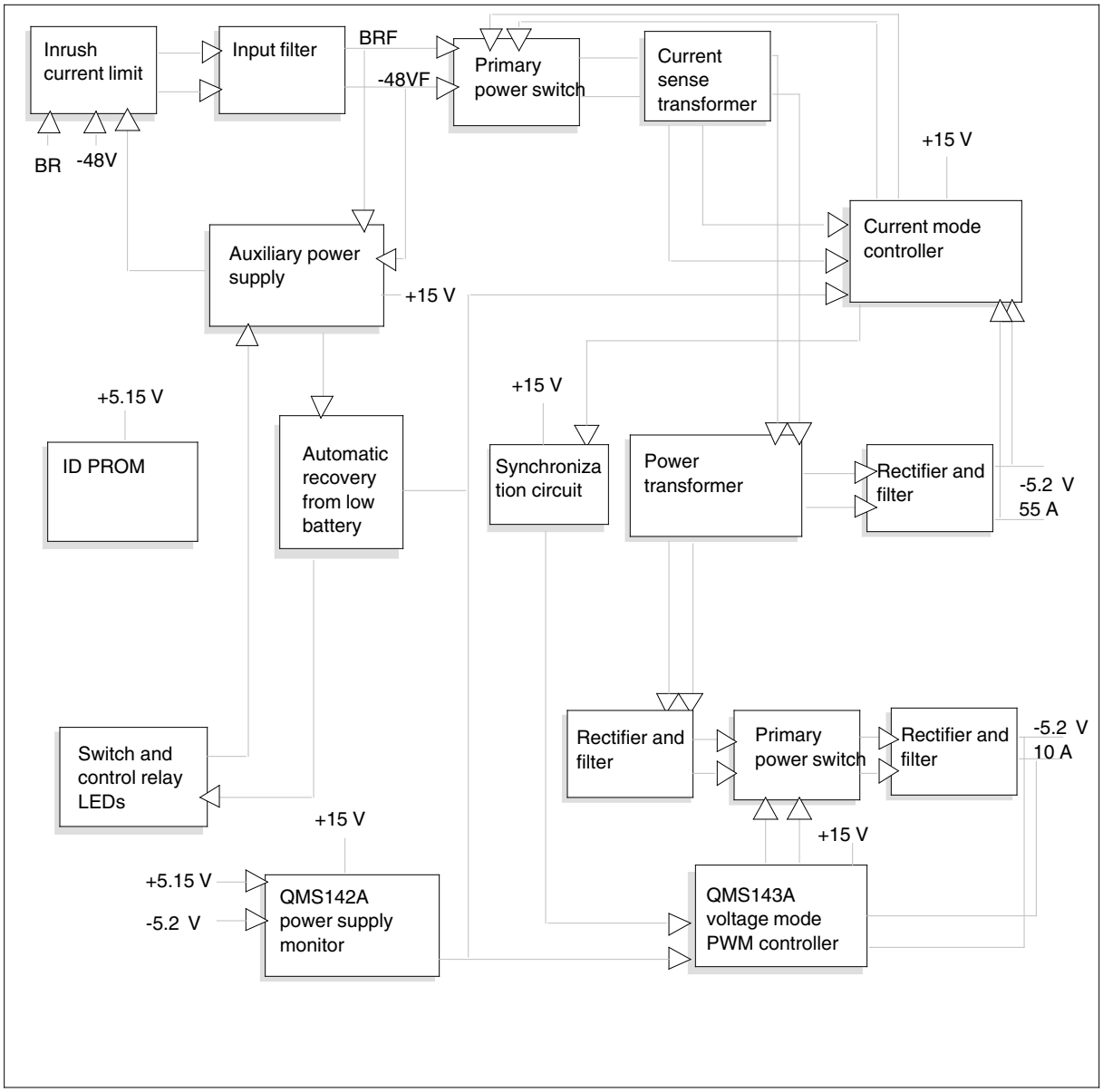
# **NTDX15AA** (continued)

## Rectifier and filter

The rectifier and filter regulate the ac waveform with a set of fullwave diodes and an inductor and capacitator (LC) filter.

The relationship between the functional blocks appears in the following figure.

**NTDX15AA functional blocks**



# Signaling

## Pin numbers

The pin numbers for the NTDX15AA appear in the following table. The explanations for the abbreviations are:

- address (A)
- data (D)
- chip select (CS)
- ring alarm sense (RAS)
- no converter (NOCON)
- no connection on the backplane but the converter has a signal on this pin (N/C)
- shutdown (SD)
- power lock–on converter (PLOCK)
- remote start converter (REM.START)
- remote shutdown converter (REM.SHDN)

**Connector P1 (Sheet 1 of 2)**

| Row | Column Z | Column B | Column D | Column F |
|---|---|---|---|---|
| 2 | N/C | SD | CS-5 | EXT.SW.OFF |
| 4 | A2-5 | A1-5 | A0-5 | A3-5 |
| 6 | D6-5 | D5-5 | D4-5 | D7-5 |
| 8 | D2-5 | D1-5 | D0-5 | D3-5 |
| 10 | EXT.SW.ON | RAS-NC | RAS-C | EXT.SW |
| 12 | BR.ABS | -48VABS | EXT.LED | RAS-NO |
| 14 | NOCON | -5SENSE | N/C | NOCON |
| 16 | -5V | -5V | -5V | -5V |
| 18 | GND | GND | GND | GND |
| 20 | -5V | -5V | -5V | -5V |
| 22 | GND | GND | GND | GND |

## **NTDX15AA** (continued)

**Connector P1 (Sheet 2 of 2)**

| Row | Column Z | Column B | Column D | Column F |
|---|---|---|---|---|
| 24 | +5V | +5V | +5V | +5V |
| 26 | GND | GND | GND | GND |
| 28 | +5V | +5V | +5V | +5V |
| 30 | GND | GND | GND | GND |
| 32 | +5V | +5V | +5V | +5V |

**Connector P2**

| Row | Column Z | Column B | Column D | Column F |
|---|---|---|---|---|
| 2 | GNDSENSE | GNDSENSE | GND | GND |
| 4 | +5V | +5V | +5V | +5V |
| 6 | GND | GND | GND | GND |
| 8 | +5V | +5V | +5V | +5V |
| 10 | GND | GND | GND | GND |
| 12 | +5V | +5V | +5V | +5V |
| 14 | GND | GND | GND | GND |
| 16 | +5V | +5V | +5V | +5V |
| 18 | GND | GND | GND | GND |
| 20 | +5V | +5V | +5V | +5V |
| 22 | -48V | -48V | -48V | +5SENSE |
| 24 | -48V | -48V | -48V | -48V |
| 26 | BR | BR | BR | N/C |
| 28 | BR | BR | BR | BR |
| 30 | -5OUVTEST | +5OUVTEST | N/C | (+15V) |
| 32 | REM.START | REM.SHDN | (-48T) | PLOCK |

# Technical data

## Power requirements

### Input specifications

The nominal voltage is -48V, and ranges from a minimum of -42.0V to a maximum of -56V. The maximum current is 14A. The converter operates at the low–battery shutdown voltage (-38.0 ±0.75V). The converter must start at the low–battery recovery voltage (-41.0 ±0.5V).

### Output specifications

The output specifications for -5.2V appear in the following tables.

**-5.2V output**

| Parameter | Value |
|---|---|
| Voltage | -5.2 V ± 2% |
| High voltage shutdown | +6.5 V ± 0.5 V |
| Low voltage shutdown | -4.3 V ± 0.3 V |
| Ripple | 50 mV rms |
| Maximum current | 10 A |
| Minimum current | 0.5 A |
| Current limit | 13.0 A ± 2 A |

The output specifications for +5.15V appear in the following table.

**+5.15V output (Sheet 1 of 2)**

| Parameter | Value |
|---|---|
| Voltage | +5.15 V ± 2% |
| High voltage shutdown | +6.5 V ± 0.5 V |
| Low voltage shutdown | +4.3 V ± 0.3 V |
| Ripple | 50 mV rms |
| Maximum current | 69 A |

## **NTDX15AA** (end)

**+5.15V output (Sheet 2 of 2)**

| Parameter | Value |
|---|---|
| Minimum current | 5 A |
| Current limit | 73 A ± 3 A |

# NTDX15AB

## Product description

The NTDX15AB card provides a nominal ±;5V to the following DMS–100 SuperNode products:

- high–speed interface (HSI)
- network programming platform (NPP)
- channel frame processor (CFP)

### Location

Each NTDX15AB card uses a frame supervisory panel (FSP) to interface with the DMS–100 office alarm circuits.

## Functional description

The NTDX15AB card provides a regulated and protected nominal output of +5.15V and -5.2V. The card operates from -48V or -60V input battery voltage.

The negative output load determines the maximum current available on the positive output. A maximum of 69A cannot draw from the positive rail at a load. At -10A, a maximum of 55A can draw from the positive rail.

### Functional blocks

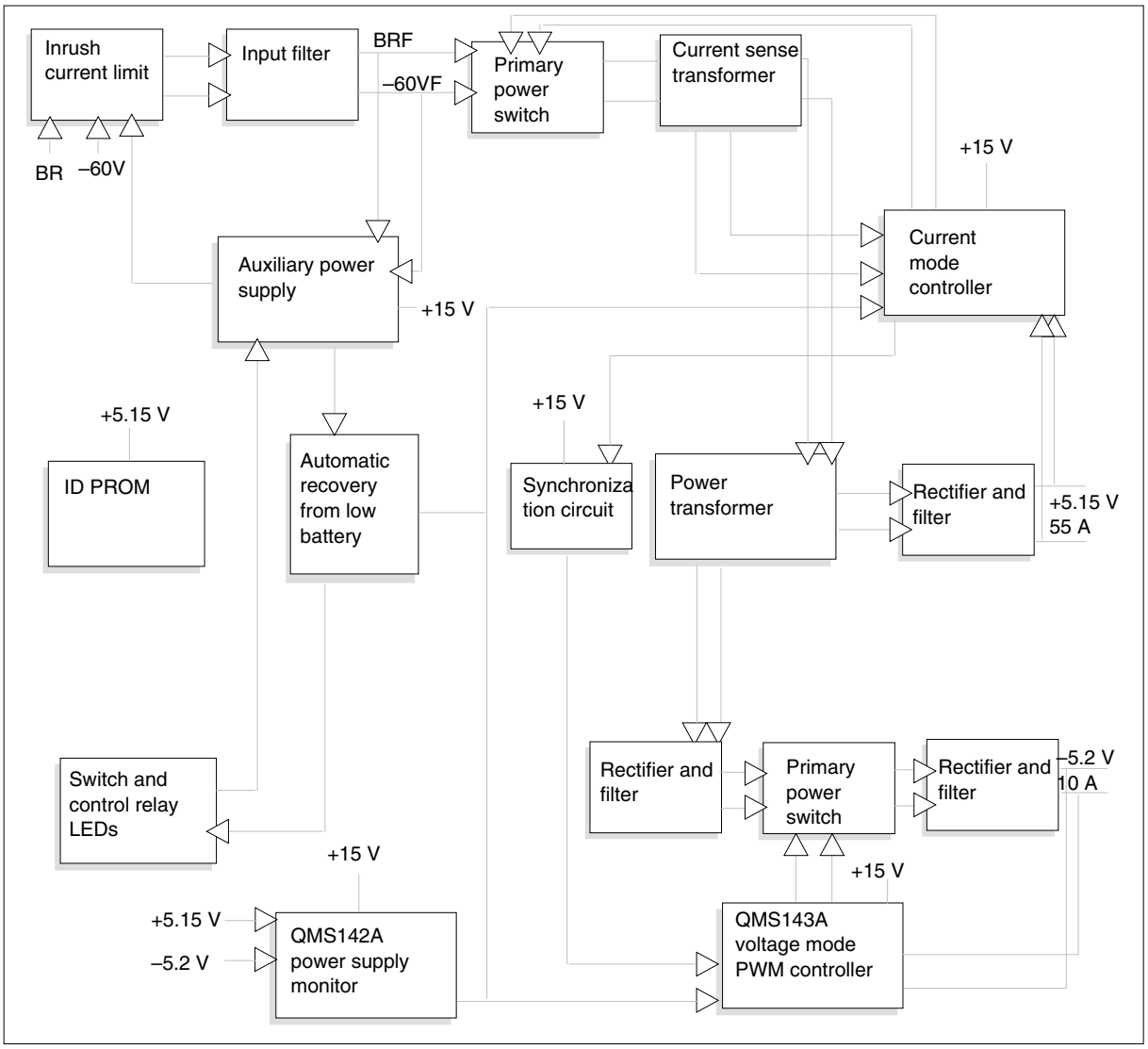
The NTDX15AB consists of the following functional blocks:

- inrush current limit
- input filter
- primary power switch and current mode controller
- auxiliary power supply and automatic recovery from low battery (ARLB)
- identification (ID) PROM
- switch and control relay light–emitting diodes (LED)
- output monitor
- secondary power switch, rectifier and control
- power transformer

The relationship between the functional blocks appears in the following table.

## **NTDX15AB** (continued)

### NTDX15AB functional blocks




### Inrush current limit

The inrush current limit is approximately 3.5A when the converter is first plugged in, or power is removed and applied again.

### Input filter

The input filter provides common and differential mode filtering for the switching power train.

### Primary power switch, current sense and control

The power switch chops the output of the input filter. The power switch consists of two switching field–effect transistors (FET) configured for push–pull operation. An NT5L57AA current–mode controller controls the two switching FETs. This hybrid controller regulates the output of +5V by direct feedback and by current information that the current–sense transformer provides.

### Auxiliary power supply and automatic recovery from low battery

An NTGL38AA hybrid provides the auxiliary power for the control circuits that an NT6L38AA hybrid provides. This hybrid provides an isolated and regulated output of +15.5V. This hybrid controls the automatic recovery from low battery (ARLB). The ARLB is a feature of the power supply. This feature allows the converter to recover from loss of input power if the converter operates when the power is lost.

### Identification PROM

The ID PROM allows the system software to determine the type and release of the power supply.

### Switch and control relay and light–emitting diodes

The NTDX15AB has a faceplate ON/OFF switch and a faceplate power converter fail LED. The NTDX15AB has a provision for a remote switch and remote fail LED. Relays are provided for remote start, remote stop, and remote alarm signaling.

### Output power supply monitor

The QMS142A power supply monitor checks for low voltage and overvoltage on the two outputs of the supply. If the monitor detects a low voltage or overvoltage, the monitor shuts down the converter.

### Power transformer

The power transformer processes the ac waveform in two outputs. The switching action of the FETs generates the ac waveform. The first output is a primary regulated output of approximately 8V peak–to–peak. The second output is an unregulated output of approximately 16V peak–to–peak. Each output is rectified and filtered.

### Secondary power switch, rectifier and control

Two power FETs chop the unregulated voltage from the power transformer. A current–sense transformer senses the source currents of the power FETs. This current sample is rectified. The system feeds the waveform that results to the input of the QMS143A voltage–mode controller. The controller uses the waveform to limit the output current.

## **NTDX15AB** (continued)

# Signaling

### Pin numbers

The pin numbers for the NTDX15AB appear in the following tables. The abbreviations used in the tables are:

- address (A)
- data (D)
- chip select (CS)
- ring alarm sense (RAS)
- no converter (NOCON)
- no connection on the backplane but the converter has a signal on this pin (N/C)
- shutdown (SD)
- power lock–on converter (PLOCK)
- remote start converter (REM.START)
- remote shutdown converter (REM.SHDN)

**Connector P1 (Sheet 1 of 2)**

| Pin | Z | B | D | F |
|---|---|---|---|---|
| 2 | N/C | SD | CS-5 | EXT.SW.OFF |
| 4 | A2-5 | A1-5 | A0-5 | A3-5 |
| 6 | D6-5 | D5-5 | D4-5 | D7-5 |
| 8 | D2-5 | D1-5 | D0-5 | D3-5 |
| 10 | EXT.SW.ON | RAS-NC | RAS-C | EXT.SW |
| 12 | BR.ABS | -48VABS | EXT.LED | RAS-NO |
| 14 | NOCON | -5SENSE | N/C | NOCON |
| 16 | -5V | -5V | -5V | -5V |
| 18 | GND | GND | GND | GND |
| 20 | -5V | -5V | -5V | -5V |
| 22 | GND | GND | GND | GND |

**Connector P1 (Sheet 2 of 2)**

| Pin | Z | B | D | F |
|---|---|---|---|---|
| 24 | +5V | +5V | +5V | +5V |
| 26 | GND | GND | GND | GND |
| 28 | +5V | +5V | +5V | +5V |
| 30 | GND | GND | GND | GND |
| 32 | +5V | +5V | +5V | +5V |

**Connector P2**

| Pin | Z | B | D | F |
|---|---|---|---|---|
| 2 | GNDSENSE | GNDSENSE | GND | GND |
| 4 | +5V | +5V | +5V | +5V |
| 6 | GND | GND | GND | GND |
| 8 | +5V | +5V | +5V | +5V |
| 10 | GND | GND | GND | GND |
| 12 | +5V | +5V | +5V | +5V |
| 14 | GND | GND | GND | GND |
| 16 | +5V | +5V | +5V | +5V |
| 18 | GND | GND | GND | GND |
| 20 | +5V | +5V | +5V | +5V |
| 22 | -48V | -48V | -48V | +5SENSE |
| 24 | -48V | -48V | -48V | -48V |
| 26 | BR | BR | BR | N/C |
| 28 | BR | BR | BR | BR |
| 30 | -5OUVTEST | +5OUVTEST | N/C | (+15V) |
| 32 | REM.START | REM.SHDN | (-48T) | PLOCK |

## **NTDX15AB** (end)

# Technical data

### Power requirements

#### Input

The nominal voltage is -48V and ranges from a minimum of -42V to a maximum of -71V. The maximum current is 14 A. The converter operates at the low–battery shutdown voltage, -38.25V ± 1.25V. The converter must start at the low–battery recovery voltage, -41 ± 1.5V.

#### Output

The output specifications for the -5.2V output appear in the following table.

**-5.2V output**

| | |
|---|---|
| Voltage | -5.2 V ± 2% |
| High voltage shutdown | +6.5 V ± 0.5 V |
| Low voltage shutdown | -4.3 V ± 3 V |
| Ripple | 50 mV rms |
| Maximum current | 10 A |
| Minimum current | 0 A |
| Current limit | 13.0 A ± 2 A |

The output specifications for the +5.15 V output appear in the following table.

**+5.15V output**

| | |
|---|---|
| Voltage | +5.15 V ± 2% |
| High voltage shutdown | +6.5 V ± 0.5 V |
| Low voltage shutdown | +4.3 V ±0.3 V |
| Ripple | 50 mV rms |
| Maximum current | 69 A |
| Minimum current | 5 A |
| Current limit | 74 A ± 4 A |

# NTDX16AA

## Product description

The NTDX16AA power converter provides a nominal ±5V to the LIS shelf of the Link Peripheral Processor (LLP) in a DMS–100 system.

## Functional description

The NTDX16AA provides a regulated and protected nominal output of +5.15V and -5.2V.

The negative output load determines the maximum current available on the positive output. You cannot draw a maximum of 5A from the positive rail. You can draw a maximum of 91A from the positive -10A rail.

### Functional blocks

The DSDX16AA has the following functional blocks:

- inrush current limit
- input filter
- primary power switch
- current mode controller
- auxiliary power supply
- identification (ID) PROM
- switch and control relay light-emitting diodes (LED)
- QMS142A power supply monitor
- current sense transformer
- power transformer
- rectifier and filter
- Output over voltage and under voltage shutdown

### Inrush current limit and filter

Surge suppression is provided by a MOV across the input. A common-mode electromagnetic interference (EMI) filter is provided to reduce converter generated noise fed back to the source. A differential-mode filter is also provided to reduce switching noise. The inrush current upon startup is limited by a thermistor. A capacitive bank provides switching current to the power switch.

### Primary power switch

The power switch is configured in a current-mode-controlled push-pull topology, with the control loop closed around the +5V output. The -5V output

## **NTDX16AA** (continued)

is regulated by a push-push buck post-regulator.

### Current mode controller

The NT5L57AA current mode controller controls the two switching FETs.

### Auxiliary power supply

The control and monitor circuits are powered by the NT6L38AA auxiliary supply module producing a nominal +15.5V isolated from the input line.

### Automatic recovery from low battery (ARLB)

The NT6L38AA Auxiliary Supply Module contains an ARLB function which senses input voltage and signals the PWM to shut down the converter when the input voltage falls below the minimum specified operating level. When the input voltage rises above the minimum startup level, ARLB boots the PWM to allow automatic restart. Manual turn-off of the converter or automatic turn-off due to a fault condition in the converter disables the ARLB function and restart must be initiated manually.

### Identification PROM

The ID PROM allows the system software to determine the type and release of the power supply.

### Switch and control relay light-emitting diodes

The DSDX16AA has a faceplate on/off switch and a faceplate power converter fail LED. The DSDX16AA has a provision for a remote switch and remote fail LED. Relays are provided for remote start, remote stop, and remote alarm signaling.

### QMS142 power supply monitor

The QMS142A power supply monitor checks for low voltage and over voltage on the two outputs of the supply. If the monitor detects a low voltage or an over voltage, the monitor shuts down the converter.

### Current sense transformer

The current sense transformer provides current information to the hybrid, that regulates the output voltage.

### Power transformer

The power transformer steps down the ac waveform by a fixed ratio to provide the voltage for the regulated output. The switching action of the FETs generates the ac waveform.

### Rectifier and filter

The rectifier and filter regulate the ac waveform with a set of fullwave diodes

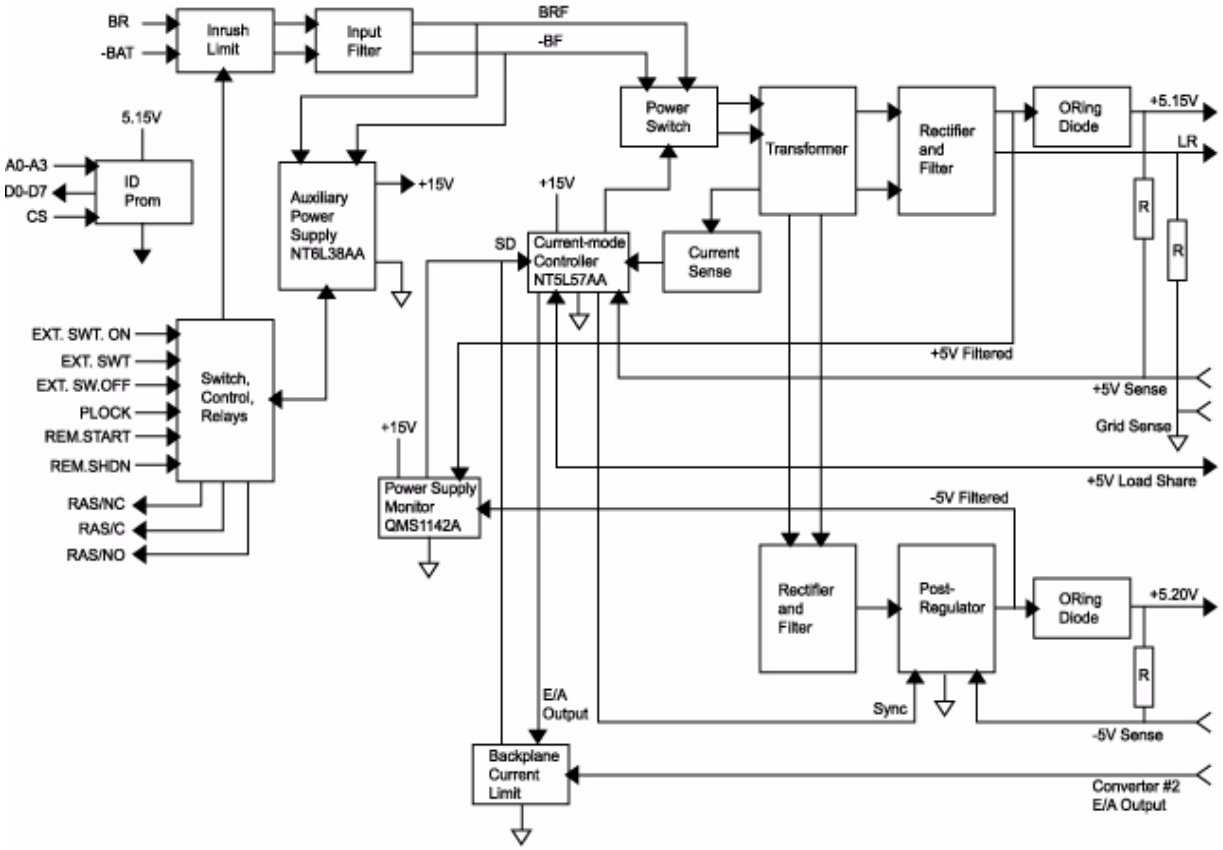
and an inductor and capacitator (LC) filter.

### Output over voltage and under voltage shutdown

An output over voltage/under voltage shutdown feature is provided on both outputs. If the regulated output voltage rises above a maximum threshold or falls below a minimum threshold, a signal is sent by the monitor circuit to the pulse width moderator to shut down the converter. Restart from this type of fault-induced shutdown must be done manually.

### NTDX16AA functional block diagram

**NTDX16AA functional blocks**




## Signaling

The NTDX16AA interfaces indirectly to the NT9X2802 power backplane via the NT9X2825 Parallel Interface Unit. The PIU routes the signals from the output connectors of the two redundant converters to connectors on the NT9X2802 power backplane. The PIU also provides the necessary

## **NTDX16AA** (continued)

communication links between the two converters to allow for active load sharing, backplane current limiting, and PLOCK control.

### Pin numbers

The pin numbers for NTDX16AA appear in the following table.

| Signal name | Pin number | Signal name | Pin number |
|---|---|---|---|
| -5 SENSE | P1-14B | EXT.SW.ON | P1-24F |
| -5V | P1-18D,B,F | EXT.SWT | P1-20D |
| | P1-16F | EXT.LED | P1-22D |
| +5 | P1-14D,F | -ABS | P1-22B |
| | P1-10D,B,Z,F | BR.ABS | P1-22Z |
| | P1-6D,B,Z,F | RAS/NO | P1-22F |
| | P1-2D,B,Z,F | NOCON-A | P1-20Z |
| | P2-30D,B,Z,F | NOCON-B | P1-20F |
| | P2-26D,B,Z,F | EAOUT | P2-12D |
| | P2-22D,B,Z,F | EAIN | P2-12B |
| P2-12Z | P2-18D,B,Z,F | +15 | P2-12Z |
| | P2-16D,F | REM.SHDN | P2-2B |
| +5 SENSE | P2-14F | REM.START | P2-2Z |
| LR | P1-16D,B,Z | -BAT | P2-6Z |
| | P1-14Z | | P2-8D,B,Z,F |
| | P1-12D,B,Z,F | | P2-10D,B,F |
| | P1-8D,B,Z,F | BR | P2-2F |
| | P1-4D,B,Z,F | | P2-4D,B,Z,F |
| | P2-32D,F | | P2-6D,B,F |
| | P2- 28D,B,Z,F | +5VTEST | P2-14B |
| | P2-24D,B,Z,F | -5VTEST | P2-14Z |
| | P2-20D,B,Z,F | EXT.SW.OFF | P1-20B |

| Signal name | Pin number | Signal name | Pin number |
|---|---|---|---|
| | P2-16B,Z | RAS/C | P1-24D |
| GNDSENSE | P2- 32Z,B | RAS/NC | P1-24B |
| ISHARE | P1-32Z | SD | P1-32B |
| -BT | P2-2D | PLOCK | P2-14D |

### Firmware interface

All packs in the DMS-100 family have a 32-byte IDPROM which contains 16 bytes of information identifying card type and vintage. The NT PEC code, pack release, and vintage are stored as outlined below. A checksum occupies the remaining two bytes.

| | | | | | | | | | PROM contents | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Addr** | **D07** | **D06** | **D05** | **D04** | **D03** | **D02** | **D01** | **D00** | **HEX** | **ASCII** |
| 0 | FMT | | | | | | STR | | 01 | |
| 1 | 0 | 0 | 0 | 0 | BLK | | | | 01 | |
| 2 | PEC | | | | | | | | 4E | N |
| 3 | | | | | | | | | 54 | T |
| 4 | | | | | | | | | 44 | D |
| 5 | | | | | | | | | 58 | X |
| 6 | | | | | | | | | 31 | 1 |
| 7 | | | | | | | | | 36 | 6 |
| 8 | | | | | | | | | 41 | A |
| 9 | | | | | | | | | 41 | A |
| 10 | REL | | | | | | | | 30 | 0 |
| 11 | | | | | | | | | 30 | 0 |
| 12 | VIN | | | | | | | | 30 | 0 |
| 13 | | | | | | | | | 31 | 1 |

## **NTDX16AA** (continued)

| | | | | | | | | | PROM contents | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Addr** | **D07** | **D06** | **D05** | **D04** | **D03** | **D02** | **D01** | **D00** | **HEX** | **ASCII** |
| 14 | FILL (CHECKSUM) | | | | | | | | 1A | |
| 15 | | | | | | | | | 25 | |

Where:

| | |
|---|---|
| BLK | Block field - defines the number of logical blocks in the PEC |
| FILL | Fill field = 1D0F - sum [Addr. 0-13] |
| FMT | Format field - must be 0 for all DMS-100 type products |
| PEC | ASCII representation of the 8-character NT PEC code |
| REL | Release field - ASCII pack release number - '00' for first release to NT |
| STR | Stride field - defines the processor access type - '01' for 16-bit word Access |
| VIN | Vintage field - starts at '01' |

# Technical data

## Power requirements

### Input specifications

The nominal voltage is -48V, and ranges from a minimum of -39.5V to a maximum of -75V. The maximum current is 18A. The converter operates at the low–battery shutdown voltage (-38.2 ±1.0V). The converter must start at the low–battery recovery voltage (-40.7 ±1.1V). The noise to the battery is a maximum of 3.9mV rms, or a maximum of 10dB rnc.

### Output specifications

The output specifications for +5.2V appear in the following table:

**+5.2V output**

| Parameter | Value |
|---|---|
| Voltage | +5.15V ± 2% |
| High voltage shutdown | 5.8V ± 0.5V |
| Low voltage shutdown | 4.3V ± 0.3V |
| Ripple | 50 mV rms |

**+5.2V output**

| Parameter | Value |
|---|---|
| Maximum current | 91 A |
| Minimum current | 0 A |
| Current limit | 102 A ± 7 A |

The output specifications for -5.2V appear in the following table:

**-5.2V output**

| Parameter | Value |
|---|---|
| Voltage | -5.2V ± 2% |
| High voltage shutdown | -5.8V ± 0.5V |
| Low voltage shutdown | -4.3V ± 0.3V |
| Ripple | 50 mV rms |
| Maximum current | 5 A |
| Minimum current | 0 A |
| Current limit | 7 A ± 1A |

# 6 NTEXnnaa

## NTEX01AB through NTEX78AA

# NTEX01AB parts

## Product description

The NTEX01AB parts fiberized link interface shelf (FLIS) cabinet is the standard DMS SuperNode cabinet. The NTEX01AB parts cabinet contains a maximum of two link interface shelves (LIS). Twenty-four link interface units (LIU7) can connect directly to the message switch (MS). The LIU7 can connect to the MS without a link interface module (LIM) cabinet and local message switch (LMS) shelves.

The figure on page 4 describes a standard FLIS configuration with one fully equipped shelf that occupies shelf position 26. A maximum of 12 LIU7s can be provisioned for each shelf with the left-most LIU7. This LIU7 occupies slots 8F, 9F and 9R. The right-most LIU7 occupies slots 30F, 31F and 31R. Each LIU7 contains two cards and one paddle board. The first card is the NTEX22AA integrated processor and frame transport bus (F-bus) interface. This card is in the even-numbered slots from 8F to 30F. The second card is the NT9X76AA signaling transfer point (STP) terminal. This card is in the next highest odd-numbered slot from 9F to 31F. The paddle board is an NT9X77AA V.35 interface or an NT9X78BA enhanced DS-0A interface, behind the NT9X76AA in the odd-numbered slots from 9R to 31R.

Empty shelf positions are provisioned with blank shelf assemblies for the forced-air cooling requirements of the cabinet. Shelf slots that are not used are filled with card NT9X19AA and paddle board filler face plates NT9X19BA. This action also fulfils the forced-air cooling requirements for the cabinet.

## Parts

The NTEX01AB parts FLIS cabinet contains the following parts:

- A0377580—core cooling unit, -48 V (dc)
- NT0X24BD—blank shelf assembly
- NT9X03AA—SuperNode frame supervisory panel (FSP)
- NT9X7204—link interface shelf
- NT9X72CA—link interface shelf common fill

### Core cooling unit

The A0377580 core cooling unit (CU) provides mechanical ventilation for equipment the FLIS cabinet contains.

### Blank shelf assembly

The NT0X24BD blank shelf fills shelf positions 00, 13 and 39 when one link interface shelf is used in position 26. If shelf positions 13 and 26 are full, NT0X24BD fills shelf positions 00 and 39.

### SuperNode frame supervisory panel

The NT9X03AA FSP provides alarm, maintenance and supervisory functions. The FSP is in the top shelf position in the NTEX01AB. Open the cabinet doors to access or view the front and rear faces of the NT9X03AA. The frame alarm light in the cabinet is visible with the cabinet doors closed.

Power from the power distribution center frame comes in the FSP. The FSP distributes the power to power supply modules in the cabinet. These modules include the NT9X30AA and NT9X31AA power converters. The power supply modules contain the power control. The power control is separate form the FSP.

### Link interface shelf

The NT9X7204 LIS assembly contains a maximum of 12 link interface units (LIU7).

The LIU7 is a peripheral module that processes messages that enter and leave the FLIS through a separate signaling data link.

When less than eight LIU7s are installed, NT9X19AA filler face plates and NT9X19BA filler paddle boards (PB) fill empty card and PB slots.

Each LIU7 consists of a set of cards and PBs, which are provisioned in one LIS of an FLIS.

If 13 to 24 LIU7s are required, two LISs in shelf positions 13 and 26 are used. These shelves are LIS1 and LIS2.

When more than 12 LIU7s are installed, NT9X19AA filler faceplates and NT9X19BA filler PBs fill the empty card and PB slots.

### Link interface shelf common fill

An NT9X72CA LIS common fill is provided for each NT9X7204 link interface shelf assembly.

The NT9X72CA LIS common CP contains a set of cards and paddle boards. These parts are provisioned in one LIS of a link peripheral processor (LPP):

- NTEX20AA—intrashelf paddle board
- NTEX20BA—intrashelf paddle board
- NT9X19BA—paddle board filler faceplate
- NT9X30AA—power converter, +5V card
- NT9X31AA—power converter, -5V card

## NTEX01AB parts (continued)

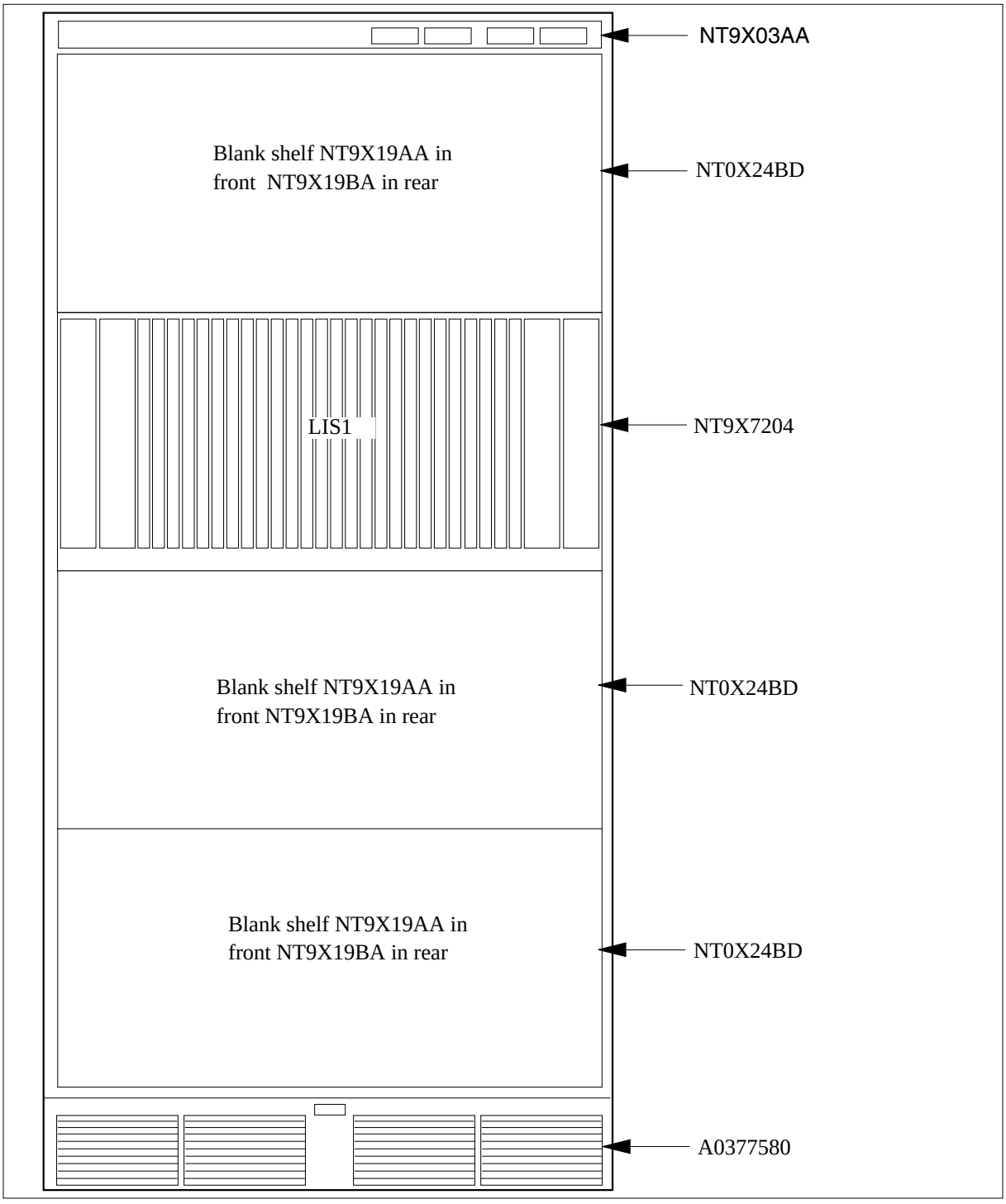
- NT9X96AA—LIS F-bus controller card
- NT9X98AA—LIS F-bus paddle board

## Design

The following figure describes the design of the NTEX01AB parts cabinet with one LIS. The LIU7s form a pair in different halves of the shelf with LIU7s assigned from the sides toward the center. The figure on page 5 illustrates the design of the NTEX01AB parts cabinet with two LISs. The LIU7s form a pair in opposite halves of different shelves. The LIU7s are assigned from the sides toward the center of each shelf.

## **NTEX01AB parts** (continued)

**NTEX01AB parts**



## **NTEX01AB parts** (end)

***Note:*** This diagram is not drawn to scale.

# NTEX17AA

## Product description

The NTEX17AA 1 Meg Modem Service (1MMS) line card provides for data networking as well as a plain ordinary telephone service (POTS) interface. The software controls transmission and signaling characteristics of the card, including loop current limit and automatic loss equalization.

### Location

The NTEX17AA occupies one card position in a line concentrating module (LCM) drawer.

## Functional description

### Functional blocks

The NTEX17AA has the following functional blocks for data:

- 64–QAM, 16–QAM, 4–QAM upstream and downstream interface to tip and ring
- downstream narrowband and wideband transmission
- dual downstream transmit levels
- power down modes
- synchronization to MCLK
- XLBUS interface to DBIC
- test port
- BERT port

The NTEX17AA has the following functional blocks for voice:

- supervisory block
- transmission block
- overvoltage protection
- overcurrent protection
- voltage regulator
- relays

## **NTEX17AA** (continued)

### Supervisory block

The supervisory block performs the following functions:

- loop detection
- ringing supervision
- loop current limiting

The network and the B11 chip monitor a loop current that flows through the transformer and the battery feed network. The B11 compares the output voltage of the amplifier with a software–selectable supervision threshold. The B11 chip determines if the line is on–hook or off–hook.

Two external low–pass filters and the loop detection comparator (in the B11 chip) provide ringing supervision.

The B11 chip in the NTEX17AA allows the software to select the loop current limit.

### Transmission block

The transmission block performs the following functions:

- generation of input impedances
- code and decode of voice signals
- establishment of hybrid balance

The differential loop current and the voltage between the tip and ring leads have a specified relationship. Establishment of the required relationship creates the input impedance.

To establish the voice path, the B11 coder–decoder (CODEC) decodes and filters the receive signal and the transmit signal. The receive signal is digital–analog and the transmit signal is analog–digital. The B11 CODEC makes frequency response corrections when the terminating impedance differs from the input impedance, as in two–element input impedances.

The balance filter accomplishes hybrid balance. The transmit signal contains parts of the receive signal. Removal of these parts must occur before coding of the transmit signal and position on the bidirectional bus.

### Overvoltage protection

The tip and ring leads of the NTEX17AA are monitored for overvoltage occurrences. When overvoltage occurs, operation of the cutover relay isolates the line circuit. System software releases the relay after removal of the fault condition.

### Overcurrent protection

The NTEX17AA has automatic protection against ground faults on the ring lead. The automatic protection function of the NT6X17BA senses the condition and limits the current that can flow in the ring lead. The function limits the current to a value that cannot damage the card.

### Voltage regulator

The B11 chip in the NTEX17AA includes a 5V regulator. The regulator takes a reference signal from the line card power supply and scales the signal. This process allows the regulator to make sure of an accurate power source of 5V.

### Relays

The NTEX17AA has the following relays:

- cutover
- test access
- ring

A cutover relay isolates the NTEX17AA line card from the subscriber loop. The relay has several purposes, including diagnostics, office installation, and protection of the line card from potential hazards.

A test access relay connects the A and B leads (tip and ring) of the NTEX17AA to the LCM test access bus during tests.

A ring relay connects the LCM ring bus to the NT6X17BA in order to ring the near–end telephone.

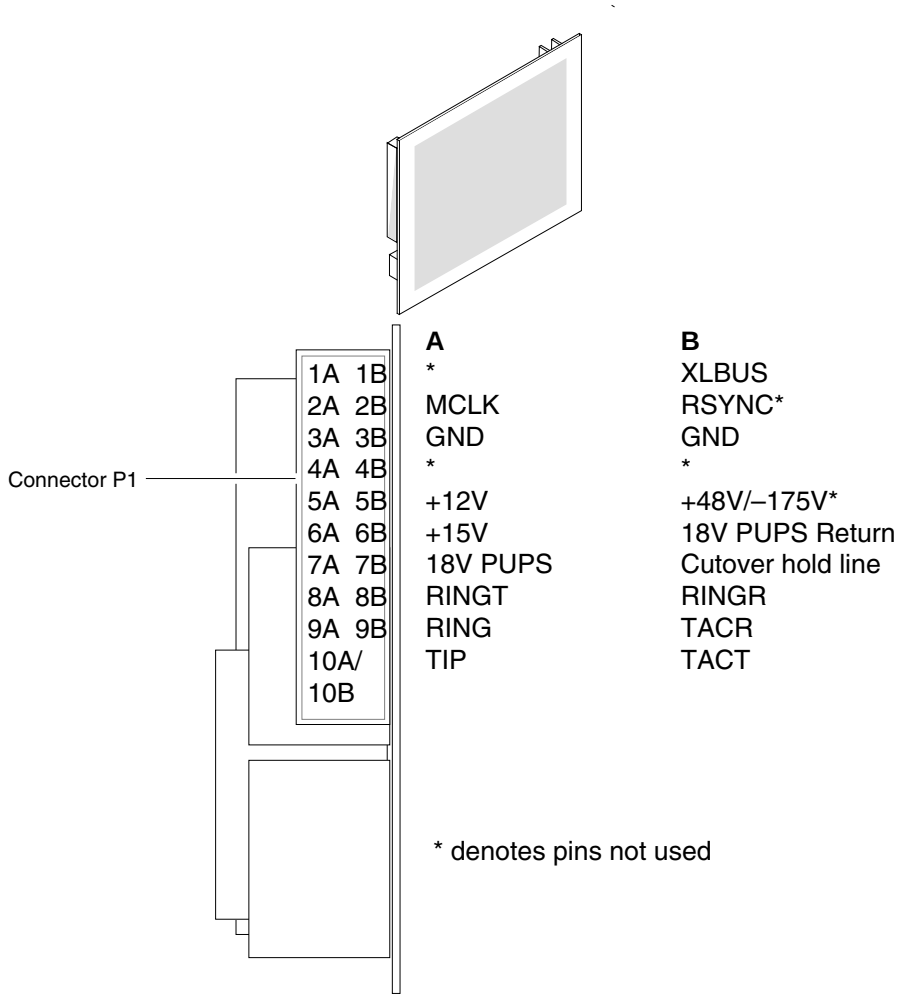
## Signaling

### Pin numbers

The pin numbers for the NTEX17AA appear in the following figure.

## **NTEX17AA** (continued)

**The NTEX17AA pin numbers**



The card has short circuit protection. The 60–Hz induction is normal with a maximum of 20 mA for each conductor. The signaling characteristics of the card appear in the following table.

**Signaling characteristics**

| Characteristic | Value |
|---|---|
| Talk battery voltage | –42.75 V to –55.8 V |
| Normal talk battery range (float charge) | –49 V to –53.5 V |
| Maximum talk battery discharge (no charge) | –42.75 V |
| Maximum talk battery charge (equalizing) | –55.8 V |
| Lightning surge protection | 1 kV (10 × 1000 μs) |
| Total loop resistance, including 500–type set for 21 mA: residential | 1900Ω |
| Conductor leakage resistance: residential | 10Ω |

## Dimensions

The dimensions of the NTEX17AA are as follows:

- height: 73 mm (2.875 in.)
- depth: 22 mm (0.875 in.)
- width: 89 mm (3.5 in.)

## Power requirements

The card requires 165 mW. The converter voltage has a power requirement of +15 V ±0.5 V. The reference voltage in the bus interface card has a power requirement of +12.7 V ±1%.

# NTEX17BA

## Product description

The NTEX17BA xDSL line card (xLC) provides full voice service and high-speed data communications in the 1-Meg Modem Service (1MMS).

### Location

The NTEX17BA occupies two slots in a line concentrating module (LCM) line drawer that supports 1MMS.

## Functional description

The NTEX17BA has the following features:

- full plain old telephone service (POTS) through the world line card (WLC)
- xDSL modem functions over subscriber loops up to 18,000 feet on 26 American wire gauge (AWG) wire and 24,000 feet on 24 AWG wire.
- rate-adaptable in downstream and upstream directions
- quadrature amplitude modulation (QAM) in both downstream and upstream directions
- forward error correction (FEC) in the downstream direction
- interleaving in downstream direction for enhanced noise immunity at wideband 256 QAM rate
- supports narrowband and wideband downstream spectra at low and high transmission levels
- higher transport rates than the NTEX17AA:
  - — raw transport downstream data rates of 1280 kilobits per second (kbit/s) to 80 kbit/s;
  - — raw transport upstream data rates of 320 kbit/s to 40 kbit/s
- extended line card bus (XLBUS) interface to backplane
- -48V power to data portion of card
- self-identifying to 1MMS data-enhanced bus interface card (DBIC) on installation
- out-of-service data loopback capability for operations, administration, and maintenance (OAM)
- low power design
- off hook detection that allows splitterless operation
- faster line resynchronization than the NTEX17AA
- downstream power-level control

- lightening protection of POTS splitter improved from NTEX17AA
- POTS splitter improved from NTEX17AA; supports wideband upstream

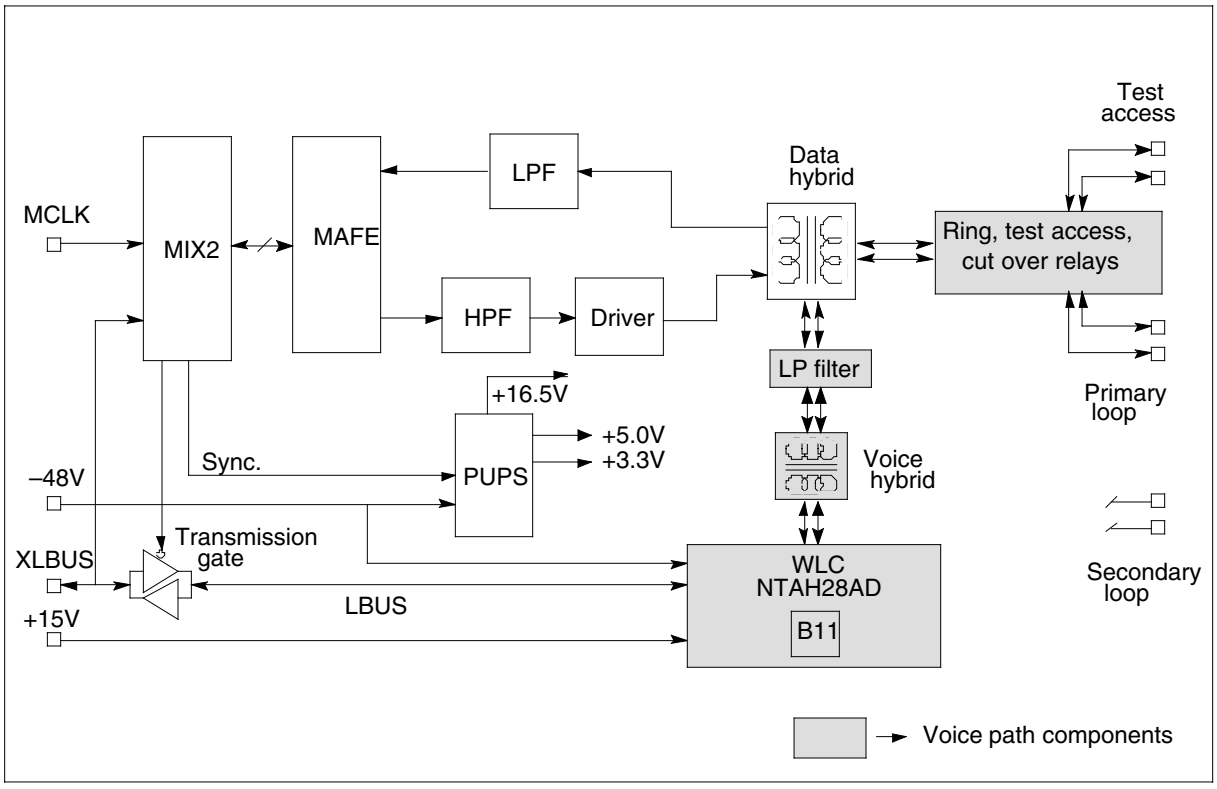
## Functional blocks

The NTEX17BA has the following functional blocks:

- relays
- world line card (WLC) application-specific integrated circuit (ASIC)
- modem analog front end (MAFE) ASIC
- modem interface to XLBUS (MIX2) ASIC

The following figure shows the relationship of the functional blocks.

**NTEX17BA functional blocks**



## NTEX17BA (continued)

### Relays

The relays present on the NTEX17BA provide functions similar to those found on a POTS line card. Some the similar functions follow:

- application of ring voltage to the loop
- disconnection of the card from the loop during provisioning and testing
- connection of the incoming tip and ring to the test access port

DMS software manages these relays, which are accessed through registers within the B11 coder-decoder (codec) that reside on the WLC dual inline package (DIP). If you disconnect the card from the loop, you disable all data transmission and voice service.

### WLC

The WLC is a thick film hybrid version, based on the B11 ASIC. The WLC provides the voice functionality. The NTEX17BA uses NTAH28AF, a DIP version of the WLC.

### MAFE

The MAFE ASIC is a full analog device that integrates many of the functions that were implemented on discrete devices on the NTEX17AA. A dedicated serial interface to the MIX2 gives the processor access to the configuration register. The MAFE is packaged in a 64-pin TQFP.

### MIX2

The MIX2 ASIC uses QAM to provide downstream and upstream data transport between the DBIC and the twisted wire pair. The MIX2 ASIC uses the XLBUS protocol to the DBIC, and it isolates XLBUS and the B11 filter codec chip during data transport.

The MIX2 architecture consists of the following blocks:

- XLBUS interface/off hook detect
- controller
- registers
- downstream FIFO
- upstream FIFO
- transmission frame generator
- receive frame decoder
- QAM modulator
- QAM demodulator

- clocks
- test access
- transmission FEC and interleaving
- receive FEC

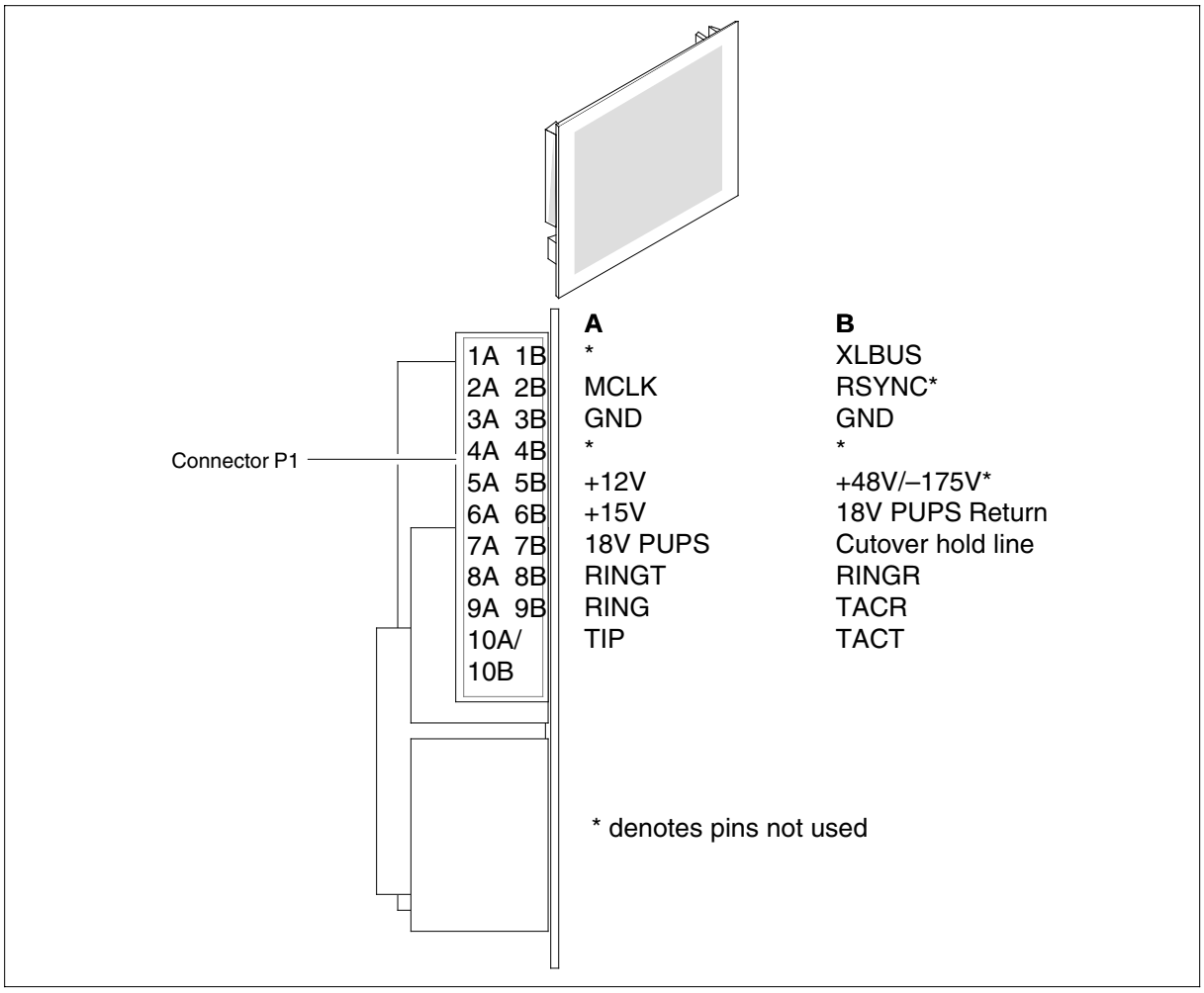
## Signaling

This section describes the signalling functions of the NTEX17BA.

### Pin outs

The following figure shows the pin outs for NTEX17BA.

**NTEX17BA pin outs**



## **NTEX17BA** (end)

# Technical data

This section provides additional technical information on the NTEX17BA.

### Dimensions

The NTEX17BA is a two-slot card. Except for height, the NTEX17BA has the same dimensions as voice line cards.

### Power requirements

The point of use power supply (PUPS) uses the -48V battery feed as input. The PUPs provides +16.5V, +5V, and +3.3V to various functions on the board.

### Drawer fill restrictions

Thermal constraints and power distribution within the LCM line card drawer create restrictions on the fill of the NTEX17BA in an LCM line drawer equipped for 1MMS. Refer to *1-Meg Modem Service Network Implementation Manual*, 297-8063-200 for information on the drawer fill restrictions for your office.

# NTEX17CA

## Product description

The NTEX17CA xDSL line card (xLC) provides full voice service and high-speed data communications in the 1-Meg Modem Service.

### Location

The NTEX17CA occupies two slots in a line concentrating module (LCM) line drawer that supports 1-Meg Modem Service.

## Functional description

The NTEX17CA has the following features:

- full plain old telephone service (POTS) through the world line card (WLC)
- xDSL modem functions over subscriber loops up to 18,000 feet on 26 American wire gauge (AWG) wire and 24,000 feet on 24 AWG wire.
- rate-adaptable in downstream and upstream directions
- quadrature amplitude modulation (QAM) in both downstream and upstream directions
- forward error correction (FEC) in the upstream and downstream direction
- interleaving in downstream direction for enhanced noise immunity at wideband 256 QAM rate
- supports narrowband and wideband downstream spectra at low and high transmission levels
- raw transport downstream data rates of 1280 kilobits per second (kbit/s) to 80 kbit/s
- raw transport upstream data rates of 320 kbit/s to 40 kbit/s
- extended line card bus (XLBUS) interface to backplane
- -48V power to data portion of card
- self-identifying to 1-Meg Modem Service data-enhanced bus interface card (DBIC) on installation
- out-of-service data loopback capability for operations, administration, and maintenance (OAM)
- low power design
- off hook detection that allows splitterless operation
- downstream power-level control
- lightening protection of POTS splitter

## **NTEX17CA** (continued)

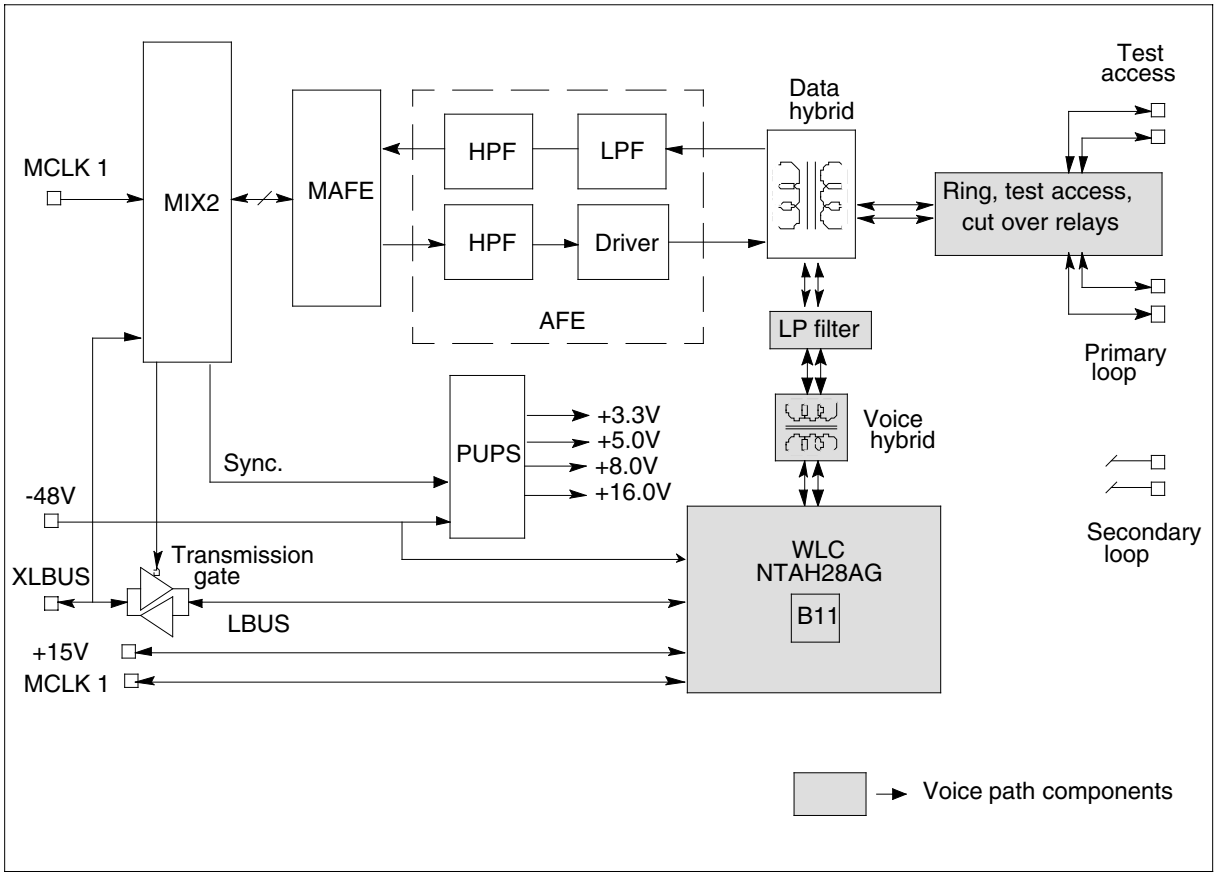
### Functional blocks

The NTEX17CA has the following functional blocks:

- relays
- world line card (WLC) application-specific integrated circuit (ASIC)
- analog front end (AFE)
- modem analog front end (MAFE) ASIC
- modem interface to XLBUS (MIX2) ASIC

The following figure shows the relationship of the functional blocks.

**NTEX17CA functional blocks**



### Relays

The relays present on the NTEX17CA provide functions similar to those found on a POTS line card. Some of the similar functions follow:

- application of ring voltage to the loop
- disconnection of the card from the loop during provisioning and testing
- connection of the incoming tip and ring to the test access port

DMS software manages these relays, which are accessed through registers within the B11 coder-decoder (codec) that reside on the WLC dual inline package (DIP). If you disconnect the card from the loop, you disable all data transmission and voice service.

### WLC

The WLC is a thick film hybrid version, based on the B11 ASIC. The WLC provides the voice functionality. The NTEX17CA uses NTAH28AG, a DIP version of the WLC.

### AFE

The AFE consists of transmit and receive sections.

The transmit section consists of a line driver and a high pass filter (HPF). The HPF filters harmonics from the digital-to-analog conversion (DAC) process and high-frequency images from the digital sampling process. The line driver increases the power of the signal on the loop.

The receive section consists of HPFs. The HPFs lower the downstream signal to the same voltage as the upstream signal.

### MAFE ASIC

The MAFE ASIC is a full analog device that integrates many of the functions that were implemented on discrete devices on the NTEX17AA and NTEX17BA. A dedicated serial interface to the MIX2 gives the processor access to the configuration register. The MAFE is packaged in a 64-pin TQFP.

### MIX2 ASIC

The MIX2 ASIC uses QAM to provide downstream and upstream data transport between the DBIC and the twisted wire pair. The MIX2 ASIC uses the XLBUS protocol to the DBIC, and it isolates XLBUS and the B11 filter codec chip during data transport.

## **NTEX17CA** (continued)

The MIX2 architecture consists of the following blocks:

- XLBUS interface/off hook detect
- controller
- registers
- downstream FIFO
- upstream FIFO
- transmission frame generator
- receive frame decoder
- QAM modulator
- QAM demodulator
- clocks
- test access
- transmission FEC and interleaving
- receive FEC

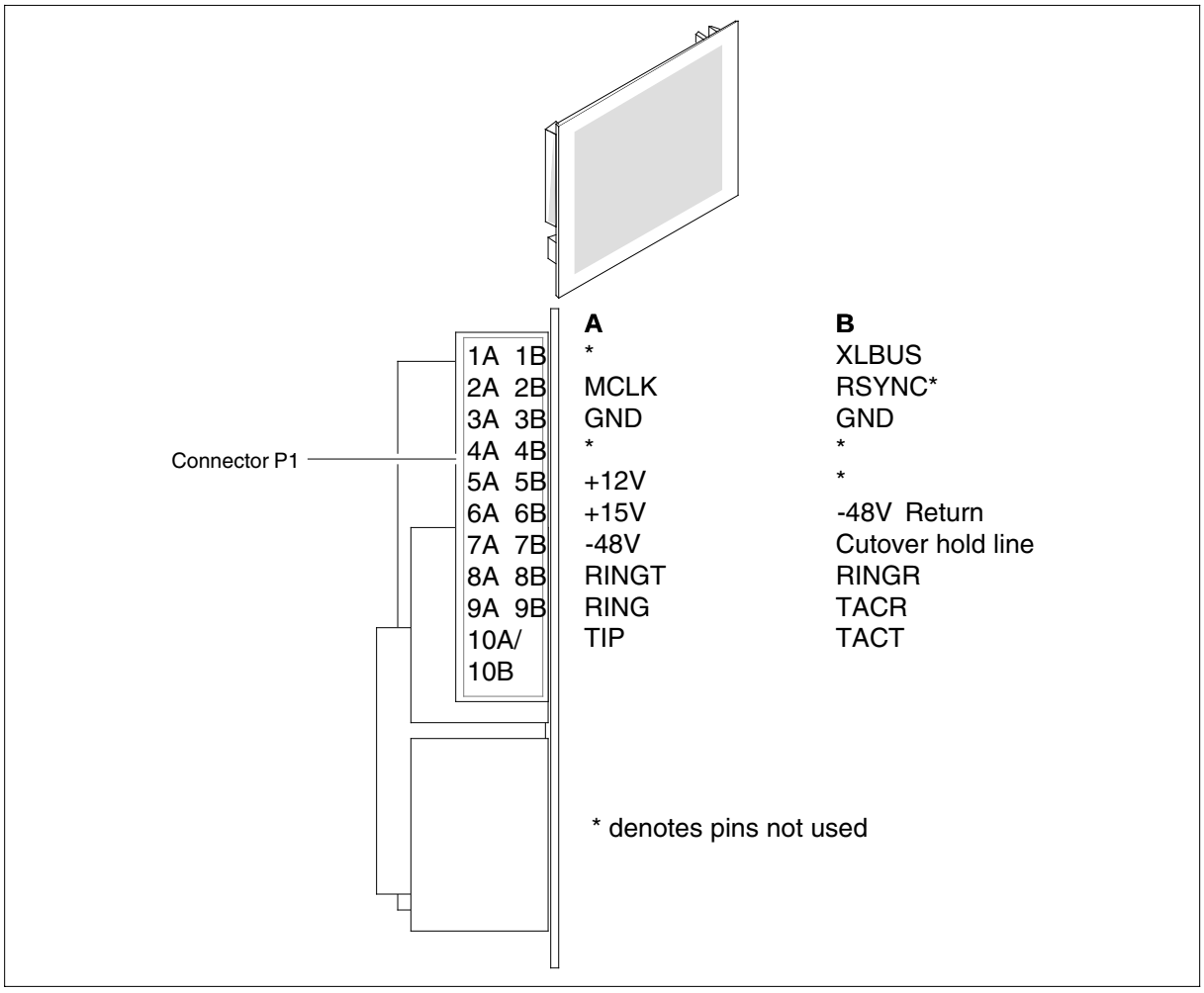
## Signaling

This section describes the signalling functions of the NTEX17CA.

### Pin outs

The following figure shows the pin outs for NTEX17CA.

**NTEX17CA pin outs**




## Technical data

This section provides additional technical information on the NTEX17CA.

### Dimensions

The NTEX17CA is a two-slot card. Except for height, the NTEX17CA has the same dimensions as voice line cards.

### Power requirements

The point of use power supply (PUPS) uses the -48V battery feed as input. The PUPs provides +16V, +7.5V, +5V, and +3.3V to various functions on the board.

## **NTEX17CA** (end)

### Drawer fill restrictions

Refer to *1-Meg Modem Service Network Implementation Manual*, 297-8063-200 for information on the drawer fill restrictions for your office.

# NTEX17DA

## Product description

The NTEX17DA xDSL line card (xLC) provides full voice service and high-speed data communications in the 1-Meg Modem Service.

### Location

The NTEX17DA occupies two slots in a line concentrating module (LCM) line drawer that supports 1-Meg Modem Service.

## Functional description

The NTEX17DA has the following features:

- full plain old telephone service (POTS) through the world line card (WLC)
- xDSL modem functions over subscriber loops up to 18,000 feet on 26 American wire gauge (AWG) wire and 24,000 feet on 24 AWG wire.
- rate-adaptable in downstream and upstream directions
- quadrature amplitude modulation (QAM) in both downstream and upstream directions
- forward error correction (FEC) in the upstream and downstream direction
- interleaving in downstream direction for enhanced noise immunity at wideband 256 QAM rate
- supports narrowband and wideband downstream spectra at low and high transmission levels
- raw transport downstream data rates of 1280 kilobits per second (kbit/s) to 80 kbit/s
- raw transport upstream data rates of 320 kbit/s to 40 kbit/s
- extended line card bus (XLBUS) interface to backplane
- -48V power to data portion of card
- self-identifying to 1-Meg Modem Service data-enhanced bus interface card (DBIC) on installation
- only compatible with NTEX54CA DBIC
- out-of-service data loopback capability for operations, administration, and maintenance (OAM)
- low power design
- off hook detection that allows splitterless operation
- downstream power-level control
- lightening protection of POTS splitter

## **NTEX17DA** (continued)

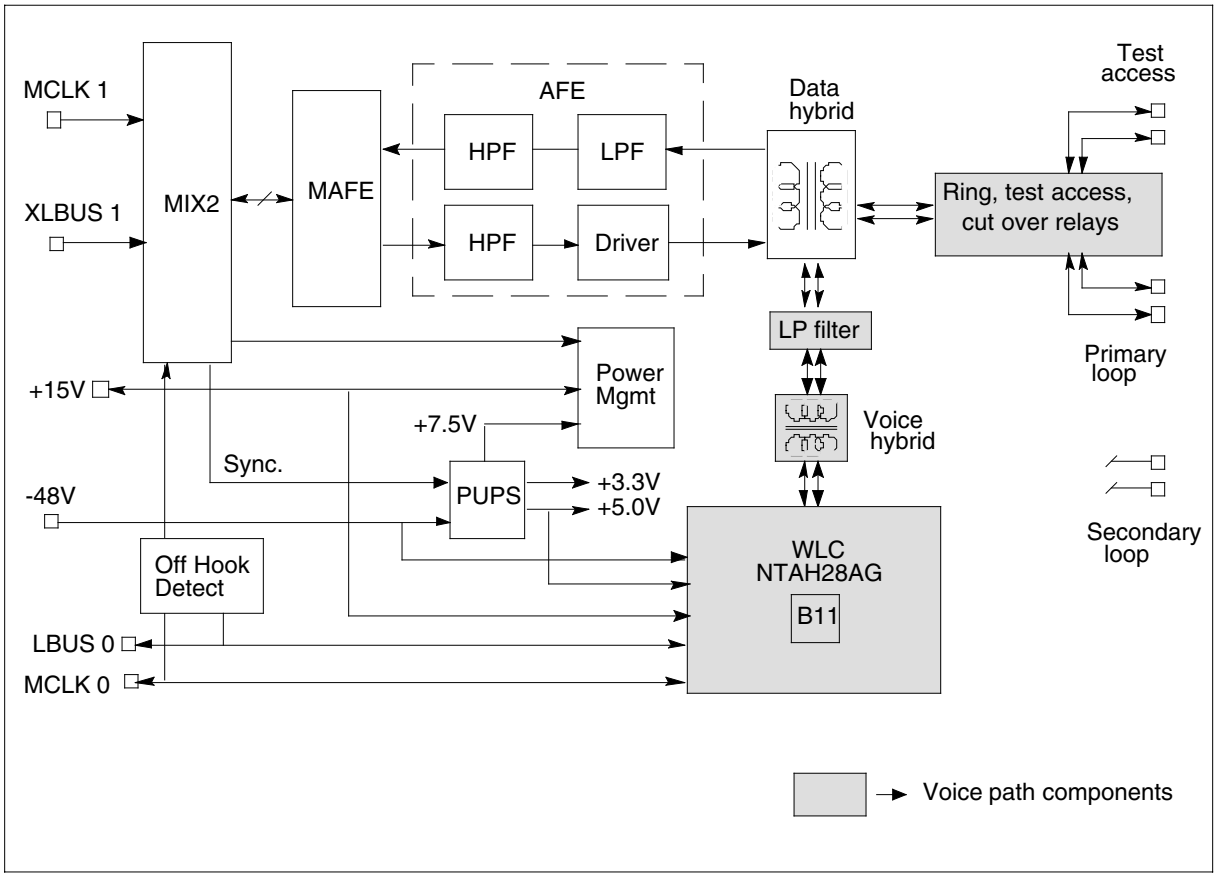
### Functional blocks

The NTEX17DA has the following functional blocks:

- relays
- world line card (WLC) application-specific integrated circuit (ASIC)
- analog front end (AFE)
- modem analog front end (MAFE) ASIC
- modem interface to XLBUS (MIX2) ASIC

The following figure shows the relationship of the functional blocks.

**NTEX17DA functional blocks**



### Relays

The relays present on the NTEX17DA provide functions similar to those found on a POTS line card. Some of the similar functions follow:

- application of ring voltage to the loop
- disconnection of the card from the loop during provisioning and testing
- connection of the incoming tip and ring to the test access port

DMS software manages these relays, which are accessed through registers within the B11 coder-decoder (codec) that reside on the WLC dual inline package (DIP). If you disconnect the card from the loop, you disable all data transmission and voice service.

### WLC

The WLC is a thick film hybrid version, based on the B11 ASIC. The WLC provides the voice functionality. The NTEX17DA uses NTAH28AG, a DIP version of the WLC.

### AFE

The AFE consists of transmit and receive sections.

The transmit section consists of a line driver and a high pass filter (HPF). The HPF filters harmonics from the digital-to-analog conversion (DAC) process and high-frequency images from the digital sampling process. The line driver increases the power of the signal on the loop.

The receive section consists of HPFs. The HPFs lower the downstream signal to the same voltage as the upstream signal.

### MAFE ASIC

The MAFE ASIC is a full analog device that integrates many of the functions that were implemented on discrete devices on the NTEX17AA and NTEX17BA. A dedicated serial interface to the MIX2 gives the processor access to the configuration register. The MAFE is packaged in a 64-pin TQFP.

### MIX2 ASIC

The MIX2 ASIC uses QAM to provide downstream and upstream data transport between the DBIC and the twisted wire pair. The MIX2 ASIC uses the XLBUS protocol to the DBIC, and it isolates XLBUS and the B11 filter codec chip during data transport.

## **NTEX17DA** (continued)

The MIX2 architecture consists of the following blocks:

- XLBUS interface/off hook detect
- controller
- registers
- downstream FIFO
- upstream FIFO
- transmission frame generator
- receive frame decoder
- QAM modulator
- QAM demodulator
- clocks
- test access
- transmission FEC and interleaving
- receive FEC

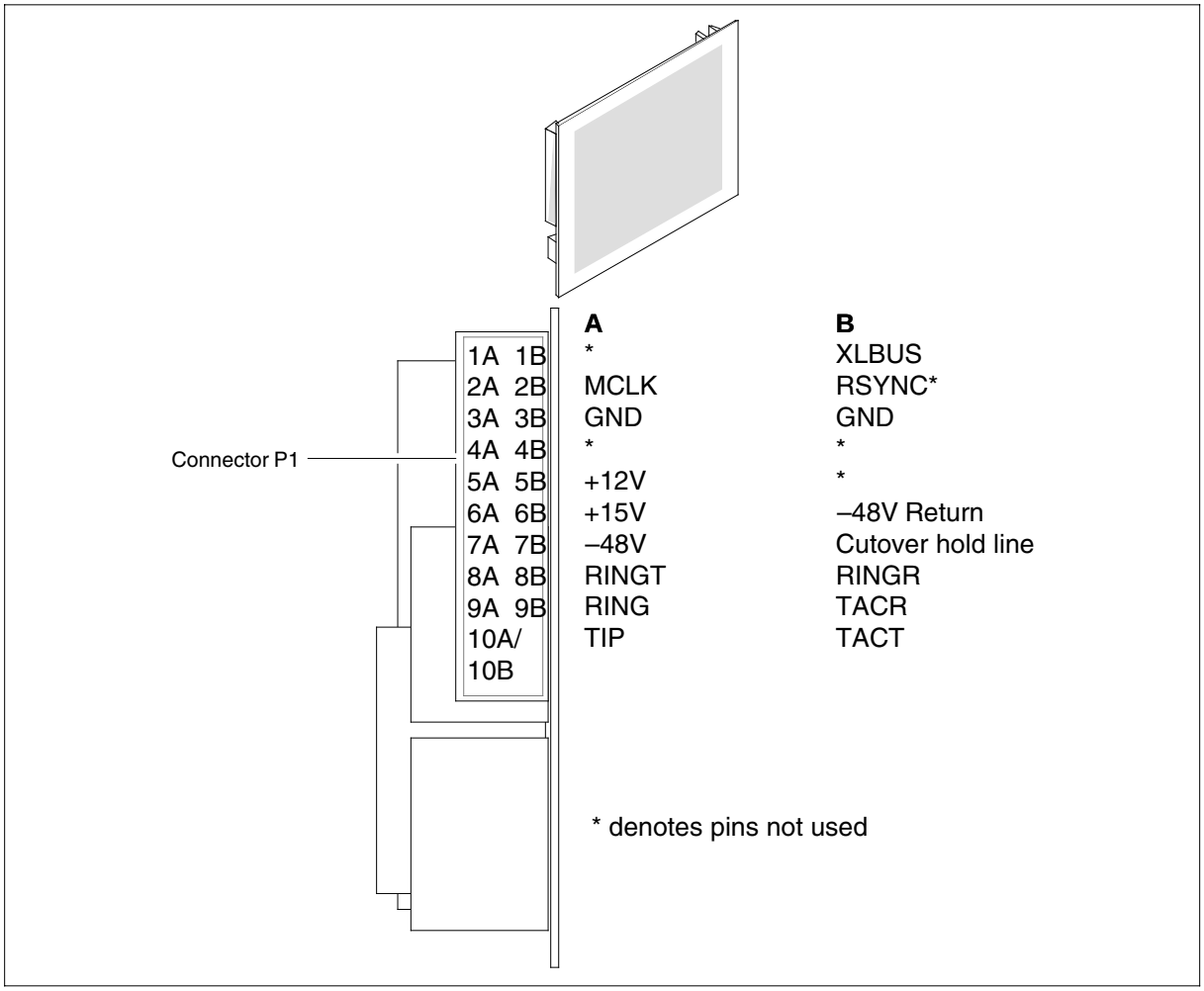
## Signaling

This section describes the signalling functions of the NTEX17DA.

### Pin outs

The following figure shows the pin outs for NTEX17DA.

**NTEX17DA pin outs**




## Technical data

This section provides additional technical information on the NTEX17DA.

### Dimensions

The NTEX17DA is a two-slot card. Except for height, the has the same dimensions as voice line cards.

### Power requirements

The point of use power supply (PUPS) uses the -48V battery feed as input. The PUPs provides +16V, +7.5V, +5V, and +3.3V to various functions on the board.

## **NTEX17DA** (end)

### Drawer fill restrictions

Refer to *1-Meg Modem Service Network Implementation Manual*, 297-8063-200 for information on the drawer fill restrictions for your office.

# NTEX20AA

## Product description

The NTEX20AA card is an intrashelf paddle board used in the link interface shelf (LIS) of the link peripheral processor (LPP). The NTEX20AA card terminates the frame transport bus A (F-bus A) and the channel transport bus A (C-bus A).

### Location

The NTEX20AA is in position 31 R of the shelf.

## Functional description

The F-bus A is a bidirectional, intrashelf, open-collector bus. A driver, on the NT9X74AA card (F-bus repeater) in slot 07 F, clocks the F-bus A. A parallel resistor network terminates the F-bus at the source. The F-bus A is in a not terminated state at the A-bus destination repeater in slot 32 F. In the original condition, the two source terminations and the conjugate bus destination terminations were on the repeaters. The removal of a repeater is required if the conjugate bus degrades through loss of the destination terminations. The NTEX20AA eliminates this problem through the position of the destination terminations on the paddle board. The position of the paddle board in a different slot also eliminates this problem. The NTEX20AA is placed in slot 31 R to terminate the F-bus A. The F-bus A must terminate before the card crosses over between slots 31 and 32.

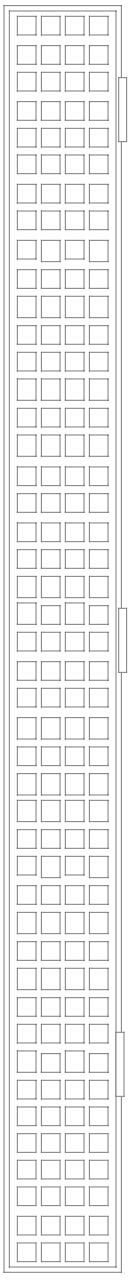
## Signaling

### Pin numbers

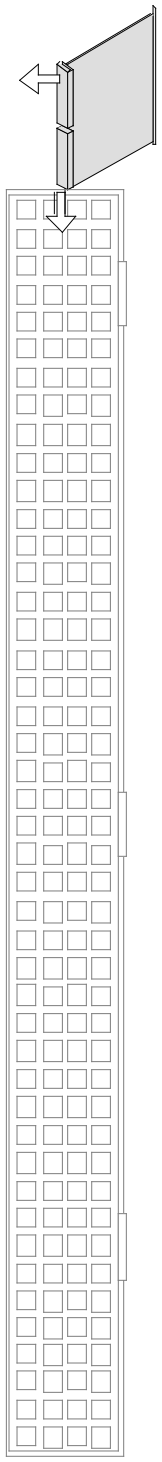
The pin numbers for the NTEX20AA appear in the following figure.

# **NTEX20AA** (continued)

### NTEX20AA pin numbers



| | A | B | C | D |
|---|---|---|---|---|
| 1 | GND | FAAD0 | FAWAIT- | |
| 2 | GND | FAAD1 | FACLR- | |
| 3 | GND | FAAD2 | FAREQ- | |
| 4 | GND | FAAD3 | FAPOLL- | |
| 5 | GND | FAAD4 | FARST- | |
| 6 | GND | FAAD5 | FAPACK- | |
| 7 | GND | FAAD6 | GND | GND |
| 8 | GND | FAAD7 | FAADREN- | |
| 9 | GND | FAPAR | FADATEN- | |
| 10 | GND | GND | FAEOS | |
| 11 | GND | | FARACK- | |
| 12 | GND | | FARRDY- | |
| 13 | | | FASRCEN- | |
| 14 | | | FADSTEN- | |
| 15 | | | GND | GND |
| 16 | | | GND | GND |
| 17 | | | | |
| 18 | | | | |
| 19 | | | | |
| 20 | | GND | | GND |
| 21 | | CLK8A | | GND |
| 22 | | CLK56A | | |
| 23 | | | | |
| 24 | | | | |
| 25 | | | | |
| 26 | | | | |
| 27 | | | | GND |
| 28 | | +5B | GND | |
| 29 | | +5B | | |
| 30 | GND | +5B | | |
| 31 | FACLK | +5B | | |
| 32 | | +5B | GND | |
| 33 | | +5B | | |
| 34 | GND | +5B | | |
| 35 | | +5B | | |
| 36 | | | | |
| 37 | | | | |
| 38 | | | | |
| 39 | | | | |
| 40 | GND | | | |
| 41 | GND | | | |
| 42 | GND | | | |
| 43 | GND | | | |
| 44 | +5V | | | |
| 45 | +5V | | | |



| | A | B | C | D |
|---|---|---|---|---|
| 46 | +5V | | | |
| 47 | +5V | GND | | |
| 48 | +5V | | | |
| 49 | +5V | | | |
| 50 | +5V | GND | | |
| 51 | +5V | CATFP- | | |
| 52 | +5V | CATCLK | | |
| 53 | +5V | GND | | |
| 54 | +5V | | | |
| 55 | +5V | | | |
| 56 | | GND | | |
| 57 | CARDST- | | | |
| 58 | CACBILP- | | | |
| 59 | CATD0 | | | |
| 60 | CATD1 | | | |
| 61 | CATD2 | | | |
| 62 | CATD3 | | | |
| 63 | CATD4 | | | |
| 64 | CATD5 | | | |
| 65 | CATD6 | | | |
| 66 | CATD7 | | | GND |
| 67 | CATACT- | | | CACBIDS- |
| 68 | CATPAR | | | |
| 69 | CARD0 | | GND | |
| 70 | CARD1 | | CSCFT | |
| 71 | CARD2 | | | |
| 72 | CARD3 | | | |
| 73 | CARD4 | | | |
| 74 | CARD5 | | | |
| 75 | CARD6 | | | D0 |
| 76 | CARD7 | | | D2 |
| 77 | CARIND- | | | D4 |
| 78 | CARPAR | | | D6 |
| 79 | GND | | | |
| 80 | GND | | | A2 |
| 81 | GND | | | A0 |
| 82 | GND | | | |
| 83 | GND | | | |
| 84 | GND | | | D7 |
| 85 | GND | | | A1 |
| 86 | GND | | | A3 |
| 87 | GND | | | |
| 88 | GND | | | D5 |
| 89 | GND | | | D3 |
| 90 | GND | | | D1 |

# Technical data

## Terminations

A parallel group of resistors forms the terminations for the F-bus and the C-bus. One value is for the clock signals. The other value is for the data, address and control signals.

For the bus characteristics of the Am26S10 transceiver, the high threshold is 2.0 to 2.25V. The low threshold is 2.0 to 1.75V. In an off state, the bus termination quiescent voltage for the clock lines is 3.4V. When the transceiver turns on and sinks the current on this line, the voltage drops. The voltage drops to the saturation voltage of the 26S10 output transistor. The saturation voltage is specified at 0.8V. The voltage has a maximum current of 100 mA. The noise margin for the clock lines is 1.4V when the bus is in an off state. The noise margin for the clock lines is 1.2V when the bus is in a low or on state.

The voltage for the data, address and control lines in a quiescent high or off state is 2.7V. The voltage is 0.7V for the 26S10 output transistor saturation when on. The result is a noise margin of 0.7V in the high or off state, and a noise margin of 1.3V in the low or on state. The devices that drive the clock lines sink the current. This current is 120 mA. The data, address and control lines deliver 70 mA in the quiescent on state.

# NTEX20BA

## Product description

The NTEX20BA is an intrashelf paddle board used in the link interface shelf (LIS) of the link peripheral processor (LPP). The NTEX20BA terminates the frame transport bus B (F-bus B) and the channel transport bus B (C-bus B).

### Location

The NTEX20BA is in position 10 R of the shelf.

## Functional description

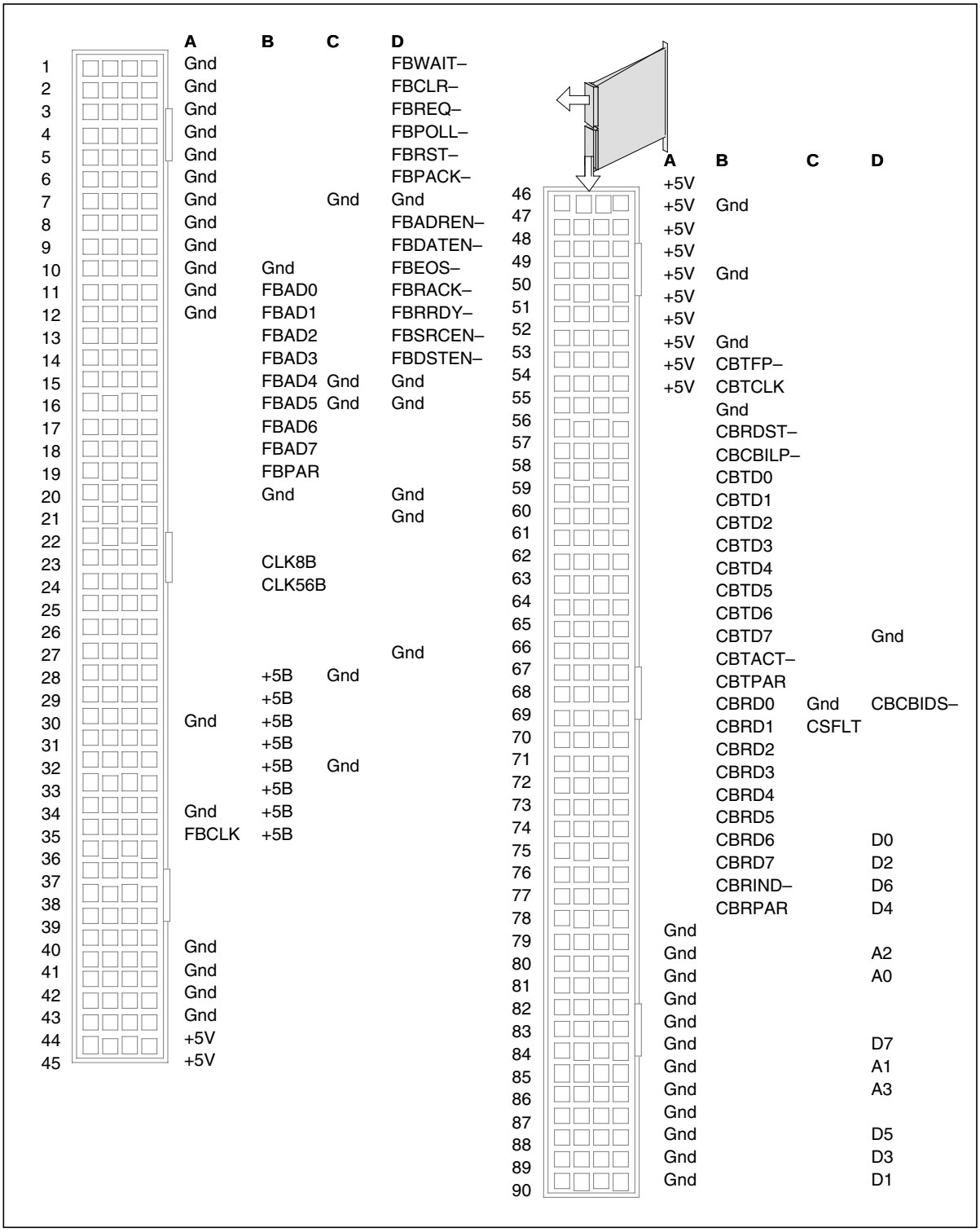
A rate adapter (RA) sources the F-bus B through the NT9X74AA repeater card in slot 32 F. Source parallel terminates in slot 32 F. The F-bus B is in a not terminated state at the B-bus destination at the repeater in slot 07 F. In the original condition, the two source terminations and the conjugate bus destination terminations were on the repeaters. The removal of a repeater is required if the conjugate bus degrades through loss of destination terminations. The NTEX20BA eliminates this problem through the position of the destination terminations on the paddle board. The position of the paddle board in a different slot also eliminates this problem. The NTEX20BA is placed in slot 10R to terminate the destination end of the F-bus B. The F-bus B is driven from the repeater in slot 32 F. The F-bus B ends at the repeater in slot 07 F.

## Signaling

### Pin numbers

The pin numbers for the NTEX20BA appear in the following figure.

### NTEX20BA pin numbers



## **NTEX20BA** (end)

# Technical data

### Terminations

A parallel group of resistors forms the terminations for the F-bus and the C-bus. One value is for the clock signals. The other value is for the data, address and control signals.

For the bus characteristics of the Am26S10 transceiver, the high threshold is 2.0 to 2.25V. The low threshold is 2.0 to 1.75V. In an off state, the bus termination quiescent voltage for the clock lines is 3.4V. When the transceiver turns on and sinks the current on this line the voltage drops. The voltage drops to the saturation voltage of the 26S10 output transistor. The saturation voltage is specified at 0.8V with a maximum current of 100 mA. The noise margin for the clock lines is 1.4V when the bus is in an off state. The noise margin is 1.2V when the bus is in a low or on state.

The voltage for the data, address, and control lines in a quiescent high or off state is 2.7V. This voltage is 0.7V for the 26S10 output transistor saturation when turned on. The result is a noise margin of 0.7V in the high or off state and a noise margin of 1.3V in the low or on state. The devices that drive the clock lines sinks the current. This current is 120 mA. The current is 120 mA when the data, address and control lines deliver 70 mA in the quiescent on state.

## Product description

The NTEX22AA card is used in the CCS7 link interface unit (LIU7) of the signaling transfer point (STP) switch. The card replaces the NT9X13CA link general processor and the NT9X75AA frame transport bus (F-bus)-to-F-bus interface.

## Functional description

The NTEX22AA card provides the following functions:

- LIU7 link general processor
- dual F-bus interface ability

The processor maintains and operates the two F-bus interface controllers, and on-board maintenance functions.

### Functional blocks

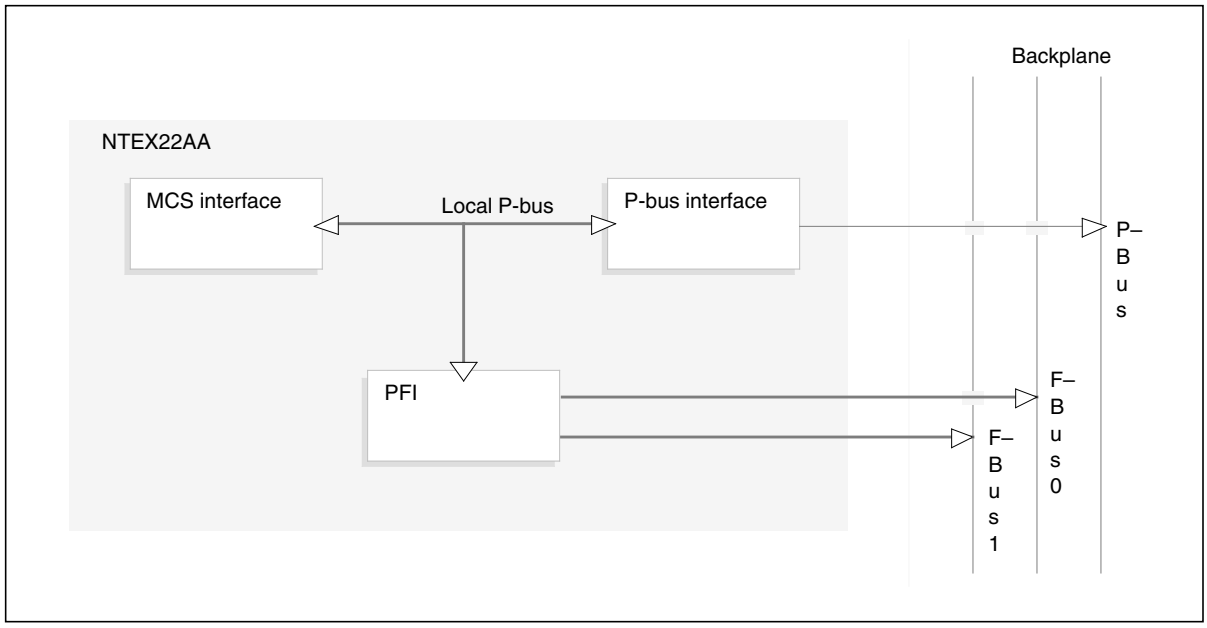
The NTEX22AA consists of the following functional blocks:

- microcontroller subsystem (MCS) interface
- processor bus (P-bus) interface
- P-bus-to-F-bus interface (PFI)

The functional relationship between these blocks appears in the following figure.

## NTEX22AA (continued)

**NTEX22AA functional blocks**




### Microcontroller subsystem interface

The MCS interface block consists of the MCS and the clock, address and data buffers, application erasable programmable read-only memory (EPROM) and control signal logic. The 68030, the MCM and the MCS DRAMSAs load the 68030 address and data buses. The buses are buffered for use on the NTEX22AA. An exception is the EPROM, which sits on the 68030 bus. The control signal logic provides the interface between the MCS and the backplane to provide P-bus and DMA capability.

### P-bus-to-F-bus interface

The PFI is between the local P-bus and the two F-buses. The local bus (L-bus) is the main bus. The L-bus/P-bus interface (LPIF), two F-bus interface controllers (FIC), and the L-bus RAM reside on the L-bus. The FICs and the LPIF connect to the address port of the L-bus through a bank of multiplexers. The L-bus arbiter controls these multiplexers. These multiplexers select the address from the current bus master. Communication with the data part of the L-bus is through tri-state drivers.

The LPIF and the two FICs are potential bus masters, and have request lines to the arbiter. The arbiter decides which device becomes the next bus master. The arbiter grants the bus to the bus master through a dedicated grant line.

An L-bus fault controller monitors LRAM cycles and generates an interrupt when the controller detects an addressing or parity error. The L-bus fault controller does not collect P-bus cycles to the FIC.

### Processor bus interface

The P-bus interface consists of the reset circuits and P-bus circuits. These circuits include P-bus parity circuitry, interrupt controllers, backplane buffering, address decoders, control register and ID PROM.

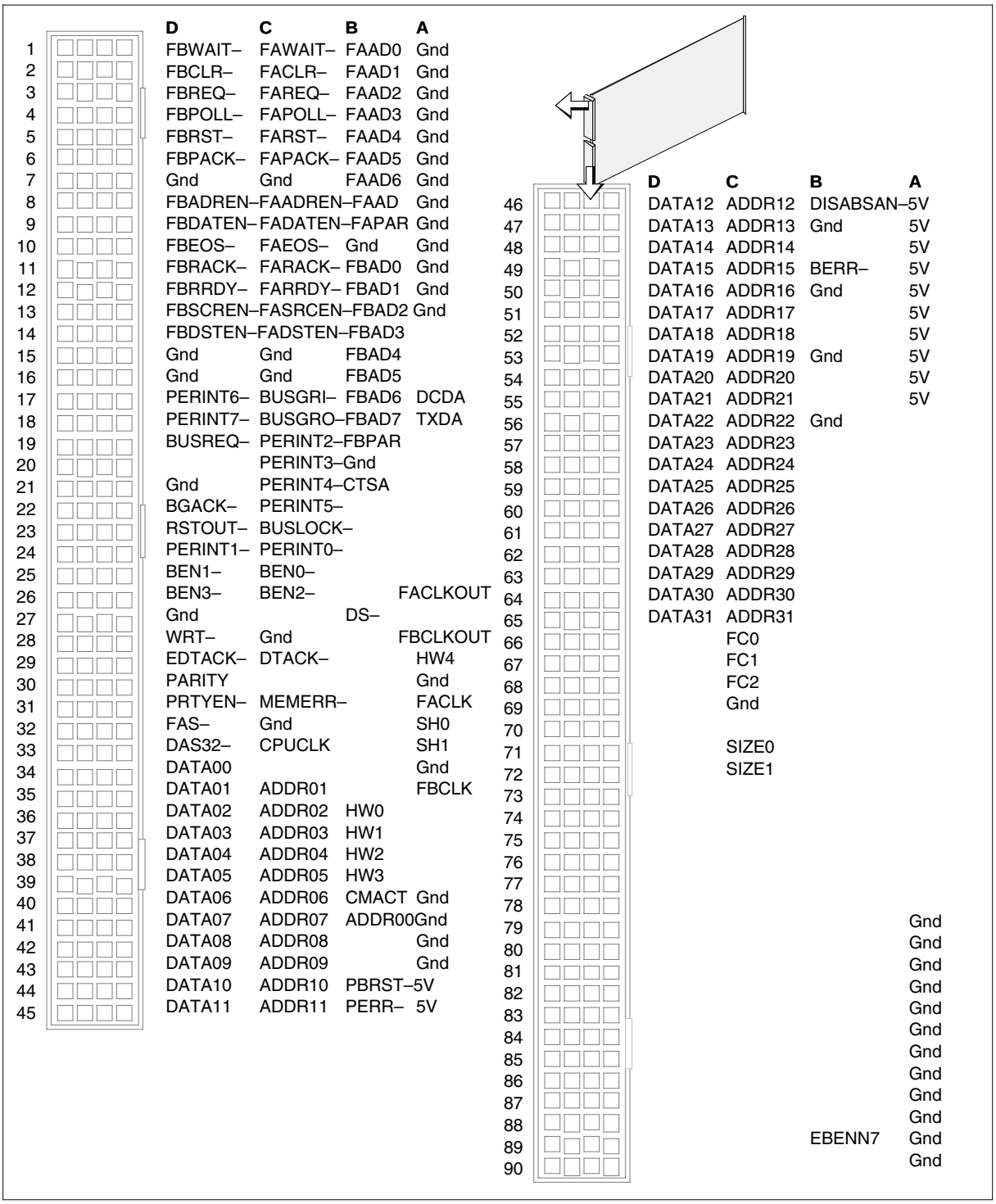
## Signaling

### Pin numbers

The pin outs for NTEX22AA appear in the following figure.

# **NTEX22AA** (continued)

### NTEX22AA pin numbers

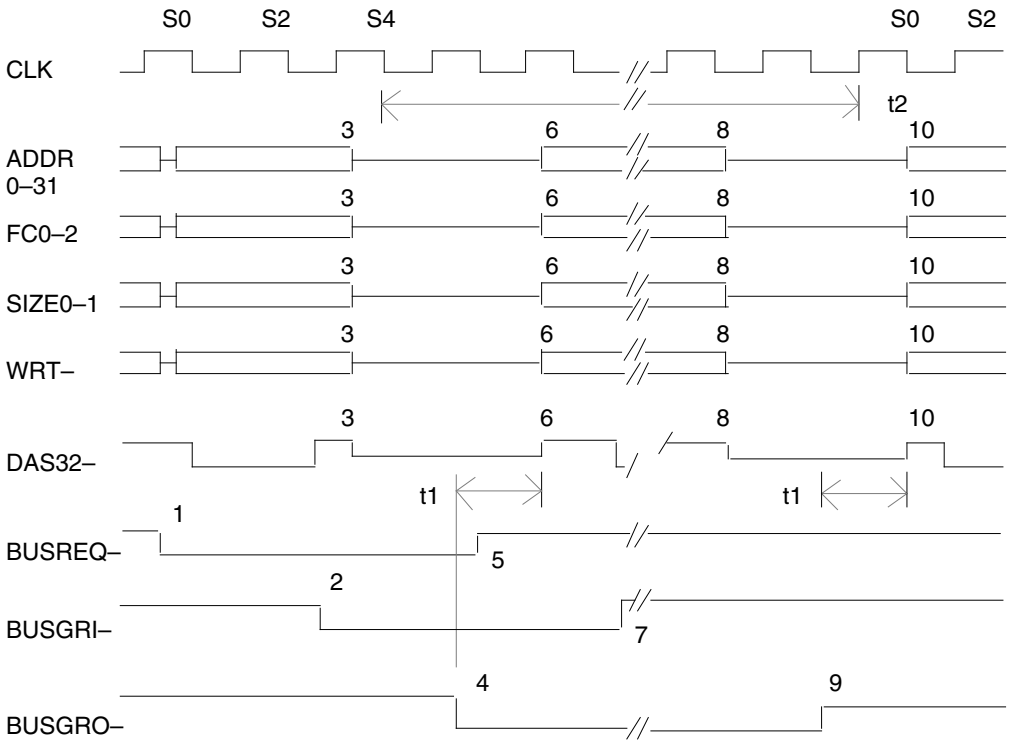


## Timing

The bus arbitration timing for the NTEX22AA appears in the following figure.

An example of L-bus arbiter timing for the NTEX22AA appears in the following figure.

**NTEX22AA Bus arbitration timing**

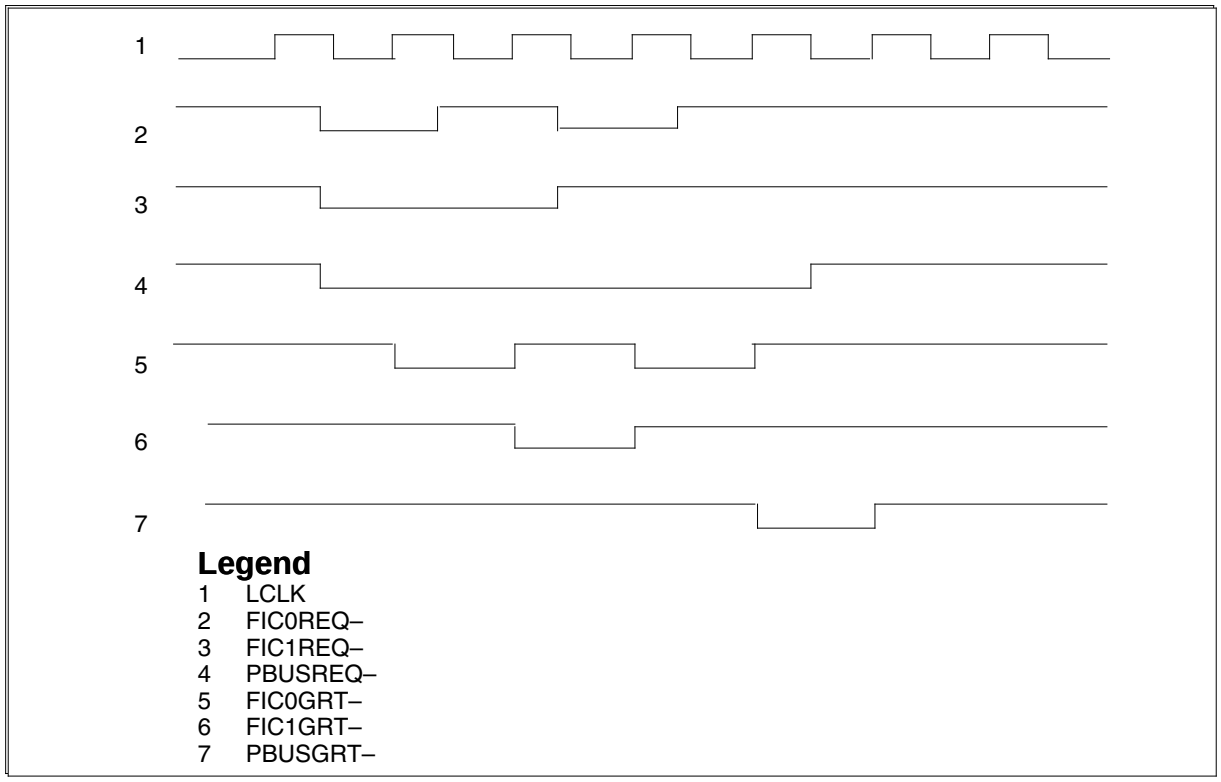



### Legend

1 External DMA controller device requests bus.
2 NTEX22AA grants bus mastership after de-glitching BUSREQ– input.
3 MCS 68030 finishes last bus cycle and releases bus.
4 External DMA controller sees that DAS32– is quiet. This condition indicates no bus activity and asserts BUSGRO–.
5 External DMA controller removes BUSREQ– next device in hierarchy can request bus mastership.
6 External DMA controller waits 100 ns (t1) and begins DMA cycles.
7 MCS 68030 removes BUSGRI– signal in response to BUSREQ– being removed.
8 External DMA controller finishes DMA transfers. External DMA controller disables bus drivers to release bus.
9 External DMA controller removes BUSGRO– signal and releases bus.
10 The MCS 68030 regains bus mastership after 100 ns (t1).

# **NTEX22AA** (end)

**NTEX22AA L-bus arbiter timing**



## Product description

The NTEX22BA integrated processor and F-bus interface card is used in the link peripheral processor (LPP). This card is used in application-specific units (ASU) that require more than 4 Mbytes of DRAM. The NTEX22BA is the equivalent of the NT9X13CA link general processor. This card is the equivalent of the NT9X75AA P-bus to F-bus interface in the 3-slot ASU.

Applications from BCS33 or before, that require more than 4 Mbytes of memory, use the NTEX22BA card. The network interfaceunit (NIU), and the applications that require more than 4 Mbytes of DRAM, use the NTEX22BB card in BCS34.

For the LIU7, the NTEX22BA card is optional in North America, but required in the United Kingdom.

The NTEX22BA is like the ntex22AA, except that the BA card has 8 Mbytes of DRAM. The AA card has 4 Mbytes of DRAM.

## Functional description

The NTEX22BA card provides a link general processor and dual F-bus interface ability.

The processor maintains and operates the two F-bus interface controllers, onboard maintenance functions and the application.

### Functional blocks

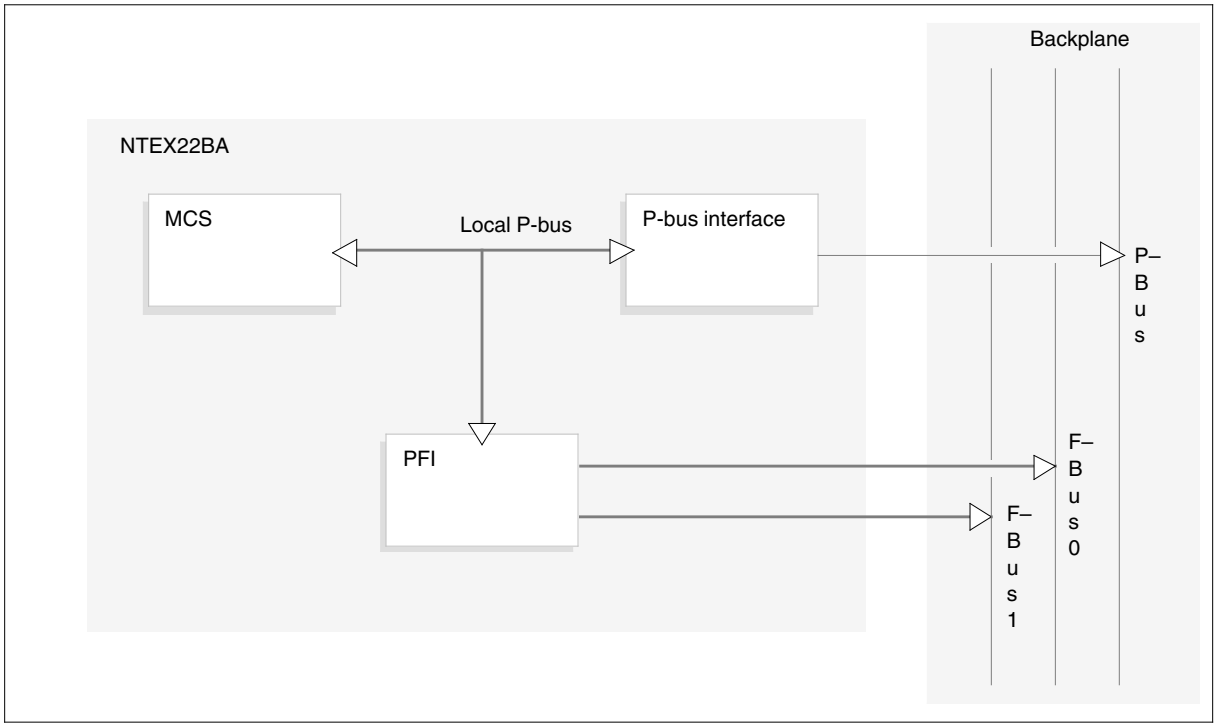
The NTEX22BA consists of the following functional blocks:

- microcontroller subsystem (MCS)
- P-bus interface
- F-bus interface (PFI)

The relationship between these functional blocks appears in the following figure.

## NTEX22BA (continued)

**NTEX22BA functional blocks**




### Microcontroller subsystem

The MCS block consists of the MCS with the clock, address and data buffers, application EPROM and control signal logic.

### Processor-bus interface

The P-bus interface consists of the reset circuits and P-bus circuits. These circuits include parity circuits, interrupt controllers, backplane buffering, address decoders, a control register and identification (ID) PROM.

### Processor to F-bus interface

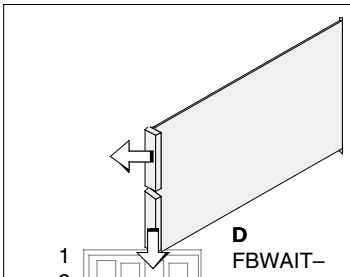
The PFI is on the local P-bus. The PFI contains the L-bus circuits and the two F-bus interfaces.

## Signaling

### Pin numbers

The pin numbers for NTEX22BA appear in the following figure.

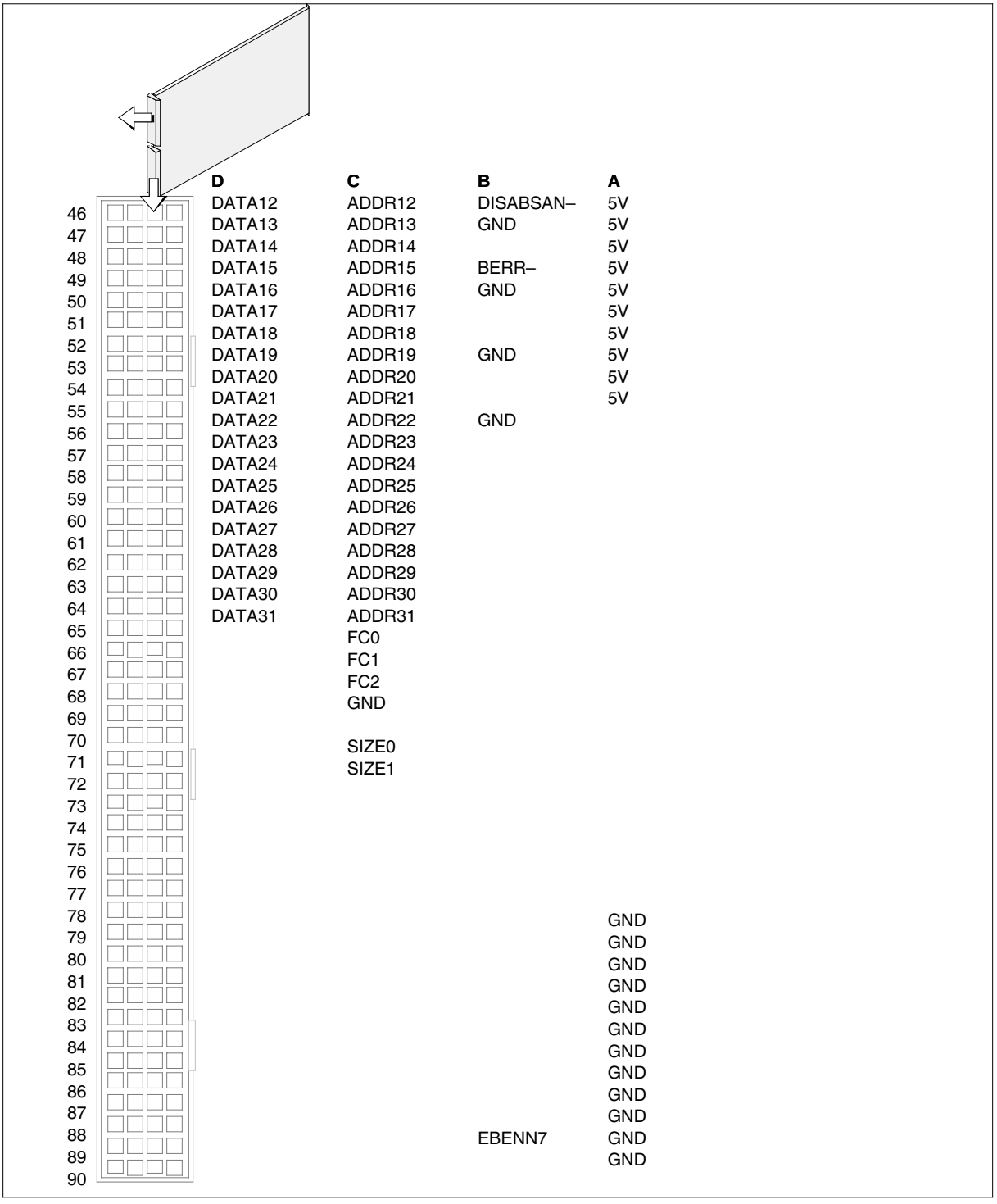
**NTEX22BA pin numbers (Part 1 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 1 | FBWAIT– | FAWAIT– | FAAD0 | GND |
| 2 | FBCLR– | FACLR– | FAAD1 | GND |
| 3 | FBREQ– | FAREQ– | FAAD2 | GND |
| 4 | FBPOLL– | FAPOLL– | FAAD3 | GND |
| 5 | FBRST– | FARST– | FAAD4 | GND |
| 6 | FBPACK– | FAPACK– | FAAD5 | GND |
| 7 | GND | GND | FAAD6 | GND |
| 8 | FBADREN– | FAADREN– | FAAD7 | GND |
| 9 | FBDATEN– | FADATEN– | FAPAR | GND |
| 10 | FBEOS– | FAEOS– | GND | GND |
| 11 | FBRACK– | FARACK– | FBAD0 | GND |
| 12 | FBRRDY– | FARRDY– | FBAD1 | GND |
| 13 | FBSCREN– | FASRCEN– | FBAD2 | RXDA |
| 14 | FBDSTEN– | FADSTEN– | FBAD3 | |
| 15 | GND | GND | FBAD4 | |
| 16 | GND | GND | FBAD5 | |
| 17 | PERINT6– | BUSGRI– | FBAD6 | DCDA |
| 18 | PERINT7– | BUSGRO– | FBAD7 | TXDA |
| 19 | BUSREQ– | PERINT2– | FBPAR | |
| 20 | | PERINT3– | GND | |
| 21 | GND | PERINT4– | | CTSA |
| 22 | BGACK– | PERINT5– | | |
| 23 | RSTOUT– | BUSLOCK– | | |
| 24 | PERINT1– | PERINT0– | | |
| 25 | BEN1– | BEN0– | | |
| 26 | BEN3– | BEN2– | | FACLKOUT |
| 27 | GND | | DS– | |
| 28 | WRT– | GND | | FBCLKOUT |
| 29 | EDTACK– | DTACK– | | HW4 |
| 30 | PARITY | | | GND |
| 31 | PRTYEN– | MEMERR– | FACLK | |
| 32 | FAS– | GND | | SH0 |
| 33 | DAS32– | CPUCLK | | SH1 |
| 34 | DATA00 | | | GND |
| 35 | DATA01 | ADDR01 | | FBCLK |
| 36 | DATA02 | ADDR02 | HW0 | |
| 37 | DATA03 | ADDR03 | HW1 | |
| 38 | DATA04 | ADDR04 | HW2 | |
| 39 | DATA05 | ADDR05 | HW3 | |
| 40 | DATA06 | ADDR06 | CMACT | GND |
| 41 | DATA07 | ADDR07 | ADDR00 | GND |
| 42 | DATA08 | ADDR08 | | GND |
| 43 | DATA09 | ADDR09 | | GND |
| 44 | DATA10 | ADDR10 | PBRST– | 5V |
| 45 | DATA11 | ADDR11 | PERR– | 5V |

# **NTEX22BA** (end)

### NTEX22BA pin numbers (Part 2 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 46 | DATA12 | ADDR12 | DISABSAN– | 5V |
| 47 | DATA13 | ADDR13 | GND | 5V |
| 48 | DATA14 | ADDR14 | | 5V |
| 49 | DATA15 | ADDR15 | BERR– | 5V |
| 50 | DATA16 | ADDR16 | GND | 5V |
| 51 | DATA17 | ADDR17 | | 5V |
| 52 | DATA18 | ADDR18 | | 5V |
| 53 | DATA19 | ADDR19 | GND | 5V |
| 54 | DATA20 | ADDR20 | | 5V |
| 55 | DATA21 | ADDR21 | | 5V |
| 56 | DATA22 | ADDR22 | GND | |
| 57 | DATA23 | ADDR23 | | |
| 58 | DATA24 | ADDR24 | | |
| 59 | DATA25 | ADDR25 | | |
| 60 | DATA26 | ADDR26 | | |
| 61 | DATA27 | ADDR27 | | |
| 62 | DATA28 | ADDR28 | | |
| 63 | DATA29 | ADDR29 | | |
| 64 | DATA30 | ADDR30 | | |
| 65 | DATA31 | ADDR31 | | |
| 66 | | FC0 | | |
| 67 | | FC1 | | |
| 68 | | FC2 | | |
| 69 | | GND | | |
| 70 | | | | |
| 71 | | SIZE0 | | |
| 72 | | SIZE1 | | |
| 73 | | | | |
| 74 | | | | |
| 75 | | | | |
| 76 | | | | |
| 77 | | | | |
| 78 | | | | GND |
| 79 | | | | GND |
| 80 | | | | GND |
| 81 | | | | GND |
| 82 | | | | GND |
| 83 | | | | GND |
| 84 | | | | GND |
| 85 | | | | GND |
| 86 | | | | GND |
| 87 | | | | GND |
| 88 | | | EBENN7 | GND |
| 89 | | | | GND |
| 90 | | | | |

# NTEX22BB

## Product description

The link peripheral processor (LPP) card uses the NTEX22BB integrated processor and frame transport bus (F-bus) interface card. This LPP is in application-specific units (ASU). These units require a minimum of 4 Mbytes of dynamic RAM (DRAM). The NTEX22BB is the operating equivalent of the NT9X13CA link general processor and the NT9X75AA processor bus (P-bus) to F-bus interface in the 3-slot ASU.

Applications from BCS33 or earlier that require a minimum of 4 Mbytes of memory use the NTEX22BA card. The network interface unit (NIU), and all applications that require more than 4 Mbytes of DRAM use the NTEX22BB card in BCS34.

The NTEX22BB functions are identical to functions in the ntex22AA, except in the following conditions:

- the BB card supports 32-bit asynchronous P-bus slaves
- the BB card has spared peripherals
- the BB card has 8 Mbytes of DRAM, where the AA card has 4 Mbytes of DRAM.

## Functional description

The NTEX22BB card provides a link general processor and dual F-bus interface capability.

The processor is responsible for the maintenance and operation of the two F-bus interface controllers. This processor is responsible for other attached maintenance functions and the application.

### Functional blocks

The NTEX22BB contains the following functional blocks:

- microcontroller subsystem (MCS)
- P-bus interface
- P-bus to F-bus interface (PFI)

The relationship between these functional blocks appears in the following figure.

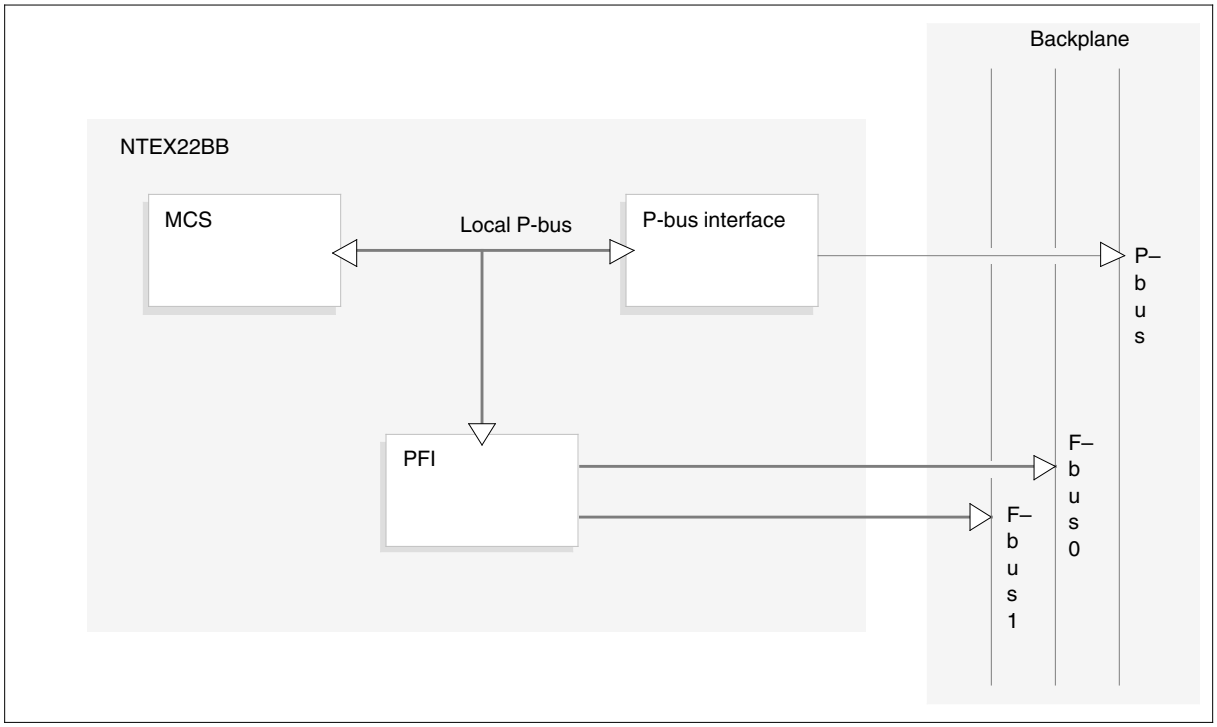
## NTEX22BB (continued)

### Microcontroller subsystem

The MCS block contains:

- the MCS with the MCS clock
- address buffers
- data buffers
- application EPROM
- control signal logic

**NTEX22BB functional blocks**




### Processor-bus interface

The P-bus interface contains the reset circuits and many P-bus circuits that include:

- parity circuits
- interrupt controllers
- backplane buffering
- address decoders

- control register
- identification (ID) PROM

### P-bus to F-bus interface

The PFI is on the local P-bus. The PFI contains the local-bus (L-bus) circuits and the two F-bus interfaces.

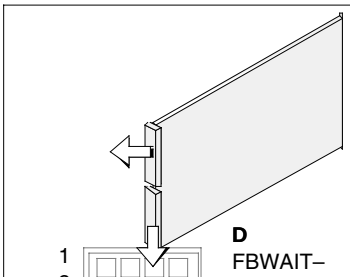
## Signaling

### Pin numbers

The pin numbers for NTEX22BB appear in the following figures.

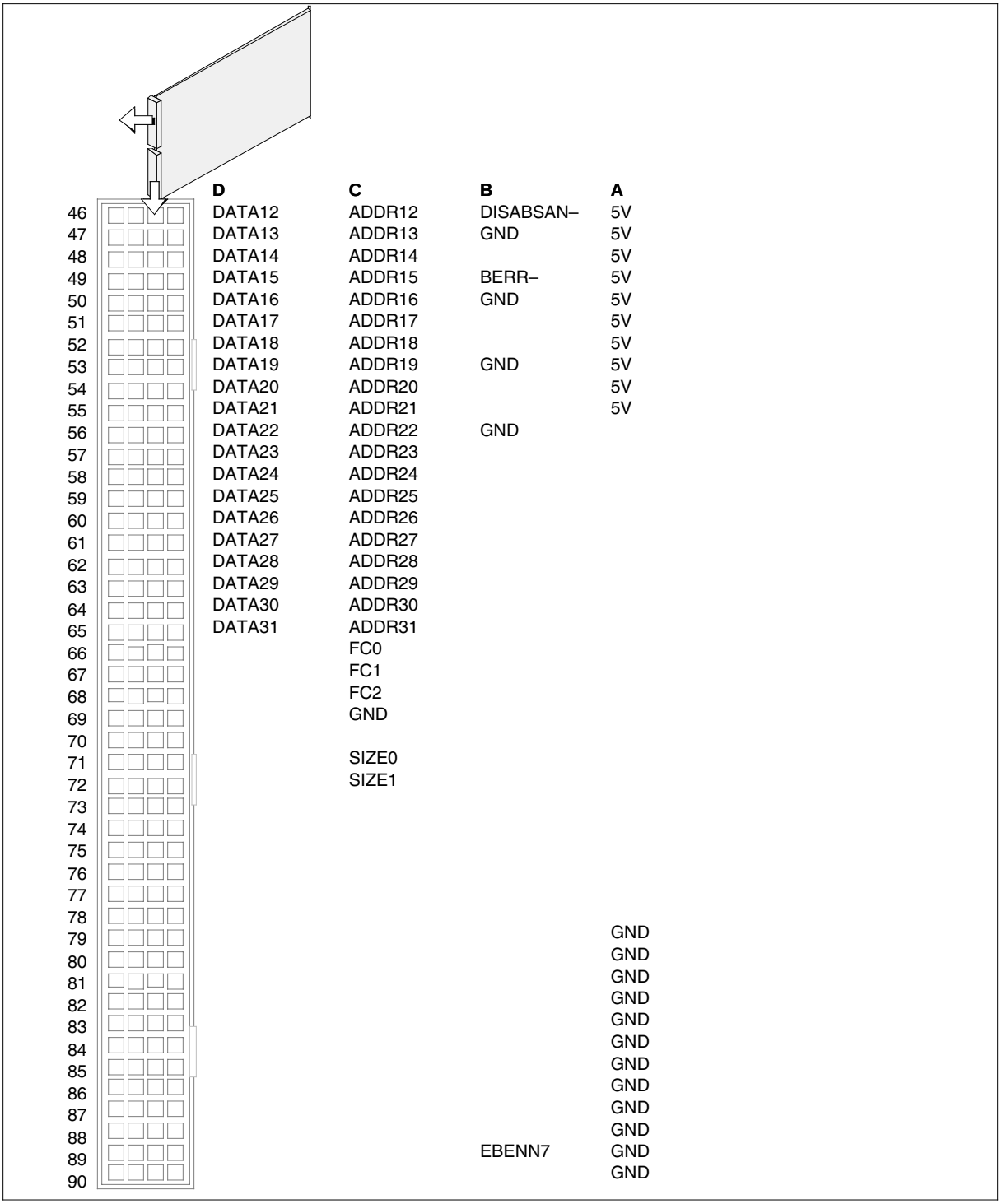
# **NTEX22BB** (continued)

### NTEX22BB pin numbers



| | D | C | B | A |
|---|---|---|---|---|
| 1 | FBWAIT– | FAWAIT– | FAAD0 | GND |
| 2 | FBCLR– | FACLR– | FAAD1 | GND |
| 3 | FBREQ– | FAREQ– | FAAD2 | GND |
| 4 | FBPOLL– | FAPOLL– | FAAD3 | GND |
| 5 | FBRST– | FARST– | FAAD4 | GND |
| 6 | FBPACK– | FAPACK– | FAAD5 | GND |
| 7 | GND | GND | FAAD6 | GND |
| 8 | FBADREN– | FAADREN– | FAAD7 | GND |
| 9 | FBDATEN– | FADATEN– | FAPAR | GND |
| 10 | FBEOS– | FAEOS– | GND | GND |
| 11 | FBRACK– | FARACK– | FBAD0 | GND |
| 12 | FBRRDY– | FARRDY– | FBAD1 | GND |
| 13 | FBSCREN– | FASRCEN– | FBAD2 | RXDA |
| 14 | FBDSTEN– | FADSTEN– | FBAD3 | |
| 15 | GND | GND | FBAD4 | |
| 16 | GND | GND | FBAD5 | |
| 17 | PERINT6– | BUSGRI– | FBAD6 | DCDA |
| 18 | PERINT7– | BUSGRO– | FBAD7 | TXDA |
| 19 | BUSREQ– | PERINT2– | FBPAR | |
| 20 | | PERINT3– | GND | |
| 21 | GND | PERINT4– | | CTSA |
| 22 | BGACK– | PERINT5– | | |
| 23 | RSTOUT– | BUSLOCK– | | |
| 24 | PERINT1– | PERINT0– | | |
| 25 | BEN1– | BEN0– | | |
| 26 | BEN3– | BEN2– | | FACLKOUT |
| 27 | GND | | DS– | |
| 28 | WRT– | GND | | FBCLKOUT |
| 29 | EDTACK– | DTACK– | | HW4 |
| 30 | PARITY | | | GND |
| 31 | PRTYEN– | MEMERR– | FACLK | |
| 32 | FAS– | GND | | SH0 |
| 33 | DAS32– | CPUCLK | | SH1 |
| 34 | DATA00 | | | GND |
| 35 | DATA01 | ADDR01 | | FBCLK |
| 36 | DATA02 | ADDR02 | HW0 | |
| 37 | DATA03 | ADDR03 | HW1 | |
| 38 | DATA04 | ADDR04 | HW2 | |
| 39 | DATA05 | ADDR05 | HW3 | |
| 40 | DATA06 | ADDR06 | CMACT | GND |
| 41 | DATA07 | ADDR07 | ADDR00 | GND |
| 42 | DATA08 | ADDR08 | | GND |
| 43 | DATA09 | ADDR09 | | GND |
| 44 | DATA10 | ADDR10 | PBRST– | 5V |
| 45 | DATA11 | ADDR11 | PERR– | 5V |

### NTEX22BB pin numbers



| | D | C | B | A |
|---|---|---|---|---|
| 46 | DATA12 | ADDR12 | DISABSAN– | 5V |
| 47 | DATA13 | ADDR13 | GND | 5V |
| 48 | DATA14 | ADDR14 | | 5V |
| 49 | DATA15 | ADDR15 | BERR– | 5V |
| 50 | DATA16 | ADDR16 | GND | 5V |
| 51 | DATA17 | ADDR17 | | 5V |
| 52 | DATA18 | ADDR18 | | 5V |
| 53 | DATA19 | ADDR19 | GND | 5V |
| 54 | DATA20 | ADDR20 | | 5V |
| 55 | DATA21 | ADDR21 | | 5V |
| 56 | DATA22 | ADDR22 | GND | |
| 57 | DATA23 | ADDR23 | | |
| 58 | DATA24 | ADDR24 | | |
| 59 | DATA25 | ADDR25 | | |
| 60 | DATA26 | ADDR26 | | |
| 61 | DATA27 | ADDR27 | | |
| 62 | DATA28 | ADDR28 | | |
| 63 | DATA29 | ADDR29 | | |
| 64 | DATA30 | ADDR30 | | |
| 65 | DATA31 | ADDR31 | | |
| 66 | | FC0 | | |
| 67 | | FC1 | | |
| 68 | | FC2 | | |
| 69 | | GND | | |
| 70 | | | | |
| 71 | | SIZE0 | | |
| 72 | | SIZE1 | | |
| 73 | | | | |
| 74 | | | | |
| 75 | | | | |
| 76 | | | | |
| 77 | | | | |
| 78 | | | | |
| 79 | | | | GND |
| 80 | | | | GND |
| 81 | | | | GND |
| 82 | | | | GND |
| 83 | | | | GND |
| 84 | | | | GND |
| 85 | | | | GND |
| 86 | | | | GND |
| 87 | | | | GND |
| 88 | | | | GND |
| 89 | | | EBENN7 | GND |
| 90 | | | | GND |

# NTEX22CA

## Product description

The NTEX22CA is an integrated processor bus (P-bus) and frame transport bus (F-bus) interface (IPF) card. The card is functionally identical to the NTEX22BB card, with the following improvements:

- The CA card has 32 Mbytes of dynamic random-access memory (DRAM), while the BB card has 8 Mbyte of DRAM.
- The CA card uses the M68LC060 processor, while the BB card uses the M68030 processor.
- The clock coming from the motherboard has frequency increased to 25 MHz.

The components listed above are part of the NTNX4820 microcontroller subsystem (MCS), which increases the processing speed of the card.

The NTEX22CA card also offers a hardware implementation of the F-bus throttling feature that maximizes bandwidth use of the F-bus without any effect on software real-time performance.

### Location

NTEX22CA is a part of the application-specific units (ASU) located on a link interface shelves (LIS) in a link peripheral processor (LPP) cabinet or enhanced LPP (ELPP) cabinet.

## Functional description

The main functions of the NTEX22CA card are as follows:

- to provide a link general processor for all LPP applications, except application processor units (APU) that use the NT9X14DB memory card. The processor is responsible for the maintenance and operation of the two F-bus interface controllers (FIC) and other on-board maintenance functions.
- to provide dual F-bus interface capability
- to provide distributed adaptive F-bus throttle (DAFT) mechanism

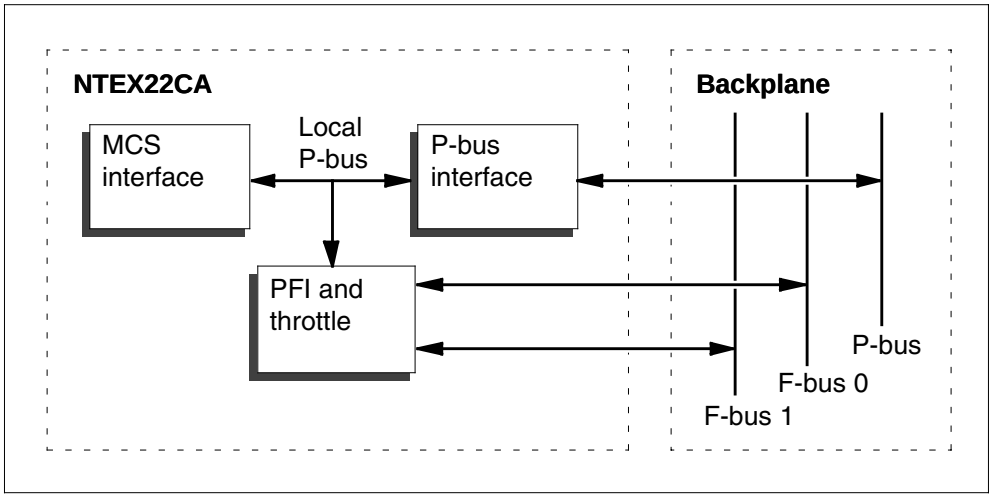
### Functional blocks

NTEX22CA has the following functional blocks:

- MCS interface
- P-bus interface
- P-bus to F-bus interface (PFI) and throttle

The following figure shows the relationship of the functional blocks.

**NTEX22CA functional blocks**




## MCS interface

The MCS interface block consists of the following components:

- the NTNX4820 MCS with its clock
- address buffers
- data buffers
- application erasable programmable read-only memory (EPROM)
- control signal logic that provides the interface between the MCS and the backplane

## P-bus interface

The P-bus interface consists of the reset circuitry and a variety of P-bus circuits, including

- parity circuitry
- interrupt controllers
- backplane buffers
- address decoders
- control register
- identification (ID) PROM

## **NTEX22CA** (continued)

### P-bus to F-bus interface

The PFI block consists of the following components:

- P-bus interface
- two F-bus interface controllers (FIC)
- local RAM (LRAM)

The components listed above are connected to a local bus (L-bus). FICs control data that moves between the F-bus and LRAM. A P-bus can access LRAM and the FIC control registers directly through the P-bus to L-bus interface.

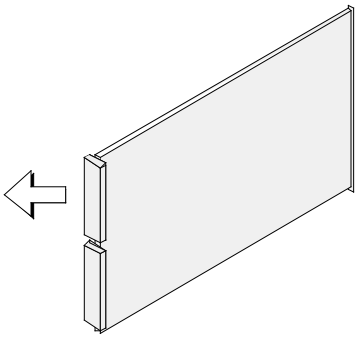
## Signaling

### Pin outs

The following figure shows the pin outs for NTEX22CA.

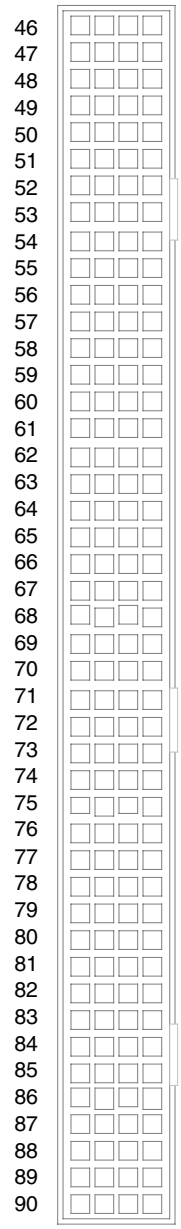
**NTEX22CA pin outs (Part 1 of 2)**

| | D | C | B | A |
|---|---|---|---|---|
| 1 | FBWAIT– | FAWAIT– | FAAD0 | GND |
| 2 | FBCLR– | FACLR– | FAAD1 | GND |
| 3 | FBREQ– | FAREQ– | FAAD2 | GND |
| 4 | FBPOLL– | FAPOLL– | FAAD3 | GND |
| 5 | FBRST– | FARST– | FAAD4 | GND |
| 6 | FBPACK– | FAPACK– | FAAD5 | GND |
| 7 | GND | GND | FAAD6 | GND |
| 8 | FBADREN– | FAADREN– | FAAD7 | GND |
| 9 | FBDATEN– | FADATEN– | FAPAR | GND |
| 10 | FBEOS– | FAEOS– | GND | GND |
| 11 | FBRACK– | FARACK– | FBAD0 | GND |
| 12 | FBRRDY– | FARRDY– | FBAD1 | GND |
| 13 | FBSRCEN– | FASRCEN– | FBAD2 | RXDA |
| 14 | FBDSTEN– | FADSTEN– | FBAD3 | |
| 15 | GND | GND | FBAD4 | |
| 16 | GND | GND | FBAD5 | |
| 17 | PERINT6– | BUSGRI– | FBAD6 | DCDA |
| 18 | PERINT7– | BUSGRO– | FBAD7 | TXDA |
| 19 | BUSREQ– | PERINT2– | FBPAR | |
| 20 | | PERINT3– | GND | |
| 21 | GND | PERINT4– | | CTSA |
| 22 | GBACK– | PERINT5– | | |
| 23 | RSTOUT– | BUSLOCK– | | |
| 24 | PERINT1– | PERINT0– | | |
| 25 | BEN1– | BEN0– | FASPARE | |
| 26 | BEN3– | BEN2– | FBSPARE | FACLKOUT |
| 27 | GND | | DS– | |
| 28 | WRT– | GND | | FBCLKOUT |
| 29 | EDTACK– | DTACK– | | HW4 |
| 30 | PARITY | | | GND |
| 31 | PRTYEN– | MEMERR– | | FACLK |
| 32 | FAS– | GND | | SH0 |
| 33 | DAS32– | CPUCLK | | SH1 |
| 34 | DATA00 | | | GND |
| 35 | DATA01 | ADDR01 | | FBCLK |
| 36 | DATA02 | ADDR02 | HW0 | |
| 37 | DATA03 | ADDR03 | HW1 | |
| 38 | DATA04 | ADDR04 | HW2 | |
| 39 | DATA05 | ADDR05 | HW3 | |
| 40 | DATA06 | ADDR06 | CMACT | GND |
| 41 | DATA07 | ADDR07 | ADDR00 | GND |
| 42 | DATA08 | ADDR08 | | GND |
| 43 | DATA09 | ADDR09 | | GND |
| 44 | DATA10 | ADDR10 | PBRST | 5 V |
| 45 | DATA11 | ADDR11 | PERR– | 5 V |



# **NTEX22CA** (continued)

### NTEX22CA pin outs (Part 2 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 46 | DATA12 | ADDR12 | DISABSAN– | 5 V |
| 47 | DATA13 | ADDR13 | GND | 5 V |
| 48 | DATA14 | ADDR14 | | 5 V |
| 49 | DATA15 | ADDR15 | BERR– | 5 V |
| 50 | DATA16 | ADDR16 | GND | 5 V |
| 51 | DATA17 | ADDR17 | | 5 V |
| 52 | DATA18 | ADDR18 | | 5 V |
| 53 | DATA19 | ADDR19 | GND | 5 V |
| 54 | DATA20 | ADDR20 | | 5 V |
| 55 | DATA21 | ADDR21 | | 5 V |
| 56 | DATA22 | ADDR22 | GND | |
| 57 | DATA23 | ADDR23 | | |
| 58 | DATA24 | ADDR24 | | |
| 59 | DATA25 | ADDR25 | | |
| 60 | DATA26 | ADDR26 | | |
| 61 | DATA27 | ADDR27 | | |
| 62 | DATA28 | ADDR28 | | |
| 63 | DATA29 | ADDR29 | | |
| 64 | DATA30 | ADDR30 | | |
| 65 | DATA31 | ADDR31 | | |
| 66 | | FC0 | | |
| 67 | | FC1 | | |
| 68 | | FC2 | | |
| 69 | | GND | | |
| 70 | | | | |
| 71 | | SIZE0 | | |
| 72 | | SIZE1 | | |
| 73 | | | | |
| 74 | | | | |
| 75 | | | | |
| 76 | | | | |
| 77 | | | | |
| 78 | | | | |
| 79 | | | | GND |
| 80 | | | | GND |
| 81 | | | | GND |
| 82 | | | | GND |
| 83 | | | | GND |
| 84 | | | | GND |
| 85 | | | | GND |
| 86 | | | | GND |
| 87 | | | | GND |
| 88 | | | | GND |
| 89 | | | EBENN7– | GND |
| 90 | | | | GND |

# Technical data

## Power requirements

The following table shows the power requirements for the NTEX22CA.

**NTEX22CA power requirements**

| Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|
| Supply voltage | 4.75 V | 5 V | 5.25 V |
| Supply current | | 5.4 V | |

# NTEX25AA

## Product description

The NTEX25AA network interface unit (NIU) channel bus controller (CBC) card in the link peripheral processor (LPP) allows direct network connection to the LPP. The NTEX25AA takes channels from the network and transmits these channels to the application specific units (ASU) over the C–bus. The NTEX25AA takes channels from the ASUs through the C–bus. The NTEX25AA transmits these channels to both planes of the network.

The NIU is a hot standby. Unit 0 uses the NTEX25AA that interfaces to C–bus 0. Unit 1 uses the NTEX25BA that interfaces to C–bus 1.

### Location

The NTEX25AA is in one of the two center ASU positions of an ASU shelf.

## Functional description

On the receive side, the NTEX25AA takes data from both planes and performs selection. The NTEX25AA bases selection integrity and parity. The NTEX25AA performs selection on a channel condition. The link data (6–bit data) changes to the C–bus format (10–bit data). On the transmit side, the NTEX25AA takes data from the C–bus. The NTEX25AA sends this data to the network on both planes. All channels include parity and accuracy.

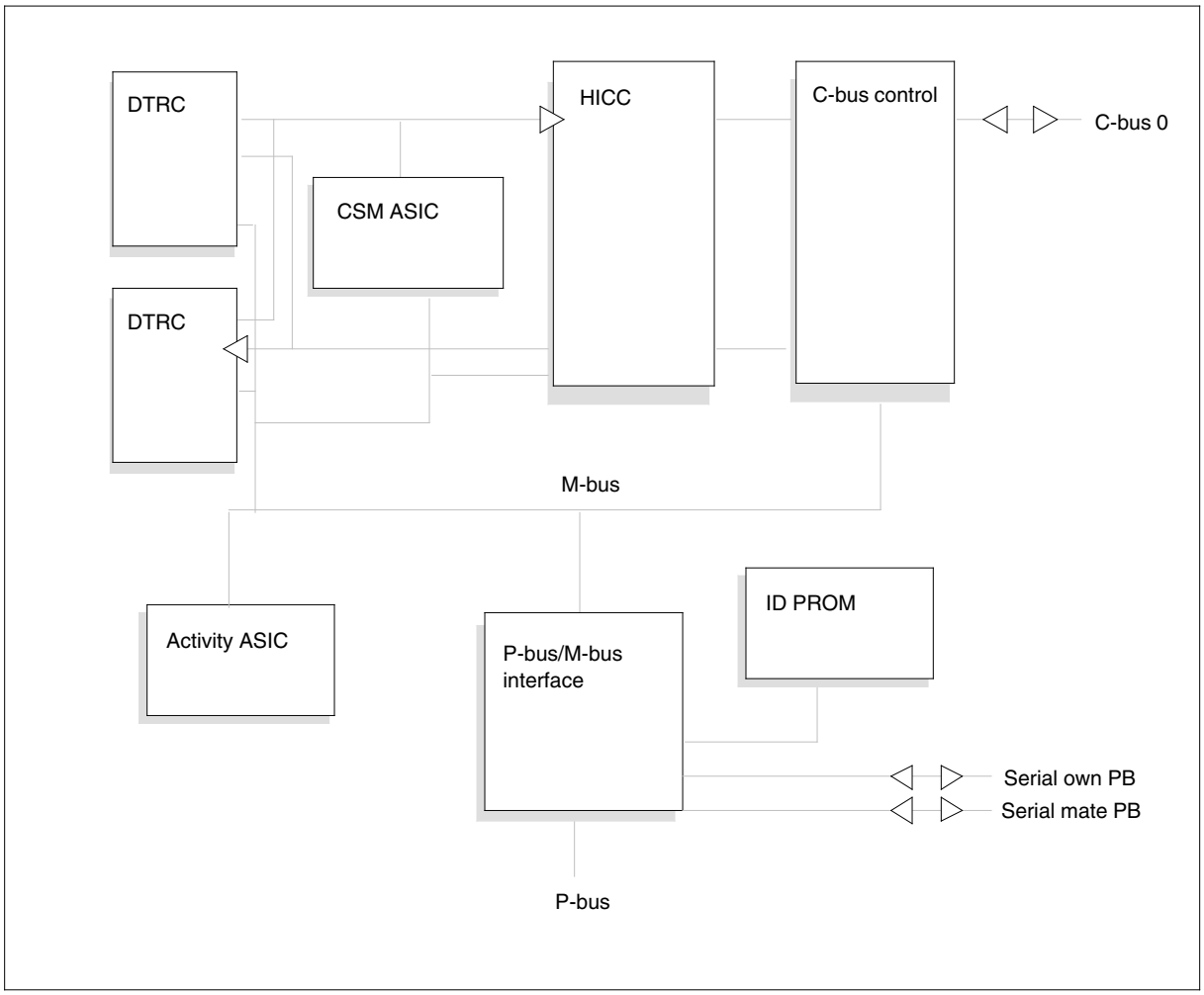
### Functional blocks

The NTEX25AA contains the following functional blocks:

- DS–512 transmit receive controller (DTRC)
- host interface chip with channel supervision message (HICC)
- channel supervision message (CSM) application–specific integrated circuit (ASIC)
- C–bus control
- activity ASIC
- P–bus/M–bus interface
- identification (ID) PROM

The relationship between these functional blocks appears in the following figure.

**NTEX25AA functional blocks**




## DS–512 transmit receive controller

The two DTRCs receive the channel data from the link interface paddle board (the NTEX28AA). These DTRCs use an elastic store to perform frame alignment. One DTRC interfaces to the link paddle board (PB) associated with plane 0. The other DTRC interfaces to the link PB associated with plane 1.

## Host interface chip with channel supervision message

The HICC takes data from the two DRTCs. The HICC performs plane selection for each channel. The HICC sends the data in parallel form to the C–bus control circuits. The HICC takes data from the C–bus control circuits and sends the data to the DTRCs.

## **NTEX25AA** (continued)

### Channel supervision message application–specific integrated circuit

The CSM ASIC chip extracts the integrity or CSM from the incoming data and checks this data against a known value. This chip passes the results to the HICC. The HICC uses this information to perform plane selection. This chip generates the integrity value for transmission on the outgoing channels.

### C–bus control

The C–bus control is in charge of the channel transfers over the C–bus.

### Activity ASIC

The activity ASIC performs two important functions:

- determines which two CBCs must be active
- synchronizes the internal CBC clocks to an external clock source (either plane 0, plane 1, or the mate)

### P–bus/M–bus interface

The P–bus gives the card access to all registers and ASICs from the P–bus. This action allows the NTEX22AA to control the NTEX25AA. The M–bus is a multiplexed version of the P–bus, and interfaces to all ASICs.

### Identification PROM

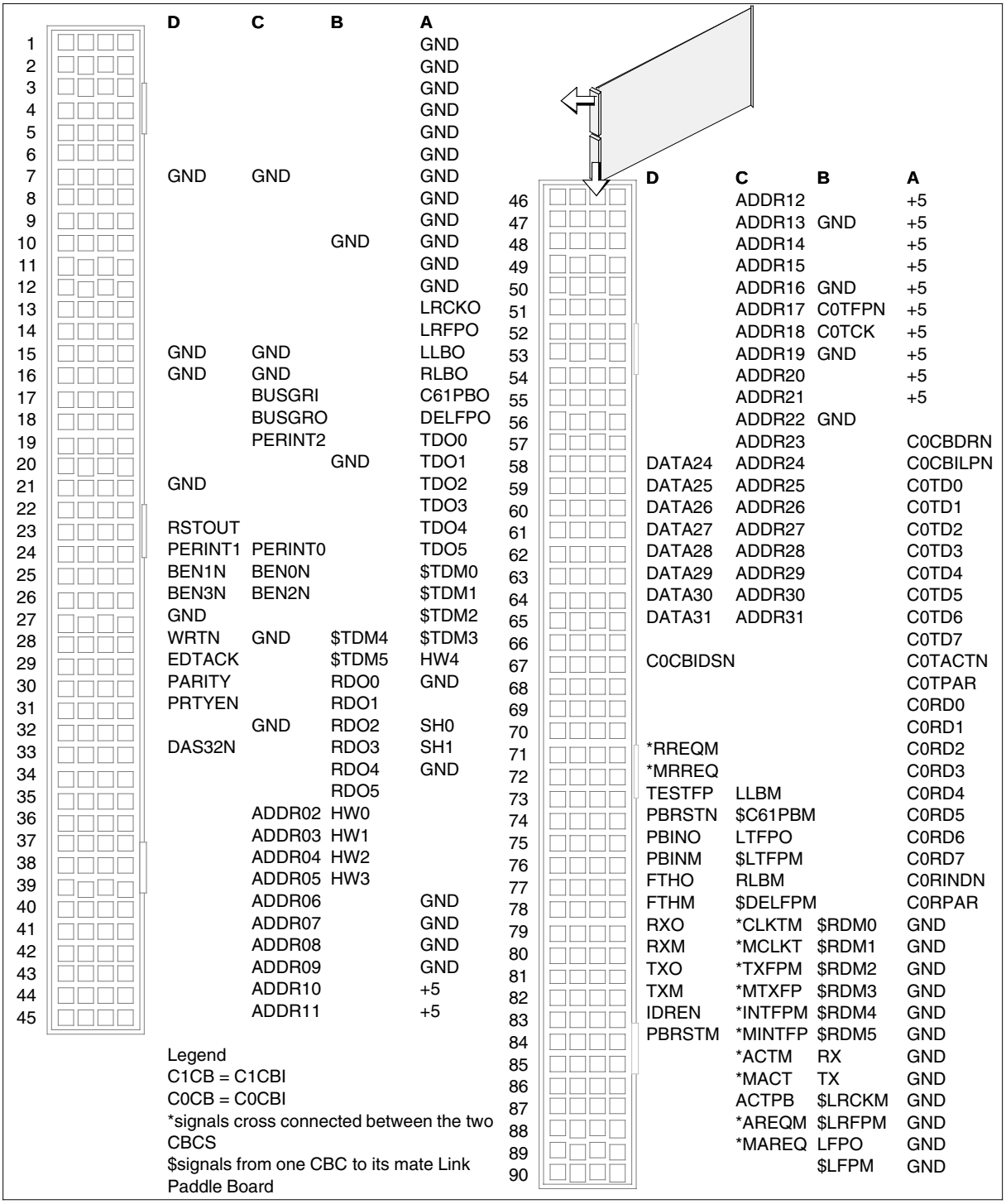
The NTEX22AA accesses the ID PROM from the P–bus. The ID PROM contains manufacturing information about the NTEX25AA.

## Signaling

### Pin numbers

The pin numbers for NTEX25AA appear in the following figure.

### NTEX25AA pin numbers



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | GND |
| 2 | | | | GND |
| 3 | | | | GND |
| 4 | | | | GND |
| 5 | | | | GND |
| 6 | | | | GND |
| 7 | GND | GND | | GND |
| 8 | | | | GND |
| 9 | | | | GND |
| 10 | | | GND | GND |
| 11 | | | | GND |
| 12 | | | | GND |
| 13 | | | | LRCKO |
| 14 | | | | LRFPO |
| 15 | GND | GND | | LLBO |
| 16 | GND | GND | | RLBO |
| 17 | | BUSGRI | | C61PBO |
| 18 | | BUSGRO | | DELFPO |
| 19 | | PERINT2 | | TDO0 |
| 20 | | | GND | TDO1 |
| 21 | GND | | | TDO2 |
| 22 | | | | TDO3 |
| 23 | RSTOUT | | | TDO4 |
| 24 | PERINT1 | PERINT0 | | TDO5 |
| 25 | BEN1N | BEN0N | | $TDM0 |
| 26 | BEN3N | BEN2N | | $TDM1 |
| 27 | GND | | | $TDM2 |
| 28 | WRTN | GND | $TDM4 | $TDM3 |
| 29 | EDTACK | | $TDM5 | HW4 |
| 30 | PARITY | | RDO0 | GND |
| 31 | PRTYEN | | RDO1 | |
| 32 | | GND | RDO2 | SH0 |
| 33 | DAS32N | | RDO3 | SH1 |
| 34 | | | RDO4 | GND |
| 35 | | | RDO5 | |
| 36 | | ADDR02 | HW0 | |
| 37 | | ADDR03 | HW1 | |
| 38 | | ADDR04 | HW2 | |
| 39 | | ADDR05 | HW3 | |
| 40 | | ADDR06 | | GND |
| 41 | | ADDR07 | | GND |
| 42 | | ADDR08 | | GND |
| 43 | | ADDR09 | | GND |
| 44 | | ADDR10 | | +5 |
| 45 | | ADDR11 | | +5 |

| | D | C | B | A |
|---|---|---|---|---|
| 46 | | ADDR12 | | +5 |
| 47 | | ADDR13 | GND | +5 |
| 48 | | ADDR14 | | +5 |
| 49 | | ADDR15 | | +5 |
| 50 | | ADDR16 | GND | +5 |
| 51 | | ADDR17 | C0TFPN | +5 |
| 52 | | ADDR18 | C0TCK | +5 |
| 53 | | ADDR19 | GND | +5 |
| 54 | | ADDR20 | | +5 |
| 55 | | ADDR21 | | +5 |
| 56 | | ADDR22 | GND | |
| 57 | | ADDR23 | | C0CBDRN |
| 58 | DATA24 | ADDR24 | | C0CBILPN |
| 59 | DATA25 | ADDR25 | | C0TD0 |
| 60 | DATA26 | ADDR26 | | C0TD1 |
| 61 | DATA27 | ADDR27 | | C0TD2 |
| 62 | DATA28 | ADDR28 | | C0TD3 |
| 63 | DATA29 | ADDR29 | | C0TD4 |
| 64 | DATA30 | ADDR30 | | C0TD5 |
| 65 | DATA31 | ADDR31 | | C0TD6 |
| 66 | | | | C0TD7 |
| 67 | C0CBIDSN | | | C0TACTN |
| 68 | | | | C0TPAR |
| 69 | | | | C0RD0 |
| 70 | | | | C0RD1 |
| 71 | *RREQM | | | C0RD2 |
| 72 | *MRREQ | | | C0RD3 |
| 73 | TESTFP | LLBM | | C0RD4 |
| 74 | PBRSTN | $C61PBM | | C0RD5 |
| 75 | PBINO | LTFPO | | C0RD6 |
| 76 | PBINM | $LTFPM | | C0RD7 |
| 77 | FTHO | RLBM | | C0RINDN |
| 78 | FTHM | $DELFPM | | C0RPAR |
| 79 | RXO | *CLKTM | $RDM0 | GND |
| 80 | RXM | *MCLKT | $RDM1 | GND |
| 81 | TXO | *TXFPM | $RDM2 | GND |
| 82 | TXM | *MTXFP | $RDM3 | GND |
| 83 | IDREN | *INTFPM | $RDM4 | GND |
| 84 | PBRSTM | *MINTFP | $RDM5 | GND |
| 85 | | *ACTM | RX | GND |
| 86 | | *MACT | TX | GND |
| 87 | | ACTPB | $LRCKM | GND |
| 88 | | *AREQM | $LRFPM | GND |
| 89 | | *MAREQ | LFPO | GND |
| 90 | | | $LFPM | GND |

Legend
C1CB = C1CBI
C0CB = C0CBI
*signals cross connected between the two CBCS
$signals from one CBC to its mate Link Paddle Board

# NTEX25BA

## Product description

The NTEX25BA network interface unit (NIU) channel bus controller (CBC) card is in the link peripheral processor (LPP). The NIU allows direct network connection to the LPP. The NTEX25BA takes channels from the network and transmits the channels to the application specific units (ASU) over the C-bus. The NTEX25BA takes channels from the ASUs over the C-bus and transmits these channels to both planes of the network.

The NIU is a hot standby. Unit 1 uses the NTEX25BA that interfaces to C-bus 1. Unit 0 uses the NTEX25AA that interfaces to C-bus 0.

### Location

The NTEX25BA is in one of the two center ASU positions of an ASU shelf.

## Functional description

On the receive side, the NTEX25BA takes data from both planes and performs selection. The NTEX25BA bases this selection on accuracy and parity. The NTEX25BA performs selection for each channel. The link data (6-bit data) changes to the C-bus format (10-bit data). On the transmit side, the NTEX25BA takes data from the C-bus. The NTEX25BA sends this data to the network on both planes. All channels include parity and accuracy.

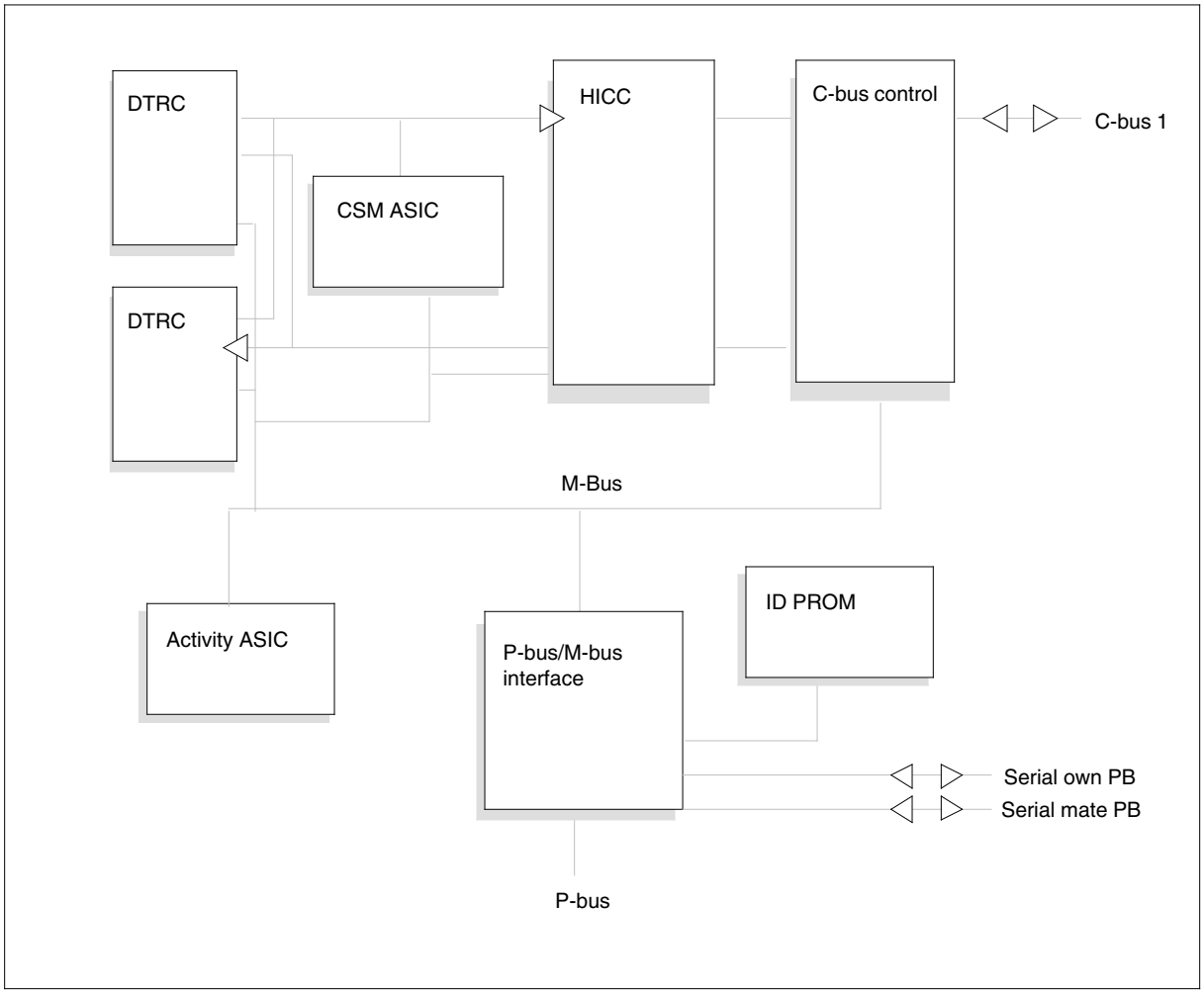
### Functional blocks

The NTEX25BA contains the following functional blocks:

- DS-512 transmit receive controller (DTRC)
- host interface chip with channel supervision message (HICC)
- channel supervision message (CSM) application-specific integrated circuit (ASIC)
- C-bus control
- activity ASIC
- P-bus/M-bus interface
- identification (ID) PROM

The relationship between these functional blocks appears in the following figure.

**NTEX25BA functional blocks**




## DS-512 transmit receive controller

The two DTRCs receive the channel data from the link interface paddle board (the NTEX28AA). These DTRCs use an elastic store to perform frame alignment. One DTRC interfaces to the link paddle board (PB) associated with plane 0. The other DTRC interfaces to the link PB associated with plane 1.

## Host interface chip with channel supervision message

The HICC takes data from the two DRTCs and performs plane selection for each channel. The HICC sends the channels in parallel form to the C-bus control circuits. The HICC receives data on channels from the C-bus control circuits and sends this data to the DTRCs.

## **NTEX25BA** (continued)

### Channel supervision message application-specific integrated circuit

The CSM ASIC chip extracts the integrity or CSM from the incoming data and checks this data against a known value. The chip passes the results to the HICC. The HICC uses this information to perform plane selection. The CSM ASIC generates the integrity value for transmission on the outgoing channels.

### C-bus control

The C-bus control regulates the channel transfers over the C-bus.

### Activity ASIC

The activity ASIC performs two main functions. The ASIC determines which of the two CBCs are active. The ASIC synchronizes the internal CBC clocks to an external clock source (plane 0, plane 1, or the mate).

### P-bus/M-bus interface

The P-bus gives the card access to all registers and ASICs from the P-bus. This function allows the NTEX22BB to control the NTEX25BA. The M-bus is a multiplexed version of the P-bus, and interfaces to all ASICs.

### Identification PROM

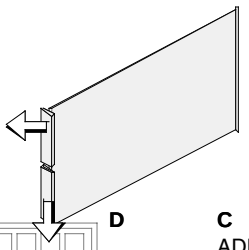
The NTEX22BB from the P-bus accesses the ID PROM. This PROM contains manufacturing information about the NTEX25BA.

## Signaling

### Pin numbers

The pin numbers for the NTEX25BA appear in the following figures.

### NTEX25BA pin numbers



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | GND |
| 2 | | | | GND |
| 3 | | | | GND |
| 4 | | | | GND |
| 5 | | | | GND |
| 6 | | | | GND |
| 7 | GND | GND | | GND |
| 8 | | | | GND |
| 9 | | | | GND |
| 10 | | | GND | GND |
| 11 | | | | GND |
| 12 | | | | GND |
| 13 | | | | LRCKO |
| 14 | | | | LRFPO |
| 15 | GND | GND | | LLBO |
| 16 | GND | GND | | RLBO |
| 17 | | BUSGRI | | C61PBO |
| 18 | | BUSGRO | | DELFPO |
| 19 | | PERINT2 | | TDO0 |
| 20 | | | GND | TDO1 |
| 21 | GND | | | TDO2 |
| 22 | | | | TDO3 |
| 23 | RSTOUT | | | TDO4 |
| 24 | PERINT1 | PERINT0 | | TDO5 |
| 25 | BEN1N | BEN0N | | $TDM0 |
| 26 | BEN3N | BEN2N | | $TDM1 |
| 27 | GND | | | $TDM2 |
| 28 | WRTN | GND | $TDM4 | $TDM3 |
| 29 | EDTACK | | $TDM5 | HW4 |
| 30 | PARITY | | RDO0 | GND |
| 31 | PRTYEN | | RDO1 | |
| 32 | | GND | RDO2 | SH0 |
| 33 | DAS32N | | RDO3 | SH1 |
| 34 | | | RDO4 | GND |
| 35 | | | RDO5 | |
| 36 | | ADDR02 | HW0 | |
| 37 | | ADDR03 | HW1 | |
| 38 | | ADDR04 | HW2 | |
| 39 | | ADDR05 | HW3 | |
| 40 | | ADDR06 | | GND |
| 41 | | ADDR07 | | GND |
| 42 | | ADDR08 | | GND |
| 43 | | ADDR09 | | GND |
| 44 | | ADDR10 | | +5 |
| 45 | | ADDR11 | | +5 |

| | D | C | B | A |
|---|---|---|---|---|
| 46 | | ADDR12 | | +5 |
| 47 | | ADDR13 | GND | +5 |
| 48 | | ADDR14 | | +5 |
| 49 | | ADDR15 | | +5 |
| 50 | | ADDR16 | GND | +5 |
| 51 | | ADDR17 | C0TFPN | +5 |
| 52 | | ADDR18 | C0TCK | +5 |
| 53 | | ADDR19 | GND | +5 |
| 54 | | ADDR20 | | +5 |
| 55 | | ADDR21 | | +5 |
| 56 | | ADDR22 | GND | |
| 57 | | ADDR23 | | C0CBDRN |
| 58 | DATA24 | ADDR24 | | C0CBILPN |
| 59 | DATA25 | ADDR25 | | C0TD0 |
| 60 | DATA26 | ADDR26 | | C0TD1 |
| 61 | DATA27 | ADDR27 | | C0TD2 |
| 62 | DATA28 | ADDR28 | | C0TD3 |
| 63 | DATA29 | ADDR29 | | C0TD4 |
| 64 | DATA30 | ADDR30 | | C0TD5 |
| 65 | DATA31 | ADDR31 | | C0TD6 |
| 66 | | | | C0TD7 |
| 67 | C0CBIDSN | | | C0TACTN |
| 68 | | | | C0TPAR |
| 69 | | | | C0RD0 |
| 70 | | | | C0RD1 |
| 71 | *RREQM | | | C0RD2 |
| 72 | *MRREQ | | | C0RD3 |
| 73 | TESTFP | LLBM | | C0RD4 |
| 74 | PBRSTN | $C61PBM | | C0RD5 |
| 75 | PBINO | LTFPO | | C0RD6 |
| 76 | PBINM | $LTFPM | | C0RD7 |
| 77 | FTHO | RLBM | | C0RINDN |
| 78 | FTHM | $DELFPM | | C0RPAR |
| 79 | RXO | *CLKTM | $RDM0 | GND |
| 80 | RXM | *MCLKT | $RDM1 | GND |
| 81 | TXO | *TXFPM | $RDM2 | GND |
| 82 | TXM | *MTXFP | $RDM3 | GND |
| 83 | IDREN | *INTFPM | $RDM4 | GND |
| 84 | PBRSTM | *MINTFP | $RDM5 | GND |
| 85 | | *ACTM | RX | GND |
| 86 | | *MACT | TX | GND |
| 87 | | ACTPB | $LRCKM | GND |
| 88 | | *AREQM | $LRFPM | GND |
| 89 | | *MAREQ | LFPO | GND |
| 90 | | | $LFPM | GND |

Legend
C1CB = C1CBI
C0CB = C0CBI
*signals cross connected between the two CBCS
$signals from one CBC to its mate Link Paddle Board

# NTEX26AA

## Product description

The CCS7 LIU (LIU7) uses the NTEX26AA link interface unit (LIU) channel-bus interface (CBI) circuit pack. The LIU7 uses the NTEX26AA in a link peripheral processor (LPP) equipped for channelized access.

### Location

The NTEX26AA is behind the NT9X76AA signaling terminal (ST) in an LIU7.

## Functional description

The NTEX26AA provides an interface between the ST serial link and one channel of the two central channel buses (C-bus). The NTEX26AA provides the following functions:

- a full-featured C-bus interface that includes support for activity switching and C-bus loop back
- data transfers between one C-bus channel and the ST at 48 Kbps, 56 Kbps, or 64 Kbps
- a data processor to support firmware features like DS-0A control code reception, and paddle board and line loopback functionality

### Functional blocks

The NTEX26AA contains the following functional blocks:

- CBI data processor (CDP)
- two C-bus interfaces

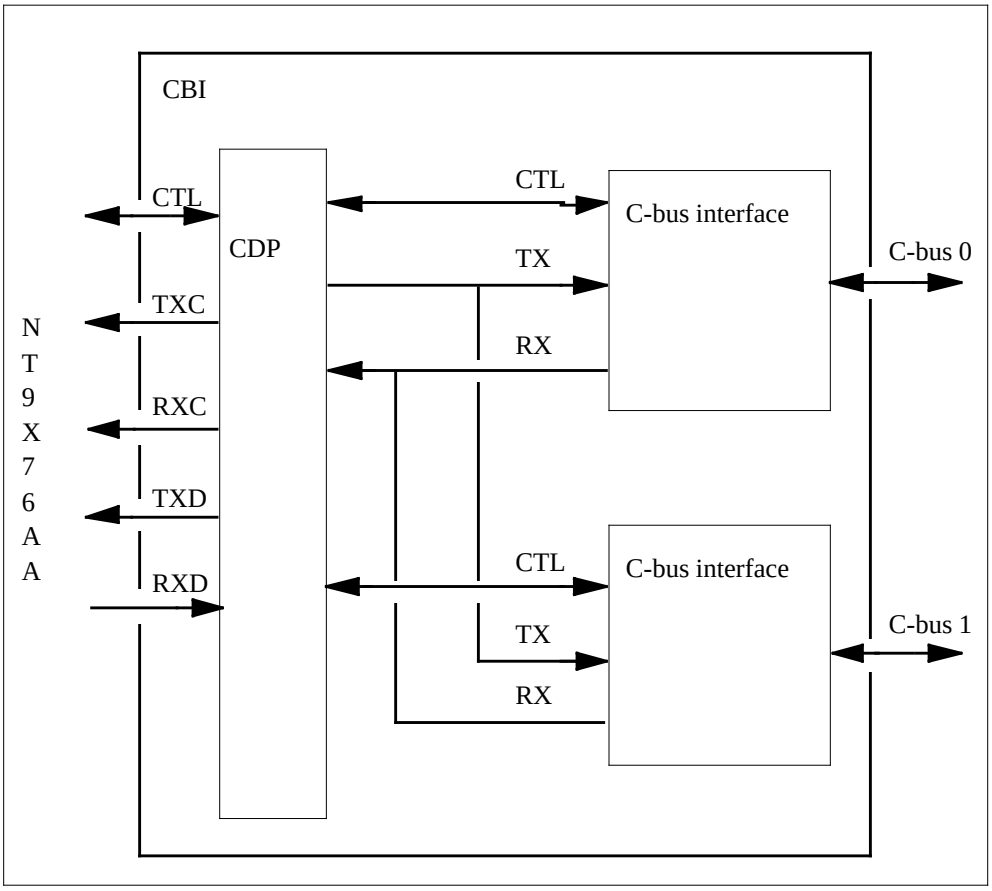
The relationship between the functional blocks appears in the following figure.

### Channel-bus interface data processor

The CDP block contains the non-duplicated digital hardware of the CBI. This hardware includes a microcontroller and the following support circuits:

- clock
- EPROM
- address decoder
- parallel port
- channel number register
- serial interface state machine
- C-bus activity state machine

**NTEX26AA functional blocks**




### Channel-bus interface

Each C-bus interface block contains the C-bus interface circuits and control logic. Duplicate the circuits and logic to make sure that a single fault does not bring both C-buses down. Control circuits that do not need duplication belong to the CDP block.

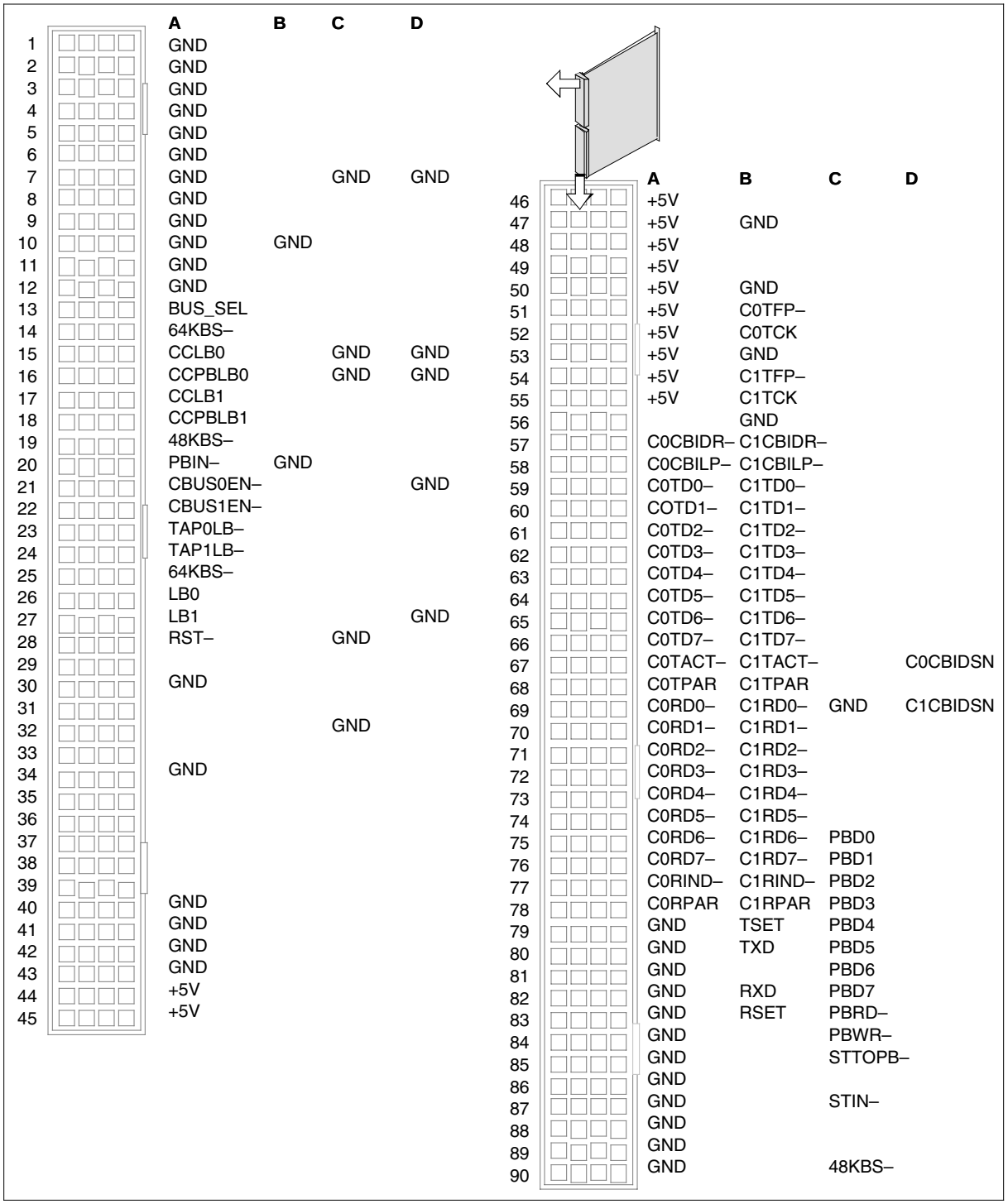
## Signaling

### Pin numbers

The pin numbers for the NTEX26AA appear in the following figure.

# **NTEX26AA** (continued)

### NTEX26AA pin numbers



## Technical data

### Power requirements

The NTEX26AA CBI uses the same power entry circuit as other STP cards. The NTEX26AA is compatible with the range of voltage the power converter provides.

# NTEX26BA

## Product description

The Cbus multi link interface unit (MLIU) paddle board provides the interface between the high speed signaling terminal (HST) and the SS7 high speed link. The SS7 high speed link comes from the enhanced network (ENET) or the dual shelf network (DST). The NTEX26BA paddle board can interface a maximum of four different SS7 links to the HST.

### Location

The NTEX26BA is in the MLIU of the signaling transfer point (STP) switch.

## Functional description

The NTEX26BA provides a duplicate Cbus interface to prevent a single hardware fault from interrupting the normal operation of both Cbuses. The paddle board allows operating company personnel to program the assignment of any four of 495 Cbus channels. The NTEX26BA supports odd/even/all/none bit inversion mode.

### Functional blocks

The NTEX26BA includes four main functional blocks.

NTEX26BA includes the functional blocks that follow:

- Cbus interface
- HST interface
- data controller
  - — central processing unit (CPU) interface block
  - — Cbus timing block
  - — HST timing block
  - — Cbus to HST converter
  - — HST to Cbus converter
  - — bit inversion
  - — parity block
  - — activity block
- identification programmable read-only memory (ID PROM)

### Cbus interface

The Cbus interface includes a set of open collector bus transceivers to drive the different Cbus signals. These transceivers provide a high current drive to allow

the terminations to be near the bus impedance. The transceivers enter to disable mode when the power is not available.

The 0 and 1 Cbuses connect to the buffers. Two activity bits, one from each Cbus, determine which Cbus the system selects.

### HST interface

The HST interface includes a set of buffers to drive the HST CPU signals and the serial communication controller (SCC) clocks.

### Data controller

The data controller includes the following sections:

- Cbus timing block
- HST timing block
- CPU interface block
- Cbus to HST block
- HST to Cbus block
- parity block
- inversion block
- activity block
- loopback block

#### CPU interface block

The CPU interface block allows the CPU on the HST pack to access the data controller registers. The interface is based on the control signals PBCS- and R/W, and the cycle termination signal DSACK. On a read cycle, data is correct from the falling edge of the paddle board chip select (PBCS-) signal until the DMS-100 cancels the data. On a write cycle, the system samples the data bus on the rising edge of the PBCS- signal. The system begins the HST processor on the falling edge of the PBCS- signal. The system samples the R/W signal and determines if the cycle is read or write.

If the DMS-100 performs a read cycle with a correct address access to the requested device, the DMS-100 outputs the requested data on the CPU data bus. The system asserts the DTACK- signal. After the system samples the DTACK- signal, the processor samples data on the falling edge of the CPU clock. If the DMS-100 performs a write cycle with a correct address, the system sets the cycle to the requested device. The system asserts the DTACK- signal. The system writes the data sampled on the rising edge of the PBCS- signal to the indicated register.

## NTEX26BA (continued)

### Cbus timing block

This block is responsible for the production of the required signals for the Cbus side. This block holds the time slot (TS) counters. The Cbus timing block also contains the following sections:

- *Counter block.* This block contains two TS counters. Each TS counter is synchronized and counts clocks from its Cbus. The system resets the TS counters on the rising edge of their Cbus FP. The transmit (xmit) TS comes one TS before the received (rcv) TS.
- *TS memory block.* The TS memory block holds the serial numbers of the four required Cbus TSs. The HST CPU initializes four registers with the required Cbus TSs carrying the SS7 signaling for the MLIU. Each register holds the TS for one SS7 link. The system can select any TS to connect to any of the four HST TSs.
- *Comparator block.* This block creates the enable read and write control signals for the Cbus receive and transmit registers. Cbus 0 and Cbus 1 each have a set of comparators. Each set has four comparators that compare the value in the TS memory block to the value of the correct TS counter. The system samples the comparator signals to determine the enable write signals.

### HST timing block

This block creates the required signals for the HST circuit. The HST timing block takes the 2Mhz clocks and Frame pulses from the 8Mhz clock. The FP is synchronized to the FP from the active Cbus. The HST timing block includes the following two pieces:

- *Counter block.* This block includes a 2 bit and an 8 bit counter that operate with the 8Mhz clock. These counters are synchronized to the FP from the active Cbus. The system loads the counter with the value 3F9h. The 8 bit counter increments when the 2 bit counter is equal to 01h.
- *Comparator block.* This block creates the enable signals for the shift registers and the HST FP. The DMS-100 uses one enable signal for parallel read from the rcv register to the rcv shift register. The system uses this enable signal to write from the xmit shift register to the xmit registers. The DMS-100 uses the second enable signal to enable the shift registers to clock in or out serial data to the HST.

### Cbus to HST converter

The Cbus to HST converter pulls out the four correct Cbus TSs, and inserts them on the data stream to the HST. This block is responsible for the loopback to the HST (PBLB).

This block includes 4x8 bit input registers and 4x8 bit shift registers, to make up one 32 bit shift register. The converter input registers of the active and not active Cbuses store the Cbus TSs. When the HST counter value is 002 h, the Data_Swap signal from the comparator block enables the data transfer from the four input registers from the active Cbus. The system transfers the data to the 32 bit shift register. The comparator block activates the HST_trn_TS signal, and the system shifts the data to the HST.

### HST to Cbus converter

This block transmits data to the Cbuses. The converter collects data from the TSs of the data stream from the HST and inserts the data on the Cbus TSs. Each Cbus has an outgoing register. On the rising edge of each Cbus clock, the system sends this data to the Cbuses. The HST marks a specific TS active to cause it to provide the enable signals. When the the Data_Swap signal is active, the system copies the data from the shift register to the output registers.

### Bit inversion

The paddle board supports even, odd, all, and none types of bit inversion. Input/output registers determine the bit inversion mode on a channel basis.

### Parity block

This block includes the following two bits:

- *Parity bit.* For the incoming TS, this bit checks the Cbus incoming data parity. The system compares the result of the incoming data to the activity bit. If the data and the activity bit are different, the DMS-100 generates an RPAR_ERR signal. For the outgoing TS, this bit calculates the parity bit for the system to send with the data to the Cbus. The system calculates the parity bit from the 8 bit data and the C_ERR signal from the activity block. The C_RPAR signal completes to an odd parity number. If the number of ones and the C_ERR is even, the circuit outputs a one. In other occurrences, the system outputs a zero.
- *Indication bit.* This block checks and notifies the Cbus about errors in the receive or transmit TS data. The DMS-100 checks parity error on the receive Cbus TS. The DMS-100 checks contention on the transmit Cbus TS. The system sends the C_ERR signal to the channel bus controller (CBC). The CBC translates the C_ERR signal as a request to change the active Cbus.

### Activity block

The activity block creates the signals for the change on the active Cbus without affecting the communication path. To change the active Cbus, the card has separate Cbus and HST circuits.

## NTEX26BA (continued)

The HST circuit uses the card clock. The Cbus circuit has two identical separate circuits that each handle Cbus signals and data. The system stores the data received through both Cbuses, but sends the data from the active Cbus to the HST.

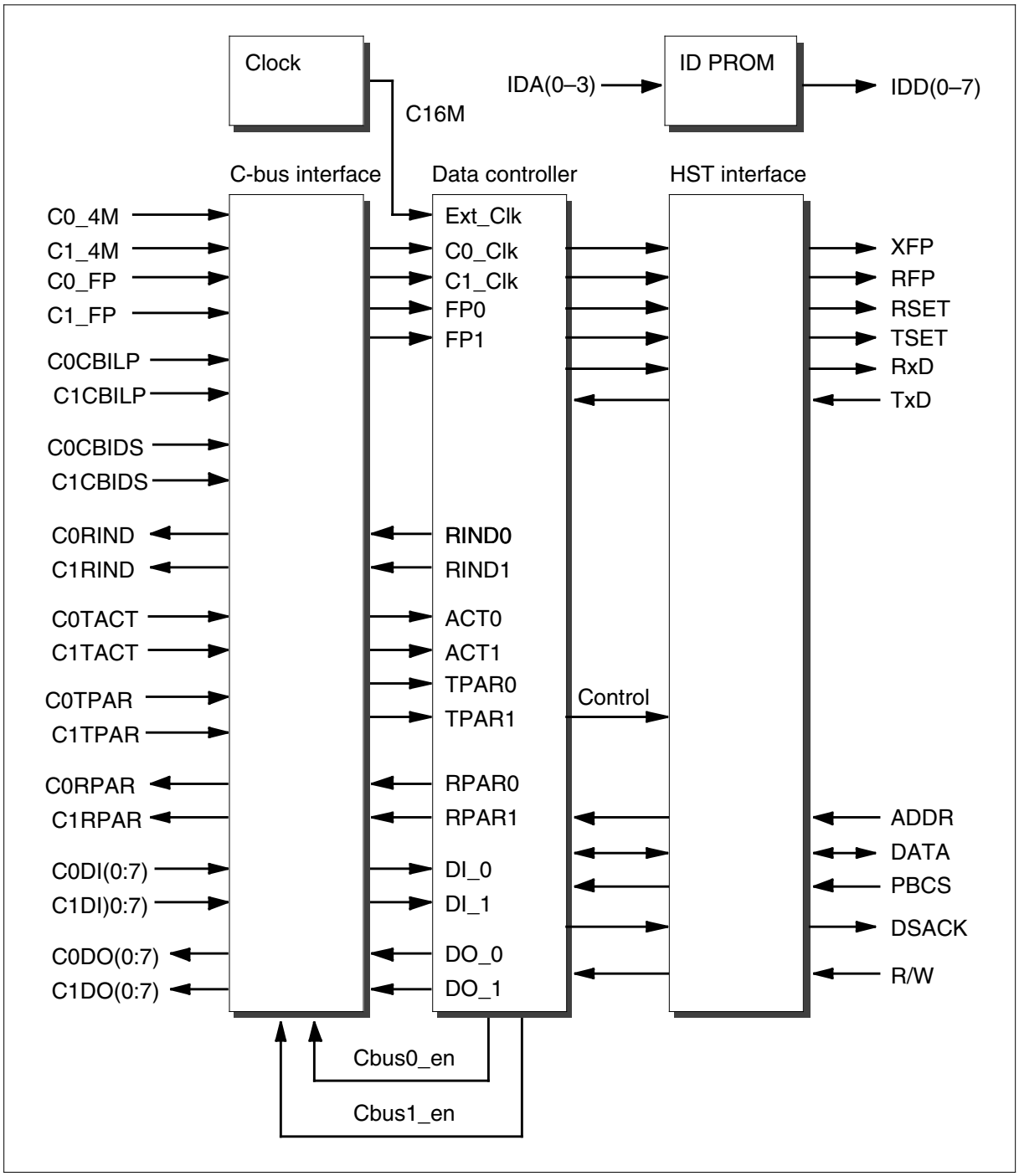
The system requires double sampling of the activity signals and CFP.

### ID PROM

The ID PROM uses 128Kx8 flash memory. The HST access to the ID PROM is in 16 sequential words, where one word is equal to 16 bits. Only the least important byte has correct values. The system performs arbitration at the HST to allow the integrated processor and Fbus card (IPF) to access the ID PROM directly.

The figure that follows shows the relationship of the functional blocks.

**NTEX26BA functional blocks**



## **NTEX26BA** (continued)

# Signaling

### Pin numbers

The table that follows shows the pin numbers for NTEX26BA.

**Pin numbers for NTEX26BA (Sheet 1 of 4)**

| PIN number | Signal | | | |
|---|---|---|---|---|
| | **A** | **B** | **C** | **D** |
| 1 | GND | | | |
| 2 | GND | | | |
| 3 | GND | | | |
| 4 | GND | | | |
| 5 | GND | | | |
| 6 | GND | | | |
| 7 | GND | | GND | Reset |
| 8 | GND | | | |
| 9 | GND | | | |
| 10 | GND | GND | | |
| 11 | GND | | | |
| 12 | GND | | | |
| 13 | PBA00 | | | |
| 14 | PBA01 | | | |
| 15 | PBA02 | | GND | GND |
| 16 | PBA03 | | GND | GND |
| 17 | PBA04 | | | |
| 18 | PBA05 | | | |
| 19 | PBA06 | | | |
| 20 | PBin | GND | | |
| 21 | PBA07 | CLK8A | | GND |

**Pin numbers for NTEX26BA (Sheet 2 of 4)**

| PIN number | Signal | | | |
|---|---|---|---|---|
| | **A** | **B** | **C** | **D** |
| 22 | PBA08 | | | |
| 23 | PBA09 | CLK8B | | |
| 24 | PBA10 | | | |
| 25 | PBA11 | | | |
| 26 | | | | |
| 27 | PBA12 | | | GND |
| 28 | Reset | | GND | |
| 29 | | | | |
| 30 | GND | | | |
| 31 | | | | |
| 32 | | | GND | |
| 33 | | | | |
| 34 | GND | | | |
| 35 | | | | |
| 36 | | | | |
| 37 | | | | |
| 38 | | | | |
| 39 | | | | |
| 40 | GND | | | |
| 41 | GND | | | |
| 42 | GND | | | |
| 43 | GND | | | |
| 44 | Power +5 | | | |

## NTEX26BA (continued)

**Pin numbers for NTEX26BA (Sheet 3 of 4)**

| PIN number | Signal | | | |
|---|---|---|---|---|
| | **A** | **B** | **C** | **D** |
| 45 | Power +5 | | | |
| 46 | Power +5 | | | |
| 47 | Power +5 | GND | | |
| 48 | Power +5 | | | |
| 49 | Power +5 | | | |
| 50 | Power +5 | GND | | |
| 51 | Power +5 | C0TFP- | | |
| 52 | Power +5 | C0TCK | | |
| 53 | Power +5 | GND | | |
| 54 | Power +5 | C1TFP- | | |
| 55 | Power +5 | C1TCK | | |
| 56 | | GND | | |
| 57 | C0CBIDR- | C1CBIDR- | | |
| 58 | C0CBILP- | C1CBILP- | | |
| 59 | C0TD0- | C1TD0- | | |
| 60 | C0TD1- | C1TD1- | | |
| 61 | C0TD2- | C1TD2- | | |
| 62 | C0TD3- | C1TD3- | | |
| 63 | C0TD4- | C1TD4- | | |
| 64 | C0TD5- | C1TD5- | | |
| 65 | C0TD6- | C1TD6- | | |
| 66 | C0TD7- | C1TD6- | | |
| 67 | C0TACT- | C1TACT- | | C0CBIDS |

**Pin numbers for NTEX26BA (Sheet 4 of 4)**

| PIN number | Signal | | | |
|---|---|---|---|---|
| | **A** | **B** | **C** | **D** |
| 68 | C0TPAR | C1TPAR- | | |
| 69 | C0RD0- | C1RD0- | Reset 2 | C1CBIDS |
| 70 | C0RD1- | C1RD1- | | |
| 71 | C0RD2- | C1RD2- | | SCC1DR |
| 72 | C0RD3- | C1RD3- | | SCC1DT |
| 73 | C0RD4- | C1RD4- | | SCC1CR |
| 74 | C0RD5- | C1RD5- | | SCC1CT |
| 75 | C0RD6- | C1RD6- | PBD00 | PBD08 |
| 76 | C0RD7- | C1RD7- | PBD01 | PBD09 |
| 77 | C0RIND- | C1RIND- | PBD02 | PBD10 |
| 78 | C0RPAR | C1RPAR | PBD03 | PBD11 |
| 79 | GND | TSET | PBD04 | PBD12 |
| 80 | GND | TxD | PBD05 | PBD13 |
| 81 | GND | XFP | PBD06 | PBD14 |
| 82 | GND | RxD | PBD07 | PBD15 |
| 83 | GND | RSET | RS232_TX | PBD16 |
| 84 | GND | RFP | RS232_RX | PBD17 |
| 85 | GND | PBA14 | PBCS- | PBD18 |
| 86 | GND | PBA15 | DTACK- | PBD19 |
| 87 | GND | SCC3DR | HSTin | SCC2DR |
| 88 | GND | SCC3DT | RXW | SCC2DT |
| 89 | GND | SCC3CR | HST_Int- | SCC2CR |
| 90 | GND | SCC3CT | PBA13 | SCC2CT |

## **NTEX26BA** (end)

# Technical data

### Power requirements

The NTEX26BA card normally uses 5 V of power.

# NTEX28AA

## Product description

The link peripheral processor (LPP) uses the NTEX28AA network interface unit (NIU) DS30 link interface paddle board (LPB) for channel access. The card is a 4-port DS30 link interface board. This card provides DS30 links between the peripheral side (P-side) of the network and the channel bus controllers (CBC). This card provides the links in an application-specific unit (ASU) shelf.

### Location

Two NTEX28AA cards are behind each CBC in the center two positions of an ASU shelf.

## Functional description

The NTEX28AA performs the following functions:

- converts DS30 serial data to 6-bit parallel data, and 6-bit parallel data to serial data
- converts serial data rate to parallel data rate, and parallel data rate to serial data rate
- sends data from the network to both CBCs
- selects data from the active CBC and sends this data to the network
- provides a serial link to the active CBC to check processor sanity, read the ID PROM, and assert lock to mate signal (LOCK)
- provides loopback path that CBC requests
- provides unit (data) selection that the NTEX28AA bases on the ACTPB and LOCK signals

### Functional blocks

The NTEX28AA contains the following functional blocks:

- identification (ID) PROM
- -5V power
- clock generator
- hybrids
- DS30 interface
- plane selection
- R41 bit rate converter (BRC)

## **NTEX28AA** (continued)

- loopback control
- differential drivers and receivers

### Identification PROM

The microcontroller of the clock generator reads the ID PROM. The microcontroller reads the ID PROM when the active CBC sends a request through the serial link.

### -5V power

Set up of the correct reference voltage for the 12-bit digital-to-analog converter in the fully-digital phase-locked loop (FDPLL) requires 5V. The FDPLL is in the clock generator.

### Clock generator

The clock generator block generates the serial rate clock (SCLK) and the FP97 frame pulse for R41 serial data transfers. A microcontroller controls the FDPLL in this block. The microcontroller communicates with the active CBC through a serial link. The active CBC commands the microcontroller to do the following:

- query the card status
- read the ID PROM
- assert or deassert the LOCK signal

The LOCK signal forces the selection from the mate R41 BRC for transmission to the network.

### Hybrids

The DS30 transformer hybrids provide the interface between the DS30 interface ASIC and the twisted pair DS30 cable. Each hybrid handles two bidirectional ports.

### DS30 interface

The DS30 interface provides the means for communication between the hybrids and the R41 BRCs. This interface receives biphase data from the hybrid and extracts the clock, frame pulse, and data. The interface passes this information to the two R41 BRCs. The DS30 interface combines transmit clock, frame pulse and data from the selected R41 BRC to biphase signals. The interface sends the data to the transformer hybrid. The hybrid sends the data to the DS30 port.

### Plane selection

The plane selection block contains a programmable array logic (PAL) that selects:

- the serial output data
- the serial frame pulse from the two R41 BRCs the PAL bases on the activity to LPB signal ACTPB
- the lock mate signal LOCK

### R41 bit rate converter

The R41 BRC converts and formats data. In the receive direction, the R41 BRC takes serial data from the DS30 interface. The R41 BRC converts this data to parallel data at the parallel rate. In the transmit direction, the R41 BRC takes parallel data from the CBC. The R41 BRC converts this data to serial data at the serial rate.

### Loopback control

The loopback control block contains two PALs: a loopback PAL and a delay PAL. The loopback PAL decodes loopback input from the CBCs. The loopback PAL sends the loopback controls to the R41 BRCs, the DS30 interface, and the delay PAL. The loopback PAL generates a 4 KHz version of the extracted DS30 link frame pulse for loss detection by the microcontroller. The loopback PAL selects the reference frame pulse from the CBCs. At the request of the active CBC, the loopback PAL generates the signal PBRST that sets the card again.

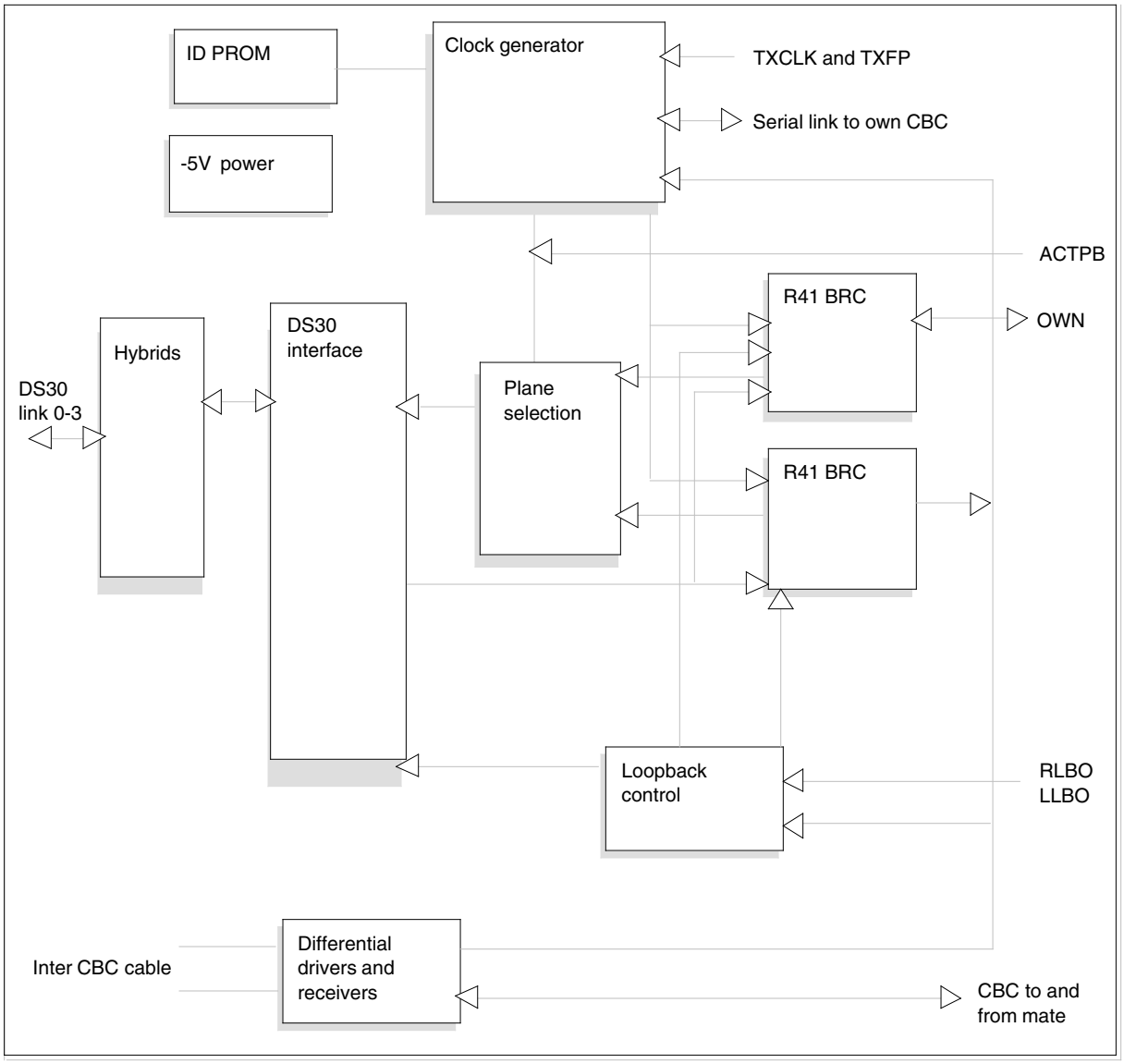
### Differential drivers and receivers

The DS30 LPB uses differential line driver and receiver pairs for inter-CBC communication. The DS30 LPB requires two cables. For correct connection, one cable must connect from window two of one LPB to window three of the other LPB.

The relationship between these functional blocks appears in the following figure.

## **NTEX28AA** (continued)

### NTEX28AA functional blocks

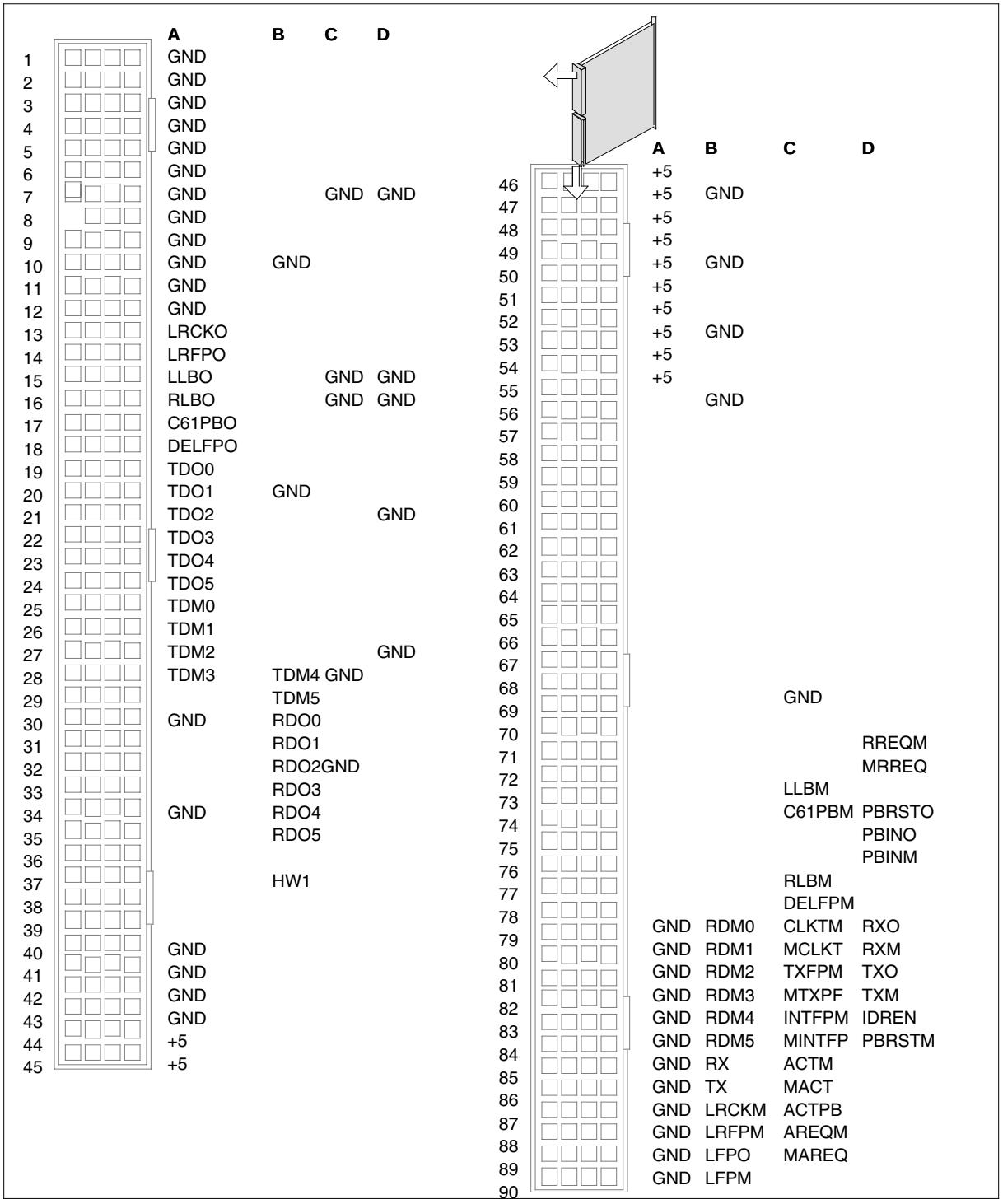



# Signaling

## Pin numbers

The pin numbers for the NTEX28AA appear in the following figure. The pin numbers for connectors J1, J2, J3, and J4 appear in the tables that follow the figure.

### NTEX28AA pin numbers



## **NTEX28AA** (continued)

**Connector J1 pin numbers**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | TXP2 | 5 | TXP3 |
| 2 | TXN2 | 6 | TXN3 |
| 3 | RXP2 | 7 | RXP3 |
| 4 | RXN2 | 8 | RXN3 |

**Connector J2 pin numbers**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | TXP0 | 5 | TXP1 |
| 2 | TXN0 | 6 | TXN1 |
| 3 | RXP0 | 7 | RXP1 |
| 4 | RXN0 | 8 | RXN1 |

**Connector J3 pin numbers (Sheet 1 of 2)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | CBCTX+ | 32 | ILFPM- |
| 2 | CBCTX- | 33 | OC61PBM+ |
| 3 | OTDM0+ | 34 | OC61PBM- |
| 4 | OTDM0- | 35 | |
| 5 | OTDM1+ | 36 | |
| 6 | OTDM1- | 37 | ODELFPM+ |
| 7 | OTDM2+ | 38 | ODELFPM- |
| 8 | OTDM2- | 39 | CLKTM+ |
| 9 | OTDM3+ | 40 | CLKTM- |
| 10 | OTDM3- | 41 | TXFPM+ |
| 11 | OTDM4+ | 42 | TXFPM- |
| 12 | OTDM4- | 43 | INTFPM+ |

**Connector J3 pin numbers (Sheet 2 of 2)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 13 | OTDM5+ | 44 | INTFPM- |
| 14 | OTDM5- | 45 | ACTM+ |
| 15 | IRDM0+ | 46 | ACTM- |
| 16 | IRDM0- | 47 | AREQM+ |
| 17 | IRDM1+ | 48 | AREQM- |
| 18 | IRDM1- | 49 | RREQM+ |
| 19 | IRDM2+ | 50 | RREQM- |
| 20 | IRDM2- | 51 | OLLBM+ |
| 21 | IRDM3+ | 52 | OLLBM- |
| 22 | IRDM3- | 53 | ORLBM+ |
| 23 | IRDM4+ | 54 | ORLBM- |
| 24 | IRDM4- | 55 | IRX+ |
| 25 | IRDM5+ | 56 | IRX- |
| 26 | IRDM5- | 57 | OTX+ |
| 27 | ILRCKM+ | 58 | OTX- |
| 28 | ILRCKM- | 59 | IPBINM |
| 29 | ILRFPM+ | 60 | ODREN |
| 30 | ILRFPM- | 61 | OPBRTMN+ |
| 31 | ILFPM+ | 62 | OPBRTMN- |

**Connector J4 pin numbers (Sheet 1 of 3)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 10 | CBCRX+ | 32 | OLFPM- |
| 2 | CBCRX- | 33 | IC61PBM+ |
| 3 | ITDM0+ | 34 | IC61PBM- |

## **NTEX28AA** (continued)

**Connector J4 pin numbers (Sheet 2 of 3)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 4 | ITDM0- | 35 | |
| 5 | ITDM1+ | 36 | |
| 6 | ITDM1- | 37 | IDELFPM+ |
| 7 | ITDM2+ | 38 | IDELFPM- |
| 8 | ITDM2- | 39 | MCLKT+ |
| 9 | ITDM3+ | 40 | MCLKT- |
| 10 | ITDM3- | 41 | MTXFP+ |
| 11 | ITDM4+ | 42 | MTXFP- |
| 12 | ITDM4- | 43 | MINTFP+ |
| 13 | ITDM5+ | 44 | MINTFP- |
| 14 | ITDM5- | 45 | MACT+ |
| 15 | ORDM0+ | 46 | MACT- |
| 16 | ORDM0- | 47 | MAREQ+ |
| 17 | ORDM1+ | 48 | MAREQ- |
| 18 | ORDM1- | 49 | MRREQ+ |
| 19 | ORDM2+ | 50 | MRREQ- |
| 20 | ORDM2- | 51 | ILLBM+ |
| 21 | ORDM3+ | 52 | ILLBM- |
| 22 | ORDM3- | 53 | IRLBM+ |
| 23 | ORDM4+ | 54 | IRLBM- |
| 24 | ORDM4- | 55 | ORX+ |
| 25 | ORDM5+ | 56 | ORX- |
| 26 | ORDM5- | 57 | ITX+ |
| 27 | OLRCKM+ | 58 | ITX- |

**Connector J4 pin numbers (Sheet 3 of 3)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 28 | OLRCKM- | 59 | OPBINM |
| 29 | OLRFPM+ | 60 | IDREN |
| 30 | OLRFPM- | 61 | IPBRTMN+ |
| 31 | OLFPM+ | 62 | IPBRTMN- |

# NTEX30AA

## Product description

The NTEX30AA T1 analog paddle board (T1PB) provides interface. This printed circuit pack (PCP) is in the frame relay interface unit (FRIU). The NTEX30AA T1PB provides the interface between the NTEX31AA frame relay access processor (FRAP) and the T1 transmission medium. The NTEX31BA-based FRIUs also use the T1PB.

The FRIU handles a single T1 circuit. The FRIU supports the following configurations:

- 24 channels of channelized data access. Each channel operates at 56 Kbps or 64 Kbps
- one channel of unchannelized data access. This channel supports frame transfers from 1.344 Mbps to 1.536 Mbps
- a maximum of four channels. Each channel operates at 384 Kbps, in NTEX31BA-based FRIUs.

Applications from BCS33 or earlier use the NTEX22AA card. All applications that require more than 4Mbytes of Dynamic Random Access chip (DRAM) use the NTEX22BB card in BCS34.

In BCS33 or earlier applications, the FRIU contains the following circuit packs:

- NTEX22AA integrated processor/frame transport bus (F-bus) interface (IPF) card
- NTEX30AA analog paddle board (T1PB)
- NTEX31AA frame relay access processor (FRAP) card.

In BCS34 applications, the FRIU contains the following circuit packs:

- NTEX22BB integrated processor/F-bus interface (IPF) card
- NTEX30AA analog paddle board (T1PB)
- NTEX31AA frame relay access processor (FRAP) card.

The NTEX22AA provides access to the local message switch (LMS) over the F-bus. The NTEX22AA also acts as the processing machine for the FRIU. The processing machine uses the 68030 microcomputer subsystem (MCS).

The NTEX22BB is like the ntex22AA except for the following differences:

- the BB card supports 32-bit asynchronous P-bus slaves
- spare peripherals
- has 8 Mbytes of DRAM.

The AA card has only 4 Mbytes of DRAM.

The NTEX30AA provides the interface to the T1 line.

The NTEX31AA provides high-level data link control (HDLC) framing, T1 formatting and alarm detection and generation.

The NTEX30AA has the following functions:

- generates balanced bipolar alternate mark inversion (AMI) data from unipolar signals
- extracts unipolar signals from incoming bipolar data
- recovers, extracts, detects, and generates clock signals
- generates the loss of signal and alarm indicator signal (blue alarm) alarm signals
- equalizes the T1 signal for all supported line lengths (to 200 m or 660 ft)
- detects incoming blue alarm
- monitors the level of jitter or clock slip, with provisions for limited jitter buffering
- stores paddle board identification and card vintage information
- protects paddle board devices from surges on power-up
- controls and filters the electromagnetic interference (EMI)
- provides overvoltage transient suppression of the T1 line.

The NTEX30AA does not support the Conference of European Postal and Telecommunications (CEPT) Administrations PCM30 mode. The T1 line interface function uses a Rockwell R8069 line interface unit.

The NTEX30AA is backward compatible with the NTEX31AA and NTEX31BA hardware.

## Location

The NTEX30AA is in the lower three shelves of a 36 slot LPP.

## **NTEX30AA** (continued)

# Functional description

The NTEX30AA T1PB provides an interface between the NTEX31AA FRAP and the medium for T1 transmission.

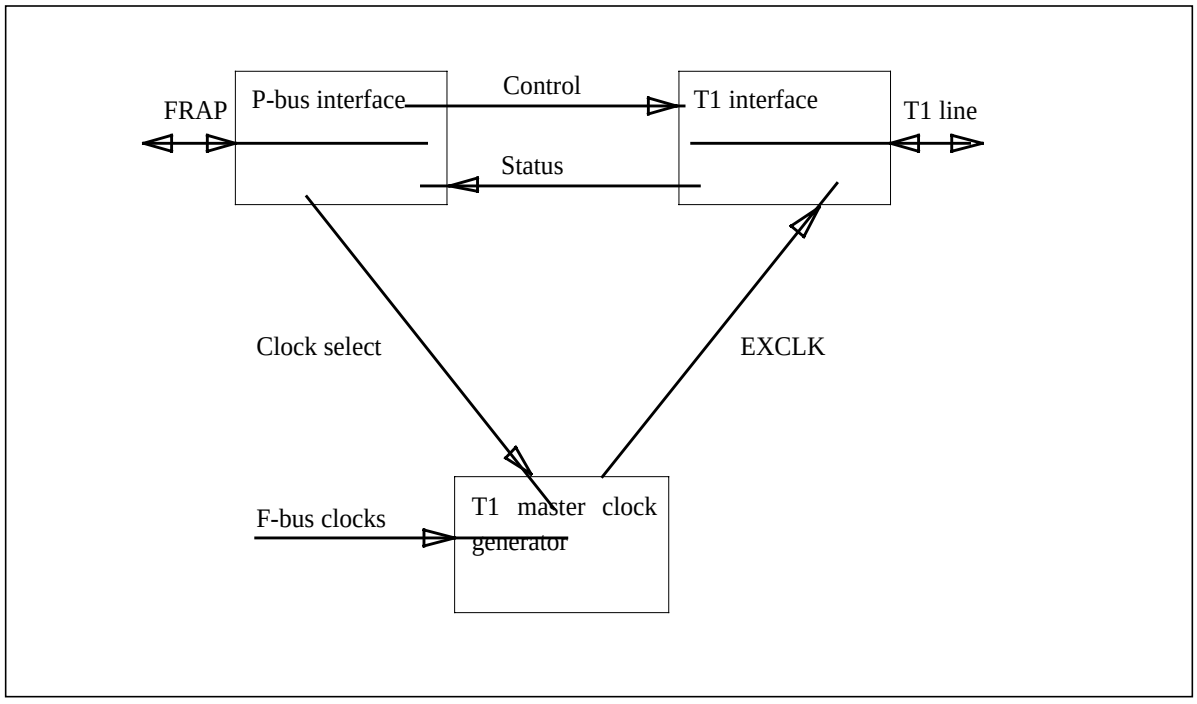
### Functional blocks

The NTEX30AA has the following functional blocks:

- P-bus interface
- T1 interface
- T1 master clock generator

The following figure indicates the relationship between the functional blocks.

**NTEX30AA functional blocks**




### P-bus interface

The IPF interface circuit connects the NTEX30AA to the link general processor (LGP) through the FRAP. The IPF interface controls the T1 physical interface (the operating mode and line length equalization). The IPF interface monitors the state and control circuits of the T1 interface.

The IPF interface provides PCP identification and vintage information. With the application of power the system resets the card.

### T1 interface

The T1 interface allows access to the T1 carrier, and supports the transmission and reception of data on the link. The interface contains an R8069 line interface unit and support circuits.

The support circuits perform the following functions:

- filters the EMI of outgoing and incoming data
- protects the transmit and receive circuits from overvoltage transients
- controls the R8069 mode under a number of link conditions
- decodes the R8069 status outputs.

### T1 master clock generator

The T1 master clock generator circuit generates the 1.544 MHz T1 clock from the 4.096 MHz F-bus clocks. This action creates a clock that synchronizes the DMS SuperNode stratum 2 clock. The system uses this clock when the FRIU is the clock source for the T1 carrier. Support circuits detect and buffer the clocks.

The T1 master clock generator performs the following functions:

- buffers the F-bus clock
- selects the F-bus clock, either clock A or B
- detects the F-bus clock A and B
- translates frequency from 4.096 MHz to 1.544 MHz
- filters and translates the T1 clock
- detects the T1 clock

## Signaling

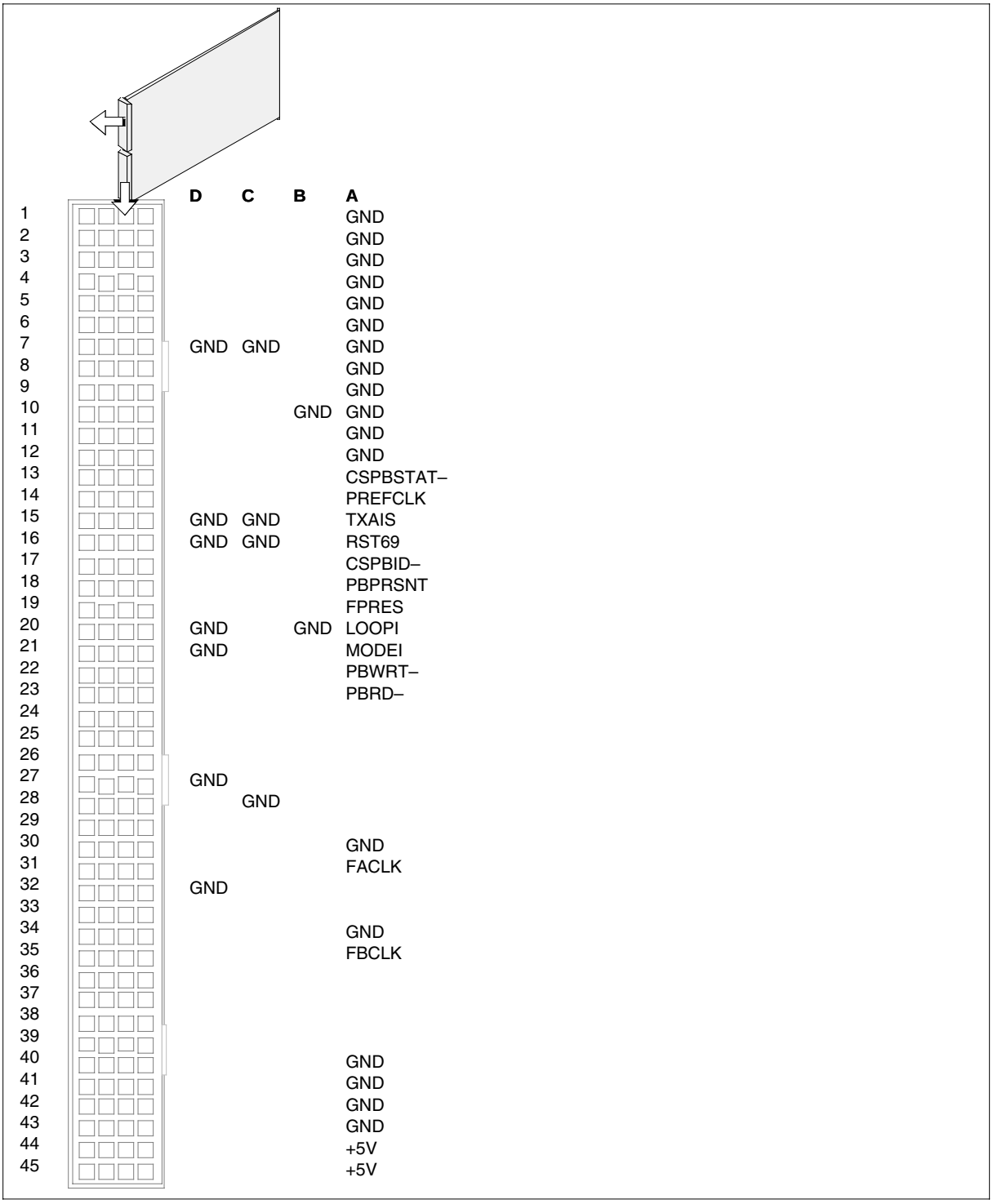
The NTEX30AA has three connectors. One connector connects the NTEX30AA to the link interface unit (LIU) backplane. The other two connectors connect the NTEX30AA with the T1 line.

### Pin numbers

The pin numbers for the NTEX30AA appear in the following figures.

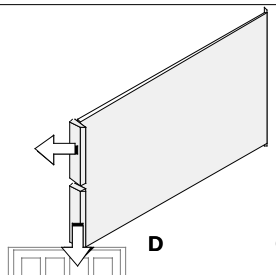
# **NTEX30AA** (continued)

### NTEX30AA pin numbers (Part 1 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | GND |
| 2 | | | | GND |
| 3 | | | | GND |
| 4 | | | | GND |
| 5 | | | | GND |
| 6 | | | | GND |
| 7 | GND | GND | | GND |
| 8 | | | | GND |
| 9 | | | | GND |
| 10 | | | GND | GND |
| 11 | | | | GND |
| 12 | | | | GND |
| 13 | | | | CSPBSTAT– |
| 14 | | | | PREFCLK |
| 15 | GND | GND | | TXAIS |
| 16 | GND | GND | | RST69 |
| 17 | | | | CSPBID– |
| 18 | | | | PBPRSNT |
| 19 | | | | FPRES |
| 20 | GND | | GND | LOOPI |
| 21 | GND | | | MODEI |
| 22 | | | | PBWRT– |
| 23 | | | | PBRD– |
| 24 | | | | |
| 25 | | | | |
| 26 | | | | |
| 27 | GND | | | |
| 28 | | GND | | |
| 29 | | | | |
| 30 | | | | GND |
| 31 | | | | FACLK |
| 32 | GND | | | |
| 33 | | | | |
| 34 | | | | GND |
| 35 | | | | FBCLK |
| 36 | | | | |
| 37 | | | | |
| 38 | | | | |
| 39 | | | | |
| 40 | | | | GND |
| 41 | | | | GND |
| 42 | | | | GND |
| 43 | | | | GND |
| 44 | | | | +5V |
| 45 | | | | +5V |

**NTEX30AA pin numbers (Part 2 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 46 | | | | +5V |
| 47 | | | GND | +5V |
| 48 | | | | +5V |
| 49 | | | | +5V |
| 50 | | | GND | +5V |
| 51 | | | | +5V |
| 52 | | | | +5V |
| 53 | | | GND | +5V |
| 54 | | | | +5V |
| 55 | | | | +5V |
| 56 | | | GND | |
| 57 | | | | |
| 58 | | | | |
| 59 | | | | |
| 60 | | | | |
| 61 | | | | |
| 62 | | | | |
| 63 | | | | |
| 64 | | | | |
| 65 | | | | |
| 66 | GND | | | |
| 67 | | | | |
| 68 | | | | |
| 69 | | GND | | |
| 70 | | | | |
| 71 | PBDAT0 | | | |
| 72 | PBDAT1 | | | |
| 73 | PBDAT2 | | | |
| 74 | PBDAT3 | | | |
| 75 | PBDAT4 | CTRCLK | | |
| 76 | PBDAT5 | PBADDR2 | | |
| 77 | PBDAT6 | PBADDR3 | | |
| 78 | PBDAT7 | PBADDR4 | | |
| 79 | PBDAT8 | PBADDR5 | GND | GND |
| 80 | PBDAT9 | GND | RPOS | GND |
| 81 | PBDAT10 | GND | RNEG | GND |
| 82 | PBDAT11 | PERR | GND | GND |
| 83 | PBDAT24 | GND | TPOS | GND |
| 84 | PBDAT25 | GND | TNEG | GND |
| 85 | PBDAT26 | LS | GND | GND |
| 86 | PBDAT27 | CTRTST | RCLK | GND |
| 87 | PBDAT28 | AIS | GND | GND |
| 88 | PBDAT29 | GND | TCLK | GND |
| 89 | PBDAT30 | MRST– | GND | GND |
| 90 | PBDAT31 | GND | SCLK | GND |

## **NTEX30AA** (end)

# Technical data

### Description

The NTEX30AA is a multi-layer card with two power layers, four routing layers, and two cap layers. Both cap layers only contain pads.

### Technology

The NTEX30AA card is a mixed technology board. The NTEX30AA uses through-hole technology for all integrated circuits, and surface-mount technology (SMT) for all passives. Exceptions to these types are:

- the fuse
- the radio frequency (RF) choke at the power input
- the transformers on the card

### Power requirements

The NTEX30AA uses a single 5V power supply that has the same specifications as a link peripheral processor paddle board.

The power requirements of the NTEX30AA appear in the following table.

**Power requirements of the NTEX30AA**

| | Normal | Maximum | Units |
|---|---|---|---|
| Current | 0.786 | 1.434 | amperes |
| Power | 3.93 | 7.17 | watts |

# NTEX31AA

## Product description

The NTEX31AA frame relay access processor (FRAP) circuit pack provides interface to the T1 trunk. This printed circuit pack (PCP) is in the frame relay interface unit (FRIU).

The FRIU handles a single T1 circuit. The FRIU supports the following configurations:

- 24 channels of channelized data access. Each channel operates at 56 Kbps or 64 Kbps
- 1 channel of unchannelized data access. This channel supports frame transfers from 1.344 Mbps to 1.536 Mbps.

Applications from BCS33 or earlier, use the NTEX22AA card. All applications that require more than 4Mbytes of Dynamic Random Access Memory chip (DRAM) use the NTEX22BB card in BCS34.

In the BCS33 or earlier applications, the FRIU contains the following circuit packs:

- NTEX22AA integrated processor/frame transport bus (F-bus) interface (IPF) card
- NTEX30AA analog paddle board (T1PB)
- NTEX31AA frame relay access processor (FRAP) card.

In BCS34 applications, the FRIU contains the following circuit packs:

- NTEX22BB integrated processor/F-bus interface (IPF) card
- NTEX30AA analog paddle board (T1PB)
- NTEX31AA frame relay access processor (FRAP) card.

The NTEX22AA provides access to the local message switch (LMS) over the F-bus. The NTEX22AA also acts as the processing machine for the FRIU. The processing machine uses the 68030 microcomputer subsystem (MCS).

The NTEX22BB is like the ntex22AA except in the following differences:

- the BB card supports 32-bit asynchronous P-bus slaves
- spare peripherals
- has 8 Mbytes of DRAM

The AA card has only 4 Mbytes of DRAM.

## **NTEX31AA** (continued)

The NTEX30AA provides the interface to the T1 line.

The NTEX31AA provides high-level data link control (HDLC) framing and T1 formatting, alarm detection and generation.

The NTEX31AA has the following features:

- frame synchronization
- loss of frame detection
- detection and transmission of an alarm indication signal (AIS) that indicates the loss of signal. The other system is not available.
- detection and transmission of a yellow alarm. This alarm indicates a frame synchronization problem. The other system is not available for service.
- T1 loopback for local and remote diagnostic purposes
- transmission and control of A- and B-bit signaling, from one channel to another channel
- reception of A- and B-bit signaling
- support of alternate mark inversion (AMI) and B8ZS line coding
- master/slave synchronization of the T1 clock source. This feature eliminates frame slips.
- support of the D4 (SF) framing format
- jitter (clock slip) performance conforming to BNR, CCITT, and AT standards
- conform to DSX-1 pulse shape templates. The CCITT determines the standards to which the templates must conform.
- insert and extract the HDLC flags
- calculate and validate frame cyclic redundancy check (CRC)
- manipulate hardware for the receive and transmit buffers
- interrupt notification of frame buffer event completion.

### Location

In a link peripheral processor (LPP), an application specific unit (ASU) occupies two or three slots. The position of the slot depends on the version of the LPP. The FRIU hardware operates in both versions of the LPP. The FRIU hardware is the FRAP and the T1PB.

## Functional description

The main functions of the NTEX31AA are the T1 interface function and the processing of the HDLC frames of data. Data includes incoming and outgoing information.

The FRAP provides frame relay service (FRS) functionality to the LPP. These functions includes access through a standard T1 trunk. The trunk supports 1.344 Mbps and 1.536 Mbps unchannelized data or 24 channel data access at 56 Kbps and 64 Kbps.

The data, channelized or unchannelized, contains HDLC frames. The FRAP processes the HDLC frames. The FRAP hardware supports only the D4 framing format (Ft framing).

### Functional blocks

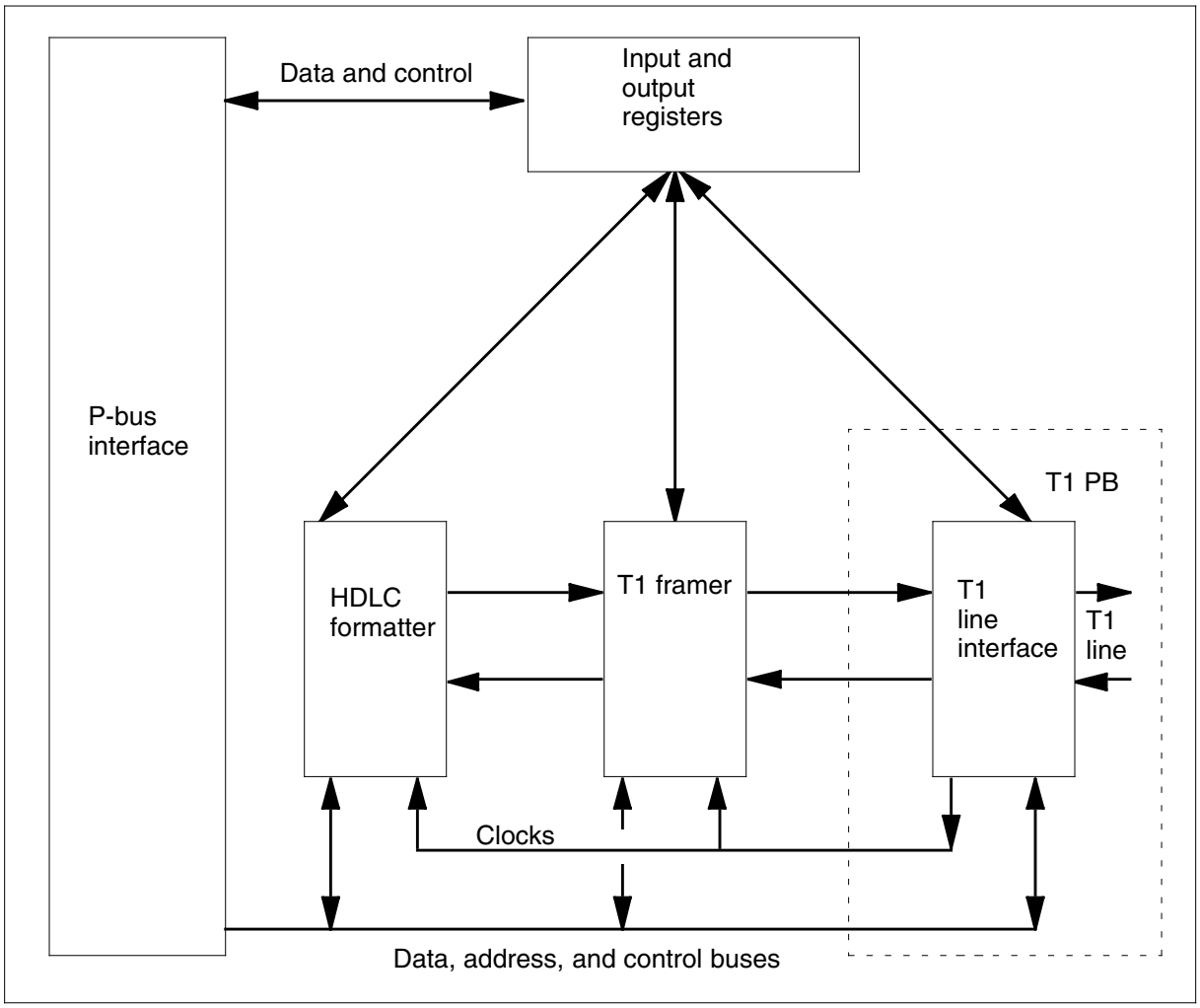
The NTEX31AA has the following functional blocks:

- integrated processor frame bus interface
- HDLC formatter
- T1 framer
- input and output registers

The following figure indicates the relationship between the functional blocks.

## **NTEX31AA** (continued)

**NTEX31AA functional blocks**




### Integrated processor frame bus interface

The IPF interface circuit connects the FRAP and the T1PB to the IPF. The IPF interface circuit has the following functions:

- buffers the bus
- generates address decoding for the FRAP
- generates data transfer acknowledge signals to the IPF
- provides parity protection on P-bus data transfers
- handles all interrupt functions for the FRAP.

### High-level data link control formatter

The HDLC formatter circuit contains the Rockwell R8071 ISDN/digital multiplex interface (DMI) link layer controller. The HDLC formatter circuit also contains the supportcircuits required to provide the HDLC formatting function for frame relay service.

The support circuits perform the following functions:

- accelerates the R8071 bus cycle to reduce the number of IPF delays. Access problems can cause a delay.
- provides access control and byte steering to allow the IPF accesses to the shared RAM to be 8 or 16 bits wide. The R8071 accesses are 8 bits wide.
- buffers the IPF from R8071 interrupts. The system generates these interrupts when the system returns used buffers to the buffer queue.

### T1 framer

The T1 framer circuit contains the Rockwell R8070 T1/Conference of European Postal and Telecommunications (CEPT) pulse code modulation (PCM) transceiver. The T1 framer supports the circuits required to provide the signaling and alarm functions on the T1 link.

The support circuits perform the following functions:

- monitors and reports alarm and error conditions of the incoming T1 line
- receives signaling on the A and B bits
- transmits A and B signaling bits
- controls outgoing signaling bits in each channel. This function allows 64 Kbps clear channel applications and 56 Kbps signaling applications to share the same carrier.

### Input and output registers

The input and output registers perform the following functions:

- configure the operation mode of the FRAP
- monitor the operation of the FRAP
- control the operation of the FRAP to meet different link conditions
- handle read and write operations. This function provides the best diagnostic information for the circuit pack.

## **NTEX31AA** (continued)

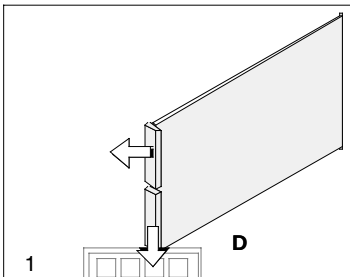
## Signaling

The NTEX31AA has a single connector that joins the NTEX31AA to the link interface unit (LIU) backplane. The FRAP gains access to the T1 link through the NTEX30AA paddle board that connects the FRAP to the LIU backplane.

### Pin numbers

The pin numbers for the NTEX31AA appears in the following figures.

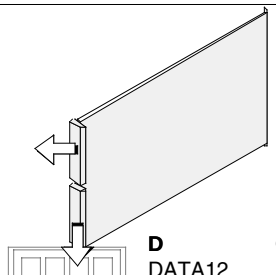
**NTEX31AA pin numbers (Part 1 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | GND |
| 2 | | | | GND |
| 3 | | | | GND |
| 4 | | | | GND |
| 5 | | | | GND |
| 6 | | | | GND |
| 7 | GND | GND | | GND |
| 8 | | | | GND |
| 9 | | | | GND |
| 10 | | | GND | GND |
| 11 | | | | GND |
| 12 | | | | GND |
| 13 | | | | CSPBSTAT– |
| 14 | | | | PREFCLK |
| 15 | GND | GND | | AIS |
| 16 | GND | GND | | RST69 |
| 17 | | BGRANT– | | CSPBID– |
| 18 | | BGRANT– | | PBPRSNT– |
| 19 | | PERINT2– | | FPRES– |
| 20 | GND | | GND | LOOPI |
| 21 | GND | | | MODEI |
| 22 | | | | PBWRT– |
| 23 | RSTOUT– | | | PBRD– |
| 24 | PERINT1– | | | |
| 25 | BEN1– | BEN0– | | |
| 26 | BEN3– | BEN2– | | |
| 27 | GND | | | |
| 28 | WRT– | GND | | |
| 29 | EDTACK– | DTACK– | | HW4 |
| 30 | PARITY– | | | GND |
| 31 | PAREN– | | | |
| 32 | | GND | | SH0 |
| 33 | DAS32– | | | SH1 |
| 34 | DATA0 | | | GND |
| 35 | DATA1 | | | |
| 36 | DATA2 | ADDR01 | HW0 | |
| 37 | DATA3 | ADDR03 | HW1 | |
| 38 | DATA4 | ADDR04 | HW2 | |
| 39 | DATA6 | ADDR05 | HW3 | |
| 40 | DATA6 | ADDR06 | | GND |
| 41 | DATA7 | ADDR07 | | GND |
| 42 | DATA8 | ADDR08 | | GND |
| 43 | DATA9 | ADDR09 | | GND |
| 44 | DATA10 | ADDR10 | | +5V |
| 45 | DATA11 | ADDR11 | LVL4INT– | +5V |

# **NTEX31AA** (continued)

### NTEX31AA pin numbers (Part 2 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 46 | DATA12 | ADDR12 | | +5V |
| 47 | DATA13 | ADDR13 | GND | +5V |
| 48 | DATA14 | ADDR14 | | +5V |
| 49 | DATA15 | ADDR15 | | +5V |
| 50 | DATA16 | ADDR16 | GND | +5V |
| 51 | DATA17 | ADDR17 | | +5V |
| 52 | DATA18 | ADDR18 | | +5V |
| 53 | DATA19 | ADDR19 | GND | +5V |
| 54 | DATA20 | ADDR20 | | +5V |
| 55 | DATA21 | ADDR21 | | +5V |
| 56 | DATA22 | ADDR22 | GND | |
| 57 | DATA23 | ADDR23 | | |
| 58 | DATA24 | ADDR24 | | |
| 59 | DATA25 | ADDR25 | | |
| 60 | DATA26 | ADDR26 | | |
| 61 | DATA27 | ADDR27 | | |
| 62 | DATA28 | ADDR28 | | |
| 63 | DATA29 | ADDR29 | | |
| 64 | DATA30 | ADDR30 | | |
| 65 | DATA31 | ADDR31 | | |
| 66 | GND | | | |
| 67 | | | | |
| 68 | | | | |
| 69 | | GND | | |
| 70 | | | | |
| 71 | PBD00 | | | |
| 72 | PBD01 | | | |
| 73 | PBD02 | | | |
| 74 | PBD03 | | | |
| 75 | PBD04 | CTRCLK | | |
| 76 | PBD05 | PBA2 | | |
| 77 | PBD06 | PBA3 | | |
| 78 | PBD07 | PBA4 | | |
| 79 | PBD08 | PBA5 | GND | GND |
| 80 | PBD09 | GND | RPOS | GND |
| 81 | PBD10 | GND | RNEG | GND |
| 82 | PBD11 | PERR– | GND | GND |
| 83 | PBD24 | GND | TPOS | GND |
| 84 | PBD25 | GND | TNEG | GND |
| 85 | PBD26 | LS | GND | GND |
| 86 | PBD27 | CTRTST | RCLK | GND |
| 87 | PBD28 | AIS | GND | GND |
| 88 | PBD29 | GND | TCLK | GND |
| 89 | PBD30 | MRST– | GND | GND |
| 90 | PBD31 | GND | SCLK | GND |

# Technical data

## Description

The NTEX31AA is a multi-layer card with two power layers, four routing layers, and two cap layers. The two cap layers contain copper balance pads.

## Technology

The NTEX31AA does not use surface-mount devices. The Rockwell Quad in-line package (QUIP) contains the R8070 and the R8071.

## Power requirements

The NTEX31AA uses a single 5V power supply with the same specifications as the power supply on other LPP paddle boards.

The power requirements for the NTEX31AA appear in the following table.

**Power requirements of the NTEX31AA**

| | Normal | Maximum | Units |
|---|---|---|---|
| Current | 4.228 | 7.042 | amperes |
| Power | 21.14 | 35.21 | watts |

# NTEX31BA

## Description

The NTEX31BA enhanced frame relay access processor (EFRAP) circuit pack is a part of the frame relay interface unit (FRIU). The EFRAP provides an interface to the T1 trunk that the frame relay service requires.

### Location

The NTEX31BA circuit pack is in shelves 2, 3, and 4 of the link peripheral processor (LPP). The pack fills in the odd-numbered slots from 9F through 31F.

## Functional description

The main functions of the EFRAP are T1 framing and synchronization, and processing high-level data link control (HDLC) frames.

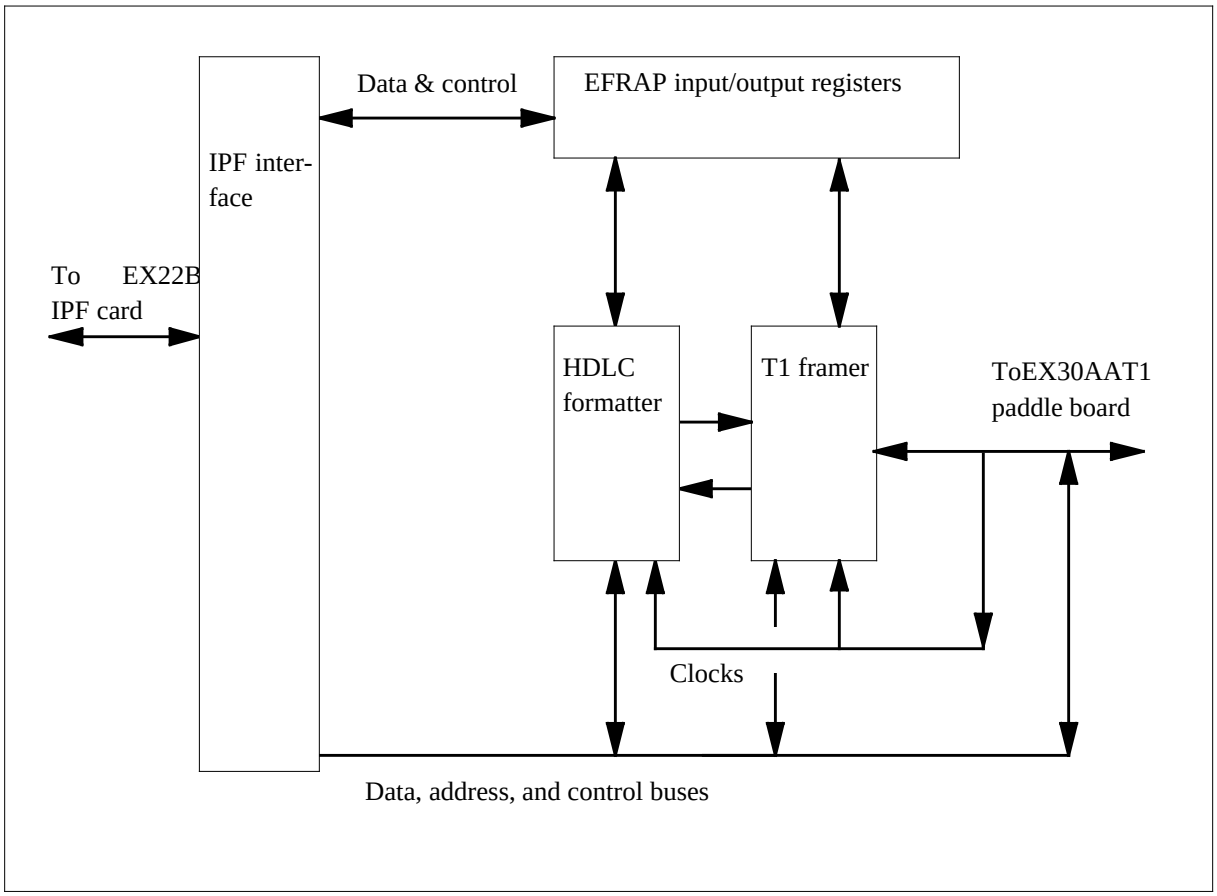
### Functional blocks

The NTEX31BA has the following functional blocks:

- integrated processor frame-transport bus (F-bus) interface (IPF interface)
- EFRAP input/output registers
- HDLC formatter
- T1 framer.

The following figure indicates the relationship between the functional blocks.

**NTEX31BA functional blocks**




## Integrated processor F-bus interface

The IPF interface circuit connects the EFRAP and the T1 paddle board to the IPF. The IPF interface circuit performs the following functions:

- acts as a buffer for the F-bus
- performs address decoding for the EFRAP
- generates data transfer acknowledge signals to the IPF
- provides parity protection on processor-bus (P-bus) transfers
- performs all interrupt functions for the EFRAP.

## EFRAP input/output registers

The EFRAP input/output registers configure the operating mode of the EFRAP. A register can monitor and control the operation of the EFRAP to meet different link conditions.

## **NTEX31BA** (continued)

### HDLC formatter

The HDLC formatter contains the R8071 ISDN link layer controller and frame relay service circuits.

The HDLC formatter performs the following functions:

- accelerates the HDLC controller bus cycle
- provides access control to the shared RAM
- provides byte steering to the shared RAM
- buffers the IPF from the HDLC controller interrupt signals.

### T1 framer

The T1 framer contains the signaling and alarm circuits, and the T1/CEPT pulse code modulation (PCM) transceiver. The Conference of European Postal and Telecommunications administrations (CEPT) defines the CEPT format. The North American standards bodies define the T1 framer. The Institute of Electrical and Electronic Engineers (IEEE) and the American National Standards Institute (ANSI), are members of this group.

The T1 framer supports IEEE and ANSI. The EX31BA hardware only supports the North American T1 versions.

The T1 framer performs the following functions:

- adds and subtracts the T1 framing information to and from the T1 trunk
- monitors alarm and error conditions
- receives and transmits A and B signaling bits in D4 and extended superframe format (ESF) modes
- controls outgoing signaling bits for each channel. This control applies to the D4 and ESF modes on A and B bits only. The C and D bits in ESF mode are not supported.
- transmits line loopback ON and OFF sequences in modes D4 and ESF
- supports transmission of priority code word messages that use the facility data link (FDL) of ESF protocol

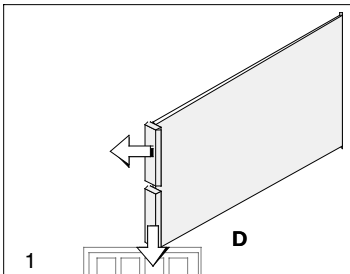
## Signaling

A single connector joins EFRAP to the LIU backplane. Access the T1 link through a paddle board, which connects to EFRAP over the LIU backplane.

### Pin numbers

The pin numbers for the NTEX31BA appear in the following figures.

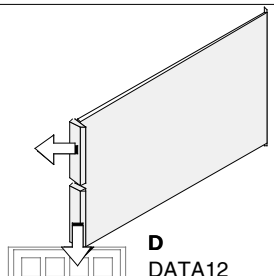
**NTEX31BA pin numbers (Part 1 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | GND |
| 2 | | | | GND |
| 3 | | | | GND |
| 4 | | | | GND |
| 5 | | | | GND |
| 6 | | | | GND |
| 7 | GND | GND | | GND |
| 8 | | | | GND |
| 9 | | | | GND |
| 10 | | | GND | GND |
| 11 | | | | GND |
| 12 | | | | GND |
| 13 | | | | CSPBSTAT– |
| 14 | | | | PREFCLK |
| 15 | GND | GND | | TXAIS |
| 16 | GND | GND | | RST69 |
| 17 | | BGRANT– | | CSPBID– |
| 18 | | BGRANT– | | PBPRSNT– |
| 19 | | PERINT2– | | FPRES– |
| 20 | GND | | GND | LOOPI |
| 21 | GND | | | MODEI |
| 22 | | | | PBWRT– |
| 23 | RSTOUT– | | | PBRD– |
| 24 | PERINT1– | | | |
| 25 | BEN1– | BEN0– | | |
| 26 | BEN3– | BEN2– | | |
| 27 | GND | | | |
| 28 | WRT– | GND | | |
| 29 | EDTACK– | DTACK– | | HW4 |
| 30 | PARITY– | | | GND |
| 31 | PAREN– | | | |
| 32 | | GND | | SH0 |
| 33 | DAS32– | | | SH1 |
| 34 | DATA00 | | | GND |
| 35 | DATA01 | | | |
| 36 | DATA02 | ADDR02 | HW0 | |
| 37 | DATA03 | ADDR03 | HW1 | |
| 38 | DATA04 | ADDR04 | HW2 | |
| 39 | DATA05 | ADDR05 | HW3 | |
| 40 | DATA06 | ADDR06 | | GND |
| 41 | DATA07 | ADDR07 | | GND |
| 42 | DATA08 | ADDR08 | | GND |
| 43 | DATA09 | ADDR09 | | GND |
| 44 | DATA10 | ADDR10 | | +5V |
| 45 | DATA11 | ADDR11 | LVL4INT– | +5V |

# **NTEX31BA** (continued)

### NTEX31BA pin numbers



| | D | C | B | A |
|---|---|---|---|---|
| 46 | DATA12 | ADDR12 | | +5V |
| 47 | DATA13 | ADDR13 | GND | +5V |
| 48 | DATA14 | ADDR14 | | +5V |
| 49 | DATA15 | ADDR15 | | +5V |
| 50 | DATA16 | ADDR16 | GND | +5V |
| 51 | DATA17 | ADDR17 | | +5V |
| 52 | DATA18 | ADDR18 | | +5V |
| 53 | DATA19 | ADDR19 | GND | +5V |
| 54 | DATA20 | ADDR20 | | +5V |
| 55 | DATA21 | ADDR21 | | +5V |
| 56 | DATA22 | ADDR22 | GND | |
| 57 | DATA23 | ADDR23 | | |
| 58 | DATA24 | ADDR24 | | |
| 59 | DATA25 | ADDR25 | | |
| 60 | DATA26 | ADDR26 | | |
| 61 | DATA27 | ADDR27 | | |
| 62 | DATA28 | ADDR28 | | |
| 63 | DATA29 | ADDR29 | | |
| 64 | DATA30 | ADDR30 | | |
| 65 | DATA31 | ADDR31 | | |
| 66 | GND | | | |
| 67 | | | | |
| 68 | | | | |
| 69 | | GND | | |
| 70 | | | | |
| 71 | PBD00 | | | |
| 72 | PBD01 | | | |
| 73 | PBD02 | | | |
| 74 | PBD03 | | | |
| 75 | PBD04 | CTRCLK | | |
| 76 | PBD05 | PBA2 | | |
| 77 | PBD06 | PBA3 | | |
| 78 | PBD07 | PBA4 | | |
| 79 | PBD08 | PBA5 | GND | |
| 80 | PBD09 | GND | RPOS | GND |
| 81 | PBD10 | GND | RNEG | GND |
| 82 | PBD11 | PERR– | GND | GND |
| 83 | PBD24 | GND | TPOS | GND |
| 84 | PBD25 | GND | TNEG | GND |
| 85 | PBD26 | LS | GND | GND |
| 86 | PBD27 | CTRTST | RCLK | GND |
| 87 | PBD28 | AIS | GND | GND |
| 88 | PBD29 | GND | TCLK | GND |
| 89 | PBD30 | MRST– | GND | GND |
| 90 | PBD31 | GND | SCLK | GND |

## Technical data

### Power requirements

The maximum power available for the EFRAP is 40 W. The EFRAP operates from a single 5V power supply.

# NTEX54AA

## Product description

The NTEX54AA data bus interface card (DBIC) is used in the 1 Meg Modem Service (1MMS) asymmetric digital subscriber loop (ADSL) access system to provide the interface between an Ethernet LAN (10Base-T) and multiple xDSL line cards (xLC, NTEX17AA or NTEX17BA) for high-speed data access. The DBIC also provides all the circuitry associated with the voice-only BIC (NT6X54AA) to allow continued POTS service. These interfaces are between 64 line cards in the line drawer and one 32-channel digroup to each line concentrating array (shelf).

### Location

The NTEX54AA is in the drawer of a line concentrating module (LCM). Each line drawer has one DBIC and a maximum of 64 line cards of different types. Each scan chip links one digroup with 32 line cards. If one digroup (scan chip) fails, the digroup that remains takes over all 64 lines.

## Functional description

The DBIC consists of two separate circuits. The first circuit consists of the components required to provide a voicepath between two digroup controllers and the line cards. The second circuit consists of the components required to provide an interface between a 10Base-T port and the xDSL line cards. The common point between these two circuits is the XLBUS (eXtended LBUS). This is a point-to-point bus which communicates with the line cards.

Two X24 Scan ASICs form the heart of the BIC. These X24s interface two 32-channel digroup controllers with the 64 line cards for voice traffic. The controllers provide unidirectional serial lines (RCON and TCON) to exchange control and for status information. The controllers provide unidirectional serial lines (RD and RT) to carry user voice data, a frame pulse (FP), and a 5.12 MHz clock (CLK). An additional line (ACT) indicates that a particular controller is active. Thus one controller manages both X24s when the other controller fails or is being upgraded.

The NTEX54AA performs the following functions:

- multiplexes and demultiplexes a 32-channel link on 32 line card buses
- receives control messages to line cards asynchronously. Stores these messages until the messages are output to line cards during channels 0 or 16
- stores responses to control messages

- scans 32 line cards for changes in supervision bits. The NTEX54AA stores a message when the card detects a change in state.
- writes new information to the ring multiplexer

The scan chip demultiplexes each 32-channel serial (RD) link on 32 line card buses. The scan chip multiplexes the line card responses on the outgoing (TD) serial links. The multiplex uses a 32-byte connection memory in each scan chip. Each scan chip is accessed in sequence each channel time. One location of the connection memory corresponds to a specified channel time. The address of the line card accessed at that time is in this location. To assign line card numbers to channel times, the system writes to the connection memory with a message written to the chip on RCON. The message has the channel number and the line card address.

Control messages to line cards are written asynchronously following the channel times on the RCON. First, an input first-in-first-out (FIFO) base stores these messages on the scan chip. The messages remain on the scan chip until channel time 0 to 16. Second, the control message is output to the line card. If requested, an output FIFO stores the line card response on the chip. If the input FIFO does not contain control messages, channels 0 and 16 scan line cards. To scan line cards, send an output and idle code to the E99 integrated circuit (IC) on the addressed line card. Compare the state of the supervision bits (SV1, SV0) with the earlier two states of those bits from earlier scans. If two consecutive scans detect a change, the system loads the address and response of the line card into the output FIFO. The system scans all 32 cards every 4 ms if the system does not send control messages during that time. When the system sends a control message, the scan is on hold for one frame. When the LCM controller outputs the appropriate code on the RCON, the controller can read these scan messages. The controller responses to control messages. This action results in a response on the TCON that consists of one word from the output FIFO. All transactions on RCON and TCON are 20 bits long. The bits contain address (or op-code) and data.

The BIC holds the TCON low to alert the controller that the output FIFO contains a minimum of one word. When the FIFO is empty, the TCON remains high.

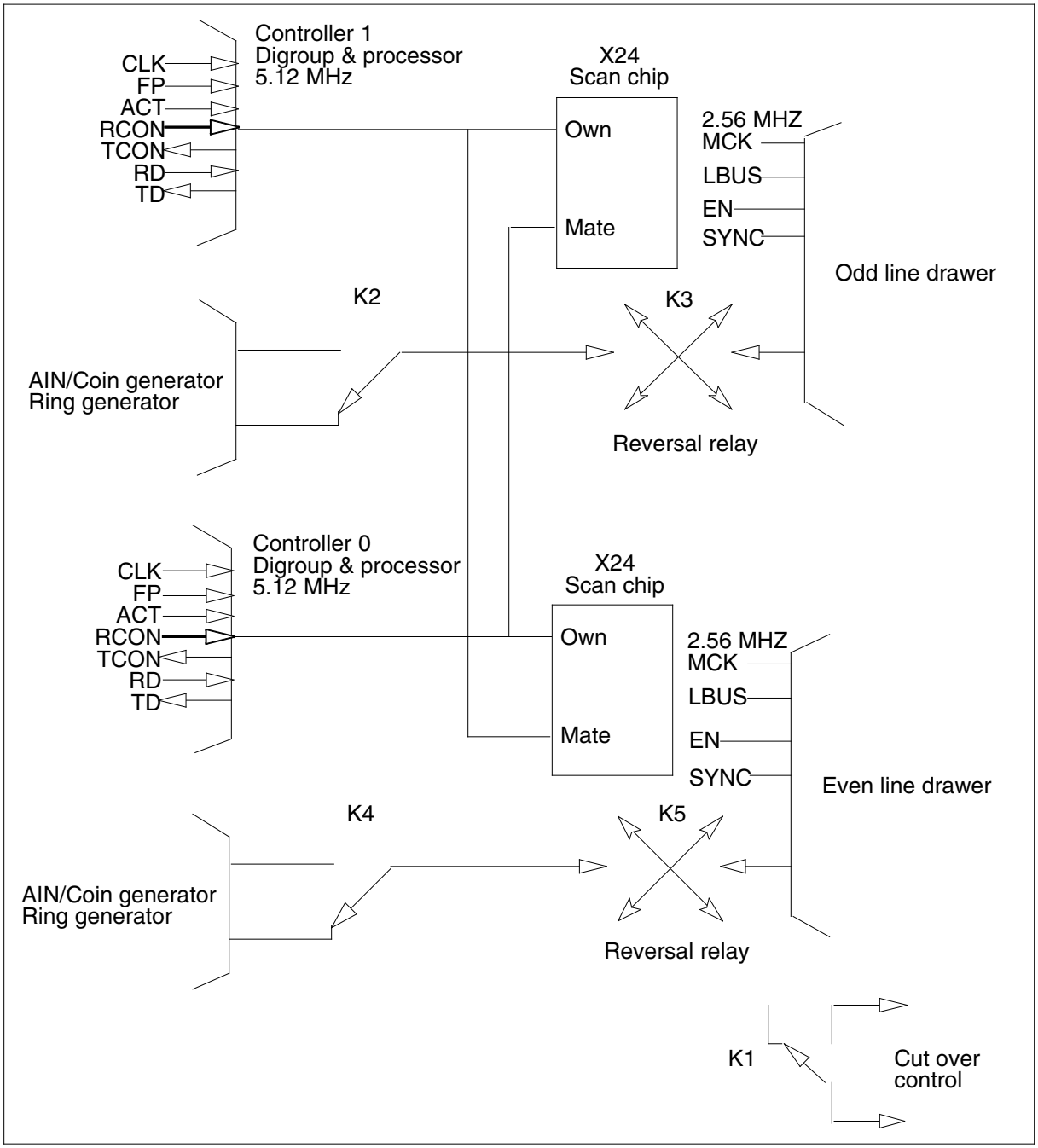
The NTEX54AA provides a +12.7V reference to all 64 line positions.

### Functional blocks

The relationship between the functional blocks appears in the following figure.

## **NTEX54AA** (continued)

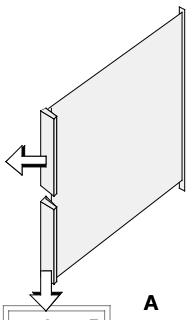
**NTEX54AA functional blocks**




### Pin numbers

The pin numbers for the NTEX54AA appear in the following figure.

### NTEX54AA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | REFGND | REFGND |
| 4A 4B | BUS62 | BUS63 |
| 5A 5B | BUS61 | BUS62 |
| 6A 6B | BUS58 | BUS59 |
| 7A 7B | BUS56 | BUS57 |
| 8A 8B | BUS54 | BUS55 |
| 9A 9B | BUS52 | BUS53 |
| 10A 10B | BUS50 | BUS51 |
| 11A 11B | BUS48 | BUS49 |
| 12A 12B | SYNCD | END |
| 13A 13B | VREF | MCLKD |
| 14A 14B | CUTO | GND |
| 15A 15B | RGBUS1T | RGBUS1R |
| 16A 16B | GND | GND |
| 17A 17B | +15V | +15V |
| 18A 18B | BUS46 | BUS47 |
| 19A 19B | BUS44 | BUS45 |
| 20A 20B | BUS42 | BUS43 |
| 21A 21B | BUS40 | BUS41 |
| 22A 22B | BUS38 | BUS39 |
| 23A 23B | BUS36 | BUS37 |
| 24A 24B | BUS34 | BUS35 |
| 25A 25B | BUS32 | BUS33 |
| 26A 26B | GND | GND |
| 27A 27B | SYNCC | ENC |
| 28A 28B | VREF | MCLKC |
| 29A 29B | CUTO | RGND |
| 30A 30B | CLK1+ | CLK1– |
| 31A 31B | FP1+ | FP1– |
| 32A 32B | RD1 | GND |
| 33A 33B | TD1+ | GND |
| 34A 34B | RCON1 | GND |
| 35A 35B | TCON1 | GND |
| 36A 36B | ACT1 | GND |
| 37A 37B | ACT0 | GND |
| 38A 38B | RCON0+ | GND |
| 39A 39B | TCON0 | GND |
| 40A 40B | TD0+ | GND |

| | A | B |
|---|---|---|
| 41A 41B | RD0+ | GND |
| 42A 42B | CLK0+ | CLK0– |
| 43A 43B | FP0+ | FP0– |
| 44A 44B | GND | GND |
| 45A 45B | GND | GND |
| 46A 46B | GND | GND |
| 47A 47B | BUS30 | BUS31 |
| 48A 48B | BUS28 | BUS29 |
| 49A 49B | BUS26 | BUS27 |
| 50A 50B | BUS24 | BUS25 |
| 51A 51B | BUS22 | BUS23 |
| 52A 52B | BUS20 | BUS21 |
| 53A 53B | BUS18 | BUS19 |
| 54A 54B | BUS16 | BUS17 |
| 55A 55B | GND | GND |
| 56A 56B | SYNCB | ENB |
| 57A 57B | VREF | MCLKB |
| 58A 58B | CUTO | RGND |
| 59A 59B | GND | GND |
| 60A 60B | BUS14 | BUS15 |
| 61A 61B | BUS12 | BUS13 |
| 62A 62B | BUS10 | BUS11 |
| 63A 63B | BUS8 | BUS9 |
| 64A 64B | BUS6 | BUS7 |
| 65A 65B | BUS4 | BUS5 |
| 66A 66B | BUS2 | BUS3 |
| 67A 67B | BUS0 | BUS1 |
| 68A 68B | GND | GND |
| 69A 69B | SYNCA | ENA |
| 70A 70B | VREF | MCLKA |
| 71A 71B | CUTO | RGND |
| 72A 72B | RGBUS0T | RGBUS0R |
| 73A 73B | RGND | RGND |
| 74A 74B | RING1T | RING1R |
| 75A 75B | A-C1T | A-C1R |
| 76A 76B | RING0T | RING0R |
| 77A 77B | A-C0T | A-C0R |
| 78A 78B | GND | GND |
| 79A 79B | +5 | +5 |
| 80A 80B | GND | GND |

# NTEX54AB

## Product description

The NTEX54AB data bus interface card (DBIC) is used in the 1 Meg Modem Service (1MMS) asymmetric digital subscriber loop (ADSL) access system to provide the interface between an Ethernet LAN (10BaseT) and multiple xDSL line cards (xLC, NTEX17AA or NTEX17BA) for high-speed data access. The DBIC also provides all the circuitry associated with the voice-only BIC (NT6X54AA) to allow continued POTS service. These interfaces are between 64 line cards in the line drawer and one 32-channel digroup to each line concentrating array (shelf).

### Location

The NTEX54AB is in the drawer of a line concentrating module (LCM). Each line drawer has one DBIC and a maximum of 64 line cards of different types. Each scan chip links one digroup with 32 line cards. If one digroup (scan chip) fails, the digroup that remains takes over all 64 lines.

## Functional description

The DBIC consists of two separate circuits. The first circuit consists of the components required to provide a voice path between two digroup controllers and the line cards. The second circuit consists of the components required to provide an interface between a 10BaseT port and the xDSL line cards. The common point between these two circuits is the XLBUS (eXtended LBUS). This is a point-to-point bus which communicates with the line cards.

Two X24 Scan ASICs form the heart of the BIC. These X24s interface two 32-channel digroup controllers with the 64 line cards for voice traffic. The controllers provide unidirectional serial lines (RCON and TCON) to exchange control and for status information. The controllers provide unidirectional serial lines (RD and RT) to carry user voice data, a frame pulse (FP), and a 5.12 MHz clock (CLK). An additional line (ACT) indicates that a particular controller is active. Thus one controller manages both X24s when the other controller fails or is being upgraded.

The NTEX54AB performs the following functions:

- multiplexes and demultiplexes a 32-channel link on 32 line card buses
- receives control messages to line cards asynchronously. Stores these messages until the messages are output to line cards during channels 0 or 16
- stores responses to control messages

- scans 32 line cards for changes in supervision bits. The NTEX54AA stores a message when the card detects a change in state.
- writes new information to the ring multiplexer

The scan chip demultiplexes each 32-channel serial (RD) link on 32 line card buses. The scan chip multiplexes the line card responses on the outgoing (TD) serial links. The multiplex uses a 32-byte connection memory in each scan chip. Each scan chip is accessed in sequence each channel time. One location of the connection memory corresponds to a specified channel time. The address of the line card accessed at that time is in this location. To assign line card numbers to channel times, the system writes to the connection memory with a message written to the chip on RCON. The message has the channel number and the line card address.

Control messages to line cards are written asynchronously following the channel times on the RCON. First, an input first-in-first-out (FIFO) base stores these messages on the scan chip. The messages remain on the scan chip until channel time 0 to 16. Second, the control message is output to the line card. If requested, an output FIFO stores the line card response on the chip. If the input FIFO does not contain control messages, channels 0 and 16 scan line cards. To scan line cards, send an output and idle code to the E99 integrated circuit (IC) on the addressed line card. Compare the state of the supervision bits (SV1, SV0) with the earlier two states of those bits from earlier scans. If two consecutive scans detect a change, the system loads the address and response of the line card into the output FIFO. The system scans all 32 cards every 4 ms if the system does not send control messages during that time. When the system sends a control message, the scan is on hold for one frame. When the LCM controller outputs the appropriate code on the RCON, the controller can read these scan messages. The controller responses to control messages. This action results in a response on the TCON that consists of one word from the output FIFO. All transactions on RCON and TCON are 20 bits long. The bits contain address (or op-code) and data.

The BIC holds the TCON low to alert the controller that the output FIFO contains a minimum of one word. When the FIFO is empty, the TCON remains high.

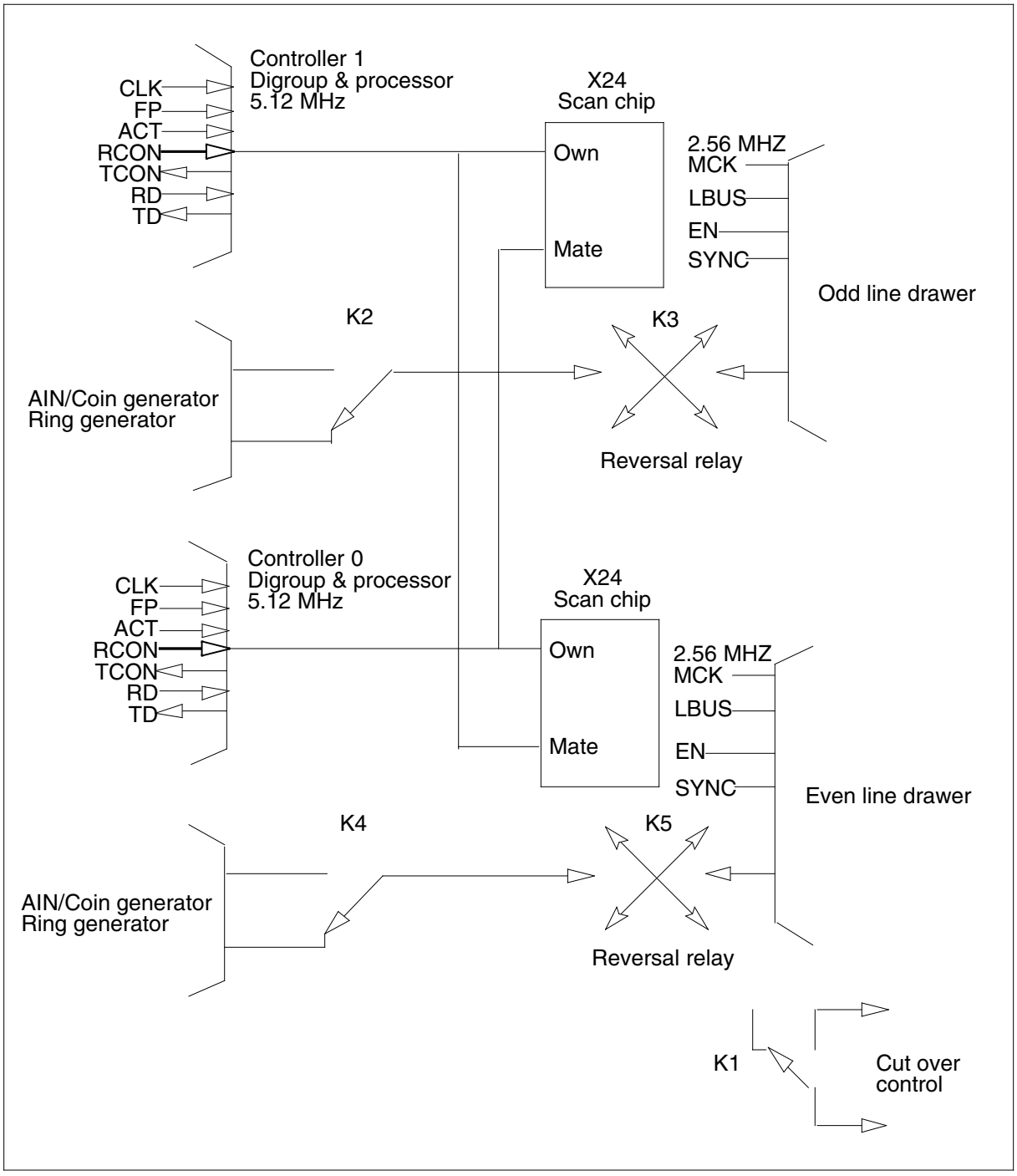
The NTEX54AB provides a +12.7V reference to all 64 line positions.

## Functional blocks

The relationship between the functional blocks appears in the following figure.

## **NTEX54AB** (continued)

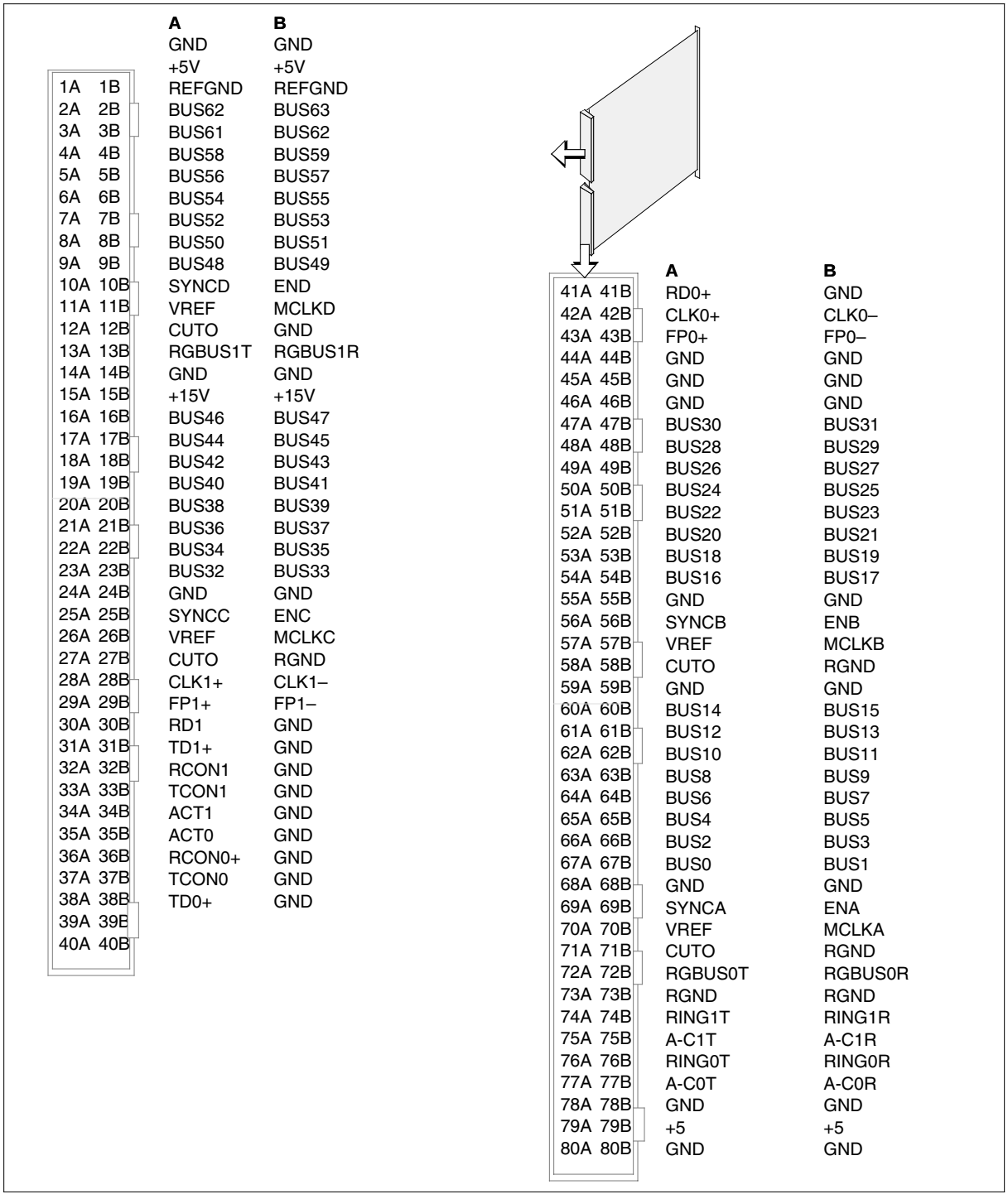
**TEX54AB functional blocks**




### Pin numbers

The pin numbers for the NTEX54AB appear in the following figure.

### NTEX54AB pin numbers



| | A | B |
|---|---|---|
| | GND | GND |
| | +5V | +5V |
| 1A 1B | REFGND | REFGND |
| 2A 2B | BUS62 | BUS63 |
| 3A 3B | BUS61 | BUS62 |
| 4A 4B | BUS58 | BUS59 |
| 5A 5B | BUS56 | BUS57 |
| 6A 6B | BUS54 | BUS55 |
| 7A 7B | BUS52 | BUS53 |
| 8A 8B | BUS50 | BUS51 |
| 9A 9B | BUS48 | BUS49 |
| 10A 10B | SYNCD | END |
| 11A 11B | VREF | MCLKD |
| 12A 12B | CUTO | GND |
| 13A 13B | RGBUS1T | RGBUS1R |
| 14A 14B | GND | GND |
| 15A 15B | +15V | +15V |
| 16A 16B | BUS46 | BUS47 |
| 17A 17B | BUS44 | BUS45 |
| 18A 18B | BUS42 | BUS43 |
| 19A 19B | BUS40 | BUS41 |
| 20A 20B | BUS38 | BUS39 |
| 21A 21B | BUS36 | BUS37 |
| 22A 22B | BUS34 | BUS35 |
| 23A 23B | BUS32 | BUS33 |
| 24A 24B | GND | GND |
| 25A 25B | SYNCC | ENC |
| 26A 26B | VREF | MCLKC |
| 27A 27B | CUTO | RGND |
| 28A 28B | CLK1+ | CLK1– |
| 29A 29B | FP1+ | FP1– |
| 30A 30B | RD1 | GND |
| 31A 31B | TD1+ | GND |
| 32A 32B | RCON1 | GND |
| 33A 33B | TCON1 | GND |
| 34A 34B | ACT1 | GND |
| 35A 35B | ACT0 | GND |
| 36A 36B | RCON0+ | GND |
| 37A 37B | TCON0 | GND |
| 38A 38B | TD0+ | GND |
| 39A 39B | | |
| 40A 40B | | |

| | A | B |
|---|---|---|
| 41A 41B | RD0+ | GND |
| 42A 42B | CLK0+ | CLK0– |
| 43A 43B | FP0+ | FP0– |
| 44A 44B | GND | GND |
| 45A 45B | GND | GND |
| 46A 46B | GND | GND |
| 47A 47B | BUS30 | BUS31 |
| 48A 48B | BUS28 | BUS29 |
| 49A 49B | BUS26 | BUS27 |
| 50A 50B | BUS24 | BUS25 |
| 51A 51B | BUS22 | BUS23 |
| 52A 52B | BUS20 | BUS21 |
| 53A 53B | BUS18 | BUS19 |
| 54A 54B | BUS16 | BUS17 |
| 55A 55B | GND | GND |
| 56A 56B | SYNCB | ENB |
| 57A 57B | VREF | MCLKB |
| 58A 58B | CUTO | RGND |
| 59A 59B | GND | GND |
| 60A 60B | BUS14 | BUS15 |
| 61A 61B | BUS12 | BUS13 |
| 62A 62B | BUS10 | BUS11 |
| 63A 63B | BUS8 | BUS9 |
| 64A 64B | BUS6 | BUS7 |
| 65A 65B | BUS4 | BUS5 |
| 66A 66B | BUS2 | BUS3 |
| 67A 67B | BUS0 | BUS1 |
| 68A 68B | GND | GND |
| 69A 69B | SYNCA | ENA |
| 70A 70B | VREF | MCLKA |
| 71A 71B | CUTO | RGND |
| 72A 72B | RGBUS0T | RGBUS0R |
| 73A 73B | RGND | RGND |
| 74A 74B | RING1T | RING1R |
| 75A 75B | A-C1T | A-C1R |
| 76A 76B | RING0T | RING0R |
| 77A 77B | A-C0T | A-C0R |
| 78A 78B | GND | GND |
| 79A 79B | +5 | +5 |
| 80A 80B | GND | GND |

# NTEX54BA

## Product description

The NTEX54BA data-enhanced bus interface card (DBIC) is a concentrator for the voice and data services in the 1-Meg Modem Service. The NTEX54BA provides the interface between xDSL line cards (xLC) and data networks for high speed data access.

### Location

The NTEX54BA resides in a line concentrating module (LCM) line drawer that provides 1-Meg Modem Service. One DBIC supports each LCM line drawer that provides 1-Meg Modem Service.

## Functional description

The NTEX54BA performs the functions that follow:

- full/half duplex, standard compliant Ethernet interface
- supports 10BaseT and 100BaseT connections through auto-sensing feature
- concentrates data from up to 31 xLCs onto 100BaseT
- backwards compatible with all POTS line cards compatible with NT6X54AA
- discovers xLCs automatically to allow for plug and play setup
- unique media access control (MAC) address for each xLC and DBIC
- demultiplexes 64 voice channels from receive data (RD) links to extended LBUS (XLBUS)
- multiplexes voice channels from XLBUS to transmit data (TD) links
- controls ring bus and automatic number ID (ANI)/COIN voltages

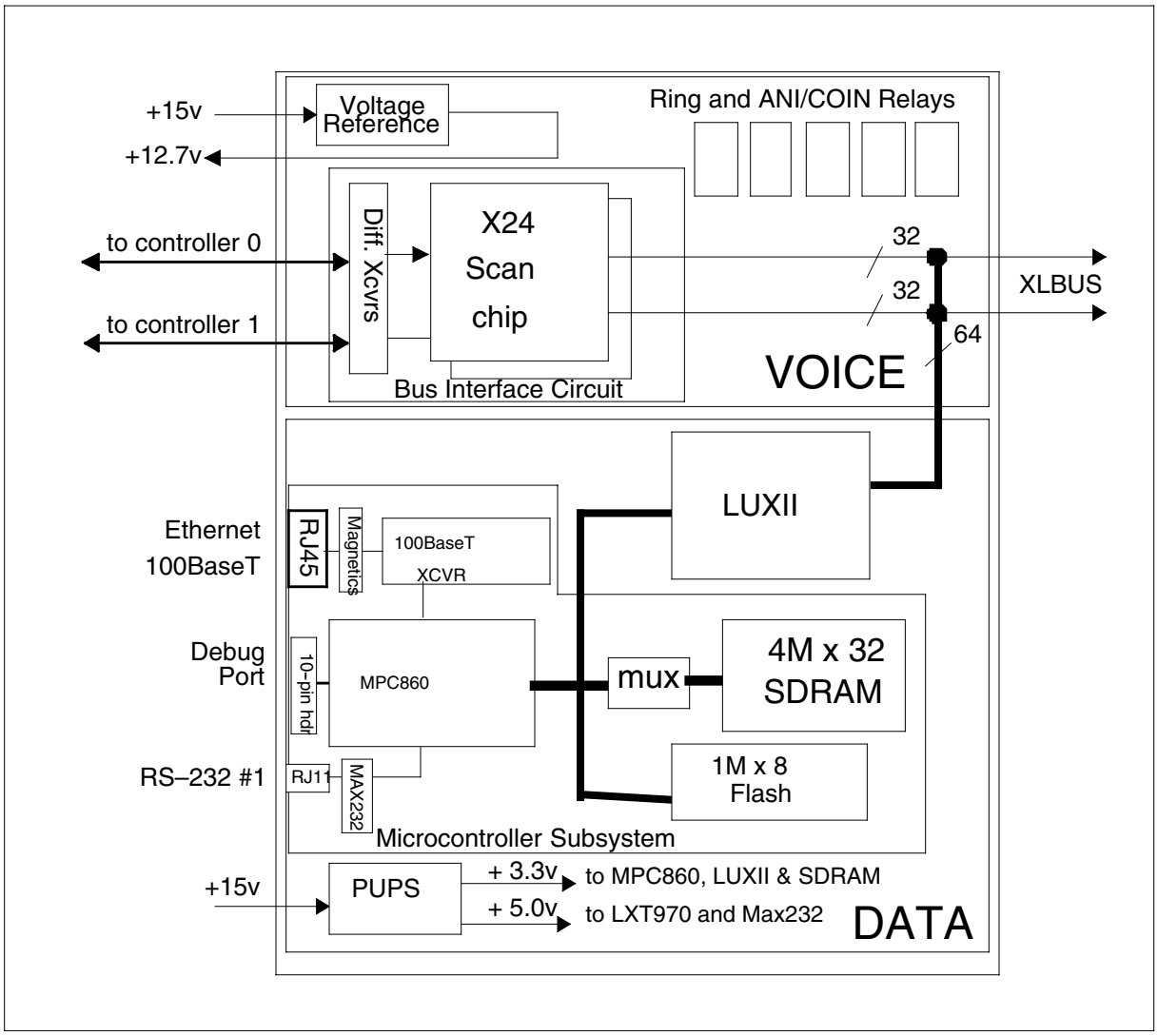
### Functional blocks

NTEX54BA includes the functional blocks that follow:

- Voice
  - — Bus interface circuit
  - — Relays
  - — Reference voltage
- Data
  - — Microcontroller subsystem
  - — LBUS-to-XLBUS ASIC II (LUXII)
  - — point-of-use power supply (PUPS)

The figure that follows shows the relationship of the functional blocks.

**NTEX54BA functional blocks**




## Bus interface circuit

The Bus interface circuit provides the interface between 64 line circuits and each of two units of the LCM. Two X24 Scan chips provide the interface between two 32-channel digroup controllers and the 64 line circuits for voice traffic.

## NTEX54BA (continued)

### Relays

Four relays control the ring bus to the line cards. The relays switch between the sources of ringing or ANI/COIN voltages. The X24 scan chips control the relays.

### Reference voltage

The coder-decoders (CODEC) on the line cards require an accurate +12.7/-0.08V at room temperature for proper operation. The backplane +15V serves as the input to a pass regulator (LM317).

### Microcontroller subsystem

Components of the microcontroller system follow:

- Motorola MPC860T PowerQUICC microcontroller with SDRAM, FLASH, and a 100BaseT Ethernet transceiver
- magnetics
- connector

### LUXII

The LUXII application specific integrated circuit (ASIC) provides the interface between the MPC860T and the xLCs over the XLBUS. Features of the LUXII follow:

- synchronizes to each line card individually and detects data opportunities on the XLBUS
- inserts downstream data on the XLBUS
- extracts upstream data from the XLBUS
- flags error conditions and assists in flow control
- sends and receives xLC control messages
- provides access to upstream and downstream control registers of LUXII and xLC

### PUPS

Two PUPS generate +5V and +3.3V for the data circuits.

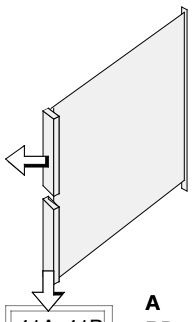
## Signaling

This section describes the signaling functions of the NTEX54BA.

### Pin outs

The figure that follows shows the pin outs for NTEX54BA.

### NTEX54BA pin outs



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | REFGND | REFGND |
| 4A 4B | BUS62 | BUS63 |
| 5A 5B | BUS60 | BUS61 |
| 6A 6B | BUS58 | BUS59 |
| 7A 7B | BUS56 | BUS57 |
| 8A 8B | BUS54 | BUS55 |
| 9A 9B | BUS52 | BUS53 |
| 10A 10B | BUS50 | BUS51 |
| 11A 11B | BUS48 | BUS49 |
| 12A 12B | SYNCD | END |
| 13A 13B | VREF | MCLKD |
| 14A 14B | CUTO | GND |
| 15A 15B | RGBUS1T | RGBUS1R |
| 16A 16B | GND | GND |
| 17A 17B | +15V | +15V |
| 18A 18B | BUS46 | BUS47 |
| 19A 19B | BUS44 | BUS45 |
| 20A 20B | BUS42 | BUS43 |
| 21A 21B | BUS40 | BUS41 |
| 22A 22B | BUS38 | BUS39 |
| 23A 23B | BUS36 | BUS37 |
| 24A 24B | BUS34 | BUS35 |
| 25A 25B | BUS32 | BUS33 |
| 26A 26B | GND | GND |
| 27A 27B | SYNCC | ENC |
| 28A 28B | VREF | MCLKC |
| 29A 29B | CUTO | RGND |
| 30A 30B | CLK1+ | CLK1– |
| 31A 31B | FP1+ | FP1– |
| 32A 32B | RD1 | GND |
| 33A 33B | TD1+ | GND |
| 34A 34B | RCON1 | GND |
| 35A 35B | TCON1 | GND |
| 36A 36B | ACT1 | GND |
| 37A 37B | ACT0 | GND |
| 38A 38B | RCON0+ | GND |
| 39A 39B | TCON0 | GND |
| 40A 40B | TD0+ | GND |

| | A | B |
|---|---|---|
| 41A 41B | RD0+ | GND |
| 42A 42B | CLK0+ | CLK0– |
| 43A 43B | FP0+ | FP0– |
| 44A 44B | GND | GND |
| 45A 45B | GND | GND |
| 46A 46B | GND | GND |
| 47A 47B | BUS30 | BUS31 |
| 48A 48B | BUS28 | BUS29 |
| 49A 49B | BUS26 | BUS27 |
| 50A 50B | BUS24 | BUS25 |
| 51A 51B | BUS22 | BUS23 |
| 52A 52B | BUS20 | BUS21 |
| 53A 53B | BUS18 | BUS19 |
| 54A 54B | BUS16 | BUS17 |
| 55A 55B | GND | GND |
| 56A 56B | SYNCB | ENB |
| 57A 57B | VREF | MCLKB |
| 58A 58B | CUTO | RGND |
| 59A 59B | GND | GND |
| 60A 60B | BUS14 | BUS15 |
| 61A 61B | BUS12 | BUS13 |
| 62A 62B | BUS10 | BUS11 |
| 63A 63B | BUS8 | BUS9 |
| 64A 64B | BUS6 | BUS7 |
| 65A 65B | BUS4 | BUS5 |
| 66A 66B | BUS2 | BUS3 |
| 67A 67B | BUS0 | BUS1 |
| 68A 68B | GND | GND |
| 69A 69B | SYNCA | ENA |
| 70A 70B | VREF | MCLKA |
| 71A 71B | CUTO | RGND |
| 72A 72B | RGBUS0T | RGBUS0R |
| 73A 73B | RGND | RGND |
| 74A 74B | RING1T | RING1R |
| 75A 75B | A-C1T | A-C1R |
| 76A 76B | RING0T | RING0R |
| 77A 77B | A-C0T | A-C0R |
| 78A 78B | GND | GND |
| 79A 79B | +5 | +5 |
| 80A 80B | GND | GND |

## **NTEX54BA** (end)

# Technical data

This section provides technical data on the NTEX54BA.

### Dimensions

The NTEX54BA has the same dimensions has the NT6X54 bus interface card (BIC).

### Power requirements

Two PUPS convert +15V from the backplane to the +3.3V and +5V for the data circuits. The voice circuits use the +15V from the backplane to ensure the reliability of the voice path.

# NTEX54CA

## Product description

The NTEX54CA data-enhanced bus interface card (DBIC) is a concentrator for the voice and data services in the 1-Meg Modem Service. The provides the interface between xDSL line cards (xLC) and data networks for high speed data access.

### Location

The NTEX54CA resides in a line concentrating module (LCM) line drawer that provides 1-Meg Modem Service. One DBIC supports each LCM line drawer that provides 1-Meg Modem Service.

## Functional description

The NTEX54CA performs the functions that follow:

- full/half duplex, standard compliant Ethernet interface
- supports 10BaseT and 100BaseT connections through auto-sensing feature
- concentrates data from up to 31 xLCs onto 100BaseT
- compatibility with other line cards
  - — with POTS line cards, backwards compatible with all line cards compatible with NT6X54AA
  - — with xDSL line cards (xLC), only compatible with NTEX17DA
- discovers xLCs automatically to allow for plug and play setup
- unique media access control (MAC) address for each xLC and DBIC
- demultiplexes 64 voice channels from receive data (RD) links to extended LBUS (XLBUS)
- multiplexes voice channels from XLBUS to transmit data (TD) links
- controls ring bus and automatic number ID (ANI)/COIN voltages

## NTEX54CA (continued)

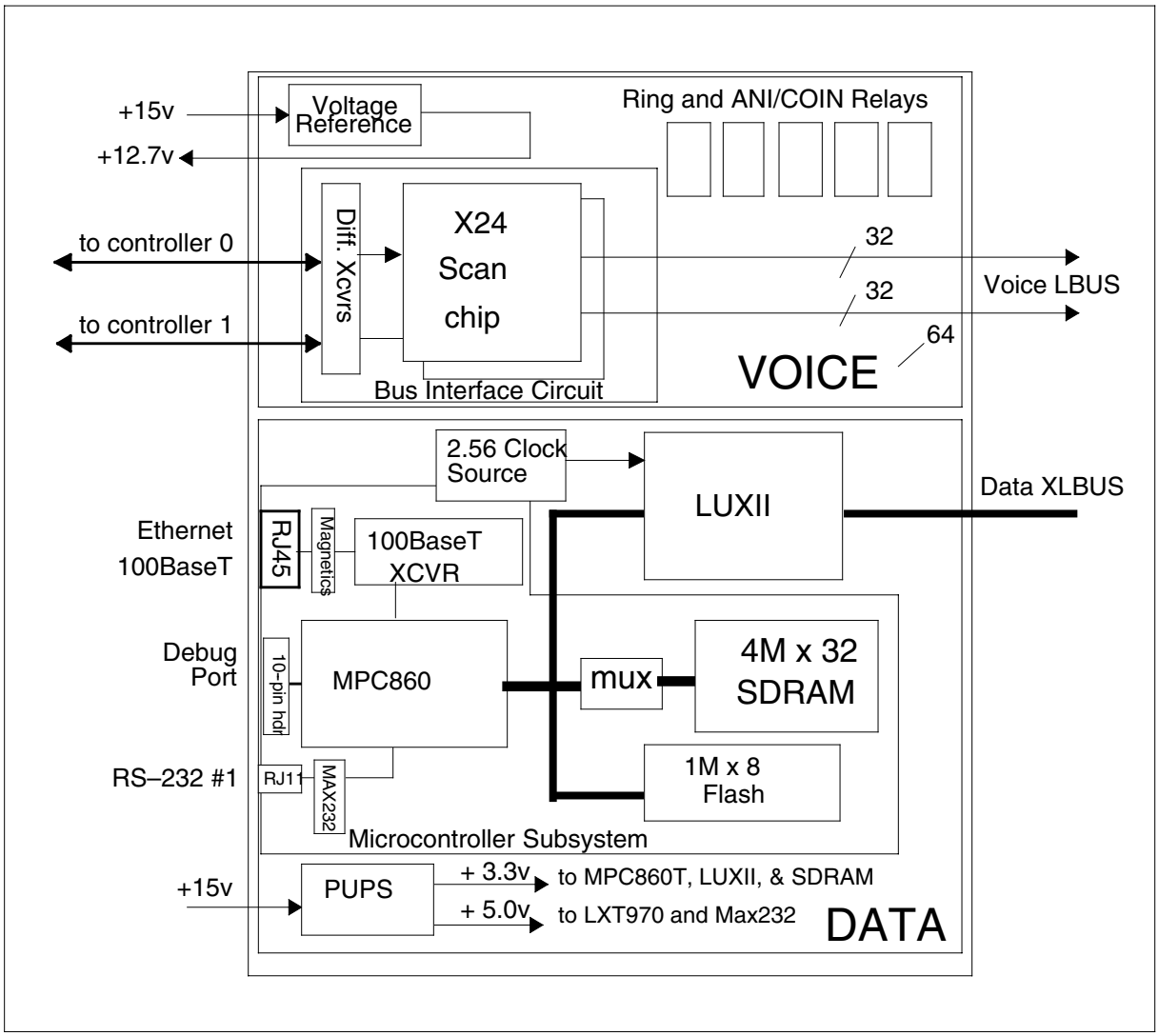
### Functional blocks

NTEX54CA includes the functional blocks that follow:

- Voice
  - — Bus interface circuit
  - — Relays
  - — Reference voltage
- Data
  - — Microcontroller subsystem
  - — LBUS-to-XLBUS ASIC II (LUXII)
  - — point-of-use power supply (PUPS)

The figure that follows shows the relationship of the functional blocks.

**NTEX54CA functional blocks**




## Bus interface circuit

The Bus interface circuit provides the interface between 64 line circuits and each of two units of the LCM. Two X24 Scan chips provide the interface between two 32-channel digroup controllers and the 64 line circuits for voice traffic.

## Relays

Four relays control the ring bus to the line cards. The relays switch between the sources of ringing or ANI/COIN voltages. The X24 scan chips control the relays.

## NTEX54CA (continued)

### Reference voltage

The coder-decoders (CODEC) on the line cards require an accurate +12.7/-0.08V at room temperature for proper operation. The backplane +15V serves as the input to a pass regulator (LM317).

### Microcontroller subsystem

Components of the microcontroller system follow:

- Motorola MPC860T PowerQUICC microcontroller with SDRAM, FLASH, and a 100BaseT Ethernet transceiver
- magnetics
- connector

### LUXII

The LUXII application specific integrated circuit (ASIC) provides the interface between the MPC860T and the xLCs over the XLBUS. Features of the LUXII follow:

- synchronizes to each line card individually and detects data opportunities on the XLBUS
- inserts downstream data on the XLBUS
- extracts upstream data from the XLBUS
- flags error conditions and assists in flow control
- sends and receives xLC control messages
- provides access to upstream and downstream control registers of LUXII and xLC

### PUPS

Two PUPS generate +5V and +3.3V for the data circuits.

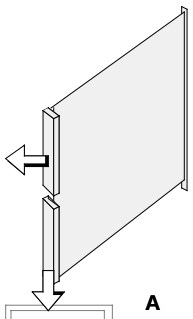
### Signaling

This section describes the signaling functions of the NTEX54CA.

#### Pin outs

The figure that follows shows the pin outs for NTEX54CA.

### NTEx54CA pin outs



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | REFGND | REFGND |
| 4A 4B | BUS62 | BUS63 |
| 5A 5B | BUS60 | BUS61 |
| 6A 6B | BUS58 | BUS59 |
| 7A 7B | BUS56 | BUS57 |
| 8A 8B | BUS54 | BUS55 |
| 9A 9B | BUS52 | BUS53 |
| 10A 10B | BUS50 | BUS51 |
| 11A 11B | BUS48 | BUS49 |
| 12A 12B | SYNCD | END |
| 13A 13B | VREF | MCLKD |
| 14A 14B | CUTO | GND |
| 15A 15B | RGBUS1T | RGBUS1R |
| 16A 16B | GND | GND |
| 17A 17B | +15V | +15V |
| 18A 18B | BUS46 | BUS47 |
| 19A 19B | BUS44 | BUS45 |
| 20A 20B | BUS42 | BUS43 |
| 21A 21B | BUS40 | BUS41 |
| 22A 22B | BUS38 | BUS39 |
| 23A 23B | BUS36 | BUS37 |
| 24A 24B | BUS34 | BUS35 |
| 25A 25B | BUS32 | BUS33 |
| 26A 26B | GND | GND |
| 27A 27B | SYNCC | ENC |
| 28A 28B | VREF | MCLKC |
| 29A 29B | CUTO | RGND |
| 30A 30B | CLK1+ | CLK1– |
| 31A 31B | FP1+ | FP1– |
| 32A 32B | RD1 | GND |
| 33A 33B | TD1+ | GND |
| 34A 34B | RCON1 | GND |
| 35A 35B | TCON1 | GND |
| 36A 36B | ACT1 | GND |
| 37A 37B | ACT0 | GND |
| 38A 38B | RCON0+ | GND |
| 39A 39B | TCON0 | GND |
| 40A 40B | TD0+ | GND |

| | A | B |
|---|---|---|
| 41A 41B | RD0+ | GND |
| 42A 42B | CLK0+ | CLK0– |
| 43A 43B | FP0+ | FP0– |
| 44A 44B | GND | GND |
| 45A 45B | GND | GND |
| 46A 46B | GND | GND |
| 47A 47B | BUS30 | BUS31 |
| 48A 48B | BUS28 | BUS29 |
| 49A 49B | BUS26 | BUS27 |
| 50A 50B | BUS24 | BUS25 |
| 51A 51B | BUS22 | BUS23 |
| 52A 52B | BUS20 | BUS21 |
| 53A 53B | BUS18 | BUS19 |
| 54A 54B | BUS16 | BUS17 |
| 55A 55B | GND | GND |
| 56A 56B | SYNCB | ENB |
| 57A 57B | VREF | MCLKB |
| 58A 58B | CUTO | RGND |
| 59A 59B | GND | GND |
| 60A 60B | BUS14 | BUS15 |
| 61A 61B | BUS12 | BUS13 |
| 62A 62B | BUS10 | BUS11 |
| 63A 63B | BUS8 | BUS9 |
| 64A 64B | BUS6 | BUS7 |
| 65A 65B | BUS4 | BUS5 |
| 66A 66B | BUS2 | BUS3 |
| 67A 67B | BUS0 | BUS1 |
| 68A 68B | GND | GND |
| 69A 69B | SYNCA | ENA |
| 70A 70B | VREF | MCLKA |
| 71A 71B | CUTO | RGND |
| 72A 72B | RGBUS0T | RGBUS0R |
| 73A 73B | RGND | RGND |
| 74A 74B | RING1T | RING1R |
| 75A 75B | A-C1T | A-C1R |
| 76A 76B | RING0T | RING0R |
| 77A 77B | A-C0T | A-C0R |
| 78A 78B | GND | GND |
| 79A 79B | +5 | +5 |
| 80A 80B | GND | GND |

## **NTEX54CA** (end)

# Technical data

This section provides technical data on the NTEX54CA.

### Dimensions

The NTEX54CA has the same dimensions has the NT6X54 bus interface card (BIC).

### Power requirements

Two PUPS convert +15V from the backplane to the +3.3V and +5V for the data circuits. The voice circuits use the +15V from the backplane to ensure the reliability of the voice path.

## Product description

The NTEX76AA high-speed signaling terminal (HST) card is part of the CCS7 high-speed link interface unit (HLIU) termination hardware set. The HLIU is a two-slot application specific unit (ASU) that consists of the following cards:

- NTEX22CA (32-Mbyte processor and F-bus controller)
- NTEX76AA (High-speed signaling terminal)
- NTEX78AA (DS-1 interface paddle board)

### Location

All HLIU card, including the NTEX76AA, are located on a link interface shelf (LIS) in an enhanced link peripheral processor (ELPP) cabinet.

## Functional description

The NTEX76AA card provides level two processing for the CCS7 high-speed links (HSL). It sends and receives data packets in the form of a serial data stream to and from the NTEX78AA paddle board. Data received from the NTEX78AA goes into the serial communications controllers (SCC) in the HST. The HST reconstructs received data packets and stores them in the interface RAM. From there, the NTEX22CA card retrieves the data.

### Functional blocks

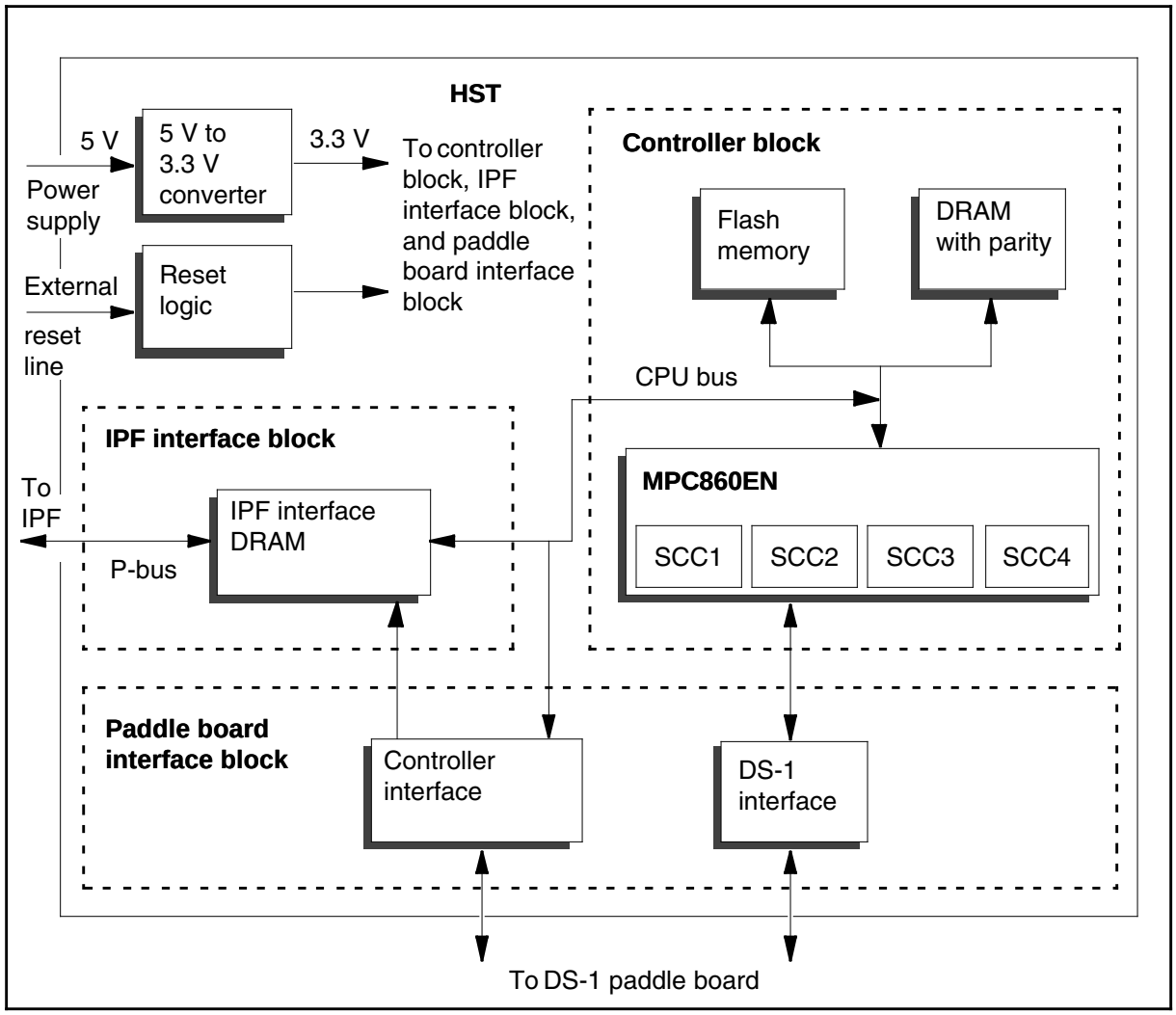
NTEX76AA has the following functional blocks:

- controller block
  - — MPC860EN microprocessor
  - — dynamic RAM (DRAM) and FLASH memory
- integrated processor and F-bus controller (IPF) interface
- paddle board interface
  - — controller interface
  - — DS-1 interface
- reset logic
- power converter for 3.3 V central processing unit (CPU) voltage

The following figure shows the relationship of the functional blocks.

## NTEX76AA (continued)

**NTEX76AA functional blocks**




### Controller block

The MPC860EN is a microprocessor that contains a 32-bit PowerPC core, four serial communication controller channels (SCC), a communications processor module (CPM), and a DRAM controller. The processor generates a 40-MHz clock.

The DRAM and FLASH memory stores codes and data for the HST processor. The FLASH memory size is 8 Mbyte and the DRAM size is 4 Mbyte.

### IPF interface

This block provides processor bus (P-bus) communication between the HST and the IPF (NTEX22CA card). Within this block there are two types of

memory: DRAM and identification (ID) PROM. The size of the IPF interface DRAM is 8 Mbytes. This memory stores the following types of messages:

- maintenance messages, which provide platform information and control
- application messages, which provide CCS7 information and control commands that affect network routing and performance
- message signaling units (MSU), which are CCS7 payload messages
- other common data, like control and sanity data, configuration data, and operational measurements (OM) data

### Paddle board interface

The controller interface provides communication between the HST and the DS-1 interface paddle board (NTEX78AA) for link maintenance. It also provides the IPF with direct access to the paddle board IDPROM.

The DS-1 interface is a matrix module that connects the unchannelized link to one of the SCC ports.

### Power converter

The power converter supplies 3.3 V to the processor.

### Reset logic

The voltage supervisor monitors the 5-V supply and generates a reset pulse (600 ms width) after power up and after any transients below 4.4 V. It also monitors the 3.3-V supply and generates a reset pulse after any transients below 2.5 V.

## Signaling

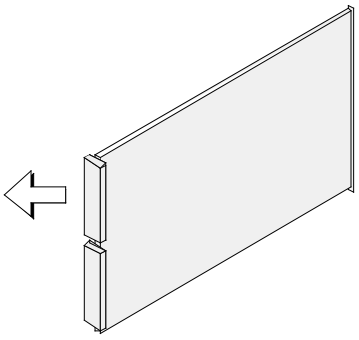
### Pin outs

The following figure shows the pin outs for NTEX76AA.

# **NTEX76AA** (continued)

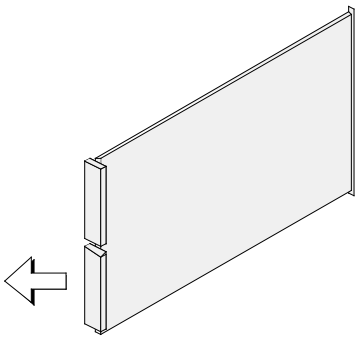
### NTEX76AA pin outs (part 1 of 2)

| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | GND |
| 2 | | | | GND |
| 3 | | | | GND |
| 4 | | | | GND |
| 5 | | | | GND |
| 6 | | | | GND |
| 7 | GND | RESET1 | | GND |
| 8 | | | | GND |
| 9 | | | | GND |
| 10 | | | GND | GND |
| 11 | | | | GND |
| 12 | | | | GND |
| 13 | | | | PBA00 |
| 14 | | | | PBA01 |
| 15 | GND | GND | | PBA02 |
| 16 | GND | GND | | PBA03 |
| 17 | | | | PBA04 |
| 18 | | | | PBA05 |
| 19 | | PERINT2– | | PBA06 |
| 20 | | PERINT3– | GND | PBin |
| 21 | GND | PERINT4– | | PBA07 |
| 22 | | | | PBA08 |
| 23 | RSTOUT– | | | PBA09 |
| 24 | | | | PBA10 |
| 25 | BEN1– | BENO– | | PBA11 |
| 26 | BEN3– | BEN2– | | |
| 27 | GND | | | PBA12 |
| 28 | WRT– | GND | | Reset |
| 29 | EDTACK | DTACK– | | HW4 |
| 30 | PARITY+ | | | GND |
| 31 | PRTYEN– | | | |
| 32 | | GND | | SH0 |
| 33 | DAS32– | | | SH1 |
| 34 | PBUSD00 | | | GND |
| 35 | PBUSD01 | PBUSA01 | | |
| 36 | PBUSD02 | PBUSA02 | HW0 | |
| 37 | PBUSD03 | PBUSA03 | HW1 | |
| 38 | PBUSD04 | PBUSA04 | HW2 | |
| 39 | PBUSD05 | PBUSA05 | HW3 | |
| 40 | PBUSD06 | PBUSA06 | | GND |
| 41 | PBUSD07 | PBUSA07 | | GND |
| 42 | PBUSD08 | PBUSA08 | | GND |
| 43 | PBUSD09 | PBUSA09 | | GND |
| 44 | PBUSD10 | PBUSA10 | | Power +5 |
| 45 | PBUSD11 | PBUSA11 | | Power +5 |



**NTEX76AA pin outs (part 2 of 2)**

| | D | C | B | A |
|---|---|---|---|---|
| 46 | PBUSD12 | PBUSA12 | | Power +5 |
| 47 | PBUSD13 | PBUSA13 | GND | Power +5 |
| 48 | PBUSD14 | PBUSA14 | | Power +5 |
| 49 | PBUSD15 | PBUSA15 | | Power +5 |
| 50 | PBUSD16 | PBUSA16 | GND | Power +5 |
| 51 | PBUSD17 | PBUSA17 | | Power +5 |
| 52 | PBUSD18 | PBUSA18 | | Power +5 |
| 53 | PBUSD19 | PBUSA19 | GND | Power +5 |
| 54 | PBUSD20 | PBUSA20 | | Power +5 |
| 55 | PBUSD21 | PBUSA21 | | Power +5 |
| 56 | PBUSD22 | PBUSA22 | GND | |
| 57 | PBUSD23 | PBUSA23 | | |
| 58 | PBUSD24 | PBUSA24 | | |
| 59 | PBUSD25 | PBUSA25 | | |
| 60 | PBUSD26 | PBUSA26 | | |
| 61 | PBUSD27 | PBUSA27 | | |
| 62 | PBUSD28 | PBUSA28 | | |
| 63 | PBUSD29 | PBUSA29 | | |
| 64 | PBUSD30 | PBUSA30 | | |
| 65 | PBUSD31 | PBUSA31 | | |
| 66 | | | | |
| 67 | | | | |
| 68 | | | | |
| 69 | | GND | | |
| 70 | | | | |
| 71 | SCC1DR | | | |
| 72 | SCC1DT | | | |
| 73 | SCC1CR | | | |
| 74 | SCC1CT | | | |
| 75 | PBD8 | PBD00 | | |
| 76 | PBD9 | PBD01 | | |
| 77 | PBD10 | PBD02 | | |
| 78 | PBD11 | PBD03 | | |
| 79 | PBD12 | PBD04 | TSET | GND |
| 80 | PBD13 | PBD05 | TxD | GND |
| 81 | PBD14 | PBD06 | TFP | GND |
| 82 | PBD15 | PBD07 | RxD | GND |
| 83 | PBA16 | RS232_RX | RSET | GND |
| 84 | PBA17 | RS232_TX | RFP | GND |
| 85 | PBA18 | PBCS- | PBA14 | GND |
| 86 | PBA19 | PBTA- | PBA15 | GND |
| 87 | SCC2DR | PWRFAIL | SCC3DR | GND |
| 88 | SCC2DT | PBR/W | SCC3DT | GND |
| 89 | SCC2CR | INT- | SCC3CR | RESET2 |
| 90 | SCC2CT | PBA13 | SCC3CT | GND |



## **NTEX76AA** (end)

# Technical data

### Power requirements

The following table shows the power requirements for the NTEX76AA.

**NTEX76AA power requirements**

| Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|
| Supply voltage | 4.75 V | 5 V | 5.25 V |

# NTEX78AA

## Product description

The NTEX78AA DS-1 interface paddle board is part of the CCS7 high-speed link interface unit (HLIU) termination hardware set. The HLIU is a two-slot application specific unit (ASU) that consists of the following cards:

- NTEX22CA (32-Mbyte processor and F-bus controller)
- NTEX76AA (High-speed signaling terminal)
- NTEX78AA (DS-1 interface paddle board)

NTEX78AA provides the physical connection between the CCS7 high-speed links (HSL) entering the HLIU unit and the high-speed signaling terminal (HST) card.

### Location

All HLIU cards, including the NTEX78AA, are located on a link interface shelf (LIS) in an enhanced link peripheral processor (ELPP) cabinet.

## Functional description

The NTEX78AA card terminates the CCS7 DS-1 HSLs. It provides the electrical interface between the HST card and the CCS7 HSLs, and performs all low-level DS-1 maintenance functions.

The NTEX78AA has the following DS-1 interface features:

- physical 100-Ω
- extended superframe
- frame synchronization, loss, and recovery
- detection and sending of the alarm indication signal (AIS)
- CRC6 error checking and generation
- alarms detection
- support for B8ZS line code
- performance monitoring
- loopback capability for local diagnostics

### Functional blocks

NTEX78AA has the following functional blocks:

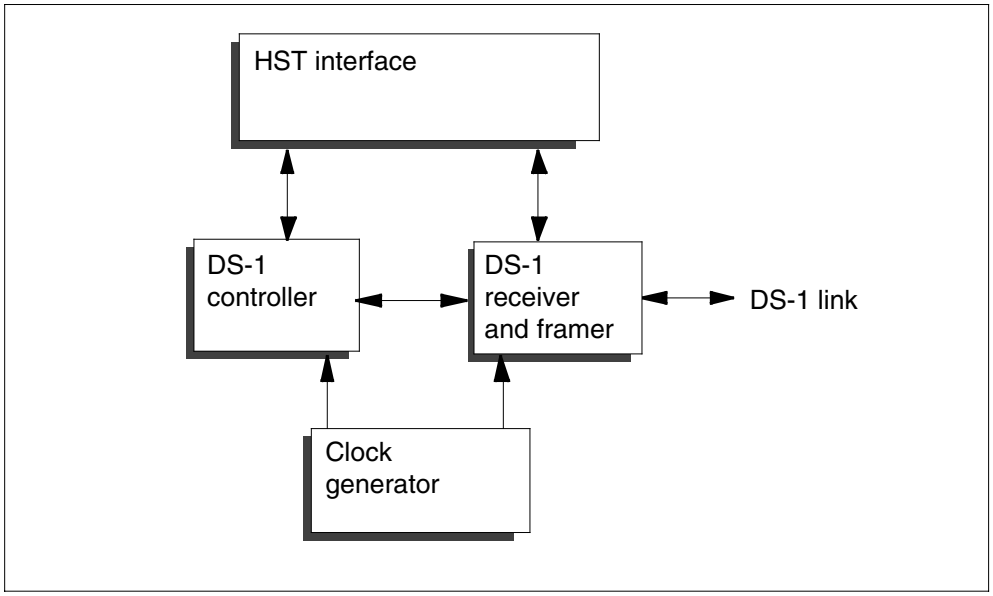
- DS-1 receiver and framer
- DS-1 controller

## NTEX78AA (continued)

- clock generator
- HST interface

The following figure shows the relationship of the functional blocks.

**NTEX78AA functional blocks**




### DS-1 receiver and framer

This block provides the analog line interface and the framing function to the DS-1 (1.544 Mbit/s) links. It receives and transmits data and operates in extended superframe (ESF) signaling format with line encoding.

The block includes a Siemens PEB2254 transceiver and a line protection circuit. The PEB2254 transceiver contains a CCS7 link interface unit (LIU7), an elastic memory, a framer, and a high-level data link controller (HDLC).

### DS-1 controller

This block performs the following functions:

- provides the monitoring of the DS-1 and the HDLC far-end performance messages
- creates the synchronized clocks for the transceiver and the HST serial communication controllers (SCC)

### Clock generator

This block checks the difference between the required and the existing clock.

It consists of the following devices:

- clock source selector
- digital-to-analog (DAC) converter
- voltage controller oscillator (VCXO)

  This clock is used for data transmission (DS-1) and DS-1 controller operation. During normal operation it is synchronized to F-bus 0 or F-bus 1. If both F-bus clocks are lost, this Stratum 3 clock is in free-running mode.

### HST interface

This block provides the interface between the NTEX78AA paddle board and the NTEX76AA card.

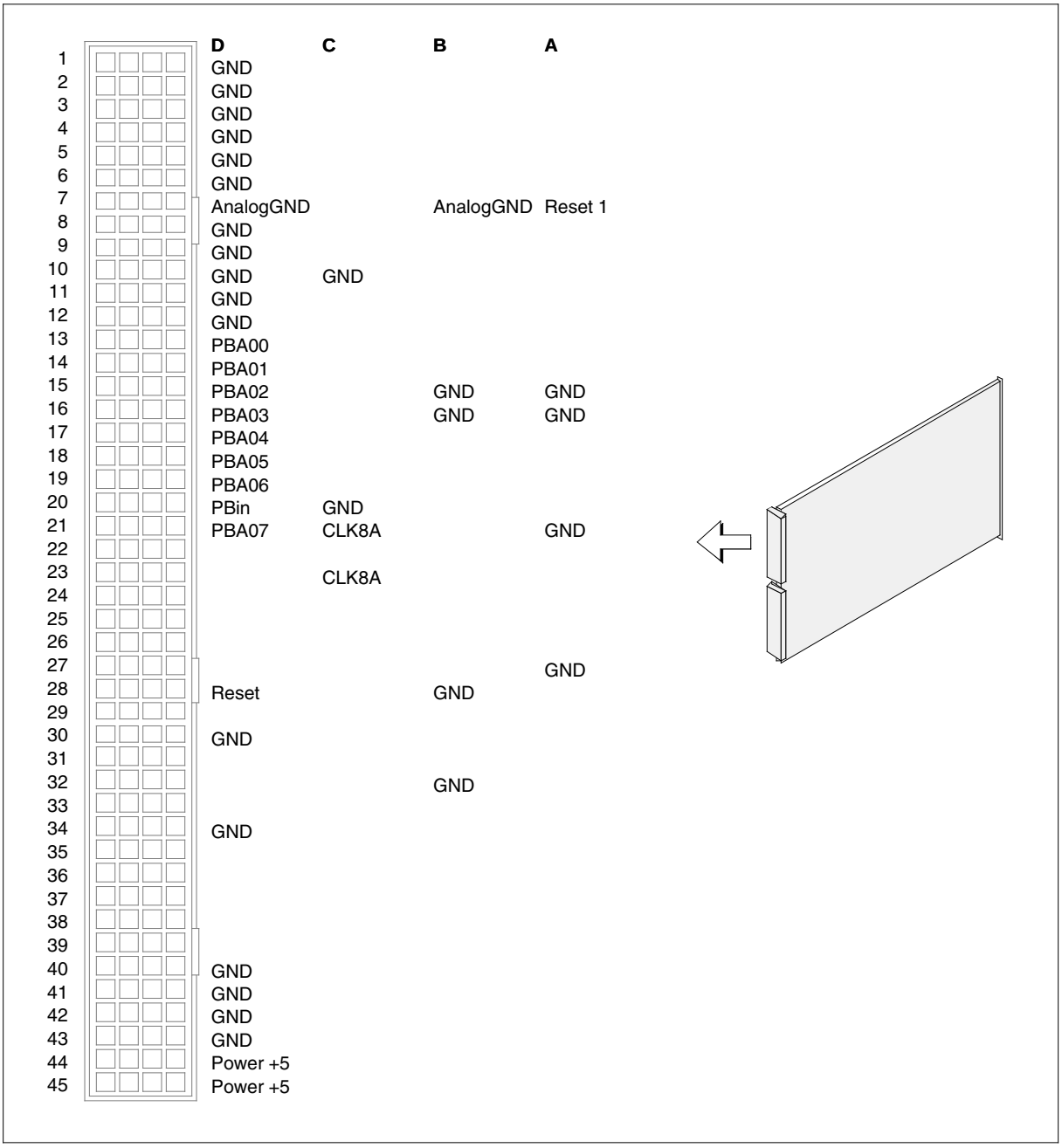
## Signaling

### Pin outs

The following figure shows the pin outs for NTEX78AA.

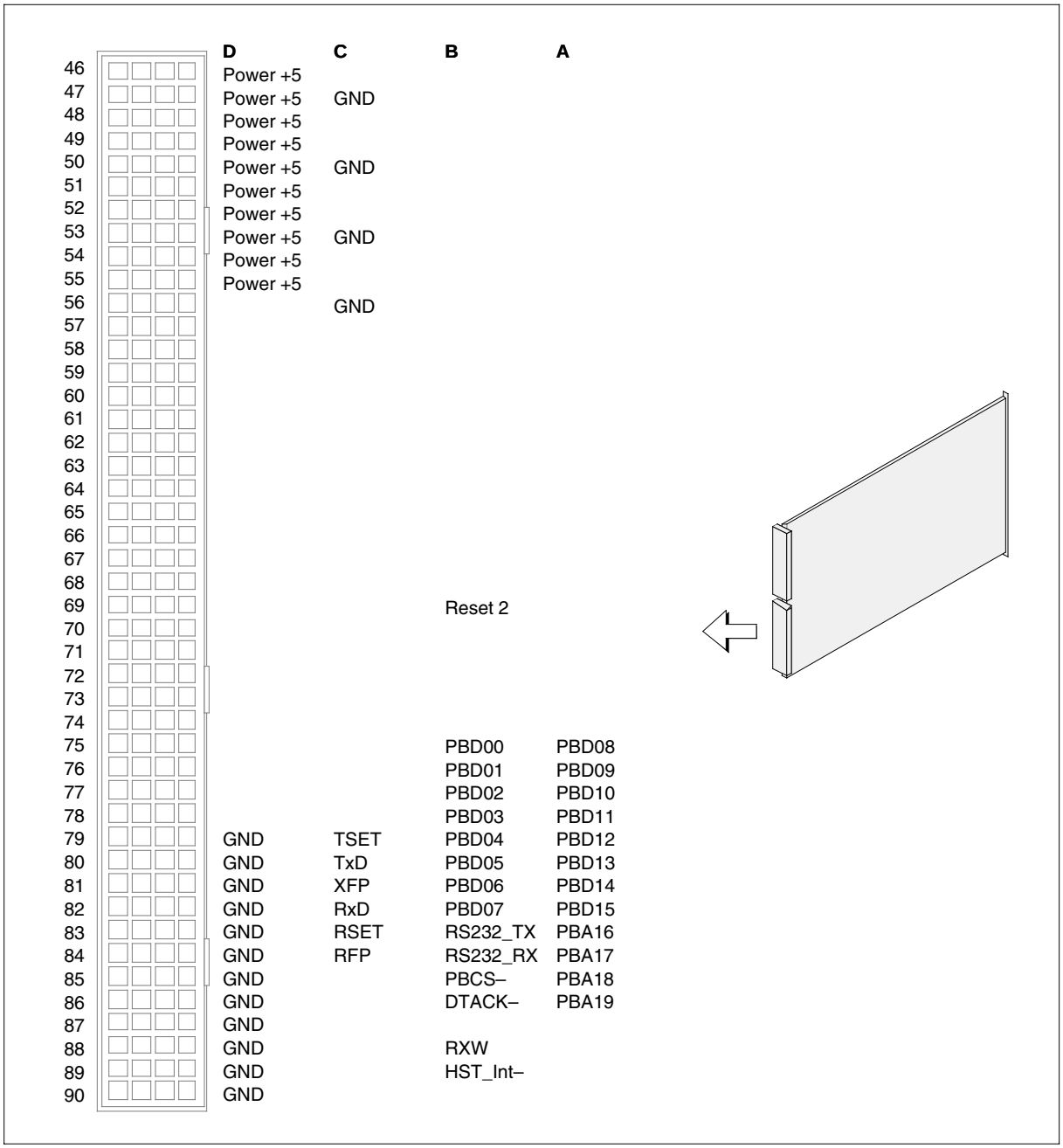
# **NTEX78AA** (continued)

### NTEX78AA pin outs (part 1 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 1 | GND | | | |
| 2 | GND | | | |
| 3 | GND | | | |
| 4 | GND | | | |
| 5 | GND | | | |
| 6 | GND | | | |
| 7 | AnalogGND | | AnalogGND | Reset 1 |
| 8 | GND | | | |
| 9 | GND | | | |
| 10 | GND | GND | | |
| 11 | GND | | | |
| 12 | GND | | | |
| 13 | PBA00 | | | |
| 14 | PBA01 | | | |
| 15 | PBA02 | | GND | GND |
| 16 | PBA03 | | GND | GND |
| 17 | PBA04 | | | |
| 18 | PBA05 | | | |
| 19 | PBA06 | | | |
| 20 | PBin | GND | | |
| 21 | PBA07 | CLK8A | | GND |
| 22 | | | | |
| 23 | | CLK8A | | |
| 24 | | | | |
| 25 | | | | |
| 26 | | | | |
| 27 | | | | GND |
| 28 | Reset | | GND | |
| 29 | | | | |
| 30 | GND | | | |
| 31 | | | | |
| 32 | | | GND | |
| 33 | | | | |
| 34 | GND | | | |
| 35 | | | | |
| 36 | | | | |
| 37 | | | | |
| 38 | | | | |
| 39 | | | | |
| 40 | GND | | | |
| 41 | GND | | | |
| 42 | GND | | | |
| 43 | GND | | | |
| 44 | Power +5 | | | |
| 45 | Power +5 | | | |

**NTEX78AA pin outs (part 2 of 2)**

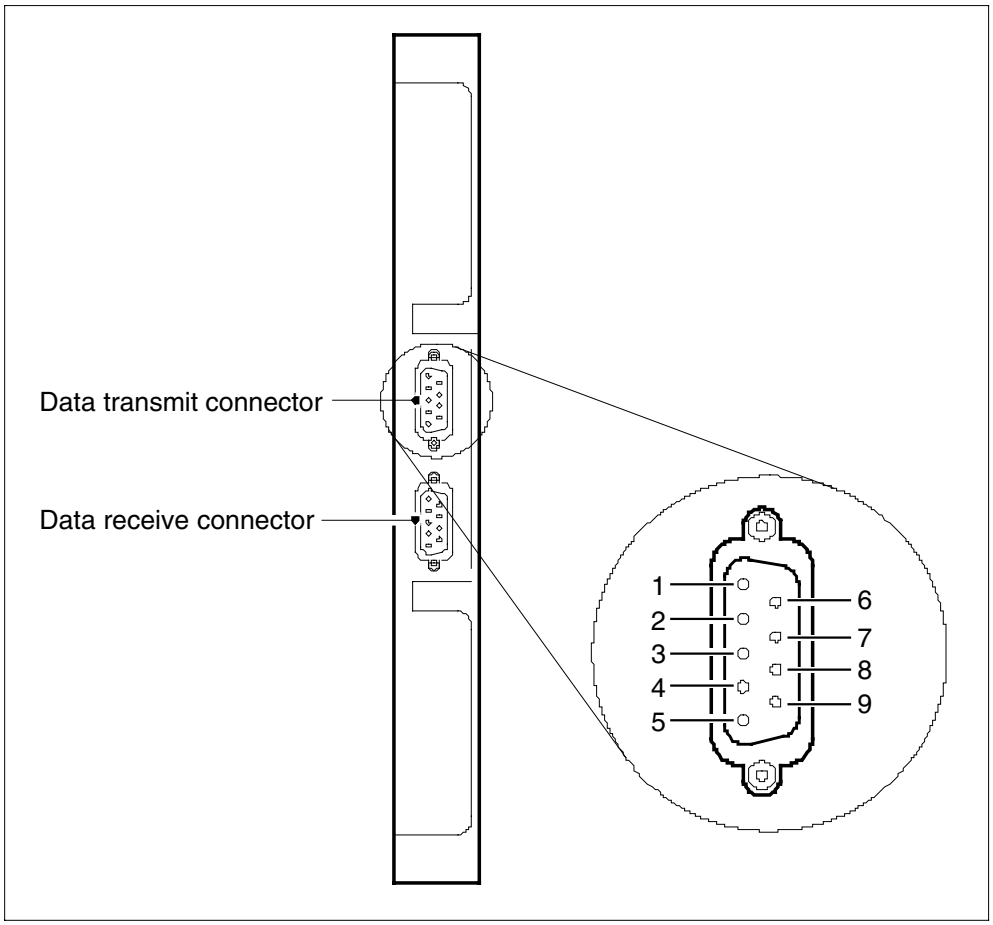



## Faceplate connectors

There are two faceplate connectors: the data transmit connector (upper) and the data receive connector (lower). Both are female, nine-pin, D-type connectors. The following figure shows the faceplace connectors.

## **NTEX78AA** (continued)

**Faceplate connectors**




The following tables list the pins and associated signals for both connectors.

**Data transmit connector**

| Pin number | Signal | Description |
|---|---|---|
| 3 | TTIP | Transmit tip |
| 7 | TRING | Transmit ring |
| 1, 2, 4, 5, 6, 8, 9 | FRAME GND | Frame ground |

**Data receive connector**

| Pin number | Signal | Description |
|---|---|---|
| 3 | RTIP | Receive tip |
| 7 | RRING | Receive ring |
| 1, 2, 4, 5, 6, 8, 9 | FRAME GND | Frame ground |

# Technical data

## Power requirements

The following table shows the power requirements for the NTEX78AA.

**NTEX78AA power requirements**

| Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|
| Supply voltage | 4.75 V | 5 V | 5.25 V |

# 7 NTFXnnaa

## NTFX09AA through NTFX44AA

# NTFX09AA

## Product description

The X.25/X.75 link interface unit (XLIU) uses the NTFX09AA network channel bus (C-bus) interface paddle board (CIP). The CIP is one of three circuit packs that form the XLIU. The CIP connects to the backplane C-bus to provide the high-level data link control (HDLC) frame processor (HFP) with channelized data. Combined with software, the XLIU hardware implements the DMS100 packet handler (DMSPH).

The NTFX09AA CIP has the following features:

- duplicated C-bus interface, that uses a single hardware fault to affect only one C-bus
- duplicated connection memory and controller, that causes a memory fault or a controller hardware fault to affect only one C-bus
- standard first-in-first-out (FIFO) interface between the CIP and the HFP, that allows the CIP to use in other applications for C-bus access
- standard processor bus (P-bus) interface for CIP control from a system master processor
- on-board 50 MHz crystal oscillator that allows P-bus access to occur, and a diagnostic mode to operate, when a CBC is not present
- loopback facility toward the C-bus (remote) and toward the HFP (local)
- the dynamic channel allocation is not permitted. Allocate channels at the time of configuration.

This CIP circuit pack is the first issue; backward compatibility is not a concern.

### Location

The NTFX09AA occupies the paddle board slot behind the HFP in the XLIU. The XLIU is an application-specific unit (ASU) that is in a link interface unit (LIU) shelf of the link peripheral processor (LPP). The XLIU can only be in a shelf with a provisioned network interface unit (NIU). The NIU requires 2 LIU positions (4 slots) in the center of the shelf.

## Functional description

The NTFX09AA routes data in the two directions between the C-bus channel and the HFP receive data highway. The data routes according to the contents of the connection memory.

The NTFX09AA CIP has the following functions:

- C-bus interfacing and plane resolution
- space switching
- P-bus access

The CIP duplicates C-bus electrical interfaces to recover and transmit data. The CIP performs active C-bus selection and provides data loopback away from and toward each channel.

The CIP duplicates connection memories to identify the C-bus channels to receive and transmit. Data received from active channels route to the HFP receive data highway. Data from the HFP transmit data highway is driven to active channels on the C-bus.

The CIP provides an interface so that an external processor (IPF) can access the connection memories and perform maintenance functions.

### Functional blocks

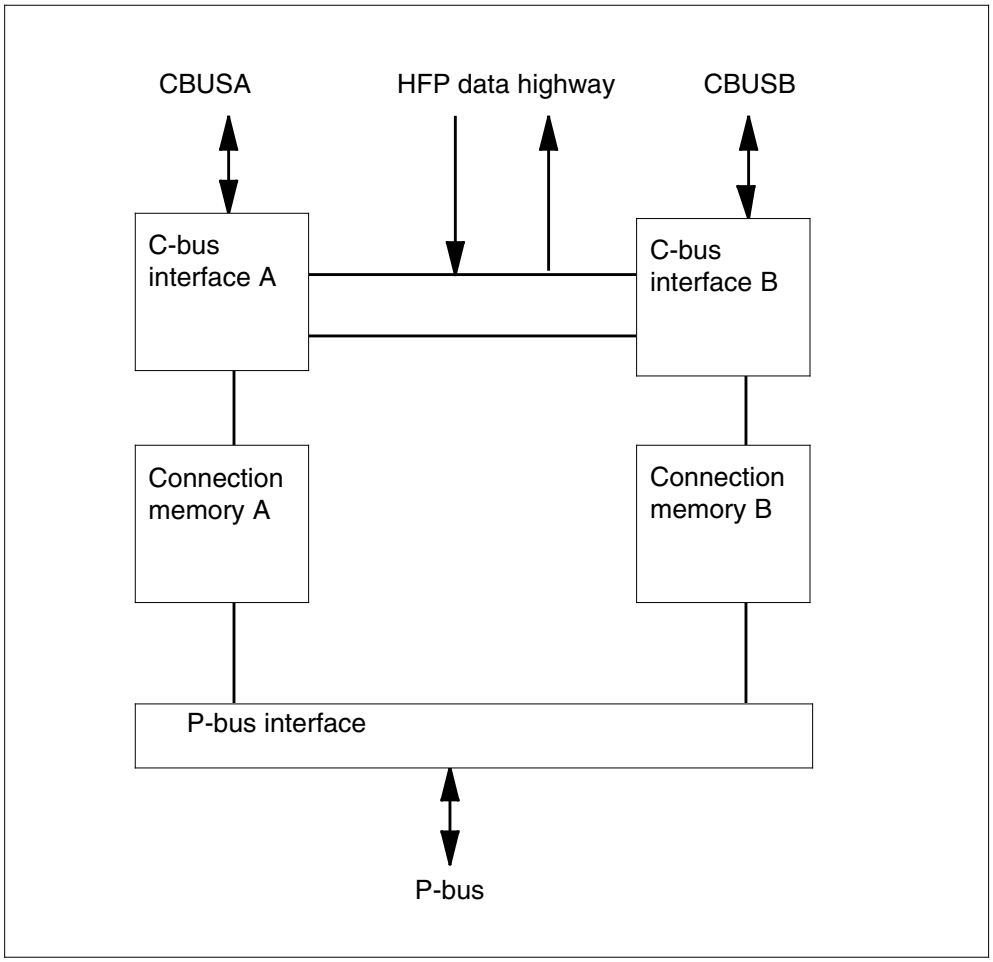
The NTFX09AA CIP has the following functional blocks:

- P-bus interface (PI)
- connection memories (CM) A and B
- C-bus interfaces (CI) A and B

The relationship between the functional blocks appears in the following figure.

## **NTFX09AA** (continued)

**NTFX09AA functional blocks**




### P-bus interface

The PI circuits provides IPF access to the connection memories, the control and status register, and identification PROM on the CIP. The interface provides data protection and C-bus error interrupt control. A programmable array logic (PAL) provides C-bus activity arbitration and latching of data from the HFP.

### Connection memories A and B

The CIP includes two CM blocks that limit the effect of a single hardware fault to only one C-bus. The CM contains a dual-port RAM that functions as a connection memory. The P-bus interface uses one port of the RAM for read/write access. The other port routes data between the C-bus and the HFP data highways.

### C-bus interfaces A and B

The CIP includes two C-bus interface (CI) blocks that limit the effect of a single hardware fault to only one C-bus. The CIs receive data from the C-bus and send data to the C-bus. The CM block controls these two operations. The CIs provide a loopback facility for each channel, outward on the C-bus, and inward across the data routing circuits. Another name for the CBUSA is the CBUS0. Another name for the CBUSB is the CBUS1.

## Technical data

### Power requirements

The NTFX09AA uses a 5V power supply.

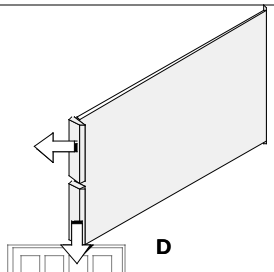
## Signaling

### Pin numbers

The pin numbers for the NTFX09AA appear in the following figures.

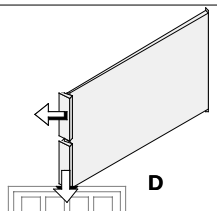
# **NTFX09AA** (continued)

### NTFX09AA pin numbers (Part 1 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | GND |
| 2 | | | | GND |
| 3 | | | | GND |
| 4 | | | | GND |
| 5 | | | | GND |
| 6 | | | | GND |
| 7 | GND | GND | | GND |
| 8 | | | | GND |
| 9 | | | | GND |
| 10 | | | GND | GND |
| 11 | | | | GND |
| 12 | | | | GND |
| 13 | | | | |
| 14 | | | | |
| 15 | GND | GND | | |
| 16 | GND | GND | | |
| 17 | | | | |
| 18 | | | | |
| 19 | | PERINT2 | | |
| 20 | | PERINT3 | GND | |
| 21 | GND | PERINT4 | | |
| 22 | | | | |
| 23 | RSTOUT | | | |
| 24 | | | | |
| 25 | BEN1N | BEN0N | | |
| 26 | BEN3N | BEN2N | | |
| 27 | GND | | | |
| 28 | WRTN | GND | | |
| 29 | EDTACK | | | |
| 30 | PARITY | | GND | |
| 31 | PRTYEN | | | |
| 32 | | GND | | |
| 33 | DAS32N | | | |
| 34 | | GND | | |
| 35 | | | | |
| 36 | | ADDR02 | | |
| 37 | | ADDR03 | | |
| 38 | | ADDR04 | | |
| 39 | | ADDR05 | | |
| 40 | | ADDR06 | | GND |
| 41 | | ADDR07 | | GND |
| 42 | | ADDR08 | | GND |
| 43 | | ADDR09 | | GND |
| 44 | | ADDR10 | | +5V |
| 45 | | ADDR11 | | +5V |

**NTFX09AA pin numbers (Part 2 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 46 | | ADDR12 | | +5V |
| 47 | | ADDR13 | GND | +5V |
| 48 | | ADDR14 | | +5V |
| 49 | | | | +5V |
| 50 | | | GND | +5V |
| 51 | | | CATFPN | +5V |
| 52 | | | CATCLK | +5V |
| 53 | | | GND | +5V |
| 54 | | | CBTFPN | +5V |
| 55 | | | CBTCLK | +5V |
| 56 | | | GND | |
| 57 | | | CBCBIDRN | CACBIDRN |
| 58 | DATA24 | ADDR24 | CBCBILPN | CACBILPN |
| 59 | DATA25 | ADDR25 | CBTD0 | CATD0 |
| 60 | DATA26 | ADDR26 | CBTD1 | CATD1 |
| 61 | DATA27 | ADDR27 | CBTD2 | CATD2 |
| 62 | DATA28 | ADDR28 | CBTD3 | CATD3 |
| 63 | DATA29 | ADDR29 | CBTD4 | CATD4 |
| 64 | DATA30 | ADDR30 | CBTD5 | CATD5 |
| 65 | DATA31 | ADDR31 | CBTD6 | CATD6 |
| 66 | | | CBTD7 | CATD7 |
| 67 | CACBIDSN | | CBTACTN | CATACTN |
| 68 | | | CBTPAR | CATPAR |
| 69 | CBCBIDSN | GND | CBRD0 | CARD0 |
| 70 | | | CBRD1 | CARD1 |
| 71 | | | CBRD2 | CARD2 |
| 72 | DCLK0 | | CBRD3 | CARD3 |
| 73 | | | CBRD4 | CARD4 |
| 74 | TXHFFL | | CBRD5 | CARD5 |
| 75 | | | CBRD6 | CARD6 |
| 76 | | TXHWY3 | CBRD7 | CARD7 |
| 77 | | TXHWY4 | CBRINDN | CARINDN |
| 78 | | TXHWY5 | CBRPAR | CARPAR |
| 79 | | TXHWY6 | | GND |
| 80 | | TXHWY7 | TXEMPTY | GND |
| 81 | | RXHWY0 | TXFMARK | GND |
| 82 | | RXHWY1 | | GND |
| 83 | | RXHWY2 | RXWR | GND |
| 84 | | RXHWY3 | RXFMARK | GND |
| 85 | | RXHWY4 | TXDR | GND |
| 86 | | RXHWY5 | TXHWY0 | GND |
| 87 | | RXHWY6 | TXHWY1 | GND |
| 88 | | RXHWY7 | TXHWY2 | GND |
| 89 | | | | GND |
| 90 | | | | GND |

# NTFX10AA

## Product description

The X.25/X.75 link interface unit (XLIU) uses the NTFX10AA high-level data link control (HDLC) frame processor (HFP) circuit pack. The HFP is one of three circuit packs that form the XLIU. The XLIU hardware implements the DMS-100 packet handler (DMS-PH) when combined with software.

Each XLIU can access the message switch frame bus (F-bus) and the network channel bus (C-bus). This condition occurs when the LIU shelf has a network interface unit (NIU) pair.

The XLIU is an application specific unit. The XLIU is a three-card set that contains the following parts:

- NTFX10AA HFP circuit pack
- NTFX09AA C-bus interface paddle board (CIP)
- current NTEX22BB integrated processor and F-bus interface (IPF)

The HFP works with the CIP.

The CIP connects to the backplane C-bus to provide the HFP with channelized data.

The IPF is the master processor where layer three processing occurs on HDLC frames that the HFP receives.

### Location

The NTFX10AA HFP circuit pack is one of three circuit packs in the XLIU. The XLIU is in an LIU shelf of the link peripheral processor (LPP). The XLIU can only be in a shelf with a provisioned NIU. The NIU pair requires two LIU positions (four slots) in the center of the shelf.

The link peripheral processor (LPP) is a current product. Units already support CCS7 (LIU7), Ethernet (EIU), and frame relay (FRIU) applications.

## Functional description

The NTFX10AA performs the following functions:

- HDLC frame reception and message recovery
- layer 2 processing
- HDLC frame formatting and transmission
- processor bus (P-bus) access for layer three processing

### HDLC frame reception and message recovery

The HFP performs the start of frame level processing of received channelized HDLC frames from the CIP. The HFP performs HDLC message recovery procedures on an interleaved basis for each channel. The HFP translates the extracted message to the buffer memory.

### Layer two processing

The microprocessor of the HFP performs layer two processing on received and transmitted HDLC frames. The microprocessor has arbitrated access to the buffer memory.

### HDLC frame formatting and transmission

The HFP transfers messages for transmission from the buffer memory and formats the messages to the HDLC frame format. This event occurs for messages to transmit across channels to the CIP.

### Processor bus access for layer three processing

The HFP provides an interface for an external processor, the IPF. This interface allows the IPF to arbitrate for access to the buffer memory for layer three processing.

## Functional blocks

The NTFX10AA has the following functional blocks:

- buffer memory (BM)
- HDLC transceiver cell (HTC)
- HFP processor (HP)
- P-bus interface (PI)

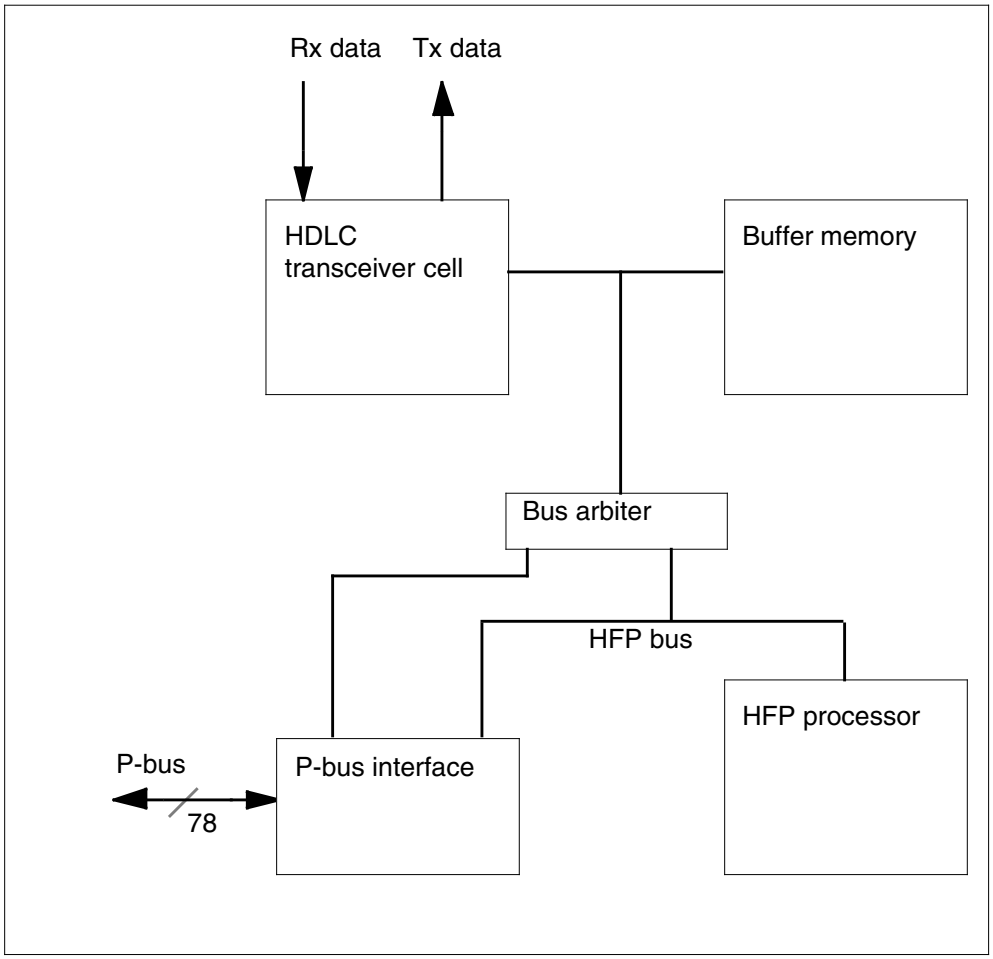
The relationship between the function blocks appears in the following figure.

### Buffer memory

The buffer memory is a memory array that stores HDLC buffers from the R75 multiport direct memory access controller (MPDMA). The data in the memory is parity protected. The bus arbiter controls the access to the buffer memory. The HFP processor or the IPF through the P-bus interface can access the buffer memory.

## **NTFX10AA** (continued)

**NTFX10AA functional blocks**




### HDLC transceiver cell

The HTC contains an S01/R75 pair. The HP controls the S01 multiport HDLC chip and the R75. This condition occurs after a request to access to the buffer memory bus from the bus arbiter.

The S01/R75 pair extracts message data from channelized HDLC format frames received from the CIP. The HTC arbitrates for access to the buffer memory and transfers the message data to memory. The HTC transfers message data from the buffer memory in the other direction. The HTC formats the message for transmission by the CIP.

### HFP processor

The HP contains a 68030 microprocessor and support circuits that performs layer two processing of the message data in the buffer memory. The HP has

two Mbytes of DRAM organized as 512 Kbytes deep 32 bits wide. These two Mbytes of DRAM are for program storage for the HFP processor.

### Processor bus interface

The PI contains arbitration and isolation circuits that provides IPF access to the HP program store or the buffer memory. The data interface is 32 bits wide for maximum data transfer speed. The data interface provides data protection and interrupt control.

## Technical data

### Power requirements

The measured power requirement of the HFP is 8W.

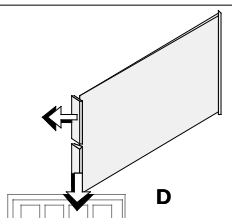
## Signaling

### Pin numbers

The NTFX10AA pin numbers appear in the following figure.

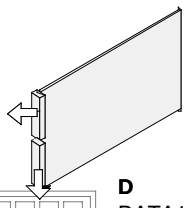
# **NTFX10AA** (continued)

### NTFX10AA pin numbers (Part 1 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | | GND |
| 2 | | | | GND |
| 3 | | | | GND |
| 4 | | | | GND |
| 5 | | | | GND |
| 6 | | | | GND |
| 7 | GND | GND | | GND |
| 8 | | | | GND |
| 9 | | | | GND |
| 10 | | | GND | GND |
| 11 | | | | GND |
| 12 | | | | GND |
| 13 | | | | RXDA |
| 14 | | | | TMS |
| 15 | GND | GND | | TCLK |
| 16 | GND | GND | | TMODE |
| 17 | | | | |
| 18 | | | | TXDA |
| 19 | | | | TSELECT |
| 20 | | | GND | TDATIN |
| 21 | GND | | | |
| 22 | | | | TDATOUT |
| 23 | RSTOUT | | | ETMEN |
| 24 | PERINT1 | PERINT0 | | |
| 25 | BEN1N | BEN0N | | |
| 26 | BEN3N | BEN2N | | |
| 27 | GND | | | |
| 28 | WRTN | GND | | |
| 29 | EDTACK | DTACK | | |
| 30 | PARITY | | | GND |
| 31 | PRTYEN | | | |
| 32 | | GND | | |
| 33 | DAS32N | | | |
| 34 | DATA00 | | | GND |
| 35 | DATA01 | | | |
| 36 | DATA02 | ADDR02 | | |
| 37 | DATA03 | ADDR03 | | |
| 38 | DATA04 | ADDR04 | | |
| 39 | DATA05 | ADDR05 | | |
| 40 | DATA06 | ADDR06 | | GND |
| 41 | DATA07 | ADDR07 | | GND |
| 42 | DATA08 | ADDR08 | | GND |
| 43 | DATA09 | ADDR09 | | GND |
| 44 | DATA10 | ADDR10 | | +5V |
| 45 | DATA11 | ADDR11 | | +5V |

**NTFX10AA pin numbers (Part 2 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 46 | DATA12 | ADDR12 | | |
| 47 | DATA13 | ADDR13 | GND | +5V |
| 48 | DATA14 | ADDR14 | | +5V |
| 49 | DATA15 | ADDR15 | | +5V |
| 50 | DATA16 | ADDR16 | GND | +5V |
| 51 | DATA17 | ADDR17 | | +5V |
| 52 | DATA18 | ADDR18 | | +5V |
| 53 | DATA19 | ADDR19 | GND | +5V |
| 54 | DATA20 | ADDR20 | | +5V |
| 55 | DATA21 | ADDR21 | | +5V |
| 56 | DATA22 | ADDR22 | GND | |
| 57 | DATA23 | ADDR23 | | |
| 58 | DATA24 | ADDR24 | | |
| 59 | DATA25 | ADDR25 | | |
| 60 | DATA26 | ADDR26 | | |
| 61 | DATA27 | ADDR27 | | |
| 62 | DATA28 | ADDR28 | | |
| 63 | DATA29 | ADDR29 | | |
| 64 | DATA30 | ADDR30 | | |
| 65 | DATA31 | ADDR31 | | |
| 66 | | | | |
| 67 | | | | |
| 68 | | | | |
| 69 | | GND | | |
| 70 | | | | |
| 71 | | | | |
| 72 | DCLK0 | | | |
| 73 | RXHFFL | | | |
| 74 | TXHFFL | | | |
| 75 | | | | |
| 76 | | TXHWY3 | | |
| 77 | | TXHWY4 | | |
| 78 | | TXHWY5 | | |
| 79 | | TXHWY6 | | GND |
| 80 | | TXHWY7 | TXEMPTY | GND |
| 81 | | RXHWY0 | TXFMARK | GND |
| 82 | | RXHWY1 | RXFULL | GND |
| 83 | | RXHWY2 | RXWR | GND |
| 84 | | RXHWY3 | RXFMARK | GND |
| 85 | | RXHWY4 | TXRD | GND |
| 86 | | RXHWY5 | TXHWY0 | GND |
| 87 | | RXHWY6 | TXHWY1 | GND |
| 88 | | RXHWY7 | TXHWY2 | GND |
| 89 | | | | GND |
| 90 | | | | GND |

# NTFX40AA

## Description

The cabinetized integrated services module (CISM) contains a maximum of four integrated services modules (ISM). The design is a modular, standard-wired cabinet with shelves. The top shelf can be provisioned.

For each new office, the first CISM must have the following units:

- an alarm cross-connect unit (NT3X89CA) in shelf position 47
- a primary alarm ISM unit (NTFX4101) mounted in shelf position 33
- a secondary ISM unit (NTFX4101) mounted in shelf positions 19
- an additional ISM unit can mount in shelf position 05

All connections to and from the ISM connect through the cabinet bulkhead to comply with electromagnetic interference (EMI).

The NTFX40AA operates only with SuperNode.

## Parts

The NTFX40AA contains the following parts:

- NTFX4101—ISM shelf assembly
- NTFX4011—modular supervisory panel kit, -48 V or -60 V (dc)
- NTRX91AA—cooling unit (CU), -48 V or -60 V (dc)
- NT3X89CA—alarm cross-connect unit (AXU)
- P0575239—filler panel for AXU
- P0684448—51 mm (2 in.) filler plate
- P0715586—personality plate for AXU
- P0745181—personality plate for ISM

### Integrated services module (ISM) shelf assembly

The NTFX4101 shelf assembly contains parts that form an ISM. The NTFX4101 provides 21 slots that connect the following:

- a single-slot ISM processor (NTFX42AA)
- a two-slot ISM DC power converter (NTFX43AA)
- a maximum of 18 service circuits

Of the 18 service circuit slots, PM service circuits that require power conversion only use slots 05 to 17. The PM service circuits that do not require

power conversion use slots 03 to 17, for example CTM. One slot (05) is available for one of the circuit cards that are not PM in a dual-card device. An example of the device is the metallic test unit (MTU).

The NTFX4101 ISM is a single shelf unit that replaces the current trunk module (TM) shelf or the maintenance trunk module (MTM) shelf. The ISM shelf attaches to the CISM that contains a maximum of four ISM shelves. Three ISM shelves are available. The top shelf can be provisioned.

The ISM shelf connects with the DMS switch in the same method as the current TM and MTM shelves. The ISM processor has a DS-30 link interface with the network. Each plane of the network has a link. The ISM processor has bus connections with service circuit cards that use the back panel. The service circuits determine the P-side interface on the ISM shelf. The ISM can operate with TM/MTM mounted on a TME and PMs in a DMS switch.

### Modular supervisory panel kit

The NTFX4011 modular supervisory panel (MSP) kit contains power control and alarm circuits. The circuits provide interfaces between the power distribution center and the equipment in the CISM.

The MSP provides a point to monitor the NTFX40AA. The NTFX4011 provides alarms to indicate problems in the NTFX40AA. Problems include a cooling unit that does not function, or functions out of the correct range.

The MSP includes the following:

- a fan-fail and frame-fail indicator
- a fuse-fail alarm output
- front and rear alarm battery supply (ABS) test jacks
- four front-panel services jacks: two telephone pairs (**TEL-A** and **TEL-B**) and two data pairs (**DATA-A** and **DATA-B**)

### Cooling unit

The NTRX91AA cooling unit cools the NTFX40AA with forced air. The NRX91AA is a subset of the NTRX92AA cooling unit kit. The NRX91AA contains an air filter, slider brackets, a fan power/alarm cable, and hardware to mount the unit.

### Alarm cross-connect unit (AXU)

The alarm cross-connect unit shelf is part of an alarm system for a large office. Each office must have one AXU shelf. The AXU requires a primary alarm maintenance trunk module, an office alarm unit (OAU). The OAU and the backup MTM contain the alarm control circuit cards. The AXU routes alarm

## **NTFX40AA** (continued)

signals. The AXU uses a secondary alarm unit. The AXU and the primary alarm maintenance trunk module and secondary alarm are a functional trio and mount on the same cabinet.

### Filler panels

The P0684448 filler plate covers space that is not used. The P0684448 filler plate is at shelf position 65 in the CISM.

The P0575239 filler panel conceals a compartment that contains the NT3X89CA AXU. The P0575239 filler panel is at shelf position 47 in the CISM.

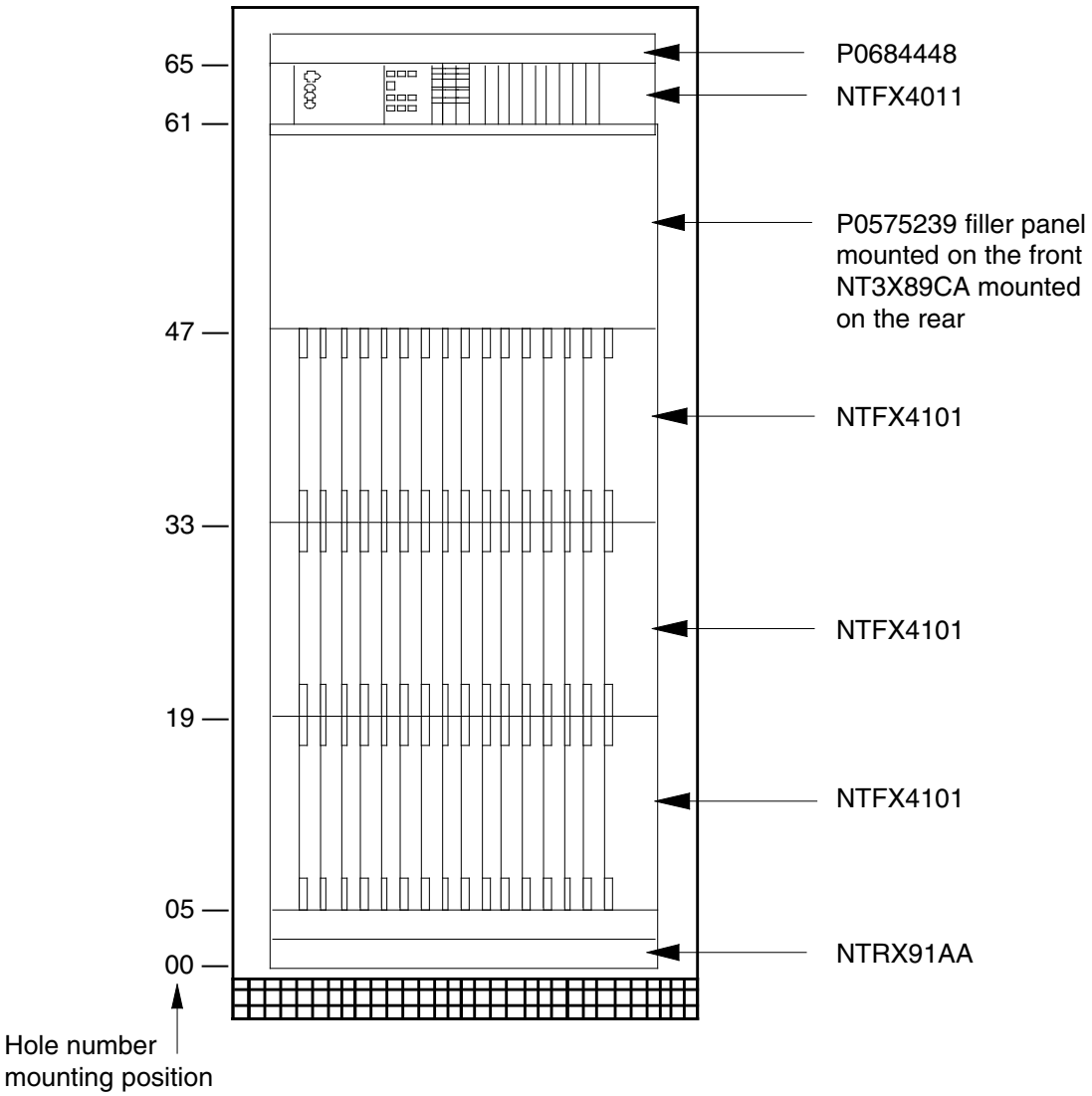
### Personality plates

Personality plates identify the correct connector mounting in the shelves of the CISM. For an AXU, P0715586 personality plate is at shelf position 47. For the primary ISM, P0748848 personality plate is at shelf position 33. For the secondary ISM, P07455181 personality plate is at shelf positions 19 and 05. Personality plate P07455181 can be provisioned on shelf positions 33 and 47.

## Design

The following figure describes the design of the NTFX40AA.

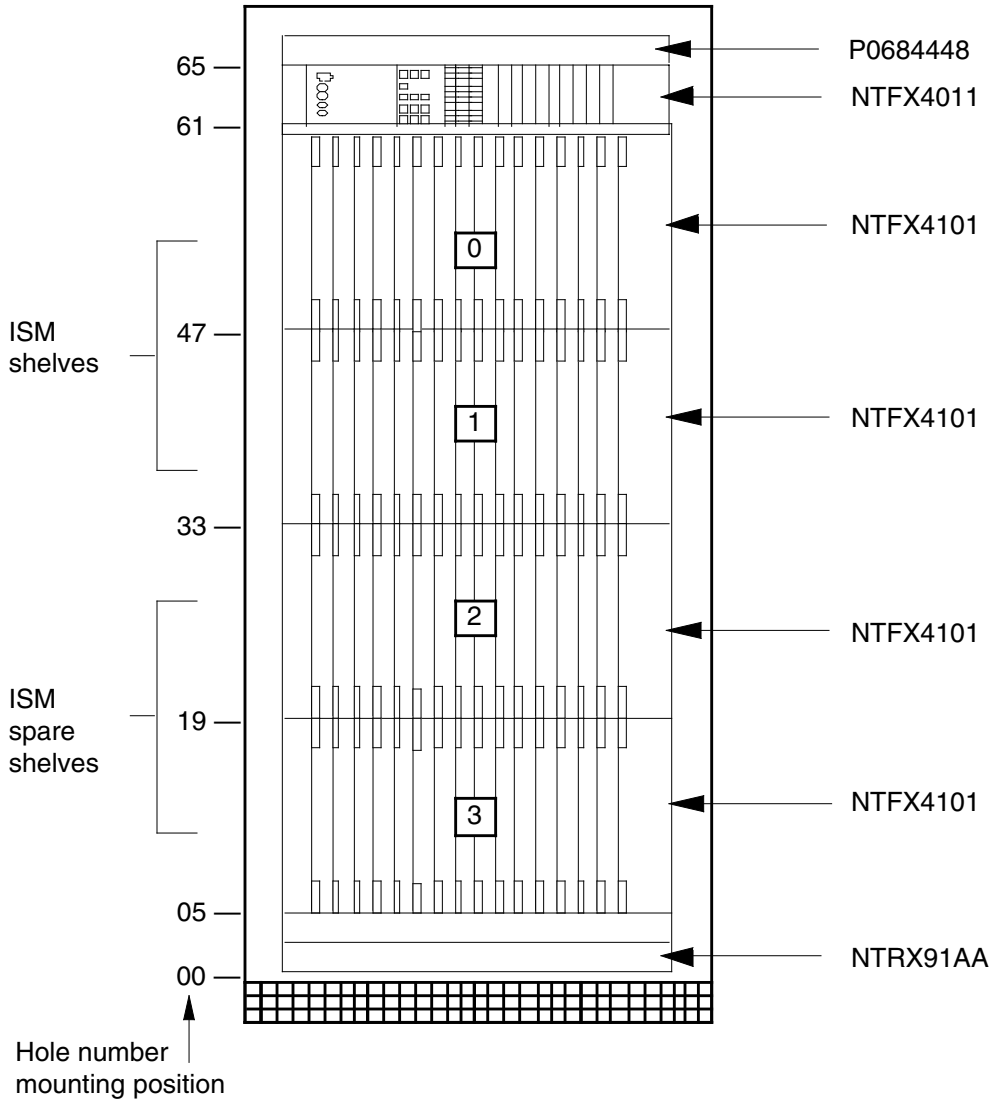
**NTFX40AA CISM with AXU**




**Note:** Front panels appear removed to illustrate NTFX40AA parts. This illustration is not drawn to scale.

# **NTFX40AA** (end)

**NTFX40AA CISM equipped with ISM shelves**




**Note:** Front panels appear removed to illustrate NTFX40AA parts. This illustration is not drawn to scale.

# NTFX40BA

## Description

The integrated services module (ISME) frame contains a maximum of four integrated services modules (ISM). The design is a standard-wired frame with shelves. The top shelf can be provisioned.

For each new office, the first ISME must contain the following units:

- an alarm cross-connect unit (NT3X89CA) mounted in shelf position 53R
- an ISM unit (NTFX4101) mounted in shelf position 39
- additional ISM units (NTFX4101) mounted in shelf positions 21 and 07

The NTFX40BA can be used only with SuperNode.

## Parts

The NTFX40BA contains the following parts:

- NTFX4101—ISM shelf assembly
- NTFX4010—modular supervisory panel (MSP) kit, -48V or -60V (dc)
- NT3X89CA—alarm cross-connect unit (AXU)
- NT6X1402—baffle assembly 101 mm (4 in.)
- P0558295—grille 76 mm (3 in.)
- P0575239—filler panel

### Integrated services module (ISM) shelf assembly

The NTFX4101 shelf assembly contains parts that contain an ISM. The NTFX4101 provides twenty-one slots that connect the following:

- a single-slot ISM processor (NTFX42AA)
- a two-slot ISM DC power converter (NTFX43AA)
- a maximum of 18 service circuits

Of the 18 service circuit slots, the PM service circuits that require power conversion can only use slots 05 to 17. The PM service circuits that do not require power conversion can use slots 03 to 17, for example CTM. One slot (05) is available for one of the non-PM circuit cards in a dual-card device, such as the metallic test unit (MTU).

The NTFX4101 ISM is a single shelf unit that replaces the current trunk module (TM) shelf or the maintenance trunk module (MTM) shelf. The ISM shelf is mounted on the ISME that contains a maximum of four ISM shelves. All shelves can be provisioned.

## **NTFX40BA** (continued)

The ISM shelf connects with the DMS switch in the same method as the current TM and MTM shelves. The ISM processor has a DS-30 link interface with the network. Each plane of the network has a link. The ISM processor has bus connections with service circuit cards that use the back panel. The service circuits determine the P-side interface on the ISM shelf. The ISM can function with TM/MTM mounted on a TME and other PMs in a DMS switch.

### Modular supervisory panel

The NTFX4010 modular supervisory panel (MSP) kit contains power control and alarm circuits. The circuits provide interfaces between the power distribution center and the equipment in the ISME.

The MSP provides a point to monitor the NTFX40BA. The NTFX4010 provides alarms to indicate problems in the NTFX40BA. The MSP includes the following parts:

- a fan-fail and frame-fail indicator
- a fuse-fail alarm output
- front and rear alarm battery supply (ABS) test jacks
- four front-panel services jacks: two telephone pairs (**TEL-A** and **TEL-B**) and two data pairs (**DATA-A** and **DATA-B**)

### Alarm cross-connect unit (AXU)

The alarm cross-connect unit shelf is part of an alarm system for a large office. Each office must have one AXU shelf. The AXU requires a primary alarm integrated service module/maintenance trunk module called an office alarm unit (OAU). The OAU and the backup MTM contain the alarm control circuit cards. The AXU routes any alarm signals. The AXU and the primary alarm maintenance trunk module are a functional pair and must be mounted on the same frame. The primary alarm is in shelf position one. The secondary alarm is in shelf position two.

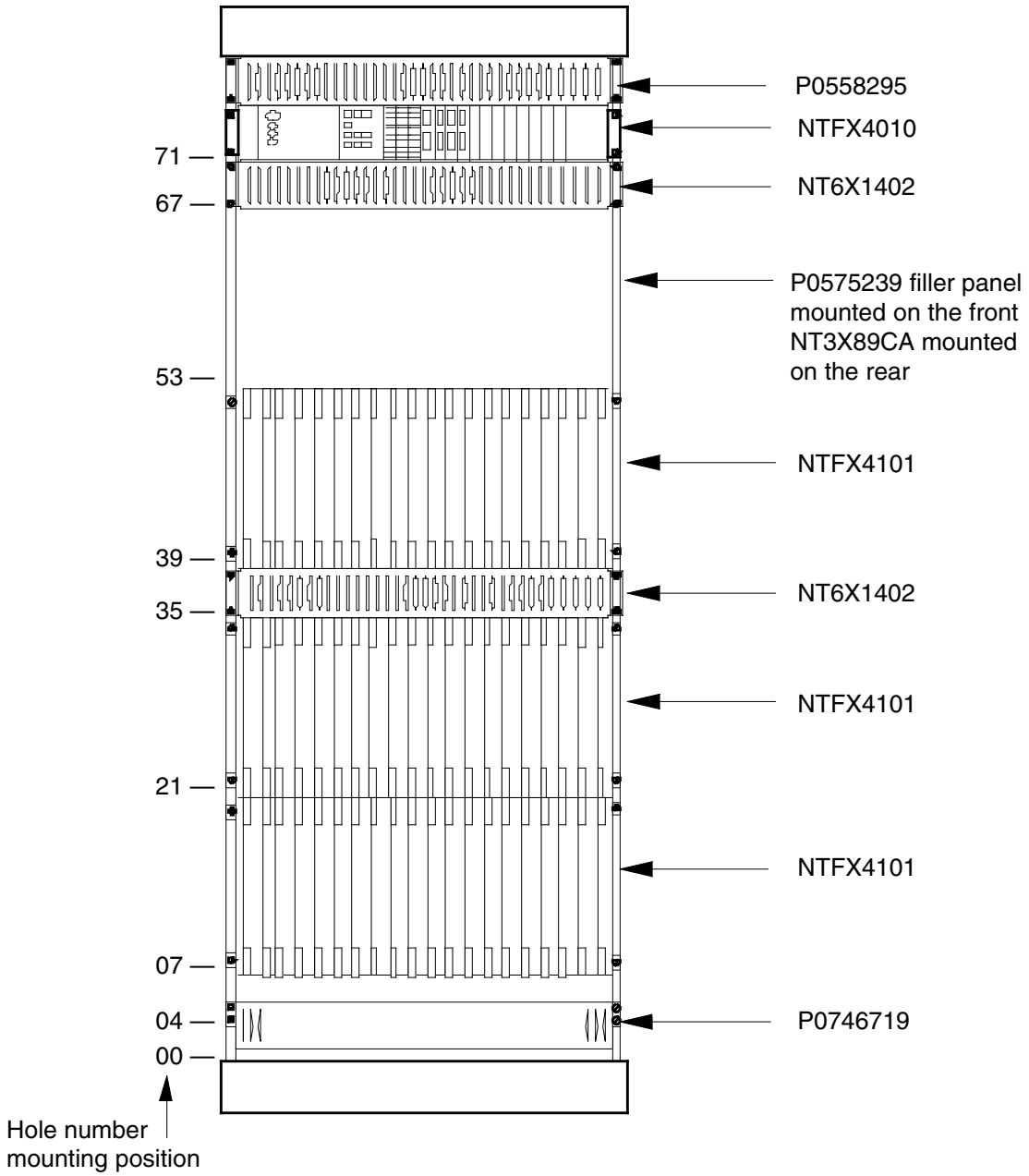
### Filler panels

The P0575239 filler panel conceals a compartment that contains the NT3X89CA AXU. The P0575239 filler panel is at shelf position 53 in the ISME.

## Design

The following figure describes the design of the NTFX40BA.

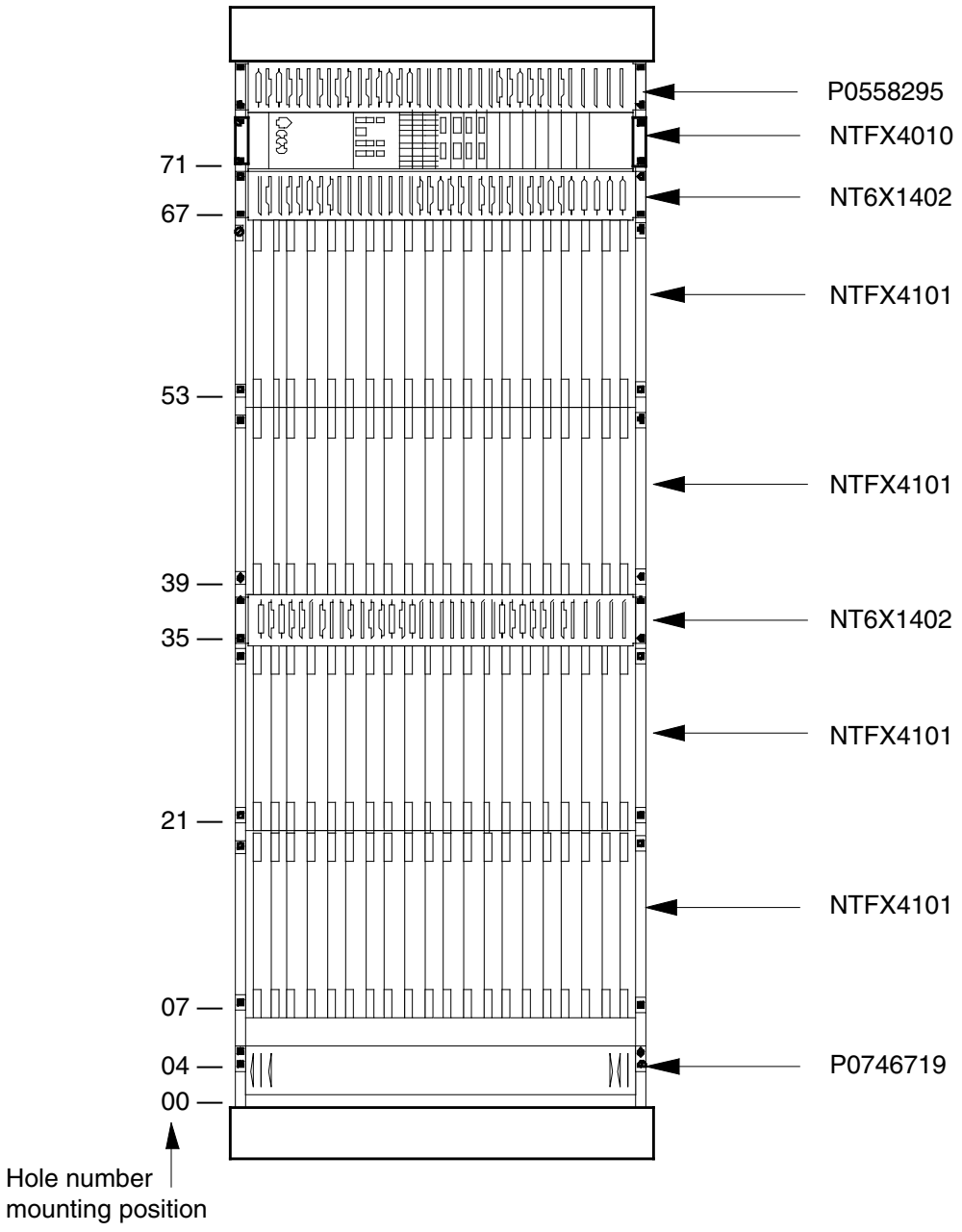
**NTFX40BA ISME with AXU**




**Note:** This illustration is not drawn to scale.

# **NTFX40BA** (end)

**NTFX40BA ISME frame with ISM shelves**




**Note:** This illustration is not drawn to scale.

# NTFX40EA

## Description

The cabinetized metallic test access (CMTA) contains three integrated services modules (ISM). The design is a modular, standard-wired cabinet with shelves.

The CMTA contains the following features:

- wideband test access (WTA) panel (NT7X76BA) in shelf position 47R
- an ISM unit (NTFX4101) cabled for metallic test access (MTA), in shelf position 33
- an ISM unit (NTFX4101) cabled for MTA, in shelf position 19
- an ISM unit (NTFX4101) cabled for multiline test unit (MTU) and monitor-talk, in shelf position 05

All connections to and from the ISM are through a bulkhead for electromagnetic interference (EMI) compliance.

You use the NTFX40EA only with SuperNode.

## Parts

The NTFX40EA contains the following parts:

- NTFX4101—ISM shelf assembly
- NTFX4025—modular supervisory panel (MSP) kit, -48V or -60V (dc)
- NTRX91AA—cooling unit (CU), -48V or -60V (dc)
- NT7X76BA—WTA panel assembly
- P0575239—filler panel for WTA
- P0684448—51 mm (2 in.) filler plate
- P0800296—personality plate for WTA
- P0800297—personality plate for WTA/ISA

### Integrated services module (ISM) shelf assembly

The NTFX4101 shelf assembly contains parts that contain an ISM. The NTFX4101 provides 21 slots that connect the following parts:

- a single-slot ISM processor (NTFX42AA)
- a two-slot ISM DC power converter (NTFX43AA)
- a maximum of 18 service circuits

## **NTFX40EA** (continued)

Two ISM shelves, shelf positions 19 and 33, provide the metallic test access (MTA). Fifteen slots, 06 to 20, accept 15 MTA circuit cards (NT3X09BA). Another ISM shelf, shelf position five, is an metallic test unit (MTU) shelf. A maximum of three dedicated MTUs, NT2X10BB and NT2X11BA circuit cards, are in slot positions 15 to 20. The first MTU is always provided. Dedicated MTUs have a maximum of five Mon-Talk (NT2X90AD) circuit cards in slot positions 8 to 12. The first Mon-Talk circuit card is provided. One rover MTU is in slot positions 13 and 14. The rover MTU has a maximum of 2 Mon-Talk circuit cards in slots six and seven. Slots three, four, and five in each of the ISM shelves are pre-wired for the improved signature accessory (ISA) circuit cards (NTFX45AA). The cabinet has a maximum of nine ISA circuit cards.

### Modular supervisory panel kit

The NTFX4025 modular supervisory panel (MSP) contains power control and alarm circuits. The circuits provide interfaces between the power distribution center and the equipment mounted in the CMTA.

The MSP provides a point to monitor the NTFX40EA. The NTFX4025 provides alarms to indicate problems in the NTFX40EA. The problems can include a cooling unit that does not work or operates in a range that is not correct. The MSP includes a fan-fail and frame-fail indicator, a fuse-fail alarm output, front and rear alarm battery supply (ABS) test jacks. The MSP contains four front-panel services jacks. The four front-panel service jacks are two telephone pairs (**TEL-A** and **TEL-B**) and two data pairs (**DATA-A** and **DATA-B**).

### Cooling unit

The NTRX91AA cooling unit cools the NTFX40EA with forced air. The NRX91AA is a subset of the NTRX92AA cooling unit. The NRX91AA contains an air filter, slider brackets, a fan power/alarm cable, and hardware required to mount the unit.

### Wideband test access (WTA) shelf assembly

The NT7X76BA is a cross-connect panel that provides metallic cross-connectability to test DMS wideband subscriber services. Wideband subscriber services include ISDN, Datapath, and voice frequency DMS-100 subscriber services. You use the NT7X76BA WTA panel for the dedicated multiline test unit (MTU) function. A maximum of five dedicated MTUs can connect to each NT7X76BA panel.

The WTA panel replaces the use of the main distributing frame (MDF) to metallic cross-connect the test circuits such as the MTU. The test circuits of the MTU include metallic test access and line equipment in DMS offices. The

current MDF cabling cannot support a test of new subscriber services. Excessive switching office cabling causes transmission impairment.

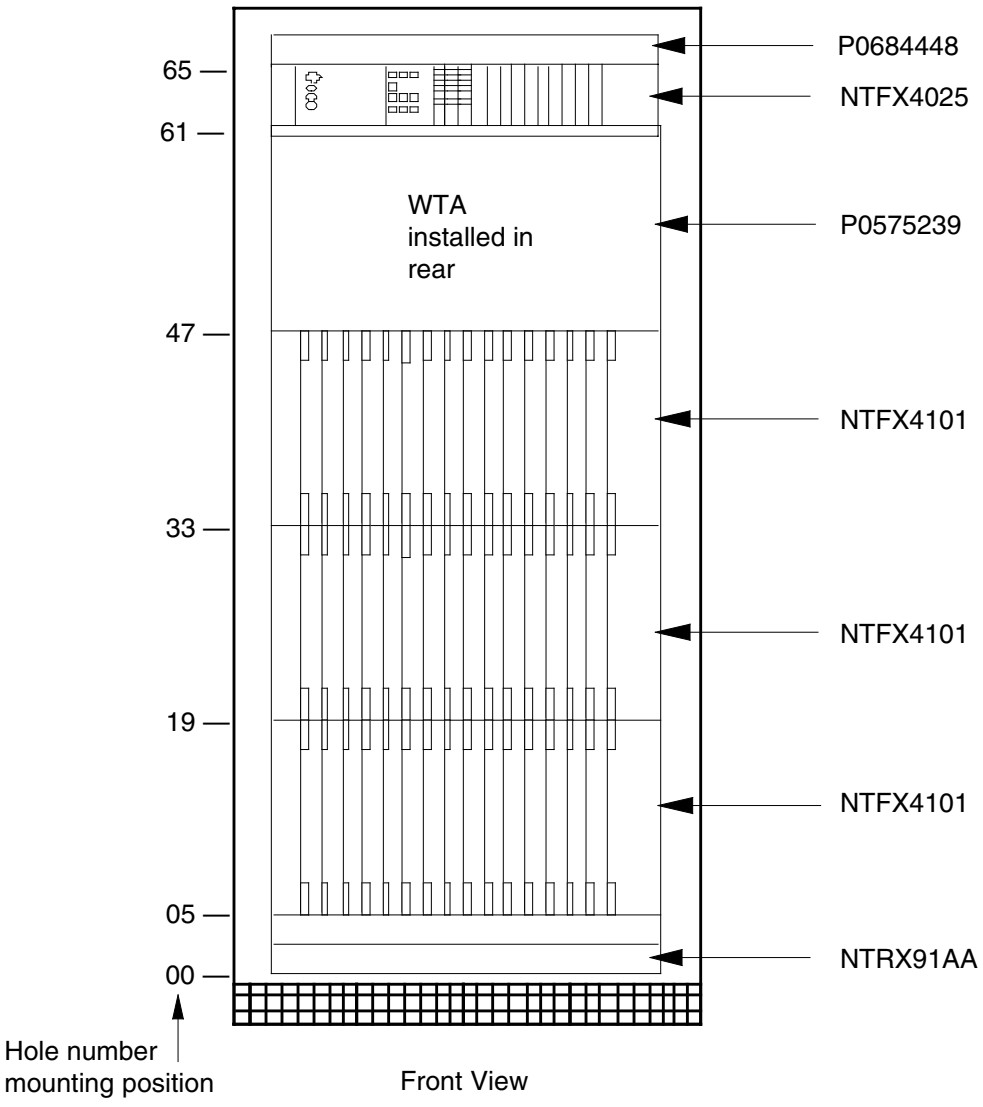
Each WTA panel supports a metallic test access matrix with a maximum of 24 horizontal (in multiples of eight) appearances. The metallic test access matrix has a maximum of 80 vertical (in multiples of eight) appearances. Each NT3X09BA MTA card contains a relay matrix with eight horizontal and eight vertical appearances. Each WTA supports a matrix of three rows of MTAs for horizontals with 10 MTAs for verticals, for a total 30 MTAs.

## Design

The design of the NTFX40EA appears in the following figure.

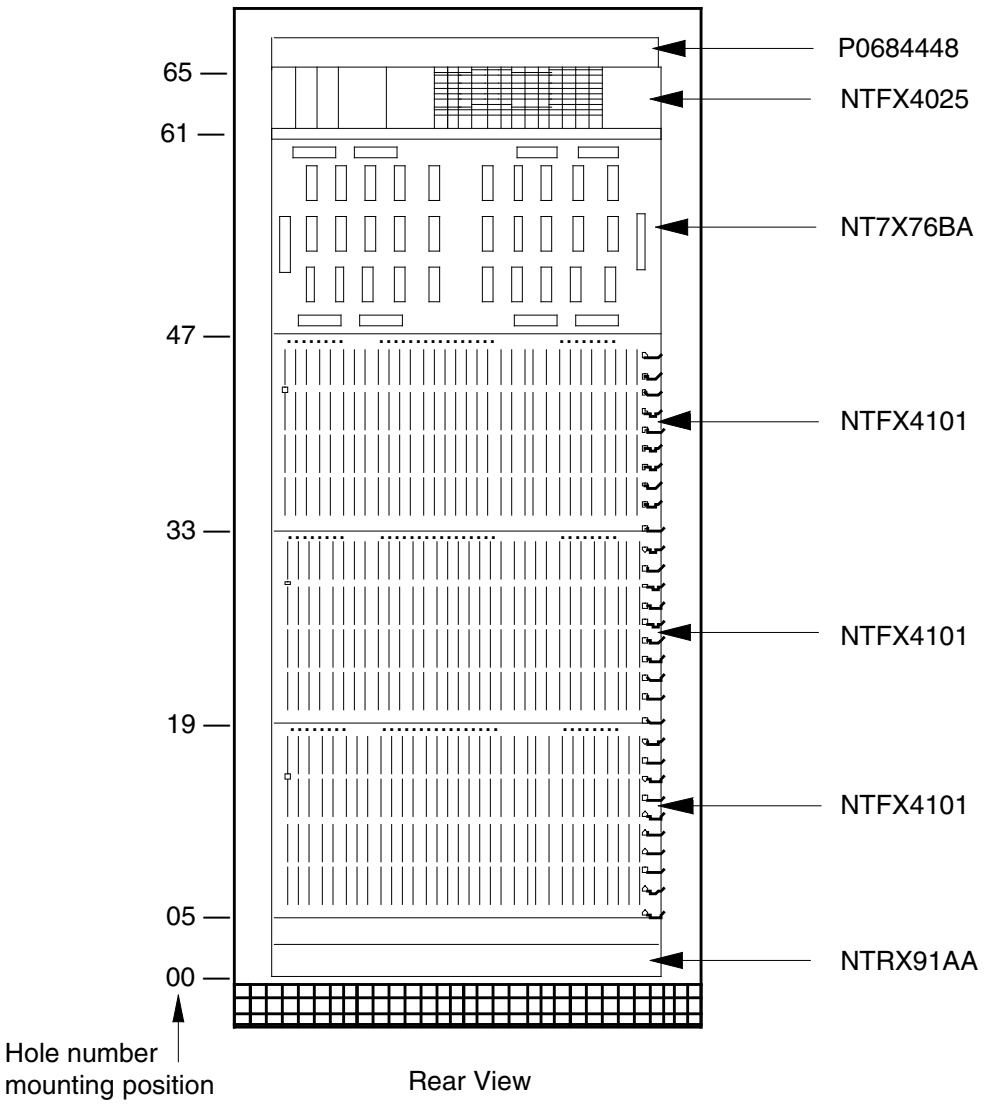
## **NTFX40EA** (continued)

**NTFX40EA CMTA front view**




**Note:** Front panels are shown removed to illustrate NTFX40EA components. This illustration is not drawn to scale.

**NTFX40EA CMTA rear view**




**Note:** This illustration is not drawn to scale.

# NTFX40FA

## Description

The metallic test access equipment (MTAE) design standardizes the DMS SuperNode metallic test access equipment, testheads, and cross-connections. The MTAE standardizes these parts for a maximum of 25 600 lines.

The metallic test access equipment (MTAE) frame contains a wideband test access (WTA) panel and three integrated services module (ISM) shelves. The design is a standard-wired frame with shelves.

The MTAE contains the following parts:

- wideband test access (WTA) panel (NT7X76BA) mounted in shelf position 53R
- an ISM unit (NTFX4101) cabled for metallic test access (MTA), mounted in shelf position 39
- an ISM unit (NTFX4101) cabled for MTA, mounted in shelf position 21
- an ISM unit (NTFX4101) cabled for multi-line test unit (MTU) and monitor-talk, mounted in shelf position seven

## Parts

The NTFX40FA contains the following parts:

- NTFX4101—ISM shelf assembly
- NTFX4026—modular supervisory panel (MSP) kit, -48V or -60V (dc)
- NT6X1402—baffle assembly 101 mm (9 in.)
- NT7X76BA—WTA panel assembly
- P0558295—grille 76 mm (3 in.)
- P0575239—filler panel for WTA

### Integrated services module (ISM) shelf assembly

The NTFX4101 shelf assembly contains parts that contain an ISM. The NTFX4101 provides 21 slots that connect the following parts:

- a single-slot ISM processor (NTFX42AA)
- a two-slot ISM DC power converter (NTFX43AA)
- a maximum of 18 service circuits

Two ISM shelves, shelf positions 21 and 39, provide the metallic test access (MTA). Fifteen slots, six to 20, accept 15 MTA circuit cards (NT3X09BA). The ISM shelf in position seven is an metallic test unit (MTU) shelf. A

maximum of three dedicated MTUs, NT2X10BB and NT2X11BA circuit cards, are in slot positions 15 to 20. The first MTU is provided. A maximum of five Mon-Talk (NT2X90AD) circuit cards are for dedicated MTUs in slot positions eight to 12. The first Mon-Talk circuit card is provided. One rover MTU is placed in slot positions 13 and 14. A maximum of two Mon-Talk circuit cards are for the rover MTU in slots six and seven. Slots three, four, and five in each of the ISM shelves are pre-wired for the improved signature accessory (ISA) circuit cards (NTFX45AA). The frame can have a maximum of nine ISA circuit cards.

### Modular supervisory panel kit

The NTFX4026 modular supervisory panel (MSP) kit contains the NTRX40AA power control and alarm circuits. The circuits provide interfaces between the power distribution center and the equipment mounted in the MTAE.

The MSP provides a point to monitor the NTFX40FA. The NTFX4026 kit provides alarms to indicate problems in the NTFX40FA. The MSP includes a fan-fail and frame-fail indicator, a fuse-fail alarm output, and front and rear alarm battery supply (ABS) test jacks. The MSP includes four front-panel services jacks. The four front-panel service jacks are two telephone pairs (**TEL-A**and **TEL-B**) and two data pairs (**DATA-A** and **DATA-B**).

### Wideband test access (WTA) shelf assembly

The NT7X76BA is a cross-connect panel that provides metallic cross-connect ability to test DMS wideband subscriber services. The DMS widband subscriber services include ISDN, Datapath, and voice frequency DMS-100 subscriber services. The NT7X76BA WTA panel is for the dedicated multiline test unit (MTU) function. A maximum of five dedicated MTUs connect to the NT7X76BA panel.

Each WTA panel supports a metallic test access matrix with a maximum of 24 horizontal (in multiples of eight) appearances. Each WTA panel supports a metallic test access matrix with a maximum of 80 vertical (in multiples of eight) appearances. Each NT3X09BA MTA card contains a relay matrix with eight horizontal and eight vertical appearances. Each WTA supports a matrix of three rows of MTAs for horizontals with 10 columns of MTAs for verticals. A total of 30 MTAs are present.

### Filler panels

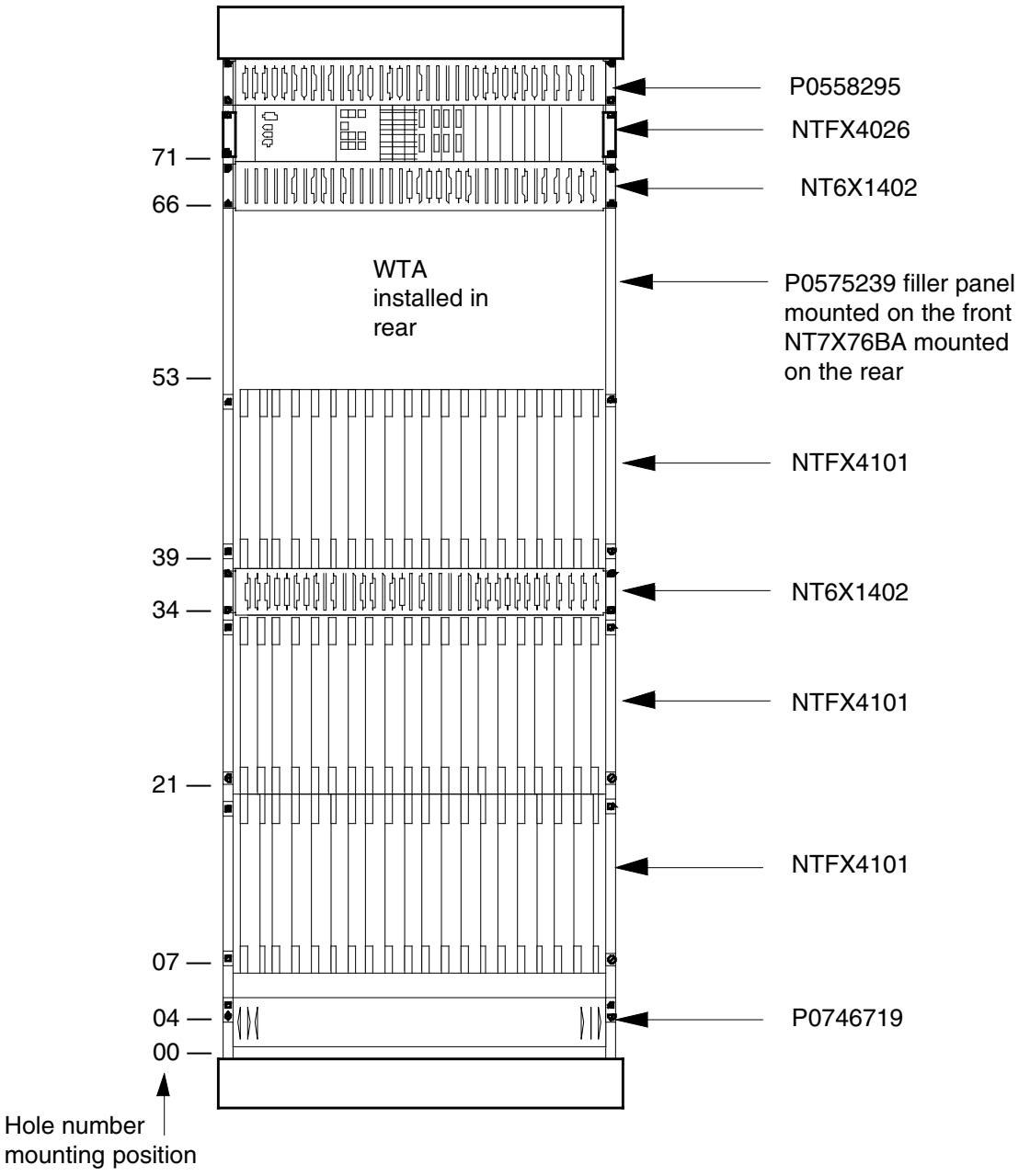
The P0575239 filler panel conceals a compartment that contains the NT7X76BA WTA. The P0575239 filler panel is at shelf position 53 in the MTAE.

## **NTFX40FA** (continued)

## Design

The following figure describes the design of the NTFX40FA.

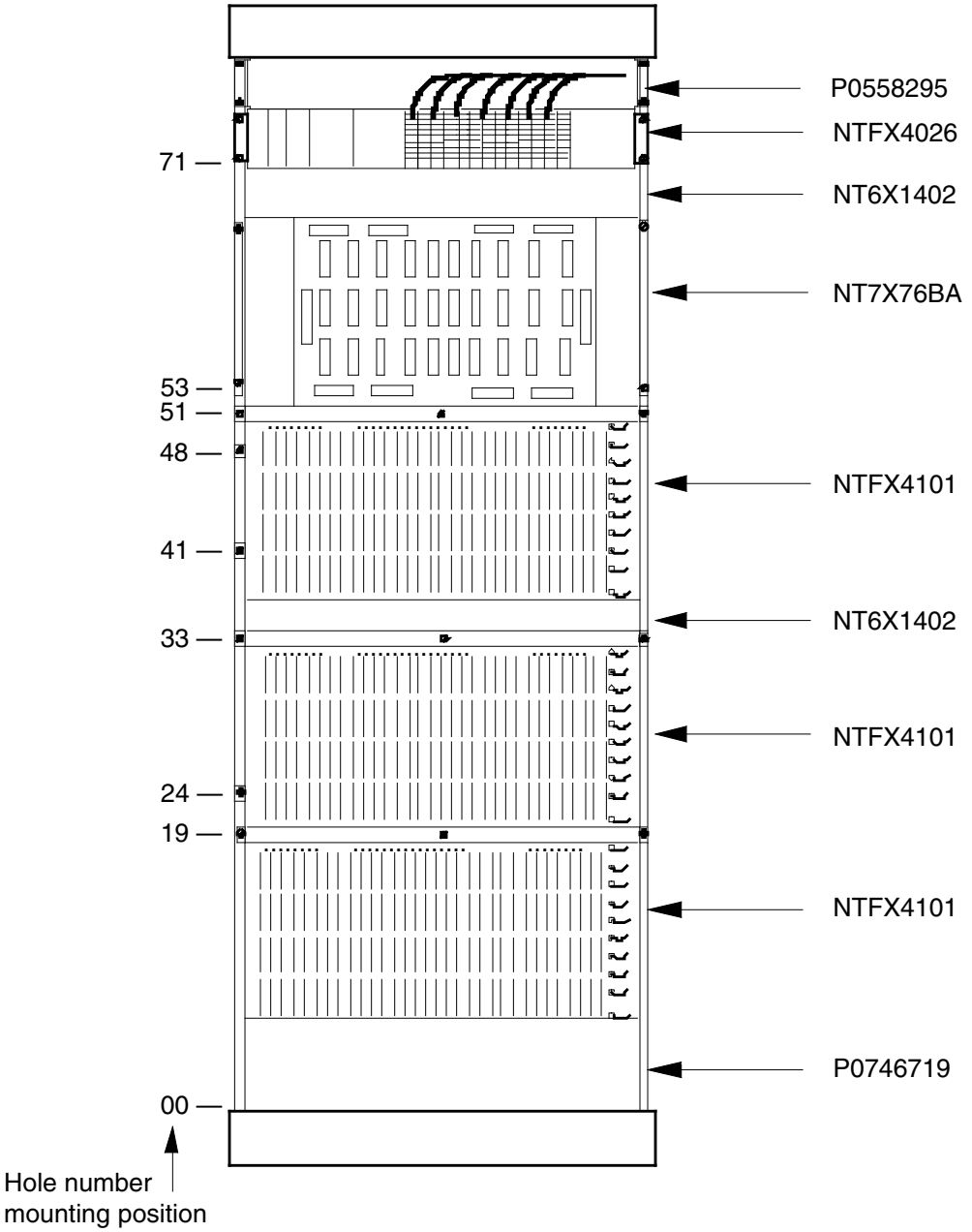
**NTFX40FA MTAE front view**




**Note:** This illustration is not drawn to scale.

# **NTFX40FA** (end)

**NTFX40FA MTAE rear view**




**Note:** This illustration is not drawn to scale.

# NTFX4101

## Product description

The integrated services module (ISM) (NTFX4101) is a single shelf unit. The ISM replaces the current trunk module (TM) shelf or the maintenance trunk module (MTM) shelf. The ISM shelf attaches to one of the following parts:

- cabinetized ISM (CISM)
- frame ISM (ISME)
- cabinetized metallic test access (CMTA)
- metallic test access equipment (MTAE)

The above circuit cards are not required if the ISM shelf operates only for conference trunk module (CTM) applications.

The peripheral module (PM) service circuits that require power conversion use slots five to 17. The PM service circuits that do not require power conversion can use slots 3 to 17. Slot five is available for one of the non-PM circuit cards in a dual-card device. An example of this device is the metallic test unit (MTU).

The ISM shelf connects with the Digital Multiplex System (DMS) in the same method as the current TM and MTM shelves. The ISM processor has a DS-30 link interface with the network and BUS connections with service circuit cards. The service circuit cards use the back panel. Each plane of the network has a link. The service circuits determine the peripheral-side (P-side) interface on the ISM shelf. The ISM can operate with TM/MTM and other PMs in a DMS switch. The TM/MTM is in another frame or cabinet.

The ISM shelf can have adjacent circuit packs that work together. The main card is on the right and the companion card is on the left. This configuration is the opposite for the configuration in the TM/MTM. The ISM contains service circuit cards that operate in pairs.

## Components

The ISM shelf contains the following parts:

- ISM DC converter (NTFX43AA)
- ISM processor (NTFX42AA)
- Filler face plate or panel (NT0X50AC)
- maximum of 18 slots for provisionable service circuit cards

## **NTFX4101** (continued)

The NTFX43AA circuit card provides regulated and protected power supplies required by the ISM shelf from an input battery feed. The converted voltages are +5V, +12V, +25V and -15V (dc).

The NTFX42AA circuit card designed to be compatible with the existing TM/MTM service circuit cards. The NTFX42AA circuit card provides a joined functionality of the NT0X70, NT2X53, NT2X59 and NT3X45 circuit cards.

### Service circuit cards

The table that follows shows a list of available circuit cards and the slots used in the ISM shelf.

**NTFX4101 parts (Sheet 1 of 5)**

| PEC | Slot | Description |
|---|---|---|
| NT0X10AA | 6F-20F | *Miscellaneous scanner* |
| NT0X50AC | 3F-20F | *Filler face plate*<br>The filler face plate or panel occupies empty card slots in the shelves. |
| NT0X50AG | 1F | *Filler face plate*<br>The filler face plate or panel occupies empty card slots in the shelves. This filler is used if the ISM DC converter (NTFX43AA) is not provided. |
| NT1X00AA, -AB | 6F-20F | *102 test tone circuit card* |
| NT1X00AC, -AD | 6F-20F | *ROH tone circuit card* |
| NT1X00AE | 6F-20F | *ROH tone international 102 test trunk circuit card* |
| NT1X00AF | 6F-20F | *ROH tone 102/10 dB test trunk circuit card* |
| NT1X00AG | 6F-20F | *ROH tone 102/20 dB test trunk circuit card* |
| NT1X00AH | 6F-20F | *ROH tone 102/15 dB test trunk circuit card* |
| NT1X00KA | 6F-20F | *102 test trunk (China) circuit card* |
| NT1X54AA | 6F-20F | *Jack ended trunk* |
| NT1X80AA | 5F-17F | *Enhanced digital recorded announcement machine (EDRAM) circuit card* |

***Note:*** * = even numbered slots. ** = odd numbered slots.

**NTFX4101 parts (Sheet 2 of 5)**

| PEC | Slot | Description |
|---|---|---|
| NT1X81AA | 3F-17F | *Conference trunk module (CTM) circuit card* |
| NT1X90AA | 8F-20F* | *Test signal generator* |
| NT1X90BA | 8F-20F* | *Test signal generator A-Law* |
| NT2X01AA | 7F-19F | *Automatic identification of outward dialing (AIOD)* |
| NT2X10BB | 5F-19F** | *Multi-line test unit* |
| NT2X11BA | 6F-20F* | *Multi-line test unit* |
| NT2X47AD | 6F-20F* | *TTU control processor* |
| NT2X47BA | 6F-20F* | *Trans test controller (A-Law)* |
| NT2X48AA, -AB | 7F-20F | *Digital 4-channel MF receiver* |
| NT2X48BA | 7F-20F | *Digital 4-channel MF receiver* |
| NT2X48BB | 7F-20F | *Digital 4-channel DTMF receiver* |
| NT2X48CA | 7F-20F | *Digital MF receiver A-Law* |
| NT2X48CB | 7F-20F | *DTMF receiver (BT)* |
| NT2X48CC | 7F-19F | *DTMF receiver A-Law* |
| NT2X56AB | 5F-19F** | *Trans test mod digital filter* |
| NT2X56BA | 5F-19F** | *Trans test filter (A-Law)* |
| NT2X57AA | 6F-20F | *SD circuit card* |
| NT2X57AB | 6F-20F | *SD circuit card with OAU monitor* |
| NT2X65AA | 6F-20F | *CAMA pos sign trunk* |
| NT2X66AA | 6F-20F | *CAMA CW susp LP trunk* |
| NT2X71AA | 6F-20F | *Transmission termination trunk* |
| NT2X71AB | 6F-20F | *Term trans flash test trunk* |
| NT2X72AA | 6F-20F | *4W E type D1 600 interface* |

***Note:*** * = even numbered slots. ** = odd numbered slots.

## **NTFX4101** (continued)

**NTFX4101 parts (Sheet 3 of 5)**

| PEC | Slot | Description |
|---|---|---|
| NT2X72AB | 6F-20F | *4W E type D1 600 E supr cont* |
| NT2X72AC | 6F-20F | *4W E 600 L GN E supr cont* |
| NT2X72BA | 6F-20F | *4W DC5A tie trunk* |
| NT2X72BB | 6F-20F | *4W CAIA 600-ohm trunk* |
| NT2X75AA | 6F-20F | *Loop around test line* |
| NT2X77AA, -AC | 6F-20F | *Comp bal network 900 ohm* |
| NT2X77AB, -AD | 6F-20F | *Comp bal network 600 ohm* |
| NT2X78AA | 6F-20F | *4W incoming/outgoing (2600 Hz) MF/DP* |
| NT2X80AA | 6F-20F | *Precision balanced network H88* |
| NT2X81AA | 6F-20F | *2W E 900 two way incoming/outgoing MF/DP* |
| NT2X81AB | 6F-20F | *2W E 600 two way incoming/outgoing MF/DP* |
| NT2X81BA | 6F-20F | *2W DC5A tie trunk* |
| NT2X82AA | 6F-20F | *2W LP 900 incoming reversal battery MF/DP* |
| NT2X83AA | 6F-20F | *2W LP 900 outgoing reversal battery MF/DP* |
| NT2X84BA | 6F-20F | *Earth calling trunk* |
| NT2X85AA | 6F-20F | *RCDG complete trunk H-L coin* |
| NT2X86AA | 6F-20F | *Toll switch 3rd w/coin FX ring* |
| NT2X88AA | 6F-20F | *4W incoming/outgoing 600 E MF/DP* |
| NT2X90AD | 6F-20F | *Incoming/outgoing test trunk* |
| NT2X92AA | 6F-20F | *2W LP 900 outgoing reverse battery MF* |
| NT2X95AA | 6F-20F | *2-way PBX trunk DID/DOD* |
| NT2X95BA | 6F-20F | *Direct dial inward trunk* |
| NT2X95BB | 6F-20F | *2W JUSMAG 600 ohm DDO trunk* |

***Note:*** * = even numbered slots. ** = odd numbered slots.

**NTFX4101 parts (Sheet 4 of 5)**

| PEC | Slot | Description |
|---|---|---|
| NT2X96AA | 7F-19F** | *PCM level meter TTT* |
| NT2X96BA | 7F-19F** | *PCM level meter (A-Law) TTT* |
| NT2X98AA | 6F-20F | *2W incoming 900 DP RB slave control* |
| NT3X02BA | 8F-20F* | *Dial up auto/TOPS control processor* |
| NT3X03AA | 7F-19F** | *TOPS digital signal processor* |
| NT3X04AA | 6F-20F | *Incoming test from AECO LTD* |
| NT3X06AA | 6F-20F | *2W outgoing trunk to AE/3CL CO-LO* |
| NT3X07AA | 6F-20F | *2W incoming trunk to AE/3CL CO-LO* |
| NT3X08AB | 6F-20F | *Coin detection circuit* |
| NT3X09BA | 6F-20F | *8x8 metallic test access circuit card* |
| NT3X68AA | 6F-20F | *Pre-empt, permanent signal, and conference tone generator circuit card* |
| NT3X68AB | 6F-20F | *Dual-tone multifrequency generator circuit card* |
| NT3X68AC | 6F-20F | *Call waiting tone generator circuit card* |
| NT3X82AF | 6F-20F | *OAS dead system w/unique AUD* |
| NT3X82AH | 6F-20F | *OAS dead system w/common AUD* |
| NT3X82AJ | 6F-20F | *OAS dead system w/common AUD* |
| NT3X82AK | 6F-20F | *OAS dead system w/common AUD, 60 V* |
| NT3X83AC | 6F-20F | *OAS alarm transfer* |
| NT3X83AD | 6F-20F | *OAS alarm transfer, 60 V* |
| NT3X84AB | 6F-20F | *OAS alarm sending* |
| NT3X85AB | 6F-20F | *OAS alarm grouping* |
| NT3X91AA | 6F-20F | *Remote office test line interface trunk* |
| NT4X23AA | 6F-20F | *DTU BERT unit circuit card* |

***Note:*** * = even numbered slots. ** = odd numbered slots.

## **NTFX4101** (continued)

**NTFX4101 parts (Sheet 5 of 5)**

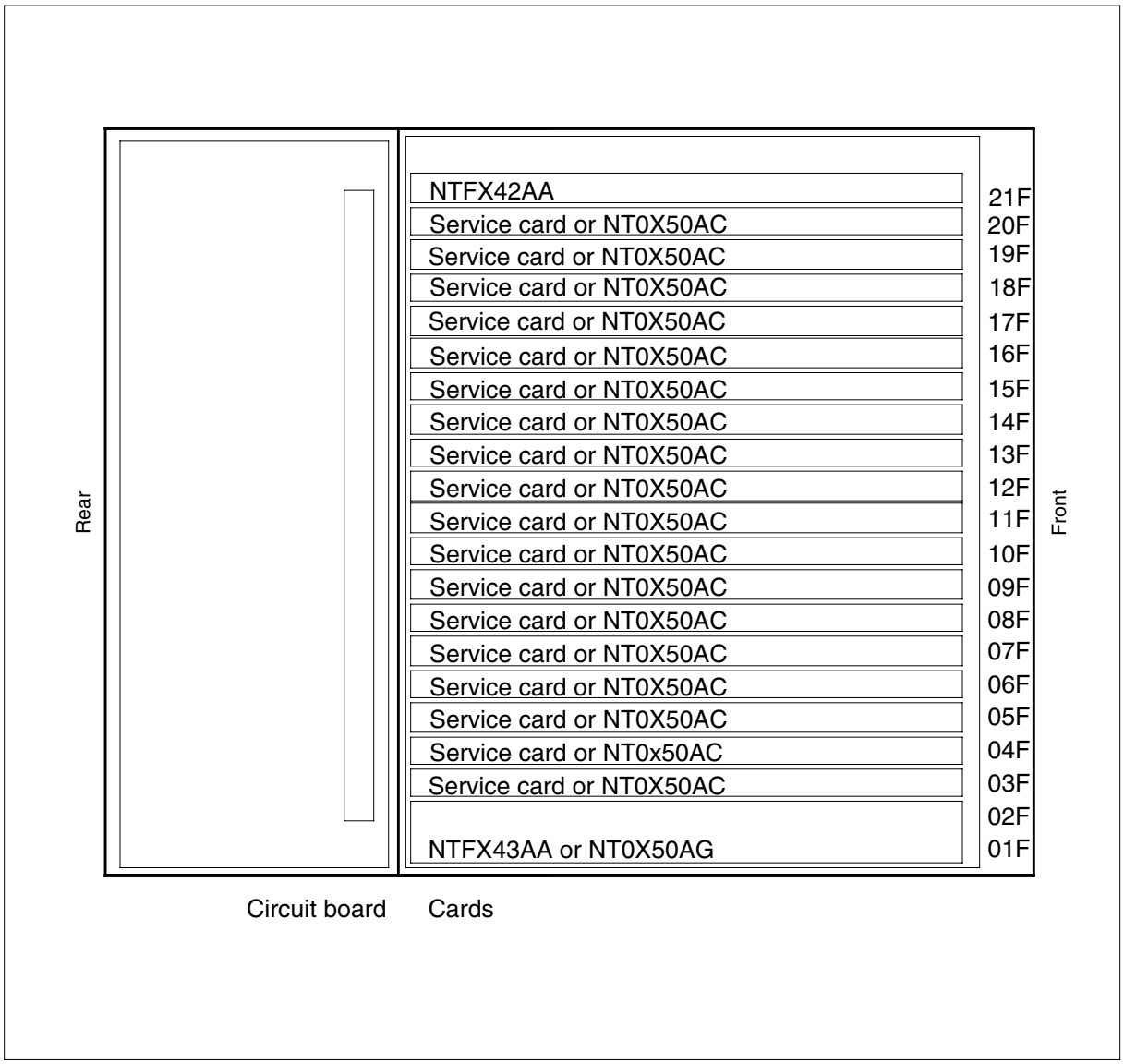
| PEC | Slot | Description |
|---|---|---|
| NT4X45AA | 7F-20F | *EDTU circuit card* |
| NT4X97AA | 6F-20F* | *MTU controller* |
| NT4X98BC | 5F-19F** | *MTU international analog* |
| NT5X03AA | 6F-20F | *CCITT R1 trunk 101 rest line DMS-306-20* |
| NT5X04AA, -AB | 6F-20F | *CCITT #5 trunk* |
| NT5X06AA | 6F-20F | *CCITT #6 trunk* |
| NT5X25AA | 6F-20F | *1 way CO trunk outgoing GRD ST or incoming LP* |
| NT5X29AA | 20F | *CCIS continuity checker* |
| NT5X29AC | 20F | *Audio answer detection digitone multi-frequency* |
| NT5X29BA | 20F | *A-Law ATD tone generator* |
| NT5X30AA | 6F-20F | *101 common test line* |
| NT5X30BA | 6F-20F | *101 common test line (UK)* |
| NTFX42AA | 21F | *ISM processor circuit card*<br>The ISM processor circuit card is to work with the current trunk module/maintenance module (TM/MTM) service circuit cards. The ISM processor circuit card provides a joined functionality of the NT0X70, NT3X45, NT2X53, and NT2X59 controller cards. |
| NTFX43AA | 1F | *ISM DC converter*<br>The ISM DC converter card provides regulated and protected power supplies required by the ISM shelf from an input battery feed. The converted voltages are +5 V, +12 V, +25 V, and -15 V (dc). |
| NTFX44AA | 6F-11/16F | *Improved loop test accessory card* |
| NTFX45AA | 3-5F | |
| NTFX45AA | 3-5F | *Improved signature accessory card* |
| NTFX45AA | 3-5F | |

***Note:*** * = even numbered slots. ** = odd numbered slots.

## Layout

The figure that follows shows the layout of the NTFX4101 shelf, showing slot positions and service card numbering.

**NTFX4101 parts**



# NTFX42AA

## Product description

The integrated services module (ISM) processor (NTFX42AA) circuit card is compatible with the current trunk module/maintenance trunk module (TM/MTM) service circuit cards. This card provides the combined functions of the NT0X70, NT2X45, NT2X53 and NT2X59 controller cards.

The NTFX42AA occupies a single slot. The NTFX42AA is available in slot 21 of the ISM shelf or NTFX41AA. The system provides the card for service circuits, that are not the PM type, are allocated in the ISM shelf.

## Functional description

The ISM processor has two separate sections. The first section is a digital logic section that contains the following:

- a standard N14B 8085 microprocessor or compatible processor
- an associated PROM and RAM
- an MTM controller application-specific integrated circuit (ASIC)
- tone PROM
- different transistor transistor logic/complementary metal-oxide semiconductor (TTL/CMOS) glue logic/buffers

The second section is an analog section that includes the following:

- analog switches
- digital-to-analog converters
- op-amps
- voltage comparators
- current/voltage references for installation of digital-to-analog and analog-to-digital conversions for 32 channels

### Functional blocks

The NTFX42AA contains of the following functional blocks:

- processor
- memory and buffers
- the MTM controller ASIC (I17BF)
- the DS-30 port interface
- the NT2X59 analog functions
- trunk interface

- supply voltage supervisor circuit
- the DS-30 interface

### Processor (N14B)

This block contains the 8085 microprocessor or an N14 ASIC that emulates the 8085 microprocessor.

### Memory and buffers

This block is the for ISM firmware store. This functional block contains the following:

- 8 kbyte of a 32 kbyte PROM
- an ISM PM load and data store held in a 32 kbyte RAM
- all the current TM/MTM tone sets held in a 128 kbyte tone PROM

The buffers provide the interface between the microprocessor and the memory devices and the I17BF ASIC.

### The MTM controller ASIC

This block includes the main part of the digital logic circuits. These circuits associate with the TM/MTM controller functions that are used in the ASIC. The current TM/MTM uses the analog phase-locked loops (PLL). The ASIC contains digital phase locked loops. These loops replace the analog PLLs. Additional features include the ability to select y-law or A-law pulse code modulation (PCM) format or a targeted tone set. Central control (CC) regulates these features.

### The DS-30 port interface

This block describes a single DS-30 link of dual network planes. The network carries both message and PCM data to and from the network. The electrical interface consists of an NT5L67AA hybrid and differential receiver plus glue logic. For both planes, the system sends the received serial data streams from the Network to the I17BF ASIC for further processing. The system sends the two outgoing serial data streams from I17BF ASIC. The system buffers and passes the streams through the hybrid to the network.

### The NT2X59 analog functions

This block combines analog circuits that for all versions of the NT2X59 circuit cards. The I17BF ASIC controls the block. This block provides a shared 32-channel coder-decoder (CODEC) for 30 trunks. The decoder can use the u-law or the A-law format. The CODEC performs the coding functions. These functions include analog-to-digital conversion of the input analog or voice

## **NTFX42AA** (continued)

signal. The CODEC also performs decoding functions. These functions include digital-to-analog conversion of the received digital input.

The additional feature enables either the u-law or A-law PCM format, while the system disables the other format.

### Trunk interface

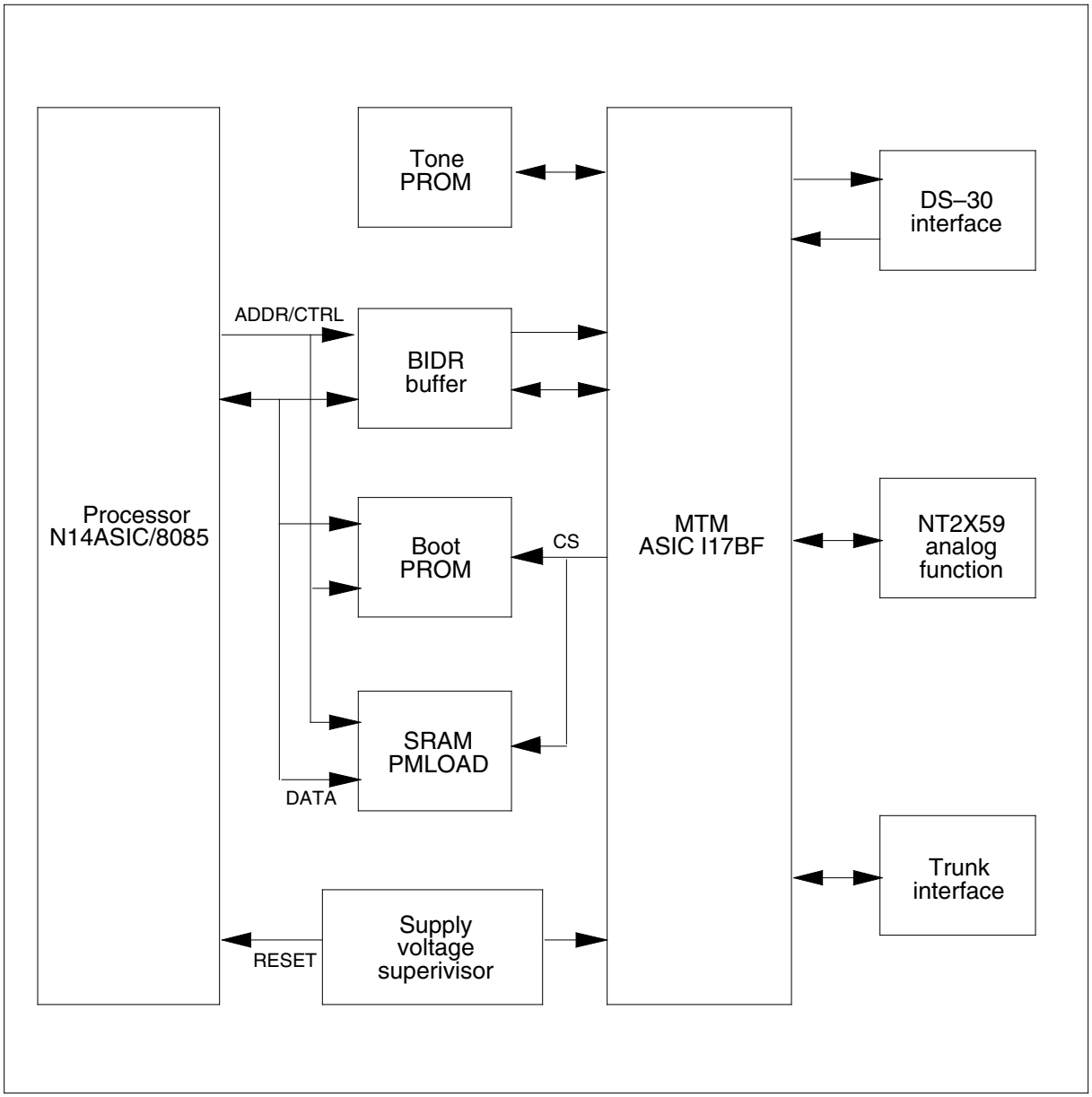
This block describes a common trunk interface that communicates with the trunks/service circuits. The system distributes the signals associated with this interface to the ISM shelf backplane to the 15 trunk card slots on the ISM shelf.

### Supply voltage supervisor circuit

This block is a circuit that generates a reset pulse. The circuit sends the pulse to the microprocessor (8085 or N14 ASIC) and the I17BF ASIC. This action occurs on power-up from the supply voltage dip.

The following figure indicates the relationship between the functional blocks.

**NTFX42AA simplified block diagram**



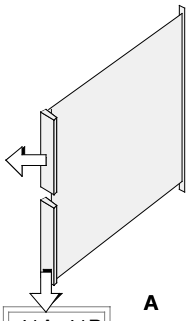

## Signaling

### Pin numbers

The following figure indicates the pin numbers for the NTFX42AA

# **NTFX42AA** (continued)

### NTFX42AA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | | |
| 3A 3B | | |
| 4A 4B | | |
| 5A 5B | P0RECF | |
| 6A 6B | P0RECT | |
| 7A 7B | P0SENDF | |
| 8A 8B | P0SENDT | |
| 9A 9B | | |
| 10A 10B | GND | GND |
| 11A 11B | | |
| 12A 12B | | |
| 13A 13B | | |
| 14A 14B | | |
| 15A 15B | | |
| 16A 16B | | TC00 |
| 17A 17B | | TC16 |
| 18A 18B | | |
| 19A 19B | | |
| 20A 20B | GND | GND |
| 21A 21B | | |
| 22A 22B | | |
| 23A 23B | | |
| 24A 24B | P1RECF | |
| 25A 25B | P1RECT | |
| 26A 26B | P1SENDF | |
| 27A 27B | P1SENDT | |
| 28A 28B | | |
| 29A 29B | | |
| 30A 30B | GND | GND |
| 31A 31B | | |
| 32A 32B | | |
| 33A 33B | | |
| 34A 34B | | |
| 35A 35B | | |
| 36A 36B | | |
| 37A 37B | | |
| 38A 38B | GND | GND |
| 39A 39B | SYNC390 | SYNC390 |
| 40A 40B | GND | GND |

| | A | B |
|---|---|---|
| 41A 41B | GND | GND |
| 42A 42B | GND | GND |
| 43A 43B | GND | GND |
| 44A 44B | R PAM P | |
| 45A 45B | R PAM N | |
| 46A 46B | GND | GND |
| 47A 47B | GND | GND |
| 48A 48B | X PAM P | |
| 49A 49B | X PAM N | |
| 50A 50B | GND | GND |
| 51A 51B | SYNC32K | |
| 52A 52B | –TE29 | –TE30 |
| 53A 53B | –TE27 | –TE28 |
| 54A 54B | –TE25 | –TE26 |
| 55A 55B | –TE23 | –TE24 |
| 56A 56B | –TE21 | –TE22 |
| 57A 57B | –TE19 | –TE20 |
| 58A 58B | –TE17 | –TE18 |
| 59A 59B | –TE15 | –TE16 |
| 60A 60B | –TE13 | –TE14 |
| 61A 61B | –TE11 | –TE12 |
| 62A 62B | –TE09 | –TE10 |
| 63A 63B | –TE07 | –TE08 |
| 64A 64B | –TE05 | –TE06 |
| 65A 65B | –TE03 | –TE04 |
| 66A 66B | –TE01 | –TE02 |
| 67A 67B | TYP | TYN |
| 68A 68B | –RDAT | |
| 69A 69B | –BUSC | |
| 70A 70B | GND | GND |
| 71A 71B | –XDAT | ANUL |
| 72A 72B | | |
| 73A 73B | | |
| 74A 74B | –15V | –15V |
| 75A 75B | | |
| 76A 76B | +12V | +12V |
| 77A 77B | | |
| 78A 78B | +5V | +5V |
| 79A 79B | +5V | +5V |
| 80A 80B | PAMG | PAMG |

# Technical data

## Power requirements

The following table indicates the power requirements for the NTFX42AA

**Power requirements**

| Voltage | Current |
|---|---|
| +5V nominal | 0.32 A |
| +4.75V minimum | |
| +5.25V maximum | |
| +12V nominal | 0.16 A |
| -15V nominal | 0.11 A |

# NTFX43AA

## Description

The NTFX43AA is an integrated services module (ISM) DC converter card. The card regulates and protects the power supplies. The ISM shelf requires this card for the input feed.

The card provides +5V, +12V, +25V and -15V dc voltages. The NTFX43AA card occupies two slot positions. The NTFX43AA card occupies two slot positions. On ISM shelf NTFX41AA, slots 01 and 02 are available for this card.

## Functional description

The NTFX43AA receives a nominal -48V power supply from the office battery. The card provides output voltages of +5V, +12V, +25V, and -15V for the ISM shelf. The card regulates these voltages and sends alarms signals. The card detects overvoltage or undervoltage conditions and sends an alarm to the modular supervisory panel (MSP).

### Functional blocks

The NTFX43AA contains of the following functional blocks:

- input filter
- automatic recovery from low battery (ARLB)
- start-up circuit
- auxiliary power supply
- power switches and drive circuit
- current sense
- power transformer
- rectifiers and output filtering
- the +5.1V output
- the +12V output
- the -15V output
- the +25V output
- minimum load circuit
- output monitoring
- control circuit
- current share circuit

- synchronization circuit
- the MSP interface
- the BUS terminations

### Input filter

The input filter provides both common and differential mode filtering for the switching power train.

### Automatic recovery from low battery

The ARLB circuit senses the input voltage. The ARLB circuit signals the auxiliary power supply to shut down the converter. The converter must shut down when the input voltage extends beyond the minimum operational level. When the input voltage rises above the minimum start-up level, the ARLB circuit enables the auxiliary supply. The circuit applies a VCC voltage to the secondary-side pulse width modulator (PWM). A switch of the power field effect transistor (FET) begins.

The ARLB circuit senses the input voltage. When the input voltage falls below the minimum start-up level the ARLB circuit signals the auxiliary power supply. As a result the converter is shut down. The ARLB circuit also enables the auxiliary supply. The system applies the VCC voltage to the secondary-side pulse width modulator (PWM). The power field effect transistor (FETs) starts to switch.

### Start-up circuit

When the start-up occurs, the BR-AF input voltage rail supplies power to the auxiliary supply. The auxiliary supply generates a supply voltage when the auxiliary supply starts the switching cycle. The supply voltage is in addition to the secondary side 15V rail. The system disconnects the supply from the start-up circuit. The ARLB can recover from a loss of input power, if the converter was operational during the loss of power.

### Auxiliary power supply

An auxiliary flyback power supply block produces a nominal +15V VCC rail to the control circuits. The control circuits are on the secondary side of the main power transformer. This block also provides a regulated supply of voltage on the primary transformer. The block derives power from the input. The ARLB circuit has partial control of the block and the overvoltage/undervoltage (OV/UV) circuits.

### Power switches and drive circuit

The power switches (power MOSFETs) are parallel. A push-pull configuration uses the power switches. A gate drive transformer drives the power switches.

## **NTFX43AA** (continued)

The gate drive transformer provides drive signals and isolation needed between the secondary control circuit and the primary side switches.

### Current sense transformer

A current sense transformer senses the strength of the current through the power switches. The transformer provides this information to the control circuit. A diode bridge rectifies the current waveform that appears as a voltage across the current sense resistor, Rs. The system filter the signal before the system applies the signal to the secondary-side PWM controller.

### Power transformer

The main power transformer transfers energy from the primary circuit to the secondary circuit. A multi-tap output winding provides the +5.1V dc, +12V dc, -15V dc, and +25V dc outputs with respect to logic return (LRTN). The transformer provides the voltage between the primary and secondary dc outputs.

### Rectifiers and output filtering

Each output is rectified, smoothed with the operations of the L-C filter network, pre-regulated and diode ORed. The output inductors are coupled to further aid in cross-regulation.

### The +5V output

This block contains a rectification section and an L-C filter network. The L-C filter network reduces the voltage ripple to a level that the specifications rule acceptable. The network provides route monitoring information (RMI) filtering that reduces switching noise to the output load. A minimum load circuit precedes the ORing diode to allow stable operation of the power supply under low load conditions.

### The +12V output

Rectification and L-C filtering provide a dc input to the series voltage regulator. This output is also diode ORed.

### The -15V output

Rectification and L-C filtering provide a dc input to the series voltage regulator. This output is also diode ORed.

### The +25V output

Rectification and L-C filtering provide a dc output. An over-voltage regulator circuit helps regulate of this output. This output is also diode ORed.

### Minimum load circuit

The +5V output has a minimum load circuit that operates when the load of the output is below a specified level. The circuit makes sure that the converter operates normally under all load conditions.

### Output monitoring

An output OV/UV shutdown feature appears on all of the outputs. If the regulated output voltage can rise above a maximum threshold, the OV/UV monitoring circuit uses an OPTO-SCR sends a shutdown signal. The monitoring circuit also sends the shutdown signal when the regulated output voltage falls below a minimum threshold. The OPTO-SCR provides the necessary primary to secondary isolation. The circuit sends the signal to the PWM of the auxiliary supply. The circuit commands the PWM to shut down the converter. At the same time, the microprocessor board receives a DC-FAIL signal through the backplane.

### Control circuit

The control circuit contains a current-mode PWM switching at a free-running frequency of 110 kHz. The control circuit receives power from the auxiliary power supply (VCC-SEC). Inputs to the control circuit contain the following:

- a current sense signal
- a current share signal
- +5V feedback information
- a divided-down synchronized signal

### Current share circuit

The current share circuit uses the error amplifier output of the current mode control circuit as a control signal. The current share circuit uses the error amplifier output because the derived control signal is related to the primary current. This voltage signal connects to the CUR-SHAR signal of the redundant mate of the voltage signal. The two signals connect through a series resistor that creates a common current sharing node. This node is related to the average of all the output currents of the equal converters. The current sharing circuit amplifies the difference between the current sharing node and the current control signal. The current sharing circuit uses the difference to modify the reference supplied to the error amplifier. This error amplifier is in the PWM of the control circuit. An increase or decrease of the reference voltage adjusts the current that the converter supplies.

### Synchronization circuit

The synchronization circuit synchronizes the PWM switching frequency of 128 kHz to an external TTL level clock that operates at 2.56 MHz.

## NTFX43AA (continued)

### The MSP interface

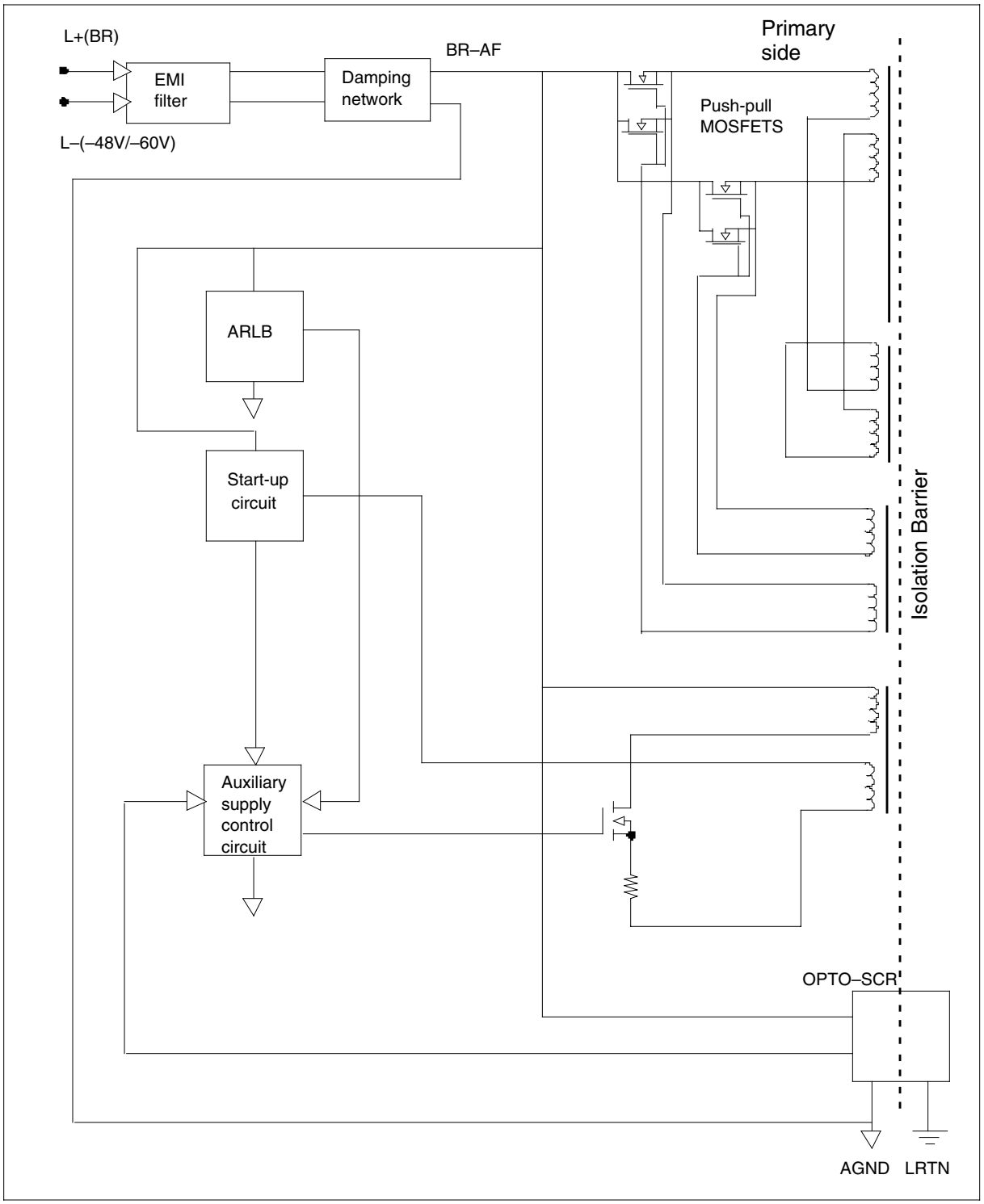
The NTFX43AA provides a direct interface to the NTFX4103 power backplane. The backplane is an interface with the NTRX42AA Breaker module.

### The BUS terminations

The power converter contains three resistive bus terminations. A 330/470W resistive network terminates signals -RDAT, ANUL and -BUSC.

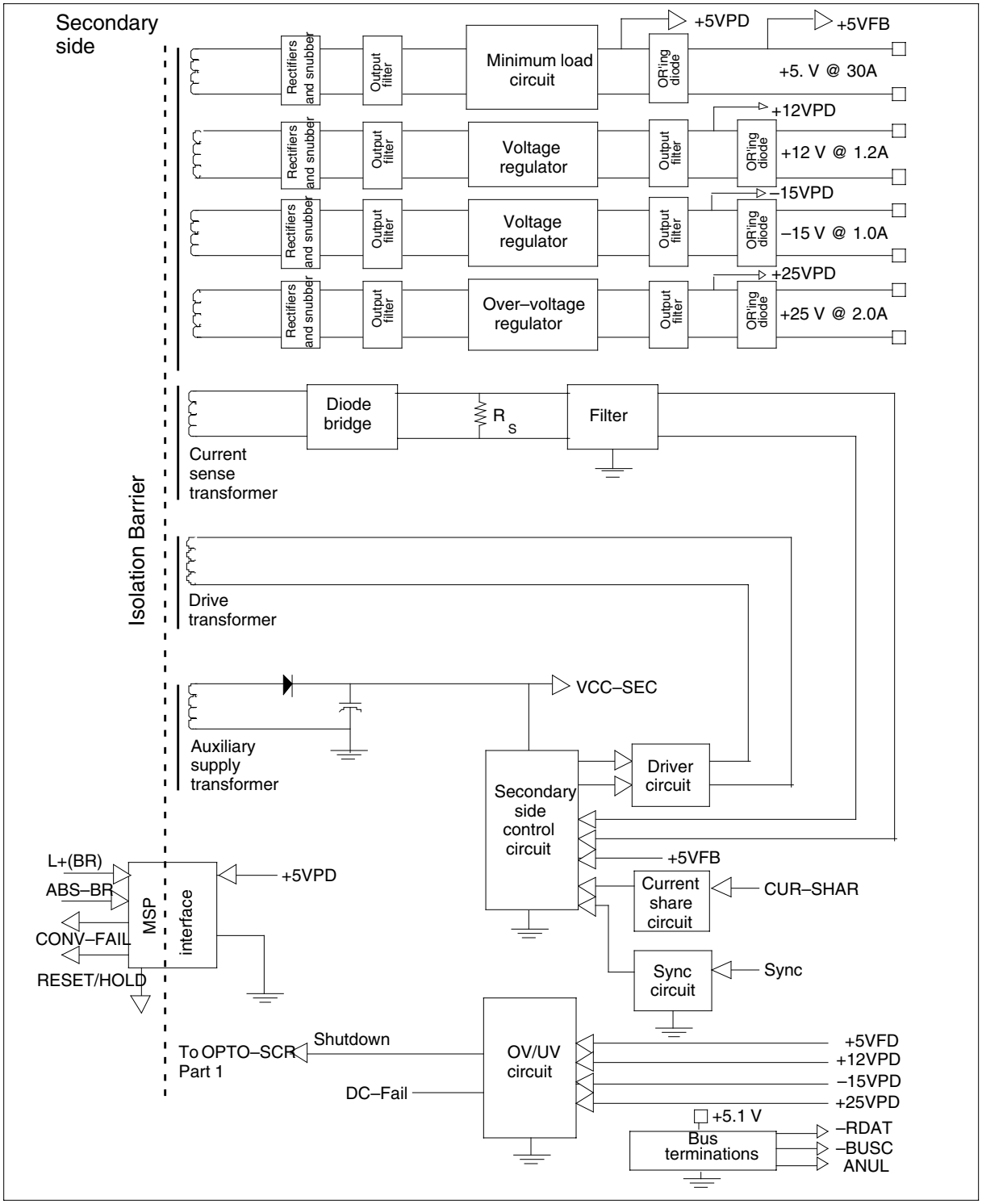
The relationship between the functional blocks appears in the following figures. The primary area appears in the first figure. The secondary area appears in the second figure.

**NTFX43AA Part 1 functional blocks**



# **NTFX43AA** (continued)

### NTFX43AA Part 2 functional blocks



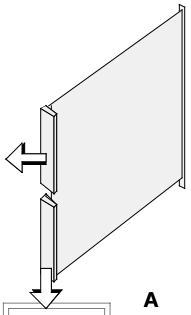
## Signaling

### Pin numbers

The pin numbers for the NTFX43AA appear in the following figure.

# **NTFX43AA** (continued)

### NTFX43AA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | LRTN (GND) | LRTN (GND) |
| 2A 2B | LRTN (GND) | LRTN (GND) |
| 3A 3B | LRTN (GND) | LRTN (GND) |
| 4A 4B | LRTN (GND ) | LRTN (GND) |
| 5A 5B | LRTN (GND) | LRTN (GND) |
| 6A 6B | | |
| 7A 7B | L– (–48V–IN) | L– (–48V–IN) |
| 8A 8B | L– (–48V–IN) | L– (–48V–IN) |
| 9A 9B | L– (–48V–IN) | L– (–48V–IN) |
| 10A 10B | L– (–48V–IN) | L– (–48V–IN) |
| 11A 11B | L– (–48V–IN) | L– (–48V–IN) |
| 12A 12B | L– (–48V–IN) | L– (–48V–IN) |
| 13A 13B | L– (–48V–IN) | L– (–48V–IN) |
| 14A 14B | | |
| 15A 15B | | |
| 16A 16B | L+ (BATT–RTN) | L+ (BATT–RTN) |
| 17A 17B | L+ (BATT–RTN) | L+ (BATT–RTN) |
| 18A 18B | L+ (BATT–RTN) | L+ (BATT–RTN) |
| 19A 19B | L+ (BATT–RTN) | L+ (BATT–RTN) |
| 20A 20B | L+ (BATT–RTN) | L+ (BATT–RTN) |
| 21A 21B | L+ (BATT–RTN) | L+ (BATT–RTN) |
| 22A 22B | L+ (BATT–RTN) | L+ (BATT–RTN) |
| 23A 23B | | |
| 24A 24B | LRTN (GND) | LRTN (GND) |
| 25A 25B | +25V–0UT | +25V–0UT |
| 26A 26B | +25V–0UT | +25V–0UT |
| 27A 27B | +25V–0UT | +25V–0UT |
| 28A 28B | +25V–0UT | +25V–0UT |
| 29A 29B | | |
| 30A 30B | +5V–OUT | +5V–OUT |
| 31A 31B | +5V–OUT | +5V–OUT |
| 32A 32B | +5V–OUT | +5V–OUT |
| 33A 33B | +5V–OUT | +5V–OUT |
| 34A 34B | +5V–OUT | +5V–OUT |
| 35A 35B | +5V–OUT | +5V–OUT |
| 36A 36B | +5V–OUT | +5V–OUT |
| 37A 37B | +5V–OUT | +5V–OUT |
| 38A 38B | +5V–OUT | +5V–OUT |
| 39A 39B | +5V–OUT | +5V–OUT |
| 40A 40B | +5V–OUT | +5V–OUT |

| | A | B |
|---|---|---|
| 41A 41B | LRTN (GND) | LRTN (GND) |
| 42A 42B | LRTN (GND) | LRTN (GND) |
| 43A 43B | LRTN (GND) | LRTN (GND) |
| 44A 44B | LRTN (GND) | LRTN (GND) |
| 45A 45B | LRTN (GND) | LRTN (GND) |
| 46A 46B | | |
| 47A 47B | | |
| 48A 48B | ABS–BR | ABS–BR |
| 49A 49B | RESET | RESET |
| 50A 50B | HOLD | HOLD |
| 51A 51B | | CONV–FAIL |
| 52A 52B | SYNC | SYNC |
| 53A 53B | LRTN (GND) | LRTN (GND) |
| 54A 54B | | |
| 55A 55B | | |
| 56A 56B | | |
| 57A 57B | DCFAIL | CUR–SHAR |
| 58A 58B | LRTN (GND) | LRTN (GND) |
| 59A 59B | –15V–OUT | –15V–OUT |
| 60A 60B | –15V–OUT | –15V–OUT |
| 61A 61B | LRTN (GND) | LRTN (GND) |
| 62A 62B | LRTN (GND) | LRTN (GND) |
| 63A 63B | +12V–OUT | +12V–OUT |
| 64A 64B | +12V–OUT | +12V–OUT |
| 65A 65B | +12V–OUT | +12V–OUT |
| 66A 66B | +12V–OUT | +12V–OUT |
| 67A 67B | +12V–OUT | +12V–OUT |
| 68A 68B | –RDAT | |
| 69A 69B | –BUSC | ANUL |
| 70A 70B | +5V–OUT | +5V–OUT |
| 71A 71B | +5V–OUT | +5V–OUT |
| 72A 72B | +5V–OUT | +5V–OUT |
| 73A 73B | +5V–OUT | +5V–OUT |
| 74A 74B | +5V–OUT | +5V–OUT |
| 75A 75B | LRTN (GND) | LRTN (GND) |
| 76A 76B | LRTN (GND) | LRTN (GND) |
| 77A 77B | LRTN (GND) | LRTN (GND) |
| 78A 78B | LRTN (GND) | LRTN (GND) |
| 79A 79B | LRTN (GND) | LRTN (GND) |
| 80A 80B | LRTN (GND) | LRTN (GND) |

# Technical data

## Power requirementsInput specifications

The nominal voltage is -48/60V. The range of the nominal voltage is between a minimum of -39.0V and a maximum of -75V. The maximum current is 8.5A. The converter operates at the low-battery shutdown voltage (-38.0 ±0.75V). The converter must start at the low-battery recovery voltage (-41.0 ±0.5V).

## Output specifications

The output specifications for +5.1V appear in the following table.

**-5.1V output**

| Parameter | Value |
|---|---|
| Nominal voltage | +5.1V ±0.25V |
| Maximum current | 30A |
| Minimum current | 0.0A |
| Maximum current limit | 6 A |
| Maximum current limit | 31A |
| Overvoltage shutdown | 6.5V ±0.5V |
| Undervoltage shutdown | 4.3V ±0.3V |
| Ripple | 50 mV (rms) |

The output specifications for +12V appear in the following table.

**+12V output**

| Parameter | Value |
|---|---|
| Nominal voltage | +12V ±.72V |
| Maximum current | 1.2A |
| Minimum current | 0.0A |
| Current limit | 2.2 A ±0.8A |
| Overvoltage shutdown | 14V ±1 V |
| Undervoltage shutdown | 10.3 V ±0.7 V |
| Ripple | 75 mV (rms) |

## **NTFX43AA** (end)

The output specifications for -15 V appear in the following table.

**The -15V output**

| Parameter | Value |
|---|---|
| Nominal voltage | -15 V ±0.9 V |
| Maximum current | 1.0A |
| Minimum current | 0.0 A |
| Current limit | 2.2 A ±0.8 A |
| Overvoltage shutdown | -17V ±1 V |
| Undervoltage shutdown | -13 V ±1 V |
| Ripple | 50 mV (rms) |

The output specifications for +25 V appear in the following table.

**The +25V output**

| Parameter | Value |
|---|---|
| Nominal voltage | 25 V ±3 V |
| Minimum current | 0.0 A |
| Maximum current limit | 12 A |
| Maximum current | 2.0 A |
| Minimum current limit | 2.1 A |
| Overvoltage shutdown | 30.05 V ±1.5 V |
| Undervoltage shutdown | 20.6 V ±1.6 V |
| Ripple | 75 mV (rms) |

### Dimensions

The dimensions for the NTFX43AA are as follows:

- height is 317.5 mm (12.5 in.)
- depth is 264.2 mm (10.4 in.)
- width is 57.2 mm (2.25 in.)

# NTFX44AA

## Description

The (NTFX44AA) improved loop test accessory (ILTA) circuit card is for use with some external test units during tests of remote subscriber lines. External test units the NTFX44AA operates with are the Nortel Networks Model 3703 Local Test Cabinet (LTC) and Teradyne[rsquor]s 4-Tel Colt. Central control software can command the ILTA to apply dc voltages to Tip (T) and Ring (R) pair of the card. The T or R pair connect to an external test unit. This action informs the external test unit of the type and the condition of the line under test. The line type can be single party, multi-party or coin. The condition of the line can be functional or bad. The ILTA implements the dc signaling that the TR-TSY-000465, Interface between Loop Carrier Systems and Loop Testing Systems, Section 5, specifies.

The NTFX44AA card occupies a single slot and can be provisioned in any of the 15 slots of the integrated services module (ISM) shelf (NTFX41AA). The card has two backplane connectors. One backplane connector connects to four NT2X90AD cards. The other backplane connector connects to four horizontal connectors on the wideband test access (WTA) panel (NT7X76BA). On the first backplane connector, each input (TTn and TRn), where n = 1 to 4, normally connects to the TT and TR leads of one NT2X90AD trunk card. The TT and TR leads of the trunk card connect to an external test unit. On the second connector, each output (Tn and Rn), where n = 1 to 4, connects to one horizontal of the metallic test access (MTA) matrix. Normally, the horizontal of the MTA matrix is a horizontal of the WTA panel.

## Functional description

The ILTA performs the following functions:

- communicates with central control (CC) through the ISM controller and the ISM backplane bus
- generates +75V dc, which is necessary for dc signaling to the external test units
- performs dc signaling to the external test units (one for each ILTA port)

### Functional blocks

The NTFX44AA contains of the following functional blocks:

- the CC/ILTA communication
- the +75V dc/dc converter

### The CC/ILTA communication

Two trunk logic circuit (TLC) chips, U2 and U3, interface between the ISM backplane bus and the rest of the ILTA card. The CC sends data to the ILTA in

## **NTFX44AA** (continued)

sequence during the ISM controller and the RDATA line of the ISM backplane bus. The CC sends data during channel 0, when the Enable signal of the TL becomes active. During each transaction, the system sends 1 byte of data to the TLC. The system latches the byte is latched on the TLC and the byte appears at eight parallel outputs. At the same time, the TLC sends the earlier latched byte to the CC. The TLC sends this byte to the CC through the TDATA line of the ISM backplane bus and the ISM controller. The earlier latched byte is the byte that the new data replaces. The transmission of the byte from the TLC to the CC is a verification that the TLC receives and latched the data without errors.

Transistors (Q20 and Q21) invert the data that the two TLCs transmit and provide an open-collector feature. The transient protection circuits supply 12V dc to the TLCs. Power-up reset circuits (R46, C12, R47 and C13) make sure that the TLC outputs reset to logic 0 at power-up or at plug-in.

### The +75 V dc/dc converter

One +75V dc/dc converter is present to complete the dc signaling that the TR-TSY-00465 specifies. The converter is based on the switched-mode regulator chip (U1) of type QM-SI9100DT5, that oscillates at a frequency of about 0.5 MHz. The input voltage is normally -48V dc. To accommodate international applications and battery supply variations the converter can operate an input voltage between -39V dc and -72V dc. The regulator chip contains an MOS switch with terminals at DRAIN (device pin 5) and SRC (device pin 7). Magnetic energy accumulates in the core of the transformer (T1) during the conduction phase of the switching cycle. The magnetic energy releases to the load during the nonconductive phase of the cycle. The magnetic energy releases through diode D8. Resistor R28 determines the converter oscillating frequency of 500 kHz. The feedback determines the output dc voltage of +75V. The feedback contains a current mirror (Q6/Q7) and resistors (R14 and R23).

A Zener diode (D5) and resistors R1 and R2 produce a voltage of +50V dc from the +75V dc.

The input filter reduces input ripple. The input filter contains of inductances (L2 and L3) and capacitors (C15 and C16). Fuse F2 provides input over-current protection. Zener diode D26 provides input over-voltage and reverse voltage protection. Resistors R24 and R27 sense the current peaks of the MOS switch. Negative feedback limits the current peaks to a safe value for the MOS switch.

The +75 V failure circuit contains of resistor R3, Zener diode D6 and transistor Q5. When the converter output voltage is above the operational voltage of Zener diode D6, approximately 62V dc, transistor Q5 conducts. This action

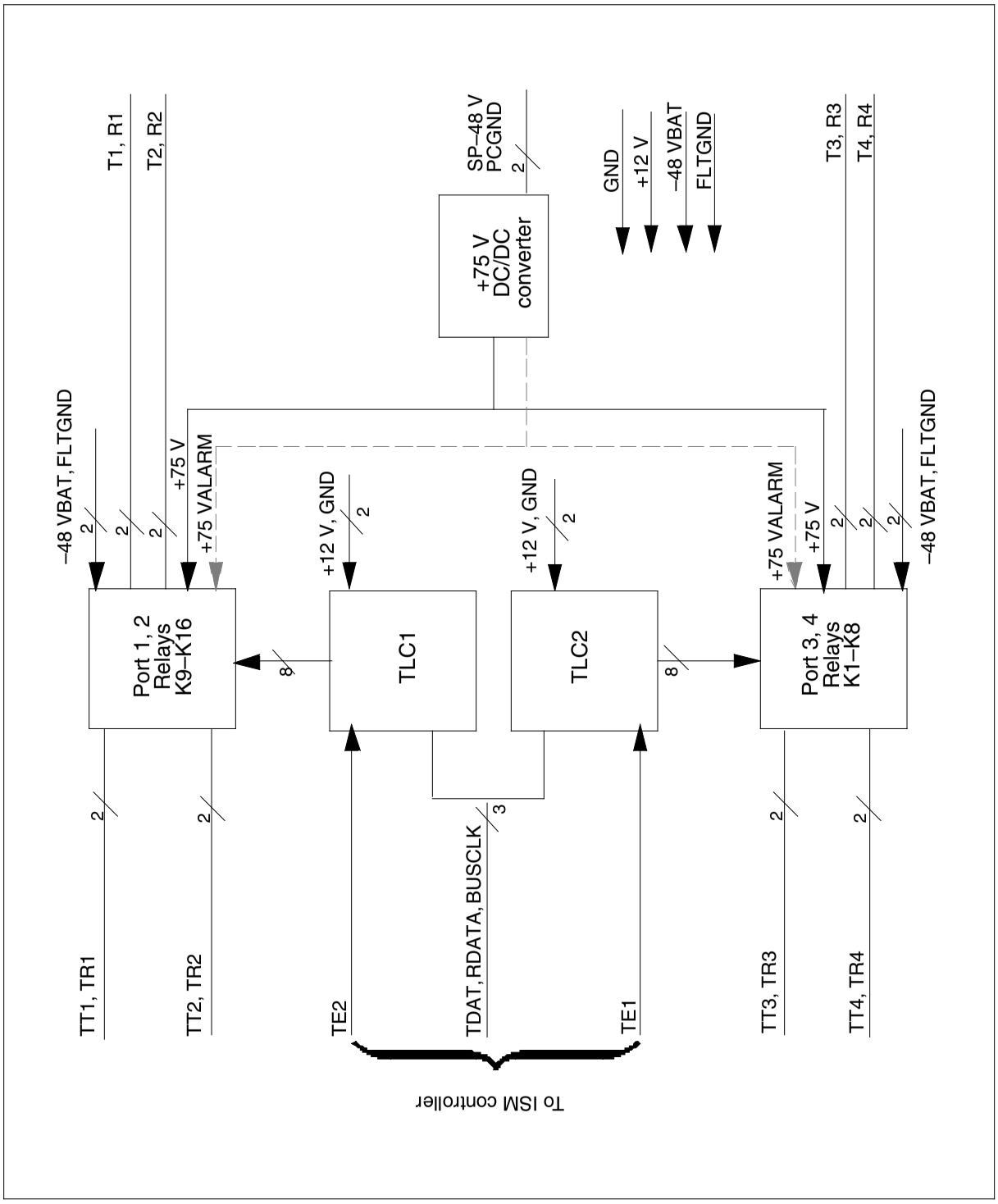
occurs to lower the collector voltage to close to 0. If switch S1-1 is closed and switch S1-2 is open, a logical 0 appears at the TLC chip (U3, pin 4). When the converter voltage drops below the operational voltage, transistor Q5 activates and +12V is applied to the TLC through resistor R43, diode D13, and switch S1-1. The CC detects this voltage every time the TLC chip is queried. To decrease the converter voltage to approximately +60V, close switch S1-3. To completely turn off the converter voltage, close S1-4.

***Note:*** The alarm feature is optional. You must keep the alarm feature OFF until the CC software can handle the feature. Until the development of CC software that can handle this feature, keep switches S1-1 and S1-2 in the OFF position.

The relationship between the functional blocks appears in the following figure.

## **NTFX44AA** (continued)

**The NTFX44AA simplified block diagram**



# Signaling

## The DC signaling

As described in the functional description of the +75V dc/dc converter, each TLC provides eight parallel outputs that the CC software can set.

**The DC signaling towards external test uinits**

| TLC nibble (EX code) | TTn | TRn | Observation |
|---|---|---|---|
| 0 | Tn | Rn | Bypass |
| 1 | Tn | Rn | Bypass |
| 2 | Tn | Rn | Bypass |
| 3 | Tn | Rn | Bypass |
| 4 | +75 V | GND | Coin line |
| 5 | +75 V | -48 V | |
| 6 | -48 V | GND | Multi-party line |
| 7 | -48 V | -48 V | |
| 8 | GND | -48 V | Single paty line |
| 9 | +50 V | -48 V | |
| A | GND | +75 V | Bad line |
| B | +50 V | +75 V | |
| C | GND | GND | Not performed/not ready |
| D | +50 V | -48 V | |
| E | GND | GND | Not performed/not ready |
| F | +50 V | -48 V | |

Sixteen TLC outputs are provided. The outputs control 16 relays (K1 to K16) through transistors Q1 to Q4 and Q8 to Q19. The transistors act as relay drivers. The contacts of the 16 relays interconnect and connect to the on-board +75V supply. These contacts also interconnect and connect to the backplane -48V battery (BAT) and ground (FLTGND). The contacts connect in this way to provide four independent signaling ports for external test units. Each port n

## **NTFX44AA** (continued)

has a pair of input leads, TTn and TRn. Each part has a pair of output leads, Tn and Rn, where n = 1 to 4. The signaling that each port performs n on on the port input leads TTn and TRn appears in the Signaling table (refer to Notes 1 through 3).

The following are the TLC nibbles for each port:

- n=1: U2, P0 to P3 (where P0 is the most significant bit [MSB])
- n=2: U2, P4 to P7 (where P4 is the MSB)
- n=3: U3, P0 to P7 (where P0 is the MSB)
- n=4: U3, P4 to P7 (where P4 is the MSB)

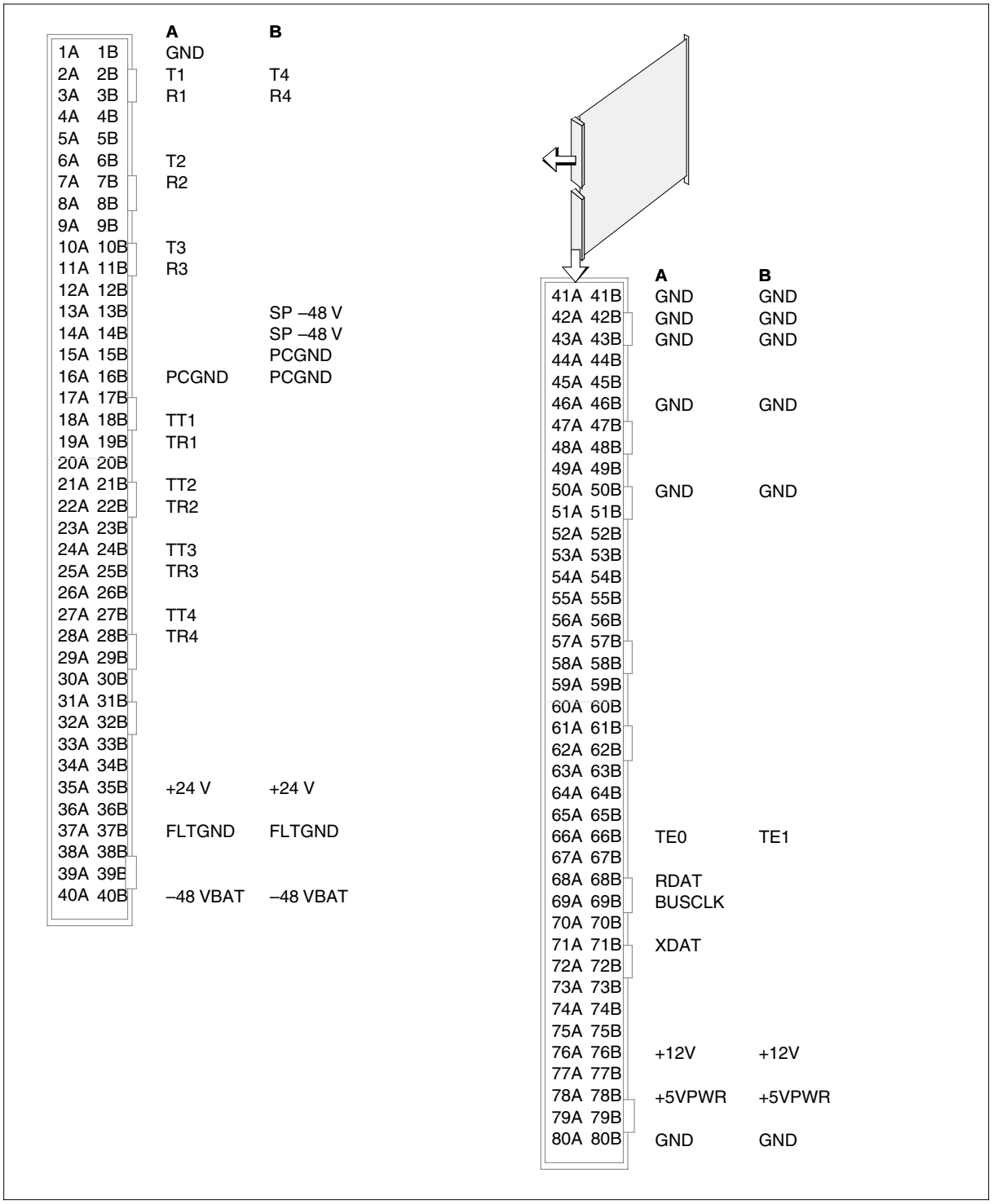
***Note 1:*** s:1 Bypass indicates that the input leads connect to the output leads. For example, TTn connects to Tn and TRn connects to Rn. This connection provides the steady-state and power-up state of the ILTA to all 4 ports.

***Note 2:*** Only the states with an inspection have meaning, as TR-TSY-000465 specifies. Now, states when the TLC nibble is an odd number are not used. The CC software never sets the least significant bit (LSB) of each nibble.

### Pin numbers

The pin numbers for the NTFX44AA appear in the following figure.

### The NTFX44AA pin numbers



## **NTFX44AA** (continued)

# Technical data

### Power requirements

The power requirements for the NTFX44AA appear in the following table.

**Power requirements**

| **Voltage** | **Voltage and current combinations** | | |
|---|---|---|---|
| **Parameter** | **Minimum** | **Nominal** | **Maximum** |
| +12V supply | | 12 V +/- 0.3 V20 mA | |
| +25V supply | | 25 V +/- 2.0 V max. 100.0 mA | |
| -48V -SP supply | -39 V | -48V max. 25 mA | -72 V |
| -48V BAT supply | -39 V | -48V max. 15 mA | -72 V |

The maximum heat distribution is 3 W. The average heat distribution is 1 W.

### Switch settings

The NTFX 44AA card has a 4-.position dip switch labeled S1. The factory sets the default setting of OFF to all four positions (S1-1, -2, -3 and -4).

**The S1 switch settings (Sheet 1 of 2)**

| **Description** | **Position setting 1** | **Position setting 2** | **Position setting 3** | **Position setting 4** |
|---|---|---|---|---|
| DC/DC converter failure alarm is applied and K1 relay is not used | **ON** | OFF | OFF | OFF |
| DC/DC converter failure alarm is inhibited and K1 relay enables | OFF | **ON** | OFF | OFF |
| DC/DC converter failure alarm and K1 relay are not used | OFF | OFF | OFF | OFF |

**The S1 switch settings (Sheet 2 of 2)**

| Description | Position setting 1 | Position setting 2 | Position setting 3 | Position setting 4 |
|---|---|---|---|---|
| Testing only. | OFF | OFF | **ON** | OFF |
| Testing only. DC/DC converter failure alarm shuts off. | OFF | OFF | OFF | **ON** |

## Dimensions

The dimensions for the NTFX44AA are as follows:

- height is 353 mm (9.0 in.)
- depth is 267 mm (10.5 in.)
- width is 29 mm (1.125 in.)

# 8 NTKXnnaa

## NTKX06AA

# NTKX06AA

## Product description

### Overview

The NTKX06AA TDM processor card is the voice controller for the Universal Edge 9000 (UE9000). The NTKX06AA

- contains a processor and time switch resources to implement DMS-100 call handling for subscriber loops. The NTKX06AA
  - — routes voice traffic from POTS loops or asymmetrical digital subscriber line (ADSL) line cards
  - — terminates a maximum of six DS-30B links to an XPM and supports link distances up to 250 ft. Extended distances requires DIP switch settings on the board to be adjusted. Either NTKX06AA can drive a DS-30B link.
- contains the messaging hub that operates a series of messaging links, in the UE9000 DMS backplane. The series of links, or GLAN, allow the processor to exchange messaging with other UE9000 shelf cards.
- operates in tandem with another NTKX06AA in a load sharing arrangement or in a fully redundant takeover mode
- provides the voice domain interface to the controlling line group controller (LGC), line/ trunk controller (LTC), or remote cluster controller 2 (RCC2)
- supports simplex (takeover) operation

### Location

The NTKX06AA resides in slots 12 and 13 of the UE9000 shelf.

## Functional description

The UE9000 provides concentrated support for 512 lines (16 line card slots x (1) 32-line multi circuit line card). Two high-speed, point-to-point serial buses, the TDM and GLAN buses, provide an interface between the 16 line card slots and each NTKX06AA:

- The GLAN bus carries upstream and downstream messaging.
- The TDM bus carries PCM/voice in both the upstream and downstream directions

***Note:*** The term “downstream” indicates the direction of flow from the controlling LGC, LTC, or RCC2 to each line circuit. The term “upstream” indicates the direction from each line circuit to the controlling LGC, LTC, or RCC2.

The Memphis application-specific integrated circuit (ASIC) on the line cards terminates the TDM and GLAN buses and provides an interface to each line circuit.

### Functional blocks

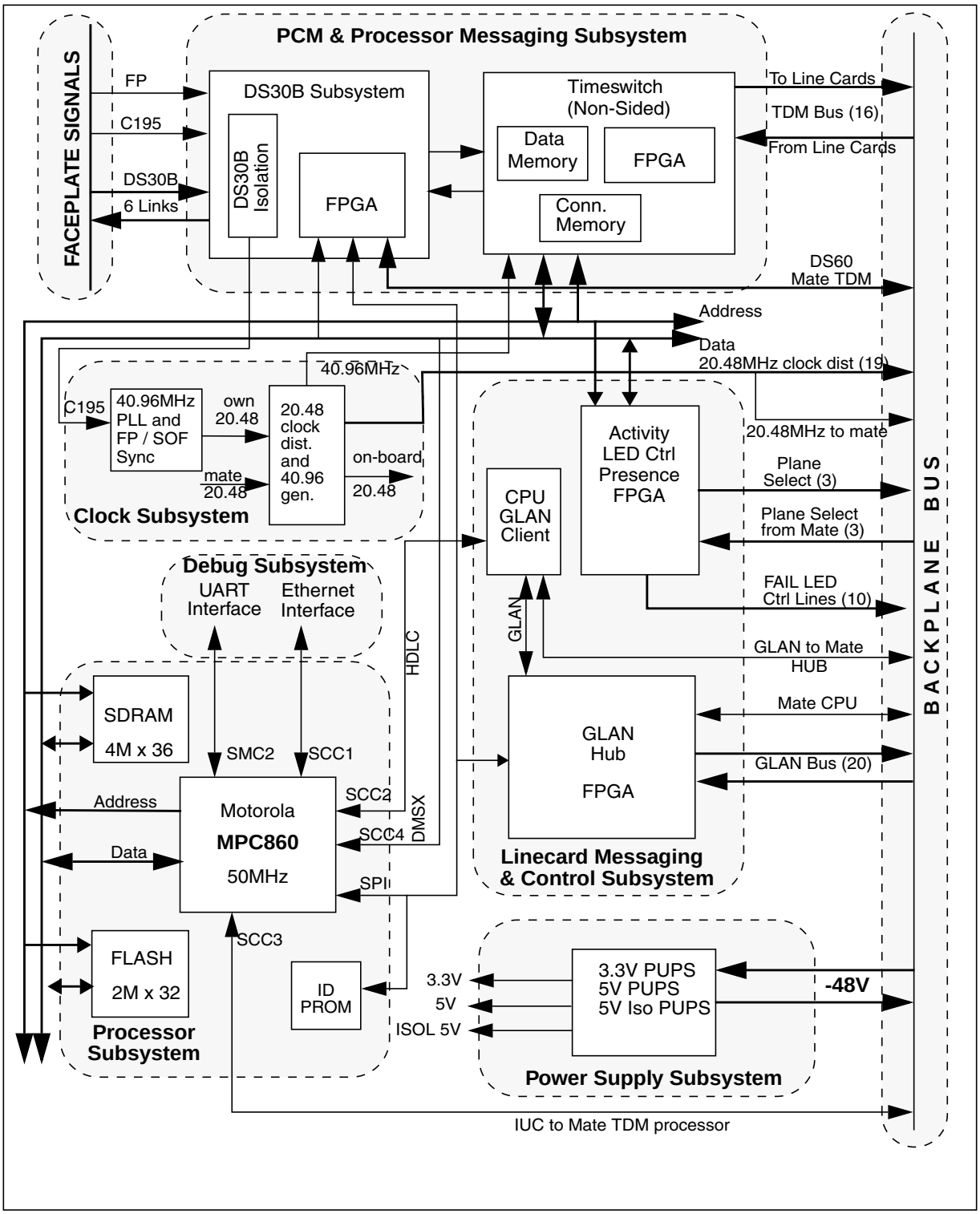
The NTKX06AA includes the functional blocks that follow:

- GLAN communications hub
- DS-30B link interface
- TDM crossover bus
- time switch and line card TDM bus interface
- processor complex
- DMS-X messaging termination
- local craft interface
- power supply

The following figure shows a block diagram of the NTKX06AA circuit card.

# **NTKX06AA** (continued)

### NTKX06AA functional blocks



### GLAN communication hub

The GLAN communication hub provides the messaging infrastructure for control message exchange between all cards on the UE9000. The GLAN hub handles the transmission and arbitration of HDLC messages between clients (1 client/card). When the GLAN hub allows a client to transmit a message, the other clients also receive and screen the message based on the destination address of the message. This design allows any client to communicate with any other client. However, messages generally flow between the TDM common equipment and the line cards.

The UE9000 has one GLAN hub in each NTKX06AA card and two GLAN hubs in each shelf. Clients use the GLAN hub on the active NTKX06AA card. The inactive GLAN hub is idle.

The GLAN is a LAN with a point-to-point physical layout. The GLAN bus is a 3-wire serial interface with the following signals:

- clock
  - — has a rate of 20.48 MHz
  - — is shared with the TDM bus
- upstream and downstream data

The data lines are unique to each slot.

The GLAN hub has 28 GLAN ports. Unused ports are inactive.

GLAN software interfaces:

- enable or disable GLAN
- limit message lengths
- monitor GLAN client presence

### DS-30B loop interface

Pulse code modulation (PCM) and messaging between the XPM and UE9000 DMS transfer over the DS-30B links. The interface has 14 physical signals for the six DS-30B links:

- 1 C195 clock signal
- 1 frame pulse
- 1 transmit and 1 receive signal for each link

Each link has thirty-two 10-bit channels that create a bit rate of 2.56 Mb/s. The TDM interface supports extended distances up to 250 feet. DIP switch settings

## NTKX06AA (continued)

allow the DS-30B field programmable gate array (FPGA) to compensate for the changes in transmission delay at different cable lengths. The DS-30B is compatible with DS-30A interfaces and can be electrically isolated from the DS-30A side of the cable.

In the in-service state, each of the two NTKX06AA cards controls three of the DS-30B links (three DS-30B links for each NTKX06AA). When one of the NTKX06AA cards is out of service, the in-service card drives the speech channels for all six DS-30B links. The NTKX06AA card always drives the messaging channels that it *owns*.

### TDM crossover bus

The TDM common equipment card includes an intermodule DS-60 link that provides

- compatibility with the LCM, which contains two DS-30A cards for PCM data exchange
- PCM exchange between the two NTKX06AA cards

The two TDM processors communicate across dedicated serial inter-unit communication links (IUC), which are separate from the DS-60 links and from other GLAN messaging links.

### Time switch and line card TDM bus interface

The time switch FPGA

- connects a DS-30B or TDM time slot to any other TDM or DS-30B time slot
- supports P-side to P-side, P-side to C-side, and C-side to C-side connections

The processor writes to the connection memory to create connections. The Time switch may also send fixed and programmable patterns to any channel.

For data flow, the time switch connects to the following buses:

- DS-30B link ports
- DS-60
  - — for TDM PCM exchange
  - — serial stream with 64 10-bit channels
- TDM
  - — 20.48 MHz to provide 156 slots, 10 bits/slot
  - — max 16 to line card slots
  - — protocol overhead includes
    - – CRC information (checking and generation are not supported)
    - – frame count
    - – framing bits
    - – parity (software control provides parity)

### Processor complex

The Motorola MPC860 Power Quad Integrated Communication Controller (QUICC) is the engine of the processor complex. The QUICC executes the controlling software that

- processes DMS-X messages from the XPM
- controls and maintains the line cards
- sets up and maintains the time switch
- performs routine diagnostics on the UE9000 hardware

### DMS-X messaging termination

DMS-X message termination occurs in a Motorola MPC860 SCC port. DS-30B circuitry sends the frame pulse and serial data stream to the Motorola MPC860. The Motorola MPC860 time slot assigner selects and sends the data channel to the SCC port. The data rate for DMS-X is 64 kb/sec.

### Local craft interface

No local craft interface (LCI) is supported for the NTKX06AA. The RS-232 asynchronous serial port is for use only by Nortel Networks. The 10/100-BaseT Ethernet port is not used.

### Power supply

The on-board point of use power supply (PUPS) creates voltages for TDMIF circuitry. A -48V to +3.3V converter provides power for the board. A -48V to

## **NTKX06AA** (continued)

+5V converter generates the isolated power for the DS-30B circuitry. A second -48V to +5V converter supports the remaining +5V circuitry that should be non-isolated.

# Signaling

### NTKX06AA DIP switch settings

Unlike the DS-30A which is limited to connecting cables of 50 ft, DS-30B can transmit over variable distances of up to 250 ft. DIP switch settings and/or software control of the delay register allow the DS-30B FPGA to compensate for the changes in transmission delay at different cable lengths. The following table provides the DIP switch settings for the NTKX06AA.

**DS-30B link length equalization DIP switch settings**

| DIP switch settings (5-1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **6** | **5** | **4** | **3** | **2** | **1** | **Cable length in feet for frame-based equipment (Note 2)** | **Cable length in feet for cabinetized equipment (Note 3)** |
| **Software controlled length** | | | | | | | |
| Note 1 | Off | Off | On | Off | Off | 50 | - |
| Note 1 | Off | Off | On | Off | On | 75 | 50 |
| Note 1 | Off | Off | On | On | Off | 100 | 75 |
| Note 1 | Off | Off | On | On | On | 125 | 100 |
| Note 1 | Off | On | Off | Off | Off | 150 | 125 |
| Note 1 | Off | On | Off | Off | On | 175 | 150 |
| Note 1 | Off | On | Off | On | Off | 200 | 175 |
| Note 1 | Off | On | Off | On | On | 225 | 200 |
| Note 1 | Off | On | On | Off | Off | 250 | 225 |
| Note 1 | Off | On | On | Off | On | - | 250 |

***Note 1:*** DIP switch number 6 is used to select between DIP switch controlled delay and software controlled delay. If DIP switch number 6 is set to On, then delay is controlled by software.
If DIP switch number 6 is set to Off, then delay is controlled by value set on DIP switches 5-1.

***Note 2:*** When hosted by a frame-based XPM (such as, LGC) or RCC2.

***Note 3:*** When hosted by a cabinetized XPM (CLGE) or RCC2 in a CRSC cabinet.

### Pin outs

The figure that follows shows the pin outs for NTKX06AA.

**NTKX06AA connector P6 pin outs**

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | ID | GND | GND | GND | ID |
| 2A 2B 2C 2D 2E | GND | | GND | | GND |
| 3A 3B 3C 3D 3E | | GND | GND | GND | |
| 4A 4B 4C 4D 4E | GND | CLK_from_Mate | GND | GND | |
| 5A 5B 5C 5D 5E | GND | GND | GND | GND | GND |
| 6A 6B 6C 6D 6E | GLAN_US | GLAN_US | GND | GLAN_US | GLAN_US |
| 7A 7B 7C 7D 7E | GLAN_US | GLAN_DS | GND | GLAN_US | GLAN_US |
| 8A 8B 8C 8D 8E | GLAN_US | GLAN_DS | GND | GLAN_US | GLAN_US |
| 9A 9B 9C 9D 9E | GLAN_US | GLAN_DS | GND | GLAN_US | GLAN_US |
| 10A 10B 10C 10D 10E | | | GND | GND | GND |
| 11A 11B 11C 11D 11E | | | GND | | |
| 12A 12B 12C 12D 12E | | | | | |
| 13A 13B 13C 13D 13E | | | | | |
| 14A 14B 14C 14D 14E | GLAN_US | GLAN_DS | GND | GLAN_US | GLAN_US |
| 15A 15B 15C 15D 15E | GLAN_US | GLAN_DS | GND | GLAN_US | GLAN_US |
| 16A 16B 16C 16D 16E | GLAN_US | GLAN_DS | GND | GLAN_US | GLAN_US |
| 17A 17B 17C 17D 17E | GLAN_US | GLAN_DS | GND | GLAN_US | GLAN_US |
| 18A 18B 18C 18D 18E | GLAN_US | GLAN_DS | GND | GND | GND |
| 19A 19B 19C 19D 19E | | | GND | GND | GND |
| 20A 20B 20C 20D 20E | GLCK | GLCK | GND | GLCK | CLK_from_Mate |
| 21A 21B 21C 21D 21E | GLCK | GLCK | GND | GLCK | GLCK |
| 22A 22B 22C 22D 22E | GLCK | GLCK | GND | GLCK | GLCK |
| 23A 23B 23C 23D 23E | GLCK | GLCK | GND | GLCK | GLCK |
| 24A 24B 24C 24D 24E | GLCK | GLCK | GND | GLCK | GLCK |
| 25A 25B 25C 25D 25E | | | | | |

# **NTKX06AA** (continued)

### NTKX06AA connector P7 pin outs

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | | GND | GND | GND | |
| 2A 2B 2C 2D 2E | GND | GND | GND | OWN_TS0 | GND |
| 3A 3B 3C 3D 3E | IUC_RDAT | | GND | | |
| 4A 4B 4C 4D 4E | | GND | GND | IUC_TDAT | GND |
| 5A 5B 5C 5D 5E | SP_OUT | | GND | BPLANESEL | MPLANESEL |
| 6A 6B 6C 6D 6E | SP_IN | GND | GND | BPLANESEL | MPLANESEL |
| 7A 7B 7C 7D 7E | IDP | ID | GND | BPLANESEL | MPLANESEL |
| 8A 8B 8C 8D 8E | SP_OUT | GND | GND | GND | SP_IN |
| 9A 9B 9C 9D 9E | | SP_IN | GND | SP_OUT | GND |
| 10A 10B 10C 10D 10E | ROW | ROW | LED_FAIL_L | ROW | ROW |
| 11A 11B 11C 11D 11E | COL | COL | GND | ID | ID |
| 12A 12B 12C 12D 12E | COL | COL | LED_FAIL_H | COL | COL |
| 13A 13B 13C 13D 13E | BTDM_FP_to_ATM | GND | GND | GND | |
| 14A 14B 14C 14D 14E | | GND | GND | GND | |
| 15A 15B 15C 15D 15E | BPLLREF_to_ATM | GND | GND | GND | |
| 16A 16B 16C 16D 16E | | PLL_REF | GND | GND | |
| 17A 17B 17C 17D 17E | TDM_FP_to_Mate | GND | GND | GND | MPLLREF |
| 18A 18B 18C 18D 18E | | BTDM_TSR | GND | TDM_MFP | GND |
| 19A 19B 19C 19D 19E | GND | GND | GND | GND | TDM_MTSRN |
| 20A 20B 20C 20D 20E | | OG_DS60 | GND | GLAN_DSMP | GND |
| 21A 21B 21C 21D 21E | OWN_INSRV | GND | GND | GND | IC_DS60 |
| 22A 22B 22C 22D 22E | GND | IUC_RDLK | GND | MATE_INSVC | GND |
| 23A 23B 23C 23D 23E | GND | GND | GND | GND | IUC_RDLK |
| 24A 24B 24C 24D 24E | | MATE_TS0 | GND | GLAN_USMMP | GND |
| 25A 25B 25C 25D 25E | SP_OUT | GND | GND | GND | SP_IN |

### NTKX06AA connector P8 pin outs

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | GND | GND | GND | GND | GND |
| 2A 2B 2C 2D 2E | TDM_DS | TDM_DS | GND | TDM_US | TDM_DS |
| 3A 3B 3C 3D 3E | TDM_US | TDM_DS | GND | TDM_US | TDM_DS |
| 4A 4B 4C 4D 4E | TDM_US | TDM_DS | GND | TDM_US | TDM_DS |
| 5A 5B 5C 5D 5E | TDM_US | TDM_DS | GND | TDM_US | TDM_DS |
| 6A 6B 6C 6D 6E | TDM_US | TDM_DS | GND | TDM_US | TDM_DS |
| 7A 7B 7C 7D 7E | GND | GND | GND | GND | GND |
| 8A 8B 8C 8D 8E | TDM_US | TDM_DS | GND | TDM_US | TDM_DS |
| 9A 9B 9C 9D 9E | TDM_US | TDM_DS | GND | TDM_US | TDM_DS |
| 10A 10B 10C 10D 10E | TDM_US | TDM_DS | GND | TDM_US | TDM_DS |
| 11A 11B 11C 11D 11E | TDM_US | TDM_DS | GND | TDM_US | TDM_DS |
| 12A 12B 12C 12D 12E | GND | TDM_DS | GND | GND | GND |
| 13A 13B 13C 13D 13E | | | | | GND |
| 14A 14B 14C 14D 14E | GND | GND | GND | GND | GND |
| 15A 15B 15C 15D 15E | GND | GND | GND | GND | |
| 16A 16B 16C 16D 16E | | GND | GND | GND | |
| 17A 17B 17C 17D 17E | | | GND | | GND |
| 18A 18B 18C 18D 18E | GND | GND | GND | GND | |
| 19A 19B 19C 19D 19E | | GND | GND | GND | |
| 20A 20B 20C 20D 20E | | | GND | | GND |
| 21A 21B 21C 21D 21E | GND | GND | GND | GND | |
| 22A 22B 22C 22D 22E | | GND | GND | GND | |
| 23A 23B 23C 23D 23E | GND | GND | GND | GND | GND |
| 24A 24B 24C 24D 24E | | GND | GND | | |
| 25A 25B 25C 25D 25E | | | GND | | |

### NTKX06AA connector P9 pin outs

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | | SBA -48 V | SBA -48 V | SBA -48 V | SBA -48 V |
| 2A 2B 2C 2D 2E | | SBB -48 V | SBB -48 V | SBB -48 V | SBB -48 V |
| 3A 3B 3C 3D 3E | | SBR -48 V | SBR -48 V | SBR -48 V | SBR -48 V |

### NTKX06AA connector P12 pin outs

| | |
|---|---|
| 1 | GND |

### NTKX06AA BDM port pin outs

| | |
|---|---|
| 1 | VFLS0 |
| 2 | SRESETN |
| 3 | GND |
| 4 | DSCK |
| 5 | GND |
| 6 | VFLS1 |
| 7 | HRESETN |

## **NTKX06AA** (end)

**NTKX06AA RS232 connector pin outs**

| | |
|---|---|
| 1 | GND |
| 2 | DBGTX |
| 3 | DBGRX |
| 4 | No connect |
| 5 | No connect |
| 6 | GND |
| 7 | GND |
| 8 | +5 V |
| 9 | No connect |
| 10 | No connect |

**NTKX06AA ethernet connector pin outs**

| | X | Y |
|---|---|---|
| JX -1 JY-1 | No connect | GND |
| JX-2 JY-2 | ETHTX | ETHRCK |
| JX-3 JY-3 | GND | GND |
| JX-4 JY-4 | ETHTENA | ETHCLSN |
| JX-5 JY-5 | GND | GND |
| JX-6 JY-6 | ETHTCK | No connect |
| JX-7 JY-7 | GND | GND |
| JX-8 JY-8 | ETHRX | +5 V |
| JX-9 JY-9 | GND | GND |
| JX-10 JY-10 | ETHRENA | +5 V |

# Technical data

### Power requirements

The NTKX06AA has the following power requirements

- -40 V minimum
- -48 V nominal
- -60 V maximum

# 9 NTGXnnaa

## NTGX01AA

# NTGX01AA

## Description

The NTGX01AA service peripheral module (SPM) cabinet is the voice mail peripheral for the DMS–100 Family. Each SPM provides voice mail services for electronic mail boxes. The SPM can handle a maximum of 192 ports. These ports include integrated operation, administration, and maintenance (OA) abilities. These ports include enhanced residential and Centrex subscriber services through display–based sets.

The SPM contains three types of nodes:

- multiserver processor (MSP)
- signal processing node (SPN)
- telephony interface node (TIFN)

### Multi–server processor

The MSP has two cards, the NTGX05AA 68–kbyte memory card and the NTGX10AA bus controller main card. The 68–kbyte card provides the processing environment for the common system program, for example, directory and message transfer agent. The 68–kbyte card supports two RS–232C Electronic Industries Association (EIA) communication ports. Two MSPs are paired to provide redundancy and capacity for larger systems. The MSPs support cross–linked disks for disk–shadowing operations.

### Signal processing node

The SPN has one NTGX05AA 68–kbyte memory card and two NTGX12AA voice channel (VP12) cards. The 68–kbyte card provides processing for the computing environments, for each channel, on the service peripheral module. Use the RS–232C communication ports in the SPN for simplified message desk interface (SMDI) links, networking and administration connections. The voice channel cards provide a maximum of 24 channels for each SPN, or 12 channels for each voice processor card. The cards provide the channels for a maximum of four SPNs to an NTGX0201 electronics shelf. The NTGX0201 electronics shelf has a maximum of two shelves. These shelves occupy the NTGX01AA cabinet.

### Telephony interface node

The TIFN has one NTGX05AA 68 kbyte memory card and an NTGX08AA T1 card. The 68 kbyte card provides processing for the T1 handling environment. The 68 kbyte card:

- relays call processing events to the software environment
- provides T1 link maintenance

- selects the T1 span to provide the master clock reference
- maps T1 timeslots to central office (CO) voice mail bus time slots

The T1 card terminates four T1 spans.

### Shelves

Four shelves are available, two NTGX0201 electronics shelf assemblies and two NTGX0301 disk shelf assemblies.

## Parts

The NTGX01AA SPM cabinet contains the following parts:

- NT9X03AA—SuperNode frame supervisory panel
- NTGX0201—electronics shelf assembly
- NTGX0301—disk shelf assembly
- NT9X95CU—cooling unit (CU)

### SuperNode frame supervisory panel

The NT9X03AA SuperNode frame supervisory panel (FSP) provides alarm, maintenance and different supervisory functions. The FSP is in the top shelf position in the NTGX01AA. Open cabinet doors to access or view the front and rear faces of the NT9X03AA. The frame alarm light in the cabinet is visible with the cabinet doors closed.

Power from the power distribution center frame goes to the FSP. The FSP distributes the power to four NT9X91AB power converters. The power converters are in slots 1, 4, 33 and 36 of the NTGX0201 primary electronics shelf assembly in position 26. The FSP distributes the power to these power converters when a maximum of 96 ports are provisioned in the cabinet.

Power from the power distribution center frame goes to the FS. The FSP distributes the power to two NT9X91AB power converters. The two power converters are in slots 1 and 4 of the NTGX0201 expansion electronics shelf assembly in position 39. The FSP distributes the power to the power converters when more than 144 ports are provisioned in the cabinet. When less than 144 ports are provisioned, two NT9X19CA power converter filler face plates are provisioned in slots 1 and 4.

Two NT9X91AB power converters in slots 33 and 36 are provisioned in the NTGX0301 upper disk shelf assembly. The power converters are in position 13 of the cabinet. Two NT9X19CA power converter filler face plates are provisioned in slots 1 and 4 when less than 96 ports are provisioned.

## **NTGX01AA** (continued)

Four NT9X91AB power converters in slots 1, 4, 33, and 36 are provisioned in the NTGX0301 lower shelf assembly. The power converters are in shelf position 00 of the cabinet.

### Electronics shelf assembly

Two NTGX0201 electronics shelf assemblies are available. One assembly is the primary shelf and the other is the expansion shelf. These shelves are in the cabinet at positions 26 and 39, in that order.

Provision cards in the primary electronics shelf first for an SPM with a maximum of 96 ports. For more than 96 ports, provision cards in the expansion shelf.

The following nodes are available in the primary electronics shelf:

- 2 MSP nodes—the NTGX05AA 68 kbyte main card and NTGX10AA bus controller card
- 2 SPN nodes—the NTGX05AA 68 kbyte main card and NTGX12AA VP 12 card, 2 more SPN nodes are provisionable
- 2 TIFN nodes—the NTGX05AA 68 kbyte main card and NTGX08AA T1 main card

The following nodes are available in the expansion electronics shelf:

- 4 SPN nodes—the NTGX05AA 68 kbyte main card and NTGX12AA VP 12 card
- 2 TIFN nodes—the NTGX05AA 68 kbyte main card and NTGX08AA T1 main card

### Disk shelf assembly

Two NTGX0301 disk shelf assemblies are available. One assembly is the upper shelf. The other assembly is the lower shelf. These shelves are in the cabinet at positions 13 and 00, in that order.

The NTGX14AA 1200 Mbyte disk card, for disk 9, is available in slot 27 of the upper disk shelf. One NT9X19AA filler faceplate is available in slot 32.

The disks are provisioned in pairs for the ability to shadow disks for the pair of SPNs that correspond. The following cards are in the upper disk shelf:

- 2 disks, disks 5 and 6,—2 NTGX13AA 600 Mbyte disk cards, NTGX14AA 1200 Mbyte disk cards, or NTGX14BA dual 1200 Mbyte disk cards in slots 7 and 12 when more than 96 ports are available
- 2 disks, disks 7 and 8,—2 NTGX13AA 600 Mbyte disk cards, NTGX14AA 1200 Mbyte disk cards, or NTGX14BA dual 1200 Mbyte disk cards in slots 17 and 22 when more than 168 ports are available

When these cards are not available, position the NT9X19AA filler face plate in slots 7, 12, 17 and 22.

The NTGX15AA disk tape card is always available in slot 27 of the lower disk shelf.

The disks are provisioned in pairs for the ability to shadow disks for the pair of SPNs that correspond. The following cards are in the lower disk shelf:

- 2 disks, disks 1 and 2,—the NTGX13AA 600 Mbyte disk card, NTGX14AA 1200 Mbyte disk card, or NTGX14BA dual 1200 Mbyte disk card when more than 24 ports are available
- 2 disks, disks 3 and 4,—the NTGX13AA 600 Mbyte disk card, NTGX14AA 1200 Mbyte disk card, or NTGX14BA dual 1200 Mbyte disk card when more than 72 ports are available

When these cards are not available, position the NT9X19AA filler face plate in slots 7, 12, 17 and 22.

### Cooling unit

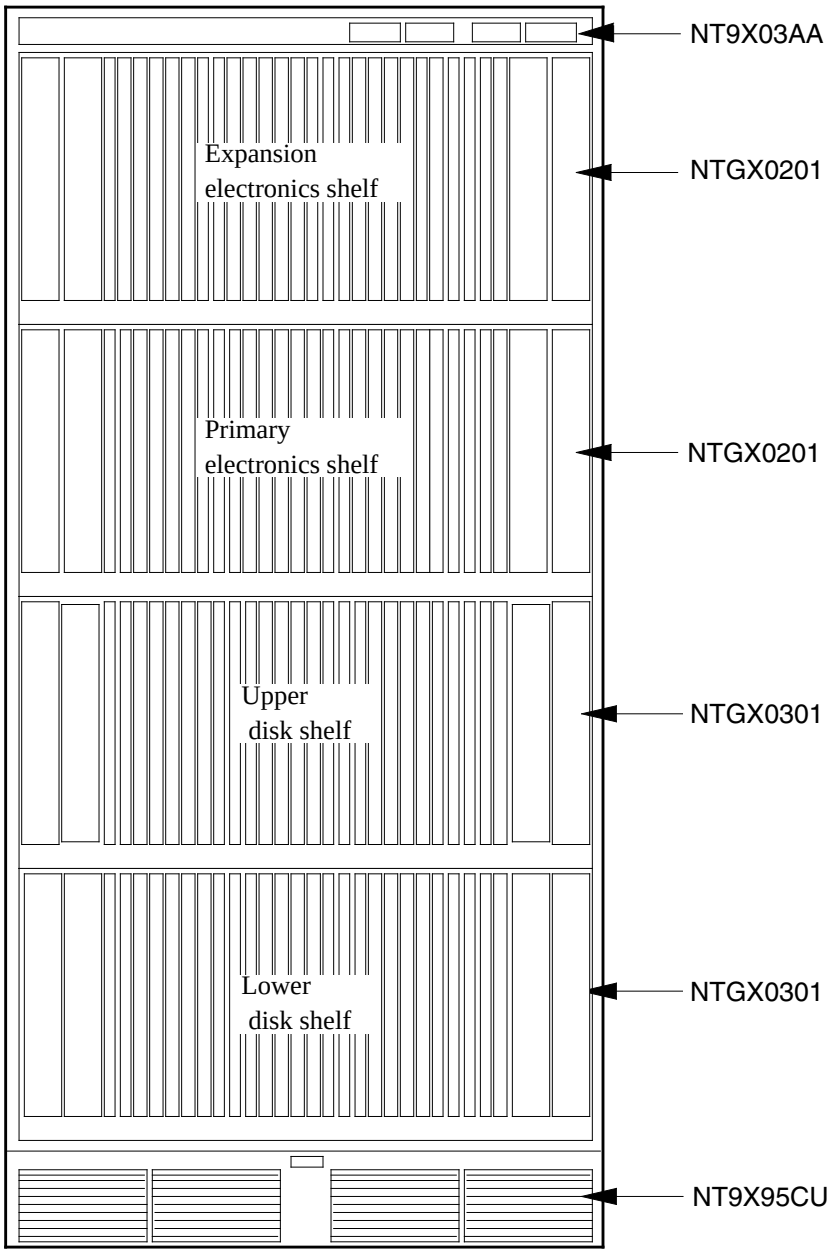
The NT9X95CU cooling unit provides mechanical ventilation for equipment that the SPM cabinet houses.

## Design

The design of the NTGX01AA appears in the following figure.

# **NTGX01AA** (end)

**NTGX01AA parts**




**Note:** This illustration is not drawn to scale.

# 10 NTLXnnaa

## NTLX44AA through NTLX99BA

# NTLX44AA Sync Resource Module

## Product description

### Overview

The NTLX44AA Sync Resource Module (SRM) provides a timing and synchronization interface for the Spectrum Peripheral Module (SPM). The SRM receives clocking information via DS1/E1 and 2048 MHz twisted pairs from a variety of sources. The SRM selects one of the input timing references and using Direct Digital Synthesis (DDS) techniques, creates a duplicated 8 KHz output reference signal, to Stratum 3E level accuracy. The output reference signal is tracked to each Common Equipment Module (CEM) in the SPM frame. The CEM will message the phase information up to the DMS Message Switch, which will in turn distribute a synchronized clock to the rest of the system, including the SPM.

.The principal functions of the Sync Resource Module are to

- Provide an interface to a Stratum 1 clock source, generally provided by a Timing Signal Generator.
- Using Direct Digital Synthesis (DDS) technology, create an 8 KHz frame signal that is frequency and phase locked to a selected input timing source. The timing source is tracked to Stratum 3E accuracy.
- Transmit the 8 KHz frame signal to the CEM via the backplane
- Support three different formats of timing signal: T1 (1.544 Mbps), E1 (2.048 Mbps) and 2.048 MHz clock
- Accept T1/E1 input from up to 4 distinct sources.
- Provide 2 separate T1/E1 outputs.
- Accept 2.048 MHz clock input from up to 3 distinct sources.
- Provide 2 separate 2.048 MHz clock outputs.
- Provide full flexibility for selecting a timing source from which to create the 8 KHz reference signal.

### Location

The SyncRM is installed in slot 6 of the Spectrum backplane.

## Functional description

The Sync RM has the following features:

- Interfaces to three Spectrum S-links, providing a control interface to the CEM.
- Embedded PowerQUICC II integrated processor with 100 MHz EC603e microprocessor core

## NTLX44AA Sync Resource Module (continued)

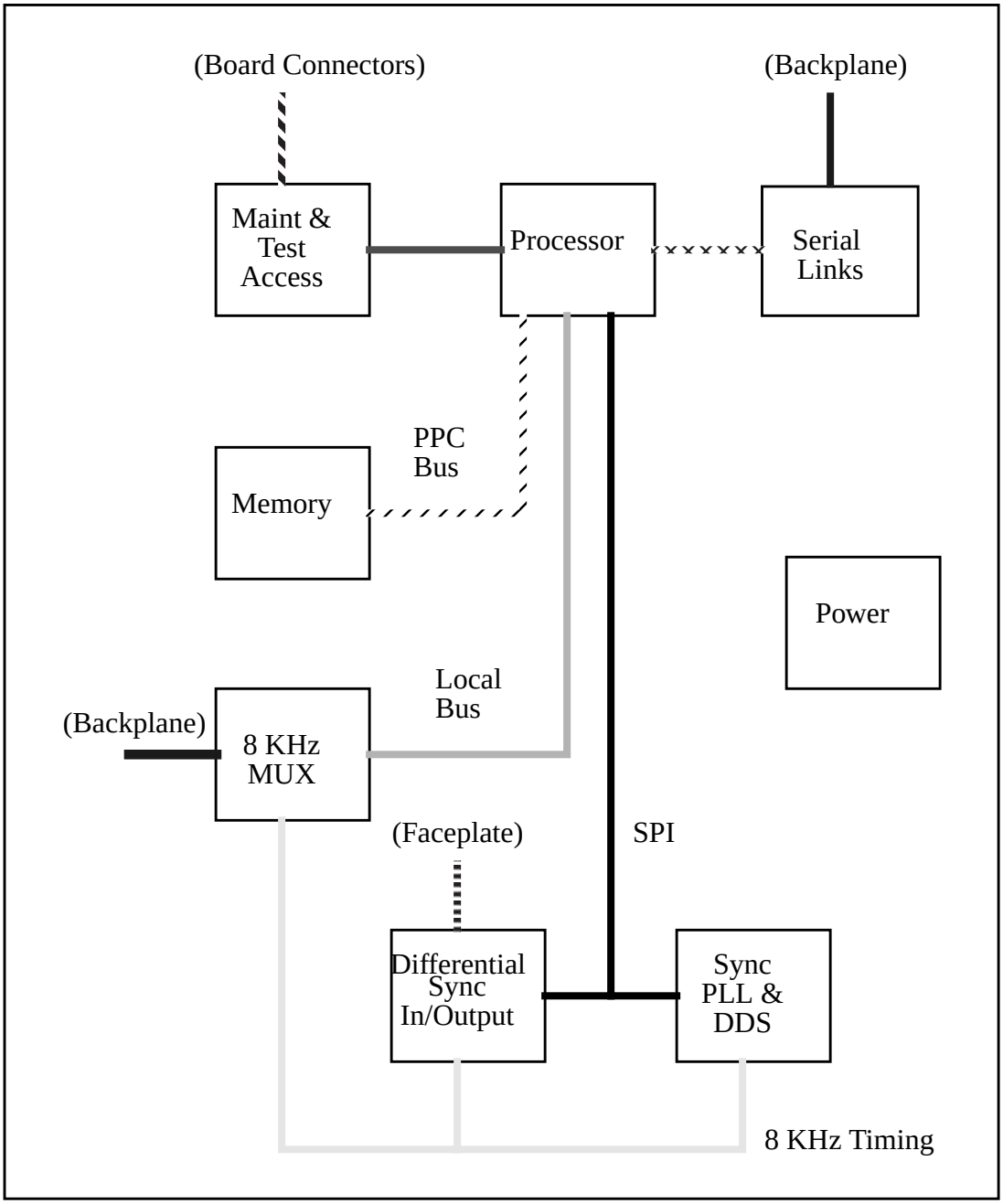
- Industry-standard faceplate RJ-45 10/100 Mbps Ethernet interface to processor (presently for debug use only).
- Industry-standard faceplate infrared IrDA interface to processor (presently unsupported).
- Separate faceplate connector for clock monitor and debug.
- OEM module set to implement synchronization functionality.
- 32 MBytes of on board synchronous DRAM - expandable to 64/128 MBytes.
- 16 MBytes of Flash memory - expandable to 32 MBytes.
- On board Point-of-Use Power Supply (PUPS).

### Functional block diagram

The next diagram is an illustration of the functional block diagram of the Sync RM.

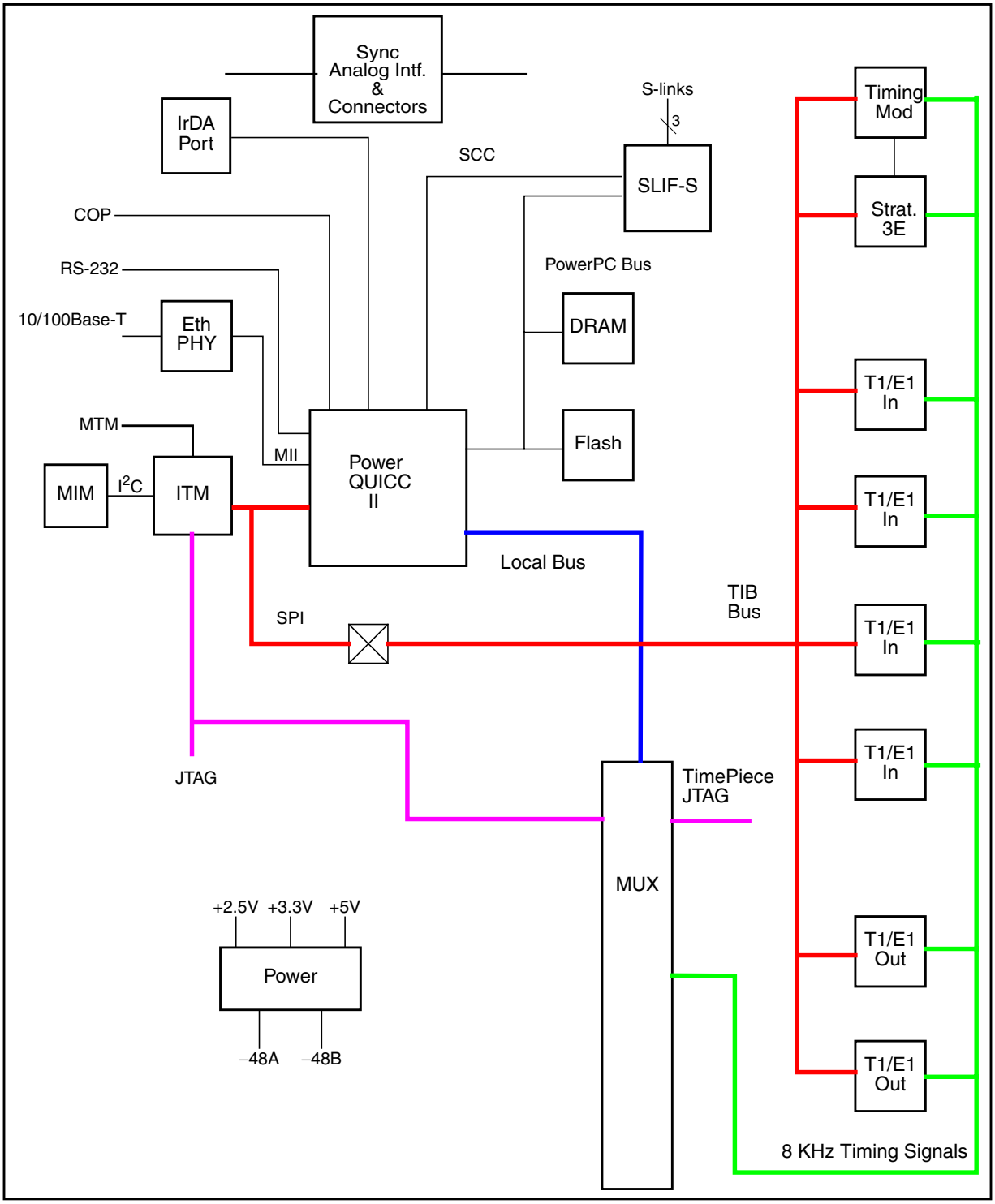
## NTLX44AA Sync Resource Module (continued)

**NTLX44AA functional block diagram (part 1)**



# NTLX44AA Sync Resource Module (continued)

### NTLX44AA functional block diagram (part 2)



## NTLX44AA Sync Resource Module (continued)

### Functional block descriptions

This section contains descriptive information pertaining to the functional blocks of the Sync RM.

**PowerQUICC II (Voyager) Processor Complex** The Processor provides the local intelligence to perform basic module control and maintenance activities. It configures and supervises the clock synchronization circuitry, executes diagnostic routines to test module circuitry, stores the Initial Boot Loader (IBL) and the application software load in non-volatile memory, and supports 10/100 Mbps Ethernet, RS-232 and IrDA interfaces for development, debug and monitoring purposes.

The Motorola PowerQUICC II is a high performance integrated communications processor which implements all of the host processing as well as the communications and supervisory functions required on the Sync resource module, all within a single device.

A 32 Mbyte bank of synchronous DRAM (expandable to 64/128 MB) provides program storage for the processor as well as message data buffer and descriptor memory

16 Mbytes of Flash memory (expandable to 32 MB) provides non-volatile storage of boot code as well as an image of the application code.

The processor communicates with the SDRAM, Flash and Slif-S device via the PowerPC bus. The memory controller within the PowerQUICC II controls all external bus cycles to the various types of memory devices, including row/column address multiplexing to DRAM. Since there are few devices on this bus, no buffering is used, and the bus is connected directly to each device.

The processor controls the sync frame pulse multiplexer array via the local bus. There are two 32-bit read/writeable registers, which provide 64 control bits which are used for various purposes.

**Serial Link Interface** Between each CEM and the SyncRM there are three S-Links. This group of three S-Links is referred to as an S-Link cluster. It is associated with a transmit and a receive clock signal, which is used to recover the timing information for the three links. One Slave S-Link Interface (SLIF-S) ASIC is responsible for the physical interface. The SLIF-S performs the following functions, not all of which are used in this application:

- recovers data from the S-Links from both CEM modules
- monitors link health by way of a CRC check
- extracts DMSW messaging channels from both CEM modules

## NTLX44AA Sync Resource Module (continued)

- selects PCM data from the CEMs, based on CEM activity; a small elastic store function is supplied to accommodate phase variations between the CEMs
- formats the selected data stream into a parallel bus for access by the resources supplied by the RM
- broadcasts outgoing PCM data to both CEMs
- inserts link CRC
- provides facilities for low level link as well as RM control and status facilities, including test and ID storage

Three S-Links, 1 primary + 2 secondary, are connected between a SLIF-S and each of the two CEMs. Logically, each S-Link consists of 8 groups of 32 channels each (a total of 256 timeslots). On group 0 of the primary S-Link, channels 0 and 31 are reserved for framing and operations, respectively, and channels 1-30 are used as a single high-speed DMSW messaging link. The remaining groups on the primary link, as well as all timeslots on the secondary links, are used for payload data. Each S-Link channel contains twelve bits, of which one is a spoiler (framing) bit, one is an out-of-band (OOB) channel bit, eight carry traffic (speech or data), one is a utility bit, and one bit is a parity check bit. The spoiler and OOB bits are terminated by the SLIF-S.

The SLIF-S is controlled by the PQII via the PowerPC bus. It has an 8-bit address and data interface. Messaging extracted from the primary S-link is transferred to the PQII via an SCC port. Messaging destined for the CEM is transferred to the SLIF-S from the PQII via the SCC port, then sent up to the CEM on the primary S-link. The CEM may also communicate with the SyncRM directly using the S-link Register Access protocol to activate an interrupt into the PQII. Since the S-link interface between the SyncRM is used only for messaging and clock synchronization, the PCM data interface is unused; the PDO and PDI busses are left unconnected.

**Sync Generation and Reference Selection** The main function of the SyncRM is to create a frame pulse that is synchronized to an external reference source, usually of Stratum 1 quality. This frame pulse is transmitted to both CEMs via the Spectrum backplane. The synchronization task is performed by a set of four OEM surface-mount modules, “TimePieces”: the DS1/E1 Input Module, the DS1/E1 Output module, the Stratum 3E Oscillator Module and the SmartTiming Module. Each of these devices comprise a processor with its own clocking and support circuits, embedded firmware, and special-purpose circuitry required by particular applications.

There are four DS1/E1 Input Modules used on the SyncRM. Each takes a twisted-pair input from the faceplate and outputs an 8KHz recovered frame

## NTLX44AA Sync Resource Module (continued)

pulse. The input signal should be 1.544 Mbps DS1. The input is optimized to a line termination of 110 ohm. It is expected (though not required) that the DS1 Input Modules will be connected to inputs from two separate BITS clocks and a monitor/test input. There are two 8 KHz reference inputs to each DS1 Input Module. The device will compile statistics on the input signal, using each of the reference inputs. The following measurements are performed by the internal processor: Maximum Time-Interval Error (MTIE), Time Deviation, Frequency offset and Phase history.

This data is stored in internal memory. In addition, performance monitoring of standard line conditions is provided: LOS, AIS, OOF, BPV and CRC. Sync Status Messaging (SSM) will be extracted if available in the input data stream. Each DS1 Input Module also terminates a 2.048 MHz square wave clock signal, that is input from the faceplate. Since the 2.048 MHz clock arrives at the faceplate as a differential signal, and the input to the DS1 Input Module is single-ended, the clock must go through differential-to-single-ended conversion (in addition to the analog conditioning described above). Since there are four DS1 Input Module on the SyncRM, one will not terminate a 2.048 MHz clock input.

There are two DS1 Output Modules used on the SyncRM. Each takes one of two 8KHz input frame pulses and produces a differential output in either 2.048 Mbps E1 format or 1.544 Mbps DS1 format, that is locked to the selected input reference. After passing through transient suppression diodes, transformer, and EMI chokes, the signal is output on twisted-pair wiring at the faceplate. The output is a frame, all-ones signal. For DS1, both SF and ESF formats are supported. For E1, CAS and CCS formats are supported. Sync Status Messaging (SSM) may be output in either signalling format.

The Stratum 3E Oscillator module provides a temperature-compensated 10 MHz output oscillator signal to the Timing module, that is accurate to the Stratum 3E level. The Timing module has five 8 KHz reference inputs, one of which will be selected as input to the Direct Digital Synthesizer (DDS), and used in conjunction with the 10 MHz oscillator to create an 8 KHz output frame pulse that is locked to the selected input with Stratum 3E accuracy. Phase Build-Out (PBO) is performed by the Timing Module.

Direct Digital Synthesis is a phase locking technique that enables output frequency resolution that is far higher than that obtainable from a traditional analog DAC-VCXO circuit. In its simplest case, a DDS can be made from an address counter, a PROM that contains amplitude values of a complete sinewave, a DAC, and a clock.

## NTLX44AA Sync Resource Module (continued)

As discussed above, 8 KHz reference inputs are used by the Timing Module to create its phase-locked output frame pulse. Selection of which of the 5 inputs are used as the reference source may be done “manually” by host S/W, or automatically by the Timing module itself. In automatic mode, the Timing module will examine its inputs sequentially, and choose the first one whose performance statistics indicates that it is stable and operating correctly. Reference inputs are also used by the Input modules to analyze their received signals, and by the Output modules to create an output signal.

If the Input module detects errors in the input signal with only one of its reference inputs, the assumption is that the reference input is bad. If the Input module detects errors in the input signal simultaneously with both of its reference inputs, the assumption is that the input signal is bad. Using its selected reference source, the Timing module performs frequency and stability measurements on the other 4 inputs. If any of the other inputs is too noisy, or exhibits excessive frequency deviation, the Timing module will eliminate it as a candidate reference source. If all the other inputs suddenly develop problems, then the assumption might be that the selected reference source has deteriorated.

The TimePieces communicate amongst themselves, and with the PQII host processor, by means of an SPI bus, that runs the TIB protocol stack. The TimePiece family shares a set of common commands. Each TimePiece also has a set of commands that relate to its specific functionality. Communication is one-way only, meaning that when a TimePiece has something to say to another TimePiece or to the host, it will master the bus and transmit the information. When TimePieces operate as slaves, they only listen to the master, and they do not transmit any data of their own. On system initialization, the TimePieces negotiate with each other (and with the host) to obtain network IDs, which are subsequently used to identify individual TimePieces in the system.

Each TimePiece also has a unique hardware chip ID, that depends on its PCB location. The chip ID allows a mapping between logical (network ID) devices and actual physical components, in systems where there is more than one instance of a particular type of device, such as the SyncRM. The host PQII must participate on the SPI bus with the TimePieces, as well as control the ITM. Since the ITM is incompatible with a SPI multimaster environment, the portion of the SPI bus that is connected to the ITM is electrically isolated from the TimePieces. When the PQII requires an ITM access, it momentarily shuts itself off from the TimePieces, services the ITM, then restores itself on the TimePiece portion of the SPI bus.

## NTLX44AA Sync Resource Module (continued)

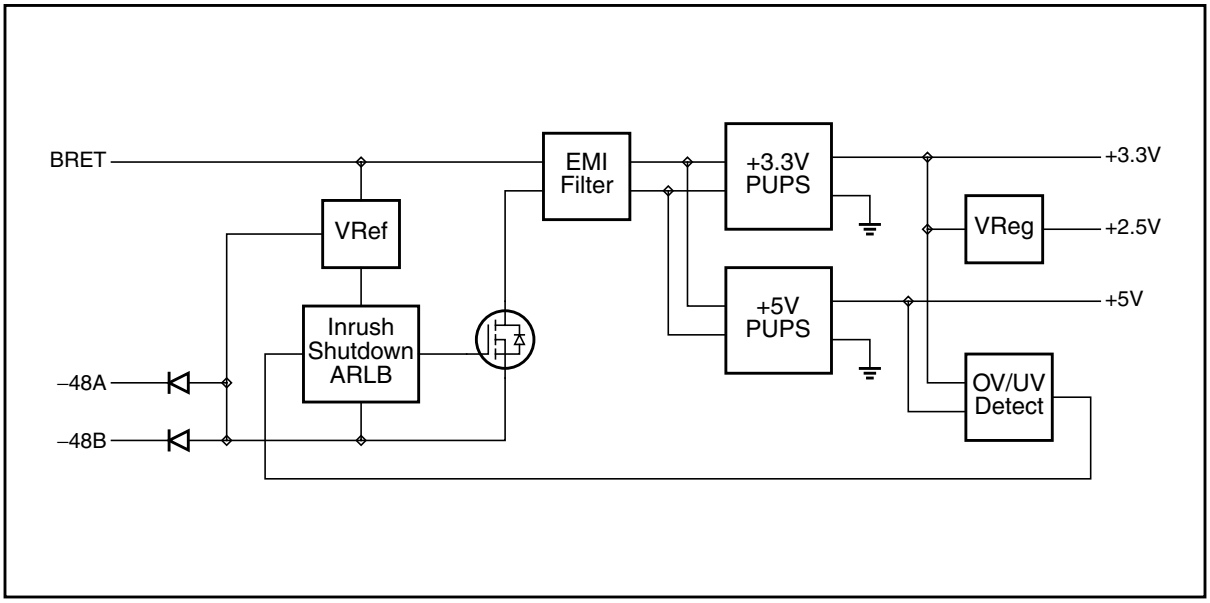
**Power Supply** Two DC-to-DC point-of-use power supplies (PUPS) will be used to convert the –48V A and B feeds to the +3.3V and +5V supply rails required for the Sync RM circuitry. In addition, a linear regulator will provide a +2V supply from the +3.3V supply in order to power the PowerQUICC II processor core. This +2V output will vary with the version of the PQII and will initially be +2.5V. This will be reduced to +2.3V, +2.0V and/or +1.8V depending on the recommendations from Motorola. The lowest voltage possible will be used to reduce power consumption while maintaining needed operating frequencies.

The shelf A and B feeds are diode ORed together to supply a fused input to the power circuit, allowing the resource module to operate with either or both of the shelf supplies. A fuse in each power feed, before the diode OR circuit, was not chosen because of problems in detecting a blown fuse in a single feed. If only one of the two fuses were to blow, it is possible an RM could be inadvertently shut down during routine maintenance procedures (by powering down one of the two feeds). The diodes used are special for this application, and are designed to fail in an open state and not catch on fire. Also, special provisions are made in circuit board layout to reduce the risk of shorts occurring before the fuse.

In-rush current protection, automatic return from low battery (ARLB), and shutdown circuitry controls a power MOSFET switch for the diode ORed –48V battery feed. Battery and return are filtered to reduce electro-magnetic interference (EMI) and then supply the input to the PUPS. Overvoltage and undervoltage conditions on both +5V and +3.3V PUPS outputs are monitored for and will cause a shutdown of the power supply circuit if detected. The battery supply must be cycled off and back on in order to reset the shutdown circuit and re-enable the PUPS. The next illustration is a diagram of the power supply.

## NTLX44AA Sync Resource Module (continued)

**Power supply**




Included in the Power block is a power monitor function. This circuit monitors the +5V, +3.3V and +2.5V voltages and asserts a single reset pulse to the SyncRM if any voltage drops below the following limits:

- 2.3V (max) for the +2.5V supply
- 3.0V for the +3.3V supply
- 4.75V for the +5V supply

The reset pulse duration is 140msec.

## Pin description

The next table contains the pin description information for the Sync RM.

### Backplane Pin Description

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P4:8A | -48A | Supply | -48 volt battery feed A |
| P4:8B | | | |
| P4:8C | | | |
| P4:8D | | | |
| P4:8E | | | |
| P4:2A | -48B | Supply | -48 volt battery feed B |
| P4:2B | | | |
| P4:2C | | | |
| P4:2D | | | |
| P4:2E | | | |
| P4:5A | RTN | Supply | Battery return (ground) |
| P4:5B | | | |
| P4:5C | | | |
| P4:5D | | | |
| P4:5E | | | |
| P3:10B | FrCEM0_CK0 | Input | S-Link clock lines from the CEMs |
| P3:10D | FrCEM1_CK0 | | |
| P3:9B | FrCEM0_D0 | Input | S-Link data lines from the CEMs |
| P3:9D | FrCEM1_D0 | | |
| P3:9A | FrCEM0_D1 | | |
| P3:9E | FrCEM1_D1 | | |
| P3:10A | FrCEM0_D2 | | |
| P3:10E | FrCEM1_D2 | | |
| P3:8B | ToCEM0_CK0 | Output | S-Link clock lines to the CEMs |
| P3:8D | ToCEM1_CK0 | | |

## NTLX44AA Sync Resource Module (continued)

### Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P3:7B | ToCEM0_D0 | Output | S-Link data lines to the CEMs |
| P3:7D | ToCEM1_D0 | | |
| P3:7A | ToCEM0_D1 | | |
| P3:7E | ToCEM1_D1 | | |
| P3:8A | ToCEM0_D2 | | |
| P3:8E | ToCEM1_D2 | | |
| P3:2A | SYNC_ToCEM0 | Output | Sync RM recovered frame pulse, used by CEM for synchronization. |
| P3:3A | SYNC_ToCEM1 | | |
| P3:18A | MMD | Input | MTM bus master data |
| P3:18E | MSD | Output | MTM bus slave data |
| P3:17D | MCLK | Input | MTM bus clock |
| P3:17B | MPR | Output | MTM bus pause request |
| P3:16C | MCTL | Input | MTM bus control |

## NTLX44AA Sync Resource Module (continued)

### Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P3:16E | SLOT_ID0 | Input | Physical slot identification |
| P3:16D | SLOT_ID1 | | |
| P3:17C | SLOT_ID2 | | |
| P3:16B | SLOT_ID3 | | |
| P3:16A | SLOT_ID4 | | |

## NTLX44AA Sync Resource Module (continued)

### Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P3:2B | LGND | Supply | Logic ground |
| P3:2C | | | |
| P3:2D | | | |
| P3:3C | | | |
| P3:4A | | | |
| P3:4B | | | |
| P3:4C | | | |
| P3:4D | | | |
| P3:4E | | | |
| P3:5C | | | |
| P3:6C | | | |
| P3:7C | | | |
| P3:8C | | | |
| P3:9C | | | |
| P3:10C | | | |
| P3:11A | | | |
| P3:11B | | | |
| P3:11C | | | |
| P3:11D | | | |
| P3:11E | | | |
| P3:12C | | | |
| P3:13C | | | |
| P3:14C | | | |
| P3:15C | | | |
| P3:18B | | | |
| P3:18C | | | |
| P3:18D | | | |

## NTLX44AA Sync Resource Module (continued)

The next table contains backplane connector P4 information.

### Backplane connector P4

| Pin no. | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | -48B | -48B | -48B | -48B | -48B |
| 3 | NC | NC | NC | NC | NC |
| 4 | NC | NC | NC | NC | NC |
| 5 | RTN | RTN | RTN | RTN | RTN |
| 6 | NC | NC | NC | NC | NC |
| 7 | NC | NC | NC | NC | NC |
| 8 | -48A | -48A | -48A | -48A | -48A |

The next table contains backplane connector P3 information.

### Backplane connector P3

| Pin no. | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | SYNC_ToCEM0 | LGND | LGND | LGND | NC |
| 3 | SYNC_ToCEM1 | NC | LGND | NC | NC |
| 4 | LGND | LGND | LGND | LGND | LGND |
| 5 | NC | NC | LGND | NC | NC |
| 6 | NC | NC | LGND | NC | NC |
| 7 | ToCEM0_D1 | ToCEM0_D0 | LGND | ToCEM1_D0 | ToCEM1_D1 |
| 8 | ToCEM0_D2 | ToCEM0_CK0 | LGND | ToCEM1_CK0 | ToCEM1_D2 |
| 9 | FrCEM0_D1 | FrCEM0_D0 | LGND | FrCEM1_D0 | FrCEM1_D1 |
| 10 | FrCEM0_D2 | FrCEM0_CK0 | LGND | FrCEM1_CK0 | FrCEM1_D2 |
| 11 | LGND | LGND | LGND | LGND | LGND |
| 12 | NC | NC | LGND | NC | NC |
| 13 | NC | NC | LGND | NC | NC |

## NTLX44AA Sync Resource Module (continued)

### Backplane connector P3 (Continued)

| Pin no. | A | B | C | D | E |
|---|---|---|---|---|---|
| 14 | NC | NC | LGND | NC | NC |
| 15 | NC | NC | LGND | NC | NC |
| 16 | SLOT_ID4 | SLOT_ID3 | MCTL | SLOT_ID1 | SLOT_ID0 |
| 17 | LGND | MPR | SLOT_ID2 | MCLK | LGND |
| 18 | MMD | LGND | LGND | LGND | MSD |

The next table contains ethernet faceplate connector information.

### Ethernet faceplate connector

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| J3:1<br>J3:2 | TX+<br>TX– | Output | Twisted-pair Transmit |
| J3:3<br>J3:6 | RX+<br>RX– | Input | Twisted-pair Receive |

The next table contains interface faceplate connection information.

### Sync interface faceplate connections

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P1.1 | BITX_OT | Output | T1/E1 Crossover differential output tip |
| P1.2 | BITX_OR | Output | T1/E1 Crossover differential output ring |
| P1.3 | BITX_INT | Input | T1/E1 Crossover differential input tip |
| P1.4 | BITX_INR | Input | T1/E1 Crossover differential input ring |
| P1.5 | CDMA_INT | Input | Secondary T1/E1 BITS (or CDMA) differential input tip |

## NTLX44AA Sync Resource Module (continued)

### Sync interface faceplate connections (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P1.10 | CDMA_INR | Input | Secondary T1/E1 BITS (or CDMA) differential input ring |
| P1.9 | BITS_INT | Input | T1/E1 BITS differential input tip |
| P1.8 | BITS_INR | Input | T1/E1 BITS differential input ring |
| P1.7 | 2MCKINT | Input | 2.048 MHz differential clock input tip |
| P1.6 | 2MCKINR | Input | 2.048 MHz differential clock input ring |
| P1.11 | 2MXCKINT | Input | 2.048 MHz crossover differential clock input tip |
| P1.12 | 2MXCKINR | Input | 2.048 MHz crossover differential clock input ring |
| P1.13 | 2MXOT | Output | 2.048 MHz crossover differential clock output tip |
| P1.14 | 2MXOR | Output | 2.048 MHz crossover differential clock output ring |
| P2.1 | 2MMONOT | Output | 2.048 MHz differential clock monitor output tip |
| P2.2 | 2MMONOR | Output | 2.048 MHz differential clock monitor output ring |
| P2.3 | 2MMONINT | Input | 2.048 MHz differential clock monitor input tip |
| P2.4 | 2MMONINR | Input | 2.048 MHz differential clock monitor input ring |

## NTLX44AA Sync Resource Module (continued)

### Sync interface faceplate connections (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P2.5 | BITM_INT | Input | T1/E1 differential monitor input tip |
| P2.9 | BITM_INR | Input | T1/E1 differential monitor input ring |
| P2.7 | BITM_OT | Output | T1/E1 differential monitor output tip |
| P2.8 | BITM_OR | Output | T1/E1 differential monitor output ring |

## 10/100BaseT Ethernet Interface

The SyncRM supports a 10/100BaseT Ethernet interface, accessible via RJ-45 connector on the faceplate. The Ethernet PHY device is connected to the Fast Communications Controller 1 (FCC1) port on the PQII. This port is set up to provide a standard Media Independent Interface (MII), supporting bit rates up to 100 Mbps. A set of LEDs (not visible from the faceplate) provide status indications for Ethernet operation.

## Interface specifications

### Faceplate Visual Indicators

The Sync Resource Module will carry a set of indicators to provide information of interest to craft personnel. The LEDs, which are located at the faceplate, indicate the current state of the module.

**Faceplate LED indicators**

| Green | Red | Module state |
|---|---|---|
| Off | Off | Sleep, un-powered or not inserted |
| On | On | Power up LED test |
| Wink | Off | Power up self-test underway |
| On | Off | Module should not be removed |
| Off | On | Alarm state: module may be removed |

Power up LED test is entered immediately after the module is first powered up or inserted. Its purpose is to allow craft personnel to verify that the LEDs are

functional. The LEDs remain in this state for the duration of the power-up self-test.

Alarm State is entered during a power up or insertion sequence if the self-test fails, or if the Common Equipment Module rejects the module as being unworkable in the system due to incompatibilities or a failure to establish communications with the module.

The Green ON, Red OFF state is entered during power up or insertion sequence when the module has passed its diagnostic test. In this case, the module should not be removed.

### Sleep mode

When not required, circuit module LEDs may enter a customer programmable "sleep" mode to extend their life. The LEDs will leave the sleep mode:

- when so directed by OAM S/W
- as a result of LED state change
- as part of an Indicator Test

The LEDs will not sleep while an alarm source is active (i.e. while there is a module in the peripheral in the RED ON, GREEN OFF state).

# NTLX44AA Sync Resource Module (end)

## Performance requirements

### Electrical specifications

The next two tables contain electrical specifications.

**Input characteristics**

| Parameter | Pin | Min. | Num. | Max. | Units | Comments |
|---|---|---|---|---|---|---|
| $C_I$ | | 3.5 | | 8 | pF | |
| $Z_I$ | | | | | MΩ | |
| $V_{IL}$ | | –0.5 | | 0.8 | Volts | |
| $V_{IH}$ | | 2.0 | | $V_{CC}$+0.5 | Volts | |
| $V_{IK}$ | | | –0.7 | –1.2 | Volts | Clamp diode |
| $I_{IL}$ | | | | 1 | µA | |
| $I_{IH}$ | | | | 1 | µA | |

**Output characteristics**

| Parameter | Pin | Min. | Num. | Max. | Units | Comments |
|---|---|---|---|---|---|---|
| $C_O$ | | | | | pF | |
| $V_{OL}$ | | | | | Volts | $I_{OL}$= |
| | | | | | | $I_{OL}$= |
| $V_{OH}$ | | | | | Volts | $I_{OH}$= |
| | | | | | | $I_{OH}$= |
| $I_{OL}$ | | | | | mA | |
| $I_{OH}$ | | | | | mA | |
| $I_{OZ}$ | | | | | µA | |

### Power requirements

The Sync Resource Module will utilize two Point-of-Use Power Supplies (PUPS) to convert –48V to 5V and 3.3V as required. Two independent –48V sources will be provided for redundancy. These will be diode-ORed within the SyncRM before being fed to the PUPS. 2.5V will be supplied from the 3.3V supply via a linear voltage regulator.

# NTLX71AA OC3 Interface Module

## Description

The NTLX71AA OC3 interface module is a synchronous optical network (SONET) OC3 trunk interface module for the DMS-Spectrum Peripheral Module (SPM). It allows the SPM to terminate SONET OC3 transmission systems carrying DS3, asynchronous VT1.5, and byte-synchronous VT1.5 payloads.

## Location

The NTLX71AA OC3 interface module occupies slots 9 and 10 on shelf 0 in NTLX51BA dual-shelf assembly.

## Functions

The NTLX71AA OC3 interface module provides the following services:

- SONET OC3 interface with DS3, floating asynchronous VT1.5, and floating byte synchronous VT1.5.
- SONET alarm support
- DS0 trunk conditioning support

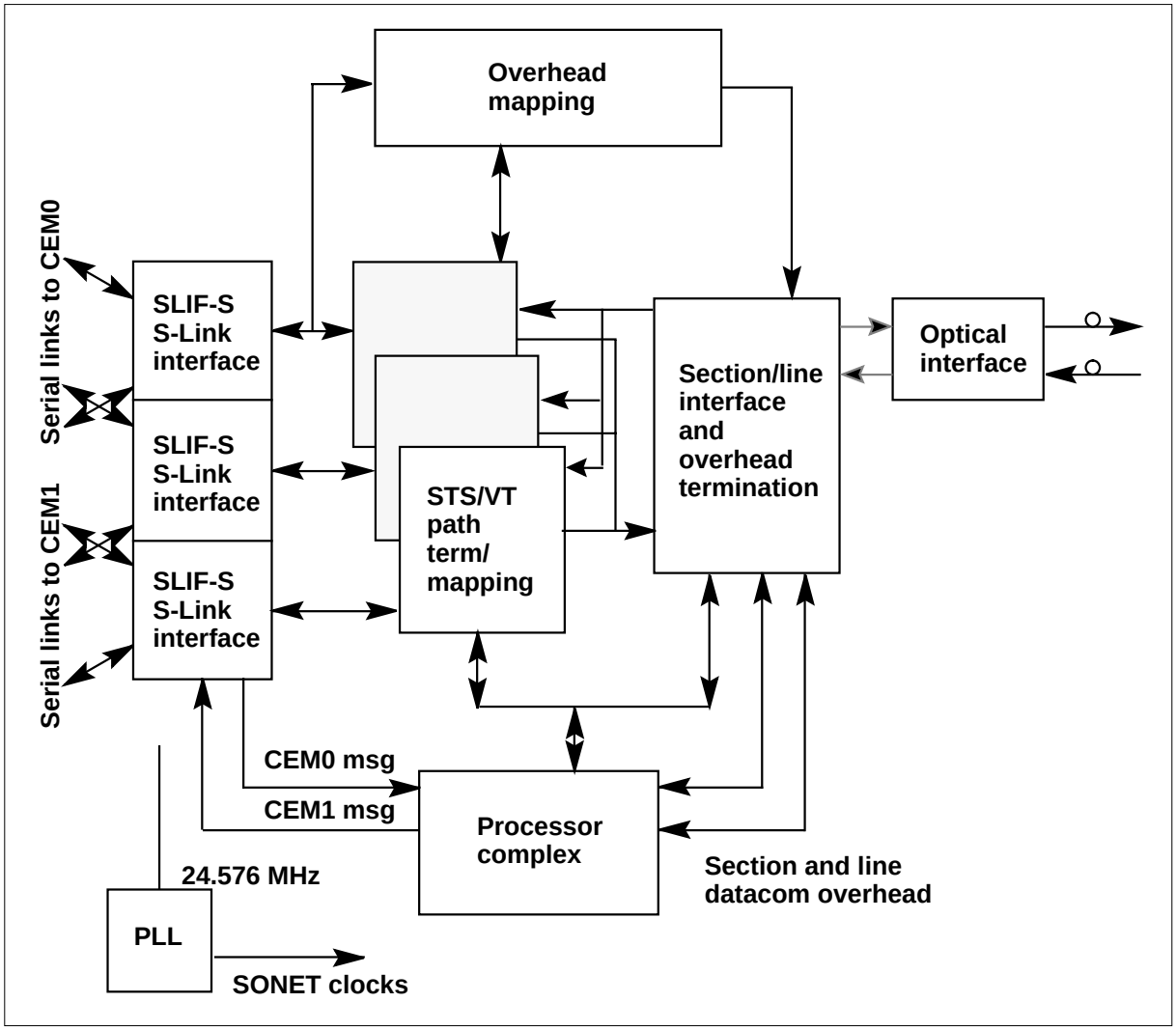
## Functional blocks

The NTLX71AA OC3 interface module has the following functional blocks:

- optical interface
- section/line interface
- STS/VT path termination and mapping
- processor platform
- overhead mapping
- S-link interface
- phase lock loop

The next figure shows the NTLX71AA OC3 interface module functional block diagram.

## NTLX71AA OC3 Interface Module (continued)




### Optical interface

The NTLX71AA OC3 interface module provides an intermediate- and a long-reach OC3 optical transceiver (155.52 Mbyte/s) to terminate the physical fiber. The NTLX71AA converts the signal to an electrical format and forwards the signal to the section/line interface.

The laser output of the transmit electro-optical module can be disabled for safety during diagnostics. In addition, it is monitored for laser bias and optical output power output. The receive module provides low light and received power indications.

## NTLX71AA OC3 Interface Module (continued)

The following tables list the optical interface specifications for the OC3 interface module.

| **OC3 optical interface circuit pack specifications** | | |
|---|---|---|
| **Parameter (see Note 1 and Note 2)** | **1310 nm Intermediate reach** | **1310 nm Long reach** |
| Product engineering code | NT7E01DA/DB/DC/DD | NT7E01CA/CB/CC/CD |
| Connector type (see Note 3) | Biconic, FC-PC, ST/PC, SC | Biconic, FC-PC, ST/PC, SC |
| Pigtaill | Single mode | |
| General fiber type | Single mode | Single mode |
| Class of fiber | 9.5 mm | Single mode |
| Mode-field diameter | | 9.5 mm |
| Optical source | | |
| Device type | MLM | MLM |
| Material composition | GaAs | GaAs |
| Spectral characteristics | | |
| Central wavelength | 1310 nm | 1310 nm |
| Spectral width | 5 nm (D1MSTM) | 5 nm (D1MSTM) |
| Spectral width | 7.7 nm (D1RMS) | 7.7 nm (D1RMS) |
| Central wavelength range | 1260-1360 nm | 1280-1335 nm |
| Optical signal | | |
| LIne rate | OC3 (155.52 Mb/s) | OC3 (155.52 Mb/s) |
| Line code | NRZ | NRZ |
| Extinction ratio | 8.2 dB | 10 dB |
| Optical Power | | |
| Guaranteed launch power | -15 dBm | -5.0 dBm |
| Maximum launch power | -8 dBm | 0 dBm |

***Note 1:*** All parameters apply on the line side of the optical connector, as specified in Bellcore Specifications TR-NWT-000253, Issue 2.

***Note 2:*** All parameters are valid over the full range of operating, environmental, and aging conditions.

***Note 3:*** All parameters are valid for each of the appropriate connector options.

## NTLX71AA OC3 Interface Module (continued)

| **OC3 optical interface receiver specifications** | | |
|---|---|---|
| **Parameter (See Note 1)** | **1310 nm Intermediate reach** | **1310 nm Long reach** |
| Product engineering code | NT7E01DA/DB/DC/DD | NT7301CA/CB/CD |
| Connector type | Biconic, FC-PC, ST/PC, SC | Biconic, FC-PC, ST/PC, SC |
| Pigtail | | |
| General fiber type | Multimode | Multimode |
| Optical detector | | |
| Device type | PIN | APD |
| Material composition | InGaAs | III-V |
| Spectral characteristics | | |
| Central wavelength | 1265-1355 nm | 1280-1335 nm |
| Optical signal | | |
| Line rate | OC3 (155.52 Mb/s) | OC3 (155.52 Mb/s) |
| Line code | NRZ | NRZ |
| Overload level (See Note 2) | -8.0 dBm | -10.0 dBm |
| Damage level (See Note 3) | N/A | -6.0 dBm |
| Maximum receiver reflectance | -14.0 dB | -14.0 dB |
| Optical path penalty (See Note 4) | 1.0 dB | 1.0 dB |
| Optical power | | |
| Guaranteed receiver sensitivity | -28.0 dBm | -34.0 dBm |

***Note 1:*** These specifications are worst-case parameters that include allowances for connector losses, aging, equipment impairments because of implementation, and temperature degradation. The values represent the power level measure at the station fiber on the link side of the connector.

***Note 2:*** Miniature variable optical attenuators (mVOAs) may be required at the receiver depending on the link loss. Overload level is the maximum received optical power for which BER of 10-*10* and all jitter tolerance specifications are met.

***Note 3:*** The damage level is the maximum optical power for which no long term damage to the components will occur.

***Note 4:*** The optical path penalty includes degradations in performance due to dispersions, reflections and optical jitter consistent with the requirements of Bellcore Specification TA-NWT-000253, Issue 2.

## NTLX71AA OC3 Interface Module (continued)

| OC3 optical interface guaranteed system gain specifications | | |
|---|---|---|
| **Parameter (See Note)** | **1310 nm Intermediate reach** | **1310 nm Long reach** |
| Product engineering code | NT7E01DA/DB/DC/DD | NT7E01CA/CB/CC/CD |
| Attenuation | 0 to 12 dB | 10 to 28 dB |
| Optical return loss | 14 dB | 24 dB |
| Dispersion | 96 ps/nm | 185 ps/nm |
| Guaranteed launch power | -15 dBm | -5.0 dBm |
| Maximum transmit power | -8.0 dBm | 0.0 dBm |
| Receiver sensitivity | -28.0 dBm | -34.0 dBm |
| Maximum receiver power | -8.0 dBm | -10.0 dBm |
| Receiver damage level | N/A | N/A |
| Guaranteed system gain | 13.0 dB | 29.0 dB |

***Note:*** These specifications are worst-case parameters that include connector losses, aging, equipment impairments because of implementation, and temperature degradation. These specifications do not include the customer unallocated link margin or the optical path penalty.

### Section/line interface

The section/line interface accepts the electrical signals from the NTLX71AA OC3 interface module and handles the overhead termination through the PMC-Sierra PM5344. The PM5344 handles line defect detection, performance related overhead, protection switching overhead, and alarms.

SONET overhead not handled by the PM5343 is routed to the overhead mapping functions for additional processing.

### Synchronous transport signal (STS)/virtual tributary (VT) path termination and mapping

#### STS termination and mapping

The STS path is terminated by the PCM-Sierra PM5344, which handles the STS pointer processing and overhead termination.

Received data is provided on the drop side of the telecom bus, along with synchronous payload envelope (SPE) and alignment indication (C1J1).

In the transmit direction, the PM5344 accepts the Add side of the telecom bus from the VT and DS3 mappers.

## NTLX71AA OC3 Interface Module (continued)

### DS1/VT termination

The three SPEs and constituent DS3 and VT1.5 structures are handled in the VT path termination and mapping section. Each of these mapping sections takes an SPE and maps the payload as DS3 or floating VT1.5. In the case of DS3, the L3M mapping device interfaces to the telecom bus and maps DS3 payloads according to SONET specifications. The DS3 signal is routed to and from an M13 multiplexing device as B3ZS signals, allowing path integrity checking. The M13 device maps 28 DS1s into a DS3 stream. The 28 DS1s are split into three groups of eight and a group of four and terminated on the octal mapping resource (OMaR) application specific integrated circuit (ASIC). Each DS1 interfaces to the M13 as a separate signal group consisting of transmit data and clock with received data and clock.

For floating VT1.5 mapped DS1 signals in the SPE, the OMaR devices interface to the demultiplexed telecom bus directly using the framing (AC1J1, DC1J1) and SPE indication signals (APL, DPL) to demultiplex the VT1.5s within the payload. Selection pins on these devices are used by the VT1.5 mappers to determine which VT1.5 payloads to handle. One OMar on each SPE is designated the master and determines and distributes SPE framing information in the transmit direction.

### SLIF-S S-link interface

Before presentation to the STS mapping and DS1/VT termination section, the telecom bus is split into three 6.48 MHz buses, each representing a single STS-1 in the STS-3 envelope. This improves signal fan-out and lowers power usage and electromagnetic emissions.

### Computing platform

The local processor on the NTLX71AA OC3 interface module contains four built-in serial communication controllers, DRAM, interfaces, timers, direct memory access controllers, and four Mbytes of flash electrically-erasable, programmable ROM and DRAM are provided.

## Signaling

The following table shows the NTLX71AA OC3 interface module connector J1 (1SU) - power pinouts.

| Pin number | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | -48B | -48B | -48B | -48B | -48B |
| 3 | NC | NC | NC | NC | NC |
| 4 | NC | NC | NC | NC | NC |

## NTLX71AA OC3 Interface Module (continued)

| Pin number | A | B | C | D | E |
|---|---|---|---|---|---|
| 5 | RTN | RTN | RTN | RTN | RTN |
| 6 | NC | NC | NC | NC | NC |
| 7 | NC | NC | NC | NC | NC |
| 8 | -48A | -48A | -48A | -48A | -48A |

The following table shows the NTLX71AA OC3 interface module connector J2 (2SU) - resource module (RM) common pinouts.

| Pin number | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | SYNC_ToCEM0 | LGND | LGND | LGND | SYNC_FrOC30 |
| 3 | SYNC_ToCEM1 | .NC. | LGND | .NC. | SYNC_FrOC31 |
| 4 | LGND | LGND | LGND | LGND | LGND |
| 5 | .NC. | .NC. | LGND | .NC. | .NC. |
| 6 | .NC. | .NC. | LGND | .NC. | .NC. |
| 7 | ToCEM0_D2 | ToCEM0_D1 | LGND | ToCEM1_D1 | ToCEM1_D2 |
| 8 | ToCEM0_D3 | ToCEM0_CK | LGND | ToCEM1_CK | ToCEM1_D3 |
| 9 | FrCEM0_D2 | FrCEM0_D1 | LGND | FrCEM1_D1 | FrCEM1_D2 |
| 10 | FrCEM0_D3 | FrCEM0_CK | LGND | FrCEM1_CK | FrCEM1_D3 |
| 11 | LGND | LGND | LGND | LGND | LGND |
| 12 | .NC. | .NC. | LGND | .NC. | .NC. |
| 13 | .NC. | .NC. | LGND | .NC. | .NC. |
| 14 | .NC. | .NC. | LGND | .NC. | .NC. |
| 15 | .NC. | .NC. | LGND | .NC. | .NC. |
| 16 | SLOT_ID4 | SLOT_ID3 | MCTL | SLOT_ID1 | SLOT_ID0 |
| 17 | LGND | MPR | SLOT_ID2 | MCLK | LGND |
| 18 | MMD | LGND | LGND | LGND | MSD |

## NTLX71AA OC3 Interface Module (continued)

The following table shows the NTLX71AA OC3 interface module connector J2 (2SU) - extra S-link pinouts.

| Pin number | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | LGND | LGND | LGND | LGND | LGND |
| 3 | .NC. | .NC. | LGND | .NC. | .NC. |
| 4 | .NC. | .NC. | LGND | .NC. | .NC. |
| 5 | .NC. | .NC. | LGND | .NC. | .NC. |
| 6 | LGND | LGND | LGND | LGND | LGND |
| 7 | LGND | LGND | LGND | LGND | LGND |
| 8 | LGND | LGND | LGND | LGND | LGND |
| 9 | ToCEM0_D8 | ToCEM0_D7 | LGND | ToCEM1_D7 | ToCEM1_D8 |
| 10 | ToCEM0_D9 | ToCEM0_CK3 | LGND | ToCEM1_CK3 | ToCEM1_D9 |
| 11 | FrCEM0_D8 | FrCEM0_D7 | LGND | FrCEM1_D7 | FrCEM1_D8 |
| 12 | FrCEM0_D9 | FrCEM0_CK3 | LGND | FrCEM1_CK3 | FrCEM1_D9 |
| 13 | LGND | LGND | LGND | LGND | LGND |
| 14 | ToCEM0_D5 | ToCEM0_D4 | LGND | ToCEM1_D4 | ToCEM1_D5 |
| 15 | ToCEM0_D6 | ToCEM0_CK2 | LGND | ToCEM1_CK2 | ToCEM1_D6 |
| 16 | FrCEM0_D5 | FrCEM0_D4 | LGND | FrCEM1_D4 | FrCEM1_D5 |
| 17 | FrCEM0_D6 | FrCEM0_CK2 | LGND | FrCEM1_CK2 | FrCEM1_D6 |
| 18 | LGND | LGND | LGND | LGND | LGND |

The following table shows the J4 OC-2 RM cross connector.

| Pin number | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | LGND | LGND | LGND | LGND | LGND |
| 3 | Drop0Data0 | Drop0Data1 | Add0Data2 | Add0Data1 | Add0Data0 |
| 4 | Drop0Data3 | Drop0Data4 | Drop0Data2 | Add0Data4 | Add0Data3 |

## NTLX71AA OC3 Interface Module (continued)

| Pin number | A | B | C | D | E |
|---|---|---|---|---|---|
| 5 | Drop0Data5 | Drop0Data6 | LGND | Add0Data6 | Add0Data5 |
| 6 | Drop0Data7 | DropSPE | LGND | Add0SPE | Add0Data7 |
| 7 | Drop0C1J1V1 | Drop0CLK | LGND | Add0CLK | Add0C1J1V1 |
| 8 | Drop0Parity | LGND | LGND | LGND | Add0Parity |
| 9 | LGND | .NC. | LGND | .NC. | LGND |
| 10 | .NC. | .NC. | .NC. | .NC. | .NC. |
| 11 | .NC. | .NC. | .NC. | .NC. | .NC. |
| 12 | .NC. | .NC. | LGND | .NC. | .NC. |
| 13 | .NC. | .NC. | LGND | .NC. | .NC. |
| 14 | .NC. | .NC. | LGND | .NC. | .NC. |
| 15 | LGND | LGND | LGND | LGND | LGND |
| 16 | SpTx0 | SpTx1 | LGND | SpRx1 | SpRx0 |
| 17 | SpTx2 | SpTx3 | LGND | SpRx3 | SpRx2 |
| 18 | LGND | LGND | LGND | LGND | LGND |

The following table shows the NTLX71AA OC3 interface module backplane pin descriptions.

| Connection number | Signal | Function | IO type | Description |
|---|---|---|---|---|
| J1 | -48B | power | | -48 V battery feed B |
| J1 | RET | power | | Battery return |
| J1 | -48A | power | | -48 V battery feed A |
| J2 | FrCEMnCKm | input | 3.3 V CMOSSLIF-S | S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1) |
| J2 | FrCEMnDm | input | 3.3 V CMOSSLIF-S | S-link data lines from common equipment (n = 0 CEM0,n = 1 CEM1) |

## NTLX71AA OC3 Interface Module (continued)

| Connection number | Signal | Function | IO type | Description |
|---|---|---|---|---|
| J2 | ToCEMnCKm | output | 3.3 V CMOSSLIF-S | S-link clock lines to common equipment (n = 0 CEM0,n = 1 CEM1) |
| J2 | ToCEMnDm | output | 3.3 V CMOSSLIF-S | S-link data lines to common equipment (n = 0 CEM0,n = 1 CEM1) n = 1, 2, 3 on J2 |
| J2 | SYNC_ToCEM0 SYNC_ToCEM0 SYNC_FrOC3SYNC_FrOC3 | output | 3.3 V TTL74LVT16244 | OC3 recovered frame pulse, used by CEM, or clock RM for synchronization |
| J2 | MMD | input | 3.3 V CMOSITM | JTAG 1149.5 bus master data |
| J2 | MSD | input/output open drain | 3.3 V CMOSITM | JTAG 1149.5 bus slave data |
| J2 | MCLK | input | 3.3 V CMOSITM | JTAG 1149.5 bus clock |
| J2 | MPR | input/outputo pen drain | 3.3 V CMOSITM | JTAG 1149.5 bus request |
| J2 | MCTL | input | 3.3 V CMOSITM | JTAG 1149.5 bus control |
| J2 | LGND | power | | logic ground of the PCP/BACKPLANE |
| J3 | FrCEMnCKm | input | 3.3 V CMOSSLIF-S | S-link clock lines from common equipment (n = 0 CEM0, n = 1 CEM1) m = 2, 3 on J3 |
| J3 | FrCEMnDm | input | 3.3 V CMOSSLIF-S | S-link data lines from common equipment (n = 0 CEM0,n = 1 CEM1) n = 4, 5, 6, 7, 8, 9 on J2 |
| J3 | ToCEMnCKm | output | 3.3 V CMOSSLIF-S | S-link clock lines to common equipment (n = 0 CEM0,n = 1 CEM1) m = 2, 3 on J3 |
| J3 | ToCEMnDm | output | 3.3 V CMOSSLIF-S | S-link data lines to common equipment (n = 0 CEM0,n = 1 CEM1) n = 4, 5, 6, 7, 8, 9 on J2 |

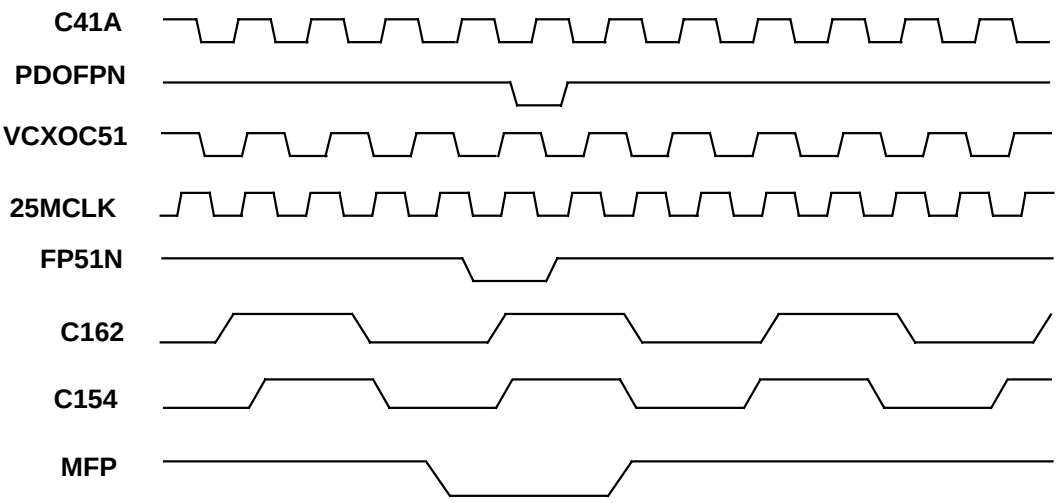
## NTLX71AA OC3 Interface Module (continued)

| Connection number | Signal | Function | IO type | Description |
|---|---|---|---|---|
| J3 | LGND | power | 3.3 V CMOSSLIF-S | Logic ground of the PCP/BACKPLANE |
| J4 | Drop0DatanDrop0C1J1Drop0PLDrop0PAR | output | 3.3 V TTL74LVT16244 | Enter OC3 resource module telecom bus DropODatan ranges from n = 0 to n = 7 |
| J4 | Add0DatanAdd0C1J1Add0PLAdd0PAR | input | 3.3 V TTL74LVT16244 | Enter OC3 resource module telecom bus Add0Datan ranges from n = 0 to n = 7 |
| J4 | LGND | power | | Logic ground of the PCP/BACKPLANE |

## Timing

The following figure shows the clock phase relationships for the NTLX71AA OC3 interface module.

## NTLX71AA OC3 Interface Module (end)




Legend:
C41A — 24.576 MHz system clock derived from the active CEM
PDOFPN — Transmit frame indication derived from the active CEM
VCXOC51 — 19.44 MHz SONET transmit clock synthesized from C41A and PDOFPN
25MCLK — 25.92 MHz SONET clock, used by OMaR devices (synthesized from VCX0C51 and FP15N)
FP51N — Frame pulse based on the 19.44 MHz synthesized clock (VCXOC51)
C162 — Transmit DS-1 clock used by OMaR devices, derived from VCXOC51 and FP51N
C154 — STS-1 rate telecom bus clock derived from VCXO51 and FP51N
MFP — Master frame pulse based on the C154 clock

## Power requirements

The following table shows the NTLX71AA OC3 interface module general power requirements.

| Parameter | Minimum | Maximum | Units |
|---|---|---|---|
| Supply voltage | 39.0 | 053.0 | V |
| Supply noise | | 100.0 | mV |
| Supply current | | 001.0 | A |

# NTLX72BA Data Link Controller Resource Module

## Product description

### Overview

The Data Link Controller (DLC2) Resource Module (RM) provides data link layer protocol termination for multiple port data communications using the HDLC frame structure for the Spectrum Peripheral Module (SPM). It is a hardware and software platform upon which HDLC messaging based feature applications can be implemented, such as LAP-D for ISDN Primary Rate Interface (PRI).

The principal functions of the DLC2 are:

- Termination of layer 2 link protocol for up to 256 independent data channels formatted as HDLC frames.
- Termination of proprietary (DMSW) data link protocol messages to/from both the active and the inactive CEM
- Protocol conversion between HDLC frames and DMSW messages for layer 3 data to be processed within the SPM or DMS Core (e.g., call control information).
- Statistical multiplexing/demultiplexing and retransmission of HDLC frames for layer 3 data to be processed externally (e.g., user data packets).
- Transmission and reception of layer 1 data to and from the CEMs through the SPM S-Link serial bus.

## Functional description

The DLC2 provides the following features:

- Support for Q.921 LAP-D protocol.
- DS0 (64 kb/s), sub-DS0 (16 kb/s), and hyper channel (n×64 kb/s) data rates.
- Embedded PowerQUICC II integrated processor with 166/200-MHz EC603e microprocessor core and 133 MHz communications processor module supporting up to 700 Mbps aggregate serial bandwidth. Supports up to 256 HDLC channels.
- 32 MBytes of on board synchronous DRAM - expandable to 64/128 MBytes.
- 16 MBytes of Flash memory - expandable to 32 MBytes
- Integrated test and maintenance support via an IEEE 1149.1 compliant JTAG boundary scan master.
- On-board point-of-use power supplies (PUPS) with under/over voltage protection.

## NTLX72BA Data Link Controller Resource Module (continued)

- 10 / 100 BaseT Ethernet debug port.
- RS232 debug port.
- Capability to terminate 256 HDLC channels when populated in the 1 S-Link only slots of the SPM.

### Backward compatibility

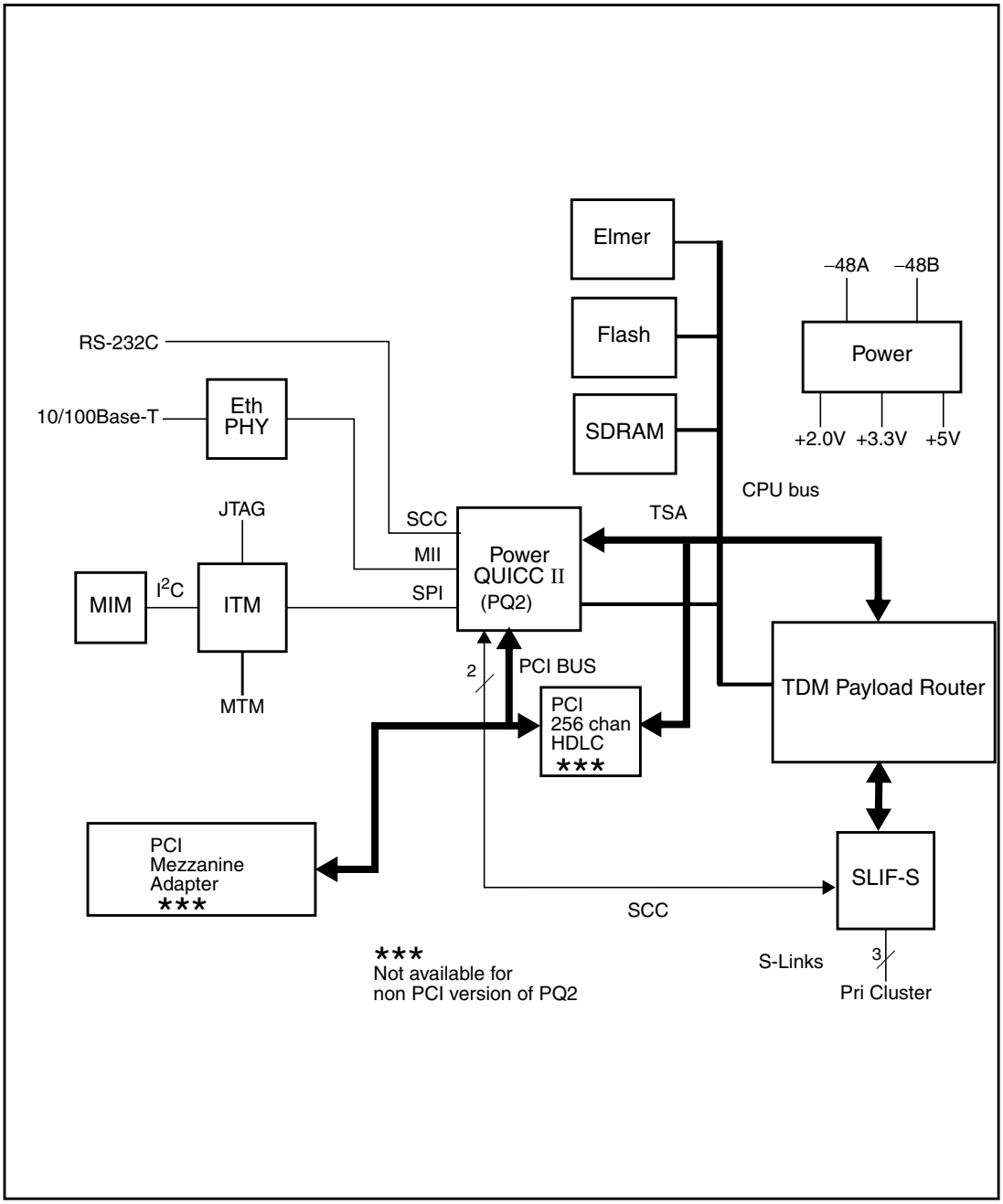
The NTLX72BA is backward compatible with it's predecessor the NTLX72AA.

## Functional block diagram

The next diagram is an illustration of the functional block diagram of the DLC2 RM.

## NTLX72BA Data Link Controller Resource Module (continued)

**DLC2 functional block diagram**




### PowerQUICC II (Voyager) Processor Complex

The processor complex along with it's imbedded communication processor module (CPM) performs the complete specific link layer protocol (e.g. LAPD). It is also responsible for the local initialization, configuration, and maintenance of the resource module, as well as communication with the

## NTLX72BA Data Link Controller Resource Module (continued)

Common Equipment modules via the S-Link messaging facility.It also initializes and configures the peripheral devices on the RM, executes diagnostic routines to test the module, stores the Initial Boot Loader (IBL) and the application software load in non-volatile memory, and provides both Ethernet and RS-232C interfaces for development and debug purposes.

The Motorola PowerQUICC II is a high performance integrated communications processor which implements all of the host processing as well as much of the communications functions required on the DLC2 resource module, all within a single device.

A 32 Mbyte bank of synchronous DRAM (expandable to 64/128 MB) provides program storage for the processor as well as message data buffer and descriptor memory. Since secondary cache on the same bus as SDRAM is expected to produce very minimal performance improvement, it will not be included in the design.

16 Mbytes of Flash memory (expandable to 32 MB) provides non-volatile storage of boot code as well as an image of the application code.

The processor communicates with the memory and application peripherals via a PowerPC bus. The memory controller within the PowerQUICC II controls all external bus cycles to the various types of memory devices, including row/column address multiplexing to SDRAM. Direct memory-to-memory transfers are handled by the IDMA controller. To manage high fanout, the address and data buses are partitioned into separate segments for the 64-bit wide synchronous memory, and the 8-bit, 16-bit, and 32-bit asynchronous memory.

### Serial link interface

Between each CEM and the DLC2 RM there is one serial link connected, consisting of one group of three S-Links. The S-Link is associated with a transmit and a receive clock signal, which is used to recover the timing information for the link, and is referred to as an S-Link cluster. One Slave S-Link Interface (SLIF-S) ASICs, one per S-Link cluster pair, are responsible for the physical interface. The SLIF-S performs the following functions:

- recovers data from the S-Links from both CEM modules
- monitors link health by way of a CRC check
- extracts DMSW messaging channels from both CEM modules
- selects PCM data from the CEMs, based on CEM activity; a small elastic store function is supplied to accommodate phase variations between the CEMs

- formats the selected data stream into a parallel bus for access by the resources supplied by the RM
- broadcasts outgoing PCM data to both CEMs
- inserts outgoing DMSW messaging timeslots to each CEM
- inserts link CRC
- provides facilities for low level link as well as RM control and status facilities, including test and ID storage

Three S-Links, 1 primary + 2 secondary, are connected between a SLIF-S and each of the two CEMs. The "Backplane pin description" table shows how the S-Link timeslots are assigned on each of the 3 S-Links. Logically, each S-Link consists of 8 groups of 32 channels each. On group 0 of the primary S-Link, channels 0 and 31 are reserved for framing and operations, respectively, and channels 1-30 are used as a single high-speed DMSW messaging link. (The messaging link is only allocated on the first S-Link cluster. For the other two clusters, the corresponding channels are used for payload instead.) The remaining groups on the primary link, as well as all timeslots on the secondary links, are used for HDLC payload data. This leaves 512 channels each capable of 64Kbits on the remaining 2 S-Links. The DLC2 supports 256 channels for PRI application.

Each S-Link channel contains twelve bits, of which one is a spoiler (framing) bit, one is an out-of-band (OOB) channel bit, eight carry traffic (speech or data), one is a utility bit, and one bit is a parity check bit. The spoiler and OOB bits are terminated by the SLIF-S, while the remaining 10-bits transport TDM payload to/from the internal RM application circuitry.

On the DLC2 RM, the SLIF-S device interfaces to the TDM Payload Router (ROUTER2), which distributes the PCM channels to/from the Power QUICC II TSA ports. The SLIF-S device connects to the ROUTER2 chip via an individual SLIF-S parallel S-Link payload bus.

**TDM Payload Router (ROUTER 2)**

The Payload Router is responsible for converting between the multiplexed parallel payload bus of the SLIF-S and the individual serial data streams of the Power QUICC II TSA interface. It also provides the clocks and framing signals required for the HDLC serial buses.

Channel mapping is fixed in the Payload Router since DS0 switching is done in the CEMs and channel-to-port assignments are configurable within the Power QUICC II MCC.

## NTLX72BA Data Link Controller Resource Module (continued)

The Payload ROUTER function is performed in a Altera 7512AE FPGA. The ROUTER2 has additional functionality such as a 8 bit processor interface to allow for additional diagnostic functions such as the setting and removal of data path loopbacks.

### DMSW Message Interface (Reference)

The PQII processor on the DLC2 communicates with the SPM control module (CEM) using DMSW messaging. Messages between each CEM and the DLC2 are passed on the primary S-Links. It is expected that the messaging links to each CEMs will both be active. The messages are evenly distributed on the link's time slots and assigned in groups of 32 timeslots. Since time slots 0 and 248 of the Group 0 are assigned to framing and operations, the scalability is 30 channels, then 62, then 126, and finally 254. However, the PQII SCC interface bandwidth limits the number of time slots to 126. Eight bits of message payload are transmitted on each time slot. The range in terms of equivalent bandwidth is (8bits/ts x 30ts/fr x 1fr/125us) 1.92Mbits/sec (1 Group used for messaging) up to 8.064Mbits/sec (4 Groups used for messaging). The message bandwidth is set in the SLIF-S Messaging Bandwidth Register.

Receive messages transmitted by the CEM to the DLC are first handled by the SLIF-S. Time slots assigned to messaging are extracted from the primary link serial stream and passed to the link handler block in the SLIF-S. The link handler performs CRC checking, acknowledges the DMSW message to the sending side, appends a valid / non-valid byte to the end of the message and passes the message to the SCC interface block. The SCC interface block performs the handshaking with the PQII SCC port. The PQII SCC is operated in the transparent mode with CRC checking disabled. The PQII does not perform any protocol or data encoding / decoding. The SLIF-S asserts the CD– signal to indicate the beginning of a message frame and continues to assert CD– until the last bit of the message is sent. Messages received by the SCC are stored in a FIFO in the PQII dual port RAM. The PQII SDMA block transfers these messages to main memory. The SDMA controller is not capable of bursting but does gather the message bytes into a four byte word before transferring to main memory. Descriptor rings for the SDMA are kept in the PQII dual port RAM and must be maintained by the host processor. The SDMA transfers each word to main memory.

Transmit messages originate by the host processor filling the transmit data buffers in main memory and configuring the transmit descriptor ring in the PQII. Additional writes to the PQII registers then begin the message transmission. The SDMA on the PQII transfers the message one word at a time from the main memory to a FIFO in the PQII dual port RAM. To read from main memory, PQII must initiates a read to main memory. Once the FIFO is sufficiently filled, the SCC port will assert RTS– to signal the beginning of a frame. The CTS– signal from the SLIF-S must be asserted before the PQII will

## NTLX72BA Data Link Controller Resource Module (continued)

assert RTS–. The gated transmit clock from the SLIF-S transfers a bit from the SCC on each clock beat. The clock is held high following each eight bits transferred in order to match the outgoing bit rate on the S-Link. RTS– is negated following the last bit of the message. The link handler in the SLIF-S prepares the message check sum per the DMSW protocol and stuffs each byte of the message in consecutive messaging time slots.

### Maintenance

The Integrated Test Master (ITM) acts as an interface to many of the hardware related diagnostic functions. One ITM is present on each of the cards in the MSP frame. The ITM terminates the Module Test and Maintenance (MTM) bus from the Spectrum backplane, which is based on the 1149.5 standard. It also is the start and end point for the JTAG 1149.1 scan chain local to each card. The ITM provides access to the module faceplate LEDs and to the Module Information Memory (MIM). Host processor access is performed via the SPI port on the PowerQUICC II. The DLC2 RM operates as a smart slave on the MTM bus whereby the DLC2 RM host processor has exclusive access to all of the ITM's internal registers.

The MIM contains information related to the board. It is comprised of several sections, which contain manufacturing, JTAG test vector and fault data. It is used by manufacturing for product tracking, and is also used by the DMS system to readily identify the module and any characteristics unique to it. The MIM is under the control of the ITM on the board to allow CEM access via the local RM processor or via the MTM bus under fault conditions.

### Power supply

Two DC-to-DC point-of-use power supplies (PUPS) will be used to convert the –48V A and B feeds to the +3.3V and +5V supply rails required for the DLC2 RM circuitry. In addition, a linear regulator will provide +2V from the +3.3V supply in order to power the PowerQUICC II processor core.

The shelf A and B feeds are diode ORed together to supply a fused input to the power circuit, allowing the resource module to operate with either or both of the shelf supplies. A fuse in each power feed, before the diode OR circuit, was not chosen because of problems in detecting a blown fuse in a single feed. If only one of the two fuses were to blow, it is possible an RM could be inadvertently shut down during routine maintenance procedures (by powering down one of the two feeds). The diodes used are special for this application, and are designed to fail in an open state and not catch on fire. Also, special provisions are made in circuit board layout to reduce the risk of shorts occurring before the fuse.

In-rush current protection, automatic return from low battery (ARLB), and shutdown circuitry controls a power MOSFET switch for the diode ORed

## NTLX72BA Data Link Controller Resource Module (continued)

–48V battery feed. Battery and return are filtered to reduce electro-magnetic interference (EMI) and then supply the input to the PUPS. Overvoltage and undervoltage conditions on both +5V and +3.3V PUPS outputs are monitored for and will cause a shutdown of the power supply circuit if detected. The battery supply must be cycled off and back on in order to reset the shutdown circuit and re-enable the PUPS.

This circuit monitors the +5V, +3.3V, and +2.5V voltages and asserts a single reset pulse to the DLC2 RM if any voltage drops below the following limits:

- 2.3V for the +2.5V supply
- 3.0V for the +3.3V supply
- 4.75V for the +5V supply

The reset pulse duration is 140msec.

# NTLX72BA Data Link Controller Resource Module (continued)

### Pin Description

The next table identifies each connector used in the design, the pin numbers, and their type (such as inputs, outputs, CMOS, I/O TTL and ECL).

## Backplane Pin Description

| Pin no. | Signal | Function | Description |
|---|---|---|---|
| P1:8A | -48A | Supply | -48 volt battery feed A |
| P1:8B | | | |
| P1:8C | | | |
| P1:8D | | | |
| P1:8E | | | |
| P1:2A | -48B | Supply | -48 volt battery feed B |
| P1:2B | | | |
| P1:2C | | | |
| P1:2D | | | |
| P1:2E | | | |
| P1:5A | RTN | Supply | Battern return (ground) |
| P1:5B | | | |
| P1:5C | | | |
| P1:5D<br>P1:5E | | | |
| P2:10B | SCKI_0 | Input | Receive S-Link clock @24.576 MHz from CEM 0 |
| P2:9B | SDI_0(P) | Input | Receive S-Link data from CEM 0 |
| P2:9A | SDI_0(S1) | | |
| P2:10A | SDI_0(S2) | | |
| P2:8B | SCKO_0 | Output | Transmit S-Link clock @24.576 MHz to CEM 0 |
| P2:7B | SDO_0(P) | Output | Transmit S-Link data to CEM 0 |
| P2:7A | SDO_0(S1) | | |
| P2:8A | SDO_0(S2) | | |

## NTLX72BA Data Link Controller Resource Module (continued)

### Backplane Pin Description (Continued)

| Pin no. | Signal | Function | Description |
|---|---|---|---|
| P2:10D | SCKI_1 | Input | Receive S-Link clock @24.576 MHz from CEM 1 |
| P2:9D | SDI_1(P) | Input | Receive S-Link data from CEM 1 |
| P2:9E | SDI_1(S1) | | |
| P2:10E | SDI_1(S2) | | |
| P2:8D | SCKO_1 | Output | Transmit S-Link clock @24.576 MHz to CEM 1 |
| P2:7D | SDO_1(P) | Output | Transmit S-Link data to CEM 1 |
| P2:7E | SDO_1(S1) | | |
| P2:8E | SDO_1(S2) | | |
| P2:16E | SLOT_ID(0) | Input | Physical slot identification |
| P2:16D | SLOT_ID(1) | | |
| P2:17C | SLOT_ID(2) | | |
| P2:16B | SLOT_ID(3) | | |
| P2:16A | SLOT_ID(4) | | |
| P2:17D | MCLK | Input | MTM clock |
| P2:16C | MCTL | Input | MTM control |
| P2:18A | MMD | Input | MTM master data |
| P2:18E | MSD | Output | MTM slave data |

# NTLX72BA Data Link Controller Resource Module (continued)

## Backplane Pin Description (Continued)

| Pin no. | Signal | Function | Description |
|---|---|---|---|
| P2:17B | MPR | Output | MTM pause request |

## NTLX72BA Data Link Controller Resource Module (continued)

### Backplane Pin Description (Continued)

| Pin no. | Signal | Function | Description |
|---|---|---|---|
| P2:2B | LGND | Supply | Logic ground |
| P2:2C | | | |
| P2:2D | | | |
| P2:3C | | | |
| P2:4A | | | |
| P2:4B | | | |
| P2:4C | | | |
| P2:4D | | | |
| P2:4E | | | |
| P2:5C | | | |
| P2:6C | | | |
| P2:7C | | | |
| P2:8C | | | |
| P2:9C | | | |
| P2:10C | | | |
| P2:11A | | | |
| P2:11B | | | |
| P2:11C | | | |
| P2:11D | | | |
| P2:11E | | | |
| P2:12C | | | |
| P2:13C | | | |
| P2:14C | | | |
| P2:15C | | | |
| P2:17A | | | |
| P2:17E | | | |
| P2:18B | | | |
| P2:18C | | | |
| P2:18D | | | |

## NTLX72BA Data Link Controller Resource Module (continued)

# Interface specifications

## Visual indicators

The DLC2 2 Resource Module will carry a set of indicators to provide information of interest to craft personnel. The LEDs, which are located at the faceplate, indicate the current state of the module as shown:

**Visual indicators - module status**

| Green | Red | Module state |
|---|---|---|
| Off | Off | Sleep, un-powered or not inserted |
| On | On | Power up LED test |
| Wink | Off | Power up self-test underway |
| On | Off | Module should not be removed |
| Off | On | Alarm State: Module may be removed |

Power up LED test is entered immediately after the module is first powered up or inserted. Its purpose is to allow craft personnel to verify that the LEDs are functional. The LEDs remain in this state for the duration of the power-up self-test.

Alarm State is entered during a power up or insertion sequence if the self-test fails, or if the Common Equipment Module rejects the module as being unworkable in the system due to incompatibilities or a failure to establish communications with the module

The Green ON, Red OFF state is entered during power up or insertion sequence when the module has passed its diagnostic test. In this case, the module should not be removed

## Sleep mode

When not required, circuit module LEDs may enter a customer programmable “sleep” mode to extend their life. The LEDs will leave the sleep mode:

- when so directed by PRI S/W
- as a result of LED state change
- as part of an Indicator Test

## NTLX72BA Data Link Controller Resource Module (end)

The LEDs will not sleep while an alarm source is active (i.e. while there is a module in the peripheral in the RED ON, GREEN OFF state.

## Hardware interfaces

### Power requirements

The DLC2 Resource Module will utilize two Point-of-Use Power Supplies (PUPS) to convert –48V to 5V and 3.3V as required. Two independent –48V sources will be provided for redundancy. These will be diode-ORed within the DLC2 RM before being fed to the PUPS. 2V will be supplied via the 3.3V supply with a linear voltage regulator.

**AC operating conditions**

| Symbols | Parameter | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| $t_{PLH}$,$t_{PHL}$ | Clock to output delay | 1.5 | 8 | ns | |
| $t_R$ | Output rise time (0.2-0.8 $V_{CC}$) | 1 | 4 | V/ns | Unloaded |
| $t_F$ | Output fall time (0.8-0.2 $V_{CC}$) | 1 | 4 | V/n | Unloaded |

The next table contains NTLX72BA power requirements.

**Power specifications**

| Symbols | Parameter | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| Supply voltage | -40 | -48 | -60 | Volts | |
| Supply noise | | | | mV | |
| Power dissipation | | 31 | 39 | Watts | Preliminary estimate |

# NTLX73BB Asynchronous Transfer Mode Resource Module

## Product description

### Overview

The Asynchronous Transfer Mode (ATM) Resource Module (RM), NTLX73BB, adapts Spectrum DS0-based voice and data channels to ATM cells for transmission over a Synchronous Optical NETwork (SONET) OC-3 or Synchronous Digital Hierarchy (SDH) STM-1 optical interface. DS0 transport over ATM is accomplished using ATM Adaptation Layer type 1 (AAL-1) Structured Data Transfer (SDT), where voice is mapped using Single Channel Adaptation (SCA). As such, the ATM RM provides DS0 trunking over an ATM transmission network. In addition to this mapping function, this Resource Module also provides the capability for ATM cell generation and reception which can be used for message transport. Anticipated applications of this messaging are transport of the Simple Network Management Protocol (SNMP), Switched Virtual Circuit (SVC) signalling, and DMS control and supervision.

## Functional description

The ATM Resource Module can be provisioned in the slots which provide three S-Link clusters (OC-3 slots) or in general purpose resource module slots.

The principal functions of the ATM Resource Module are to:

- Map between TDM channels from 9 S-Links and ATM cells using AAL-1 Structured Data Transfer.
- Physically interface to a single OC-3/STM-1 rate (155.52 Mbps) SONET/SDH Single Mode Fiber (SMF).
- Establish DS0 trunking over the ATM AAL-5 based messaging.
- Terminate and process ATM AAL-5 based messaging.
- Terminate and process F4 and F5 OAM cells.
- Terminate and process SONET/SDH overhead.
- Generate the SONET/SDH OC-3/STM-1 transmit clock from the Spectrum S-Link clock.
- Extract the SONET/SDH Network OC-3/STM-1 clock reference for system timing.
- Implement ATM Virtual Circuit Performance Monitoring.
- Send generated ATM traffic to the mate RM. Select the source of ATM traffic to be transmitted out the physical link from the either the local or the mate RM ATM layer.

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

- Send received ATM traffic to the mate RM. Select the source of received ATM traffic to be processed from either the local or the mate RM physical layer.
- Terminate proprietary (DMSW) data link protocol messages to/from both the active and the inactive CEMs.
- Terminate layer 2 link protocol on multiple independent channels formatted as HDLC frames.

### Location

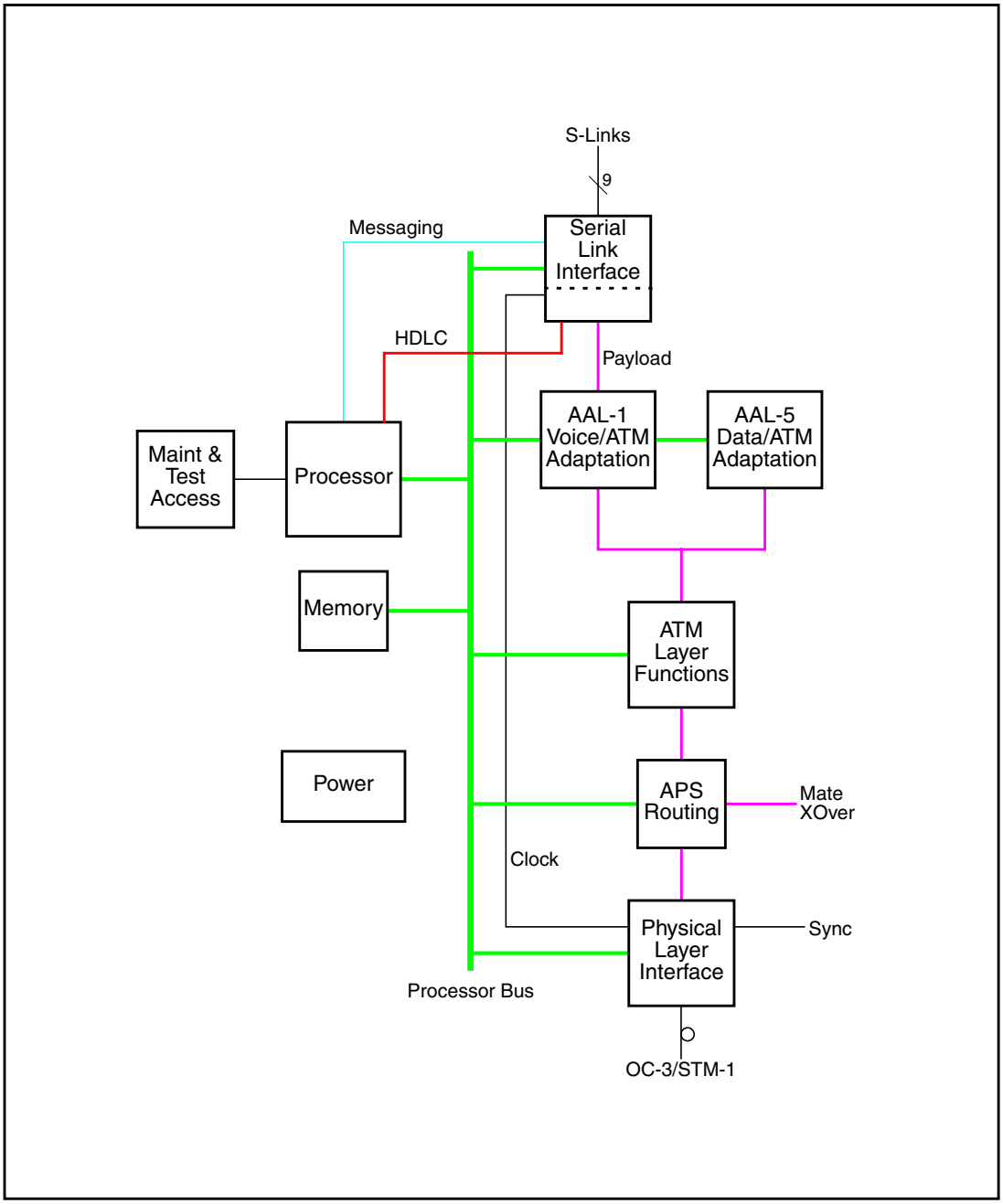
The NTLX44AA is functionally backward compatible with its original predecessor, the NTLX73AA. It also offers increased capabilities, with lower material cost and reduced power dissipation. However, its hardware architecture is significantly different and so will not be compatible with an unmodified software load intended for the original design.

## Functional block diagram

The next diagram is an illustration of the functional block diagram of the ATM RM.

# NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

**NTLX73BB functional block diagram**




## PowerQUICC II (Voyager) Processor Complex

The Processor provides the local intelligence to perform basic module control and maintenance activities, and to manage the various ATM adaptation and supervision devices on the RM. It communicates with the CEM and services requests to establish DS0 voice trunks over ATM, and administers data packet

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

transfers between the ATM SAR and the DMS link protocol engines. It also initializes and configures the peripheral devices on the RM, executes diagnostic routines to test the module, stores the Initial Boot Loader (IBL) and the application software load in non-volatile memory, and provides both Ethernet and RS-232 interfaces for development and debug purposes.

The Motorola PowerQUICC II is a high performance integrated communications processor which implements all of the host processing as well as much of the communications functions required on the ATM resource module, all within a single device.

### Serial Link Interface

Between each CEM and the ATM RM there are nine serial links connected, consisting of three groups of three S-Links each. Each group of three S-Links is associated with a transmit and a receive clock signal, which is used to recover the timing information for the three links, and is referred to as an S-Link cluster. Three Slave S-Link Interface (SLIF-S) ASICs, one per S-Link cluster pair, are responsible for the physical interface.

Three S-Links, 1 primary + 2 secondary, are connected between a SLIF-S and each of the two CEMs. The “Backplane pin description” table shows how the S-Link timeslots are assigned on each of the 3 S-Links. Logically, each S-Link consists of 8 groups of 32 channels each. On group 0 of the primary S-Link, channels 0 and 31 are reserved for framing and operations, respectively, and channels 1-30 are used as a single high-speed DMSW messaging link. (The messaging link is only allocated on the first S-Link cluster. For the other two clusters, the corresponding channels are used for payload instead.) The remaining groups on the primary link, as well as all timeslots on the secondary links, are used for payload data.

On the ATM RM, the three SLIF-S devices interface to the TDM Payload Router (TPR), which distributes the PCM channels to/from the ATM adaptation layer devices. The SLIF-S devices connect to the TPR chip via the individual SLIF-S parallel S-Link payload busses.

The SLIF-S used to pass DMSW messaging and register access messaging between the CEM and the ATM RM is the primary SLIF-S. The messaging and software interrupt (register access) interfaces for the other two SLIF-S devices are not used. The hardware interrupts and processor bus interfaces to all SLIF-S devices are used. The primary SLIF-S device also carries transport and path overhead data to be inserted and extracted from the OC-3c carrier handled by the ATM RM. This mapping function is provided by the TPR.

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

### TDM Payload Router

The TDM Payload Router interfaces the three parallel TDM payload streams from the SLIF-S devices to the AAE ASICs, PowerQUICC II multi-channel TDM ports, DMSY messaging block, and the overhead channel input of the SATURN User Network Interface - Plus (SUNI+). This function allocates 2,048 DS0s (2,016 dedicated plus 32 which can be used for expanded messaging instead) out of the total S-Link capacity of 2,304 for possible use by the ATM adaptation devices. Additionally, another 32 DS0s have been reserved to transport the unterminated SONET overhead channels from the SUNI+ device.

TDM payload routing to the AAE ASICs is accomplished by a control strobe identifying the above noted 2,048 available AAE DS0s out of the total 2,304 supplied by the SLIF-S devices combined with an additional number of null channels to simplify system clocking. (Total of 3,072 channels.) This data stream / control strobe is supplied to both AAEs. The AAE control software must identify the active channels for a particular AAE and must assure that a particular channel is used by one and only one AAE. The TDM Payload Multiplexer has an eight bit processor interface allowing for device configuration and the setting and removal of data path loopbacks.

### ATM Voice Adaptation

ATM Adaptation Layer type 1 (AAL-1) is defined for constant bit rate (CBR) services that require a timing relation between the endpoints of the connection, such as voice telephony. The mapping of TDM voice channels to ATM cells is performed by a Nortel custom ASIC device designated the ATM Adaptation Entity, or AAE. A pair of AAEs is used on the ATM RM to map up to 2,048 DS0s into a maximum of 2,048 ATM virtual circuits. The AAE is capable of mapping DS0s to ATM cells via the following adaption methods: AAL-1 SDT, AAL-1 SUDT (Synchronous Unstructured Data Transfer), and AAL-0 SUDT. For the ATM RM application, AAL-1 SDT (Structured Data Transfer) will be used.

This mapping has two general cases: N×64 trunking, and single DS0 trunking (voice/modem/single-channel data traffic). N×64 traffic aggregates multiple DS0s from a single frame into a single data path. To transfer N×64 traffic, the AAE will map the indicated DS0s into the payload of an ATM cell. AAL-1 SDT allows this “structure” to be repeated within the cell payload for efficient bandwidth utilization. Thus, multiple frames of data will exist within a single cell. To indicate the start of a structure within the payload, a pointer is sent as the second ATM cell payload byte once during every 8-cell sequence. Note that in addition to this pointer byte, a modulo eight sequence counter is inserted as the first payload byte of every AAL-1 SDT cell. In the limiting case where a single DS0 is mapped to a virtual circuit, the AAE fills the cell’s

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

payload with 47 bytes (frames) of data. The first payload byte is still the sequence count which is included in every cell. However, no pointer is required in this case, making it identical to AAL-1 SUDT. This method of ATM Adaptation is sometimes referred to as AAL-1 Single Channel Adaptation or SCA.

### ATM Data Adaptation

AAL type 5 is defined for variable bit rate (VBR) services that do not require any timing relation between the endpoints, such as data packets. Typically, AAL-5 encapsulated data packets are used in Spectrum for three main purposes: 1) messages from Spectrum to the ATM network for establishing and removing switched virtual circuit (SVC) connections, 2) control/maintenance messages between the DMS core and a subtended non-integrated Spectrum, and 3) messages between Spectrums inter-connected by the ATM network.

### HDLC Message Interface

Depending on system software partitioning, it may be advantageous to have direct RM-to-RM messaging links in the Spectrum. For example, this would allow for synchronization of protocol stacks running on active and standby interface RMs without any processing or messaging resource usage in the CEM. A proposed solution to this is to run HDLC over nailed-up N×DS0 connections between the resource modules.

### UTOPIA Bus Control

The Universal Test & Operations PHY Interface for ATM (UTOPIA) defines the interface between the physical layer (PHY) and upper layer modules, such as the ATM layer. It provides a standard interface used on commercial ATM devices. Utopia Level 1 defines an 8-bit data path, operating up to 25 MHz, using either cell-level or byte-level handshaking, and with a single PHY. Utopia Level 2 expands the specification to cover a 16-bit interface, operating up to 50 MHz, and with multiple PHYs. In addition to this, SCI-PHY Level 2 defines extensions beyond Utopia Level 2, the most pertinent being extended cell formats.

As used in this document, the terms ingress and egress refer to the flow of traffic with respect to the core ATM network, which in this case means the OC-3/STM-1 carrier side. This definition is consistent with the AAE documentation. However, this can be a source of confusion as most commercial ATM device documentation is written from the perspective of an ATM switch application, where the carrier interface is opposite from the switch. This means that the ingress (incoming) ports on the SUNI+ and ATLAS will carry network egress traffic, while their egress (outgoing) ports will carry network ingress traffic.

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

### ATM User Network Interface

The physical layer of the OC-3/STM-1 stream is terminated in the PMC-Sierra PM5347, SATURN User Network Interface - Plus (S/UNI-Plus or SUNI+) chip. This device receives the 155 Mbit/s electrical signal and terminates link framing and all of the associated SONET/SDH overhead channels. It also extracts ATM cells from the received STS-3c/STM-1 synchronous payload envelope (SPE) using ATM cell HEC delineation and passes them to a 16-bit UTOPIA interface for higher level processing. SONET/SDH overhead bytes not terminated by the SUNI+ are routed to the overhead mapping portion of the TDM Payload Router. Those bytes which are terminated within the SUNI+ are made available to the host processor via an asynchronous eight bit processor data bus.

The SUNI+ also performs clock recovery and generation for the OC-3/STM-1 rate stream. Using an external byte rate clock, the SUNI+ generates a 155.52 MHz internal clock and uses that for synchronization to the incoming data stream. Once in lock, the PLL reverts to the local reference if no data transitions occur within 80 bit periods or if the recovered clock drifts beyond 488 ppm of the reference clock. The clock recovery unit also has a software interface to determine the sync status and a loss of signal input that clamps the incoming data under alarm.

### OC-3/STM-1 Optical Interface

The optical interface consists of three functional blocks: 1) the external optical interface, 2) the electro-optical conversion circuitry, and 3) the alarm and monitoring circuitry.

The external optical interface connects the ATM RM to the external world. The optics operate at a nominal wavelength of 1310 nanometers into a single-mode fiber and at a data rate of 155.52 Mb/s. A digital acquisition system (DAS) contains several analog-to-digital converters (ADC) and provides a means for monitoring the carrier interface circuitry. Laser bias current (LBC), laser back facet monitor (BFM), receive light level (RLL), temperature sensor, and transmit clock VCXO control voltage signals are all monitored via the DAS. This information is then accessible to the processor via an 8-bit interface on the DAS.

### Clock Generation, Recovery, and Distribution

Transmit clocks for the OC-3/STM-1 line payloads are generated on the ATM RM from the 24.576 MHz S-Link Clock, provided by the primary SLIF-S device. The SLIF-S phase locks this clock to the master S-Link from the active CEM. The SLIF-S provides buffering of clock and data to achieve a stable switch of data paths in the event of a CEM activity switch.

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

Clock recovery from the incoming optical stream is performed internal to the PM5347. In the receive direction, the SUNI+ interfaces to the receiver and recovers clock and data from the incoming differential PECL data stream. The clock recovery function is performed by using an embedded PLL, which uses an external byte rate (19.44 MHz) reference. This external clock is internally multiplied by 8 and is used to improve PLL lock time and generate a 155.52 Mb/s clock in the absence of incoming data. The SUNI+ also derives an 8 kHz frame signal from the receive SONET/SDH data stream, which can be used for system timing synchronization.

In the transmit direction, the SUNI+ generates a line rate clock from the external 19.44 MHz reference, which is synchronized to the 24.576 MHz SLIF-S output clock. The re-timed data stream is then sent to the transmitter. The PM5347 also contains an internal loopback that is controlled via the host processor which allows the transmit data to be looped into the receive data stream for diagnostic purposes.

### Maintenance

The Integrated Test Master (ITM) acts as an interface to many of the hardware related diagnostic functions. One ITM is present on each of the cards in the MSP frame. The ITM terminates the Module Test and Maintenance (MTM) bus from the Spectrum backplane, which is based on the 1149.5 standard. It also is the start and end point for the JTAG 1149.1 scan chain local to each card. The ITM provides access to the module faceplate LEDs and to the Module Information Memory (MIM). Host processor access is performed via the SPI port on the PowerQUICC II. The ATM RM operates as a smart slave on the MTM bus whereby the ATM RM host processor has exclusive access to all of the ITM's internal registers.

### Power Supply

Two DC-to-DC point-of-use power supplies (PUPS) will be used to convert the –48V A and B feeds to the +3.3V and +5V supply rails required for the ATM RM circuitry. In addition, a linear regulator will provide a +2V supply from the +3.3V supply in order to power the PowerQUICC II processor core. This +2V output will vary with the version of the PQII and will initially be +2.5V. This will be reduced to +2.3V, +2.0V and/or +1.8V depending on the recommendations from Motorola. The lowest voltage possible will be used to reduce power consumption while maintaining needed operating frequencies.

# NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

## Pin description

The next table identifies each connector used in the design, the pin numbers, and their type (such as inputs, outputs, CMOS, I/O TTL and ECL).

### Backplane Pin Description

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P1:8A | -48A | Supply | -48 volt battery feed A |
| P1:8B | | | |
| P1:8C | | | |
| P1:8D | | | |
| P1:8E | | | |
| P1:2A | -48B | Supply | -48 volt battery feed B |
| P1:2B | | | |
| P1:2C | | | |
| P1:2D | | | |
| P1:2E | | | |
| P1:5A | RTN | Supply | Battery return (ground) |
| P1:5B | | | |
| P1:5C | | | |
| P1:5D | | | |
| P1:5E | | | |
| P2:10B | FrCEM0_CK0 | Input | S-Link clock lines from the CEMs |
| P2:10D | FrCEM1_CK0 | | |
| P3:17B | FrCEM0_CK1 | | |
| P3:17D | FrCEM1_CK1 | | |
| P3:12B | FrCEM0_CK2 | | |
| P3:12D | FrCEM1_CK2 | | |

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

### Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P2:9B | FrCEM0_D0 | Input | S-Link data lines from the CEMs |
| P2:9D | FrCEM1_D0 | | |
| P2:9A | FrCEM0_D1 | | |
| P2:9E | FrCEM1_D1 | | |
| P2:10A | FrCEM0_D2 | | |
| P2:10E | FrCEM1_D2 | | |
| P3:16B | FrCEM0_D3 | | |
| P3:16D | FrCEM1_D3 | | |
| P3:16A | FrCEM0_D4 | | |
| P3:16E | FrCEM1_D4 | | |
| P3:17A | FrCEM0_D5 | | |
| P3:17E | FrCEM1_D5 | | |
| P3:11B | FrCEM0_D6 | | |
| P3:11D | FrCEM1_D6 | | |
| P3:11A | FrCEM0_D7 | | |
| P3:11E | FrCEM1_D7 | | |
| P3:12A | FrCEM0_D8 | | |
| P3:12E | FrCEM1_D8 | | |
| P2:8B | ToCEM0_CK0 | Output | S-Link clock lines to the CEMs |
| P2:8D | ToCEM1_CK0 | | |
| P3:15B | ToCEM0_CK1 | | |
| P3:15D | ToCEM1_CK1 | | |
| P3:10B | ToCEM0_CK2 | | |
| P3:10D | ToCEM1_CK2 | | |

# NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

## Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P2:7B | ToCEM0_D0 | Output | S-Link data lines to the CEMs |
| P2:7D | ToCEM1_D0 | | |
| P2:7A | ToCEM0_D1 | | |
| P2:7E | ToCEM1_D1 | | |
| P2:8A | ToCEM0_D2 | | |
| P2:8E | ToCEM1_D2 | | |
| P3:14B | ToCEM0_D3 | | |
| P3:14D | ToCEM1_D3 | | |
| P3:14A | ToCEM0_D4 | | |
| P3:14E | ToCEM1_D4 | | |
| P3:15A | ToCEM0_D5 | | |
| P3:15E | ToCEM1_D5 | | |
| P3:9B | ToCEM0_D6 | | |
| P3:9D | ToCEM1_D6 | | |
| P3:9A | ToCEM0_D7 | | |
| P3:9E | ToCEM1_D7 | | |
| P3:10A | ToCEM0_D8 | | |
| P3:10E | ToCEM1_D8 | | |
| P2:2A | SYNC_ToCEM0 | Output | OC-3/STM-1 recovered frame pulse, used by CEM or Clock RM for synchronization. |
| P2:3A | SYNC_ToCEM1 | | |
| P2:2E | SYNC_FrOC30 | | |
| P2:3E | SYNC_FrOC31 | | |
| P2:18A | MMD | Input | MTM bus master data |
| P2:18E | MSD | Output | MTM bus slave data |
| P2:17D | MCLK | Input | MTM bus clock |
| P2:17B | MPR | Output | MTM bus pause request |
| P2:16C | MCTL | Input | MTM bus control |

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

### Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P2:16E | SLOT_ID0 | Input | Physical slot identification |
| P2:16D | SLOT_ID1 | | |
| P2:17C | SLOT_ID2 | | |
| P2:16B | SLOT_ID3 | | |
| P2:16A | SLOT_ID4 | | |
| P4:3A | Rx0Data0 | Output | Receive data to mate ATM |
| P4:3B | Rx0Data1 | | |
| P4:4C | Rx0Data2 | | |
| P4:4A | Rx0Data3 | | |
| P4:4B | Rx0Data4 | | |
| P4:5A | Rx0Data5 | | |
| P4:5B | Rx0Data6 | | |
| P4:6A | Rx0Data7 | | |
| P4:8A | Rx0Prty | Output | Receive parity to mate ATM |
| P4:6B | Rx0SOC | Output | Receive start of cell to mate ATM |
| P4:16A | Rx0Enb– | Input | Receive enable from mate ATM |
| P4:7A | Rx0Clav | Output | Receive cell available to mate ATM |
| P4:7B | Rx0Clk | Input | Receive clock from mate ATM |

# NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

## Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P4:3E | Rx1Data0 | Input | Receive data from mate PHY |
| P4:3D | Rx1Data1 | | |
| P4:3C | Rx1Data2 | | |
| P4:4E | Rx1Data3 | | |
| P4:4D | Rx1Data4 | | |
| P4:5E | Rx1Data5 | | |
| P4:5D | Rx1Data6 | | |
| P4:6E | Rx1Data7 | | |
| P4:8E | Rx1Prty | Input | Receive parity from mate PHY |
| P4:6D | Rx1SOC | Input | Receive start of cell from mate PHY |
| P4:16E | Rx1Enb– | Output | Receive enable to mate PHY |
| P4:7E | Rx1Clav | Input | Receive cell available from mate PHY |
| P4:7D | Rx1Clk | Output | Receive clock to mate PHY |
| P4:9B | Tx0Data0 | Output | Transmit data to mate PHY |
| P4:10A | Tx0Data1 | | |
| P4:10B | Tx0Data2 | | |
| P4:11C | Tx0Data3 | | |
| P4:11A | Tx0Data4 | | |
| P4:11B | Tx0Data5 | | |
| P4:12A | Tx0Data6 | | |
| P4:12B | Tx0Data7 | | |
| P4:14A | Tx0Prty | Output | Transmit parity to mate PHY |
| P4:13B | Tx0SOC | Output | Transmit start of cell to mate PHY |

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

### Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P4:17A | Tx0Enb– | Output | Transmit enable to mate PHY |
| P4:13A | Tx0Clav | Input | Transmit cell available from mate PHY |
| P4:14B | Tx0Clk | Output | Transmit clock to mate PHY |
| P4:9D | Tx1Data0 | Input | Transmit data from mate ATM |
| P4:10E | Tx1Data1 | | |
| P4:10D | Tx1Data2 | | |
| P4:10C | Tx1Data3 | | |
| P4:11E | Tx1Data4 | | |
| P4:11D | Tx1Data5 | | |
| P4:12E | Tx1Data6 | | |
| P4:12D | Tx1Data7 | | |
| P4:14E | Tx1Prty | Input | Transmit parity from mate ATM |
| P4:13D | Tx1SOC | Input | Transmit start of cell from mate ATM |
| P4:17E | Tx1Enb– | Input | Transmit enable from mate ATM |
| P4:13E | Tx1Clav | Output | Transmit cell available to mate ATM |
| P4:14D | Tx1Clk | Input | Transmit clock from mate ATM |
| P4:16B | Act0 | Output | ATM layer activity indicator to mate |
| P4:16D | Act1 | Input | ATM layer activity indicator from mate |
| P4:17B | Sel0 | Output | Receive PHY layer selection indicator to mate |

# NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

## Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P4:17D | Sel1 | Input | Receive PHY layer selection indicator from mate |
| P3:3B | Clk0 | Output | Overhead crossover clock output to mate |
| P3:4A | FP0 | Output | Overhead crossover frame pulse to mate |
| P3:3A | TxD0 | Output | Overhead crossover transmit data to mate |
| P3:5A | RxD0 | Input | Overhead crossover receive data from mate |
| P3:5B | TxEn0 | Output | Overhead crossover transmit enable to mate |
| P3:4B | RxVal0 | Input | Overhead crossover receive valid from mate |
| P3:3B | Clk1 | Input | Overhead crossover clock input from mate |
| P3:4A | FP1 | Input | Overhead crossover frame pulse from mate |
| P3:3A | TxD1 | Input | Overhead crossover transmit data from mate |
| P3:5A | RxD1 | Output | Overhead crossover receive data to mate |
| P3:5B | TxEn1 | Input | Overhead crossover transmit enable from mate |
| P3:4B | RxVal1 | Output | Overhead crossover receive valid to mate |

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

### Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P2:2B | LGND | Supply | Logic ground |
| P2:2C | | | |
| P2:2D | | | |
| P2:3C | | | |
| P2:4A | | | |
| P2:4B | | | |
| P2:4C | | | |
| P2:4D | | | |
| P2:4E | | | |
| P2:5C | | | |
| P2:6C | | | |
| P2:7C | | | |
| P2:8C | | | |
| P2:9C | | | |
| P2:10C | | | |
| P2:11A | | | |
| P2:11B | | | |
| P2:11C | | | |
| P2:11D | | | |
| P2:11E | | | |
| P2:12C | | | |
| P2:13C | | | |
| P2:14C | | | |
| P2:15C | | | |
| P2:18B | | | |
| P2:18C | | | |
| P2:18D | | | |
| P3:2A | | | |
| P3:2B | | | |
| P3:2C | | | |

# NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

## Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P3:2D | | | |
| P3:2E | | | |
| P3:3C | | | |
| P3:4C | | | |
| P3:5C | | | |
| P3:6A | | | |
| P3:6B | | | |
| P3:6C | | | |
| P3:6D | | | |
| P3:6E | | | |
| P3:7A | | | |
| P3:7B | | | |
| P3:7C | | | |
| P3:7D | | | |
| P3:7E | | | |
| P3:8A | | | |
| P3:8B | | | |
| P3:8C | | | |
| P3:8D | | | |
| P3:8E | | | |

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

### Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P3:9C | | | |
| P3:10C | | | |
| P3:11C | | | |
| P3:12C | | | |
| P3:13A | | | |
| P3:13B | | | |
| P3:13C | | | |
| P3:13D | | | |
| P3:13E | | | |
| P3:14C | | | |
| P3:15C | | | |
| P3:16C | | | |
| P3:17C | | | |
| P3:18A | | | |
| P3:18B | | | |
| P3:18C | | | |
| P3:18D | | | |
| P3:18E | | | |

# NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

## Backplane Pin Description (Continued)

| Pin No. | Signal | Function | Description |
|---|---|---|---|
| P4:2A | | | |
| P4:2B | | | |
| P4:2C | | | |
| P4:2D | | | |
| P4:2E | | | |
| P4:5C | | | |
| P4:6C | | | |
| P4:7C | | | |
| P4:8B | | | |
| P4:8C | | | |
| P4:8D | | | |
| P4:9A | | | |
| P4:9C | | | |
| P4:9E | | | |
| P4:12C | | | |
| P4:13C | | | |
| P4:14C | | | |
| P4:15A | | | |
| P4:15B | | | |
| P4:15C | | | |
| P4:15D | | | |
| P4:15E | | | |
| P4:16C | | | |
| P4:17C | | | |
| P4:18A | | | |
| P4:18B | | | |
| P4:18C | | | |
| P4:18D | | | |
| P4:18E | | | |

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

### External Optical Interface

The transmitter module consists of an uncooled laser operating at a wavelength of 1310 nanometers and meets the short reach (SR) and intermediate reach-1 (IR-1) SONET specifications of GR-253-CORE, as well as specifications for SDH and ATM operation on singlemode fiber. The transmitter uses proprietary Silicon V-groove technology for precise fiber alignment and optical output level control. Also included in the device is an integrated laser driver IC for laser control, as well as analog monitor outputs of the laser bias current (LBC) and the optical power output level as measured using a back facet monitor (BFM). The transmitter operates from a single 5 volt supply and is packaged in a plastic dual in-line package (DIP) and utilizes an industry standard 20 pin footprint, thus allowing for multiple sources. The optical interface is terminated with a ruggedized (perisil) singlemode fiber pigtail using an SC connector.

The receiver module consists of a PIN photodiode detector operating at 1310 nanometers and meets the SR and IR-1 SONET specifications of GR-253-CORE, as well as specifications for SDH and ATM operation on single-mode fiber. The receiver also uses Silicon V-groove technology for precise fiber alignment and optimum sensitivity. Also included in this device is an integrated limiting amplifier, as well as a loss of signal (LOS) alarm and an analog monitor output of the received light level. The receiver operates from a single 5 volt supply and is packaged in a plastic dual in-line package (DIP) and utilizes an industry standard 20 pin footprint. The optical interface is terminated with a ruggedized (perisil) multimode fiber pigtail using an SC connector. Specifications for the transmitter as used in the ATM RM design are listed in the next table.

**ATM RM Optical transmitter specifications**

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply voltage | 4.7 | 5.5 | Volts |
| Case temperature | -40 | 70 | Degrees C |
| Center wavelength | 1261 | 1360 | nm |
| Mean output power | -15 | -8 | dBm |
| RMS spectral width | | 7.7 | nm |
| Extinction ratio | 8.2 | | dB |

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

Specifications for the receiver as used in the ATM RM design are listed in the next table.

**ATM Optical receiver specifications**

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply voltage | 4.7 | 5.5 | Volts |
| Case temperature | -40 | 70 | Degrees C |
| Center wavelength | 1261 | 1360 | nm |
| Sensitivity | | -37 | dBm |
| Overload | -5 | | dBm |

### Optical Loss Budget Calculations

The SPM OC-3c optical loss budget calculations are shown. The numbers used in this example are based on the parameters listed for singlemode OC-3 IR-1 operation given in GR-253-CORE, and connector losses given in Table 4-2 of GR-326-CORE. GR-253-CORE considers an intermediate reach span to be a maximum of 15km. It is assumed the only connectors in the system, other than the connection at the transmitter and receiver, are 2 optical DSX panels, with one at each end of the fiber span.

**Optical loss budget calculation**

| Loss factor | Calculation | Loss (dB) |
|---|---|---|
| Fiber loss | 15 km @ 0.4 dB/km | 6.0 |
| Connection loss | 2 connectors @ 0.3 dB each | 0.6 |
| Dispersion penalty | | 1.0 |
| Power margin | | 3.0 |
| Total | | 11.0 |

The loss budget indicates the difference between minimum transmitter power and receiver sensitivity for proper system operation. In this case, the minimum transmitter output per (GR-253-CORE) is -8 dBm and the minimum receiver sensitivity is -28dBm. The output power level at the receiver is simply the input power minus the total loss, which is (-8dBm) - 11dBm = -19dBm. The

## NTLX73BB Asynchronous Transfer Mode Resource Module (continued)

output power level is greater than the minimum receiver level of -28dBm, which means that the system will operate correctly while ensuring a minimum power margin of 3 dB.

### uClock Generation, Recovery & Distribution

Transmit clocks for the OC-3c line payloads are generated on the ATM RM from the 24.576MHz S-Link Clock, provided by the SLIF-S device. The SLIF-S phase locks this clock to the master S-Link from the active CEM. The SLIF-S provides buffering of clock and data to achieve a stable switch of data paths in the event of a CEM activity switch.

Clock recovery from the incoming optical stream is performed internal to the PM5347. In the receive direction, the PM5347 interfaces to the receiver and recovers clock and data from the incoming differential PECL data stream. The clock recovery function is performed by using an embedded PLL, which uses an external byte rate (19.44 MHz) reference. This external clock is internally multiplied by 8 and is used to improve PLL lock time and generate a 155.52 Mb/s clock in the absence of incoming data.

## Interface specifications

This part is to be used to describe the hardware, software, and firmware interfaces. The interface requirements are to be identified by the software, hardware, firmware, and silicon primes.

### Faceplate Visual Indicators

The ATM Resource Module will carry a set of indicators to provide information of interest to craft personnel. The LEDs, which are located at the faceplate, indicate the current state of the module as shown in the next table.

**Visual indicators - module status**

| Green | Red | Module state |
|---|---|---|
| Off | Off | Sleep, un-powered or not inserted |
| On | On | Power up LED test |
| Wink | Off | Power up self-test underway |
| On | Off | Module should not be removed |
| Off | On | Alarm state: module may be removed |

Power up LED test is entered immediately after the module is first powered up or inserted. Its purpose is to allow craft personnel to verify that the LEDs are

## NTLX73BB Asynchronous Transfer Mode Resource Module (end)

functional. The LEDs remain in this state for the duration of the power-up self-test.

Alarm State is entered during a power up or insertion sequence if the self-test fails, or if the Common Equipment Module rejects the module as being unworkable in the system due to incompatibilities or a failure to establish communications with the module.

The Green ON, Red OFF state is entered during power up or insertion sequence when the module has passed its diagnostic test. In this case, the module should not be removed.

When the module detects loss of signal from the external source, the LED is lit. This indicator allows the craftsperson to decide quickly whether a fault lies in the MSP itself, or at the signal source (or in connections between).

### Sleep mode

When not required, circuit module LEDs may enter a customer programmable "sleep" mode to extend their life. The LEDs will leave the sleep mode:

- when so directed by OAM S/W
- as a result of LED state change
- as part of an Indicator Test

The LEDs will not sleep while an alarm source is active (i.e. while there is a module in the peripheral in the RED ON, GREEN OFF state.).

# NTLX74AA STS-1 Interface

## Product description

### Overview

An STS-1 interface is a SONET Transport Signal, 51.84 MB/s electrical interface implemented via a 75 ohm co-axial cable. The STS-1 interface will allow Nortel's Succession Networks MG4000 platform to terminate SONET STS-1 coaxial transmission systems carrying DS3, Asynchronous VT1.5, and Byte Synchronous VT1.5 payloads, and it also maps the DS0s in those payloads to the internal format of the MG4000.

implementation of a single STS-1 trunk interface on the MG4000 with a high degree of redundancy - requires four separate elements. The STS-1 resource complex (RC), as the total assembly is referred to, consists of a STS-1 Wiring Access Assembly (WAA) and two STS-1 Unit Processor (SUP) Modules. The STS-1 Wiring Access Assembly (WAA) consists of a STS-1 mini backplane and a STS-1 Wiring Access Module (WAM).

### STS-1 unit processor - NTLX74AA

The STS-1 Unit Processor (SUP) contains the majority of the electrical circuitry necessary to implement an STS-1 interface. There are two SUPs per STS-1 interface, arranged in a 1+1 equipment sparing configuration. One SUP is active, the other SUP is in hot standby mode. The two interface with each other, the STS-1 trunk and the other cards in the MG4000 system via the STS-1 Mini backplane

## Functional description

An STS-1 interface is a SONET Transport Signal, 51.84 MB/s electrical interface implemented via a 75 ohm co-axial cable. The STS-1 interface will allow Nortel's Succession Networks MG4000 platform to terminate SONET STS-1 coaxial transmission systems carrying DS3, Asynchronous VT1.5, and Byte Synchronous VT1.5 payloads, and it also maps the DS0s in those payloads to the internal format of the MG4000.

- Single bidirectional STS-1 Line Interface (2 Resource Modules + Mini Backplane + Termination Interface Module are required per STS-1 link).
- Hardware support for 1+1 Equipment Sparing per GR499
- STS-1 Electrical Interface per GR-253-CORE
- Dedicated Processing Complex Performs:
  - — Low Level Maintenance Functions
  - — Performance Monitoring data collection
  - — SONET Overhead Termination

## NTLX74AA STS-1 Interface (continued)

- Terminates up to 672 DS0s using several different SONET payload mappings:
  - — DS3 Mapping with integrated M13 multiplexing function, 28 DS1s per DS3
  - — Floating Asynchronous VT1.5 mapping for DS1
  - — Floating Byte-Synchronous VT1.5 mapping
- Channel Associated Signaling supported by hardware
- The STS-1 Resource Module can support both M23 and C-Bit parity formats for DS3, as specified in T1.107
- Jitter performance as per GR-253-CORE, and T1.105.03
- Synchronization of incoming payloads to the CEM clock (S-Link clock from CEM) CEM clock source could be:
  - — BITS interface
  - — ATM Network
  - — STS-1 trunk if Resource Complex is provisioned in slots 4, 5 & 6
- Translation of link payload to and from the internal SPM S-Link protocol
- On-board diagnostics, self-test and JTAG capability
- Timing recovery from incoming STS-1 for distribution to SPM Common Equipment Module (CEM) if provisioned in the appropriate SPM RM slots. (4,5 & 6).
- Cat II interface with respect to Jitter requirements from GR253.

### Backward compatibility

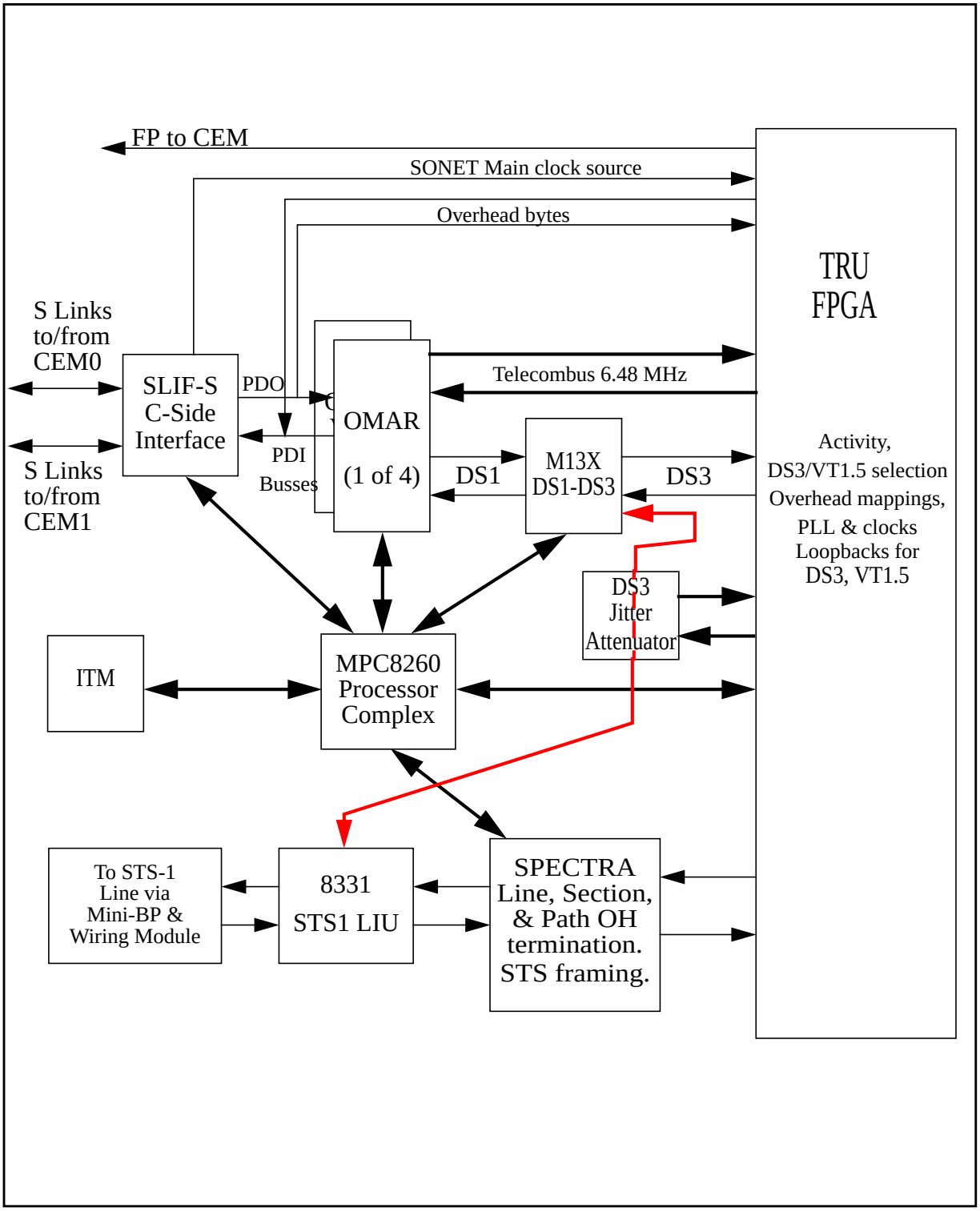
Since the STS-1 RM is a new design for the SPM, backward compatibility is not applicable. This hardware may be added to the MG4000 product without requiring any changes to pre-existing MG4000 system hardware.

### Functional block diagram

The next diagram is an illustration of the functional block diagram of the STS-1 RM.

## NTLX74AA STS-1 Interface (continued)

### NTLX74AA functional block diagram



## NTLX74AA STS-1 Interface (continued)

### Functional block descriptions

The STS-1 Resource Module is composed of several major subsections, described briefly in the following paragraphs.

#### STS-1 line interface

The heart of the STS-1 Line Interface is a Conexant 8331 STS-1 Line Interface Unit integrated component. This device terminates/originates the analog STS-1 trunk

The STS-1 LIU has no direct connection to the SUP processor. It has several I/O pins that need to be connected to the 8260 via the Altera 10K family "TRU" FPGA. These signals must be latched/registered inside the FPGA to allow the 8260 processor read/write access for configuration, control, interrupt and alarm purposes.

#### SONET framing, line, section & path overhead termination/generation

The PMC-Sierra SPECTRA155 PM5342 component, referred to as SPECTRA, performs the STS SONET line framing, line, section and path overhead termination/origination for the STS-1 trunk. The Spectra can extract/map the STS1 payload, as well as extract/map a serial DS3 into the STS1 payload.

#### DS3-DS1 M13X mapping, framing & termination

The M13 mapping function on the STS-1 Unit Processor is handled by the TranSwitch M13X Enhanced DS1 - DS3 Mux/Demux device.

#### VT1.5 OMAR mapping and framing

The OMaR is a full featured VT1.5 and DS1 termination device, providing full SF, ESF, and SLC-96 format support for M13 mapped asynchronous DS1 and STS-1 mapped byte synchronous/asynchronous VT1.5 mappings. The OMAR supports all associated overhead pertaining to the given payload format such as framing, alarms, FDL, per trunk signalling,... This allows full compatibility with a variety of legacy equipment. The OMAR also supports collection and generation of performance monitoring criterion. Each OMAR device has the capability to terminate 8 DS1 trunks (two VT groups) - for the STS-1 application, a total of 4 devices are required, with only 1/2 the capacity of the 4th device being utilized.

#### SLIF-S CEM - SUP interface

The link between the STS-1 Unit Processor and the rest of the MG4000 system is a Nortel proprietary serial link commonly referred to as the SLIF, or S-Link. All RMs' in the MG4000 system commnicate with the Common Equipment via S-Links. The CEM is the Master of the S-Link, and has a SLIF-M device. Each RM has a slave S-Link device, known as a SLIF-S, that communicates

## NTLX74AA STS-1 Interface (continued)

with the SLIF-M on the CEM via a set of dedicated point to point signals. There is one clock line and three serial data lines exchanged from a SLIF-S to the SLIF-M. Each serial line is referred to a s an S-Link. Each Slink carries 256 12 bit channels between the CEM and the RM at a 24.576 MHz rate.

### Timing and routing unit (TRU)

The TRU is a multi-faceted device implementing many important functions on the STS-1 RM. These functions are defined in the following paragraphs.

**TRU local processor access** There are several registers in the TRU that require SW control to enable proper RM functionality. The TRU has an 8 bit interface structure coming from the 8260 processor to facilitate SW access to all internal registers.

**SONET overhead insertion and extraction** The STS-1 SONET Line, Section and Path overhead channels must be made accessible to various portions of the MG4000 system, including the STS-1 Local Processor. Another issue is the continuing evolution of SONET standards, which may result in the need to terminate overhead channels currently not defined at the STS-1 RM initial release. The SONET STS-1 interface provides two methods of handling such overhead:

- Routing capabilities via the SPM CEM.
  - — Most of the SONET overhead channels in the Section, Line, and STS Path are routed to the CEM via the S-Links. This is done by the TRU FPGA - the overhead channels are extracted by the SPECTRA device, output on dedicated I/O pins and captured by the TRU. On the TRU, these overhead channels are multiplexed into the SLIF-S PDI bus so they may be transmitted by the SLIF-S to the CEM for eventual distribution to the relevant RM for further processing. The incoming channels are slip buffered in the TRU to account for any timing differences between the received STS-1 stream and the SLIFS stream.The incoming channels are slip buffered in the TRU to account for any timing differences between the received STS-1 stream and the SLIFS stream. In the opposite direction, outgoing overhead signals are picked up from the PDO bus by the TRU. The overhead bytes are then routed to the dedicated overhead pins on the SPECTRA device for incorporation into the SONET frame structure.
- On-board resources.
  - — The TRU has the capability to connect overhead bytes to the Serial controllers of the 8260 via a TDM interface. Certain overhead bytes, such as the line & section HDLC channels (D1-D3 and D4-D12

datacom channels could potentially be routed into the 8260 for HDLC termination.

There exists bits in the overhead stream that have not been tested. Any bit that is not utilized by software in the Byte Sync STS-1 functionally, has not been fully tested.

**Redundancy and protection switching (activity)** The STS-1 application on the MG4000 implements a 1+1 protection scheme. Two STS-1 RMs will be configured in an STS-1 mini backplane, along with a single STS-1 Wiring Module as depicted. Both SUPs will receive the STS-1 signal from the trunk. On the transmit side, only one SUP will actively drive the trunk. The transmit line from the other SUP will be isolated via a relay on each of the SUPs.

The circuitry that controls the relay is located in the TRU FPGA. This circuitry is referred to as the Activity circuitry. It is implemented as a State Machine. A pair of cross-connected signals is run between the SUPs to allow each activity state machine to share status information with the other.

**DS3 VT1.5 mode selection** The TRU plays a critical role in addressing a drawback of the SPECTRA device. The SPECTRA shares I/O pins between the Telecombus applications (VT 1.5) and the DS3 application. When the STS-1 RM is operating in DS3 mode, certain SPECTRA I/O pins must be routed to the M13X device. When the STS-1 RM is operating in VT1.5 mode, some of the same pins must be routed to the OMAR devices.

It is not feasible in the design to connect the two directly together - therefore, the TRU provides a multiplexing/demultiplexing function to select which device the shared pins are routed to/from. In DS3 mode, the connections are made between the SPECTRA and the M13X via the TRU. In VT1.5 mode, the connections are made between the OMAR and the SPECTRA via the TRU.

A processor accessible register will control which mode of operation the card is configured for.

**DS3 vs STS-1 selection** It is desirable, although not required, that the STS-1 RC be capable of supporting DS3. The hardware is designed to facilitate this. All DS3 signals are routed through the TRU. An extra set of DS3 I/O pins will be defined in the TRU. These extra signals will be routed to a multiplexer. The SPECTRA STS-1 signal output is also routed to the multiplexor. This muliplexor selects which signals are sent to the STS-1 LIU.

If SW chooses to run the RM in DS3 mode, the multiplexer will be set up to route the DS3 signals between the LIU and the TRU. In STS-1 mode, the

## NTLX74AA STS-1 Interface (continued)

multiplexer is set up to route the STS-1 signals between the SPECTRA and the LIU.

A processor accessible register will control the mode of operation - STS-1 or DS3. This register is in the TRU.

### Clock generation, distribution and recovery

This section contains information regarding clock generation, distribution and recovery.

**24.576 MHz clock** The SLIF-s extracts a 24.576 MHZ clock from the S-Link. This clock is generated by a PLL inside the SLIF ASIC, and is locked to the master clock coming from the CEM in order to achieve an accuracy of +/- 20 ppm. The SLIF-S also provides a 6.144 MHz clock (24.576/4) of accuracy +/- 32ppm. The 24.576 and 6.144 MHz SLIF-s originated clocks are both routed to each OMAR device and also to the TRU FPGA.

The SLIF-s also supplies the master 8 KHz timing reference from the CEM. This is used on the SUP RM to keep the different clocks phase aligned with the system master clock source.

**25.92 MHZ PLL** The STS-1 RM's 25.92 MHz PLL is used to provide a highly accurate clock source to the four OMAR devices as well as the TRU FPGA. This clock is the master clock input to the OMAR devices. It has an accuracy of +/- 20 ppm. This clock is phase locked to the CEM sourced 8 KHz phase signal in order to meet the T1.105.03 requirement that the stratum level of these clocks is the same as the system stratum level.

The 25.92 MHz clock is also routed to the TRU FPGA. Within the TRU, the clock is part of the feedback mechanism of the PLL function. Additionally, the FPGA divides this clock by 4 to generate the 6.48 MHz telecom bus clock (+/- 20 ppm), which is routed to the OMAR and the SPECTRA devices. There are phase detection registers within the TRU FPGA that SW can read to detect the phase difference of the 25.92 MHZ clock relative to the 24.576 MHz clock, and a control register that allows SW the capability to adjust the frequency of the 25.92 MHz VCXO until it is properly aligned with the 24.576 MHz clock signal.

**6.48 MHz clock** The 6.48 MHz clock is generated within the TRU FPGA from the 25.92 MHz PLL originated clock. This clock is a highly accurate +/- 20 ppm source, necessary to comply with GR-253. It is routed to the OMAR and SPECTRA devices.

Within the SPECTRA, this clock serves as the master clock source. The SPECTRA device extracts a received 51.84 MHz clock from the incoming

STS-1 signal. The SPECTRA trains the clock recovery PLL to the 6.48 MHz reference clock. Further downstream, the SPECTRA uses the 6.48 MHz clock to clock parallel data out onto the DROP bus.

In the transmit direction, the 6.48 MHz clock is used to clock data into the SPECTRA on the ADD bus. Additionally, the SPECTRA device uses this clock to synthesize the STS-1 Transmit clock frequency of 51.84 MHz. This synthesized clock is used as the source from which a gapped clock clocks data out of the DS3 elastic store and into the STS_1 synchronizer.

Within the TRU, the 6.48 MHZ clock is also used in the Telecombus application.

**6.176 MHz clock** The 6.176 MHz clock is generated from the TRU FPGA based off the 25.92 MHz clock source. This clock is a gapped clock, and is used by the OMAR devices for DS1 transmit clocking operations. This clock is 4 times the DS1 rate of 1.544 MHz.

**44.736 MHz PLL** Transmit clocks for the DS3 payload is generated on the STS-1 RM, phase locked to the CEM sourced 8 KHz reference signal provided by the SLIF-S device. The DS3 clock is routed to the M13X device, providing a minimal +/- 50 ppm degree of accuracy for the DS3 transmit operation.

Additionally, this clock is routed to the DS3 jitter attenuator. It is used to clock out the received data from the jitter attenuator into the M13X. (The received data is clocked into the jitter attenuator using the Spectra 44.736 MHz gapped clock).

The 44.736 MHz clock is also routed to the TRU FPGA, within which the digital portion of the PLL is implemented. There are phase detection registers within the TRU FPGA that SW can read to detect the phase difference of the 44.736 MHZ clock relative to the 24.576 MHz clock, and a control register that allows SW the capabilty to adjust the frequency of the 44.736 MHz VCXO until it is properly aligned with the 24.576 MHz clock signal.

**51.84 MHz STS-1 clock** In the receive direction, the 51.84 MHz STS-1 clock and the received data stream is recovered by the STS-1 LIU. The recovered clock and data are fed to the PM5342 SPECTRA.The PM5342 divides the 51.84 MHz received clock by eight and aligns the received data in byte wide format for internal SONET path termination. The PM5342 performs pointer arithmetic and adjustment on the H1 and H2 bytes to align the received data to the drop bus clock.

In DS3 mapping mode, the PM5342 SPECTRA generates a nominally 44.736 MHz DS3 clock. The 44.736 MHZ clock is generated by gapping the

## NTLX74AA STS-1 Interface (continued)

51.84MHz recovered STS1 line clock. The gapped 44.736 MHz clock is fed through an EXAR XRT7100D jitter attenuator device, which uses a PLL to smooth the gapped clock into an accurate reference. The DS3 data is also fed into this device. After the clock is de-jittered, the clock and DS3 data stream are fed back into the TRU FPGA, and then fed to the M13X DS3 - DS1 multiplexer.

**8260 processor complex** The local processor on the SONET STS-1 RM is a Motorola MPC8260 Power QUICC II, running at a clock rate of 150 MHz. The processor provides the local intelligence to perform basic module control and maintenance activities. It communicates with the CEM and services requests to establish DS0 voice trunks over STS1. It also initializes and configures the peripheral devices on the RM, executes diagnostic routines to test the module, stores the Initial Boot Loader (IBL) and the application software load in non-volatile memory, and provides both Ethernet and RS-232 interfaces for development and debug purposes.

**Point of use power supplies (PUPS)** The system feeds two independent -48V feeds into the SUP via the backplane pins. Onboard the SUP, the -48V signals are diode-or'd together, creating a single -48V feed that is subsequently passed through a fuse. The -48V feed and the -48V return (battery return) pass through an EMI filter, preventing any noise that was induced on the power cables/backplane from corrupting the supply on the SUP. After passing through the EMI filter, -48 V is fed through an inrush control circuit to limit the inrush current presented to the rest of the system by the insertion of the SUP into the shelf.

The -48V feed is routed through a shutdown FET, to two Point of Use Power Supplies, or PUPS. One converts the voltage from -48 to +5V @15Watts, the other converts -48 to 3.3V @ 33 Watts.

**Diagnostic capabilities** The NTLX74 will offer several diagnostic capabilities to address the needs of the craftsperson. This includes the following:

- STS-1 Line and System side loopbacks
- STS-1 Line and System side loopbacks
- DS3 Line side loopback
- DS1 system side loopback
- DS3 system side loopback
- VT1.5 line side loopback

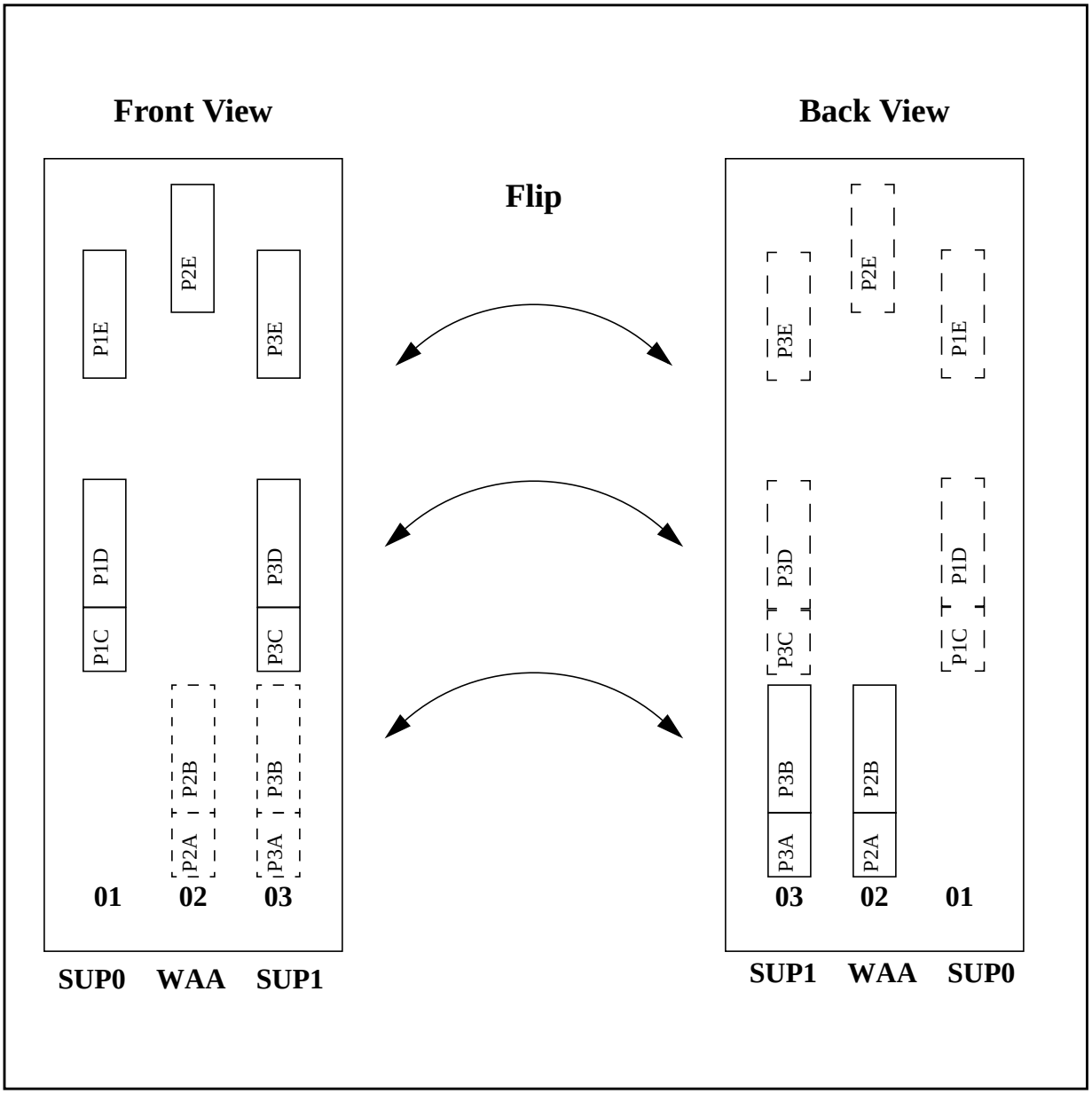
## NTLX74AA STS-1 Interface (continued)

# Interface specifications

## STS-1 backplane connectivity

The STS-1 Resource Complex has several areas of connections that need to be defined. These include the mini backplane to main backplane connections, mini backplane to STS-1 RM connections and mini backplane to STS-1 wiring module connections. The following sections document the connectivity between the different entities that make up the resource complex.

### STS-1 mini backplane connector locations, labels and types



## NTLX74AA STS-1 Interface (continued)

Prior to investigating into the actual connections between the various entities, it is necessary to identify the connectors used in the resource complex. The mini backplane will interconnect to the main backplane in two slots, labeled 02 and 03, reference the “STS-1 mini backplane connector locations, labels and types” diagram. The two connectors used on the mini-backplane for this connection are special variants of the 1SU and 2SU produced by Molex for use initially in the LSA program, and now being used in the STS-1 program

There are three connectors located on the mini backplane in slots 01 and 03 that interface to the STS-1 electronics module. These connectors are the standard 1SU/2SU backplane connectors used throughout the Spectrum product line.

### STS-1 resource complex signal definitions

This section defines the signals that connect the various entities of the STS-1 Resource Complex to each other, as well as to the main Spectrum backplane. Ground signal definitions are not included in this section.

#### Power signal definitions

This section attempts to present a unified view of the signal connectivity between the different entities making up the STS-1 Resource Complex. The next table defines the functions of the signals contained in connectors P2A, P3A, P1C and P3C.

**STS-1 resource complex to main BP power/RTN signal definitions**

| Signal | Connector P2A, P3A, Pin# | Connector P1C, P3C Pin # | Purpose/Description |
|---|---|---|---|
| -48B | 2A - 2E | 2A - 2E | -48 V B feed from Main backplane to STS-1 RM via Mini Backplane |
| -48A | 8A - 8E | 8A - 8E | -48V A feed from main backplane to STS-1 RM via Mini Backplane |
| RTN | 5A - 5E | 5A - 5E | Battery return from STS-1 RM to main backplane via Mini Backplane |

### STS-1 unit processor 0 to main backplane signal definitions

The next table defines the signals that make up the connections between the main Spectrum backplane and the STS-1 Unit Processor in slot 1 of the STS-1

mini backplane via the STS-1 Mini Backplane. In this table, SUP1 refers to the STS-1 Unit Processor located in slot1 of the STS-1 RCM.

**STS-1 unit processor 0 to main BP signal definitions**

| Signal | Connector P2B Pin # | Connector P1D Pin # | Purpose/Description |
|---|---|---|---|
| SYNC_ToCEM0S1 | 2A | 2A | Recovered Frame Pulse sent to CEM0 from SUP1 |
| SYNC_ToCEM1S1 | 3A | 3A | Recovered Frame Pulse sent to CEM1 from SUP1 |
| ToCEM0_D1S1 | 7A | 7A | S-Link Data Line #1 to CEM0 from SUP1 |
| ToCEM0_D2S1 | 8A | 8A | S-Link Data Line #2 to CEM0 from SUP1 |
| FrCEM0_D1S1 | 9A | 9A | S-Link Data Line #1 to SUP1 from CEM0 |
| FrCEM0_D2S1 | 10A | 10A | S-Link Data Line #2 to SUP1 from CEM0 |
| SLOT_ID4S1 | 16A | 16A | Slot ID bit #4 from main backplane to SUP1 |
| MMD_S1 | 18A | 18A | JTAG 1149.5 Bus Slave Data input into SUP1 from CEM |
| ToCEM0_D0S1 | 7B | 7B | S-Link Data Line #0 from SUP1 to CEM0 |
| ToCEM0_CKS1 | 8B | 8B | S-Link Clock Line from SUP1 to CEM0 |
| FrCEM0_D0S1 | 9B | 9B | S-Link Data Line #0 from CEM0 to SUP1 |
| FrCEM0_CKS1 | 10B | 10B | S-Link Clock Line from CEM0 to SUP1 |
| SLOT_ID3S1 | 16B | 16B | Slot ID bit #3 from main backplane to SUP1 |

## NTLX74AA STS-1 Interface (continued)

**STS-1 unit processor 0 to main BP signal definitions**

| Signal | Connector P2B Pin # | Connector P1D Pin # | Purpose/Description |
|---|---|---|---|
| MPR_S1 | 17B | 17B | JTAG 1149.5 Bus Request input from CEM to SUP1 |
| MCTL_S1 | 16C | 16C | JTAG 1149.5 Bus Control input from CEM to SUP1 |
| SLOT_ID2S1 | 17C | 17C | Slot ID bit#2 from main backplane to SUP1 |
| ToCEM1_D0S1 | 7D | 7D | S-Link data line #0 from SUP1 to CEM1 |
| ToCEM1_CKS1 | 8D | 8D | S-Link clock line from SUP1 to CEM1 |
| FrCEM1_D0S1 | 9D | 9D | S-Link data line #0 from CEM1 to SUP1 |
| FrCEM1_CKS1 | 10D | 10D | S-Link clock line from CEM1 to SUP1 |
| SLOT_ID1S1 | 16D | 16D | Slot ID bit #1 from main backplane to SUP1 |
| MCLK_S1 | 17D | 17D | JTAG 1149.5 clock input from CEM to SUP1 |
| ToCEM1_D1S1 | 7E | 7E | S-Link data line #1 from SUP1 to CEM1 |
| ToCEM1_D2S1 | 8E | 8E | S-Link data line #2 from SUP1 to CEM1 |
| FrCEM1_D1S1 | 9E | 9E | S-Link data line #1 from CEM1 to SUP1 |
| FrCEM1_D2S1 | 10E | 10E | S-Link data line #2 from CEM1 to SUP1 |

**STS-1 unit processor 0 to main BP signal definitions**

| Signal | Connector P2B Pin # | Connector P1D Pin # | Purpose/Description |
|---|---|---|---|
| SLOT_ID0S1 | 16E | 16E | Slot ID bit #0 from main backplane to SUP1 |
| MSD_S1 | 17E | 17E | JTAG 1149.5 slave data output from SUP1 to CEM |

### STS-1 unit processor 1 to main backplane signal definitions

The next table defines the signals that make up the connections between the main Spectrum backplane and the STS-1 Unit Processor in slot 3 of the STS-1 mini backplane via the STS-1 Mini Backplane. In this table, SUP3 refers to the STS-1 Unit Processor located in slot 3 of the STS-1 mini backplane.

**STS-1 unit processor 1 to main backplane signal definitions**

| Signal | Connector P3B | Connector P3D | Purpose/Description |
|---|---|---|---|
| SYNC_ToCEM0S3 | 2A | 2A | Recovered Frame Pulse sent to CEM0 from SUP3 |
| SYNC_ToCEM1S3 | 3A | 3A | Recovered Frame Pulse sent to CEM1 from SUP3 |
| ToCEM0_D1S3 | 7A | 7A | S-Link Data Line #1 to CEM0 from SUP3 |
| ToCEM0_D2S3 | 8A | 8A | S-Link Data Line #2 to CEM0 from SUP3 |
| FrCEM0_D1S3 | 9A | 9A | S-Link Data Line #1 to SUP3 from CEM0 |
| FrCEM0_D2S3 | 10A | 10A | S-Link Data Line #2 to SUP3 from CEM0 |
| SLOT_ID4S3 | 16A | 16A | Slot ID bit #4 from main backplane to SUP3 |
| MMD_S3 | 18A | 18A | JTAG 1149.5 Bus Slave Data input into SUP3 from CEM |

## NTLX74AA STS-1 Interface (continued)

**STS-1 unit processor 1 to main backplane signal definitions**

| Signal | Connector P3B | Connector P3D | Purpose/Description |
|---|---|---|---|
| ToCEM0_D0S3 | 7B | 7B | S-Link Data Line #0 from SUP3 to CEM0 |
| ToCEM0_CKS3 | 8B | 8B | S-Link Clock Line from SUP3 to CEM0 |
| FrCEM0_D0S3 | 9B | 9B | S-Link Data Line #0 from CEM0 to SUP3 |
| FrCEM0_CKS3 | 10B | 10B | S-Link Clock Line from CEM0 to SUP3 |
| SLOT_ID3S3 | 16B | 16B | Slot ID bit #3 from main backplane to SUP3 |
| MPR_S3 | 17B | 17B | JTAG 1149.5 Bus Request input from CEM to SUP3 |
| MCTL_S3 | 16C | 16C | JTAG 1149.5 Bus Control input from CEM to SUP3 |
| SLOT_ID2S3 | 17C | 17C | Slot ID bit#2 from main backplane to SUP3 |
| ToCEM1_D0S3 | 7D | 7D | S-Link data line #0 from SUP3 to CEM1 |
| ToCEM1_CKS3 | 8D | 8D | S-Link clock line from SUP3 to CEM1 |
| FrCEM1_D0S3 | 9D | 9D | S-Link data line #0 from CEM1 to SUP3 |
| FrCEM1_CKS3 | 10D | 10D | S-Link clock line from CEM1 to SUP3 |
| SLOT_ID1S3 | 16D | 16D | Slot ID bit #1 from main backplane to SUP3 |
| MCLK_S3 | 17D | 17D | JTAG 1149.5 clock input from CEM to SUP3 |
| ToCEM1_D1S3 | 7E | 7E | S-Link data line #1 from SUP3 to CEM1 |

**STS-1 unit processor 1 to main backplane signal definitions**

| Signal | Connector P3B | Connector P3D | Purpose/Description |
|---|---|---|---|
| ToCEM1_D2S3 | 8E | 8E | S-Link data line #2 from SUP3 to CEM1 |
| FrCEM1_D1S3 | 9E | 9E | S-Link data line #1 from CEM1 to SUP3 |
| FrCEM1_D2S3 | 10E | 10E | S-Link data line #2 from CEM1 to SUP3 |
| SLOT_ID0S3 | 16E | 16E | Slot ID bit #0 from main backplane to SUP3 |
| MSD_S3 | 17E | 17E | JTAG 1149.5 slave data output from SUP3 to CEM |

### SUP0 to SUP1 signal definitions

The next table defines the signals that are used to connect the two STS-1 RMs together across the STS1 mini-backplane using connectors P1D and P3D only

**SUP0 to SUP1 connections through the mini-backplane P1D and P3D - definitions**

| Signal | Connector P1D | Connector P3D | Purpose/Description |
|---|---|---|---|
| ToSRM_MateS3 | 3D | 3B | Sync signal from SUP slot 3 to SUP slot 1 |
| FrSRM_MateS3 | 3B | 3D | Sync signal from SUP slot 1 to SUP slot 3 |

The next table defines the signals that are used to connect the two STS-1 RMs together across the STS1 mini-backplane using connectors P1D and P3D only. Signals that also run onto the WAA are not listed in this table.

**SUP0 to SUP1 connections through the mini-backplane P1E and P3E - definitions**

| Signal | Connector P1E | Connector P3E | Purpose/Description |
|---|---|---|---|
| OWNOUT | 14D | 15D | Activity status from SUP0 to SUP1 |
| MATEIN | 15D | 14D | Activity status from SUP1 to SUP0 |

## NTLX74AA STS-1 Interface (continued)

**SUP0 to SUP1 connections through the mini-backplane P1E and P3E - definitions**

| Signal | Connector P1E | Connector P3E | Purpose/Description |
|---|---|---|---|
| SPARE_OUT | 17D | 18D | Spare cross connect signal 0 |
| SPARE_IN | 18D | 17D | Spare cross connect signal 1 |

### SUP0 to SUP1 to WAA signal definitions

The next table defines the signals that make up the connectivity between STS-1 Unit Processor 0, STS-1 Unit Processor 1 and the Wiring Access Assembly RM, going through the STS1 RCM via the "E" connectors only. SUP1 is the STS1 Unit Processor in slot 1 of the RCM, SUP3 is the STS1 Unit Processor in slot 3 of the RCM.

**SUP0 - WAA - SUP1 mini-backplane connector "E" signal definitions**

| Signal | Connector P11 or SUP1 | Connector P1E on RCM | Connector P2E on RCM P1 on WAA | Connector P11 on SUP3 | Conn. or P3E on RCM | Purpose/ Description |
|---|---|---|---|---|---|---|
| TXS1S3 | 3A | 3A | 5A | 3A | 3A | STS-1 Trunk Tx output from SUP1/SUP3 to WAA |
| TX_S1 | 5A | 5A | 7A | nc | nc | STS-1 Trunk Tx output from SUP1 to WAA |
| TX_S3 | nc | nc | 9A | 5A | 5A | STS-1 Trunk Tx output from SUP3 to WAA |
| RX_TIP_S1 | 7A | 7A | 11A | nc | nc | STS-1 Trunk TIP Rx input from WAA to SUP1 |
| RX_RING_S1 | 8A | 8A | 12A | nc | nc | STS-1 Trunk RING Rx input from WAA to SUP1 |
| RX_TIP_S3 | nc | nc | 14A | 7A | 7A | STS-1 Trunk TIP Rx input from WAA to SUP3 |

## NTLX74AA STS-1 Interface (continued)

**SUP0 - WAA - SUP1 mini-backplane connector “E” signal definitions**

| Signal | Connect or P11 or SUP1 | Connect or P1E on RCM | Connect or P2E on RCM P1 on WAA | Connect or P11 on SUP3 | Conn. or P3E on RCM | Purpose/ Description |
|---|---|---|---|---|---|---|
| RX_RING_S3 | nc | nc | 15A | 8A | 8A | STS-1 Trunk RING Rx input from WAA to SUP3 |
| RELAY_LO | 8E | 8E - nc | 13E | 8E | 8E | Tx relay control lo |
| RELAY_HI | 9E | 9E - nc | 14E | 9E | 9E | Tx relay control hi |
| SENSE_HI | 9C | 9C | 16C | 9C | 9C | Sense relay coil high side |
| SENSE_LO | 11C | 11C | 18C | 11C | 11C | Sense relay coil low side |
| WAA_VER00 | 11E | 11E | 16E | 11E | 11E | Wiring Access Assembly version bit 0 |
| WAA_VER01 | 12E | 12E | 17E | 12E | 12E | Wiring Access Assembly version bit 1 |
| WAA_VER02 | 13E | 13E | 18E | 13E | 13E | Wiring Access Assembly version bit 2 |
| OWNOUT | 14D | 14D | nc | 14D | 14D | Activity status from SUP0 to SUP1 |
| MATEIN | 15D | 15D | nc | 15D | 15D | Activity status from SUP1 to SUP0 |
| RCM_SLOT_S1 | 18A | 18A-gnd | nc | nc | nc | RCM Slot ID - slot 1- no connections across the RCM |
| RCM_SLOT_S3 | nc | nc | nc | 18A - Open | 18A | RCM Slot ID - slot 3 - no connections across RCM |

## NTLX74AA STS-1 Interface (continued)

**SUP0 - WAA - SUP1 mini-backplane connector "E" signal definitions**

| Signal | Connect or P11 or SUP1 | Connect or P1E on RCM | Connect or P2E on RCM P1 on WAA | Connect or P11 on SUP3 | Conn. or P3E on RCM | Purpose/ Description |
|---|---|---|---|---|---|---|
| SPARE_OUT | 17D | 17D | nc | 18D | 17D | Spare cross connect signal 0 |
| SPARE_IN | 18D | 18D | nc | 17D | 18D | Spare cross connect signal 1 |

## STS-1 resource complex connector pin assignments

This section identifies the signal assigned to each pin on each connector that makes up the STS-1 Resource Complex.

### Pin assignments - mini-BP to main BP connectors P2A and P3A

The connections between the STS-1 mini-backplane and the MG4000 main backplane are made through two connectors per slot. A Molex type 1SU connector provides two -48V feeds and a return between the main and mini-backplanes.

The next table lists the pin assignments for the mini to main backplane 1SU connector.

**Main BP to mini-BP ISU connector P2A, P3A pin assignments**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | -48B | -48B | -48B | -48B | -48B |
| 3 | NC | NC | NC | NC | NC |
| 4 | NC | NC | NC | NC | NC |
| 5 | RTN | RTN | RTN | RTN | RTN |
| 6 | NC | NC | NC | NC | NC |
| 7 | NC | NC | NC | NC | NC |
| 8 | -48A | -48A | -48A | -48A | -48A |

### Pin assignments - mini-BP to main BP connectors P2B and P3B

The exchange of all logic signals between the main and mini-backplanes is handled by a Molex type 2SU connector. The 2SU connectors between the

mini and main backplanes are labeled as P2B and P3B. The next table lists the pinout for P2B as mounted on the mini-backplane.

**Main BP to mini-BP 2SU connector P2B pin assignments**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | SYNC_ToCEM 0S1 | GND | GND | GND | .NC. |
| 3 | SYNC_ToCEM 1S1 | .NC. | GND | .NC. | .NC. |
| 4 | GND | GND | GND | GND | GND |
| 5 | FRMFLS1 | .NC. | GND | .NC. | .NC. |
| 6 | .NC. | .NC. | GND | .NC. | .NC. |
| 7 | ToCEM0_D1S1 | ToCEM0_D0S1 | GND | ToCEM1_D0S1 | ToCEM1_D1S1 |
| 8 | ToCEM0_D2S1 | ToCEM0_CKS 1 | GND | ToCEM1_CKS 1 | ToCEM1_D2S1 |
| 9 | FrCEM0_D1S1 | FrCEM0_D0S1 | GND | FrCEM1_D0S1 | FrCEM1_D1S1 |
| 10 | FrCEM0_D2S1 | FrCEM0_CKS1 | GND | FrCEM1_CKS1 | FrCEM1_D2S1 |
| 11 | GND | GND | GND | GND | GND |
| 12 | .NC. | .NC. | GND | .NC. | .NC. |
| 13 | .NC. | .NC. | GND | .NC. | .NC. |
| 14 | .NC. | .NC. | GND | .NC. | .NC. |
| 15 | .NC. | .NC. | GND | .NC. | .NC. |
| 16 | SLOT_ID4S1 | SLOT_ID3S1 | MCTLS1 | SLOT_ID1S1 | SLOT_ID0S1 |
| 17 | GND | MPRS1 | SLOT_ID2S1 | MCLKS1 | GND |
| 18 | MMDS1 | GND | GND | GND | MSDS1 |

## NTLX74AA STS-1 Interface (continued)

The next table lists the pinout for STS-1 mini-backplane connector P3B.

**Main BP to mini-BP 2SU connector P3B pin assignments**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | SYNC_ToCEM 0S3 | GND | GND | GND | .NC. |
| 3 | SYNC_ToCEM 1S3 | .NC. | GND | .NC. | .NC. |
| 4 | GND | GND | GND | GND | GND |
| 5 | FRMFLS3 | .NC. | GND | .NC. | .NC. |
| 6 | .NC. | .NC. | GND | .NC. | .NC. |
| 7 | ToCEM0_D1S 3 | ToCEM0_D0S 3 | GND | ToCEM1_D0S 3 | ToCEM1_D1S 3 |
| 8 | ToCEM0_D2S 3 | ToCEM0_CKS 3 | GND | ToCEM1_CKS 3 | ToCEM1_D2S 3 |
| 9 | FrCEM0_D1S3 | FrCEM0_D0S3 | GND | FrCEM1_D0S3 | FrCEM1_D1S3 |
| 10 | FrCEM0_D2S3 | FrCEM0_CKS3 | GND | FrCEM1_CKS3 | FrCEM1_D2S3 |
| 11 | GND | GND | GND | GND | GND |
| 12 | .NC. | .NC. | GND | .NC. | .NC. |
| 13 | .NC. | .NC. | GND | .NC. | .NC. |
| 14 | .NC. | .NC. | GND | .NC. | .NC. |
| 15 | .NC. | .NC. | GND | .NC. | .NC. |
| 16 | SLOT_ID4S3 | SLOT_ID3S3 | MCTLS3 | SLOT_ID1S3 | SLOT_ID0S3 |
| 17 | GND | MPRS3 | SLOT_ID2S3 | MCLKS3 | GND |
| 18 | MMDS3 | GND | GND | GND | MSDS3 |

## Pin assignments - mini-backplane slot 1

The pinout definition for connector P1D, joining SUP0 with the mini-backplane, is listed in the next table.

**Mini-backplane 2SU connector P1D pin assignments**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | SYNC_ToCEM0 S1 | GND | GND | GND | .NC. |
| 3 | SYNC_ToCEM1 S1 | .NC. | GND | .NC. | .NC. |
| 4 | GND | GND | GND | GND | GND |
| 5 | FRMFLS1 | .NC. | GND | .NC. | .NC. |
| 6 | .NC. | .NC. | GND | .NC. | .NC. |
| 7 | ToCEM0_D1S1 | ToCEM0_D0S1 | GND | ToCEM1_D0S1 | ToCEM1_D1S1 |
| 8 | ToCEM0_D2S1 | ToCEM0_CKS1 | GND | ToCEM1_CKS1 | ToCEM1_D2S1 |
| 9 | FrCEM0_D1S1 | FrCEM0_D0S1 | GND | FrCEM1_D0S1 | FrCEM1_D1S1 |
| 10 | FrCEM0_D2S1 | FrCEM0_CKS1 | GND | FrCEM1_CKS1 | FrCEM1_D2S1 |
| 11 | GND | GND | GND | GND | GND |
| 12 | .NC. | .NC. | GND | .NC. | .NC. |
| 13 | .NC. | .NC. | GND | .NC. | .NC. |
| 14 | .NC. | .NC. | GND | .NC. | .NC. |
| 15 | .NC. | .NC. | GND | .NC. | .NC. |
| 16 | SLOT_ID4S1 | SLOT_ID3S1 | MCTLS1 | SLOT_ID1S1 | SLOT_ID0S1 |
| 17 | GND | MPRS1 | SLOT_ID2S1 | MCLKS1 | GND |
| 18 | MMDS1 | GND | GND | GND | MSDS1 |

The next table lists pin assignments for Resource Complex mini-backplane connector P1E.

## NTLX74AA STS-1 Interface (continued)

**Mini-backplane 2SU connector P1E pin assignments**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | NC | GND | GND | NC | GND |
| 3 | TX_S1S3 | NC | GND | NC | GND |
| 4 | GND | GND | GND | NC | GND |
| 5 | TX_S1 | NC | GND | NC | GND |
| 6 | GND | GND | GND | NC | GND |
| 7 | RX_TIP_S1 | NC | GND | NC | GND |
| 8 | RX_RING_S1 | NC | GND | NC | RELAY_LO |
| 9 | GND | NC | SENSE_HI | NC | RELAY_HI |
| 10 | GND | GND | GND | NC | GND |
| 11 | GND | NC | SENSE_LO | NC | WAA_VER00 |
| 12 | GND | GND | GND | NC | WAA_VER01 |
| 13 | GND | GND | GND | NC | WAA_VER02 |
| 14 | GND | GND | NC | OWN_OUT | NC |
| 15 | GND | GND | NC | MATE_IN | NC |
| 16 | GND | GND | GND | GND | GND |
| 17 | GND | GND | NC | SPARE_OUT | NC |
| 18 | RCM_SLOT_S 1 (GND on Mini BP) | NC | NC | SPARE_IN | NC |

Power & ground pin assignments are listed in the next table for SUP in slot 1.

**Mini-backplane 1SU connector P1E pin assignments**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | -48B | -48B | -48B | -48B | -48B |
| 3 | NC | NC | NC | NC | NC |
| 4 | NC | NC | NC | NC | NC |
| 5 | RTN | RTN | RTN | RTN | RTN |
| 6 | NC | NC | NC | NC | NC |
| 7 | NC | NC | NC | NC | NC |
| 8 | -48A | -48A | -48A | -48A | -48A |

## Pin assignments - mini-backplane slot 3

Power & ground pin assignments are listed in the next table for SUP in slot 3.

**Mini-backplane 1SU connector P3E pin assignments**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | -48B | -48B | -48B | -48B | -48B |
| 3 | NC | NC | NC | NC | NC |
| 4 | NC | NC | NC | NC | NC |
| 5 | RTN | RTN | RTN | RTN | RTN |
| 6 | NC | NC | NC | NC | NC |
| 7 | NC | NC | NC | NC | NC |
| 8 | -48A | -48A | -48A | -48A | -48A |

This section lists the pin assignments for connector P3D, which connects the STS-1 Unit Processor with slot 3 of the STS-1 mini-backplane.

## NTLX74AA STS-1 Interface (continued)

**Mini-backplane 2SU connector P3D pin assignments**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | SYNC_ToCEM0S3 | GND | GND | GND | .NC. |
| 3 | SYNC_ToCEM1S3 | .NC. | GND | .NC. | .NC. |
| 4 | GND | GND | GND | GND | GND |
| 5 | FRMFLS3 | .NC. | GND | .NC. | .NC. |
| 6 | .NC. | .NC. | GND | .NC. | .NC. |
| 7 | ToCEM0_D1S3 | ToCEM0_D0S3 | GND | ToCEM1_D0S3 | ToCEM1_D1S3 |
| 8 | ToCEM0_D2S3 | ToCEM0_CKS3 | GND | ToCEM1_CKS3 | ToCEM1_D2S3 |
| 9 | FrCEM0_D1S3 | FrCEM0_D0S3 | GND | FrCEM1_D0S3 | FrCEM1_D1S3 |
| 10 | FrCEM0_D2S3 | FrCEM0_CKS3 | GND | FrCEM1_CKS3 | FrCEM1_D2S3 |
| 11 | GND | GND | GND | GND | GND |
| 12 | .NC. | .NC. | GND | .NC. | .NC. |
| 13 | .NC. | .NC. | GND | .NC. | .NC. |
| 14 | .NC. | .NC. | GND | .NC. | .NC. |
| 15 | .NC. | .NC. | GND | .NC. | .NC. |
| 16 | SLOT_ID4S3 | SLOT_ID3S3 | MCTLS3 | SLOT_ID1S3 | SLOT_ID0S3 |
| 17 | GND | MPRS3 | SLOT_ID2S3 | MCLKS3 | GND |
| 18 | MMDS3 | GND | GND | GND | MSDS3 |

## NTLX74AA STS-1 Interface (continued)

The next table lists the connections on the Resource Complex mini-backplane connector P3E that connects to SUP.

**Mini-backplane 2SU connector P3D pin assignments**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | NC | GND | GND | NC | GND |
| 3 | TXS1S3 | NC | GND | NC | GND |
| 4 | GND | GND | GND | NC | GND |
| 5 | TX_S3 | NC | GND | NC | GND |
| 6 | GND | GND | GND | NC | GND |
| 7 | RX_TIP_S3 | NC | GND | NC | GND |
| 8 | RX_RING_S3 | NC | GND | NC | RELAY_LO |
| 9 | GND | NC | SENSE_HI | NC | RELAY_HI |
| 10 | GND | GND | GND | NC | GND |
| 11 | GND | NC | SENSE_LO | NC | WAA_VER00 |
| 12 | GND | GND | GND | NC | WAA_VER01 |
| 13 | GND | GND | GND | NC | WAA_VER02 |
| 14 | GND | GND | NC | OWN_OUT | NC |
| 15 | GND | GND | NC | MATE_IN | NC |
| 16 | GND | GND | GND | GND | GND |
| 17 | GND | GND | NC | SPARE_OUT | NC |
| 18 | RCM_SLOT_S 3 (Open on Mini BP) | NC | NC | SPARE_IN | NC |

## NTLX74AA STS-1 Interface (continued)

### Pin assignments - mini-backplane slot 2

This section lists the pin assignments for mini-backplane 2SU connector P2E, which connects with the STS-1 WAA in slot 2 of the mini-backplane.

**Mini-backplane 2SU connector P2E pin assignments**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | NC | GND | GND | NC | GND |
| 3 | NC | GND | GND | NC | GND |
| 4 | GND | GND | GND | NC | GND |
| 5 | TX_S1S3 | NC | GND | NC | GND |
| 6 | GND | GND | GND | NC | GND |
| 7 | TX_S1 | NC | GND | NC | GND |
| 8 | GND | GND | GND | NC | GND |
| 9 | TX_S3 | NC | GND | NC | GND |
| 10 | GND | GND | GND | NC | GND |
| 11 | RX_TIP_S1 | NC | GND | NC | GND |
| 12 | RX_RING_S1 | NC | GND | NC | GND |
| 13 | GND | GND | GND | NC | RELAY_LO |
| 14 | RX_TIP_S3 | NC | GND | NC | RELAY_HI |
| 15 | RX_RING_S3 | NC | GND | NC | GND |
| 16 | GND | NC | SENSE_HI | NC | WAA_VER00 |
| 17 | NC | GND | GND | NC | WAA_VER01 |
| 18 | GND | NC | SENSE_LO | NC | WAA_VER02 |

## STS-1 unit processor pin assignments

### Power and battery return connections - STS1 unit processor

All power and return signals on the SUP card are routed through 1SU connectors.The pin assignment of these connectors is per the next table.

**STS-1 electronics module 1SU connector pin assignment**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | -48B | -48B | -48B | -48B | -48B |
| 3 | NC | NC | NC | NC | NC |
| 4 | NC | NC | NC | NC | NC |
| 5 | RTN | RTN | RTN | RTN | RTN |
| 6 | NC | NC | NC | NC | NC |
| 7 | NC | NC | NC | NC | NC |
| 8 | -48A | -48A | -48A | -48A | -48A |

### Spectrum interface signals - STS-1 unit processor

All Spectrum interface signals on the USP card are routed through a 2SU connector onto the mini-backplane and to the main Spectrum backplane. This connector contains all “standard” Spectrum RM backplane signals.

**SUP standard spectrum 2SU connector pin assignment**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | SYNC_ToCEM 0 | GND | GND | GND | .NC. |
| 3 | SYNC_ToCEM 1 | .NC. | GND | .NC. | .NC. |
| 4 | GND | GND | GND | GND | GND |
| 5 | FRMFLL | .NC. | GND | .NC. | .NC. |
| 6 | .NC. | .NC. | GND | .NC. | .NC. |
| 7 | ToCEM0_D1 | ToCEM0_D0 | GND | ToCEM1_D0 | ToCEM1_D1 |
| 8 | ToCEM0_D2 | ToCEM0_CK | GND | ToCEM1_CK | ToCEM1_D2 |
| 9 | FrCEM0_D1 | FrCEM0_D0 | GND | FrCEM1_D0 | FrCEM1_D1 |

## NTLX74AA STS-1 Interface (continued)

**SUP standard spectrum 2SU connector pin assignment**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 10 | FrCEM0_D2 | FrCEM0_CK | GND | FrCEM1_CK | FrCEM1_D2 |
| 11 | GND | GND | GND | GND | GND |
| 12 | .NC. | .NC. | GND | .NC. | .NC. |
| 13 | .NC. | .NC. | GND | .NC. | .NC. |
| 14 | .NC. | .NC. | GND | .NC. | .NC. |
| 15 | .NC. | .NC. | GND | .NC. | .NC. |
| 16 | SLOT_ID4 | SLOT_ID3 | MCTL | SLOT_ID1 | SLOT_ID0 |
| 17 | GND | MPR | SLOT_ID2 | MCLK | GND |
| 18 | MMD | GND | GND | GND | MSD |

### STS-1 specific backplane signals - STS-1 unit processor

Signals specific to the STS-1 Resource Complex are routed through a separate 2SU connector on the STS-1 Unit Processor. This table lists the pin assignments of this connector.

**SUP STS-1 specific signals - 2SU connector pin assignment**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | NC | GND | GND | NC | GND |
| 3 | TXS1S3 | NC | GND | NC | GND |
| 4 | GND | GND | GND | NC | GND |
| 5 | TX | NC | GND | NC | GND |
| 6 | GND | GND | GND | NC | GND |
| 7 | RX_TIP | NC | GND | NC | GND |
| 8 | RX_RING | NC | GND | NC | RELAY_LO |
| 9 | GND | NC | WAA_SEN_HI | NC | RELAY_HI |
| 10 | GND | GND | GND | NC | GND |
| 11 | GND | NC | WAA_SEN_LO | NC | WAA_VER00 |

## NTLX74AA STS-1 Interface (continued)

**SUP STS-1 specific signals - 2SU connector pin assignment**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 12 | GND | GND | GND | NC | WAA_VER01 |
| 13 | GND | GND | GND | NC | WAA_VER02 |
| 14 | GND | GND | NC | OWN_OUT | NC |
| 15 | GND | GND | NC | MATE_IN | NC |
| 16 | GND | GND | GND | GND | GND |
| 17 | GND | GND | NC | SPARE_OUT | NC |
| 18 | RCM_SLOT | NC | NC | SPARE_IN | NC |

### STS-1 wiring access assembly 2SU connector pin assignments

There is only one connector on the WAA, a 2SU Molex backplane connector. All connections between the WAA, both SUPs and the mini-backplane are made through this connector.

**Wiring access assembly 2SU connector pin assignment**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | NC | GND | GND | NC | GND |
| 3 | NC | GND | GND | NC | GND |
| 4 | GND | GND | GND | NC | GND |
| 5 | TXS1S3 | NC | GND | NC | GND |
| 6 | GND | GND | GND | NC | GND |
| 7 | TX_S1 | NC | GND | NC | GND |
| 8 | GND | GND | GND | NC | GND |
| 9 | TX_S3 | NC | GND | NC | GND |
| 10 | GND | GND | GND | NC | GND |
| 11 | RX_TIP_S1 | NC | GND | NC | GND |
| 12 | RX_RING_S1 | NC | GND | NC | GND |
| 13 | GND | GND | GND | NC | RELAY_LO |

## NTLX74AA STS-1 Interface (continued)

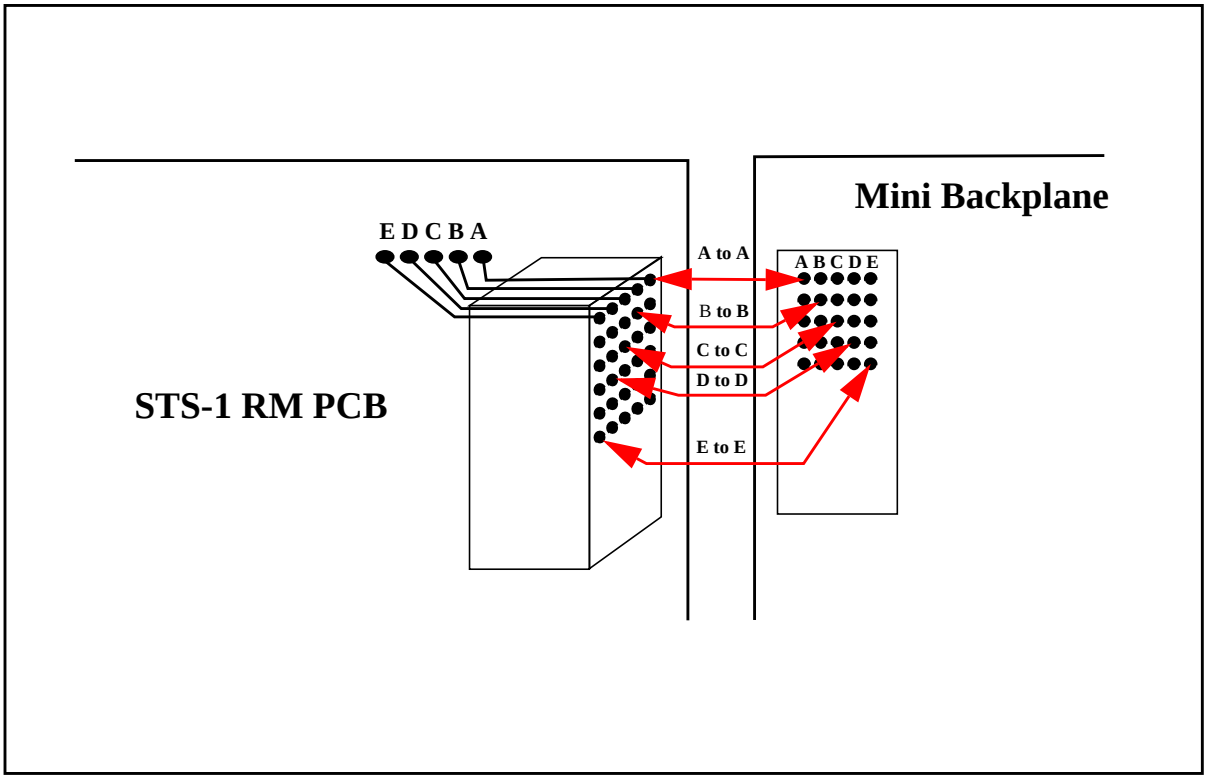
**Wiring access assembly 2SU connector pin assignment**

| Pin# | A | B | C | D | E |
|---|---|---|---|---|---|
| 14 | RX_TIP_S3 | NC | GND | NC | RELAY_HI |
| 15 | RX_RING_S3 | NC | GND | NC | GND |
| 16 | GND | NC | SENSE_HI | NC | WAA_VER00 |
| 17 | NC | GND | GND | NC | WAA_VER01 |
| 18 | GND | NC | SENSE_LO | NC | WAA_VER02 |

It is important to note that the pinouts on the mini-backplane connector are identical to those of the connector mounted on the STS-1 Resource module. The pins are arranged on the connectors such that pin 2A of the 1SU mini-backplane connector will mate with pin 2A of the 1SU connector mounted on the resource module. This is illustrated in the next figure. Additionally, the “A” row of pins is closest to the PCB - all STS-1 trunks are routed through the “A” row of pins, keeping these high speed signals as close to the PCB as possible.

# NTLX74AA STS-1 Interface (end)

**Interfacing of connector pins, identification of pin numbers**



# NTLX83AA Multi-Service Gateway 4000

## Product description

### Overview

The Succession Multi-service Gateway 4000 provides a series of frame, shelf, and module based visual indicators to act as “health” monitors for various parts of the whole system. The MG 4000 is a multi-application high-speed peripheral platform for the Digital Multiplex System (DMS) family, or third party central office switches.

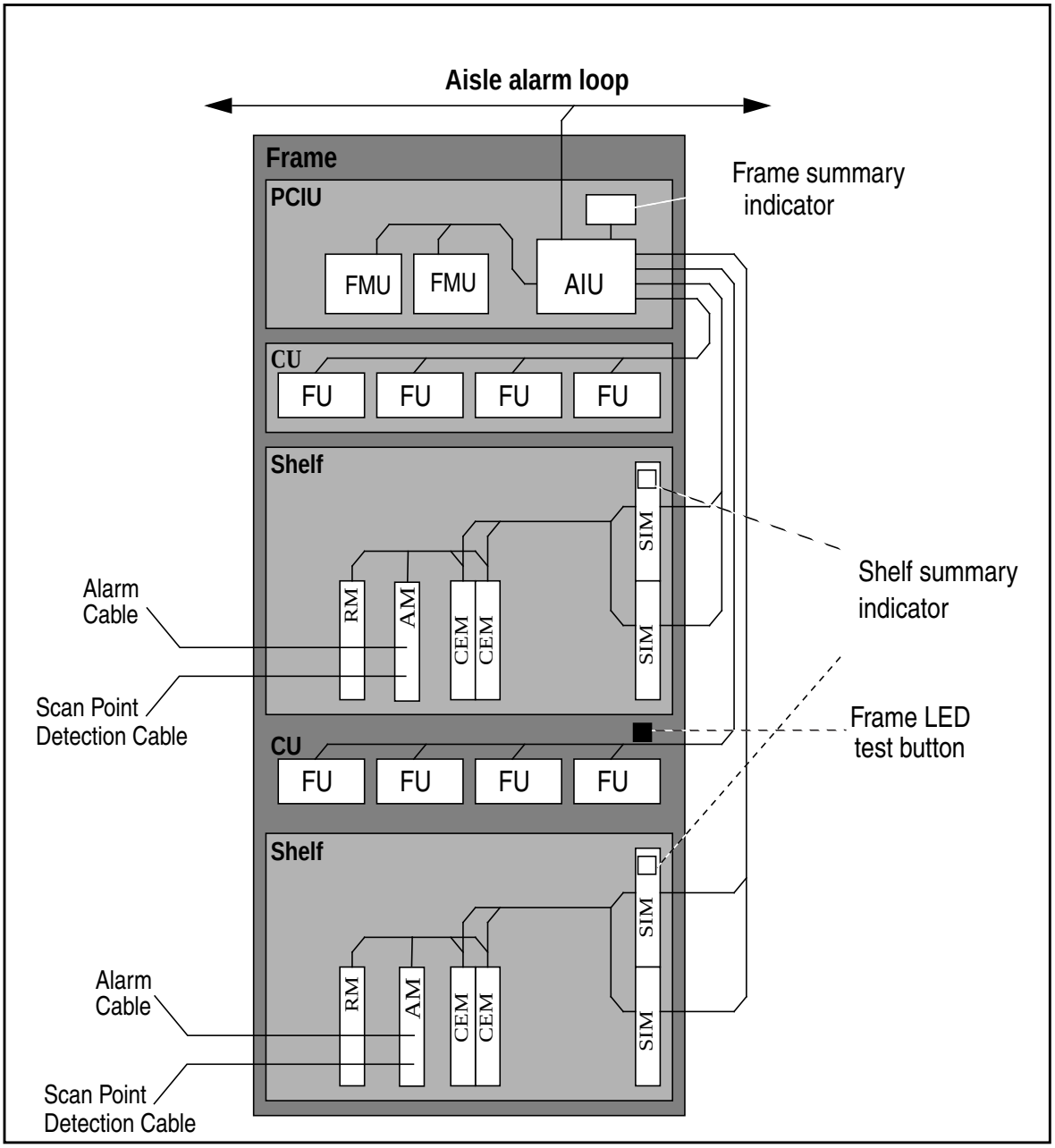
The different levels of visual indicators work together to provide the following capabilities:

- Any MG 4000 based Field Replaceable Unit (FRU) in the office may be flagged for replacement. Its location may be indicated by a change in the state of that FRUs faceplate indicators; this is initiated by either maintenance software control or autonomous hardware control. Software action can flag only shelf-based circuit modules (CEM, RMs and SIM). Other entities depend on hardware autonomous control.
- As FRUs are installed into an MG 4000 shelf, the craftsperson doing the installation is notified that the FRU is healthy (as best as it can determine) and ready to assume its role in the MG 4000 peripheral.
- Personnel can check for failed indicators at any time, to verify the indicators’ operation.
- The indicators’ lives are extended, where necessary, through a feature that automatically deactivates them when they are not required. The indicators are reactivated automatically when they are required again.
- Faults in facilities-interface modules can be differentiated from a lack of signal on the incoming facility.
- Cooling subsystem failures are indicated even with both common equipment modules removed from the shelf.
- Active primary power in the shelf is indicated.
- Available alarm battery supply is indicated.
- Failures of either the primary power supplies or the cooling and alarms subsystems are visible to software running in the common equipment modules.

Frames carrying MG 4000 equipment are compatible with aisle-level signals associated with the DMS alarm system.

## NTLX83AA Multi-Service Gateway 4000 (continued)

**System block diagram**




The Alarm Module extends the MG 4000's alarm indicators by providing generic visual and audible alarm (critical, major, and minor) contact (loop) closure and scan point detection for a stand alone or 3rd party End Office (EO) environment.

## NTLX83AA Multi-Service Gateway 4000 (continued)

## Functional description

The principal functions of the Alarm Module are:

- visual contact (loop) closure for critical, major, and minor MG 4000 alarms.
- audible alarm contact (loop) closure for critical, major, and minor MG 4000 alarms.
- visual indicators for MG 4000 level critical, major, and minor alarms
- scan point detection for up to four customer definable external events.
- 30 second watch dog timer.
- separate audible and visual relays and contacts for extension of system Critical, Major and Minor alarms.
- faceplate visual indicator LEDs for MG 4000 level Critical, Major, and Minor alarms.
- Dead System Alarm (DSA) to raise Critical alarms in the event of a total system outage.
- provisionable in any MG 4000 slot, including 1, 3, or 9 S-Link slots.

### Backward compatibility

The NTLX83AA is a new product designed for the Distributed Access Succession Multi-service Gateway 4000 Platform (MG 4000) and the 3G GSM Base Station Controller, and is therefore not required to be Backward Compatible with an existing module or RM.

The NTLX83AA can be placed in any RM slot that utilizes three or nine S-Links in the existing SPM backplane (NTLX5201). However, if the Alarm Module is used in the existing backplane, the Alarm Module will not be able to drive the frame fail (FRMFAIL) lamp during a Dead System Alarm condition (FRMFAIL can only be driven by the CEMs to the SIMs in the existing backplane).

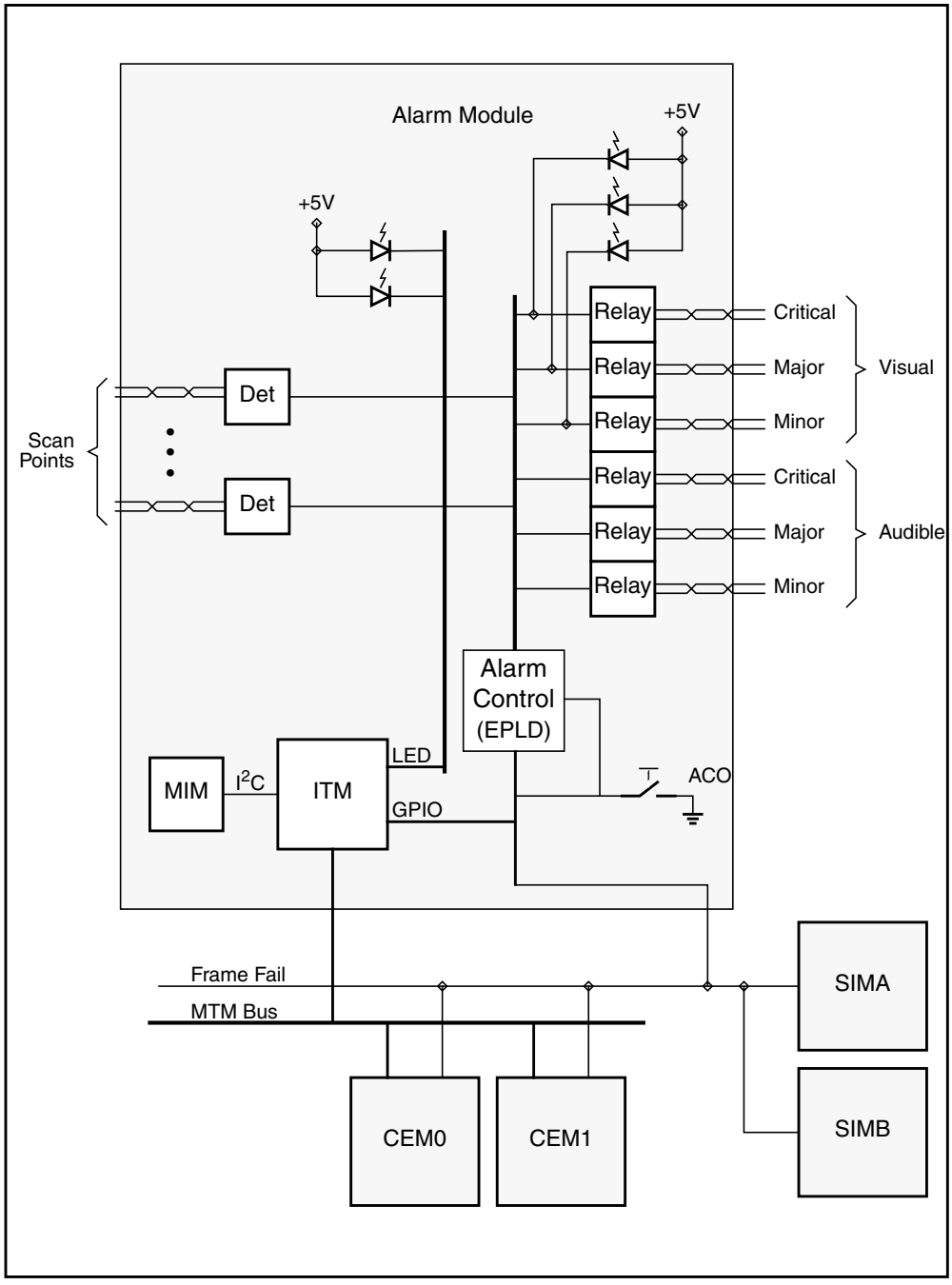
The NTLX83AA can be placed in any RM slot that utilizes one, three, or nine S-Links in the new MG 4000 backplane (NTLX5211).

## Functional block diagram

The next diagram is an illustration of the functional block diagram of the NTLX83AA.

## NTLX83AA Multi-Service Gateway 4000 (continued)

**NTLX83AA functional block diagram**



## NTLX83AA Multi-Service Gateway 4000 (continued)

### Alarm control

A small EPLD (existing component currently used on Spectrum) will be used in order to manage the following functions:

- Appearance of visual/audible alarms
- Alarm Cut-Off (ACO) switch
- Dead System Alarm Timer

### Alarm appearance

Upon reception of a critical, major, or minor alarm from software, the EPLD will drive the contact closure for the office audible and visual alarms, as well as the visual indicators on the faceplate of the Alarm Module. In order to set a particular alarm, software will issue a command (ALM_SET active low) coincident with the applicable level alarm (CRIT_ALM, MAJ_ALM, or MIN_ALM active high).

The EPLD will ensure the visual indicators will be changed from an unacknowledged state (i.e. flashing) to an acknowledged state (i.e. non flashing) when the Alarm Cut-Off is initiated either locally from the faceplate mounted ACO switch, or remotely (ACK_ALM - active low). If the alarmed state is acknowledged locally, software will be notified via an acknowledgment (ACK_STAT - active low). Also, software will have to account for relay debounce - i.e. confirm the status of loop closure at defined intervals in order to allow the relay contacts enough time to settle.

***Note:*** When the state of the card is changed to disabled (MANB, SYSB, OFFL state), the CEM clears all alarm relays on the alarm card and no System alarm events are reported via the alarm relays and visual indicator LEDs on the card.

At any point in time, software will have the ability to query the pack in order to determine the alarm state of the Alarm Module (CRIT_STAT, MAJ_STAT and MIN_STAT).

The Alarm Control EPLD will verify the operation of the audible and visual alarm relays. If the second relay contact does not operate given an alarm condition, the Alarm Module will assume the relay has burned out. As a result, the Alarm Module will report a lack of alarm condition via the alarm status bits (CRIT_STAT, MAJ_STAT, and MIN_STAT). The craftsperson will be notified of a blown relay, thus requiring the replacement of the Alarm Module.

In the event there is a loss of power to the Alarm Module, a system level critical alarm will be raised via constant critical alarm contact closure. Since there will be a lack of power to the Alarm Module, the platform level visual alarm

indicators on the faceplate will not illuminate. In the scenario just described, the craftsperson will have to utilize the EMS in order to determine the severity of all the alarms (in addition to the critical alarm set by the loss of power to the Alarm Module). Although it is possible for the loss of power to be localized to just the Alarm Module, there is a higher probability that loss of power to the Alarm Module indicates loss of power to the entire shelf.

Lastly, visual and audible alarms will be interconnected into the customer's system (wire wrapped at an MDF) via a new cable from the faceplate of the Alarm Module (NT0X96NE - MSP Alarm Cable).

### Alarm cut-off

The Alarm Cut-Off capability has the ability to be initiated either from a local switch provided on the faceplate of the Alarm Module, or remotely by craft-personnel accessing the MTM bus. The Alarm Control EPLD (ACE) will continuously monitor the ACO's current state. The Alarm Cut Off functionality will inhibit any existing audible alarms, including the dead system alarm. However, the Alarm Cut Off capability will not inhibit (mask) subsequent CO audible/visual indications, which indicate additional/new alarms.

### Dead system alarm timer

The purpose of the Dead System Alarm mechanism incorporated on the Alarm Module, is to monitor the sanity of the active CEM and to report a loss of sanity by releasing the critical audible and critical visual alarm relays. The sanity of the CEM is determined by the ability of the CEMs to service a 30 second watchdog timer found within the EPLD.

If the DSA timer is allowed to expire, the CEMs are considered to be insane or severely degraded and the DSA hardware alerts operating company personnel by raising a visual and audible critical alarm, as well as lights the Frame Fail lamp on the MG 4000. The currently active CEM is considered to have regained sanity when it is able to send a timer reset message to the alarm card.

The DSA condition may be a result of multiple faults in hardware (e.g., DSA function on the alarm card, MTM bus) or in overloaded or insane Spectrum system CEMs.

The DSA critical alarm indications are not latched. If the timer has timed out and has operated the alarms, a subsequent watchdog reset by the CEM will result in a clearing of the critical alarms.

DSA time-out events are not reported by the CEM to the EMS nor are they logged.

## NTLX83AA Multi-Service Gateway 4000 (continued)

The Dead System Alarm is an integral component of each Alarm Module and does not require that the card be enabled or disabled by operating company personnel action.

The DSA function cannot be disabled once the 30 second watchdog timer has been enabled. The DSA is disabled on power-up and enabled by the first watchdog timer reset.

### Audible and visual alarm relays

Six separate physical alarm relays are provided on the card for the reporting of Critical, Major and Minor Audible and Visual alarms. The states of the relays are controlled by the CEM and indicate the various possible states of alarm.

Critical, Major and Minor alarmable events result in the corresponding audible and visual relays being SET. When an alarmable event is cleared, either by system or manual action, the audible and visual relays are CLEARED by the CEM.

When an alarmable event is detected or is cleared, both the audible and visual relays are controlled as a pair.

Note that both the audible and visual relays are CLEARED only if:

- all previously reported alarms with the same severity have cleared
- the alarm reporting function has been disabled by command at the EMS

The Critical, Major and Minor Audible alarm relays can be cleared by a craftsperson by pressing the ACO push-button on the faceplate or via an alarm acknowledgment command sent via the EMS. Alarm acknowledgment does not affect the state of the current visual alarm relays nor does it prevent the audible alarm relay from operating as a result of a subsequent alarm.

The audible and visual alarm relays are CLEARED (released) only when all alarms of the given severity have cleared.

The CRITICAL audible and visual relay contacts are normally closed. In other words, when power to the alarm card is lost (e.g. power supply failure or card removed from the shelf) the critical alarm relay contacts will immediately close.

A hardware fault which results in a failure to operate any alarm relay will not impact the operation of the other relays.

## NTLX83AA Multi-Service Gateway 4000 (continued)

### Integral alarm relay test

The Alarm Module ensures that alarm relays are correctly set or released when requested by the active CEM.

When an alarmable event is detected, the CEM sends a message to the alarm card to operate the audible and visual relays and set the Visual Indicator LED to WINK.

Immediately following the setting of a pair of relays, the CEM sends a second message to read their state. If one or both of the relays failed to operate, a new alarm is generated indicating the cause of the failure.

The expected state of the relays is sensed each time an alarmable event is detected whether an alarm is active, inactive or has been previously acknowledged (audible relay cut-off).

### Visual indicator LEDs

In the event of Critical, Major and/or Minor alarms, there are three corresponding Visual Indicator LEDs on the NTLX83AA faceplate.

In the event of unacknowledged alarmable events, an LED on the ACO switch ignites. When the system is free of all alarms, or has acknowledged all alarms, the LED on the ACO switch is extinguished.

### Scan point detectors

Four (4) customer definable scan points reside on the Alarm Module. Each detector senses loop closure on four (4) pair of pins on the 25 pin alarm drive / scan point connector located on the faceplate of the Alarm Module.

Each set of detectors employ the following protective measures:

- in rush current limiting inductors
- a voltage suppressor (limits loop voltage to 60V
- current limiting thermistors and resistors
- an opto-isolator

Each scan point detector can detect a loop closure characterized by a resistance of 500 Ohms or less. *Note: The MSP Alarm Cable is made up of 26 AWG wires which have a resistance of approximately 41 Ohms per 1,000 feet at 20 degrees Celsius.*

Primary protection must be used in any inter-building (leaving the building) application.

## NTLX83AA Multi-Service Gateway 4000 (continued)

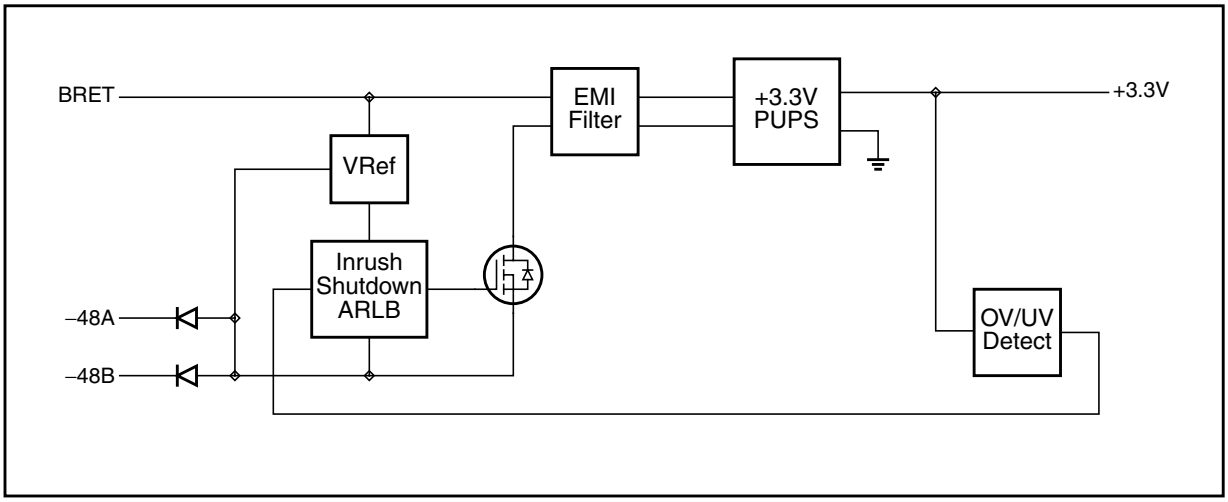
### Power supply

A DC-to-DC point-of-use power supply (PUPS) will be used to convert the –48V A and B feeds to the +3.3V supply rail required for the Alarm Module circuitry. The shelf A and B feeds are individually filtered to reduce EMI/EMC and then diode OR'ed together to supply a fused input to the PUPS, allowing the module to operate with either or both of the shelf supplies.

A fuse in each power feed, before the diode OR circuit, was not chosen because of problems in detecting a blown fuse in a single feed. If only one of the two fuses were to blow, it is possible an RM could be inadvertently shut down during routine maintenance procedures (by powering down one of the two feeds). The diodes used are special for this application, and are designed to fail in an open state and not catch on fire. Also, special provisions are made in circuit board layout to reduce the risk of shorts occurring before the fuse.

In-rush current protection, automatic return from low battery (ARLB), and shutdown circuitry controls a power MOSFET switch for the diode OR'ed -48V battery feed. Battery and return are filtered to reduce electro-magnetic interference (EMI) and then supply the input to the PUPS. Over-voltage and under-voltage conditions on the +3.3V PUPS outputs are monitored for and will cause a shutdown of the power supply circuit if detected. The battery supply must be cycled off and back on in order to reset the shutdown circuit and re-enable the PUPS.

**Power supply**



Included in the Power block is a power monitor function. This circuit monitors the +3.3V voltage rail and asserts a single reset pulse to the Alarm Module if any voltage drops below the following limits:

- 3.0V for the +3.3V supply

The reset pulse duration is 140msec.

In order to drive the pack level and platform level status LEDs, a Linear Technologies Micropower DC/DC converter will supply a +5V voltage rail from the +3.3V supply, with up to 300 mW of power.

### Pin Description

The next table contains the backplane pin descriptions for the alarm module.

**Alarm module backplane pin description**

| Conn. no. | Signal | Function | IO type | Description |
|---|---|---|---|---|
| P1 | -48B | Power | | -48V Battery Feed B |
| P1 | RET | Power | | Battery Return |
| P1 | -48A | Power | | -48V Battery Feed A |
| P2 | FRMFL | Output | | Frame Fail |
| P2 | MMD | Input | 3.3V CMOS ITM | JTAG 1149.5 Bus Master Data |
| P2 | MSD | Input/Output Open Drain | 3.3V CMOS ITM | JTAG 1149.5 Bus Slave Data |
| P2 | MCLK | Input | 3.3V CMOS ITM | JTAG 1149.5 Bus Clock |
| P2 | MPR | Input/Output Open Drain | 3.3V CMOS ITM | JTAG 1149.5 Bus Request |
| P2 | MCTL | Input | 3.3V CMOS ITM | JTAG 1149.5 Bus Control |
| P2 | LGND | Power | | logic ground of the PCP/BACKPLANE |

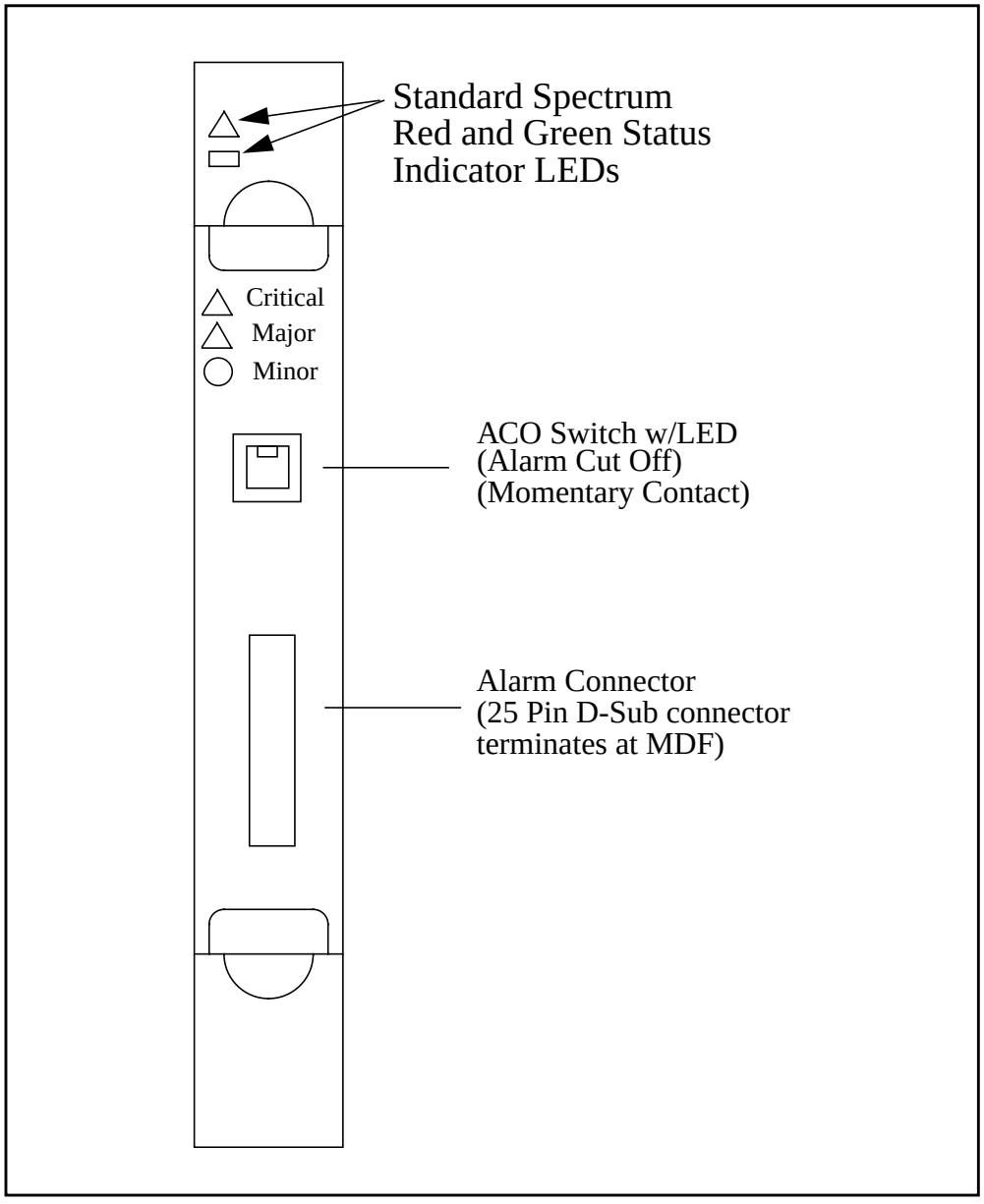
## NTLX83AA Multi-Service Gateway 4000 (continued)

# Interface specifications

### Visual indicators

The Alarm Module will carry two sets of visual indicators to provide information of interest to craft personnel. In addition to the standard Spectrum pack status indicator LEDs (located on the lock latch), the alarm module will have platform level critical, major and minor alarm LEDs located on the faceplate of the Alarm Module (see the next figure).

**Faceplate**



### Module status LEDs

The module status LEDs, which are located at the lock latch, indicate the current state of the module as shown in the next table.

**Visual indicators - module status**

| Green | Red | Module state |
|---|---|---|
| Off | Off | Sleep, un-powered or not inserted |
| On | On | Power up LED test |
| Wink | Off | Power up self-test underway |
| On | Off | Module should not be removed |
| Off | On | Alarm state: module may be removed |

Power up LED test is entered immediately after the module is first powered up or inserted. Its purpose is to allow personnel to verify the LEDs are functional. The LEDs remain in this state for the duration of the power-up self-test.

Alarm State is entered during a power up or insertion sequence if the self-test fails, or if the Common Equipment Module rejects the module as being unworkable in the system due to incompatibilities or a failure to establish communications with the module.

The Green ON, Red OFF state is entered during power up or insertion sequence when the module has passed its diagnostic test. In this case, the module should not be removed.

## NTLX83AA Multi-Service Gateway 4000 (continued)

### MG 4000 platform status LEDs

The next table contains visual indicators for the MG 4000.

**Visual indicators - MG 4000 status**

| Red | Red | Amber | MG 4000 status |
|---|---|---|---|
| Off | Off | Off | No alarms present in the system |
| Off | Off | On | Minor alarm is present |
| Off | On | Off | Major alarm is present |
| Off | On | On | Major and minor alarms are present |
| On | Off | Off | Critical alarm is present |
| On | Off | On | Critical and minor alarms are present |
| On | On | Off | Critical and major alarms are present |
| On | On | On | Critical, major and minor alarms are present |

All Visual Indicator LEDs will change state as indicated in the next table.

| Initial | New | Meaning |
|---|---|---|
| Off | Wink | New alarm generated |
| Wink | On | Alarms(s) acknowledged localy through the ACO or remotely through the EMS. |
| Wink | Off | All alarms cleared |
| On | Off | All alarms cleared |
| On | Wink | New alarm generated with existing alarm(s) previously acknowledged. |
| Visual indicator LEDs cannot be tested locally | | |

### Alarm acknowledgement status LED

In the event there is one or more unacknowledged alarms found in the system, the LED located on the ACO switch is ignited. If the system is either clear of

alarms, or if all of the existing alarms have been acknowledged, the LED is extinguished.

| ACO LED | Meaning |
|---|---|
| On | One or more unacknowledged alarms exist within the sysem |
| Off | All alarms are acknowledged, or there are no existing alarms found within the system. |

### Sleep mode

When not required, the Alarm Module status LEDs (located on the lock latch) may enter a customer programmable “sleep” mode to extend their life. The LEDs will leave the sleep mode:

- when so directed by OAM S/W
- as a result of LED state change
- as part of an Indicator Test

The LEDs will not sleep while a pack level alarm source is active (i.e. while there is a module in the peripheral in the RED ON, GREEN OFF state.)

## Performance requirements

### Electrical specifications

The next table contains the input characteristics for all input pins on the backplane.

**Input characteristics**

| Parameter | Pin | Min. | Nom. | Max. | Units | Comments |
|---|---|---|---|---|---|---|
| $C_I$ | | 3.5 | | 8 | pF | |
| $Z_I$ | | | | | MΩ | |
| $V_{IL}$ | | –0.5 | | 0.8 | Volts | |
| $V_{IH}$ | | 2.0 | | $V_{CC}$+0.5 | Volts | |
| $V_{IK}$ | | | –0.7 | –1.2 | Volts | Clamp diode |
| $I_{IL}$ | | | | 1 | µA | |
| $I_{IH}$ | | | | 1 | µA | |

## NTLX83AA Multi-Service Gateway 4000 (end)

The next table contains the output characteristics for all output or bidirectional pins on the backplane.

**Output characteristics**

| Parameter | Pin | Min. | Nom. | Max. | Units | Comments |
|---|---|---|---|---|---|---|
| $C_O$ | | 3.5 | | 10 | pF | |
| $V_{OL}$ | | $V_{CC}$-0.2 | | 0.2 | Volts | $I_{OL}$=0.1mA |
| | | 2.4 | | 0.4 | | $I_{OL}$=24mA |
| $V_{OH}$ | | | | | Volts | $I_{OH}$=-0.1mA |
| | | | | | | $I_{OH}$=-24mA |
| $I_{OL}$ | | 6 | | 36 | mA | |
| $I_{OH}$ | | -6 | | -36 | mA | |
| $I_{OZ}$ | | | | | mA | |

### Power requirements

The Alarm Module will utilize a Point-of-Use Power Supply (PUPS) to convert –48V to 3.3V as required. Two independent –48V sources will be provided for redundancy. These will be diode-ORed within the Alarm Module before being fed to the PUPS.

# NTLX89DA Interface Electronics Module

## Product description

### Overview

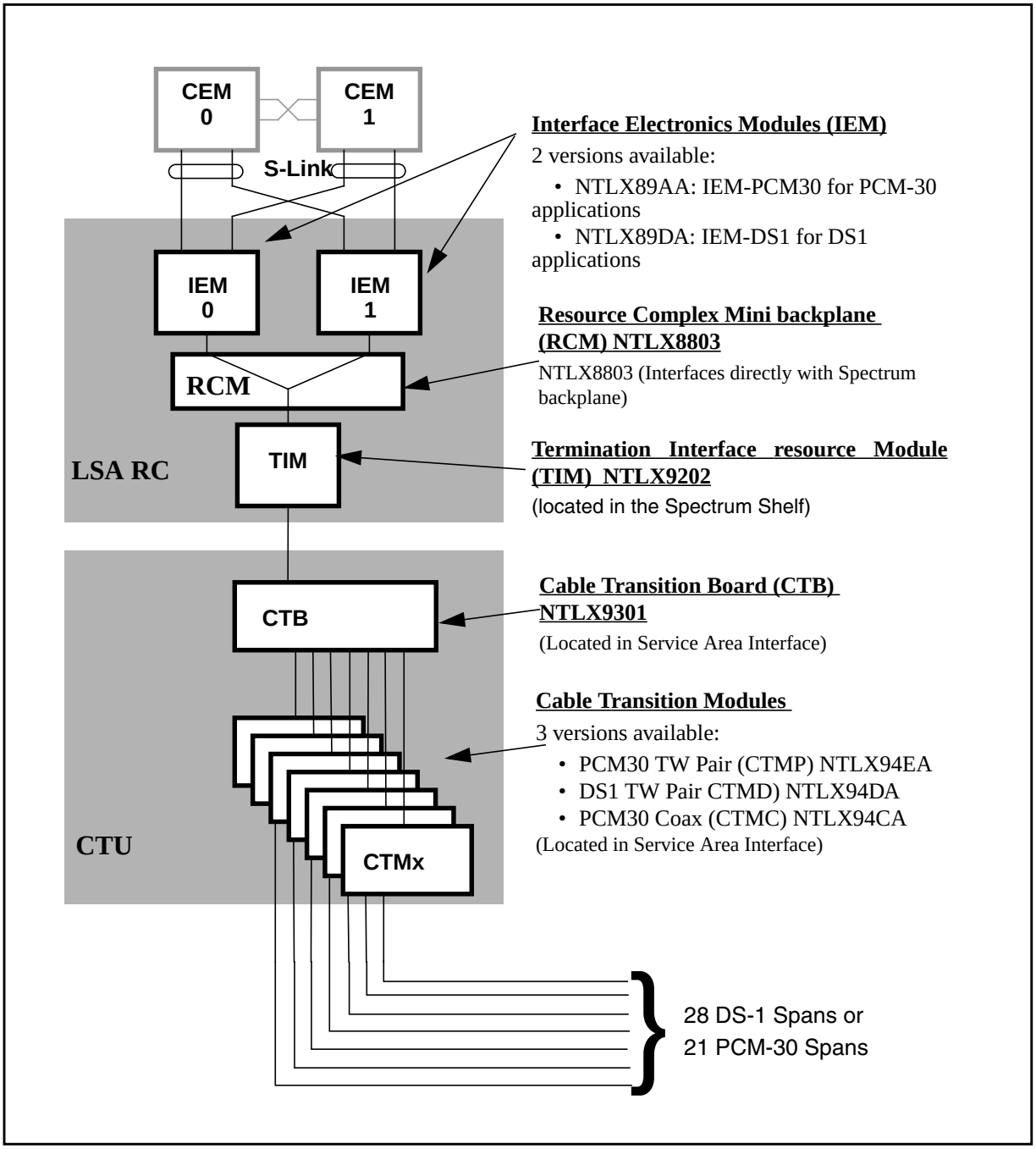
The Interface Electronics Module DS1 (IEMD) Resource Module (RM) provides Layer 1 termination for multiple DS1 trunks for the Spectrum Peripheral Module (SPM) platform. It is a hardware and software interface upon which existing and future T1 interfaces can be implemented, such as GSM applications (3G BSC/TCU) and Succession Networks applications (MG4000).

The NTLX89DA IEMD is an integral part of Low Speed Access (LSA) for the Spectrum platform. Low Speed Access (for MG4000 or 3G BSC/TCU) is achieved via the Low Speed Access Resource Complex (LSA RC) and the Cable Transition Unit (CTU).

The next figure is an illustration of the electrical architecture of the LSA RC.

## NTLX89DA Interface Electronics Module (continued)

**Block diagram of LSA electrical architecture**



## NTLX89DA Interface Electronics Module (continued)

### DS-1 LSA RC

The nomenclature “Resource Complex” was derived to define a multi-slot product in the Spectrum platform. Instead of one Resource Module (RM), the LSA RC consists of:

- two NTLX89AA IEMD RMs
- one NTLX92AA Termination Interface Module (TIM)

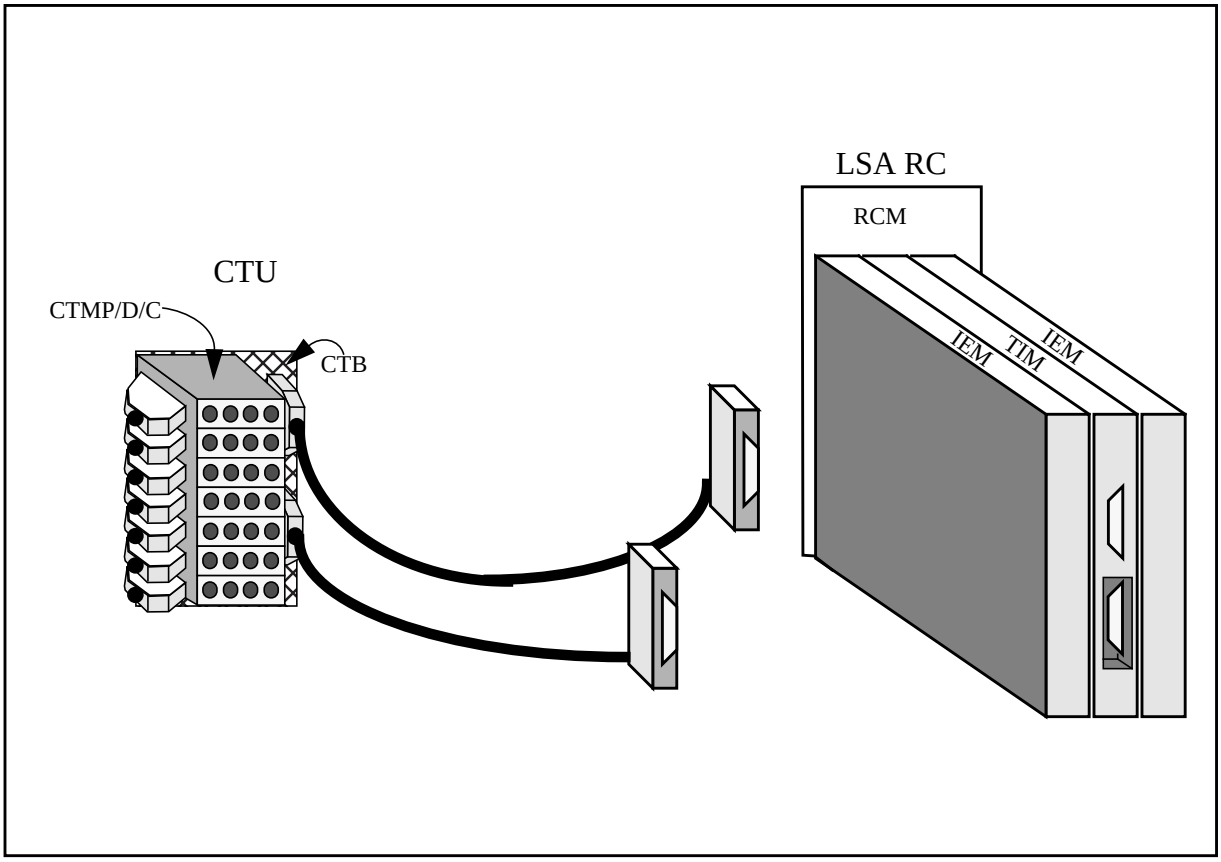
These 3 RMs are connected by the Resource Complex Mini-backplane (RCM), which inserts into the Spectrum backplane.

The IEMD RM provides the termination for 28 DS-1 span connections. This number of spans allows full utilization of the S-Link bandwidth available at an RM interface on the Spectrum backplane. The TIM provides the physical wiring management for the 28 DS1 interfaces and provides the mechanism for insertion/extraction of the TIM and RCM combined PEC. The RCM backplane capabilities are twofold; 1) provide an interconnect between both IEMs and TIM and 2) provide an interconnect between the LSA RC and the Spectrum backplane. The interconnect between the IEMs contains QUICC messaging and presence (working and spare) signals, whereas the interconnect between the LSA RC and the Spectrum backplane contains access to the S-LINK interfaces, test bus, and -48v power rails.

The cutaway view of SAI cabinet and spectrum shelf illustration shows the physical architecture of the LSA. The TIM and the two IEMs are removable resource modules that are located in the Spectrum shelf. The CTU, which provides connectors for wiring to the customer’s network, is located in the Service Area Interface (SAI). A high density cable connects the TIM to the CTU. Refer to the next illustration to see how the LSA RC connects to the CTU.

## NTLX89DA Interface Electronics Module (continued)

**LSA RC and CTU interconnection**




Notwithstanding, the CTU provides cable management of 28 DS1s from the DSX to the LSA RC. The CTU also provides individual DS1 loopback capability, secondary protection, and if needed, impedance matching. Components of the CTU are:

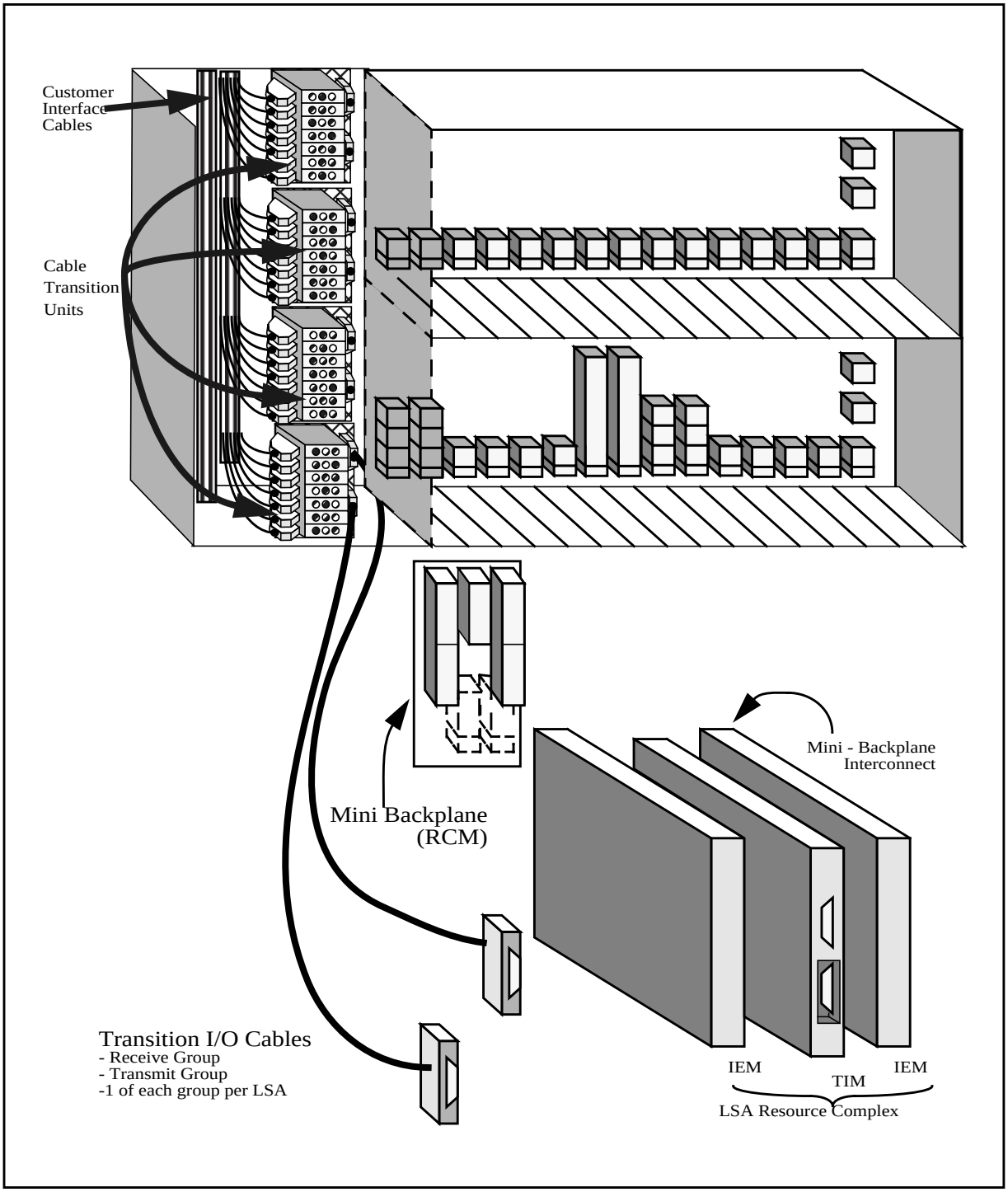
- one Cable Transition Board (CTB) backplane
- up to seven Cable Transition Modules DS1 (CTMD)

This CTU is housed in the Service Area Interface (SAI), which is an outrigger cabinet installed beside the Spectrum frame. This cabinet houses up to eight CTUs.

The next illustration shows the physical architecture of the LSA RC in a Spectrum shelf and CTUs in the SAI.

## NTLX89DA Interface Electronics Module (continued)

**Cut-away view of SAI cabinet & spectrum shelf**

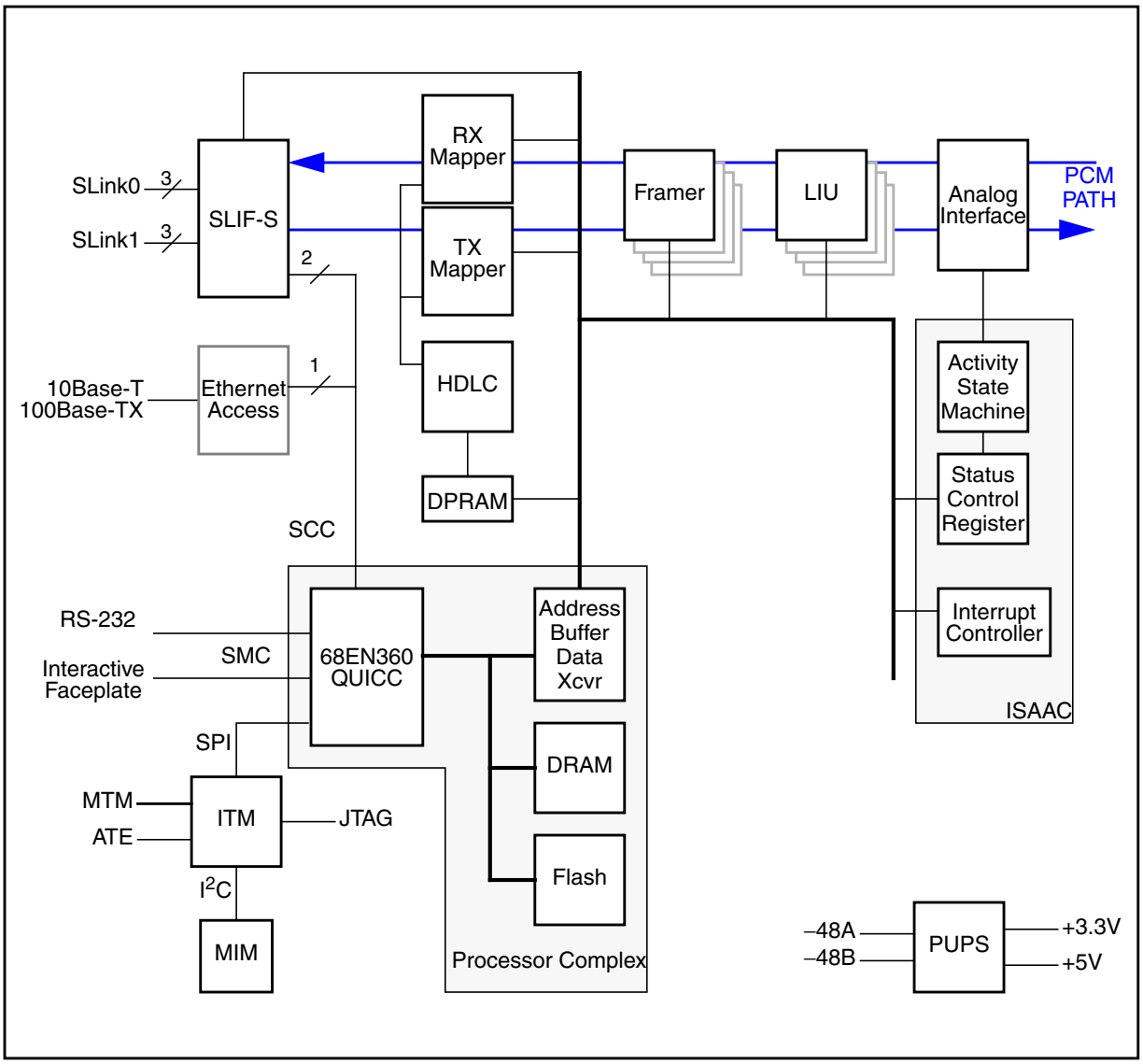


## NTLX89DA Interface Electronics Module (continued)

# Functional block diagram

A functional block diagram of the IEMD Resource Module is shown in the next illustration.

**IEMD functional block diagram**




## Functional block descriptions

### Processor complex

The local processor on the IEMD is a Motorola 68EN360 QUICC (QUad Integrated Communications Controller). This processor controls the terminating circuitry (peripheral devices) and TX/RX Mappers to provide an

interface between external DS1 links and internal proprietary Serial interface Links (S-Links). The QUICC provides the following functions:

- Two serial communication controller (SCC) buses which transport data to/from the SLIF-S DMSW messaging block. The QUICC provides FIFO buffering of the messages, descriptor based data structures, and DMA transfer of message data to/from main memory.
- A serial peripheral interface (SPI) bus for ITM access.
- A UART interface used for initial hardware and software debug
- Chip Selects and write enables for Motorola bus peripherals (Flash, DRAM, SLIF-S, DPRAM, TX/RX Mappers, Framers, LIUs).

The QUICC includes four built in Serial Communication Controllers (SCCs), two built in Serial Messaging Controllers (SMCs), DRAM interfaces, timers, and Direct Memory Access controllers. The SCCs are used for communication to the Spectrum CEMs, Ethernet and inter-IEM communication. The SMCs are used for debug purposes, such as an RS232 interface and interactive faceplate control.

External to the QUICC are 8 Mbytes of Flash EEPROM for software and boot load storage as well as 16 Mbytes of Dynamic RAM.

In addition, the address and data of the QUICC are distributed to the rest of the devices on the IEMD via address buffers and data transceivers to handle fanout of the devices on the board. These devices include the TX and RX Mapper FPGAs, Framers, LIUs, the ISAAC EPLD, and DPR (Dual Port RAM) for HDLC functionality.

### ISACC EPLD

The Interrupt, Status, Addressing and Control (ISAAC) EPLD is an Altera MAX7256AE EPLD device that provides the following functions:

- Chip decoding
- Status and control registers
- Interrupt controller (interrupt status and interrupt control registers)
- Activity state machine

Additional chip decoding on the IEMD is provided by the ISAAC.

### Mappers

The interface between external DS0s and internal SLIFS channels is accomplished via the Transmit (TX) and Receive (RX) Mappers. These Mappers provide the channel assignment for 672 DS0s plus 32 channels of

## NTLX89DA Interface Electronics Module (continued)

HDLC, placing them into the 768 channel S-Link format. The Mappers also provide T1 Robbed Bit Signaling.

The mappers will also be responsible for creating the clock and synchronization signals needed by the framers and the HDLC controller. Robbed Bit Signalling (RBS) bits will be passed between the framers and a separate signaling resource module over specific S-Link channels. There will also be a capability to provide a loopback of all the channels received from the framers and HDLC controller back to their respective transmit data inputs.

### HDLC controller and dual port RAM

The IEMD provides termination of up to 32 channels of HDLC via the Multichannel Network Interface Controller for HDLC (MUNICH32) by Siemens and the 32K x 16 Dual Port RAM (DPR) by IDT. The MUNICH32 provides the following features:

- Serial interface
- Dynamic Programmable Channel Allocation
- HDLC protocol (formatting and deformatting)
- Motorola processor interface (compatible with QUICC 68EN360)
- JTAG boundary scan test

Data is passed between the QUICC 68EN360 and the MUNICH32 via the Dual Port RAM (DPR). Incoming HDLC channels are passed through the IEMD to the CEM, where they are grouped into Bandwidth Allocator Groups (1 BAG consists of 32 channels). This HDLC BAG is passed back down to the IEMD, where the MUNICH32 deformats the HDLC messages and stores them in the DPR. The MUNICH32 notifies the QUICC that there is an HDLC message waiting in the DPR. The QUICC retrieves the HDLC message from DPR, wraps the message in a DMSW wrapper and sends it back up to the CEM.

This functionality was designed for the GSM application and is currently not being used in the MG4000 application for initial release.

### Analog interface

External DS0s pass through analog circuitry before terminating at the Line Interface Unit (LIU). The analog circuitry consists of relays, transformers and protection diodes.

The relays on the IEMD provide sparing between the active and spare IEMDs. When the relays are closed, the incoming and outgoing DS0s pass through the relays on the active IEMD.

## NTLX89DA Interface Electronics Module (continued)

When the relays are open, the PCM path is disconnected. This allows the spare IEMD to be removed and replaced without interrupting the performance of the working IEMD. Furthermore, it also provides a higher level of protection from high voltage transients on the spans. The relays, of double-pole type, are orientated in such a way that when the IEM port is isolated from the span, its transmit output will be looped back to its receive input. This will provide a local loopback that will test all of the active circuitry of the PCM path.

Between the relays and the LIUs will be a network which provides DC isolation, impedance matching, and over-voltage protection.

### Line interface unit

Behind the analog section lies four LXT384 “Warbird” Octal T1/E1 Transceivers by Level One. Each LXT384 LIU contains 8 separate PCM transceivers in a BGA-160 package. The IEMD provides 4 LIUs, having a capacity of terminating 28 DS1s, or 672 DS0s. The LIUs provide the following functions:

- low impedance transmit drivers
- shaped waveforms that meet G.703 and T1.102 specifications
- T1 clock (1.544Mbps) extraction
- high noise interference margin
- jitter attenuation
- driver failure monitoring
- B8ZS encoding and decoding
- analog, digital, and remote loopback capability
- Boundary Scan capability (IEEE 1149.1)

On the receive side, the LIU performs the following: 1) it converts the bipolar (also known as AMI - Alternate Mark Inversion) ternary level signal, received from the DSX, to a unipolar binary level signal, 2) it recovers the DS-1 clock from the received data or PCM, 3) provides jitter tolerance and jitter attenuation to the received data and recovered clock. The recovered clock from the incoming PCM will be used to clock the received data or PCM from the output of the LIU to the framer.

On the transmit side, the LIU converts the unipolar PCM signals or data from the framer to bipolar signal or data and drives appropriately shaped bipolar pulses to the digital cross-connect. The LIU transmitter will also monitor the span line for short circuits. Finally, the LIU will provide compensation to maintain the proper pulse shape based on the cable length of cable from CTU to DSX.

## NTLX89DA Interface Electronics Module (continued)

On the processor side, each LIU can be controlled via an 8 bit interface that controls normal operation or any one of the 3 loopback configurations.

### Framer

The IEMD is equipped with four T1FX8 Framers by Transwitch. The T1FX8 is an 8 channel DS1 framer (1.544 Mbps) which provide the following features:

- Line coding and decoding (AMI or B8ZS)
- Framing (D4, SF or ESF)
- TX and RX slip buffers for each channel
- supports robbed bit signalling
- Alarm detection and transmission (AIS, Remote Alarm, and Remote Multiframe Alarm)
- Performance monitoring (CRC errors, Loss of Frame, Frame Errors, Frame slips, BPV/code errors, Loss of Signal)
- Boundary Scan capability (IEEE 1149.1)

TheT1FX8 frames the incoming PCM stream from the LIU and transmits the data to the RX Mapper. Conversely, the TX Mapper will send data to the framer to be transmitted out to the LIUs.

### SLIF-S, S-link interface

A slave S-Link interface ASIC (SLIF-S), common to all RM types, is responsible for the physical interface. It performs the following:

- recovers data from the S-Links from both CEM modules
- monitors link health by way of a CRC check
- extracts DMSW messaging channels from both CEM modules
- selects PCM data from the CEMs, based on CEM activity; a small elastic store function is supplied to accommodate phase variations between the CEMs
- formats the selected data stream into a parallel bus for access by the resources supplied by the RM
- broadcasts outgoing PCM data to both CEMs
- inserts outgoing DMSW messaging timeslots to each CEM
- inserts link CRC
- provides facilities for low level link as well as RM control and status facilities, including test and ID storage

## NTLX89DA Interface Electronics Module (continued)

The IEMD communicates with the CEM via a messaging channel in the high speed serial link (SLINK) on the Spectrum backplane. The RM interface to the SLINK is accomplished via the SLIF-S (Serial Link InterFace - Slave) ASIC developed for the Spectrum platform. The SLIF-S combines the PCM payload channels with the channels received from the MC68360. The SLINK interface also provides clocks to synchronize the high speed serial data.

The SLIF-S has three interfaces to the RM; two SCC ports, one parallel processor interface, and one parallel payload interface. DMSW messaging data is carried over a pair of serial communication control (SCC) buses, one for each of the CEMs. These SCC busses are terminated by the QUICC chip which in turn transfers the DMSW message to/from the host processor. The host processor may access internal registers in the SLIF-S via a parallel Motorola 68030 style bus port on the SLIF-S. HDLC payload channels for the active CEM only are sent and received on a parallel time-division multiplexed payload bus. The parallel payload bus is converted to a serial format and connected to the HDLC controllers by the Payload Router circuit.

### ITM, test bus master

The IEMD communicates on the Spectrum Maintenance Bus via the ITM (Integrated Test Master) ASIC, also developed for the Spectrum platform. The ITM ASIC interfaces the system Module Test and Maintenance (MTM) bus to the resource module, providing access to the internal JTAG bus, processor communication, circuit card reset control, module information memory (MIM) access, and circuit card LED control. The MTM bus is an IEEE 1149.5 standard bus, which is a 5 wire multi-drop bus used to facilitate communication of test and maintenance commands, and serial data between a system test/maintenance control module and up to 250 slave modules. The DLC operates as an MTM bus slave. Communication with the ITM may be initiated by the DLC host processor via the SPI bus which is one of the peripheral functions provided by the QUICC.

### Power supply

Two DC-to-DC point-of-use power supplies (PUPS) will be used to convert the –48V A and B feeds to the +3.3V and +5V supply rails required for the IEMD RM circuitry.

The shelf A and B feeds are diode OR'ed together to supply a fused input to the power circuit, allowing the resource module to operate with either or both of the shelf supplies. A fuse in each power feed, before the diode OR circuit, was not chosen because of problems in detecting a blown fuse in a single feed. If only one of the two fuses were to blow, it is possible an RM could be inadvertently shut down during routine maintenance procedures (by powering down one of the two feeds). The diodes used are special for this application, and are designed to fail in an open state and not catch on fire. Also, special

## NTLX89DA Interface Electronics Module (continued)

provisions are made in circuit board layout to reduce the risk of shorts occurring before the fuse.

In-rush current protection, automatic return from low battery (ARLB), and shutdown circuitry controls a power MOSFET switch for the diode ORed –48V battery feed. Battery and return are filtered to reduce electro-magnetic interference (EMI) and then supply the input to the PUPS. Overvoltage and undervoltage conditions on both +5V and +3.3V PUPS outputs are monitored for and will cause a shutdown of the power supply circuit if detected. The battery supply must be cycled off and back on in order to reset the shutdown circuit and re-enable the PUPS.

Included in the Power block is a power monitor function. This circuit monitors the +5V and +3.3V voltages and asserts a single reset pulse to the IEMD RM if any voltage drops below the following limits:

- 3.0V for the +3.3V supply
- 4.75V for the +5V supply

The reset pulse duration is 140msec.

## Human machine interfaces

### Locklatch indicators

The locklatch indicators will follow the Spectrum standard. There will be three indicators on the locklatch. Amber indicates span interface status. Green and red indicate IEM status.

***Note:*** Note the TIM LEDs, echo the status on the IEM.

### Amber “external input” status LED

The circular amber “External Input” status LED is required on the IEM since it is an interface module.

**External status LED**

| Amber | External input status |
|---|---|
| Off | All external inputs entering the module through the faceplate appear to be carrying a valid signal. |
| On | At least one of the external inputs entering the module through the faceplate does not appear to be carrying a valid signal. |

The LED is lit when the module detects loss of signal on one of the external PCM30/DS1 spans. The intention of this indicator is to allow operating

company personnel to quickly decide whether a fault lies in the Spectrum peripheral itself, or at the signal source (or connections between).

### Red and green IEM module state LEDs

The triangular “red” and rectangular “green” module state LEDs will convey the information summarized in the next table.

**Module state LEDs**

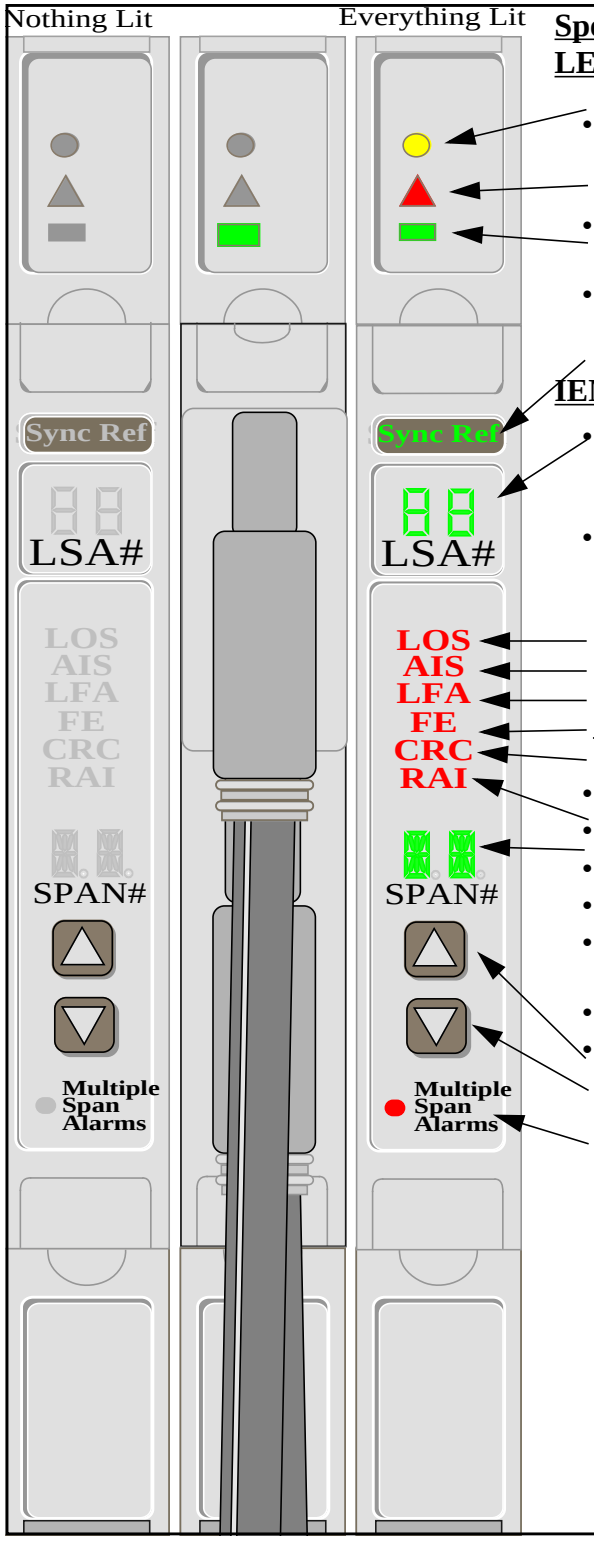
| Green | Red | Module state |
|---|---|---|
| Off | Off | Sleep, unpowered or not inserted |
| On | On | Powerup LED test |
| Wink | Off | Powerup self-test underway |
| On | Off | Module should not be removed |
| Off | On | Alarm State: Module may be removed |

### Faceplate information

The next figure is a drawing of the IEM and TIM faceplate interfaces. This figure uses color for indicators as color will be used in the product for indicators. If printed in black and white, the functionality will still be discernible. This figure is an example of the LSA RC faceplates. The two IEM faceplates are for demonstration purposes only. They demonstrate how a blank IEM faceplate will appear and what are the features that can be indicated by LEDS.

## NTLX89DA Interface Electronics Module (continued)

### LSA RC faceplates




**Spectrum Resource Module LOCKLATCH LEDS:**

- Yellow indicates a problem with at least ONE of the external interfaces into the Resource Module.
- Red indicates a problem with the Resource Module
- Green indicates that this Resource Module is operating and should not be removed.

**IEM Faceplate User Interface Indicators**

- Green Sync Ref indicates the one IEM that is serving as the sync reference for the Spectrum product.
- Green LSA # alpha-numeric display indicates LSA number. This number is the LSA number as defined by software. This is to assist the association between the CTU in the SAI and the LSA in the Spectrum Shelf.

**The following indicates a fault condition on the span in the 'SPAN #' display:**

- Red LOS indicates Loss Of Signal frame.
- Red AIS indicates Alarm Indication Signal.
- Red LFA indicates a Loss of Frame Alignment.
- Red FE indicates Frame Error rate is too high.
- Red CRC indicates the number of Cyclic Redundancy Check errors is too high.
- Red RAI indicates Remote Alarm Indication.
- **Working IEM:** Green SPAN # is used to display either 'OK' if there are no problems on any spans, a span number with its associated problems, or '--' showing not enough information to determine problem on all spans. ( The '--' will occur when there is a problem with the copper connection between the IEM and the CTB.)

# Performance requirements

## DS-1 electrical specifications

All components have been selected such that they will meet or exceed the industry standard requirements. DS-1 will support cable lengths of up to 655 feet (200 meter). All pulse measurements will be made at the DSX.

**Transmitter electrical specifications**

| Parameter | Specification | Reference |
|---|---|---|
| Nominal Line rate | 1.544 Mbits/sec | ANSI T1.102, SEC. 6.1<br>TR-TSY 499 SEC. 9.3<br>CCITT G.703 SEC 2. |
| Line Rate Accuracy | In free-running mode, the line-rate accuracy shall be +/- 50 bits/sec (+/- 32 ppm). In a synchronized mode, the line rate accuracy shall be that of the network clock. | ANSI T1.102, SEC. 6.1<br>TR-TSY 499 SEC. 9.3<br>CCITT G.703 SEC 2. |
| Line Code | AMI with no more than 15 consecutive zeros, and at least N ones in each and every window of 8(N+1) or B8ZS. | ANSI T1.102, SEC. 6.1<br>TR-TSY 499 SEC. 9.3 |
| Test Load | A resistive load of 100 ohms (+/- 5%) shall be used at the interface for the evaluation of pulse shape and electrical parameters | ANSI T1.102, SEC. 6.1<br>TR-TSY 499 SEC. 9.3 |
| Pulse Amplitude | The amplitude of an isolated pulse (mark) shall be between 2.4 v and 3.6 v. The peak undershoot shall not exceed 40% of the peak pulse. | ANSI T1.102, SEC. 6.1<br>TR-TSY 499 SEC. 9.3<br>CCITT G.703 SEC 2. |
| | The amplitude of a zero (space) within a timeslot shall be no greater than either the value produced in that timeslot by other pulses (marks) within the mask of FIG. 10/G.703 or +/- 0.1 of the peak pulse amplitude, whichever is greater. | CCITT G.703 SEC 2. |

## NTLX89DA Interface Electronics Module (continued)

**Transmitter electrical specifications**

| Parameter | Specification | Reference |
|---|---|---|
| Pulse Shape | The shape of every pulse that approximates a normalized isolated pulse preceded by four zeros and followed by one or more zeros shall conform to the masks shown in Figure 24, Figure 25 and Table 4. | ANSI T1.102, SEC. 6.1<br>TR-TSY 499 SEC. 9.3 |
| Pulse imbalance | In any window of seventeen consecutive bits, the maximum variation in pulse amplitude shall be less than 200 mV, and the maximum variation in pulse widths (half amplitude) shall be less than 20 ns | ANSI T1.102, SEC. 6.1<br>TR-TSY 499 SEC. 9.3 |
| Power Level | For all ones signal, the power in a 3KHz +/- 1KHz band centered at 772 KHz shall be between 12.6 dBm and 17.9 dBm. | ANSI T1.102, SEC. 6.1<br>TR-TSY 499 SEC. 9.3 |
| | For all ones signal, the power in a 3KHz +/- 1KHz band centered at 1544 KHz shall be at least 29 dB below that at 772 kHz | ANSI T1.102, SEC. 6.1<br>TR-TSY 499 SEC. 9.3 |
| D.C. Power | There shall be no DC power applied to the interface. | ANSI T1.102, SEC. 6.1<br>TR-TSY 499 SEC. 9.3 |
| Output Jitter | (10 Hz - 8 KHz) ----------> 0.020 $UI_{pk-pk}$<br>(8 KHz - 40 KHz) ---------> 0.025 UI<br>(10 Hz - 40 KHz) ---------> 0.025 UI | TR 62411, SEC 4.7 |

## NTLX89DA Interface Electronics Module (end)

**ANSI T1. 102 93 DS1 interface isolated pulse corner points**

| Minimum curve | | Maximum curve | |
|---|---|---|---|
| **Time (U.1.)** | **Normalized amplitude** | **Time (U.1.)** | **Normalized Amplitude** |
| -0.77 | -0.05 | -0.77 | 0.05 |
| -0.23 | -0.05 | -0.39 | 0.05 |
| -0.23 | 0.50 | -0.27 | 0.80 |
| -0.15 | 0.95 | -0.27 | 1.15 |
| 0.00 | 0.95 | -0.12 | 1.15 |
| 0.15 | 0.90 | 0.00 | 1.05 |
| 0.23 | 0.50 | 0.27 | 1.05 |
| 0.23 | -0.45 | 0.35 | -0.07 |
| 0.46 | -0.45 | 0.93 | 0.05 |
| 0.66 | -0.20 | 1.16 | 0.05 |
| 0.93 | -0.05 | | |
| 1.16 | -0.05 | | |

# NTLX99BA STM-1 Resource Module

## Product description

### Overview

The NTLX99BA STM-1 Resource Module (STM-1 RM) is an SDH STM-1 carrier interface module for the Spectrum Peripheral Module (SPM). It allows the SPM to terminate SDH STM-1 transmission systems carrying asynchronous E1 payloads, and it also maps the DS0s in those payloads to the internal format of the SPM. The STM-1 RM terminates sixty three (63) floating asynchronous E1s within the STM-1 carrier, providing the capability of handling 1953 DS-0 payload channels. With two STM-1 RMs per SPM, the STM-1 interface can be protected with SDH 1+1 automatic protection switching (APS) with the far end terminal as required.

### Features

The following is a list of features provided by the STM-1 resource module.

- Single bidirectional STM-1 Line Interface (2 Resource Modules are required for Protected Link operation).
- Hardware support for 1+1 Protection Switching.
- STM-1 optical interface compliant with G.703.
- On-board Local Processing Complex Performs
  - — Low Level Maintenance Functions
  - — Performance Monitoring data collection
- Terminates up to 1953 DS0s mapped to up to 63 asynchronous (PDH) E1s.
- Channel Associated Signaling supported by hardware on a per E1 basis.
- Jitter performance as per G.825.
- Synchronization of incoming payloads to the DMS clock.
- Translation of link payload to and from the internal SPM S-Link protocol.
- On-board diagnostics, self-test and JTAG capability.
- Timing recovery from incoming STM-1 for distribution to SPM Common Equipment Module (CEM).
- QUICC-base RM compliant.

### Principle functions

The following is a list of functions provided by the STM-1 resource module.

- STM-1 optical interface, including data and clock recover.
- SDH STM-1 interface termination including frame generation, alarm detection and generation, and error detection hardware.

- Termination of Asynchronous E1 payloads.
- Overhead support at all multiplexing levels.
- STM-1 and E1 transmit clock generation.
- SDH alarm support.
- Mapping of DS0s and overhead to nine SPM S-Link interfaces to each SPM Common Equipment Module (CEM).
- Interfaces to two SPM Common Equipment Modules (active and inactive) via 9 SPM Serial Links to each CEM. Messaging and payload data is passed over one link and the remainder are used for payload data.

### SDH multiplexing and mapping

The STM-1 RM supports a sub-set of the complete SDH multiplexing structure defined in ITU-T G.707.

### Backward compatibility

Since the STM-1 RM is a new design for SPM, backward compatibility is not applicable.

## Block diagram and functional description

The STM-1 RM is composed of the following functional blocks.

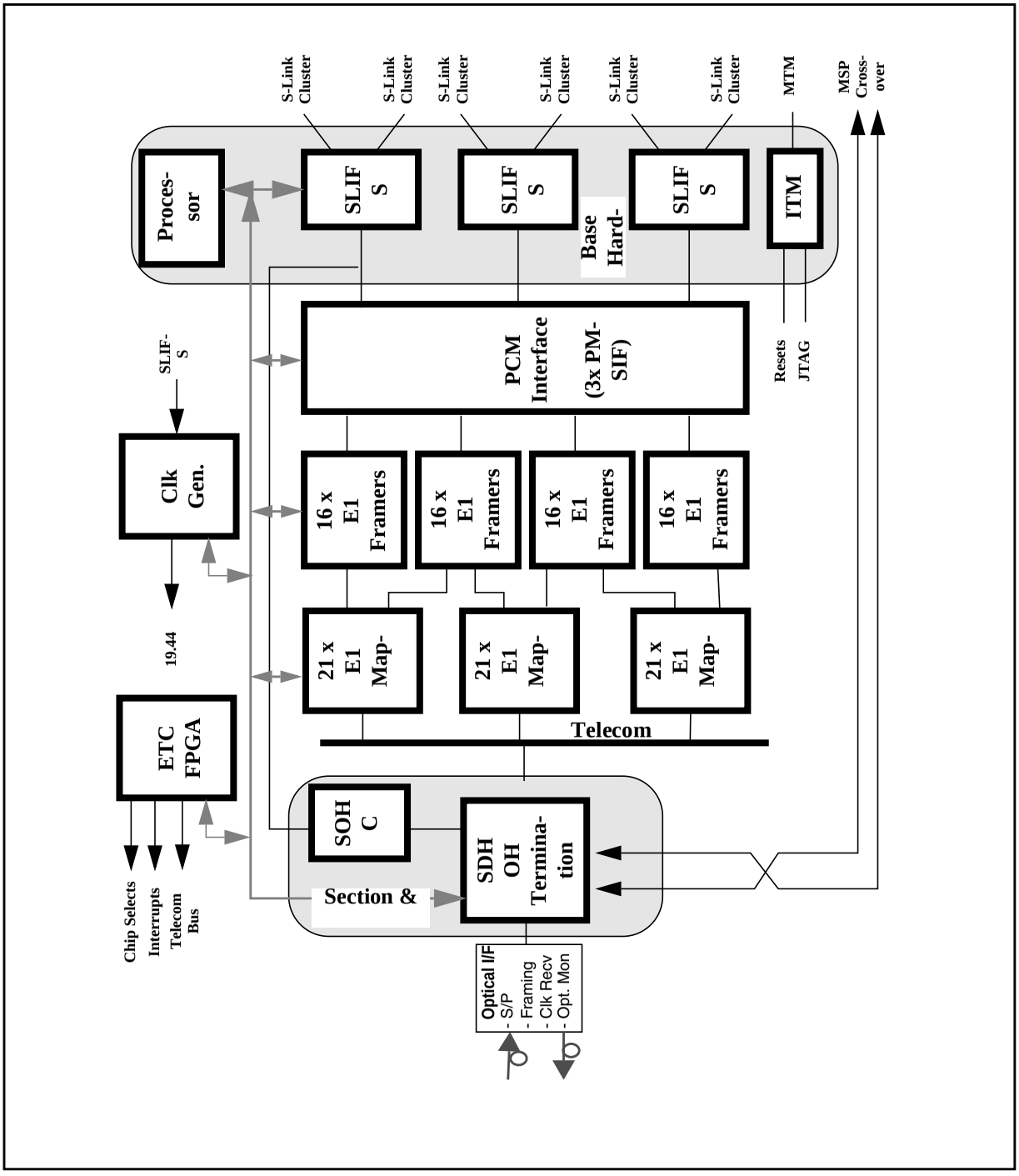
- Optical and Section/Line Interface
- E1 Mapping and Multiplexing
- E1 Framing
- PCM Interface
- Base Hardware
- Clock Generation
- ETC

### Functional block diagram

The next diagram is an illustration of the functional block diagram of the STM-1 RM.

# NTLX99BA STM-1 Resource Module (continued)

### NTLX99BA functional block



## NTLX99BA STM-1 Resource Module (continued)

### Optical and section/line interface

This subsection is responsible for providing a Short and Intermediate reach STM-1 optical transceiver (155.52Mb/s), and termination of the section and line portions of the overhead. The Electro-Optic (E/O) modules are separate. receiver and transmitter units which provide both short reach and intermediate reach capabilities. The laser output can be disabled for safety and diagnostic purposes. The transmit module is monitored for laser bias and optical output power level to detect end of life conditions. The receive module provides low light and received power indications.

Overhead termination is provided with a third party vendor device, the PMC-Sierra PM5343 SONET/SDH Transport Overhead Transceiver. Line defect detection, performance related overhead, protection switching overhead, and alarms are detected by this device, which is serviced by the local processor.

The PM5343 SONET/SDH is assigned the highest interrupt priority of all the devices on the board to ensure the capability of performing an immediate protection switch should a link fault occur. To assist in severe link fault detection, the E/O module and clock/data recovery sections monitor for loss of light and signal and report these error conditions though the PM5343. The current version of the PM5343 SONET/SDH provides a special B2 error monitor is provided which monitors B2 errors over programmable periods of time. If the error rate during a period should exceed a programmable limit, an interrupt will be generated via the PM5343 and software can determine if a protection switch is required.

The system side of the PM5343 datapath interfaces directly with the PM5344 via a byte parallel PCM data bus which is parity protected.

STM-1 section and high order path hardware handles both the section and high order path overhead. Overhead is handled in one of three ways:

- terminated directly in hardware
- extracted and made available to the STM-1 RM local processor
- extracted and passed to the Common Equipment Module (CEM), via the SDH OverHead Controller (SOHC) FPGA

The principle components of the SDH Section and High Order Path Termination block are the PMC-Sierra PM5343 SONET/SDH Transport Overhead Transceiver (STXC) and PM5344 SONET/SDH Path Terminating Transceiver (SPTX). These devices are used in the same way as the OC-3 RM and the SARD reference design from PMC-Sierra.

## NTLX99BA STM-1 Resource Module (continued)

The functional block also supports the necessary hardware to control the multiplexor section protection (MSP) path betweeen the two STM-1 resource modules in the Spectrum shelf MSH is an SDH requirement.

### Optical interface

The optical receiver recovers the STM-1 signal from the fiber, the recovered 155.52 Mb/s data signal is delivered to the Cypress Semiconductor CY7B952 SONET Serial Transceiver (SST). This device recovers clock from the data signal, and provides retimed Positive ECL (PECL) data and clock signal at 155.52Mb/s to the PM5343 (STXC).

The STXC performs SONET/SDH frame recovery and termination of the Section and Line overhead. The receive features of this device are:

- SDH Framing
- B1 and B2 bit interleaved parity checking and counting
- J0 Trace or STS ID support
- Diagnostic loopback
- Line side loopback

The PM5343 performs most of the hardware performance monitoring required for the STM-1 RM application, including B2 error counting, B2 error rate monitoring frame, and signal loss monitoring. There are a few performance monitoring needs that are not handled by this device. Loss of signal and receive optical power monitoring are performed externally.

### External optical interface

The external optical interface connects the STM-1 RM to the external world. The optics operate at a nominal wavelength of 1310 nanometers into a singlemode fiber and at a data rate of 155.52 Mb/s. The STM-1 RM uses separate transmitter and receiver modules developed by the Nortel Optoelectronics Group.

The transmitter module consists of an uncooled laser operating at a wavelength of 1310 nanometers and meets the short reach (SR) and intermediate reach-1 (IR-1) SDH specifications, as well as specifications for SONET and ATM. The transmitter uses proprietary Silicon V-groove technology for precise fiber alignment and optical output level control. Also included in the device is an integrated laser driver IC for laser control, as well as analog monitor outputs of the laser bias current (LBC) and the optical power output level as measured using a back facet monitor (BFM). The laser can be externally disabled for safety and diagnostics. The transmitter operates from a single 5 volt supply and is packaged in a plastic dual inline package (DIP) and utilizes an industry

## NTLX99BA STM-1 Resource Module (continued)

standard 20 pin footprint, thus allowing for multiple sources. The optical interface is terminated with a ruggedized (perisil) singlemode fiber pigtail using an SC connector. Specifications for the transmitter as used in the STM-1 RM design are listed in the next table.

**STM-1 RM optical transmitter specifications**

| Parameter | MIn. | Max. | Units |
|---|---|---|---|
| Supply Voltage | 4.7 | 5.5 | Volts |
| Case Temperature | -40 | 70 | Degrees C |
| Center Wavelength | 1261 | 1360 | nm |
| Mean Output Power | -15 | -8 | dBm |
| RMS Spectral Width | | 7.7 | nm |
| Extinction Ratio | 8.2 | | dB |

The receiver module consist of a PIN photodiode detector operating at 1310 nanometers and meets the SR and IR-1 SDH specification, as well as specifications for SONET and ATM. The receiver also uses Silicon V-groove technology for precise fiber alignment and optimum sensitivity. Also included in this device is an integrated limiting amplifier, as well as a loss of signal (LOS) alarm and an analog monitor output of the received light level. The receiver operates from a single 5 volt supply and is packaged in a plastic dual inline package (DIP) and utilizes an industry standard 20 pin footprint. The optical interface is terminated with a ruggedized (perisil) multimode fiber pigtail using an SC connector. Specifications for the receiver as used in the STM-1 RM design are listed in the next table.

**STM-1 RM optical receiver specifications**

| Parameter | Min. | Max. | Units |
|---|---|---|---|
| Supply Voltage | 4.7 | 5.5 | Volts |
| Case Temperature | -40 | 70 | Degrees C |
| Center Wavelength | 1261 | 1360 | nm |
| Sensitivity | | -37 | dBm |
| Overload | -5 | | dBm |

## NTLX99BA STM-1 Resource Module (continued)

### E1 Mapping and multiplexing

The E1 Mapping and Multiplexing block maps sixty three E1 payloads into sixty three VC-12 containers which are then multiplexed up to three TUG-3s. This function is performed entirely by three SXT6251 “21 E1 Mapper” devices from Level1 Communications.

### E1 Framing

In the receive direction framing is the process of locating the start-of-frame in an incoming stream of bits; converting the bit stream to a synchronous payload byte stream; detecting alarms and extracting signalling information.

In the transmit direction, synchronous payload and signalling byte streams are encapsulated in a frame structure and sent off as a stream of bits.

In addition to the function above, the framers used on the STM-1 RM support slip buffers on the receive side to absorb the phase and frequency differences between the received E1 stream and the PCM Interface block.

The STM-1 RM supports sixty three independent E1 framers.

### PCM interface

The role of the PCM Interface block is to provide a glue-logic function between the synchronous PCM interface of the three SLIF-S devices and the E1 framers. The PCM Interface block is implemented using the PCM, Metering and Signalling Interface (PMSIF) design which is fitted into an Altera 10K100 FPGA. Three PMSIF devices are used, one per SLIF-S. Each PMSIF interfaces to four quad E1 framers.

### Base hardware

The principle features of the STM-1 base hardware are listed below:

- Motorola MC68EN360 (QUICC) based processor complex
- Spectrum S-Link interface to the CEM supported by three SLIF-S ASIC
- Module Test, Reset and Maintenance supported by the ITM ASIC
- Point of Use Power Supply (PUPS) providing both +5V and +3.3V

### Clock generation

The STM-1 Resource Module uses five separate clock structures:

- Processor clock: A 25 MHz clock generated by a 3.3V crystal oscillator.
- SLIF-S clock: 24.576 MHz selected from the active CEM. This clock and associated framing signals are provided by the SLIF-S device, as well as the 6.144 MHz byte clock used by the PCM Interface block (PMSIF).

- E1 clock: 2.048 MHz clock generated by the PMSIF FPGA by dividing down the SLIF-S clock.
- Transmit line rate clock: 19.44MHz generated from the selected S-Link Interface clock via an on board phase-locked loop.
- Receive line rate clock: 155.52 and 19.44 MHz clocks are extracted from the receive data by the LIU, and used to clock data into the STXC.

### ETC

The ETC is an FPGA which supports all the glue logic functions on the STM-1 RM. Its primary roles are chip select generation, interrupt consolidation and Telecom Bus control.

## Backplane interface

### Backplane signal description

The NTLX99BA is designed to install in one of the so-called “high-speed” slots of the Spectrum shelf. These slots are called high-speed because they support the physical connections for three S-Link clusters (total of nine S-Links). The naming convention, function and type of signals presented to Resources Modules in a Spectrum shelf is given in the next table.

| Conn. NO. | Signal | Function | IO type | Description |
|---|---|---|---|---|
| J1 | -48B | Power | | -48V Battery Feed B |
| J1 | RET | Power | | Battery Return |
| J1 | -48A | Power | | -48V Battery Feed A |
| J2 | FrCEMnCKm | Input | 3.3V CMOS SLIF-S | S-Link Clock Lines from Common Equipment (n=0 CEM0, n=1 CEM1) |
| J2 | FrCEMnDm | Input | 3.3V CMOS SLIF-S | S-Link Data Lines from Common Equipment (n=0 CEM0, n=1 CEM1) n=1,2,3 on J2 |
| J2 | ToCEMnCKm | Output | 3.3V CMOS SLIF-S | S-Link Clock Lines to Common Equipment (n=0 CEM0, n=1 CEM1) |

## NTLX99BA STM-1 Resource Module (continued)

| Conn. NO. | Signal | Function | IO type | Description |
|---|---|---|---|---|
| J2 | ToCEMnDm | Output | 3.3V CMOS<br>SLIF-S | S-Link Data Lines to Common Equipment (n=0 CEM0, n=1 CEM1)<br>n=1,2,3 on J2 |
| J2 | SYNC_ToCEM0<br>SYNC_ToCEM0<br>SYNC_FrOC3<br>SYNC_FrOC3 | Output | 3.3V TTL<br>(74LVT16244) | STM-1 Recovered Frame Pulse, used by CEM, or Clock RM for synchronization. |
| J2 | MMD | Input | 3.3V CMOS<br>ITM | JTAG 1149.5 Bus Master Data |
| J2 | MSD | Input/Output<br>Open Drain | 3.3V CMOS<br>ITM | JTAG 1149.5 Bus Slave Data |
| J2 | MCLK | Input | 3.3V CMOS<br>ITM | JTAG 1149.5 Bus Clock |
| J2 | MPR | Input/Output<br>Open Drain | 3.3V CMOS<br>ITM | JTAG 1149.5 Bus Request |
| J2 | MCTL | Input | 3.3V CMOS<br>ITM | JTAG 1149.5 Bus Control |
| J2 | LGND | Power | | logic ground of the PCP/BACKPLANE |
| J3 | FrCEMnCKm | Input | 3.3V CMOS<br>SLIF-S | S-Link Clock Lines from Common Equipment (n=0 CEM0, n=1 CEM1)<br>m=2,3 on J3 |
| J3 | FrCEMnDm | Input | 3.3V CMOS<br>SLIF-S | S-Link Data Lines from Common Equipment (n=0 CEM0, n=1 CEM1)<br>n=4,5,6,7,8,9 on J3 |

## NTLX99BA STM-1 Resource Module (continued)

| Conn. NO. | Signal | Function | IO type | Description |
|---|---|---|---|---|
| J3 | ToCEMnCKm | Output | 3.3V CMOS<br>SLIF-S | S-Link Clock Lines to Common Equipment (n=0 CEM0, n=1 CEM1)<br>m=2,3 on J3 |
| J3 | ToCEMnDm | Output | 3.3V CMOS<br>SLIF-S | S-Link Data Lines to Common Equipment (n=0 CEM0, n=1 CEM1)<br>n=4,5,6,7,8,9 on J3 |
| J3 | LGND | Power | | logic ground of the PCP/BACKPLANE |
| J4 | Drop0Datan<br>Drop0C1J1<br>Drop0PL<br>Drop0PAR | Output | 3.3V TTL<br>(74LVT16244) | Inter STM-1 Resource Module Telecom Bus Drop0Datan ranges from n=0 to n=7. |
| J4 | Add0Datan<br>Add0C1J1<br>Add0PL<br>Drop0Par | Input | 3.3V TTL<br>(74LVT16244) | Inter STM-1 Resource Module Telecom Bus Add0Datan ranges from n=0 to n=7. |
| J4 | LGND | Power | | logic ground of the PCP/BACKPLANE |

## NTLX99BA STM-1 Resource Module (continued)

### Backplane connector and pin description

The STM-1 RM supports four Molex box receptacle backplane connectors, which on the 1W1 board are labeled P3, P4, P5 and P8 (the connector labels are likely to change for later revisions of the board). P3 is a 1U 5x7 (35 pin) connector while P4, P5 and P8 are 2U 5x17 (85 pin) connectors. The pins for all connectors are identified by a column letter (A through E) and a row number (2 through N). The primary interfaces supported by each of the four connectors is as follows:

- P3, battery supply
- P4, S-link cluster #1 and MTM bus
- P5, S-link clusters #2 and #3
- P8, cross-over

***Note:*** The shaded cells indicate advanced length pins.

| Pin No. | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | -48B | -48B | -48B | -48B | -48B |
| 3 | NC | NC | NC | NC | NC |
| 4 | NC | NC | NC | NC | NC |
| 5 | RTN | RTN | RTN | RTN | RTN |
| 6 | NC | NC | NC | NC | NC |
| 7 | NC | NC | NC | NC | NC |
| 8 | -48A | -48A | -48A | -48A | -48A |

## NTLX99BA STM-1 Resource Module (continued)

| Pin No. | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | SYNC_ToCEM0 | LGND | LGND | LGND | SYNC_FrOC30 |
| 3 | SYNC_ToCEM1 | .NC. | LGND | .NC. | SYNC_FrOC31 |
| 4 | LGND | LGND | LGND | LGND | LGND |
| 5 | .NC. | .NC. | LGND | .NC. | .NC. |
| 6 | .NC. | .NC. | LGND | .NC. | .NC. |
| 7 | ToCEM0_D2 | ToCEM0_D1 | LGND | ToCEM1_D1 | ToCEM1_D2 |
| 8 | ToCEM0_D3 | ToCEM0_CK | LGND | ToCEM1_CK | ToCEM1_D3 |
| 9 | FrCEM0_D2 | FrCEM0_D1 | LGND | FrCEM1_D1 | FrCEM1_D2 |
| 10 | FrCEM0_D3 | FrCEM0_CK | LGND | FrCEM1_CK | FrCEM1_D3 |
| 11 | LGND | LGND | LGND | LGND | LGND |
| 12 | .NC. | .NC. | LGND | .NC. | .NC. |
| 13 | .NC. | .NC. | LGND | .NC. | .NC. |
| 14 | .NC. | .NC. | LGND | .NC. | .NC. |
| 15 | .NC. | .NC. | LGND | .NC. | .NC. |
| 16 | SLOT_ID4 | SLOT_ID3 | MCTL | SLOT_ID1 | SLOT_ID0 |
| 17 | LGND | MPR | SLOT_ID2 | MCLK | LGND |
| 18 | MMD | LGND | LGND | LGND | MSD |

## NTLX99BA STM-1 Resource Module (continued)

| Pin No. | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | LGND | LGND | LGND | LGND | LGND |
| 3 | .NC. | .NC. | LGND | .NC. | .NC. |
| 4 | .NC. | .NC. | LGND | .NC. | .NC. |
| 5 | .NC. | .NC. | LGND | .NC. | .NC. |
| 6 | LGND | LGND | LGND | LGND | LGND |
| 7 | LGND | LGND | LGND | LGND | LGND |
| 8 | LGND | LGND | LGND | LGND | LGND |
| 9 | ToCEM0_D8 | ToCEM0_D7 | LGND | ToCEM1_D7 | ToCEM1_D8 |
| 10 | ToCEM0_D9 | ToCEM0_CK 3 | LGND | ToCEM1_CK 3 | ToCEM1_D9 |
| 11 | FrCEM0_D8 | FrCEM0_D7 | LGND | FrCEM1_D7 | FrCEM1_D8 |
| 12 | FrCEM0_D9 | FrCEM0_CK3 | LGND | FrCEM1_CK3 | FrCEM1_D9 |
| 13 | LGND | LGND | LGND | LGND | LGND |
| 14 | ToCEM0_D5 | ToCEM0_D4 | LGND | ToCEM1_D4 | ToCEM1_D5 |
| 15 | ToCEM0_D6 | ToCEM0_CK 2 | LGND | ToCEM1_CK 2 | ToCEM1_D6 |
| 16 | FrCEM0_D5 | FrCEM0_D4 | LGND | FrCEM1_D4 | FrCEM1_D5 |
| 17 | FrCEM0_D6 | FrCEM0_CK2 | LGND | FrCEM1_CK2 | FrCEM1_D6 |
| 18 | LGND | LGND | LGND | LGND | LGND |

## NTLX99BA STM-1 Resource Module (continued)

| Pin No. | A | B | C | D | E |
|---|---|---|---|---|---|
| 2 | LGND | LGND | LGND | LGND | LGND |
| 3 | Drop0Data0 | Drop0Data1 | Add0Data2 | Add0Data1 | Add0Data0 |
| 4 | Drop0Data3 | Drop0Data4 | Drop0Data2 | Add0Data4 | Add0Data3 |
| 5 | Drop0Data5 | Drop0Data6 | LGND | Add0Data6 | Add0Data5 |
| 6 | Drop0Data7 | Drop0SPE | LGND | Add0SPE | Add0Data7 |
| 7 | Drop0C1J1V1 | Drop0CLK | LGND | Add0CLK | Add0C1J1V1 |
| 8 | Drop0Parity | LGND | LGND | LGND | Add0Parity |
| 9 | LGND | .NC. | LGND | .NC. | LGND |
| 10 | .NC. | .NC. | .NC. | .NC. | .NC. |
| 11 | .NC. | .NC. | .NC. | .NC. | .NC. |
| 12 | .NC. | .NC. | LGND | .NC. | .NC. |
| 13 | .NC. | .NC. | LGND | .NC. | .NC. |
| 14 | .NC. | .NC. | LGND | .NC. | .NC. |
| 15 | LGND | LGND | LGND | LGND | LGND |
| 16 | SpTx0 | SpTx1 | LGND | SpRx1 | SpRx0 |
| 17 | SpTx2 | SpTx3 | LGND | SpRx3 | SpRx2 |
| 18 | LGND | LGND | LGND | LGND | LGND |

## NTLX99BA STM-1 Resource Module (end)

# Performance specifications

### Thermal profile

The Spectrum STM-1 module is designed to operate in a controlled environment room in a forced air cooled DMS-100 frame. Component temperatures will be less than 75 ºC (167 ºF) over the specified operating temperature range of -5 ºC (+23 ºF) to +45 ºC (+113 ºF). (104 ºF).

### Electromagnetic interference

### RF susceptibility

The equipment satisfies Bellcore Technical Reference TR-NWT-001089, Sections 3.3.1 through 3.3.5 and TR-NWT-000063.

### Electromagnetic compliance

The equipment satisfies Bellcore Technical Reference TR-NWT-001089, Emissions Requirements, Sections 3.2.1 through 3.2.6 and FCC Regulations, part 15.

### Electrostatic discharge

The equipment satisfies Bellcore Technical Reference TR-NWT-001089, ESD Immunity Requirements, Sections 2.4 through 2.6.

# 10 NTMXnnaa

## NTMX45AA through NTMX99AA

# NTMX45AA

## Product description

The NTMX45AA is a Motorola 68020–based processor card that provides Emergency Stand–Alone (ESA) capability to the following extended multiprocessor system (XMS)–based peripheral modules (XPM) of the DMS–100:

- remote line concentrating module (RLCM)
- PCM30 remote line concentrating module (PRLCM)
- outside plant access cabinet (OPAC)
- international outside plant access cabinet (IOPAC)

### Location

The NTMX45AA is located in slot 15 of the host interface equipment (HIE) shelf.

## Functional description

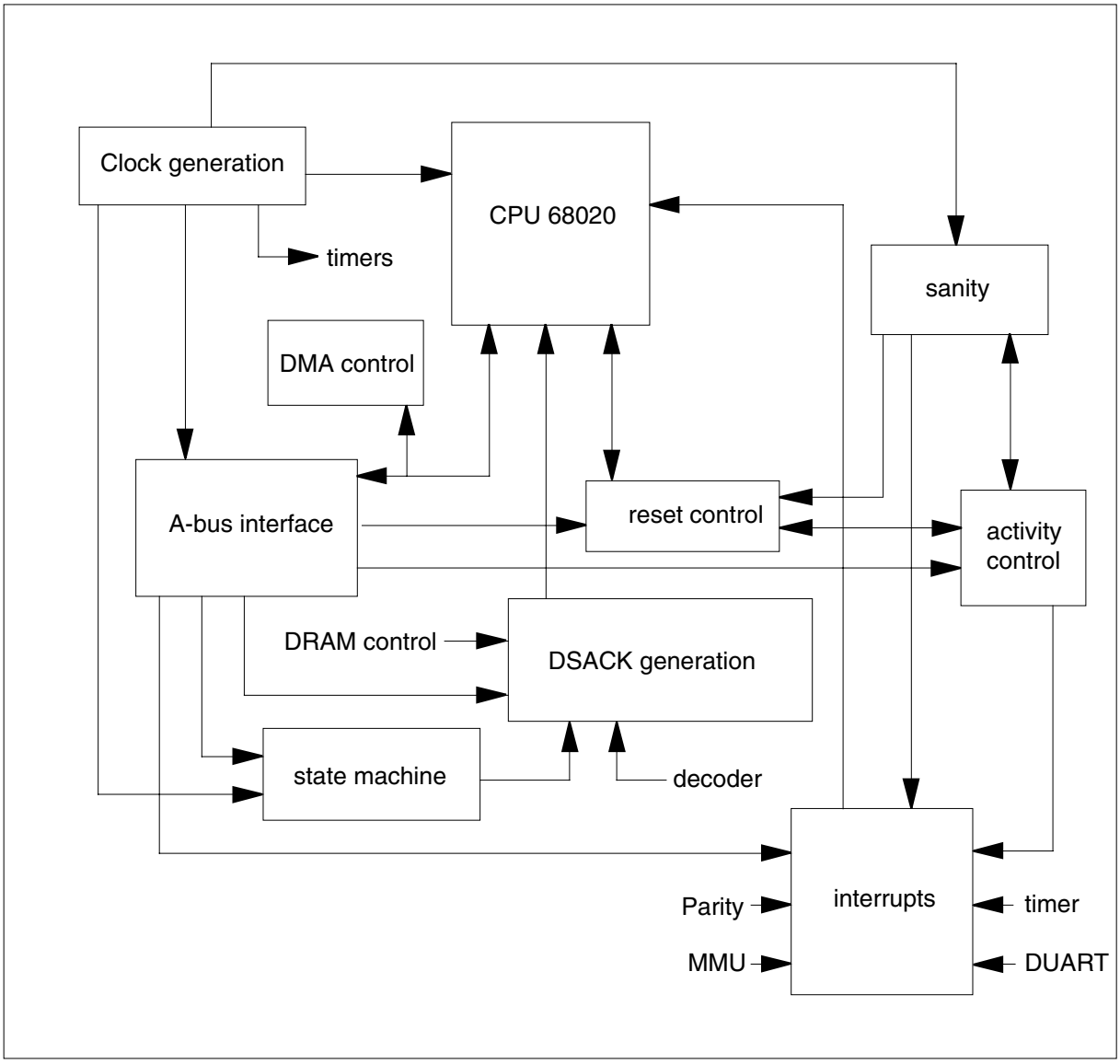
The NTMX45AA contains the following functional blocks:

- CPU 68020
- clock generation
- timing state machine
- decoder
- data strobe acknowledge signal (DSACK) generation
- memory management unit (MMU)
- dynamic RAM (DRAM)
- programmable read–only memory (PROM)
- identification PROM
- E2PROM
- address–bus (A–bus) interface
- direct memory access (DMA)
- dual universal asynchronous receiver transmitter (DUART)
- programmable timers
- status register
- command register
- activity control

- interrupts
- sanity timers
- reset

The figure that follows shows the relationship of the functional blocks.

**NTMX45AA functional blocks**



## **NTMX45AA** (continued)

### CPU 68020

The CPU is a 16 MHz 68020 processor with the capacity for 32 bits of data and 32 bits of address storage. This processor has a 256 byte logical instruction cache. The cache operates under normal conditions.

### Clock generation

The 16 MHz oscillator provides clock signals for the pack. A phase–locked loop (PLL) based clock generator provides 32 MHz, 16 MHz, and 8 MHz clocks with synchronous edges. An application specific integrated circuit (ASIC) uses dividers to generate the 1.28 MHz and 71.1 kHz clocks from the 32 MHz clock.

### State machine

The state machine synchronizes CPU activity. The state machine is the basis of the timing for DRAM, DSACK signals, and other control signals. The CPU restarts the state machine at the beginning of each bus cycle. DMA also restarts the state machine at the beginning of each bus cycle.

### Decoder

All address decoding is off the CPU address bus. This avoids delays or translation performed by the MMU.

### Data strobe acknowledge signal generation

The bus master waits for the DSACK signal when a bus cycle begins. This DSACK signal indicates that a data transfer completed. DSACK signals generated from the state machine, timing signals from the gray–bus, decoder outputs, and DSACK equivalent signals generated from DRAM and the A–bus are inputs to the DSACK logic. DSACK signals are generated back to the CPU and A–bus.

### Memory management unit

The MMU translates the CPU virtual address to a real address for the memory. The MMU also provides access protection for each segment of the address space. The MMU has a fast SRAM capacity of 2 kbytes times 28 bits. The CPU completes a read or write to the MMU SRAM within one wait state.

The MMU has two logical sections. One half of the MMU is for CPU address and the other half is for DMA accesses. In the event of a protection violation, the error information is latched and an interrupt generated. The CPU can read and write to the translation data in the SRAM. Likewise, the CPU can read the MMU error register.

### Dynamic RAM

The NTMX45AA has 8 Mbytes of DRAM. DRAM is in two banks. Each bank accepts 4 Mbytes arranged as 1 Mbit by 32 bits, plus parity. A parity generator and a parity checker generate parity. The system writes parity bit to a parity RAM chip.

The CPU normally completes a read or write to the DRAM within one wait state. When a DRAM refresh cycle collides with a DRAM access, the access requires five wait states to complete.

### PROM

The programmable read only memory (PROM) has a storage capacity of 128 kbytes. The PROM stores a bootstrap loader that is nonvolatile. After a reset, the bootstrap loader selects which E2PROM bank is executable. Access time to the PROM is three wait states.

### Identification PROM

The identification PROM (IDPROM) has 8 kbytes of storage. This part maintains board identification information such as the PEC and version of the card. Software reads this information from the chip within three wait states.

### E2PROM

The electrically erasable PROM (E2PROM) has two identical banks of 128 kbytes by 16 bits. One bank of memory is executable and the other is loadable. Each bank stores a complete copy of the main XPM firmware code. The firmware is downloadable and allows the operating company to update firmware for new features with the pack in service. Access to the E2PROM occurs within three wait states.

### A–bus interface

Communication with the rest of the peripheral occurs through the A–bus interface. The ESA processor is a bus master to most other cards in the unit. The A–bus interface is also available as a slave device through DMA.

### Direct memory access

Cards such as the enhanced ISDN signaling preprocessor (EISP) or ethernet paddle card (EPC) can access the memory of the ESA processor through DMA. The DMA master device seizes control of the A–bus and the CPU address bus within the ESA processor. The MMU translates the address inputs before memory access. The ESA processor can use both byte and word DMA accesses.

## NTMX45AA (continued)

### DUART

The dual universal asynchronous receiver/trasmitter (DUART) supplies two serial ports for the ESA processor. The serial interface meets with Electronics Industry Association (EIA) standard RS–232C. Baud rates for the DUART are programmable. The CPU determines the DUART mode of operation and the DUART interrupts the CPU when the DUART sends or receives a byte.

### Programmable timers

The ESA processor has two timer chips. Each timer chip has three separate 16 bit counters clocked with the 1.28MHz clock. These two programmable timers have the following functions:

- Timer one generates timing clocks for the two serial interfaces and does not use the third counter.
- Timer two generates the clock tick interrupt for the card and interrupts the CPU every 10 ms. The second and third counters operate as a 32 bit counter to generate the software controlled sanity clock.

Access to the timers occurs within four wait states.

### Status register

The status register is a 32 bit register available to the CPU. The register holds information about activity, memory size, parity interrupts, E2PROM status, and other operational data. Access to the status register occurs within two wait states.

### Command register

The CPU uses the command register to control parity calculation, faceplate LEDs, and to disable DMA. Access to the command register occurs within two wait states.

### Activity control

The activity control circuit starts or stops (gains or drops) unit activity.

The unit starts activity when the following two events occur:

- No activity drop is present.
- The mate unit is inactive.

The unit stops activity when the following five events occur:

- The activity timer expires.
- Software requests an activity drop.
- The ESA processor is reset.

- The main CPM clock fails. The main clock fails when the clock loses clocking for more than 1 ms or loses frame pulse for 540 ms.
- The ESA processor card is not fully inserted in the shelf.

### Interrupts

The CPU has seven levels of interrupts:

- Level 7 Sanity timer, backplane break pin
- Level 6 Parity error during DRAM read
- Level 5 MMU protection violation
- Level 4 External interrupt from the messaging card
- Level 3 Clock tick interrupt from timer two
- Level 2 DUART communication
- Level 1 Peripheral input/output, eight sources can cause this interrupt
  - port 0: activity gain interrupt
  - port 1: 3 ms timeswitch interrupt
  - port 2: unused
  - port 3: unused
  - port 4: 2 ms interrupt from NT6X28
  - port 5: STB interrupt for TAC daughterboard interrupts
  - port 6: unused
  - port 7: switch activity clock interrupt

### Sanity timers

A sanity circuit protects the system from software failures. The sanity circuit contains a software sanity timer and a hardware sanity timer. Both timers feed output to the same circuit. If a timer expires once, that expiration is latched. If it expires again before the CPU acknowledges the sanity, the CPU receives a level 7 non–maskable interrupt. If the CPU does not reset the sanity timer in another one–half the sanity interval, the sanity circuit triggers a shelf reset. Time intervals for hardware and software are different.

The software watchdog expires every 160 ms. This timer is potentially not protected because insane software can disable it.

## **NTMX45AA** (continued)

The hardware watchdog is a free running counter separate from the software watchdog. This timer expires approximately every 14.5 seconds. Three sources reset this timer:

- CPU access to activity acknowledge address
- a shelf reset
- the ESA processor gaining activity

### Reset

The system sends a reset signal to the CPU when any of the following events occur:

- power up
- an activity drop without software prepare
- unacknowledged sanity timer expiration
- an external reset from the message card
- reset output from the CPU

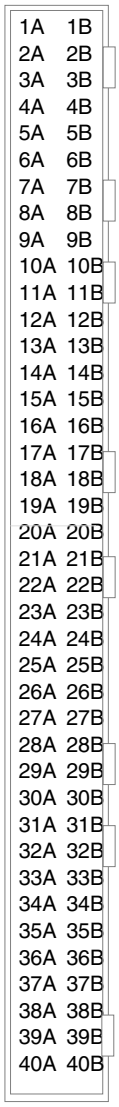
The reset duration is 100 ms.

# Signaling

### Pin outs

The figure that follows shows the pin outs for NTMX45AA.

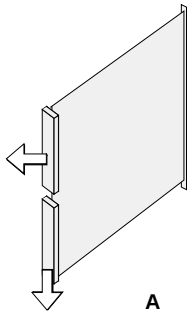
### NTMX45AA pin outs



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | +5V | +5V |
| 4A 4B | +5V | +5V |
| 5A 5B | GND | GND |
| 6A 6B | *–BREQ | –BG |
| 7A 7B | –BUSGRI | –MODRST |
| 8A 8B | **–ACTIVE0 | –MSGRST |
| 9A 9B | –BUSBSY | MATECK FAIL |
| 10A 10B | 32MEG | |
| 11A 11B | GND | –ACTIVE1 |
| 12A 12B | –DAS | AS+ |
| 13A 13B | –LDS | 16MEG |
| 14A 14B | –DTACK | |
| 15A 15B | –UDS | |
| 16A 16B | –BWRT | –SANDIS |
| 17A 17B | 8MEG | |
| 18A 18B | –RSTIN | |
| 19A 19B | | PARINT |
| 20A 20B | –PERINT1 | –MSGIRQ |
| 21A 21B | –PERINT2 | –ECS |
| 22A 22B | GND | +5MFAIL |
| 23A 23B | –PERINT3 | –RMC |
| 24A 24B | –PERINT4 | |
| 25A 25B | –PERINT5 | –MATEACT |
| 26A 26B | –PERINT6 | –OWNACT |
| 27A 27B | –PERINT7 | GND |
| 28A 28B | –MEMIRQ | |
| 29A 29B | ADD1 | |
| 30A 30B | ADD2 | HPU+12 |
| 31A 31B | ADD3 | HDICLK |
| 32A 32B | ADD4 | HDOCLK |
| 33A 33B | ADD5 | HACKOUT |
| 34A 34B | GND | HDOUT |
| 35A 35B | ADD6 | HDIN |
| 36A 36B | ADD7 | TPU12+ |
| 37A 37B | ADD8 | TACKIN |
| 38A 38B | ADD9 | TDOUT |
| 39A 39B | ADD10 | TDIN |
| 40A 40B | ADD11 | GND |

**Legend**

| | |
|---|---|
| *CPM version | –BG is 6B |
| | –ACTIVE0 is 8A |
| **XPM version | –BG is 8A |
| | –ACTIVE0 is 6B |



| | A | B |
|---|---|---|
| 41A 41B | GND | BERR– |
| 42A 42B | ADD12 | –DS |
| 43A 43B | ADD13 | –DSACK0 |
| 44A 44B | ADD14 | |
| 45A 45B | ADD15 | CKFAIL |
| 46A 46B | ADD16 | –BREAK |
| 47A 47B | ADD17 | GND |
| 48A 48B | ADD18 | ST3 |
| 49A 49B | ADD19 | ST2 |
| 50A 50B | ADD20 | ST1 |
| 51A 51B | ADD21 | ST0 |
| 52A 52B | ADD22 | SPAR1 |
| 53A 53B | GND | SPAR2 |
| 54A 54B | ADD23 | SPAR3 |
| 55A 55B | FC0 | SIZE0 |
| 56A 56B | FC1 | SIZE1 |
| 57A 57B | FC2 | ADD0 |
| 58A 58B | D0 | –ACTIVE3 |
| 59A 59B | D1 | GND |
| 60A 60B | D2 | –DCHFAIL |
| 61A 61B | D3 | –ACTIVE2 |
| 62A 62B | D4 | SPARE0 |
| 63A 63B | D5 | –CDIS |
| 64A 64B | GND | |
| 65A 65B | D6 | |
| 66A 66B | D7 | |
| 67A 67B | D8 | |
| 68A 68B | D9 | |
| 69A 69B | D10 | |
| 70A 70B | D11 | GND |
| 71A 71B | D12 | |
| 72A 72B | D13 | ST0 |
| 73A 73B | D14 | ST1 |
| 74A 74B | D15 | ST2 |
| 75A 75B | SWACST3 | |
| 76A 76B | GND | ST4 |
| 77A 77B | +12V | +12V |
| 78A 78B | GND | GND |
| 79A 79B | –12V | –12V |
| 80A 80B | GND | GND |

## **NTMX45AA** (end)

# Technical data

### Power requirements

The NTMX45AA requires a maximum of 4.0 A from the +5V supply.

## Product description

The DMS–100 peripheral modules use the NTMX71AA bus terminator card when operating company personnel upgrade the modules to XPM PLUS units. Use the NTMX71AA with the NTMX77AA card. The NTMX77AA card is the unified processor (UP).

## Functional description

The NTMX71AA terminates the address, data, and control signals from the NTMX77AA processor card on the XPM backplane. The NTMX77AA uses the XPM backplane to distribute the signals in the system.

The NTMX71AA is a passive circuit pack. This pack does not have active devices. The pack contains resistors, resistor networks, and capacitors.

You can use the NTMX71AA with the NTMX77AA card.

### Functional blocks

This chapter does not include a block diagram. The NTMX71AA has a simple design.

## Technical data

### Power requirements

The normal power use for the NTMX71AA is 0.25W. The NTMX71AA has a maximum power of 0.35W.

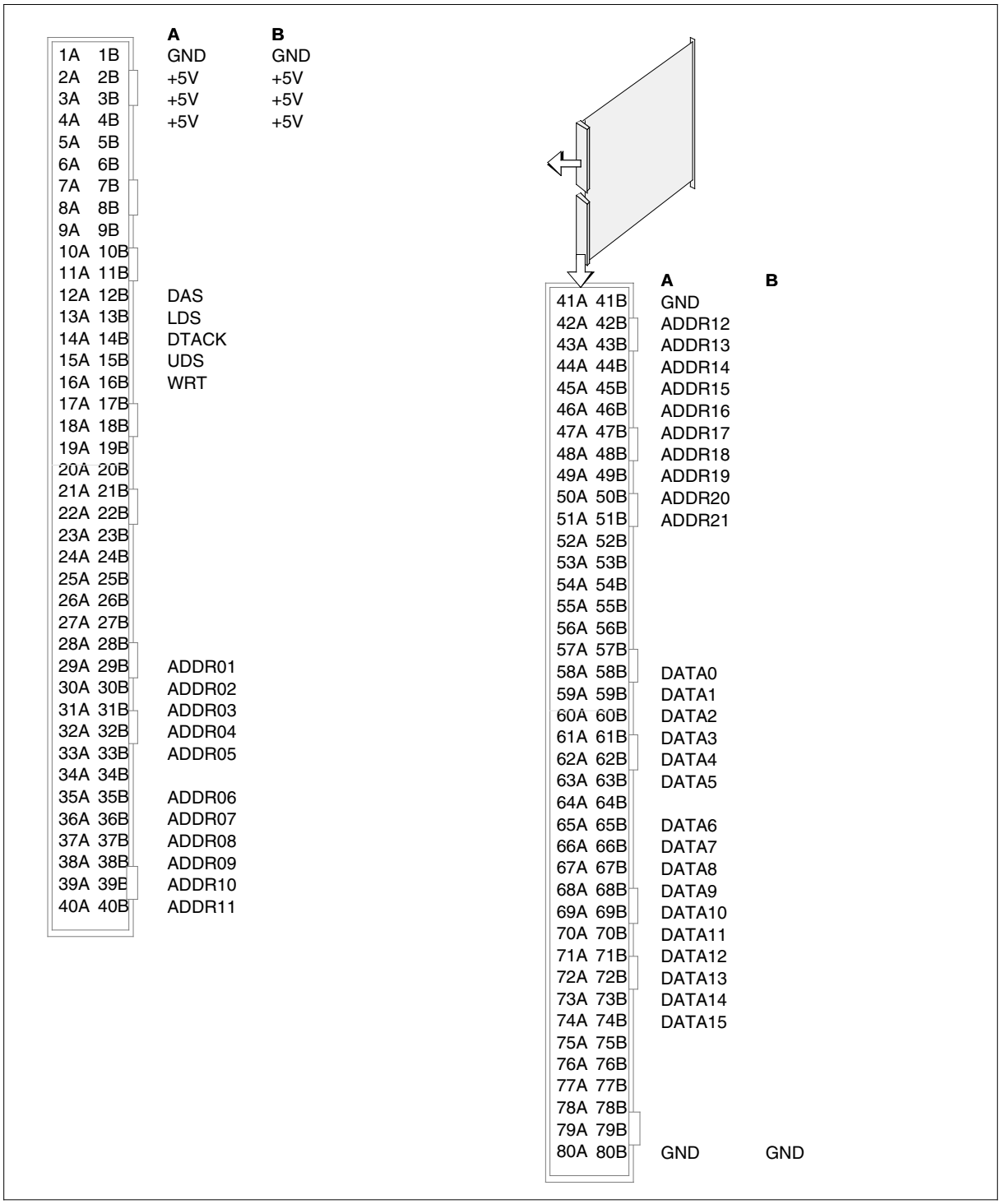
## Signaling

### Pin numbers

The pin numbers for the NTMX71AA appear in the following figure.

# **NTMX71AA** (end)

### NTMX71AA pin numbers



## Product description

The DMS–100 peripheral modules NTMX71BA use the XPM+ terminator paddleboard when operating company personnel upgrade the modules to XPM PLUS units. You can use the NTMX71BA with the NT6X0211 international 3–processor shelf.

## Functional description

The NTMX71BA is not backward compatible with NTMX71AA.

The NTMX71BA terminates the address bus, data, bus and four control signals from the NT6X0211 international 3–processor shelf. The NT6X0211 uses the XPM backplane to distribute the signals in the system.

The NTMX71BA is a passive circuit pack. The NTMX71BA does not have active devices. The pack contains resistors, resistor networks, and capacitors.

You can use the NTMX71BA with the NT6X0211 international 3–processor shelf.

### Functional blocks

This chapter does not include a block diagram. The NTMX71BA has a simple design. The circuit for the NTMX71BA has three sections:

### Address bus terminations

Each of the address lines terminates with a 75 ohm/330 pF shunt RC termination to GND. These terminations distribute high frequency noise and crosstalk on the address bus.

### Data bus terminations

Each of the data lines terminates with pull–up resistors. These resistors provide a steady–state value of approximately 3.5V.

### Control signal terminations

The control signals LDS, UDS, and DAS terminate with pull–up and pull–down resistors. These resistors provide steady–state value of approximately 3.2V.

## Technical data

### Power requirements

The normal power use for the NTMX71BA is 0.25W. The NTMX71BA has a maximum power of 0.35W.

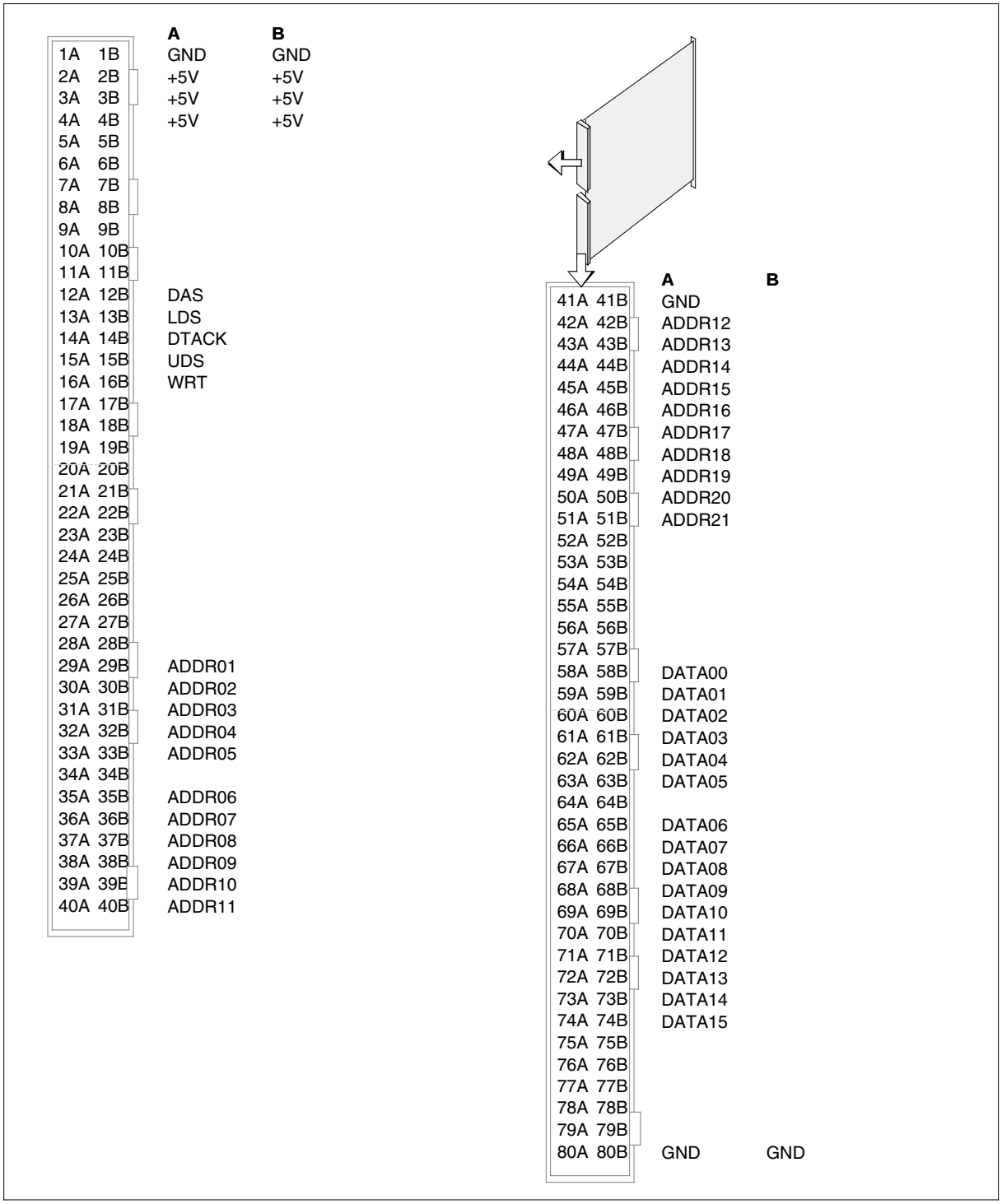
## **NTMX71BA** (continued)

# Signaling

### Pin numbers

The pin numbers for the NTMX71BA appear in the following figure.

### NTMX71BA pin numbers



# NTMX72AA

## Product description

The NTMX72AA power converter provides power for central processor and memory (CPM) digital switching equipment.

The NTMX72AA is a current circuit pack, and is not backward compatible.

### Location

The NTMX72AA fits in the right and left slots of the CPM shelf. The board faceplate is two slots wide.

## Functional description

The NTMX72AA power converter provides a regulated power supply with three different output voltages referenced to a common ground.

The power converter receives voltage from the nominal -48V office battery.

The NTMX72AA has the following features:

- three voltage outputs: +5V, +12V, -12V
- messaging with the signaling processor
- protection against overvoltage, undervoltage, overcurrent, and overtemperature
- a light-emitting diode (LED) maintenance status indicator on the faceplate
- test jacks for each output on the faceplate
- mate-converter power fail detection
- a D-channel handler (DCH) power fuse with trip signaling on the common frame supervisory panel (FSP) alarm lamp

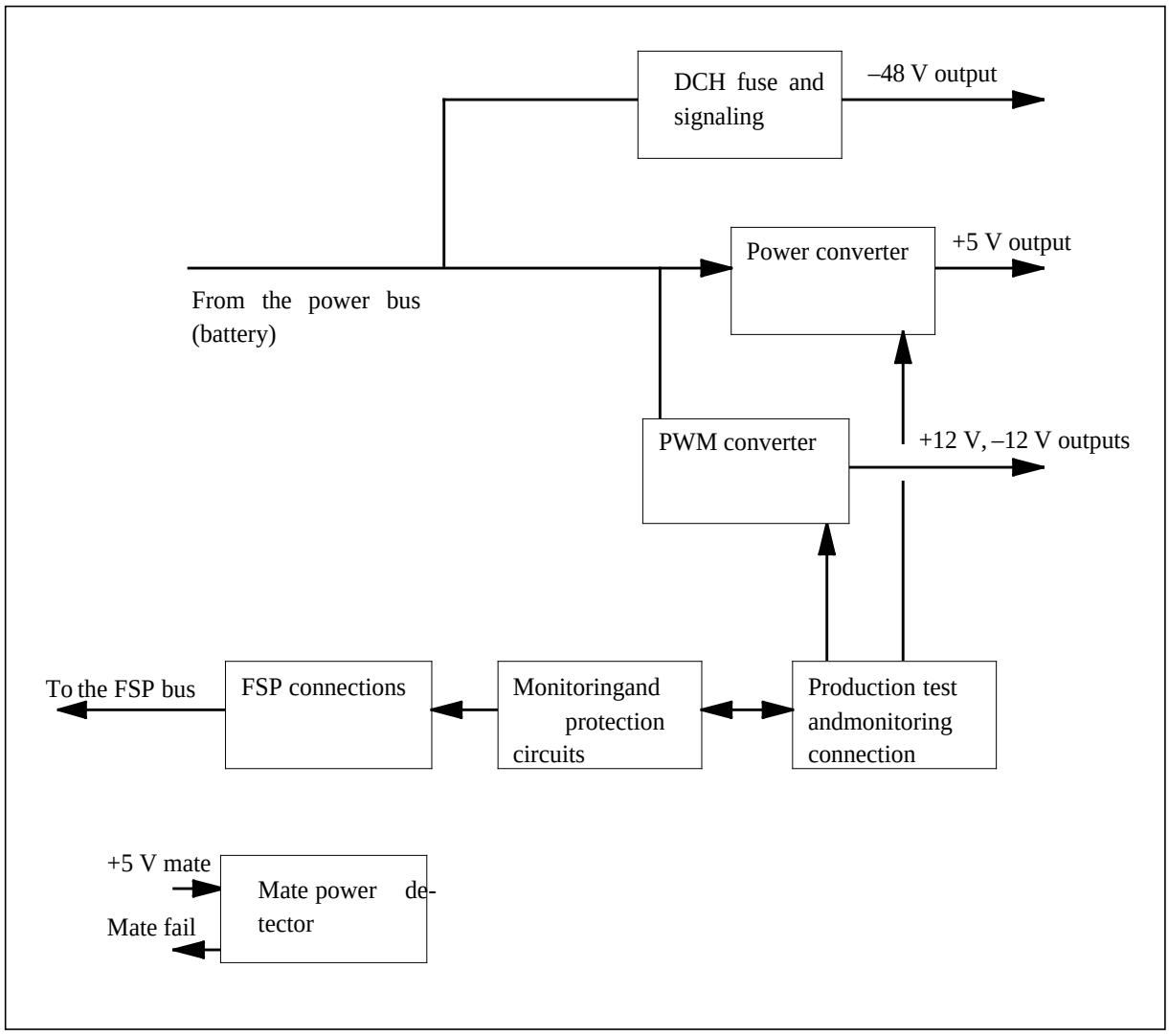
### Functional blocks

The NTMX72AA has the following functional blocks:

- 5V, 40A power converter
- 12V pulse width modulation (PWM) converter
- monitoring and protection circuits
- test and production monitoring connections
- FSP connections
- mate power detector
- DCH fuse and signaling

The relationship between the functional blocks appears in the following figure.

**NTMX72AA functional blocks**




### 5V, 40A power converter

The 5V 40A power converter contains VI-200 series direct current-to-direct current (dc-to-dc) converters. Each of these converters handles a maximum of 100W. The VI-200 series is a family of zero-current-switching component-level dc-to-dc resonant converters. These converters have an operating frequency of a maximum of 2 MHz. The converters have an internal overvoltage, overcurrent protection, and thermal shutdown. For normal operation, the +5V converters require external heatsinks and forced-air cooling.

## **NTMX72AA** (continued)

### 12V pulse width modulation converter

The 12V PWM converter is an isolated, dual-output, common-ground, 30W, dc-to-dc converter. This converter can support an indefinite short circuit. The converter has an internal thermal shutdown, and a 100 KHz PWM switching frequency.

### Monitoring and protection circuits

The monitoring and protection circuits detect and protect outputs from undervoltage and overvoltage faults. The circuits are internal to the converter pack monitor. When a fault condition occurs, the circuit switches the K1 relay to OFF. This action causes the circuit breaker at the FSP to switch to OFF.

### Test and production monitoring connections

The following signals test and control internal circuits for factory use:

- 12V OV/UV CONT
- -12V OV/UV CONT
- 5V US.CONT
- EXT REL. CNTR
- TEST GND
- 12V ON/OFF
- 5V ON/OFF
- +5 MATE
- MATE FAIL
- 5V OV/CONT

### Frame supervisory panel connection

The following signals connect to the FSP for monitoring and signaling purposes:

- POWER, which trips the -48V circuit breaker in the FSP when ground is not available. Use the switch on the converter faceplate to operate the circuit breaker.
- HOLD, which trips the -48V circuit breaker in the FSP in failure conditions. The converter pack activates the line when the following events occur:
  - — an undervoltage condition is present on the +5V supply
  - — an undervoltage or overvoltage condition is present on the +12V supply or the -12V supply
  - — an overcurrent condition is present on one of the supplies
- RESET, which allows the circuit breaker to be set to the ON position when you seat the power converter again. Raise the switch on the faceplate to the reset position to activate the line.
- CONV. FAIL, which activates a visual alarm when the power converter is in the OFF condition

### Mate power detector

The mate converter has a +5V monitoring circuit that checks if the mate converter is in operation. The power detector sends output to the activity circuit and the processor pack.

### D-channel handler fuse and signaling

The DCH fuse and signaling circuit is an internal circuit that detects the condition of the faceplate-mounted fuse. This circuit protects the -48V output voltage from overcurrent conditions.

## Technical data

Overcurrent protection is available on each output to limit the maximum output current to a safe value.

An overvoltage and undervoltage protection circuit monitors every output and turns the converter off if an output voltage exceeds the preset level.

## **NTMX72AA** (continued)

# Signaling

### Pin numbers

The power supply card uses two standard 48-pin connectors to connect to the CPM backplane. The signals group globally as follows:

- battery power input pins
- power output pins
- FSP connection interface pins
- factory-used test pins

The pin numbers for connectors P1 and P2 on the appear in the following table.

**Connector P1 pin numbers**

| Pin number | Signal | Pin number | Signal | Pin number | Signal |
|---|---|---|---|---|---|
| 2Z | +5 | 2B | +5 | 2D | +5 |
| 4Z | +5 | 4B | +5 | 4D | +5 |
| 6Z | +5 | 6B | +5 | 6D | +5 |
| 8Z | +5 | 8B | +5 | 8D | +5 |
| 10Z | +5 | 10B | +5 | 10D | +5 |
| 12Z | +5 | 12B | +5 | 12D | +5 |
| 14Z | +5 | 14B | +5 | 14D | +5 |
| 16Z | – | 16B | – | 16D | – |
| 18Z | – | 18B | – | 18D | – |
| 20Z | GND | 20B | GND | 20D | GND |
| 22Z | GND | 22B | GND | 22D | GND |
| 24Z | GND | 24B | GND | 24D | GND |
| 26Z | GND | 26B | GND | 26D | GND |
| 28Z | GND | 28B | GND | 28D | GND |
| 30Z | GND | 30B | GND | 30D | GND |
| 32Z | GND | 32B | GND | 32D | GND |

**Connector P2 pin numbers**

| Pin number | Signal | Pin number | Signal | Pin number | Signal |
|---|---|---|---|---|---|
| 2Z | -48D | 2B | -48D | 2D | -48D |
| 4Z | – | 4B | DCH ALARM | 4D | -48VF1 |
| 6Z | -48V | 6B | -48V | 6D | -48V |
| 8Z | -48V | 8B | -48V | 8D | -48V |
| 10Z | 5 OV/UVCONT | 10B | – | 10D | 5V ON/OFF |
| 12Z | POWER | 12B | ABS-GND | 12D | HOLD |
| 14Z | – | 14B | – | 14D | RESET |
| 16Z | – | 16B | 12V ON/OFF | 16D | – |
| 18Z | MATE FAIL | 18B | – | 18D | +5 MATE |
| 20Z | DCH FAIL | 20B | – | 20D | – |
| 22Z | – | 22B | 12 OV/UV.CONT | 22D | +12 |
| 24Z | EXT REL CON | 24B | TEST (GND) | 24D | GND |
| 26Z | – | 26B | -12 OV/UV CONT | 26D | -12 |
| 28Z | LED. CONTR | 28B | -48VF2 | 28D | CONV FAIL |
| 30Z | BR | 30B | BR | 30D | BR |
| 32Z | BR | 32B | BR | 32D | BR |

## **NTMX72AA** (end)

### Power requirements

The power requirements of the NTMX72AA appear in the following table for two occurrences:

- normal operation. The NTMX72AA is loaded, and both converters operate
- completely loaded, but the mate converter fails

**Voltage and current for the NTMX72AA**

| | Maximum required current | |
|---|---|---|
| **Voltage (V)** | **Normal operation (A)** | **Mate converter failed (A)** |
| +5 | 24.00 | 29.00 |
| +12 | 0.12 | 0.24 |
| -12 | 0.30 | 0.60 |

# NTMX72AB

## Product description

The NTMX72AB power converter provides power for central processor and memory (CPM) digital switching equipment.

The NTMX72AB is a current circuit pack and is not backward compatible.

### Location

The NTMX72AB fits in the left and right slots of the CPM shelf. The board faceplate is two slots wide.

## Functional description

The NTMX72AB power converter provides a regulated power supply with three different output voltages referenced to a common ground.

The power converter receives voltage from the nominal -48V office battery.

The NTMX72AB has the following features:

- three voltage outputs: +5.15V, +12V, -12V
- messaging with the signaling processor
- automatic recovery from low battery (ARLB) circuit. This circuit senses the input voltage and signals the auxiliary power supply to shut down the converter. The power supply shuts down the converter when the input voltage falls below the minimum specified operating level. When the input voltage rises above the minimum startup level, the ARLB circuit enables the auxiliary supply.
- protection against overvoltage, undervoltage, overcurrent, and overtemperature
- a light-emitting diode (LED) maintenance status indicator on the faceplate
- a +5V monitoring circuit to check that the mate converter is in operation
- a D-channel handler (DCH) power fuse with trip signaling on the common frame supervisory panel (FSP) alarm lamp
- support for -48V and -60V input voltages

### Functional blocks

The NTMX72AB has the following functional blocks:

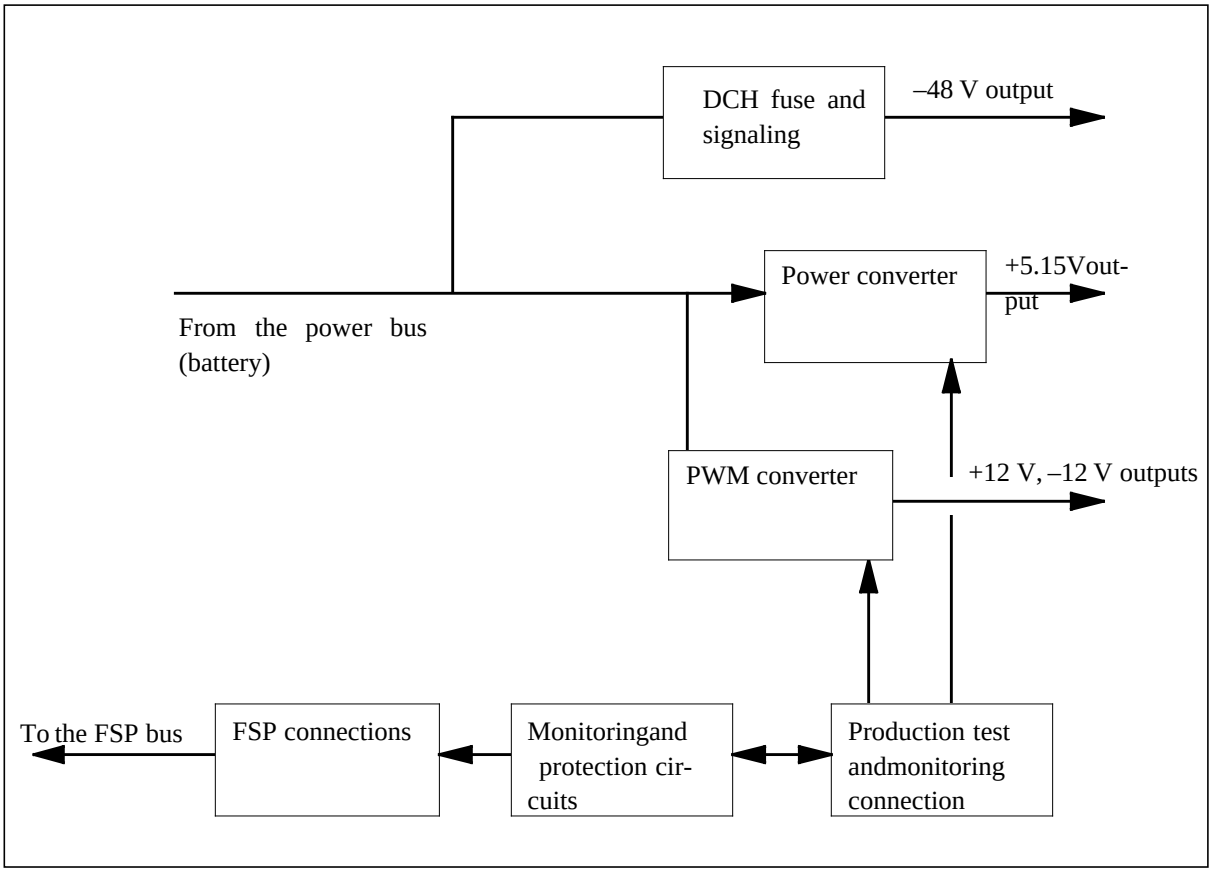
- 5.15V, 40A power converter
- 12V pulse width modulation (PWM) converter
- monitoring and protection circuits

## **NTMX72AB** (continued)

- test and production monitoring connections
- FSP connections
- mate power detector
- DCH fuse and signaling

The relationship between the functional blocks appears in the following figure.

**NTMX72AB functional blocks**




### 5.15V, 40A power converter

The 5.15V 40A power converter contains VI-200 series direct current-to-direct current (dc-to-dc) converters. Each of these converters handles a maximum of 100W. The VI-200 series is a family of zero-current-switching component-level dc-to-dc resonant converters. These converters have a maximum frequency of 2 MHz. The converters have an internal overvoltage, overcurrent protection, and thermal shutdown. For normal operation, the +5.15V converters need external heatsinks and forced-air cooling.

### 12V pulse width modulation converter

The 12V PWM converter is an isolated, dual-output, common-ground, 30W, dc-to-dc converter. This converter can support an indefinite short circuit. The converter has an internal thermal shutdown and a 100 KHz PWM switching frequency.

### Monitoring and protection circuits

The monitoring and protection circuits detect and protect the outputs from undervoltage and overvoltage faults. The circuits are internal to the converter pack monitor. When a fault condition occurs, the circuit switches the K1 relay to OFF. This action causes the circuit breaker at the FSP to switch to OFF.

### Test and production monitoring connections

The following signals test and control internal circuits for factory use:

- 12V OV/UV CONT
- -12V OV/UV CONT
- 5.15V US.CONT
- EXT REL. CNTR
- TEST GND
- 12V ON/OFF
- 5.15V ON/OFF
- +5.15 MATE
- MATE FAIL
- 5.15V OV/CONT

### Frame supervisory panel connection

The following signals connect to the FSP for monitoring and signaling purposes:

- POWER, which trips the -48V circuit breaker in the FSP when ground is not present. Use the switch on the converter faceplate to operate the circuit breaker manually.
- HOLD, which trips the -48V circuit breaker in the FSP in failure conditions. The converter pack activates the line when
  - — an undervoltage condition is present on the +5.15V supply
  - — an undervoltage or overvoltage condition is present on the +12V supply or the -12V supply
  - — an overcurrent condition is present on any of the supplies

## **NTMX72AB** (continued)

- RESET, which allows the circuit breaker to be set to the ON position when you seat the power converter again. Raise the switch on the faceplate to the reset position to activate the line.
- CONV. FAIL, which activates a visual alarm when the power converter is in the OFF condition

### Mate power detector

The mate converter has a +5.15V monitoring circuit that checks if the mate converter is in operation. The power detector sends output to the activity circuit and the processor pack.

### D-channel handler fuse and signaling

The DCH fuse and signaling circuit is an internal circuit that detects the condition of the faceplate-mounted fuse. This circuit protects the -48V output voltage from overcurrent conditions.

## Technical data

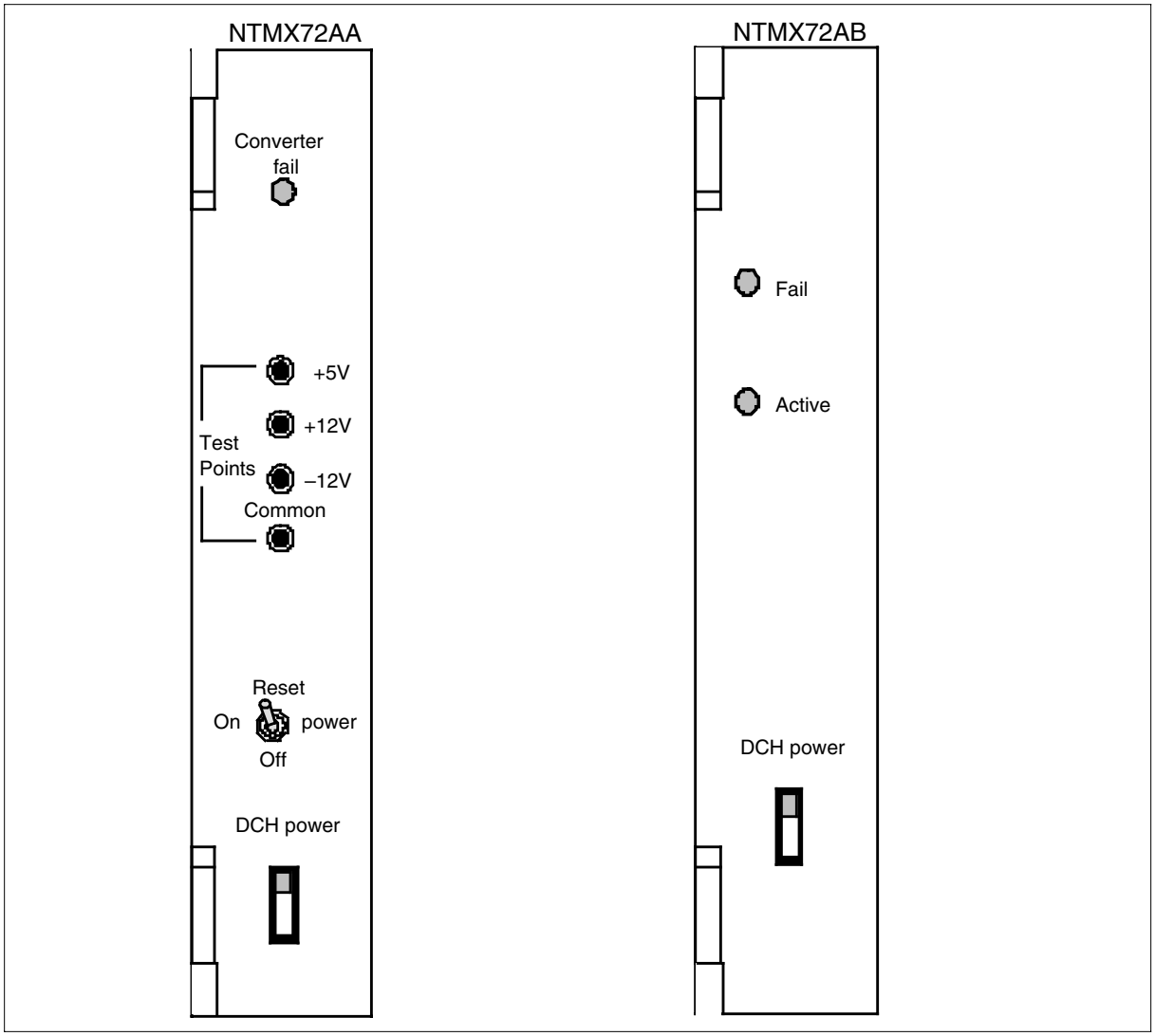
Overcurrent protection is available on the outputs to limit the maximum output current to a safe value.

An overvoltage and undervoltage protection circuit monitors the outputs. The circuit turns the converter of if an output voltage exceeds the preset level.

### Circuit card status indicators

The status indicators for the NTMX72AA and AB appear in the following figure.

**Circuit cards with status indicators**




The indicators on the circuit cards in the previous figure appear in the following table. The table describes the function of the indicators.

**System status indicators**

| Indicator name | Circuit card | LED color | Function |
|---|---|---|---|
| Active | NTMX72AB | Green | Indicates the converter is functional |
| Fail | NTMX72AB | Red | The converter fails (+5, +12 V or -12 V) |

## NTMX72AB (continued)

# Signaling

### Pin numbers

The power supply card uses two standard 48-pin connectors to connect to the CPM backplane. The signals group globally as follows:

- battery power input pins
- power output pins
- FSP connection interface pins
- factory-used test pins

The pin numbers for connectors P1 and P2 on the NTMX72AB appear in the following table.

**Connector P1 pin numbers**

| Pin number | Signal | Pin number | Signal | Pin number | Signal |
|---|---|---|---|---|---|
| 2Z | +5.15 | 2B | +5.15 | 2D | +5.15 |
| 4Z | +5.15 | 4B | +5.15 | 4D | +5.15 |
| 6Z | +5.15 | 6B | +5.15 | 6D | +5.15 |
| 8Z | +5.15 | 8B | +5.15 | 8D | +5.15 |
| 10Z | +5.15 | 10B | +5.15 | 10D | +5.15 |
| 12Z | +5.15 | 12B | +5.15 | 12D | +5.15 |
| 14Z | +5.15 | 14B | +5.15 | 14D | +5.15 |
| 16Z | – | 16B | – | 16D | – |
| 18Z | – | 18B | – | 18D | – |
| 20Z | LRTN | 20B | LRTN | 20D | LRTN |
| 22Z | LRTN | 22B | LRTN | 22D | LRTN |
| 24Z | LRTN | 24B | LRTN | 24D | LRTN |
| 26Z | LRTN | 26B | LRTN | 26D | LRTN |
| 28Z | LRTN | 28B | LRTN | 28D | LRTN |
| 30Z | LRTN | 30B | LRTN | 30D | LRTN |
| 32Z | LRTN | 32B | LRTN | 32D | LRTN |

**Connector P2 pin numbers**

| Pin number | Signal | Pin number | Signal | Pin number | Signal |
|---|---|---|---|---|---|
| 2Z | -BATTD | 2B | -BATTD | 2D | -BATTD |
| 4Z | – | 4B | DCH ALARM | 4D | -48VF1 |
| 6Z | L- | 6B | L- | 6D | L- |
| 8Z | L- | 8B | L- | 8D | L- |
| 10Z | 5.15V TEST | 10B | – | 10D | 5V ON/OFF |
| 12Z | POWER | 12B | ABS-RTN | 12D | HOLD |
| 14Z | – | 14B | – | 14D | RESET |
| 16Z | – | 16B | 12V ON/OFF | 16D | – |
| 18Z | MATE FAIL | 18B | – | 18D | +5 MATE |
| 20Z | DCH FAIL | 20B | – | 20D | – |
| 22Z | – | 22B | +12V TEST OV/UV.CONT | 22D | +12V |
| 24Z | EXT REL CONTR | 24B | TEST (LRTN) | 24D | LRTN |
| 26Z | – | 26B | -12V TEST | 26D | -12V |
| 28Z | LED. CONTR | 28B | -48VF2 | 28D | CONV FAIL |
| 30Z | L+ | 30B | L+ | 30D | L+ |
| 32Z | L+ | 32B | L+ | 32D | L+ |

# NTMX73AA

## Product description

The NTMX73AA pulse code modulation (PCM) signaling pack controls all low–level PCM and DS–1 signaling tasks. This signaling pack generates the system clock. The PCM and DS–1 signaling tasks include the following:

- link maintenance
- reception and transmission of derived data link (DDL)
- reception and transmission of ABCD bits

The NTMX73AA supports DS–1 and PCM30 trunks on the core side (C–side) and the peripheral side (P–side). This pack replaces the 6X28, 6X41, 6X44, and 6X86 packs, in part or completely.

## Functional description

The NTMX73AA signaling pack supports the following:

- signaling bits hardware interface
- maintenance bytes hardware interface
- clock generation and distribution

For the DS–1, the NTMX73AA perform the following functions:

- assembly and transfer of ABCD bits to and from the microprocessor
- pre–processing of the maintenance status
- setting of the maintenance control byte
- all DDL functions that the NT6X86 performed before

For the PCM30, the NTMX73AA performs the following functions:

- assembly and transfer of ABCD bits to and from the microprocessor
- setting of the maintenance control byte

### Functional blocks

The NTMX73AA has the following functional blocks:

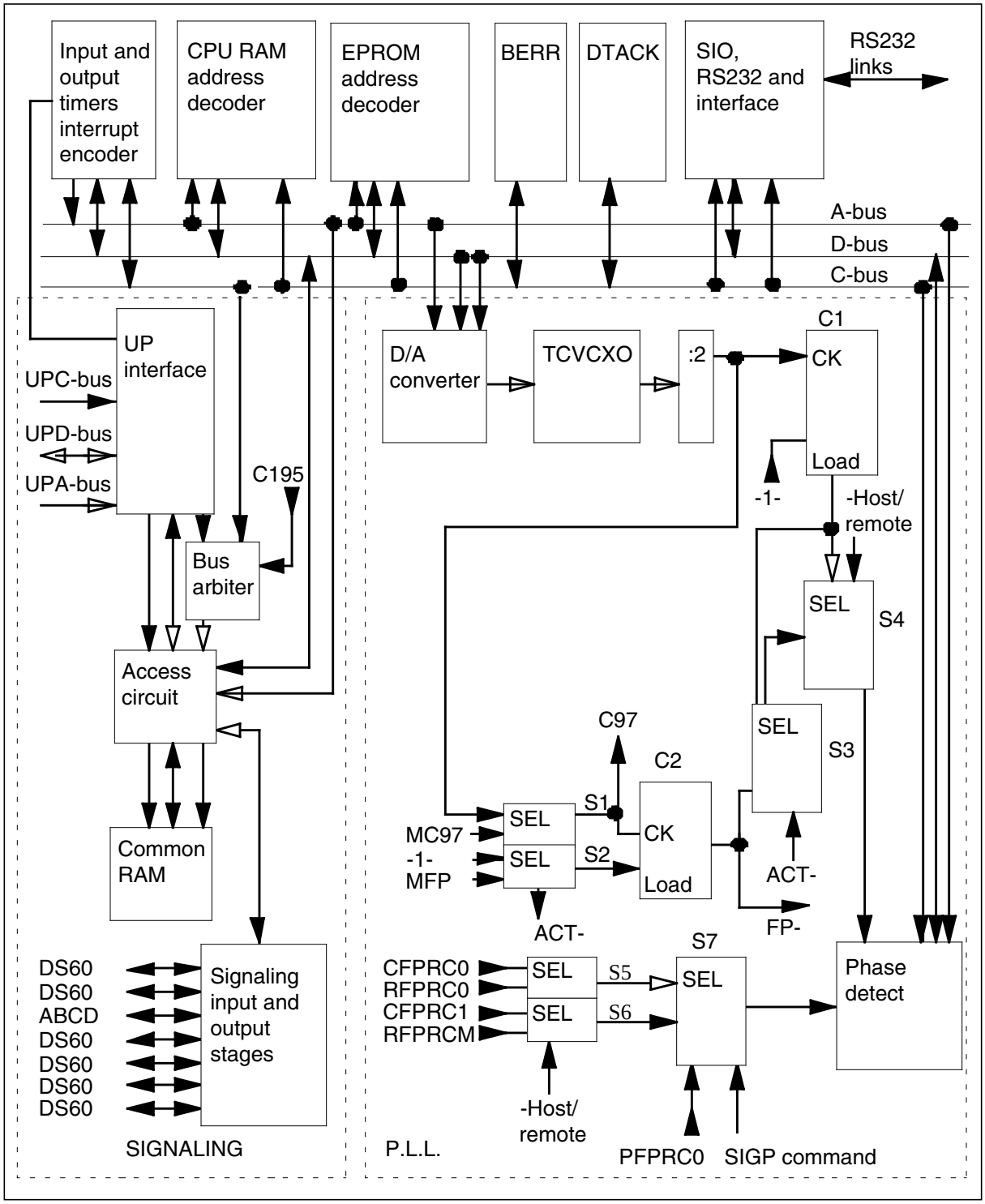
- central processing unit (CPU) 68000
- the CPU clock
- reset
- timers
- time–out logic

- watchdog
- erasable programmable read–only memory (EPROM) and CPU random–access memory (RAM)
- input/output (I/O) port
- common RAM
- serial input/output (SIO)
- phase–locked loop (PLL) and clock distribution
- interrupts arbiter

The following diagram shows the relationship between the functional blocks.

## **NTMX73AA** (continued)

**The NTMX73AA functional blocks**



### CPU 68000

The CPU has the following important features:

- a 16 bit data bus
- a 23 bit address bus
- eight data registers
- eight address registers

### CPU clock

A 25 MHz oscillator and a divide–by–2 circuit generates the 12.5 MHz clock.

### Reset

The NTMX73AA resets when the system powers up, or the unified processor (UP) (NTMX77AA) resets a single card or a complete shelf.

### Timers

The NTMX73AA has two on–board timers. One timer functions as a phase comparator for the clock generation function. The second timer provides a real–time clock for the CPU, and two separate Baud rates for serial input/output.

### Time–out logic

To control termination of a bus cycle, the bus error circuit asserts the BERR input of the 68000. The circuit asserts the BERR input when the addressed device does not assert the DTACK input in 51 ms.

### Watchdog

The UP performs the watchdog function. The UP performs checks if the signaling processor (SIGP) writes the correct information to the common RAM. The UP performs these checks at fixed intervals. The UP can reset the SIGP if the SIGP does not function correctly.

### EPROM and CPU RAM

The CPU uses a 64 Kword EPROM and 128 Kwords of RAM.

### Input/output port

The CPU has one 16 bit general purpose I/O port for signaling, and clock–function supervision and control.

### Common RAM

This fast access RAM is an I/O buffer for the signaling data. This RAM is a communication medium between the UP and the SIGP. The UP, the SIGP, and

## **NTMX73AA** (continued)

the on–board hardware share access to this memory. Each of these users has a data write buffer, a data read latch, and an address buffer.

### Serial input/output

The SIO implements two links. One link is between the main and mate PCM signaling packs. A second link is from the pack to the debug monitor.

### Phase–locked loop and clock distribution

This circuit provides the general system clock, frame pulse (FP), and FP48 for the CPM shelf.

Software controls the PLL. The CPU updates the PLL. The SIGP chooses the reference input for clock generation.

### Interrupts arbiter

Four levels of interrupts are present with fixed priority. Each interrupt can be separately masked. The interrupt levels are as follows:

- 2/3MSINT—2/3 ms interrupt
- UARTINT—UART interrupt
- CLKINT—real time clock interrupt
- PTYINT—parity interrupt

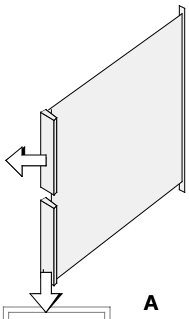
## Signaling

### Pin numbers

The pin number diagram for the NTMX73AA appears in the following diagram.

# **NTMX73AA** (continued)

### NTMX73AA pin numbers



| | | A | B |
|---|---|---|---|
| 1A | 1B | GND | GND |
| 2A | 2B | +5V | +5V |
| 3A | 3B | +5V | +5V |
| 4A | 4B | +5V | +5V |
| 5A | 5B | GND | GND |
| 6A | 6B | FP-/o | C97+/o |
| 7A | 7B | GND | C97C+/o |
| 8A | 8B | ACT-/i | C97A+/o |
| 9A | 9B | | C97B+/o |
| 10A | 10B | C97MA+/o | C97M+/o |
| 11A | 11B | GND | C97D+/o |
| 12A | 12B | DAS-/i | FPA-/o |
| 13A | 13B | LDS-/i | FPB-/o |
| 14A | 14B | DSACK1-/o | FPM-/o |
| 15A | 15B | UDS-/i | FPMA-/o |
| 16A | 16B | R/-W/i | INFPM- |
| 17A | 17B | | OUTFPM- |
| 18A | 18B | RSTIN-/i | 2/3MSINT-/o |
| 19A | 19B | CKFAIL/o | C324c/o |
| 20A | 20B | C324/o | C324M/o |
| 21A | 21B | C324A/o | C324MA/o |
| 22A | 22B | C324B/o | GND |
| 23A | 23B | INC97M+ | OUTC97M+ |
| 24A | 24B | INF720- | OUTF720- |
| 25A | 25B | FP48-/o | FP48M-/o |
| 26A | 26B | FP48A-/o | FP48MA-/o |
| 27A | 27B | RMC-/i | FP48C-/o |
| 28A | 28B | GND | FP48B-/o |
| 29A | 29B | ADD1 | CH01T-/o |
| 30A | 30B | ADD2 | CH01M-/o |
| 31A | 31B | ADD3 | HDICLK/i |
| 32A | 32B | ADD4 | HDOCLK/o |
| 33A | 33B | ADD5 | |
| 34A | 34B | GNDHDOUT/o | |
| 35A | 35B | ADD6 | HDIN/i |
| 36A | 36B | ADD7 | GND |
| 37A | 37B | ADD8 | |
| 38A | 38B | ADD9 | TDOUT/o |
| 39A | 39B | ADD10 | TDIN/i |
| 40A | 40B | ADD11 | GND |

| | | A | B |
|---|---|---|---|
| 41A | 41B | GND | GND |
| 42A | 42B | ADD12 | SIGDSO74/i |
| 43A | 43B | ADD13 | SIGDSO74/o |
| 44A | 44B | ADD14 | SIGDSO76/i |
| 45A | 45B | ADD15 | SIGSO76i |
| 46A | 46B | ADD16 | |
| 47A | 47B | ADD17 | SIGCONT0/i |
| 48A | 48B | ADD18 | SIGCONT1/i |
| 49A | 49B | ADD19 | SIGCONT2/i |
| 50A | 50B | ADD20 | SIGCONT3/i |
| 51A | 51B | ADD21 | |
| 52A | 52B | ABIN0/o | ABOUT0/i |
| 53A | 53B | ABIN1/o | ABOUT1/i |
| 54A | 54B | ABIN2/o | ABOUT2/i |
| 55A | 55B | ABIN3/o | ABOUT3/i |
| 56A | 56B | MACT- | |
| 57A | 57B | GND | GND |
| 58A | 58B | DATA0 | C97MB/o |
| 59A | 59B | DATA1 | C97E+/o |
| 60A | 60B | DATA2 | FPMB-/o |
| 61A | 61B | DATA3 | FPC-/o |
| 62A | 62B | DATA4 | FPD-/o |
| 63A | 63B | DATA5 | FPE-/o |
| 64A | 64B | GND | |
| 65A | 65B | DATA6 | |
| 66A | 66B | DATA7 | |
| 67A | 67B | DATA8 | CFPRC1/i |
| 68A | 68B | DATA9 | CFPRC0/i |
| 69A | 69B | DATA10 | -HOST/REM |
| 70A | 70B | DATA11 | RFPRCM/i |
| 71A | 71B | DATA12 | RFPRCO/i |
| 72A | 72B | DATA13 | |
| 73A | 73B | DATA14 | |
| 74A | 74B | DATA15 | PFPRC1/i |
| 75A | 75B | SWACK+/o | PFPRC0/i |
| 76A | 76B | GND | GND |
| 77A | 77B | +12V | +12V |
| 78A | 78B | GND | GND |
| 79A | 79B | -12V | -12V |
| 80A | 80B | GND | GND |

## **NTMX73AA** (end)

# Technical data

### Power requirements

The following table lists the power requirements of the NTMX73AA.

**Power requirements of the NTMX73AA**

| Voltage (Volt) | Current (Ampere) |
|---|---|
| 5 | 1.90 |
| +12 | 0.06 |
| –12 | 0.04 |
| –48 | – |

## Product description

The NTMX74AA interface pack is an interface between the common peripheral module (CPM) matrix and the following three modules:

- the line concentrating module (LCM)
- the enhanced integrated services digital network (ISDN) LCM (LCME)
- the remote maintenance module (RMM)

This pack follows the NT6X48 pack design, except this pack has 32 ports instead of 10.

## Functional description

The NTMX74AA performs two main functions. One function is to convert data that comes from the matrix in DS60 format to balanced DS30A format for the LCM. The other main function is to convert balanced DS30A signals from the LCM to DS60 format for the matrix.

### Functional blocks

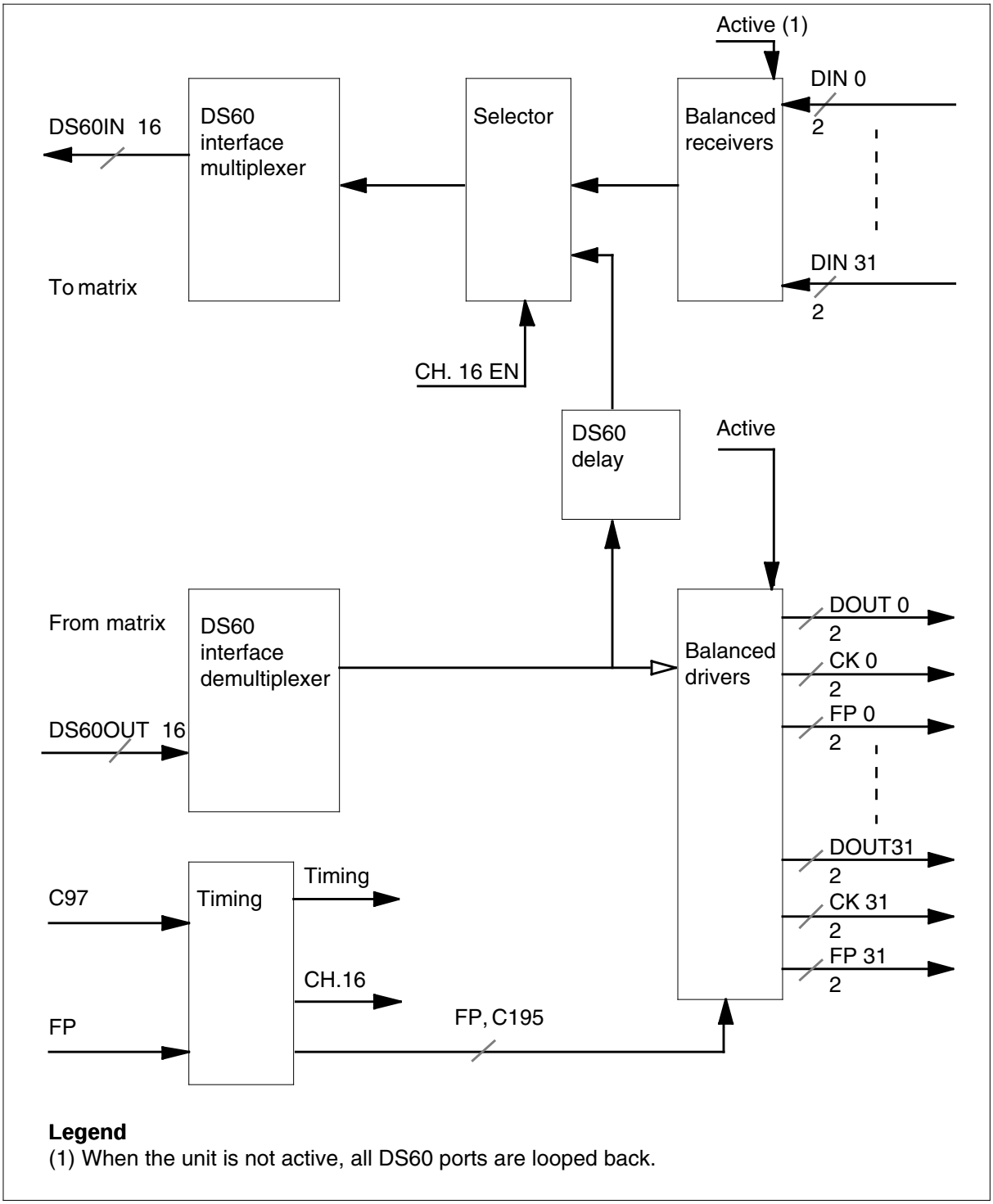
The NTMX74AA has the following functional blocks:

- input port multiplexing
- output port demultiplexing
- differential drivers
- differential receivers
- channel 16 looparound
- clock generation

The following diagram shows the functional relationship between the blocks.

## **NTMX74AA** (continued)

**NTMX74AA functional blocks**




**Legend**
(1) When the unit is not active, all DS60 ports are looped back.

### Input port multiplexing

Input port multiplexing multiplexes and transmits the DS60IN data from the LCM to the matrix. Ports next to each other are multiplexed together. These ports are 0–1, 2–3, 4–5.

### Output port demultiplexing

The output port demultiplexing block demultiplexes the DS60OUT data from the matrix.

### Differential drivers

The differential drivers transmit DOUT, C195 clock, and frame pulse (FP) data to each DS30A port of the LCM. Transmission requires the use of three of the drivers in each device. To improve the reliability and to reduce heat expansion, the process does not use the fourth driver in the package.

### Differential receivers

The differential receivers are balanced receivers that accept the DIN differential data from the LCM. These receivers produce a transistor–transistor logic output.

### Channel 16 loop–around

The channel 16 data from the matrix loops back to the matrix. A delay of the DS60OUT data results from a delay of the DS60IN data. The DS60IN data delay is approximately four time slots. The DS60OUT data transmits back to the input. The input port multiplexing inserts channel 16 in the PCM data that goes to the matrix.

### Clock generation

The timing circuit divides the shelf clock (C97) in C195 and C390 clocks. These clocks are synchronized to have a positive transition in the center of the shelf frame pulse.

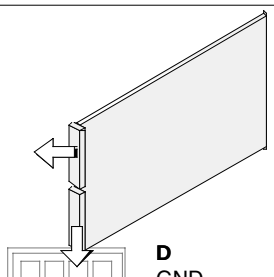
## Signaling

### Pin numbers

The pin numbers for the NTMX74AA appear in the following figure.

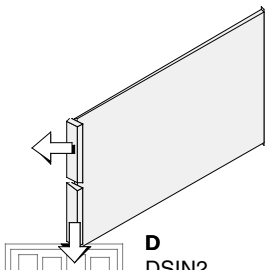
# **NTMX74AA** (continued)

### NTMX74AA pin numbers (Part 1 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 1 | GND | GND | GND | GND |
| 2 | +5V | +5V | +5V | +5V |
| 3 | +5V | +5V | +5V | +5V |
| 4 | +5V | +5V | +5V | +5V |
| 5 | GND | GND | GND | GND |
| 6 | | | C97+ | FP- |
| 7 | GND | GND | GND | GND |
| 8 | | | | ACT- |
| 9 | PCLK-2 | PCLK+2 | PCLK-0 | PCLK+0 |
| 10 | PFP-2 | PFP+2 | PFP-0 | PFP+0 |
| 11 | RPCM-2 | RPCM+2 | RPCM-0 | RPCM+0 |
| 12 | XPCM-2 | XPCM+2 | XPCM-0 | XPCM+0 |
| 13 | PCLK-3 | PCLK+3 | PCLK-1 | PCLK+1 |
| 14 | PFP-3 | PFP+3 | PFP-1 | PFP+1 |
| 15 | RPCM-3 | RPCM+3 | RPCM-1 | RPCM+1 |
| 16 | XPCM-3 | XPCM+3 | XPCM-1 | XPCM+1 |
| 17 | PCLK-6 | PCLK+6 | PCLK-4 | PCLK+4 |
| 18 | PFP-6 | PFP+6 | PFP-4 | PFP+4 |
| 19 | RPCM-6 | RPCM+6 | RPCM-4 | RPCM+4 |
| 20 | XPCM-6 | XPCM+6 | XPCM-4 | XPCM+4 |
| 21 | PCLK-7 | PCLK+7 | PCLK-5 | PCLK+5 |
| 22 | PFP-7 | PFP+7 | PFP-5 | PFP+5 |
| 23 | RPCM-7 | RPCM+7 | RPCM-5 | RPCM+5 |
| 24 | XPCM-7 | XPCM+7 | XPCM-5 | XPCM+5 |
| 25 | PCLK-10 | PCLK+10 | PCLK-8 | PCLK+8 |
| 26 | PFP-10 | PFP+10 | PFP-8 | PFP+8 |
| 27 | RPCM-10 | RPCM+10 | RPCM-8 | RPCM+8 |
| 28 | XPCM-10 | XPCM+10 | XPCM-8 | XPCM+8 |
| 29 | PCLK-11 | PCLK+11 | PCLK-9 | PCLK+9 |
| 30 | PFP-11 | PFP+11 | PFP-9 | PFP+9 |
| 31 | RPCM-11 | RPCM+11 | RPCM-9 | RPCM+9 |
| 32 | XPCM-11 | XPCM+11 | XPCM-9 | XPCM+9 |
| 33 | PCLK-14 | PCLK+14 | PCLK-12 | PCLK+12 |
| 34 | PFP-14 | PFP+14 | PFP-12 | PFP+12 |
| 35 | RPCM-14 | RPCM+14 | RPCM-12 | RPCM+12 |
| 36 | XPCM-14 | XPCM+14 | XPCM-12 | XPCM+12 |
| 37 | PCLK-15 | PCLK+15 | PCLK-13 | PCLK+13 |
| 38 | PFP-15 | PFP+15 | PFP-13 | PFP+13 |
| 39 | RPCM-15 | RPCM+15 | RPCM-13 | RPCM+13 |
| 40 | XPCM-15 | XPCM+15 | XPCM-13 | XPCM+13 |
| 41 | GND | GND | GND | GND |
| 42 | DSOUT6 | DSOUT4 | DSOUT2 | DSOUT0 |
| 43 | DSOUT14 | DSOUT12 | DSOUT10 | DSOUT8 |
| 44 | DSOUT22 | DSOUT20 | DSOUT18 | DSOUT16 |
| 45 | DSOUT30 | DSOUT28 | DSOUT26 | DSOUT24 |

**NTMX74AA pin numbers (Part 2 of 2 )**



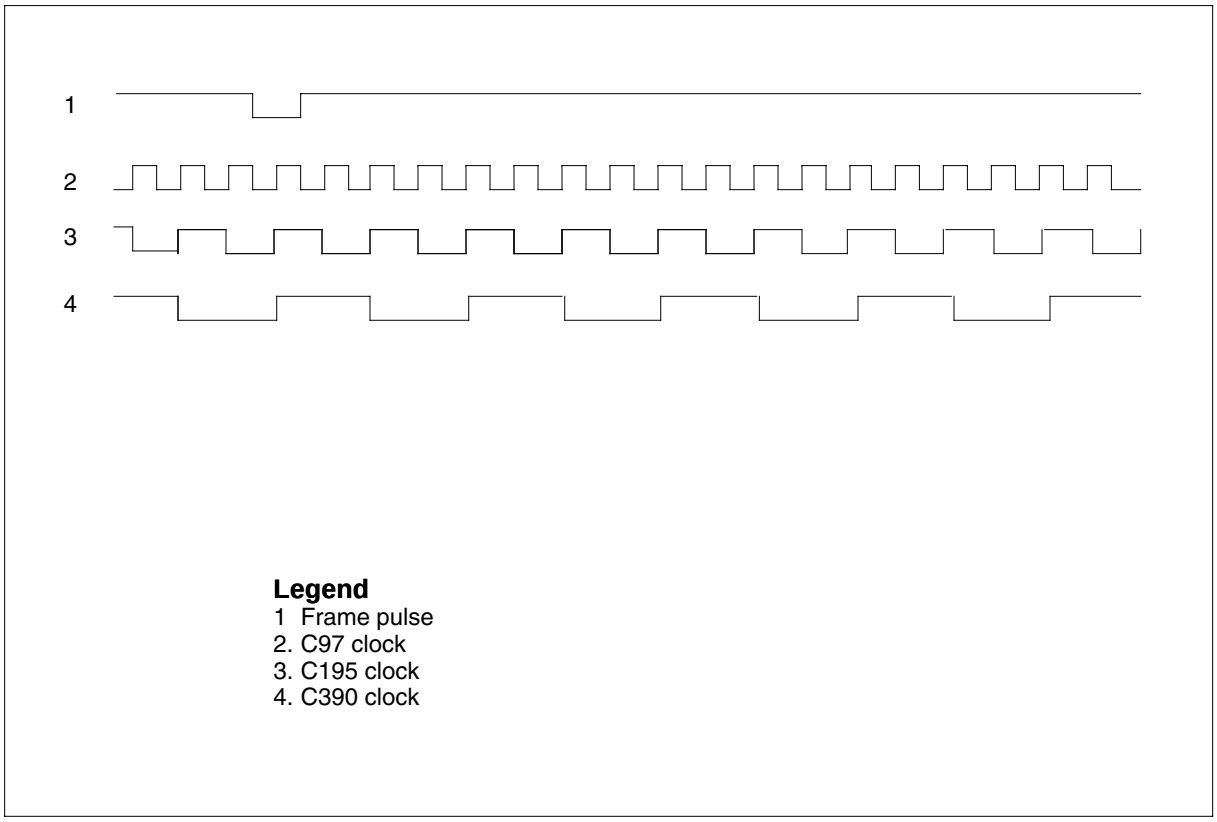
| | D | C | B | A |
|---|---|---|---|---|
| 46 | DSIN2 | DSIN0 | GND | GND |
| 47 | DSIN6 | DSIN4 | GND | GND |
| 48 | DSIN10 | DSIN8 | | |
| 49 | DSIN14 | DSIN12 | | |
| 50 | DSIN18 | DSIN16 | | |
| 51 | DSIN22 | DSIN20 | | |
| 52 | DSIN26 | DSIN24 | GND | GND |
| 53 | DSIN30 | DSIN28 | GND | GND |
| 54 | PCLK-18 | PCLK+18 | PCLK-16 | PCLK+16 |
| 55 | PFP-18 | PFP+18 | PFP-16 | PFP+16 |
| 56 | RPCM-18 | RPCM+18 | RPCM-16 | RPCM+16 |
| 57 | XPCM-18 | XPCM+18 | XPCM-16 | XPCM+16 |
| 58 | PCLK-19 | PCLK+19 | PCLK-17 | PCLK+17 |
| 59 | PFP-19 | PFP+19 | PFP-17 | PFP+17 |
| 60 | RPCM-19 | RPCM+19 | RPCM-17 | RPCM+17 |
| 61 | XPCM-19 | XPCM+19 | XPCM-17 | XPCM+17 |
| 62 | PCLK-22 | PCLK+22 | PCLK-20 | PCLK+20 |
| 63 | PFP-22 | PFP+22 | PFP-20 | PFP+20 |
| 64 | RPCM-22 | RPCM+22 | RPCM-20 | RPCM+20 |
| 65 | XPCM-22 | XPCM+22 | XPCM-20 | XPCM+20 |
| 66 | PCLK-23 | PCLK+23 | PCLK-21 | PCLK+21 |
| 67 | PFP-23 | PFP+23 | PFP-21 | PFP+21 |
| 68 | RPCM-23 | RPCM+23 | RPCM-21 | RPCM+21 |
| 69 | XPCM-23 | XPCM+23 | XPCM-21 | XPCM+21 |
| 70 | PCLK-26 | PCLK+26 | PCLK-24 | PCLK+24 |
| 71 | PFP-26 | PFP+26 | PFP-24 | PFP+24 |
| 72 | RPCM-26 | RPCM+26 | RPCM-24 | RPCM+24 |
| 73 | XPCM-26 | XPCM+26 | XPCM-24 | XPCM+24 |
| 74 | PCLK-27 | PCLK+27 | PCLK-25 | PCLK+25 |
| 75 | PFP-27 | PFP+27 | PFP-25 | PFP+25 |
| 76 | RPCM-27 | RPCM+27 | RPCM-25 | RPCM+25 |
| 77 | XPCM-27 | XPCM+27 | XPCM-25 | XPCM+25 |
| 78 | PCLK-30 | PCLK+30 | PCLK-28 | PCLK+28 |
| 79 | PFP-30 | PFP+30 | PFP-28 | PFP+28 |
| 80 | RPCM-30 | RPCM+30 | RPCM-28 | RPCM+28 |
| 81 | XPCM-30 | XPCM+30 | XPCM-28 | XPCM+28 |
| 82 | PCLK-31 | PCLK+31 | PCLK-29 | PCLK+29 |
| 83 | PFP-31 | PFP+31 | PFP-29 | PFP+29 |
| 84 | RPCM-31 | RPCM+31 | RPCM-29 | RPCM+29 |
| 85 | XPCM-31 | XPCM+31 | XPCM-29 | XPCM+29 |
| 86 | GND | GND | GND | GND |
| 87 | +12V | +12V | +12V | +12V |
| 88 | GND | GND | GND | GND |
| 89 | -12V | -12V | -12V | -12V |
| 90 | GND | GND | GND | GND |

## **NTMX74AA** (end)

### Timing

The timing for the NTMX74AA appears in the following figure.

**NTMX74AA timing**



## Product description

The NTMX75AA time switch or matrix circuit pack performs every speech channel switching function for the common peripheral module (CPM) family of peripheral shelves. The NTMX75AA is a pack that performs more than one function. This pack is in a remote cluster controller 2 (RCC2) shelf of a cabinetized remote switching center (CRSC). The pack has direct access to the following:

- the NTMX77AA unified processor (UP) card
- the DS–1 cards
- the DS30 cards
- the signaling card
- the parallel bus

The NTMX75AA time switch circuit pack has the following features:

- time switching of input channels to output channels
- plane selection for time slots for the central side (C–side)
- the DS60 highway–select multiplexers (MUX) allow the selection of one 32–channel link out of the DS60
- conversion from parallel to a serial format and serial to a parallel format for the application–specific integrated circuit (ASIC)
- a DS–1 A–bit and B–bit two–way transmission interface to the DS–1 packlet, with optional extended frame capability
- programmable digital speech conversion for each channel
- parity checks and tests for incoming C–side data
- a parity generator for outgoing C–side data
- an interface to the parallel speech bus on the input and output of the matrix
- a new interface to the CSM function
- an interface to the C–side and peripheral side (P–side) physical interface packs
- an interface to the signaling processor (SIGP) pack
- a C–bit control to select pack locations in the P–side, as speech sources for the matrix
- an interface to the UP pack
- a global loopback from the output to the input for maintenance

## **NTMX75AA** (continued)

The NTMX75AA circuit pack is not backward compatible.

### Location

The NTMX75AA circuit pack fits slots 10 or 18 of an RCC2 shelf of a CRSC.

## Functional description

The NTMX75AA performs every speech channel switching function for the RCC2 shelf. The NTMX75AA performs the following functions:

- digital connections between all C– and P–side channels
- movement of ABCD bits from the DS1 ports to the SIGP pack
- support of the parallel buses for service circuits
- selection of C–side input and output links and channels
- selection of P–side link connections

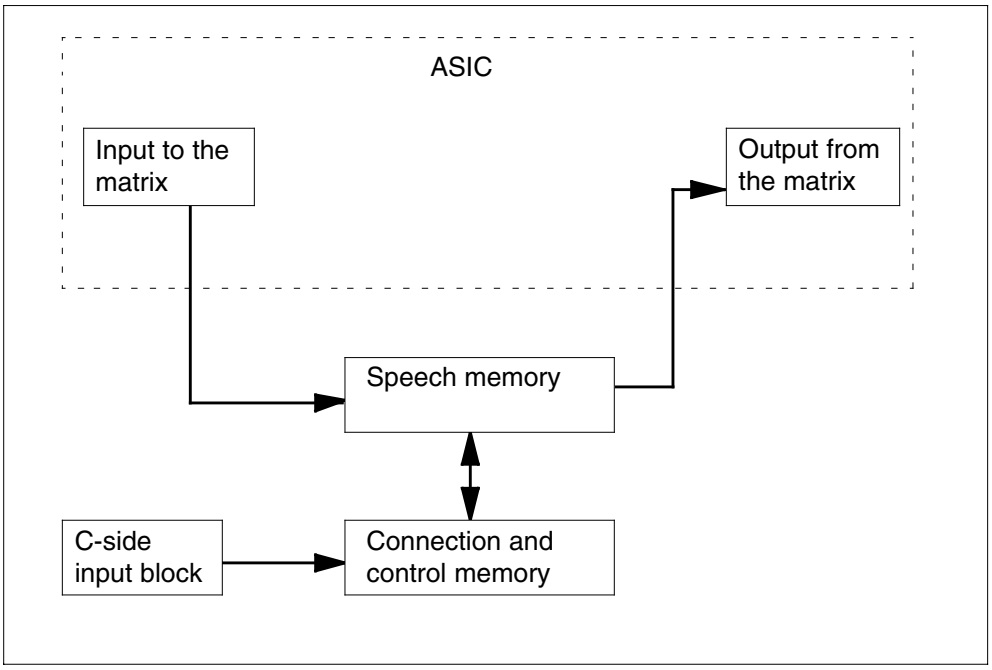
### Functional blocks

The NTMX75AA has the following functional blocks:

- input to the matrix
- output from the matrix
- speech memory
- connection memory
- control memory
- C–side input block
- dual formatter ASIC

The following diagram shows the relationship between the functional blocks.

**The NTMX75AA functional blocks**




### Input to the matrix

Four groups of 10 lines are present at the input side of the matrix. Each line is DS60 (64CH). A total of 2560 channels is at the input side. Each input channel can connect to any output channel.

### Output from the matrix

Four groups of 10 lines are present at the output side of the matrix. Each line is DS60 (64CH), except the last line. The last line has 32 channels for output and 32 channels for the UP to access. Only 2528 channels are present at the output side. Each output channel can connect to any input channel.

### Speech memory

The speech memory converts input data streams from serial to a parallel format, and writes the data to the random–access memory (RAM). The UP can read the speech memory. The hardware can write to and read from the speech memory.

### Connection memory

The connection memory is the switching memory. The hardware can read this memory. The UP can write to and read from the connection memory.

## **NTMX75AA** (continued)

### Control memory

The control memory contains special functions for each channel. The hardware can read this memory. The UP can write to and read from the control memory.

### Core–side input block

This block selects from the two possible inputs, and converts data from serial to a parallel format.

### Dual formatter ASIC

The dual formatter ASIC integrates functions of some ICs in one device that has the following functions:

- on the input section
  - — serial–to–parallel conversion
- on the output section
  - — parallel–to–serial conversion
  - — programmable delay
  - — loopback from 10 outputs to 10 inputs

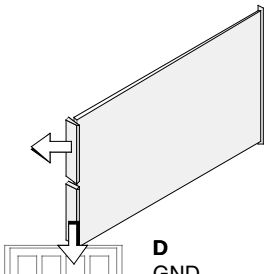
## Signaling

Some signals are sent or received differentially. The pin number diagram shows the signals to be negative and positive.

### Pin number

The pin numbers for the NTMX75AA appear in the following figures.

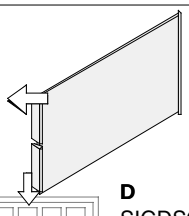
**NTMX75AA pin numbers (Part 1 of 2 )**



| | D | C | B | A |
|---|---|---|---|---|
| 1 | GND | GND | GND | GND |
| 2 | +5V | +5V | +5V | +5V |
| 3 | +5V | +5V | +5V | +5V |
| 4 | +5V | +5V | +5V | +5V |
| 5 | GND | GND | GND | GND |
| 6 | EXDSO78- | EXDSO78+ | C97IN | -FPIN |
| 7 | EXC97- | EXC97+ | GND | GND |
| 8 | EXACT- | EXACT+ | DSOUT42 | ACT- |
| 9 | EXC122- | EXC122+ | DSOUT44 | -DS1P |
| 10 | EXDCHRST- | EXDCHRST+ | DSOUT46 | C122/i |
| 11 | EXDSO30- | EXDSO30+ | DSOUT48 | -FIBACTP |
| 12 | EXDSI30- | EXDSI30+ | DSOUT50 | DAS- |
| 13 | SPARE | SPARE | DSOUT52 | LDS- |
| 14 | EXDSO32- | EXDSO32+ | DSOUT54 | DSACK1- |
| 15 | EXDSI32- | EXDSI32+ | DSOUT56 | UDS- |
| 16 | EXDSO34- | EXDSO34+ | DSOUT58 | R/-W |
| 17 | EXDSI34- | EXDSI34+ | DSOUT60 | C324/i |
| 18 | EXDSO38- | EXDSO38+ | DSOUT62 | DCHRST-/i |
| 19 | EXDSI38- | EXDSI38+ | DSOUT64 | PARITY |
| 20 | EXDSO40- | EXDSO40+ | DSOUT66 | CSMIN |
| 21 | EXDSI40- | EXDSI40+ | DSOUT68 | CSMOUT |
| 22 | EXDSO44- | EXDSO44+ | DSOUT70 | -U0/U1 |
| 23 | EXDSI44- | EXDSI44+ | DSOUT72 | -HOST/REM |
| 24 | EXDSO46- | EXDSO46+ | POUT0 | PIN0 |
| 25 | EXDSI46- | EXDSI46+ | POUT1 | PIN1 |
| 26 | EXDSO48- | EXDSO48+ | POUT2 | PIN2 |
| 27 | EXDSI48- | EXDSI48+ | POUT3 | PIN3 |
| 28 | EXDSO50- | EXDSO50+ | POUT4 | PIN4 |
| 29 | EXDSI50- | EXDSI50+ | POUT5 | PIN5 |
| 30 | EXDSI78- | EXDSI78+ | POUT6 | PIN6 |
| 31 | EXDS48- | EXFP48+ | POUT7 | PIN7 |
| 32 | EXDSO52- | EXDSO52+ | GND | GND |
| 33 | EXDSI52- | EXDSI52+ | T1IN36 | ADD1 |
| 34 | EXDSO54- | EXDSO54+ | T1IN38 | ADD2 |
| 35 | EXDSI54- | EXDSI54+ | T1IN40 | ADD3 |
| 36 | EXDSO56- | EXDSO56+ | T1IN42 | ADD4 |
| 37 | EXDSI56- | EXDSI56+ | -DS1C | ADD5 |
| 38 | T1IN20 | T1IN20M | -FIBACTC | ADD6 |
| 39 | T1IN22 | T1IN22M | SVBIT | ADD7 |
| 40 | T1IN24 | T1IN24M | | ADD8 |
| 41 | T1IN26 | T1IN26M | | ADD9 |
| 42 | T1IN28 | T1IN28M | | ADD10 |
| 43 | T1IN30 | T1IN30M | | ADD11 |
| 44 | T1IN32 | T1IN32M | | ADD12 |
| 45 | T1IN34 | T1IN34M | | ADD13 |

# **NTMX75AA** (end)

### NTMX75AA pin numbers (Part 2 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 46 | SIGDSO74 | SIGDSI74 | NMLPCNT | ADD14 |
| 47 | SIGDSO76 | SIGDSI76 | NMLPCNTM | ADD15 |
| 48 | SIGCONT1 | SIGCONT0 | NMLPLT | ADD16 |
| 49 | SIGCONT3 | SIGCONT2 | NMLPLTM | ADD17 |
| 50 | GNDGND | DS60I78 | ADD18 | |
| 51 | ABOUT0 | ABIN0 | DS60O78 | ADD19 |
| 52 | ABOUT1 | ABIN1 | | ADD20 |
| 53 | ABOUT2 | ABIN2 | | ADD21 |
| 54 | ABOUT3 | ABIN3 | GND | GND |
| 55 | SOUT0-0 | SOUT0-1 | T1OUT20 | T1OUT20M |
| 56 | SOUT2-0 | SOUT2-1 | T1OUT22 | T1OUT22M |
| 57 | SOUT4-0 | SOUT4-1 | T1OUT24 | T1OUT24M |
| 58 | SOUT6-0 | SOUT6-1 | T1OUT26 | T1OUT26M |
| 59 | SOUT8-0 | SOUT8-1 | T1OUT28 | T1OUT28M |
| 60 | SOUT10-0 | SOUT10-1 | T1OUT30 | T1OUT30M |
| 61 | SOUT12-0 | SOUT12-1 | T1OUT32 | T1OUT32M |
| 62 | SOUT14-0 | SOUT14-1 | T1OUT34 | T1OUT34M |
| 63 | GND | GND | GND | GND |
| 64 | SIN0 | SIN0M | T1OUT36 | -C195A |
| 65 | SIN2 | SIN2M | T1OUT38 | |
| 66 | SIN4 | SIN4M | T1OUT40 | |
| 67 | SIN6 | SIN6M | T1OUT42 | |
| 68 | SIN8 | SIN8M | GND | GND |
| 69 | SIN10 | SIN10M | PSPEN | -FP48IN |
| 70 | SIN12 | SIN12M | CSPEN | DATA0 |
| 71 | SIN14 | SIN14M | | DATA1 |
| 72 | GND | GND | | DATA2 |
| 73 | | | DSIN42 | DATA3 |
| 74 | | | DSIN44 | DATA4 |
| 75 | | | DSIN46 | DATA5 |
| 76 | | | DSIN48 | DATA6 |
| 77 | | | DSIN50 | DATA7 |
| 78 | | | DSIN52 | DATA8 |
| 79 | | | DSIN54 | DATA9 |
| 80 | | | DSIN56 | DATA10 |
| 81 | | | DSIN58 | DATA11 |
| 82 | | | DSIN60 | DATA12 |
| 83 | | | DSIN62 | DATA13 |
| 84 | | | DSIN64 | DATA14 |
| 85 | | | DSIN66 | DATA15 |
| 86 | | | DSIN68 | |
| 87 | | | DSIN70 | |
| 88 | | | DSIN72 | |
| 89 | | | | |
| 90 | GND | GND | GND | GND |

# NTMX76AA

## Product description

The NTMX76AA card provides the following functions for DMS–100 extended multiprocessor system (XMS)–based peripheral modules (XPM):

- the DMSX messaging capability
- high–level data link control (HDLC) messaging capability
- tone generation

The NTMX76AA is a hybrid of the features in the NT6X69 and NT6X42, with added logic for additional features. The NTMX76AA has the following features:

- parallel speech bus interface
- speech bus connection memory
- intramodule connection to mate card
- tone generation with interface to a tone random–access memory (RAM) (downloadable tones), or a tone erasable programmable read–only memory (EPROM)
- cyclic redundancy check
- interface to the unified processor
- host–remote message select
- three application–specific integrated circuits (ASIC)—message processor, message logic, and tone sequencer
- test function for ASICs
- a 32–channel HDLC transceiver that can connect to each of the time slots off the parallel bus, or to the mate card
- intramodule communication link that contains 30 channels of 64 Kbit/s each
- matrix that controls data flow in the card
- common RAM shared that the HDLC controller and the main shelf processor (unified processor) share
- on–board processor control of the 32–channel HDLC transceiver chip
- ability to connect a maximum of 30 speech channels between the active unit and the inactive unit for communication between units
- ability to send and receive DS30 messages to and from the network in a host XPM Plus application

## **NTMX76AA** (continued)

- ability to send and receive DMSX or HDLC messages between an XPM Plus host and a common peripheral module (CPM) remote
- ability to control messaging on the incoming and outgoing parallel speech bus

The NTMX76AA is compatible with current XPM Plus and CPM configurations.

### Location

The NTMX76AA fits in the following shelves and slots:

- the CPM shelf, slot 8 and 20
- the XPM Plus shelf, slot 18

## Functional description

The NTMX76AA performs several main functions. The NTMX76AA performs the following functions:

- transmission and reception of DMSX and DS30 messages to and from the network or to lower level peripheral modules (PM).
- generation of call progress tones and transmission of the tones to the outgoing parallel speech bus
- control of the use of the 640 time slots of the two parallel speech buses
- transmission and reception of HDLC messages through 32 HDLC channels
- connection of each 32 HDLC channel to a parallel bus, or mate card in the mate unit, through a channel switching matrix

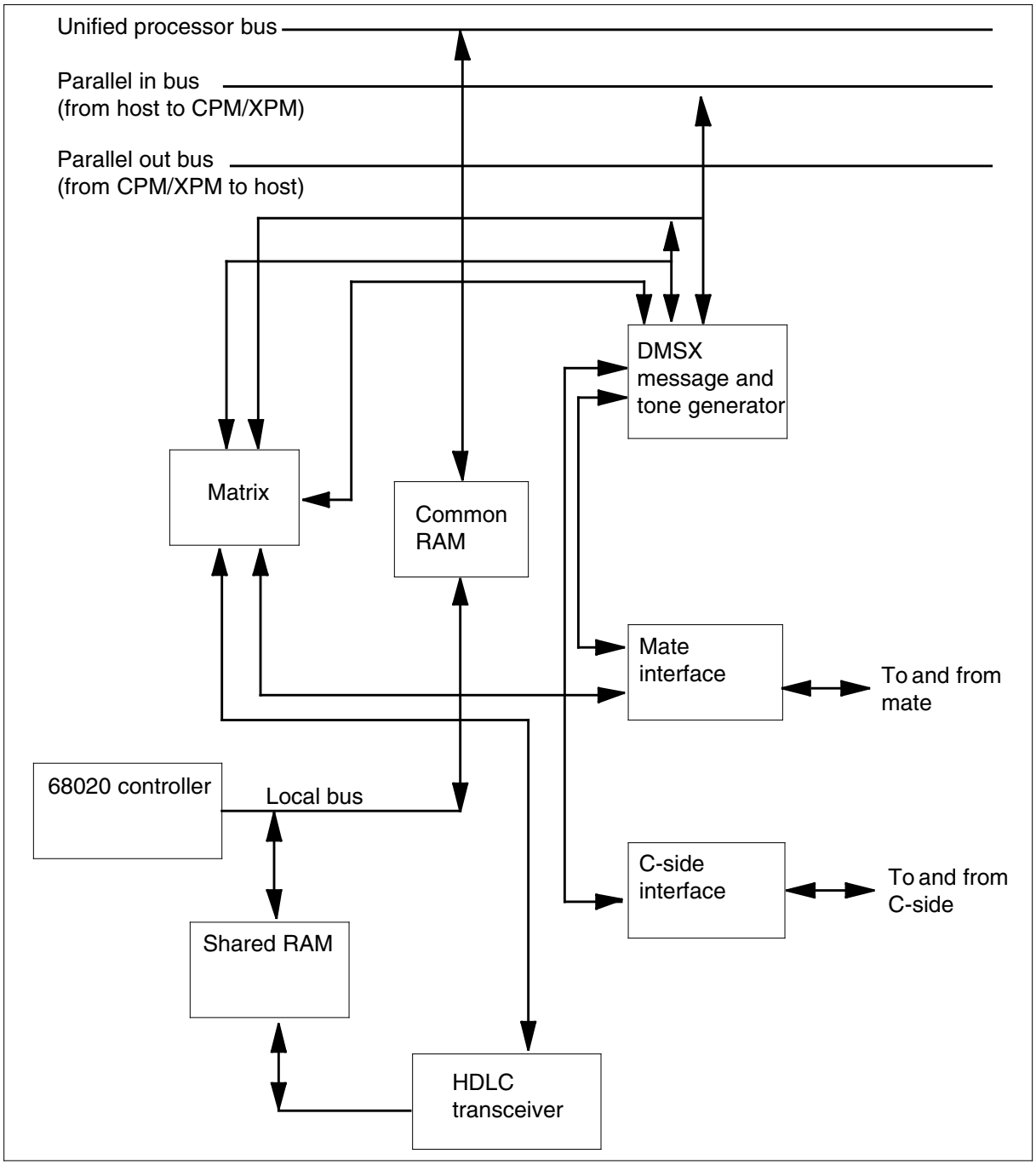
### Functional blocks

The NTMX76AA has the following functional blocks:

- a 68020 controller
- a HDLC transceiver
- shared RAM
- common RAM
- a DMSX message and tone generator
- matrix
- mate interface
- central–side (C–side) interface

The following diagram shows the relationship between the functional blocks.

**NTMX76AA functional blocks**



## NTMX76AA (continued)

### 68020 controller

The controller is based on the Motorola 68020 master processor. The controller controls the activity of the HDLC transceiver.

The controller has the following features:

- static RAM of 128 Kbytes
- real–time clock
- bus error circuit
- input/output (I/O) that includes universal synchronous/asynchronous receiver/transmitter (USART) to connect to a visual display unit terminal
- interrupt circuits

### HDLC transceiver

The HDLC transceiver is based on the Rockwell chip R8071. The HDLC transceiver has the following features:

- a clock that adapts the signal from the CPM system of 10.24 MHz to the Rockwell clock of 4.096 MHz
- an FIFO to notify the controller of a message reception or transmission

### Shared RAM

The shared RAM is a 64 Kbyte RAM. The controller and HDLC transceiver exchange messages through this RAM.

### Common RAM

The common RAM is a 16 Kbit–by–16 bit static RAM. The on–board 68020 controller and unified processor can access the common RAM. The common RAM transfers messages between the unified processor and the controller.

### DMSX message and tone generator

The DMSX message and tone generator is based on three ASICS with the functions of the NT6X69AC and NT6X69LA. The unified processor can read the contents of the tone memory. The unified processor can select the tone source as EPROM or RAM. The NT6X69AC uses EPROM. The NT6X69LA uses RAM.

### Matrix

The matrix provides channel switching between the functional blocks of the NTMX76AA. The matrix provides channel switching between the two parallel speech buses, and the HDLC transceiver and the mate card.

The unified processor controls the matrix. The matrix can perform the following functions:

- connection of each of 640 channels from each of two parallel speech buses to a target as follows:
  - — the 32 HDLC receiver channels
  - — the 30 intramodule communication channels
- connection of each of 32 HDLC transmitters to a target as follows:
  - — the 640 channels of each parallel speech bus
  - — the 30 intramodule communication channels
  - — the 32 HDLC channels
- connection of each of 30 intramodule communication channels to a target as follows:
  - — the 640 channels of each parallel speech bus
  - — the 32 HDLC channels
  - — the 30 intramodule communication channels

### Mate interface

The mate interface includes the following functions:

- A multiplexer routes one fixed channel to and from the message part of the card. The multiplexer routes all other channels to the matrix.
- On the receive side, an elastic buffer receives incoming signals. After reception, the signals transmit to the HDLC transceiver. The transceiver compensates for varying phases between the clocks of the two units in the module.
- On the transmit side, a local loop is present on the transmit data to the mate. This loop allows data to the mate to loop back for tests.

### C–side interface

The C–side interface allows the transmission and reception of messages directly to and from the host unit, separate from the matrix.

## Technical data

### Power requirements

The NTMX76AA requires approximately 2A of +5V.

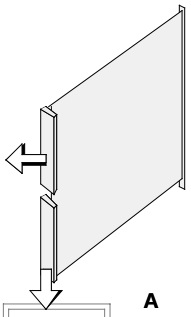
## **NTMX76AA** (continued)

# Signaling

### Pin numbers

The pin numbers for the NTMX76AA appear in the following figure.

### NTMX76AA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5 V | +5 V |
| 3A 3B | +5 V | +5 V |
| 4A 4B | +5 V | +5 V |
| 5A 5B | GND | GND |
| 6A 6B | FP- | C97+ |
| 7A 7B | GND | GND |
| 8A 8B | -ACT | C195TB |
| 9A 9B | -CHADIS | |
| 10A 10B | -CPROCS | |
| 11A 11B | GND | GND |
| 12A 12B | -DAS | |
| 13A 13B | -LDS | |
| 14A 14B | -DTACK1 | CPROCB |
| 15A 15B | -UDS | RUN |
| 16A 16B | -WRT | TADDR |
| 17A 17B | IMCOUT | IMCIN |
| 18A 18B | GND | -INT4REQ |
| 19A 19B | | |
| 20A 20B | | |
| 21A 21B | PIN 0 | POUT 0 |
| 22A 22B | PIN 1 | POUT 1 |
| 23A 23B | PIN 2 | POUT 2 |
| 24A 24B | PIN 3 | POUT 3 |
| 25A 25B | PIN 4 | POUT 4 |
| 26A 26B | PIN 5 | POUT 5 |
| 27A 27B | PIN 6 | POUT 6 |
| 28A 28B | PIN 7 | POUT 7 |
| 29A 29B | ADDR01 | CMSGOUT 0 |
| 30A 30B | ADDR02 | CMSGIN 0 |
| 31A 31B | ADDR03 | CMSGOUT 2 |
| 32A 32B | ADDR04 | CMSGIN 2 |
| 33A 33B | ADDR05 | -HOST/REM |
| 34A 34B | GND | GND |
| 35A 35B | ADDR06 | FPM- |
| 36A 36B | ADDR07 | GND |
| 37A 37B | ADDR08 | C97M+ |
| 38A 38B | ADDR09 | GND |
| 39A 39B | ADDR10 | CHOT |
| 40A 40B | ADDR11 | CHO1M |

| | A | B |
|---|---|---|
| 41A 41B | -XPMDIS | |
| 42A 42B | ADDR12 | |
| 43A 43B | ADDR13 | DEST00 |
| 44A 44B | ADDR14 | DEST01 |
| 45A 45B | ADDR15 | DEST02 |
| 46A 46B | ADDR16 | DEST03 |
| 47A 47B | ADDR17 | DEST04 |
| 48A 48B | ADDR18 | DEST05 |
| 49A 49B | ADDR19 | DEST06 |
| 50A 50B | ADDR20 | DEST07 |
| 51A 51B | ADDR21 | -RAMWRPB |
| 52A 52B | SEN 0 | -DESTXT0 |
| 53A 53B | SEN 1 | -DESTXT1 |
| 54A 54B | SEN 2 | -FIFOWRPB |
| 55A 55B | +PSPEN | PCH00 |
| 56A 56B | +CSPEN | PCH01 |
| 57A 57B | GND | GND |
| 58A 58B | DATA0 | PCH02 |
| 59A 59B | DATA1 | PCH03 |
| 60A 60B | DATA2 | PCH04 |
| 61A 61B | DATA3 | PCH05 |
| 62A 62B | DATA4 | PCH06 |
| 63A 63B | DATA5 | PCH07 |
| 64A 64B | GND | PCH08 |
| 65A 65B | DATA6 | PCH09 |
| 66A 66B | DATA7 | -AENPB |
| 67A 67B | DATA8 | RMSGOUT 0 |
| 68A 68B | DATA9 | RSMGIN 0 |
| 69A 69B | DATA10 | RMSGOUT M |
| 70A 70B | DATA11 | RSMGIN M |
| 71A 71B | DATA12 | TDOUT |
| 72A 72B | DATA13 | TDIN |
| 73A 73B | DATA14 | GND |
| 74A 74B | DATA15 | -MODRST |
| 75A 75B | UNIT | AUXRST- |
| 76A 76B | GND | GND |
| 77A 77B | | |
| 78A 78B | GND | GND |
| 79A 79B | | |
| 80A 80B | GND | GND |

## NTMX76BA

## Product description

The NTMX76BA card provides DMSX and HDLC messaging capability and tone generation for DMS–100 XMS–based peripheral modules.

The NTMX76BA is a hybrid of the features in the NT6X69 and NT6X42, with added logic for additional features. The NTMX76BA has the following features:

- parallel speech bus interface
- speech bus connection memory
- intermodule connection to mate card
- tone generation with interface to a tone RAM (downloadable tones), or a tone erasable programmable read–only memory (EPROM)
- cyclic redundancy check
- interface to the unified processor
- host–remote message select
- three application specific integrated circuits (ASIC), message processor, message logic, and tone sequencer
- test function for ASICs
- 32 channel HDLC transceiver that can connect to each of the time slots off the parallel bus or to the mate card
- intermodule communication link that contains 30 channels of 64 Kbit/s each
- matrix to controls data flow in the card
- common RAM that the HDLC controller and the main shelf processor or (unified processor) share
- on–board processor control of the 32 channel HDLC transceiver chip
- ability to connect a maximum of 30 speech channels between the active unit and the inactive unit for communication between units
- ability to send and receive DS30 messages to and from the network in a host XMS–based peripheral module (XPM) Plus application
- ability to send and receive DMSX or HDLC messages between an XPM Plus host and a common peripheral module (CPM) remote
- ability to control messaging on the incoming and outgoing parallel speech bus

The is NTMX76BA compatible with current XPM Plus and CPM configurations.

### Location

The NTMX76BA fits in the following shelves and slots:

- CPM shelf, slot 8 and 20
- XPM Plus shelf, slot 18

## Functional description

The functions of the NTMX76BA are as follows:

- send and receive DMSX and DS30 messages to and from the network or to lower level peripheral modules.
- generate call progress tones and send the tones to the outgoing parallel speech bus
- control the use of the 640 time slots of the two parallel speech buses
- send and receive HDLC messages through 32 HDLC channels
- use a channel switching matrix to connect each of the 32 HDLC channels to a parallel bus or to the mate card. The mate card is in the mate unit

### Functional blocks

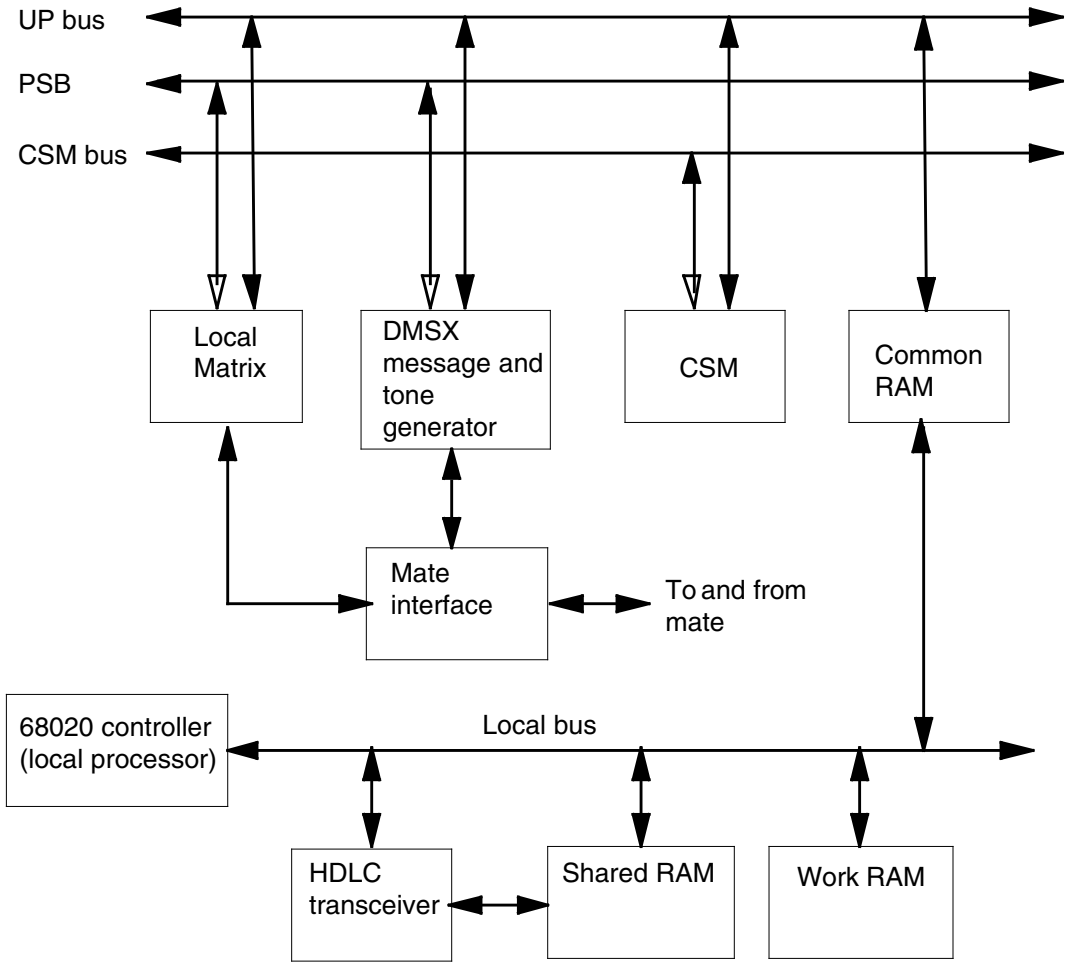
The NTMX76BA has the following functional blocks:

- 68020 controller
- HDLC transceiver
- shared RAM
- common RAM
- DMSX message and tone generator
- matrix
- mate interface
- C–side interface

The relationship between the functional blocks appears in the following figure.

## **NTMX76BA** (continued)

**NTMX76BA functional blocks**




UP unified processor
PSB parallel speech bus
CSM channel supervision message

### 68020 controller

The controller is based on the Motorola 68020 master processor. This controller controls the activity of the HDLC transceiver.

The controller has the following features:

- 128 Kbytes of static RAM
- real–time clock
- bus error circuit
- I/O with USART to connect to a visual display unit terminal
- interrupt circuits

### HDLC transceiver

The HDLC transceiver is based on the Rockwell chip R8071. This transceiver has the following features:

- a clock that adapts the signal from the CPM system of 10.24 MHz to the Rockwell clock of 4.096 MHz
- a FIFO that notifies the controller when the system receives or transmits a message
- shared RAM I/F between the CPU and R8071

### Shared RAM

The shared RAM is a 64 Kbyte RAM. The controller and HDLC transceiver exchange messages through the shared RAM.

### Common RAM

The common RAM is a 16 Kbit–by–16 bit static RAM. The unified processor and the on–board 68020 controller can access common RAM. The common RAM transfers messages between the unified processor and the controller.

### DMSX message and tone generator

The DMSX message and tone generator is based on three ASICS with the functions of the NT6X69AC and NT6X69LA. The unified processor can read the contents of the tone memory. The unified processor can select the tone source as EPROM or RAM. The unified processor selects EPROM like the NT6X69AC or RAM like the NT6X69LA.

### Matrix

The matrix provides channel switching between the functional blocks of the NTMX76BA and the two parallel speech buses. The matrix provides channel switching between the HDLC transceiver and the mate card.

## **NTMX76BA** (continued)

The unified processor controls the matrix. The processor can perform the following:

- connect each of the 640 channels from each of the two parallel speech buses. The channels connect to the 32 HDLC receiver channels or the 30 IMC channels.
- connect each of the 32 HDLC transmitters. The transmitters connect to the 640 channels of each parallel speech bus, the 30 IMC channels or the 32 HDLC channels.
- connect each of the 30 IMC channels. The channels connect to the 640 channels of each parallel speech bus, the 32 HDLC channels or the 30 IMC channels.

### Mate interface

The mate interface includes the following functions:

- A multiplexer routes one fixed channel to the message part of the card and from the message part of the card. A multiplexer routes the other fixed channels to the matrix.
- On the receive side, an elastic buffer receives incoming signals. The buffer sends the signals to the HDLC transceiver. The HDLC transceiver compensates for different phases between the clocks of the two units in the module.
- Two separate local loopbacks test the IMC link. For old DMSX, the loop back is from H83B output toward the mate pack to the input. For new HDLC, the loopback is from RX ASIC output toward the mate pack to the input.

### C–side interface

The C–side interface allows the direct transmission and reception of messages to and from the host unit. This action is independent of the matrix.

# Technical data

### Power requirements

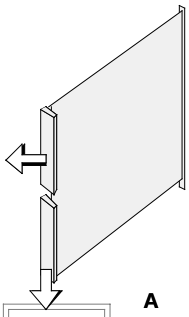
The NTMX76BA requires approximately 2 A of +5V.

# Signaling

### Pin numbers

The pin numbers for the NTMX76BA appear in the following figure.

### NTMX76BA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5 V | +5 V |
| 3A 3B | +5 V | +5 V |
| 4A 4B | +5 V | +5 V |
| 5A 5B | GND | GND |
| 6A 6B | FP- | C97+ |
| 7A 7B | GND | GND |
| 8A 8B | -ACT | C195TB |
| 9A 9B | -CHADIS | F720 |
| 10A 10B | -CPROCS | |
| 11A 11B | GND | GND |
| 12A 12B | -DAS | |
| 13A 13B | -LDS | |
| 14A 14B | -DSACK1 | CPROCB |
| 15A 15B | -UDS | RUN |
| 16A 16B | -WRT | TADDR |
| 17A 17B | IMCOUT | IMCIN |
| 18A 18B | GND | -INT4REQ |
| 19A 19B | PARTYER | SVBIT |
| 20A 20B | CSMIN | CSMOUT |
| 21A 21B | PIN 0 | POUT 0 |
| 22A 22B | PIN 1 | POUT 1 |
| 23A 23B | PIN 2 | POUT 2 |
| 24A 24B | PIN 3 | POUT 3 |
| 25A 25B | PIN 4 | POUT 4 |
| 26A 26B | PIN 5 | POUT 5 |
| 27A 27B | PIN 6 | POUT 6 |
| 28A 28B | PIN 7 | POUT 7 |
| 29A 29B | ADDR01 | CMSGOUT 0 |
| 30A 30B | ADDR02 | CMSGIN 0 |
| 31A 31B | ADDR03 | CMSGOUT 2 |
| 32A 32B | ADDR04 | CMSGIN 2 |
| 33A 33B | ADDR05 | -HOST/REM |
| 34A 34B | GND | GND |
| 35A 35B | ADDR06 | FPM- |
| 36A 36B | ADDR07 | GND |
| 37A 37B | ADDR08 | C97M+ |
| 38A 38B | ADDR09 | GND |
| 39A 39B | ADDR10 | CHO1T |
| 40A 40B | ADDR11 | CHO1M |

| | A | B |
|---|---|---|
| 41A 41B | -XPMDIS | GND |
| 42A 42B | ADDR12 | |
| 43A 43B | ADDR13 | DEST00 |
| 44A 44B | ADDR14 | DEST01 |
| 45A 45B | ADDR15 | DEST02 |
| 46A 46B | ADDR16 | DEST03 |
| 47A 47B | ADDR17 | DEST04 |
| 48A 48B | ADDR18 | DEST05 |
| 49A 49B | ADDR19 | DEST06 |
| 50A 50B | ADDR20 | DEST07 |
| 51A 51B | ADDR21 | |
| 52A 52B | SEN 0 | -DESTXT0 |
| 53A 53B | SEN 1 | -DESTXT1 |
| 54A 54B | SEN 2 | - |
| 55A 55B | +PSPEN | PCH00 |
| 56A 56B | +CSPEN | PCH01 |
| 57A 57B | GND | GND |
| 58A 58B | DATA0 | PCH02 |
| 59A 59B | DATA1 | PCH03 |
| 60A 60B | DATA2 | PCH04 |
| 61A 61B | DATA3 | PCH05 |
| 62A 62B | DATA4 | PCH06 |
| 63A 63B | DATA5 | PCH07 |
| 64A 64B | GND | PCH08 |
| 65A 65B | DATA6 | PCH09 |
| 66A 66B | DATA7 | |
| 67A 67B | DATA8 | RMSGOUT 0 |
| 68A 68B | DATA9 | RSMGIN 0 |
| 69A 69B | DATA10 | RMSGOUT M |
| 70A 70B | DATA11 | RSMGIN M |
| 71A 71B | DATA12 | TDOUT |
| 72A 72B | DATA13 | TDIN |
| 73A 73B | DATA14 | GND |
| 74A 74B | DATA15 | -MODRST |
| 75A 75B | UNIT | AUXRST- |
| 76A 76B | GND | GND |
| 77A 77B | | |
| 78A 78B | GND | GND |
| 79A 79B | | |
| 80A 80B | GND | GND |

# NTMX76CA

## Product description

The NTMX76CA card provides DMSX messaging capability and tone generation for DMS–100 XMS–based peripheral modules and channel supervision message (CSM) collection.

The NTMX76CA is a hybrid of the features in the NT6X69 and NT6X42, with added logic for additional features. The NTMX76CA has the following features:

- parallel speech bus interface
- speech bus connection memory
- intermodule connection to mate card
- tone generation with interface to tone erasable programmable read–only memory (EPROM)
- cyclic redundancy check
- interface to the unified processor
- host–remote message select
- three application–specific integrated circuits (ASIC), message processor, message logic, and tone sequencer
- test function for ASICs
- intermodule communication link that contains 30 channels of 64 Kbit/s each
- matrix that controls data flow in the card
- ability to connect a maximum of 30 speech channels between the active unit and the inactive unit for communication between units
- ability to send and receive DS30 messages to and from the network in a host XMS–based peripheral module (XPM) Plus application
- ability to send and receive DMSX messages between an XPM Plus host and a common peripheral module (CPM) remote
- ability to control messaging on the incoming and outgoing parallel speech bus

### Location

The NTMX76CA fits into the following shelves and slots:

- GPP shelf, slot 8 and 20
- SMA2 shelf, slot 8 and 20

## Functional description

The functions of the NTMX76CA are as follows:

- send and receive DMSX and DS30 messages to the network and from the network or to lower level peripheral modules.
- generate call progress tones and send the tones to the outgoing parallel speech bus
- control the use of the 640 time slots of the two parallel speech buses

### Functional blocks

The NTMX76CA has the following functional blocks:

- DMSX message and tone generator
- matrix
- mate interface
- C–side interface

### DMSX message and tone generator

The DMSX message and tone generator is based on three ASICS with the functions of the NT6X69AC. The unified processor can read the contents of the tone memory. The unified processor can select the tone source as EPROM like in the NT6X69AC.

### Matrix

The matrix provides channel switching between the functional blocks of the NTMX76CA, and the two parallel speech buses and the mate card.

### Mate interface

A multiplexer routes one fixed channel to the message part of the card and from the message part of the card. A multiplexer routes the other fixed channels to the matrix.

### C–side interface

The C–side interface allows direct transmission and reception of messages to and from the host unit. This action occurs independent of the matrix.

## Technical data

### Power requirements

The NTMX76CA requires approximately 2 A of +5V.

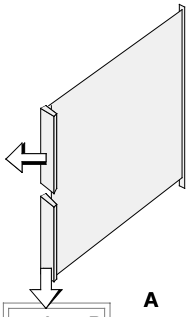
## **NTMX76CA** (continued)

# Signaling

### Pin numbers

The pin numbers for the NTMX76CA appear in the following figure.

### NTMX76CA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5 V | +5 V |
| 3A 3B | +5 V | +5 V |
| 4A 4B | +5 V | +5 V |
| 5A 5B | GND | GND |
| 6A 6B | FP- | C97+ |
| 7A 7B | GND | GND |
| 8A 8B | -ACT | C195TB |
| 9A 9B | | F720 |
| 10A 10B | CPROCS- | |
| 11A 11B | GND | GND |
| 12A 12B | -DAS | |
| 13A 13B | -LDS | |
| 14A 14B | -DSACK1 | CPROCB |
| 15A 15B | -UDS | RUN |
| 16A 16B | -WRT | TADDR |
| 17A 17B | IMCOUT | IMCIN |
| 18A 18B | GND | -INT4REQ |
| 19A 19B | PARTYER | SVBIT |
| 20A 20B | CSMIN | CSMOUT |
| 21A 21B | PIN 0 | POUT 0 |
| 22A 22B | PIN 1 | POUT 1 |
| 23A 23B | PIN 2 | POUT 2 |
| 24A 24B | PIN 3 | POUT 3 |
| 25A 25B | PIN 4 | POUT 4 |
| 26A 26B | PIN 5 | POUT 5 |
| 27A 27B | PIN 6 | POUT 6 |
| 28A 28B | PIN 7 | POUT 7 |
| 29A 29B | ADDR01 | CMSGOUT 0 |
| 30A 30B | ADDR02 | CMSGIN 0 |
| 31A 31B | ADDR03 | CMSGOUT 2 |
| 32A 32B | ADDR04 | CMSGIN 2 |
| 33A 33B | ADDR05 | -HOST/REM |
| 34A 34B | GND | GND |
| 35A 35B | ADDR06 | FPM- |
| 36A 36B | ADDR07 | GND |
| 37A 37B | ADDR08 | C97M+ |
| 38A 38B | ADDR09 | GND |
| 39A 39B | ADDR10 | CH01T |
| 40A 40B | ADDR11 | CH01M |

| | A | B |
|---|---|---|
| 41A 41B | -XPMDIS | GND |
| 42A 42B | ADDR12 | |
| 43A 43B | ADDR13 | DEST00 |
| 44A 44B | ADDR14 | DEST01 |
| 45A 45B | ADDR15 | DEST02 |
| 46A 46B | ADDR16 | DEST03 |
| 47A 47B | ADDR17 | DEST04 |
| 48A 48B | ADDR18 | DEST05 |
| 49A 49B | ADDR19 | DEST06 |
| 50A 50B | ADDR20 | DEST07 |
| 51A 51B | ADDR21 | |
| 52A 52B | SEN 0 | -DESTXT0 |
| 53A 53B | SEN 1 | -DESTXT1 |
| 54A 54B | SEN 2 | - |
| 55A 55B | +PSPEN | PCH00 |
| 56A 56B | +CSPEN | PCH01 |
| 57A 57B | GND | GND |
| 58A 58B | DATA0 | PCH02 |
| 59A 59B | DATA1 | PCH03 |
| 60A 60B | DATA2 | PCH04 |
| 61A 61B | DATA3 | PCH05 |
| 62A 62B | DATA4 | PCH06 |
| 63A 63B | DATA5 | PCH07 |
| 64A 64B | GND | PCH08 |
| 65A 65B | DATA6 | PCH09 |
| 66A 66B | DATA7 | |
| 67A 67B | DATA8 | RMSGOUT 0 |
| 68A 68B | DATA9 | RSMGIN 0 |
| 69A 69B | DATA10 | RMSGOUT M |
| 70A 70B | DATA11 | RSMGIN M |
| 71A 71B | DATA12 | |
| 72A 72B | DATA13 | |
| 73A 73B | DATA14 | GND |
| 74A 74B | DATA15 | -MODRST |
| 75A 75B | UNIT | AUXRST- |
| 76A 76B | GND | GND |
| 77A 77B | | |
| 78A 78B | GND | GND |
| 79A 79B | | |
| 80A 80B | GND | GND |

# NTMX77AA

## Product description

The NTMX77AA is a 68020–based unified processor (UP) circuit pack. The following DMS–100 peripheral modules use the UP pack:

- line trunk controller (LTC2)
- digital trunk controller (DTC2)
- remote cluster controller (RCC2)
- international line trunk controller (ILTC2)
- international digital trunk controller (IDTC2)
- international remote cluster controller (IRCC2)

## Functional description

The NTMX77AA is the main processing unit in the central processor and memory (CPM) shelf. This processing unit controls all the service packs, the trunks and the lines. This processing unit communicates with the central control.

### Functional blocks

The NTMX77AA contains the following functional blocks:

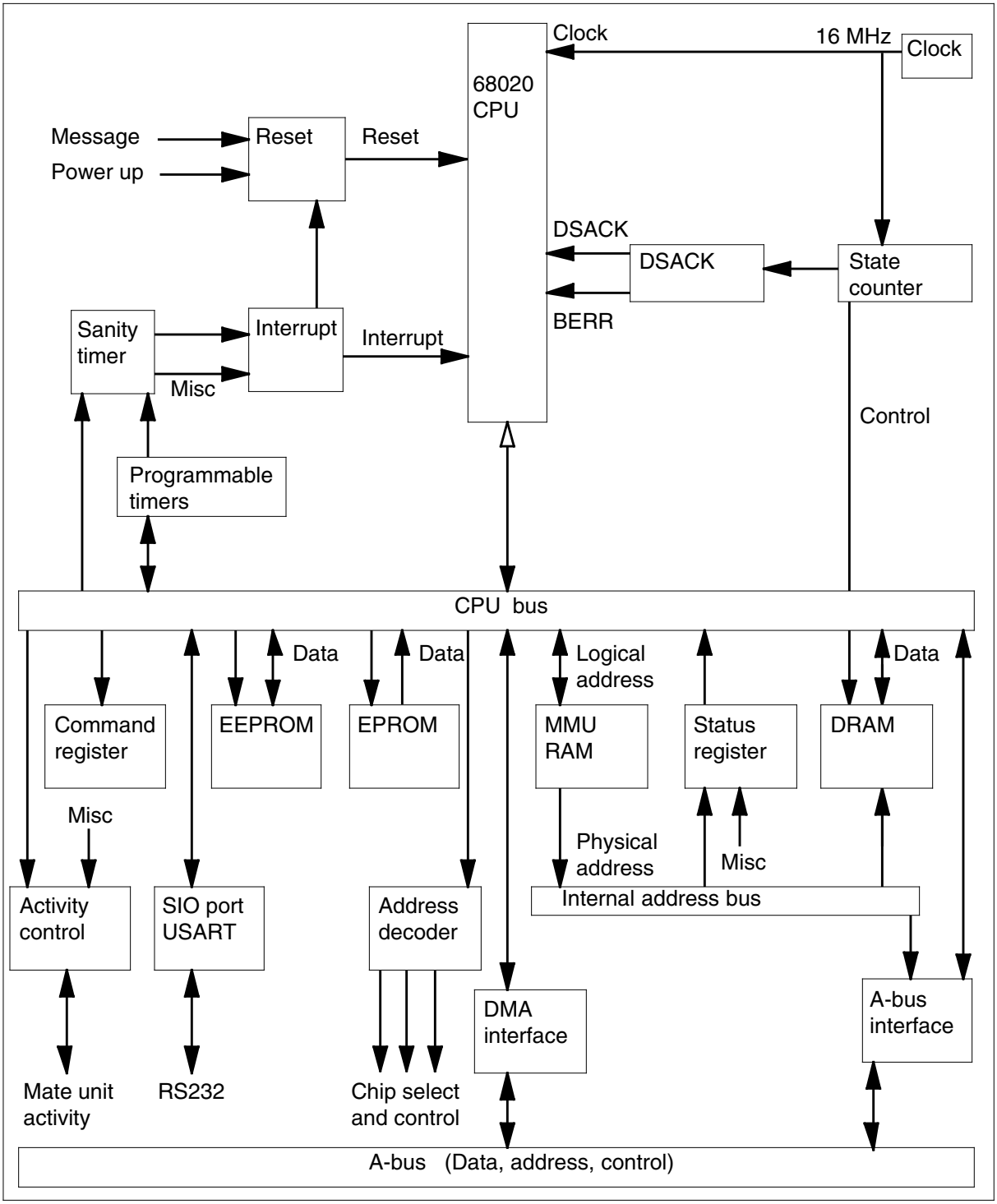
- CPU 68020
- state counter
- reset
- programmable timers
- data strobe acknowledge signal (DSACK) logic
- sanity timers
- interrupts
- activity control
- memory management unit (MMU)
- direct memory access (DMA)
- universal synchronous asynchronous receiver transmitter (USART)
- address–bus (A–bus) interface
- erasable programmable read–only memory (EPROM)
- EEPROM
- dynamic RAM (DRAM)

- address decoder
- status register
- command register

The relationship between the functional blocks appears in the following figure.

## **NTMX77AA** (continued)

### NTMX77AA functional blocks



### CPU 68020

The CPU is a 68020 processor with the capacity for 32 bits of data and 32 bits of address storage.

### State counter

The state counter synchronizes CPU activity. The state counter controls the DSACK signals and DRAM activity.

The state counter clears at the beginning of each CPU cycle when the CPU activates the external cycle start signal (–ECS). The counter clears in the DMA cycle when the master card sends the address strobe (–AS) signal. The outputs of the counter indicate state of the cycle to the card devices. This action allows the card devices to send a synchronous DSACK signal. This action prevents the addition of an additional wait state.

### Reset

The system sends a reset signal to the CPU when the following events occur:

- a power up
- an activity switch
- a sanity timer overflow
- the expiration of the watchdog counter
- an external reset from the message card
- a software reset or the processor resets

### Programmable timers

The four programmable timers have the following functions:

- One timer operates as a real time clock and interrupts the CPU every 10 ms.
- One timer operates as a software watchdog. This timer must be reset every 160 ms. This action prevents a sanity interrupt.
- Two timers set a serial input–output communication baud rate.

### Data strobe acknowledge signal logic

The DSACK logic sends a data strobe acknowledge signal when the CPU accesses an external device. If the DSACK signal does not arrive in 100 ms, the time out logic sends a bus error (BERR) signal to the CPU.

### Sanity timers

A sanity circuit protects the system from software failures. The sanity circuit contains a software watchdog and a hardware watchdog.

## **NTMX77AA** (continued)

The software watchdog is a sanity timer that the CPU must call and reset every 160 ms. The CPU does not always reset the sanity timer. If this event occurs the software watchdog sends an interrupt level 7 (nonmaskable) signal to the CPU.

The hardware watchdog is a sanity timer that the CPU cannot program. If the CPU does not reset this timer in 25 s, an interrupt level 7 (nonmaskable) signal to the CPU. If the CPU does not reset the timer in 12.5 s, the hardware watchdog sends another RESET signal to the CPU.

### Interrupts

The CPU has seven levels of interrupts. Only level 7 is nonmaskable.

- Level 7 Sanity interrupt request or break
- Level 6 Memory interrupt request (parity error)
- Level 5 Memory management unit interrupt
- Level 4 Message card interrupt
- Level 3 Real time clock interrupt
- Level 2 USART interrupt
- Level 1 Peripheral input/output 8 input ports can cause this interrupt
- Level 1 Activity interrupt that a drop activity port 0 causes
- Level 1 a 3 ms or 2 ms interrupt from the matrix port 1
- Level 1 sp ports 2–7

### Activity control

The activity control circuit starts or stops (gains or drops) unit activity.

The unit starts activity when the following events occur:

- the hardware forces a start, through the backplane
- the mate unit stops activity

The unit stops activity when the following events occur:

- when a software failure causes a sanity timer expiration.
- when the main CPM clock fails. The main CPM clock fails when the clock is missing for more than 1 ms. The main CPM clock fails when the frame pulse is missing for 540 ms.
- when the software causes activity to stop.

- after a CPU reset.
- after a message reset.

### Memory management unit

The MMU translates the CPU virtual address to a real address for the memory. The MMU has a RAM with a capacity of 2 Kbytes times 28 bits.

The upper 10 bits (bits 19 to 28) determine the size of the data segment. The low 14 bits (bits 1 to 14) give the start address of the segment. Bits 15 to 18 determine the protection status of the segment. These bits indicate if the segment is present in the memory.

The MMU sends an interrupt message to the CPU if the CPU address is missing from the segment. The MMU sends an interrupt message to the CPU if a protection problem occurs. The CPU reads the MMU register to identify the type of error that caused the interrupt message.

### Direct memory access

An ISP card uses DMA cycles to read or write bytes or 16 bit words to the DRAM of the CPU. The ISP uses the A–bus of the CPM and takes control of the internal bus of the CPU.

### USART

The USART converts data from serial format to parallel format and from parallel format to serial format. Two serial input/output ports share the dual USART. After a reset, the CPU has to start the USART. The physical interface is in an RS232 format and the baud rate is programmable. The USART interrupts the CPU when the USART receives information. The USART interrupts the CPU when the USART is ready to transmit a new byte.

### Address–bus interface

The memory and input/output controllers communicate with the processor through the synchronous A–bus. The A–bus uses ADDR0 to ADDR31 and DATA0 to DATA31. The A–bus uses handshake signals.

### EPROM

The EPROM has a storage capacity of 64 Kbytes times 16 bits. The EPROM stores a bootstrap loader that is nonvolatile. After a reset the loader chooses one of the two EEPROM banks available.

Access time to the EPROM is 5 clocks or 2 wait states or 312 ns.

## **NTMX77AA** (continued)

### EEPROM

The downloadable EEPROMs on this UP card are FLASH MEMORIES. Each EEPROM has a storage capacity of 256 Kbytes times 16 bits. The EEPROM stores a duplicate form of the low–level monitor and test procedures. FLASH MEMORIES allow the replacement of software versions in the EEPROM. FLASH MEMORIES use central control to load a tape and replace software. This condition eliminates the need to replace the EPROMs on all UP cards already in use.

The order of the EEPROM is two identical banks of 256 Kbytes times 16 bits. The EPROM selects one memory bank for on–line operation. The other memory bank operates as a backup when a system failure occurs during firmware changes.

Access time to the EEPROM is 5 clocks or 2 wait states or 312 ns.

### Dynamic RAM

The order of the DRAM in this pack is in four banks of 4 Mbytes of storage. Each bank is 1 Mbyte times 32 bits.

A parity generator and a parity checker generate parity. The system writes parity bit to a parity RAM chip. The DRAM contains four parity RAM chips. Each RAM chip has a capacity of 4 Mbytes times 1 bit.

The DRAM refreshes every 16 ms.

### Address decoder

The address decoder decodes microprocessor accesses to fixed locations in the memory map. Fixed locations are hardware locations. Chip–select or control lines on peripheral devices, memory banks, memory management units and status registers use these locations.

### Status register

The status register is a 32 bit register. This register latches the status of different card functions from the upper 16 bits (bits 17–32). The status register latches the address of the memory location that caused a parity error. This action occurs from the lower 16 bits (bits 1–16). The functions that the status register reports include card activity, memory size, power failure, parity error and clock fail status.

### Command register

The command register in the CPU accesses a 5–bit register through the data bus. The command register uses the 5–bit register to control internal activities like parity calculation and LED indications.

## Technical data

### Power requirements

The NTMX77AA requires a maximum of 4.0 A from the +5V supply, and a maximum of 100.0 mA from the +12V or –12V supplies.

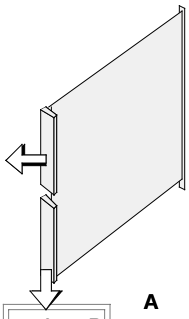
## Signaling

### Pin numbers

The pin numbers for NTMX77AA appear in the following figure.

# **NTMX77AA** (end)

### NTMX77AA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | +5V | +5V |
| 4A 4B | +5V | +5V |
| 5A 5B | GND | GND |
| 6A 6B | *-BREQ | -BG |
| 7A 7B | -BUSGRI | -MODRST |
| 8A 8B | **-ACTIVE0 | -MSGRST |
| 9A 9B | -BUSBSY | MATECK FAIL |
| 10A 10B | 32MEG | |
| 11A 11B | GND | -ACTIVE1 |
| 12A 12B | -DAS | AS+ |
| 13A 13B | -LDS | 16MEG |
| 14A 14B | -DTACK | |
| 15A 15B | -UDS | |
| 16A 16B | -BWRT | -SANDIS |
| 17A 17B | 8MEG | |
| 18A 18B | -RSTIN | |
| 19A 19B | | PARINT |
| 20A 20B | -PERINT1 | -MSGIRQ |
| 21A 21B | -PERINT2 | -ECS |
| 22A 22B | GND | +5MFAIL |
| 23A 23B | -PERINT3 | -RMC |
| 24A 24B | -PERINT4 | |
| 25A 25B | -PERINT5 | -MATEACT |
| 26A 26B | -PERINT6 | -OWNACT |
| 27A 27B | -PERINT7 | GND |
| 28A 28B | -MEMIRQ | |
| 29A 29B | ADD1 | |
| 30A 30B | ADD2 | HPU+12 |
| 31A 31B | ADD3 | HDICLK |
| 32A 32B | ADD4 | HDOCLK |
| 33A 33B | ADD5 | HACKOUT |
| 34A 34B | GND | HDOUT |
| 35A 35B | ADD6 | HDIN |
| 36A 36B | ADD7 | TPU12+ |
| 37A 37B | ADD8 | TACKIN |
| 38A 38B | ADD9 | TDOUT |
| 39A 39B | ADD10 | TDIN |
| 40A 40B | ADD11 | GND |

**Legend**

| | |
|---|---|
| *CPM version | -BG is 6B |
| | -ACTIVE0 is 8A |
| **XPM version | -BG is 8A |
| | -ACTIVE0 is 6B |

| | A | B |
|---|---|---|
| 41A 41B | GND | BERR- |
| 42A 42B | ADD12 | -DS |
| 43A 43B | ADD13 | -DSACK0 |
| 44A 44B | ADD14 | |
| 45A 45B | ADD15 | CKFAIL |
| 46A 46B | ADD16 | -BREAK |
| 47A 47B | ADD17 | GND |
| 48A 48B | ADD18 | ST3 |
| 49A 49B | ADD19 | ST2 |
| 50A 50B | ADD20 | ST1 |
| 51A 51B | ADD21 | ST0 |
| 52A 52B | ADD22 | SPAR1 |
| 53A 53B | GND | SPAR2 |
| 54A 54B | ADD23 | SPAR3 |
| 55A 55B | FC0 | SIZE0 |
| 56A 56B | FC1 | SIZE1 |
| 57A 57B | FC2 | ADD0 |
| 58A 58B | D0 | -ACTIVE3 |
| 59A 59B | D1 | GND |
| 60A 60B | D2 | -DCHFAIL |
| 61A 61B | D3 | -ACTIVE2 |
| 62A 62B | D4 | SPARE0 |
| 63A 63B | D5 | -CDIS |
| 64A 64B | GND | |
| 65A 65B | D6 | |
| 66A 66B | D7 | |
| 67A 67B | D8 | |
| 68A 68B | D9 | |
| 69A 69B | D10 | |
| 70A 70B | D11 | GND |
| 71A 71B | D12 | |
| 72A 72B | D13 | ST0 |
| 73A 73B | D14 | ST1 |
| 74A 74B | D15 | ST2 |
| 75A 75B | SWACST3 | |
| 76A 76B | GND | ST4 |
| 77A 77B | +12V | +12V |
| 78A 78B | GND | GND |
| 79A 79B | -12V | -12V |
| 80A 80B | GND | GND |

# NTMX79AA

## Product description

The NTMX79AA extension pack is an interface between the common peripheral module and the extension shelf of the common peripheral module.

The NTMX79AA has the following features:

- power converter that supplies +5V, +12V, and –12V to this extension pack and other packs in the shelf
- transfers data between the main shelf and the extension shelf backplane
- splits five incoming DS60 signals from the main shelf to ten DS60 signals and forwards the signals to the DCH packs
- converts five pairs of DS60 signals from the DCH packs to five DS60 signals and forwards the signals to the main shelf
- each time slot can loop back to the main shelf for maintenance purposes
- supplies –48V through a diode to the DCH packs to make the 48V supply redundant

The NTMX79AA is not backward compatible.

### Location

The CPM extension shelf holds four NTMX79AA extension packs. The extension packs fit in slots 2, 13, 14, and 25 of the CPM extension shelf.

## Functional description

The NTMX79AA transfers signals between the main shelf and the packs in the extension shelf of the CPM. The NTMX79AA provides +5V and +12V or –12V of power. Each extension pack connects to unit 0 or unit 1 of the CPM main shelf. The activity line of the main shelf determines if each extension pack is active or inactive.

### Functional blocks

The NTMX79AA has the following functional blocks:

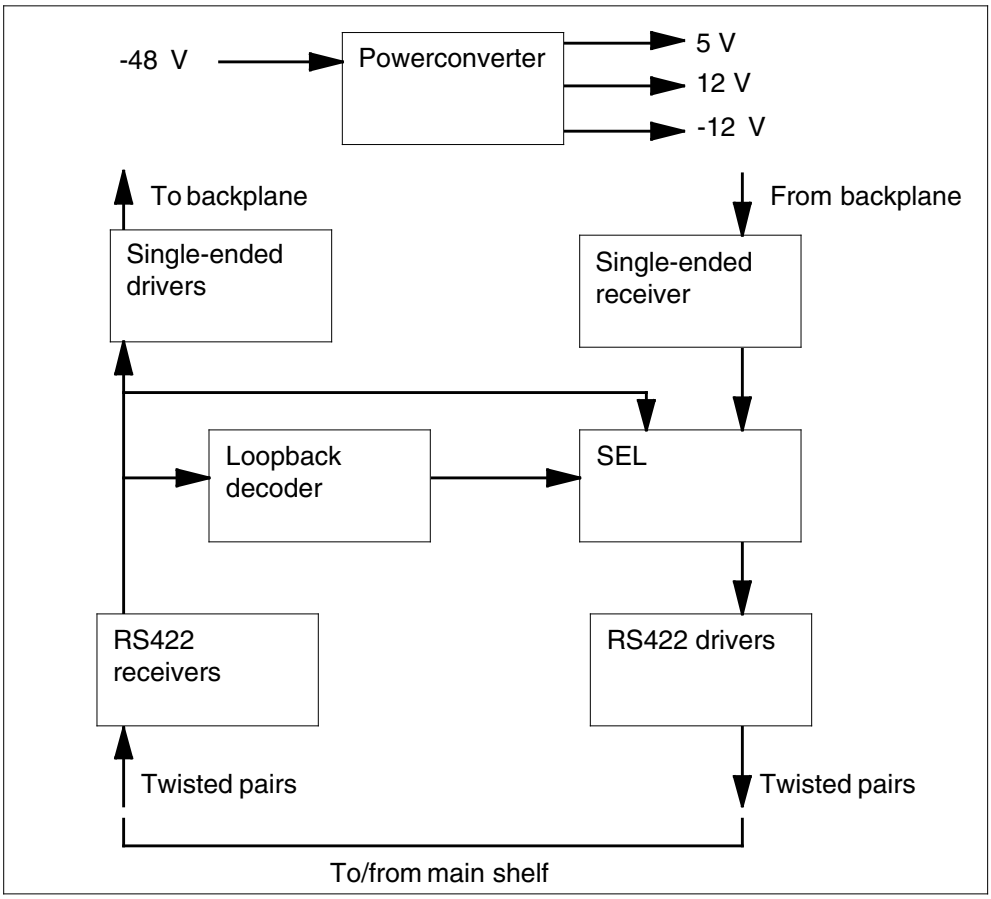
- RS422 receiver
- single–ended drivers
- DS60 receivers and RS422 drivers
- loopback
- power converter
- DS60 splitter

## NTMX79AA (continued)

- DS60 concentrator
- output delay
- loopback delay and loopback register
- status word registers

The relationship between the functional blocks appears in the following figure.

**NTMX79AA functional blocks**




### RS422 receiver

Signals transmitted from the main shelf to the extension pack are in RS422 format. The RS422 receiver converts the signals to NRZ format.

### Single–ended drivers

The single–ended drivers move the signal in NRZ format. The drivers move the signal from the RS422 receiver in the main shelf to the extension packs in the extension shelf.

### DS60 receivers and RS422 drivers

Signals from the extension packs arrive at the DS60 receivers in NRZ format. The receivers convert the signals to RS422 format. The RS422 drivers transmit the signals in RS422 format to the main shelf.

### Loopback

The loopback circuits provides the ability to loop back every time slot in each DS60. The content of bit 0 of the time slot determines if the loopback circuits loops back the time slot.

### Power converter

The power converter of the extension pack supplies +5V, +12V, and –12V to the main shelf.

### DS60 splitter

The connection between the main shelf and the extension shelf of the CPM occurs with 12 DS60 signals.

Twelve DS60 signals come from the main shelf to the extension shelf. The DS60 splitter divides five of the signals. This splitter changes the signals into ten DS30s. Each of the split signals contains data important to some DS30s, as the DCH pack requires.

### DS60 concentrator

Twelve DS60 signals provide the connection between the main shelf and the extension shelf of the CPM.

The DS60 concentrator combines five pairs of DS30 signals from the DCH packs to five DS60 signals. The DS60 concentrator sends the signals to the main shelf.

### Output delay

The output delay adjusts the output signal timing to match the timing of the main shelf. The delay from the peripheral extension packs to the main shelf is one frame.

### Loopback delay and loopback register

For maintenance purposes, every time slot in the extension shelf can loop back to the main shelf. The loopback delay adjusts the timing of the looped signal.

## **NTMX79AA** (continued)

The loopback delay sends the signal to the main shelf with the correct timing. The delay from the peripheral packs to the main shelf is two frames.

The loopback register can loopback every time slot of the DS60.

### Status word registers

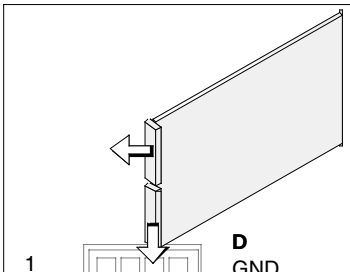
The status word registers receive and transmit status information between the main shelf and the extension shelf.

# Signaling

### Pin numbers

The pin numbers for the NTMX79AA appear in the following figure.

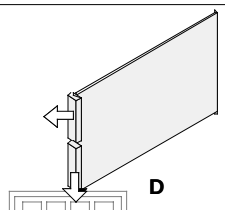
**NTMX79AA pin numbers (Part 1 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 1 | GND | GND | GND | GND |
| 2 | +5Vout | +5Vout | +5Vout | +5Vout |
| 3 | +5Vout | +5Vout | +5Vout | +5Vout |
| 4 | +5Vout | +5Vout | +5Vout | +5Vout |
| 5 | GND | GND | GND | GND |
| 6 | GND | GND | GND | GND |
| 7 | | -FPC | -FPB | -FPA |
| 8 | | | -ACTB | -ACTA |
| 9 | 12VNU | | CB7B | C97A |
| 10 | | C97E | C97D | C97C |
| 11 | GND | GND | GND | GND |
| 12 | GND | GND | GND | GND |
| 13 | GND | GND | GND | GND |
| 14 | | | DSO30EV | DSO30OD |
| 15 | | | DSO32EV | DSO40EV |
| 16 | -48V | -48V | -48V | -48V |
| 17 | -48V | -48V | -48V | -48V |
| 18 | -48V | -48V | -48V | -48V |
| 19 | -48V | -48V | -48V | -48V |
| 20 | -48VOUT | -48VOUT | -48VOUT | -48VOUT |
| 21 | -48VOUT | -48VOUT | -48VOUT | -48VOUT |
| 22 | -48VOUT | -48VOUT | -48VOUT | -48VOUT |
| 23 | -48VOUT | -48VOUT | -48VOUT | -48VOUT |
| 24 | -48V | -48V | -48VR | -48VR |
| 25 | -48V | -48V | -48VR | -48VR |
| 26 | -48V | -48V | -48VR | -48VR |
| 27 | -48V | -48V | -48VR | =48VR |
| 28 | | | DSI44 | |
| 29 | AL.SPAR | | C122A | DSI52 |
| 30 | -48VABSR | LED CONTR | DSI48 | DSI56 |
| 31 | RESET | HOLD | DCHRST- | |
| 32 | -48VABS | POWER | C122C | C122B |
| 33 | | AL.DCH | | DSI31 |
| 34 | GND | GND | GND | GND |
| 35 | GND | GND | GND | GND |
| 36 | | | DSI46 | DSI54 |
| 37 | | | | DSI33 |
| 38 | | | DSI38 | |
| 39 | | | C324B | C324A |
| 40 | | | | C324C |
| 41 | | | | |
| 42 | | | | |
| 43 | | | | |
| 44 | | | DSI20 | -C195out |
| 45 | +5VTEST | RC1 | DSI50 | DSI34 |

# **NTMX79AA** (end)

### NTMX79AA pin numbers (Part 2 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 46 | | RC2 | | |
| 47 | | | DSO44 | DSO30 |
| 48 | | | DSO46 | DSO32 |
| 49 | | | DSO48 | DSO38 |
| 50 | | | DSO50 | DSO40 |
| 51 | EXDSO78- | EXDSO78+ | DSO54 | |
| 52 | EXC97- | EXC97+ | DSO56 | |
| 53 | EXACT- | EXACT+ | DSO52 | |
| 54 | EX122- | EX122+ | DSO34 | |
| 55 | EXDCHRST- | EXDCHRST+ | -FP48B | -FP48A |
| 56 | EXDSO30- | EXDSO30+ | | -FP48C |
| 57 | EXDSI30- | EXDSI30+ | | |
| 58 | | | GND | GND |
| 59 | EXDSO32- | EXDSO32+ | GND | GND |
| 60 | EXDSI32- | EXDSI32+ | | |
| 61 | EXDSO34- | EXDSO34+ | | |
| 62 | EXDSI34- | EXDSI34+ | | |
| 63 | EXDSO38- | EXDSO38+ | | |
| 64 | EXDSI38- | EXDSI38+ | | |
| 65 | EXDSO40- | EXDSO40+ | | |
| 66 | EXDSI40- | EXDSI40+ | | |
| 67 | EXDSO44- | EXDSO44+ | -DS1.4/23 | -DS1.8/19 |
| 68 | EXDSI44- | EXDSI44+ | | -DS1.6/21 |
| 69 | EXDSO46- | EXDSO46+ | MATE OUT FAIL | MATE IN FAIL |
| 70 | EXDSI46- | EXDSI46+ | | |
| 71 | EXDSO48- | EXDSO48+ | | |
| 72 | EXDSI48- | EXDSI48+ | DSI30 | |
| 73 | EXDSO50- | EXDSO50+ | DSI32EV | DSI40EV |
| 74 | EXDSI50- | EXDSI50+ | | |
| 75 | EXDSO78- | EXDSO78+ | DSI30EV | DSI30D |
| 76 | EXFP48- | EXFP48+ | DSI16 | |
| 77 | EXDSO52- | EXDSO52+ | | |
| 78 | EXDSI52- | EXDSI52+ | | |
| 79 | EXDSO54- | EXDSO54+ | | |
| 80 | EXDSI54- | EXDSI54+ | | |
| 81 | EXDSO56- | EXDSO56+ | | |
| 82 | EXDSI56- | EXDSI56+ | | |
| 83 | | | | |
| 84 | +12V | +12V | +12V | +12V |
| 85 | GND | GND | GND | GND |
| 86 | GND | GND | GND | GND |
| 87 | | | | |
| 88 | -12V | -12V | -12V | -12V |
| 89 | GND | GND | GND | GND |
| 90 | GND | GND | GND | GND |

# NTMX81AA

## Product description

The NTMX81AA dual DS–1 interface card provides an interface between common peripheral module (CPM) shelves and local transmission equipment. The local transmission equipment can be office repeaters and channel banks. The dual DS–1 interface card uses a new pack size that is 1/6 the size of the standard DMS–100. The new pack size is a packlet.

### Location

A quad frame carrier can contain four NTMX81AA packlets. The quad frame carrier is NTMX87. This frame carrier occupies a standard size CPM slot.

## Functional description

The NTMX81AA card provides an interface between two physical DS–1 links and the CPM. This card performs low–level DS–1 signaling and speech interface functions.

### Functional blocks

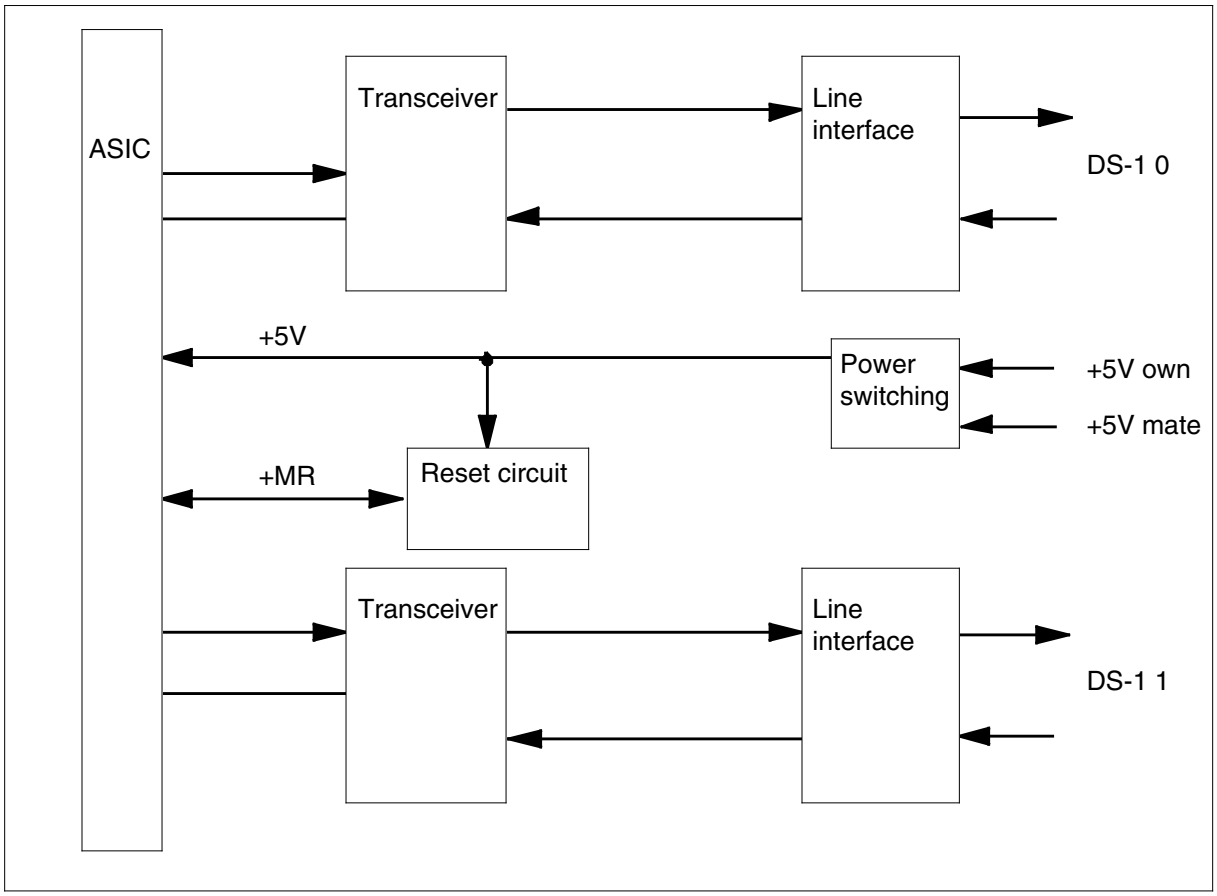
The NTMX81AA has the following functional blocks:

- application–specific integrated circuit (ASIC) interface
- QMV184 transceiver
- line interface integrated circuit
- power feed switching

The relationship between the functional blocks appears in the following figure.

## **NTMX81AA** (continued)

**NTMX81AA functional blocks**




### Application–specific integrated circuit interface

The ASIC interface provides the following functions:

- selects the DS60
- performs a loop back
- extracts control bits from channel 0
- multiplexes signals to the matrix and from the matrix

### QMV184 transceiver

Two QMV184 custom silicon transceivers are present on this circuit pack. One transceiver is present for each of the two ports. Each QMV184 has an associated 4 Kbyte times 4 bit static RAM for framing.

The transmit section of the QMV184 accepts serial data from the host, adds overhead framing and control bits. The transmit section encodes the composite

signal for DS–1 transmission. The receive section of the QMV184 decodes the linecoded DS–1 signal and acquires frame. The receive section extracts the overhead control information and outputs serial data to the host.

The QMV814 transceiver supports the following features:

- super frame (SF) format
- extended super frame (ESF) format
- SLC96 data link
- facility data link (FDL)
- signaling bit freeze
- line codes: ZCSIB8ZSI no encoding
- cyclic redundancy check (CRC6)
- carrier fail alarm (CFA)
- alarm indication signal (AIS)

### Line interface integrated circuit

The line interface integrated circuit has the following functions:

- shapes output waves for different line lengths
- clock recovery
- DS–1 input amplification
- drives and receives physical lines
- input jitter attenuator
- all ones (111...) transmission
- remote loop around

### Power feed switching

The NTMX81AA has a feed circuits that change the power source from the active power supply to the mate power supply. The feed circuits change the power supply when the active power supply fails.

## **NTMX81AA** (continued)

# Technical data

### Power requirements

The power requirements of the NTMX81AA appear in the following table.

**Power requirements of the NTMX81AA**

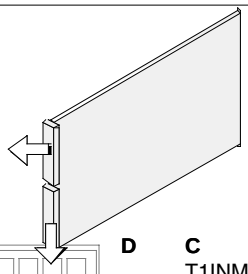
| Voltage (V) | Current (mA) |
|---|---|
| +5 | 330 |
| +12 | 3 |
| –12 | |
| –48 | |

# Signaling

### Pin numbers

The pin numbers for the NTMX81AA appear in the following figure.

**NTMX81AA pin numbers**



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | T1INM/C1 | T1IN/C1 | GND |
| 2 | | T1OUT/P0 | T1INM/P0 | C97 |
| 3 | | T1OUT/P1 | T1INM/P1 | -ACT |
| 4 | | T1OUT/C0 | T1INM/C0 | C324 |
| 5 | | T1OUT/C1 | +5VM | SENDT0 |
| 6 | | T1OUTM/P0 | FRPCOM | SENDR0 |
| 7 | | T1OUTM/P1 | -FP48M | SENDT1 |
| 8 | | T1OUTM/C0 | C324M | SENDR1 |
| 9 | | T1OUTM/C1 | P/-C | RECT0 |
| 10 | | MSGIN0 | -U0/U1 | RECR0 |
| 11 | | MSGOUT | +12V | RECT1 |
| 12 | | FPRC0 | -12V | RECR1 |
| 13 | | FPRC2 | +12VM | C97M |
| 14 | | FP48- | -12VM | T1IN/P0 |
| 15 | | | T1INCO | T1IN/P1 |
| 16 | | +5V | MSGEN | GND |
| 17 | | | | |
| 18 | | | | |
| 19 | | | | |
| 20 | | | | |
| 21 | | | | |
| 22 | | | | |
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| 41 | | | | |
| 42 | | | | |
| 43 | | | | |
| 44 | | | | |
| 45 | | | | |

# NTMX82AA

## Product description

The NTMX82AA Dual PCM30 interface card provides a link between CPM shelves and co–located transmission equipment. Office repeaters and channel banks are co–located transmission equipment.

This dual PCM30 interface uses a new pack size that is 1/6th of the standard DMS–100 size. The new pack size is a packlet and is the same as the dual DS1 interface NTMX81.

### Location

Four of these packlets fit in a quad frame carrier. The quad carrier frame occupies a standard size CPM slot. The quad frame carrier is NTMX81.

## Functional description

The NTMX82AA Dual PCM30 interface contains:

- application–specific integrated circuit (ASIC)
- Conference of European Postal and Telecommunications (CEPT) Administrations transceiver DS2181A
- line interface integrated circuit and power feed switching

### Application–specific integrated circuit (ASIC) functional blocks

The NTMX82AA has the following ASIC functional blocks:

- bidirectional serial interface between a DS60 line and two DS2181A PCM30 transceivers
- select the active DS60 line from own or mate DS60 according to an activity pin
- generate the 5.12 MHz and 2.56 MHz internal clocks and the 2.048 MHz system clock from the 10.24 MHz clock input
- generate synchronization pulses for the PCM30 transceiver and for the internal elastic buffer
- loopback for each timeslot—The ASIC extracts a timeslot from the outgoing PCM30 stream to the DS2181A transceiver. The ASIC inserts a timeslot in the incoming PCM30 stream. Each timeslot, except for timeslot 0, can loop back according to a software controlled register.
- Message control channel—The ASIC provides a bidirectional interface for the DMSX message between the message pack and the host switch. The ASIC inserts the message received from the message pack on timeslot 1 or 16 of the outgoing PCM30 stream. In the opposite direction, the ASIC extracts the message received on timeslot 1 or 16. The ASIC sends the

message to the message pack. The software selects timeslot 1 or 16 for the message channel.

- signaling buffer—The ASIC stores and inserts timeslot 16 of the incoming PCM30 stream. The ASIC inserts the timeslot as timeslot 16 in a specified frame of the 16–frame multiframe. The incoming PCM30 stream contains the signaling information. The signaling buffer operates when the Channel Associated Signaling mode is active.
- slip counter—The ASIC samples slip output of the internal elastic buffer. An 8–bit counter registers the number of slips.
- timeslot 0 odd—The ASIC detects an odd timeslot 0 out of the 16–frame multiframe. The ASIC sends the timeslot to the matrix pack. In the opposite direction, the ASIC controls the odd timeslot 0 the DS2181A transceiver sends.
- serial interface—A serial bidirectional interface controls each DS2181A transceiver. The ASIC accesses each register of the DS2181A in read/write or read–only mode.
- CRC4 error indication bits (E–bits)—These E–bits indicate sub–multiframes that contains errors. On the transmit side, the ASIC inserts two E–bits in the outgoing data stream. The hardware circuit or the software–loop register provide these bits. On the receive side, the ASIC extracts two E–bits from the incoming data stream. The ASIC inserts the E–bits in the odd register.
- E–bit count register (EBCR)—The EBCR register counts the E–bits received in the incoming data.
- facility data link (FDL)—This function creates a communication link. On the transmit side, the ASIC inserts FDL bits in the odd frames of the outgoing data. The FDL register provides the FDL bits. On the receive side, the ASIC inserts FDL bits in the FDL register. The odd frames of the incoming data provide the FDC bits.
- international bits (INB)—On the transmit side, the ASIC inserts INB in the odd and even frames of the outgoing data. The loop register provides the INB. On the receive side, the ASIC inserts the INB in the odd register. The odd and even frames of the incoming data provide the INB.
- blanking data interface—The ASIC inserts all ones in the channels (1–31) sent to the matrix, after loss of frame synchronization (RFSA=1).
- internal elastic store—There is an elastic store of two frames depth. The store slips on the frame boundary. The store has slip detection and control.

## NTMX82AA (continued)

### Conference of European Postal and Telecommunications (CEPT) administrations transceiver DS2181A functional blocks

The NTMX82AA has the following CEPT transceiver DS2181A functional blocks:

- primary rate transceiver to execute International Telegraph and Telephone Consultative Committee (CCITT) standards
- supports cyclic redundancy check–4 (CRC4)–based framing standards
- supports common associated signaling (CAS) and common channel signaling (CCS) signaling standards
- contains on–chip alarm generation, alarm detection, and error logging logic
- operates with the DS2175 elastic store or with the internal elastic store in the ASIC

### Line interface integrated circuit functional blocks

The NTMX82AA has the following line interface integrated circuit functional blocks:

- wave shaping according to CCITT
- clock recovery
- CEPT input amplifier (with AGC)
- physical line driving and receiving
- input jitter attenuator

### Power feed switching functional blocks

The NTMX82AA has the following power feed switching functional blocks:

- power supply redundancy—the feed circuits change the power source from the own power supply to the mate power supply. This event occurs when the own power supply fails
- blown fuse indication—a special detection logic that detects and sets a bit if a fuse blows. The redundant fuses on the pack provides this feature.

## Signaling

### Pin numbers

The pin numbers for the NTMX82AA appear in the following table.

**NTMX82AA pin numbers**

| Pin | A | B | C | D |
|---|---|---|---|---|
| 1 | GND | T1IN/C1 | T1INM/C1 | – |
| 2 | C97 | T1INM/P0 | T1OUT/P0 | – |
| 3 | –ACT | T1INM/P1 | T1OUT/P0 | – |
| 4 | C324 | T1INM/C0 | T1OUT/C0 | – |
| 5 | SENDT0 | +5VM | T1OUT/C1 | – |
| 6 | SENDR0 | FRPC1 | T1OUTM/P0 | – |
| 7 | SENDT1 | –FP48M | T1OUTM/P1 | – |
| 8 | SENDR1 | C324M | T1OUTM/C0 | – |
| 9 | RECT0 | P/–C | T1OUTM/C1 | – |
| 10 | RECR0 | –U0/U1 | MSGIN0 | – |
| 11 | RECT1 | +12V | MSGOUT | – |
| 12 | RECR1 | –12V | FPRC0 | – |
| 13 | C97M | +12VM | FPRC0M | – |
| 14 | T1IN/P0 | –12VM | FP48– | – |
| 15 | T1IN/91 | T1IN/C0 | – | – |
| 16 | GND | MSGEN | +5V | – |

***Note:*** Blank cells indicate pins that are not in use.

## Technical data

The dual PCM30 packlet consumes the following:

## **NTMX82AA** (end)

### Power requirements

The power requirements for the NTMX82AA appear in the following table.

**Power requirements**

| Voltage | Current |
|---|---|
| +5 V | 300 mA |
| +12 V | 3 mA |
| –48 V | —— |

### Environmental requirements

The environmental requirements for the NTMX82AA follows:

1. Ambient air temperature: <70 deg C
2. Relative humidity: 20–80% for short term; 20–55% normal

# NTMX82CA

## Product description

The NTMX82AA Dual PCM30 interface card provides a link between CPM shelves and co–located transmission equipment. Office repeaters and channel banks are co–located transmission equipment.

This dual PCM30 interface uses a new pack size (packlet) that is 1/6th of the standard DMS–100 size. The packlet is the same as the dual DS1 interface NTMX81.

The NTMX82CA is an improved version of the NTMX82CA card which incorporates minor hardware changes in order to support the Loss Of Signal (LOS) alarm indication.

### Location

Four packlets fit in a quad frame carrier. The quad carrier frame occupies a standard size CPM slot. The quad frame carrier is NTMX87.

## Functional description

The NTMX82CA Dual PCM30 interface contains:

- application–specific integrated circuit (ASIC)
- Conference of European Postal and Telecommunications (CEPT) Administrations transceiver DS2181A
- line interface integrated circuit and power feed switching

### Application–specific integrated circuit (ASIC) functional blocks

The NTMX82CA has the following ASIC functional blocks:

- bidirectional serial interface between a DS60 line and two DS2181A PCM30 transceivers
- select the active DS60 line from own or mate DS60 according to an activity pin
- generate the 5.12 MHz and 2.56 MHz internal clocks and the 2.048 MHz system clock from the 10.24 MHz clock input
- generate synchronization pulses for the PCM30 transceiver and for the internal elastic buffer
- loopback for each timeslot—The ASIC extracts a timeslot from the outgoing PCM30 stream to the DS2181A transceiver. The ASIC inserts a timeslot in the incoming PCM30 stream. Each timeslot, except for timeslot 0, can loop back according to a software controlled register.

## **NTMX82CA** (continued)

- Message control channel—The ASIC provides a bidirectional interface for the DMSX message between the message pack and the host switch. The ASIC inserts the message received from the message pack on timeslot 1 or 16 of the outgoing PCM30 stream. In the opposite direction, the ASIC extracts the message received on timeslot 1 or 16. The ASIC sends the message to the message pack. The software selects timeslot 1 or 16 for the message channel.
- signaling buffer—The ASIC stores and inserts timeslot 16 of the incoming PCM30 stream. The ASIC inserts the timeslot as timeslot 16 in a specified frame of the 16–frame multiframe. The incoming PCM30 stream contains the signaling information. The signaling buffer operates when the Channel Associated Signaling mode is active.
- slip counter—The ASIC samples slip output of the internal elastic buffer. An 8–bit counter registers the number of slips.
- timeslot 0 odd—The ASIC detects an odd timeslot 0 out of the 16–frame multiframe. The ASIC sends the timeslot to the matrix pack. In the opposite direction, the ASIC controls the odd timeslot 0 the DS2181A transceiver sends.
- serial interface—A serial bidirectional interface controls each DS2181A transceiver. The ASIC accesses each register of the DS2181A in read/write or read–only mode.
- CRC4 error indication bits (E–bits)—These E–bits indicate sub–multiframes that contains errors. On the transmit side, the ASIC inserts two E–bits in the outgoing data stream. The hardware circuit or the software–loop register provide these bits. On the receive side, the ASIC extracts two E–bits from the incoming data stream. The ASIC inserts the E–bits in the odd register.
- E–bit count register (EBCR)—The EBCR register counts the E–bits received in the incoming data.
- facility data link (FDL)—This function creates a communication link. On the transmit side, the ASIC inserts FDL bits in the odd frames of the outgoing data. The FDL register provides the FDL bits. On the receive side, the ASIC inserts FDL bits in the FDL register. The odd frames of the incoming data provide the FDC bits.
- international bits (INB)—On the transmit side, the ASIC inserts INB in the odd and even frames of the outgoing data. The loop register provides the INB. On the receive side, the ASIC inserts the INB in the odd register. The odd and even frames of the incoming data provide the INB.

- blanking data interface—The ASIC inserts all ones in the channels (1–31) sent to the matrix, after loss of frame synchronization (RFSA=1).
- internal elastic store—There is an elastic store of two frames depth. The store slips on the frame boundary. The store has slip detection and control.

### Conference of European Postal and Telecommunications (CEPT) administrations transceiver DS2181A functional blocks

The NTMX82CA has the following CEPT transceiver DS2181A functional blocks:

- primary rate transceiver to execute International Telegraph and Telephone Consultative Committee (CCITT) standards
- supports cyclic redundancy check–4 (CRC4)–based framing standards
- supports common associated signaling (CAS) and common channel signaling (CCS) signaling standards
- contains on–chip alarm generation, alarm detection, and error logging logic
- operates with the DS2175 elastic store or with the internal elastic store in the ASIC

### Line interface integrated circuit functional blocks

The NTMX82CA has the following line interface integrated circuit functional blocks:

- wave shaping according to CCITT
- clock recovery
- CEPT input amplifier (with AGC)
- physical line driving and receiving
- input jitter attenuator

### Power feed switching functional blocks

The NTMX82CA has the following power feed switching functional blocks:

- power supply redundancy—the feed circuits change the power source from the own power supply to the mate power supply. This event occurs when the own power supply fails
- blown fuse indication—a special detection logic that detects and sets a bit if a fuse blows. The redundant fuses on the pack provides this feature.

## **NTMX82CA** (continued)

# Signaling

### Pin numbers

The pin numbers for the NTMX82CA appear in the following table.

**NTMX82CA pin numbers**

| Pin | A | B | C | D |
|---|---|---|---|---|
| 1 | GND | T1IN/C1 | T1INM/C1 | – |
| 2 | C97 | T1INM/P0 | T1OUT/P0 | – |
| 3 | –ACT | T1INM/P1 | T1OUT/P0 | – |
| 4 | C324 | T1INM/C0 | T1OUT/C0 | – |
| 5 | SENDT0 | +5VM | T1OUT/C1 | – |
| 6 | SENDR0 | FRPC1 | T1OUTM/P0 | – |
| 7 | SENDT1 | –FP48M | T1OUTM/P1 | – |
| 8 | SENDR1 | C324M | T1OUTM/C0 | – |
| 9 | RECT0 | P/–C | T1OUTM/C1 | – |
| 10 | RECR0 | –U0/U1 | MSGIN0 | – |
| 11 | RECT1 | +12V | MSGOUT | – |
| 12 | RECR1 | –12V | FPRC0 | – |
| 13 | C97M | +12VM | FPRC0M | – |
| 14 | T1IN/P0 | –12VM | FP48– | – |
| 15 | T1IN/91 | T1IN/C0 | – | – |
| 16 | GND | MSGEN | +5V | – |

***Note:*** Blank cells indicate pins that are not in use.

# Technical data

The dual PCM30 packlet consumes the following:

## Power requirements

The power requirements for the NTMX82CA appear in the following table.

**Power requirements**

| Voltage | Current |
|---|---|
| +5 V | 300 mA |
| +12 V | 3 mA |
| –48 V | —— |

## Environmental requirements

The environmental requirements for the NTMX82CA follows:

1. Ambient air temperature: <70 deg C
2. Relative humidity: 20–80% for short term; 20–55% normal

# NTMX87AA

## Product description

The Quad PCM Carrier (QPC) pack is a 3.048 m x 3.81 m (10 inch x 12.5 inch) frame that fits in dedicated slots in the CPM shelf. The QPC accepts four smaller packlets. These packlets plug into the QPC from the front of the QPC.

The QPC has a metal frame and five connectors where a printed circuit board (PCB) connects. The PCB contains AC terminal resistors. The PCB does not contain active components.

### Location

The NTMX87AA QPC pack fits slots 9, 12, 14, 16 and 19 in the main shelf. The QPC fits in the extension shelf in locations 4, 6, 8 and 19, 21, 23.

## Functional description

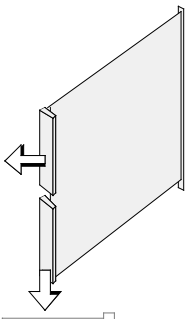
The QPC pack accepts a maximum of four packlets. These packlets are dual pulse code modulation (PCM) interface (DS–1 or 2 Mb) packlets. The QPC pack also accepts blank packlets in place of dual PCM packlets. The QPC pack allows addition, removal, and maintenance to dual PCM interface packlets.

## Signaling

### Pin numbers

The pin numbers for NTMX87AA appear in the following figure.

### NTMX87AA pin numbers



| | | A | B |
|---|---|---|---|
| 1A | 1B | GND | GND |
| 2A | 2B | +5V | +5V |
| 3A | 3B | +5V | +5V |
| 4A | 4B | +5V | +5V |
| 5A | 5B | GND | GND |
| 6A | 6B | | C97 |
| 7A | 7B | GND | GND |
| 8A | 8B | ACT- | C324 |
| 9A | 9B | | GND |
| 10A | 10B | SENDT0 | SENDR0 |
| 11A | 11B | | GND |
| 12A | 12B | SENDT1 | SENDR1 |
| 13A | 13B | GND | GND |
| 14A | 14B | SENDT2 | SENDR2 |
| 15A | 15B | | GND |
| 16A | 16B | SENDT3 | SENDR3 |
| 17A | 17B | C97M | |
| 18A | 18B | SENDT4 | SENDR4 |
| 19A | 19B | | |
| 20A | 20B | SENDT5 | SENDR5 |
| 21A | 21B | GND | GND |
| 22A | 22B | SENDT6 | SENDR6 |
| 23A | 23B | | |
| 24A | 24B | SENDT7 | SENDR7 |
| 25A | 25B | GND | GND |
| 26A | 26B | | |
| 27A | 27B | T1IN0M | T1IN0 |
| 28A | 28B | T1IN2M | T1IN2 |
| 29A | 29B | T1IN4M | T1IN4 |
| 30A | 30B | T1IN6M | T1IN6 |
| 31A | 31B | T1IN8M | T1IN8 |
| 32A | 32B | T1IN10M | T1IN10 |
| 33A | 33B | T1IN12M | T1IN12 |
| 34A | 34B | T1IN14M | T1IN14 |
| 35A | 35B | T1IN2M | T1IN2 |
| 36A | 36B | +5VM | |
| 37A | 37B | | C97M |
| 38A | 38B | +5VM | |
| 39A | 39B | -FP48M | |
| 40A | 40B | C324M | |

| | | A | B |
|---|---|---|---|
| 41A | 41B | | |
| 42A | 42B | | |
| 43A | 43B | | |
| 44A | 44B | | |
| 45A | 45B | T1IN6 | |
| 46A | 46B | P/-C | |
| 47A | 47B | T1OUT0M | T1OUT0 |
| 48A | 48B | T1OUT2M | T1OUT2 |
| 49A | 49B | T1OUT4M | T1OUT4 |
| 50A | 50B | T1OUT6M | T1OUT6 |
| 51A | 51B | T1OUT8M | T1OUT8 |
| 52A | 52B | T1OUT10M | T1OUT10 |
| 53A | 53B | T1OUT12M | T1OUT12 |
| 54A | 54B | T1OUT14M | T1OUT14 |
| 55A | 55B | -FP48 | T1IN6M |
| 56A | 56B | RECT0 | RECR1 |
| 57A | 57B | T1OUT0 | GND |
| 58A | 58B | RECT1 | RECR0 |
| 59A | 59B | GND | GND |
| 60A | 60B | RECT2 | RECR2 |
| 61A | 61B | T1OUT8 | |
| 62A | 62B | RECT3 | RECR3 |
| 63A | 63B | T1OUT10 | GND |
| 64A | 64B | RECT4 | RECR4 |
| 65A | 65B | T1OUT12 | GND |
| 66A | 66B | RECT5 | RECR5 |
| 67A | 67B | GND | GND |
| 68A | 68B | RECT6 | RECR6 |
| 69A | 69B | | |
| 70A | 70B | RECT7 | RECR7 |
| 71A | 71B | | GND |
| 72A | 72B | -U0/U1 | FPRC0M |
| 73A | 73B | FPRC1 | FPRC0 |
| 74A | 74B | +12VM | |
| 75A | 75B | MSGOUT0 | MSGIN0 |
| 76A | 76B | MSGOUT2 | MSGIN2 |
| 77A | 77B | +12V | +12VM |
| 78A | 78B | GND | GND |
| 79A | 79B | -12V | -12V |
| 80A | 80B | GND | GND |

## **NTMX87AA** (end)

# Technical data

### Power requirements

The NTMX87AA pack does not have any current requirements. The pack transfers the –5V and –12V from the backplane to the NTMX81 packlets.

# NTMX97AA

## Product description

The NTMX97AA recording–announcement processor (RAP) card contains devices that provide voice services. The RAP card controls these devices to perform the following functions:

- record the voice of the caller
- play back the voice to the operator
- detect dual–tone multifrequency (DTMF) tones

The NTMX97AA detects DTMF tones according to instructions from RAP input/output drivers. These drivers are in the integrated processor and F–bus interface (IPF).

### Location

The NTMX97AA fits in the front of the shelf at the NTMX99AA card position.

## Functional description

The NTMX97AA functions with the NTMX99AA in link interface shelves. The NTMX97AA provides the following functions:

- high storage density. The 24 Mbytes of storage holds 52.4 min of recorded speech that is not compressed.
- Motorola 68302 integrated multiprocessor (IMP) provides an easy, highly integrated central controller for all card functions
- 1 Mbyte static RAM for application software. The system stores speech data and application software separately.
- high–speed interface provides direct memory access of data from microcontroller system (MCS) memory to RAP speech memory
- all application software and announcements can be downloaded
- software allows announcement selection (access) to provide a flexible announcement structure
- the IMP maintenance functions monitor specified board activities to make sure hardware integrity occurs
- local terminal access for debugging that serial data link provides from the IMP

## **NTMX97AA** (continued)

### Functional blocks

The NTMX97AA has the following functional blocks:

- control block complex (CBC)
- expansion bus interface (EBI)
- speech memory (SMEM)

### Control block complex

The control block complex serves as the central intelligence for the RAP card. The control block complex controls and monitors all functions this card provides. The CBC is the bus master of the RAP processor bus (RPBUS). The CBC can arbitrate with the microcontroller system for ownership of the peripheral bus (PBUS).

The primary responsibilities of the CBC are the following:

- store, retrieve and maintain pointers to speech memory for recorded announcements and short–term stored speech
- schedule and execute tasks, like play announcement, record speech
- communicate with the microcontroller system through the message chip first in first out (FIFO)
- direct memory access (DMA) data among the different memory entities of the RAP card, like speech memory and system RAM
- DMA data between the microcontroller system memory and the RAP card
- arbitrate with microcontroller system for ownership of the PBUS
- provide a visual indication of card status (card fail LED)
- provide an asynchronous communications port for maintenance terminal access
- perform background maintenance tasks

### Expansion bus interface

The expansion bus interface provides the electrical interface between the IPF processor card and the RAP card. The EBI device has the drivers and receivers required to interface the signals from the backplane to the RAP card. The EBI device also has a message chip FIFO. The receivers of the EBI provide the least possible loading of the signals from the IPF. The receivers of the EBI provide least possible delay to the data path. The drivers of the EBI provide the high capacity, minimal delay buffers to the signals from the RAP to the IPF. The drivers of the EBI use a method like the method of the receivers of the EBI.

The order of the receivers and drivers in the EBI device is like the order of the functional signal grouping. The three primary groups of signals from the IPF are:

- the highway group (HWYGRP)
- the RAP processor bus (RPBUS)
- the element test and maintenance (ETM) bus

### Speech memory

The speech memory device provides the mass storage facilities that store recorded announcements and short–term stored subscriber speech. The dynamic RAM array can store 52.4 min of uncompressed, sequentially recorded subscriber voice data and nonhierarchical recorded announcements. The system stores subscriber voice data and recorded announcement data in the DRAM array with the same method. The system accesses these data types with the same method.

The speech memory device organizes speech data for announcements in a hierarchical manner to achieve the best use of memory. The device breaks announcements to subphrases and subphrases to speech blocks. Announcements can be of variable length. All speech blocks are of a standard size. The standard size of a speech block is 256 bytes and corresponds to 32 ms of speech. This order applies to announcements only. The system stores subscriber speech data in memory in a time sequence format. The system does not always store data in a contiguous way. All announcement and subscriber speech blocks are 256 bytes in length and 32 ms in duration.

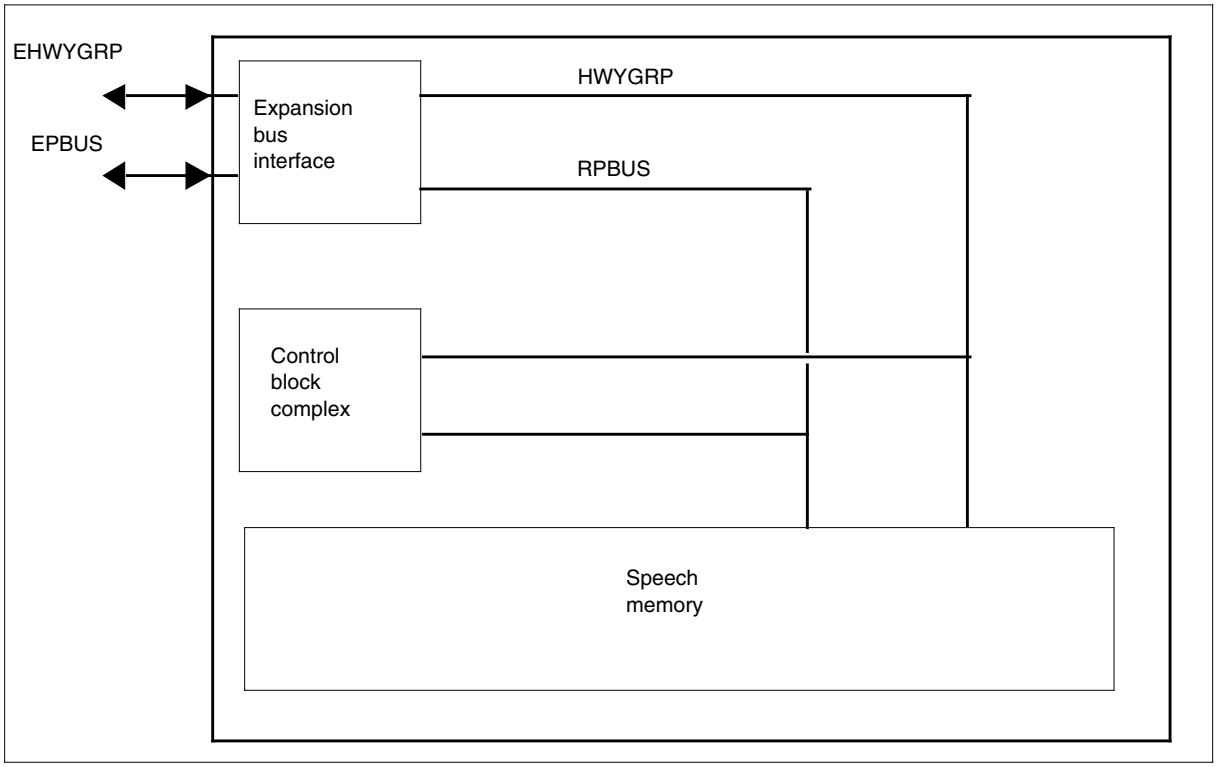
The speech memory device contains the following main components:

- 24MX9 dynamic RAM array
- 2KX16 dual port RAM
- XC3090 programmable gate array

The relationship between the functional blocks appears in the following diagram.

## **NTMX97AA** (continued)

**NTMX97AA functional blocks**




# Signaling

### Highway group bus

The highway group (HWYGRP) bus contains the parallel transmit and receive time division multiplexed (TDM) pulse–coded modulation (PCM) data links and associated clock and control signals. The system transmits PCM data to and from the RAP card through this bus. This PCM data is announcement and subscriber data.

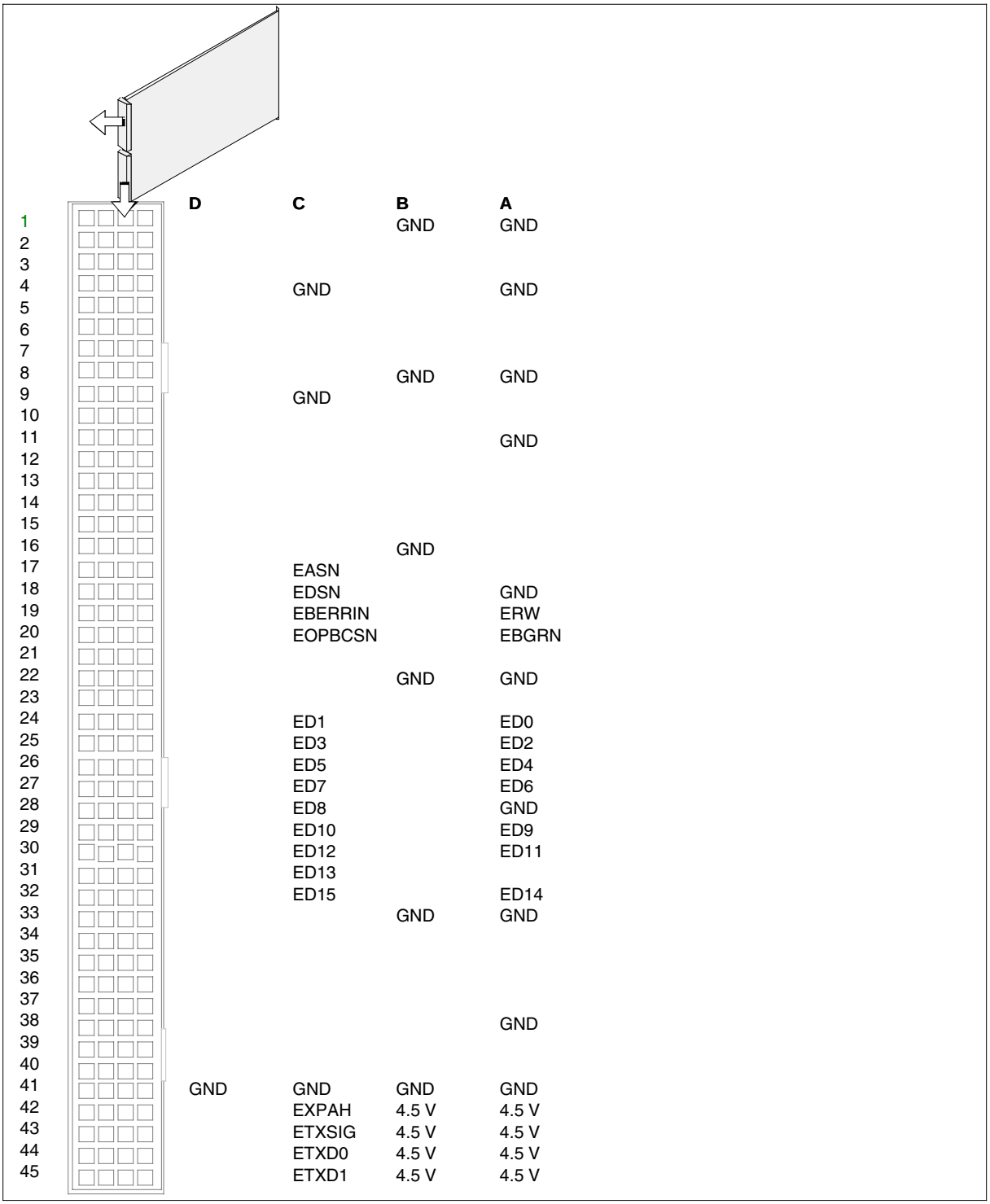
### Pin numbers

The pin numbers for connector P1 appear in the following figures.

### RAP processor bus

The RAP processor bus (RPBUS) contains different device selects and control signals. The RPBUS also contains the MC68302 processor address and data buses. As a group, these signals control the operation of the RAP card. Refer to the table that follows the pin numbers figures.

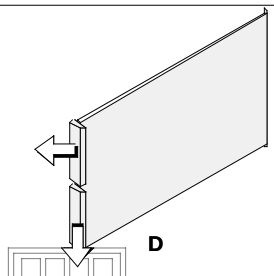
**NTMX97AA pin numbers (Part 1 of 2)**



| | D | C | B | A |
|---|---|---|---|---|
| 1 | | | GND | GND |
| 2 | | | | |
| 3 | | | | |
| 4 | | GND | | GND |
| 5 | | | | |
| 6 | | | | |
| 7 | | | | |
| 8 | | | GND | GND |
| 9 | | GND | | |
| 10 | | | | |
| 11 | | | | GND |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |
| 15 | | | | |
| 16 | | | GND | |
| 17 | | EASN | | |
| 18 | | EDSN | | GND |
| 19 | | EBERRIN | | ERW |
| 20 | | EOPBCSN | | EBGRN |
| 21 | | | | |
| 22 | | | GND | GND |
| 23 | | | | |
| 24 | | ED1 | | ED0 |
| 25 | | ED3 | | ED2 |
| 26 | | ED5 | | ED4 |
| 27 | | ED7 | | ED6 |
| 28 | | ED8 | | GND |
| 29 | | ED10 | | ED9 |
| 30 | | ED12 | | ED11 |
| 31 | | ED13 | | |
| 32 | | ED15 | | ED14 |
| 33 | | | GND | GND |
| 34 | | | | |
| 35 | | | | |
| 36 | | | | |
| 37 | | | | |
| 38 | | | | GND |
| 39 | | | | |
| 40 | | | | |
| 41 | GND | GND | GND | GND |
| 42 | | EXPAH | 4.5 V | 4.5 V |
| 43 | | ETXSIG | 4.5 V | 4.5 V |
| 44 | | ETXD0 | 4.5 V | 4.5 V |
| 45 | | ETXD1 | 4.5 V | 4.5 V |

# **NTMX97AA** (continued)

### NTMX97AA pin numbers (Part 2 of 2)



| | D | C | B | A |
|---|---|---|---|---|
| 46 | | ETXD2 | 4.5 V | 4.5 V |
| 47 | | ETXD3 | 4.5 V | 4.5 V |
| 48 | | ETXD4 | 4.5 V | 4.5 V |
| 49 | | ETXD5 | 4.5 V | 4.5 V |
| 50 | | ETXD6 | 4.5 V | 4.5 V |
| 51 | | ETXD7 | 4.5 V | 4.5 V |
| 52 | GND | GND | GND | GND |
| 53 | | EA1 | | EA0 |
| 54 | | EA3 | | EA2 |
| 55 | | EA5 | | EA4 |
| 56 | | EA7 | | EA6 |
| 57 | | EA9 | | EA8 |
| 58 | | EA11 | | EA10 |
| 59 | | EA12 | GND | GND |
| 60 | | EA14 | | EA13 |
| 61 | | EA16 | | EA15 |
| 62 | | EA18 | | EA17 |
| 63 | | EA20 | | EA19 |
| 64 | | EA22 | | EA21 |
| 65 | | EA23 | GND | GND |
| 66 | | | | |
| 67 | | ERXD0 | | |
| 68 | | ERXD2 | | ERXD1 |
| 69 | | ERXD4 | | ERXD3 |
| 70 | | ERXD6 | | ERXD5 |
| 71 | | ERXD7 | GND | GND |
| 72 | | | | |
| 73 | | ERXSIG | | ERXPAR |
| 74 | | | GND | |
| 75 | | | | |
| 76 | | EFPN | | EC61 |
| 77 | | EMRSTN | GND | GND |
| 78 | | | | |
| 79 | | | | ESINT0N |
| 80 | | | | GND |
| 81 | | | OPBROVN | |
| 82 | | EDSACK1N | | EDSACK0N |
| 83 | | EBGACKN | GND | GND |
| 84 | | | | |
| 85 | | ESIZE1 | | ESIZE0 |
| 86 | | EBREQN | | GND |
| 87 | | | | |
| 88 | | EFC1 | | EFC0 |
| 89 | | | | EFC2 |
| 90 | | | GND | GND |

The signal characteristics of the RAP card appear in the following table.

**RAP card signal description (Sheet 1 of 2)**

| Signal | Input/output | Description |
|---|---|---|
| EA0:EA23 | Input/output | Buffered MCS address lines |
| ED0:ED15 | Input/output | Buffered MCS data lines |
| EASN | Input/output | Buffered MCS address strobe |
| EDSN | Input/output | Buffered MCS data strobe |
| ERW | Input/output | Buffered MCS read/write |
| EDSACK0N | Input/output | Buffered MCS data transfer, size acknowledge |
| EDSACK1N | Input/output | Buffered MCS data transfer, size acknowledge |
| ESIZE0:ESIZE1 | Input/output | Buffered MCS size codes |
| EFC0:EFC2 | Input/output | Buffered MCS function codes |
| EBREQN | Output | Buffered MCS bus request |
| EBGRN | Input | Buffered MCS bus grant |
| EBGACKN | Output | Buffered MCS bus grant acknowledge |
| EBERRIN | Output | Buffered MCS bus error |
| EBEROUTN | Input | Buffered MCS bus error |
| ESINT0N | Output | Interrupt 0 signal to the MCS |
| ETXPAR | Output | Transmit data parity bit |
| ETXSIG | Output | Transmit data signaling bit |
| ETXD0:ETXD7 | Output | Transmit data (PCM) lines |
| ERXPAR | Input | Receive data parity bit |
| ERXSIG | Input | Receive data signaling bit |
| ERXD0:ERXD7 | Input | Receive data (PCM) lines |
| EC61 | Input | 16.384–MHz clock |

## **NTMX97AA** (end)

**RAP card signal description (Sheet 2 of 2)**

| Signal | Input/output | Description |
|---|---|---|
| EFPN | Input | 8–kHz frame pulse |
| EOPBCSN | Input | Card select |
| OPBPROVN | Output | Card presence signal |
| EMRSTN | Input | Master reset |
| TX | Output | Transmitted serial data |
| RX | Input | Received serial data |
| RTS | Output | Request to send |
| CTS | Input | Clear to send |
| TPRES– | Input | Terminal present |

# Technical data

### Power requirements

The nominal supply voltage is 5V.

# NTMX99AA

## Product description

The NTMX99AA provides the interface that allows the NTMX97AA recording-announcement processor (RAP) card inputs and outputs. This interface allows pulse coded modulation (PCM) audio information feed to and from the time-division multiplex (TDM) bus in the link interface shelf. The link interface shelf carries a maximum of 512 voice channels to and from the network interface unit (NIU).

### Location

The NTMX99AA plugs in the back of the shelf at the NTMX97AA card position.

## Functional description

The NTMX99AA operates with the NTMX97AA in link interface shelves. The NTMX99AA provides the following functions:

- RAP connectivity to network channels through a full duplex, 512 channel TDM bus
- a register-driven, memory-mapped interface. This interface gives the integrated processor and frame bus (FBUS) interface (IPF) control over channel allocation, parity reporting and loopbacks. This condition allows the IPF to monitor channel status.
- NIU selection for each channel. The activity bit received from each channel bus controller (CBC) over the channel bus (CBUS) supports this selection.
- duplicate RAP data driven on assigned channels to both CBUSs
- CBC with control over loopback for each channel. Allows the CBC to disable the channel bus interface (CBI) from either CBUS unit through control signals on the bus.
- a report on any CBUS errors to the CBC with a CBUS control signal
- optional network data format conversion that the software can configure. The format conversions include even bit inversion (EBI) and inversion or non-inversion of network data that passes to the RAP.

### Functional blocks

The NTMX99AA consists of the following functional blocks:

- CBUS interface and control
- peripheral bus (PBUS) interface
- PCM interface and control

## **NTMX99AA** (continued)

### CBUS interface and control

Each CBUS interface and control contains the circuits required to receive and drive signals on one CBUS unit. This interface is duplicated. Duplication reduces possible errors on one of the CBUS units that can cause both CBUSs to fail. Each unit interfaces to all of the signals on one of the two CBUSs.

This interface includes parity detection and generation for the CBUS and control signals that enable and disable the CBUS interface. Each interface contains an XILINX 3042 programmable logic cell array (PLCA). The PLCA controls all the functions required for the PCM data that passes between the CBUS and the PCMBUS of the RAP.

Inputs to these XILINX devices include the PCM data from the CBUS and the PCMBUS. Inputs also include control information in the PBUS registers and CBUS control information.

Outputs include the CBUS and PCMBUS outgoing PCM data, interrupt information, status information for the PBUS registers and timing signals. Each CBUS XILINX generates a channel control register in the PBUS interface.

### Peripheral bus (PBUS) interface

The PBUS interface contains all circuits required to interface with the IPF card over the PBUS. These circuits contain the CBI-512 ID programmable read-only memory (PROM) and dual-port random access memory (RAM). The RAM stores control registers for each channel. The circuits also contain global control and status registers. Each CBUS unit has a set of control registers for each channel. A single error does not affect both CBUS units with this condition. These two sets of control registers have the same address in memory. The IPF sees the control registers as one set of 512 registers. The interface contains an XILINX 3042 PLCA, which contains most of the PBUS control circuits as well as the interrupt generation. Power-up reset circuits are also in the interface.

### PCM interface and control

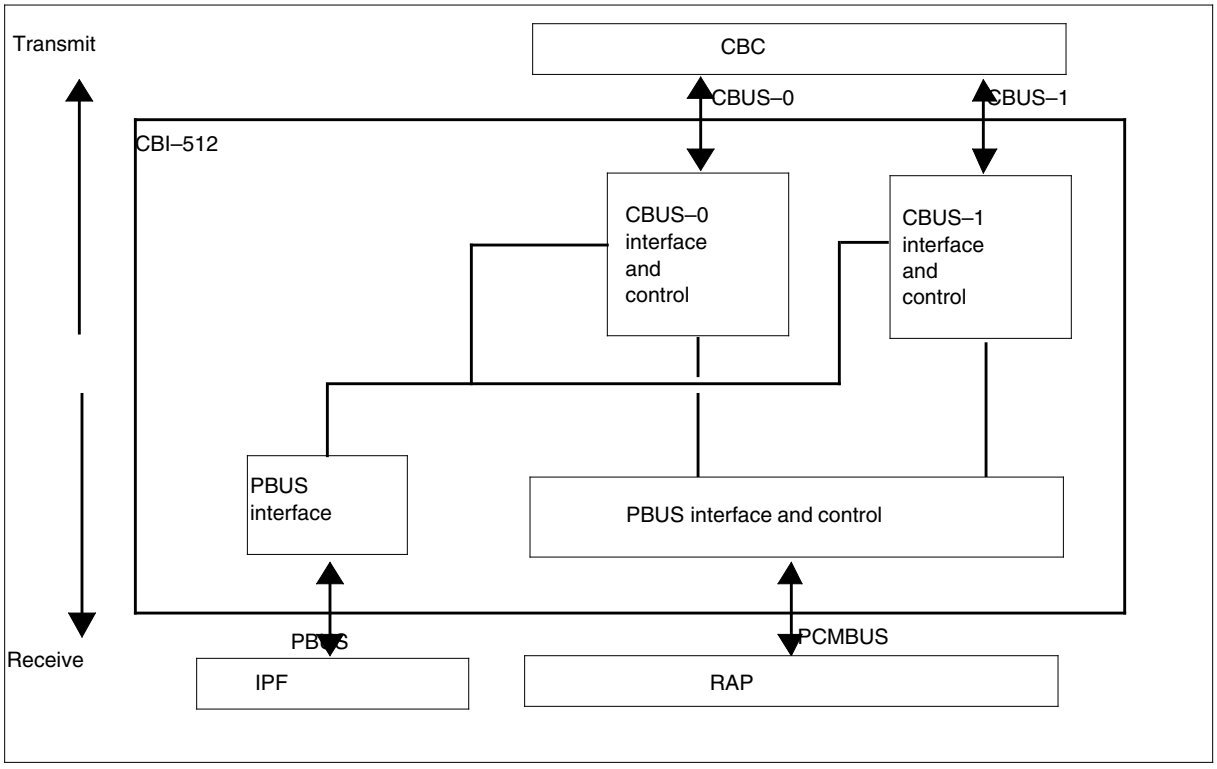
The PCM interface and control contains drivers for outgoing PCM data to the RAP card. The PCM interface and control contains a buffer for incoming PCM data from the RAP card. The system buffers PCM data and control information in the transmit direction (from the RAP card) in a synchronous delay-RAM. This condition allows the correct outgoing CBUS timing to occur. The system does not buffer PCM data in the receive direction (from the CBC). The system delays the PCM data two timeslots when the data passes through the PLCA devices and several latches. This PCM interface and control device takes CBUS data from the PLCAs of both the CBUS interface and control devices.

The PCM interface performs an NIU resolution based on the activity bit from each CBC. In the transmit direction (toward the CBC), the PCM interface device duplicates data from the RAP to both PLCAs. The PCM interface duplicates data to both CBUSs. Parity detection and generation circuits for the PCMBUS that connect to the RAP card are also present in this block. A loopback path for PCM data the software controls is available in each direction for fault isolation.

The PCM interface and control device contains a phase-locked loop circuit. The loop circuit generates a 16.384 MHz clock from the active CBUS unit 4.096 MHz clock. This device determines the active NIU based on the control signals received on each CBUS.

The relationship between the functional blocks appears in the following figure.

**NTMX99AA functional blocks**




## Signaling

### Loopbacks

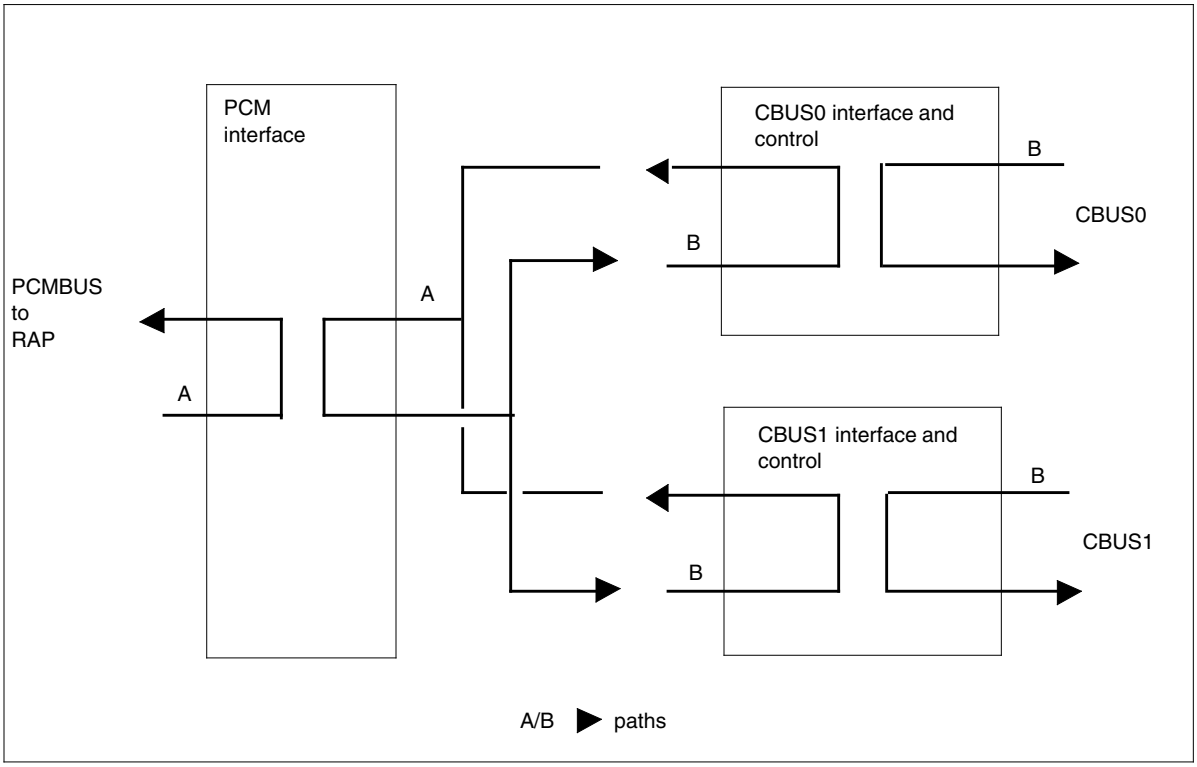
Different loopback paths for the network data are available on the CBI-512 card. Four loopbacks that the integrated processor and F-bus (IPF) controls are global. Two loopbacks are performed on each channel. A global loopback

## **NTMX99AA** (continued)

occurs on all network channels. The NIU controls one per-channel CBUS loopback with a control signal on the CBUS.

Loopbacks can occur in the PCM interface (path A) or in the CBUS interface (path B). Loopback paths that loop back data to the PCMBUS are local loopbacks. The IPF controls a global (all channel) loopback on each of the mutually exclusive paths A and B. Local loopbacks for each channel can occur with path A. Paths that loop back data to the CBUS are remote loopbacks. The IPF controls a global (all channel) loopback on each of the mutually exclusive paths A and B. Per-channel remote loopbacks occur on path B. The IPF or the NIU can control these loopbacks.

**NTMX99AA loopback paths**




### Pin numbers

The pin numbers for connector P1 appear in the following figures.

The tables that follow the figures list the signal characteristics of the CBUS, RAP interface, and PBUS. The characteristics appear in the sequence given.

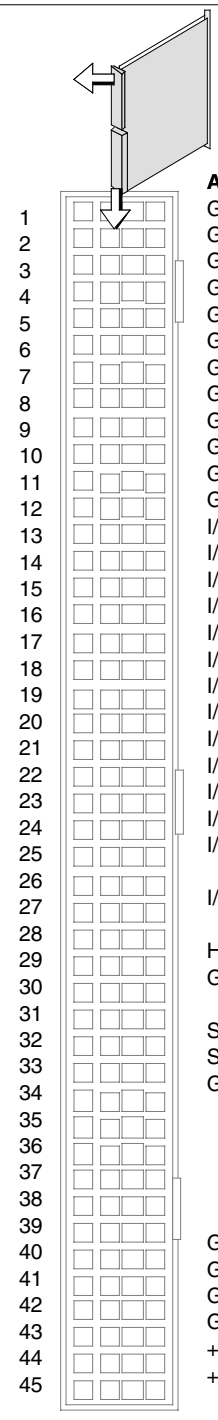
## Technical data

### Power requirements

The nominal supply voltage is 5V. The nominal ripple is 50mV route mean square (rms). The maximum supply current is 1.6A.

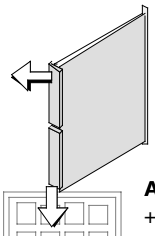
# **NTMX99AA** (continued)

### NTMX99AA pin numbers (Part 1 of 2 )



| | A | B | C | D |
|---|---|---|---|---|
| 1 | GND | | | |
| 2 | GND | | | |
| 3 | GND | | | |
| 4 | GND | | | |
| 5 | GND | | | |
| 6 | GND | | | |
| 7 | GND | | GND | GND |
| 8 | GND | | | |
| 9 | GND | | | |
| 10 | GND | GND | | |
| 11 | GND | | | |
| 12 | GND | | | |
| 13 | I/O 01 | | | |
| 14 | I/O 02 | | | |
| 15 | I/O 03 | | GND | GND |
| 16 | I/O 04 | | GND | GND |
| 17 | I/O 05 | | | PINT6– |
| 18 | I/O 06 | | | PINT7– |
| 19 | I/O 07 | | PINT2– | |
| 20 | I/O 08 | GND | PINT3– | |
| 21 | I/O 09 | | PINT4– | GND |
| 22 | I/O 10 | | PINT5– | |
| 23 | I/O 11 | | RMC– | RSTOUT– |
| 24 | I/O 12 | | PINT0– | PINT1– |
| 25 | I/O 13 | | BEN0– | BEN1– |
| 26 | | | BEN2– | BEN3– |
| 27 | I/O 15 | | | GND |
| 28 | | | GND | WRT– |
| 29 | HW4 | | DTACK– | EDTACK– |
| 30 | GND | | | |
| 31 | | | | |
| 32 | SH0 | | GND | |
| 33 | SH1 | | | DAS32– |
| 34 | GND | | | DATA00 |
| 35 | | | | DATA01 |
| 36 | | HW0 | ADDR02 | DATA02 |
| 37 | | HW1 | ADDR03 | DATA03 |
| 38 | | HW2 | ADDR04 | DATA04 |
| 39 | | HW3 | ADDR05 | DATA05 |
| 40 | GND | | ADDR06 | DATA06 |
| 41 | GND | | ADDR07 | DATA07 |
| 42 | GND | | ADDR08 | DATA08 |
| 43 | GND | | ADDR09 | DATA09 |
| 44 | +5V | PBRST– | ADDR10 | DATA10 |
| 45 | +5V | | ADDR11 | DATA11 |

**NTMX99AA pin numbers (Part 2 of 2 )**



| | A | B | C | D |
|---|---|---|---|---|
| 46 | +5V | DISSAN– | ADDR12 | DATA12 |
| 47 | +5V | GND | ADDR13 | DATA13 |
| 48 | +5V | | ADDR14 | DATA14 |
| 49 | +5V | | ADDR15 | DATA15 |
| 50 | +5V | GND | ADDR16 | DATA16 |
| 51 | +5V | C0TFP– | ADDR17 | DATA17 |
| 52 | +5V | C0TCLK | ADDR18 | DATA18 |
| 53 | +5V | GND | ADDR19 | DATA19 |
| 54 | +5V | C1TFP– | ADDR20 | DATA20 |
| 55 | +5V | C1TCLK | ADDR21 | DATA21 |
| 56 | | GND | ADDR22 | DATA22 |
| 57 | C0CBDR– | C1CBDR | –ADDR23 | DATA23 |
| 58 | C0CBLP– | C1CBLP– | ADDR24 | DATA24 |
| 59 | C0TD0– | C1TD0– | ADDR25 | DATA25 |
| 60 | C0TD1– | C1TD1– | ADDR26 | DATA26 |
| 61 | C0TD2– | C1TD2– | ADDR27 | DATA27 |
| 62 | C0TD3– | C1TD3– | ADDR28 | DATA28 |
| 63 | C0TD4– | C1TD4– | ADDR29 | DATA29 |
| 64 | C0TD5– | C1TD5– | ADDR30 | DATA30 |
| 65 | C0TD6– | C1TD6– | ADDR31 | DATA31 |
| 66 | C0TD7– | C1TD7– | | |
| 67 | C0TACT– | C1TACT– | | C0CDS– |
| 68 | C0TPAR | C1TPAR | | |
| 69 | C0RD0– | C1RD0– | GND | C0CDS– |
| 70 | C0RD1– | C1RD1– | | |
| 71 | C0RD2– | C1RD2– | | I/O 61 |
| 72 | C0RD3– | C1RD3– | | GND |
| 73 | C0RD4– | C1RD4– | | CLK244 |
| 74 | C0RD5– | C1RD5– | | GND |
| 75 | C0RD6– | C1RD6– | RES00 | CLK61 |
| 76 | C0RD7– | C1RD7– | RES01 | GND |
| 77 | C0RIND– | C1RIND– | RES02 | RXFP– |
| 78 | C0RPAR | C1RPAR– | RES03 | RXACT– |
| 79 | GND | I/O 17 | RES04 | RLP– |
| 80 | GND | TXACT– | RES05 | TXCNT– |
| 81 | GND | MBPST– | RES06 | PBPR– |
| 82 | GND | TXD0 | RES07 | RXD0 |
| 83 | GND | TXD1 | RES08 | RXD1 |
| 84 | GND | TXD2 | RES09 | RXD2 |
| 85 | GND | TXD3 | RES10 | RXD3 |
| 86 | GND | TXD4 | RES11 | RXD4 |
| 87 | GND | TXD5 | RES12 | RXD5 |
| 88 | GND | TXD6 | RES13 | RXD6 |
| 89 | GND | TXD7 | RES14 | RXD7 |
| 90 | GND | TXPAR | RES15 | RXPAR |

## **NTMX99AA** (continued)

| Signal | Input/output | Description |
|---|---|---|
| CxTCLK | Input | CBUS clock (4.096 MHz) |
| CxTFP- | Input | CBUS frame pulse |
| CxCBLP- | Input | CBI loopback |
| CxCDS- | Input | CBI disable |
| CxTD0-:CxTD7- | Input | CBUS transmit data |
| CxTACT- | Input | CBC activity bit |
| CxTPAR | Input | CBUS transmit parity |
| CxCBIDR- | Output | CBI driving |
| CxRD0-:CxRD7 | Output | CBUS receive data |
| CxRIND- | Output | Receive indicator |
| CxRPAR | Output | CBUS receive parity |

***Note:*** For the CBUS signals, transmit refers to the data that goes from the CBC toward the CBI, and receive refers to the data from the CBI toward the CBC.

**(Sheet 1 of 2)**

| Signal | Input/output | Description |
|---|---|---|
| TXACT- | Input | Transmit data activity |
| TXD0:TXD7 | Input | Transmit data |
| TXPAR | Input | Transmit data parity |
| RXFP- | Output | Receive frame pulse |
| RXACT- | Output | Receive data activity |
| RXD0:RXD7 | Output | Receive data |
| RXPAR | Output | Receive data parity |
| RLP- | Output | Remote loopback status signal |

***Note:*** For RAP signals and all other internal CBI signals, receive refers to data that passes from the CBI to the RAP. Transmit refers to data that passes from the RAP to the CBI. These conditions do no apply to the CBUS signals.

**(Sheet 2 of 2)**

| Signal | Input/output | Description |
|---|---|---|
| TXCNT- | Output | Transmit contention status signal |
| CLK224 | Output | 4.096 MHz clock |
| CLK61 | Output | 16.384 MHz clock |
| IO01:IO13 | Input/output | Unused |
| IO15,IO17 | Input/output | Unused |
| IO61 | Input/output | Unused |
| RES00:RES15 | Input/output | Unused |

***Note:*** For RAP signals and all other internal CBI signals, receive refers to data that passes from the CBI to the RAP. Transmit refers to data that passes from the RAP to the CBI. These conditions do no apply to the CBUS signals.

**(Sheet 1 of 2)**

| Signal | Input/output | Description |
|---|---|---|
| BEN0-:BEN3- | Input | Processor byte enablers |
| DAS32- | Input | Processor address strobe |
| ADDR02:ADDR31 | Input | Processor address lines |
| DATA00:DATA15 | Input/output | Processor data lines (only least significant 16 bits used) |
| WRT- | Input | Processor read/write- |
| RMC- | Input | Processor read-modify-write |
| DTACK- | Input/output | Processor data transfer acknowledge |
| EDTACK- | Input/output | Processor data transfer acknowledge |
| PINT0-:PINT7- | Input | Processor interrupt lines |
| PBRST- | Input | Master reset from backplane |
| RSTOUT- | Input | Master reset from IPF |

## **NTMX99AA** (end)

**(Sheet 2 of 2)**

| Signal | Input/output | Description |
|---|---|---|
| MBPST- | Input | Motherboard presence signal |
| HW0:HW4 | Input | Physical slot address |
| SH0:SH1 | Input | Logical shelf address |
| PBPR- | Output | Paddleboard presence signal |

# 11 NTNPnnaa

## NTNP20AA through NTNP50AA

# NTNP20AA

## Product description

The NTNP20AA Power input / output (I/O) card provides filtering of talk battery A/B and signal battery A/B feeds. The NTNP20AA has the following characteristics:

- contains a heavy 8-pin D-sub connector through which power to the UE9000 shelf are fed
- contains the shelf Id PROM, which stores shelf manufacturing and operating history
- provides the connector receptacles for the shelf to accept signal and talk battery supplies and returns
- controls both differential and common mode electromagnetic interference (EMI) / electromagnetic compatibility (EMC) conducted and radiated emissions and helps to inhibit any additional EMI / EMC which may couple onto the power feeds across the backplane

### Location

The NTNP20AA resides in the lower half of slot 0 in the UE9000 shelf.

## Functional description

### Functional blocks

NTNP20AA includes the functional blocks that follow:

- signal battery filter
- talk battery filter

#### Signal battery filter

Signal battery is the primary power source for the UE9000 shelf. In addition to the filtering provided by other power supplies in the shelf, the NTNP20AA uses decoupling capacitors from the signal battery feeds to frame ground and logic ground to inhibit common mode noise on the bus.

#### Talk battery filter

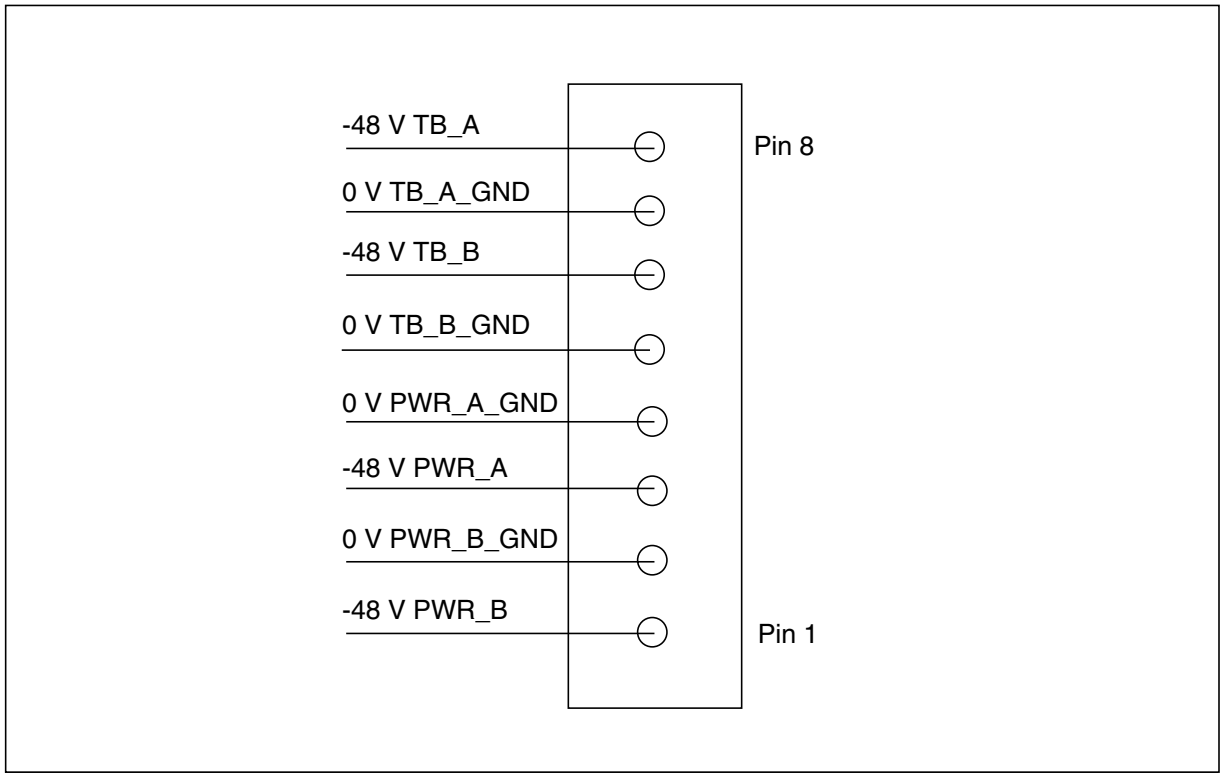
The talk battery feeds into the UE9000 shelf are provided as tip / ring power source for the line cards in the system. While the line cards are responsible for inhibiting noise resulting from ringing, the NTNP20AA uses decoupling capacitors across the feeds to inhibit differential noise on the bus.

# Signaling

## Pin outs

The figure that follows shows the pin outs for NTNP20AA.

**NTNP20AA connector pin outs**




# Technical data

## Power requirements

The NTNP20AA has the following power requirements

- -40 V minimum
- -48 V nominal
- -60 V maximum

# NTNP32AA

## Product description

The NTNP32AA, UE9000 ATM Control card (ACC) is the ATM network interface for the UE9000 shelf. The ACC card

- interfaces multiple data carrying line cards to single inverse multiplexer for ATM (IMA) interface
- performs a number of traffic flow control functions

The ACC card communicates with the ATM network through an eight DS-1 link IMA interface

### Location

The NTNP32AA resides in the ATM control card slots 9 and 10 of the UE9000 shelf.

## Signaling

### Pin outs

The figure that follows shows the pin outs for NTNP32AA.

**NTNP32AA type A connector pin outs**

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | ATMUSP02/N02 | ATMUSP02/N02 | GND | ATMUSP21/N21 | ATMUSP21/N21 |
| 2A 2B 2C 2D 2E | GND | GND | GND | GND | GND |
| 3A 3B 3C 3D 3E | ATMDSP02/N02 | ATMDSP02/N02 | GND | ATMDSP21/N21 | ATMDSP21/N21 |
| 4A 4B 4C 4D 4E | GND | GND | GND | GND | GND |
| 5A 5B 5C 5D 5E | ATMUSP03/N03 | ATMUSP03/N03 | GND | ATMUSP20/N20 | ATMUSP20/N20 |
| 6A 6B 6C 6D 6E | GND | GND | GND | GND | GND |
| 7A 7B 7C 7D 7E | ATMDSP03/N03 | ATMDSP03/N03 | GND | ATMDSP20/N20 | ATMDSP20/N20 |
| 8A 8B 8C 8D 8E | GND | GND | GND | GND | GND |
| 9A 9B 9C 9D 9E | ATMUSP04/N04 | ATMUSP04/N04 | GND | ATMUSP19/N19 | ATMUSP19/N19 |
| 10A 10B 10C 10D 10E | GND | GND | GND | GND | GND |
| 11A 11B 11C 11D 11E | ATMDSP04/N04 | ATMDSP04/N04 | GND | ATMDSP19/N19 | ATMDSP19/N19 |
| 12A 12B 12C 12D 12E | GND | GND | GND | GND | GND |
| 13A 13B 13C 13D 13E | ATMUSP05/N05 | ATMUSP05/N05 | GND | ATMUSP18/N18 | ATMUSP18/N18 |
| 14A 14B 14C 14D 14E | GND | GND | GND | GND | GND |
| 15A 15B 15C 15D 15E | ATMDSP05/N05 | ATMDSP05/N05 | GND | ATMDSP18/N18 | ATMDSP18/N18 |
| 16A 16B 16C 16D 16E | GND | GND | GND | GND | GND |
| 17A 17B 17C 17D 17E | ATMUSP06/N06 | ATMUSP06/N06 | GND | ATMUSP17/N17 | ATMUSP18/N18 |
| 18A 18B 18C 18D 18E | GND | GND | GND | GND | GND |
| 19A 19B 19C 19D 19E | ATMDSP06/N06 | ATMDSP06/N06 | GND | ATMDSP17/N17 | ATMDSP17/N17 |
| 20A 20B 20C 20D 20E | GND | GND | GND | GND | GND |
| 21A 21B 21C 21D 21E | ATMUSP07/N07 | ATMUSP07/N07 | GND | ATMUSP16/N16 | ATMUSP16/N16 |
| 22A 22B 22C 22D 22E | GND | GND | GND | GND | GND |
| 23A 23B 23C 23D 23E | ATMDSP07/N07 | ATMDSP07/N07 | GND | ATMDSP16/N16 | ATMDSP16/N16 |
| 24A 24B 24C 24D 24E | GND | GND | GND | GND | GND |
| 25A 25B 25C 25D 25E | ATMUSP08/N08 | ATMUSP08/N08 | GND | ATMUSP15/N15 | ATMUSP15/N1 |

### NTNP32AA type B connector pin outs

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | GND | GND | GND | GND | GND |
| 2A 2B 2C 2D 2E | ATMDSP08/N08 | ATMDSP08/N08 | GND | ATMDSP15/N15 | ATMDSP15/N15 |
| 3A 3B 3C 3D 3E | GND | GND | GND | GND | GND |
| 4A 4B 4C 4D 4E | ATMUSP09/N09 | ATMUSP09/N09 | GND | ATMUSP14/N14 | ATMUSP14/N14 |
| 5A 5B 5C 5D 5E | GND | GND | GND | GND | GND |
| 6A 6B 6C 6D 6E | ATMDSP09/N09 | ATMDSP09/N09 | GND | ATMDSP14/N14 | ATMDSP14/N14 |
| 7A 7B 7C 7D 7E | GND | GND | GND | GND | GND |
| 8A 8B 8C 8D 8E | ATMUSP12/N12 | ATMUSP12/N12 | GND | ATMUSP13/N13 | ATMUSP13/N13 |
| 9A 9B 9C 9D 9E | GND | GND | GND | GND | GND |
| 10A 10B 10C 10D 10E | ATMUSP12/N12 | ATMUSP12/N12 | GND | ATMUSP13/N19 | ATMUSP13/N13 |
| 11A 11B 11C 11D 11E | GND | GND | GND | GND | GND |
| 12A 12B 12C 12D 12E | | | | | |
| 13A 13B 13C 13D 13E | | | | | |
| 14A 14B 14C 14D 14E | | | | | |
| 15A 15B 15C 15D 15E | GND | GND | GND | GND | GND |
| 16A 16B 16C 16D 16E | ATM03ACT | ATM02ACT | GND | ATM21ACT | ATM20ACT |
| 17A 17B 17C 17D 17E | ATM05ACT | ATM04ACT | GND | ATM19ACT | ATM18ACT |
| 18A 18B 18C 18D 18E | ATM07ACT | ATM06ACT | GND | ATM17ACT | ATM16ACT |
| 19A 19B 19C 19D 19E | ATM09ACT | ATM08ACT | GND | ATM15ACT | ATM14ACT |
| 20A 20B 20C 20D 20E | GND | ATM12ACT | GND | ATM13ACT | GND |
| 21A 21B 21C 21D 21E | | GND | GND | GND | |
| 22A 22B 22C 22D 22E | | PLANSEL0 | GND | PLANSEL1 | PLANSEL2 |
| 23A 23B 23C 23D 23E | GND | GND | GND | GND | GND |
| 24A 24B 24C 24D 24E | ATM-BP/BN | ATM-BP/BN | GND | ATM-AP/AN | ATM-AP/AN |
| 25A 25B 25C 25D 25E | GND | GND | | GND | GND |

### NTNP32AA type C connector pin outs

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | | ATMA_ACT0/1 | GND | ATMA_ACT0/1 | GND |
| 2A 2B 2C 2D 2E | | ATMB_ACT0/1 | GND | ATMB_ACT0/1 | GND |
| 3A 3B 3C 3D 3E | PLLA-A_B/A | GND | PLLT-A_B | GND | PLLA-A_B/A |
| 4A 4B 4C 4D 4E | GND | FPA-A_B/A | GND | FPA-A_B/A | GND |
| 5A 5B 5C 5D 5E | PLLT-A_A | GND | FPT-A_B | GND | PLLA-T_A |
| 6A 6B 6C 6D 6E | GND | FPT-A_A | GND | FPA-T_A | GND |
| 7A 7B 7C 7D 7E | GLANADS10 | GND | GND | GND | GLANAUS10 |
| 8A 8B 8C 8D 8E | GND | GLANBUS10 | GND | GLANBDS10 | GND |
| 9A 9B 9C 9D 9E | TDMAUS10/BUS10 | GND | GND | GND | TDMAUS10/BUS10 |
| 10A 10B 10C 10D 10E | GND | CLKA10/B10 | GND | CLKA10/B10 | GND |
| 11A 11B 11C 11D 11E | TDMADS10/BDS10 | GND | GND | GND | TDMADS10/BDS10 |

### NTNP32AA power connector pin outs

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | | BA -48 A | SBA -48 A | SBA -48 A | SBA -48 A |
| 2A 2B 2C 2D 2E | | SBRTN | SBRTN | SBRTN | SBRTN |
| 3A 3B 3C 3D 3E | | SBB -48 B | SBB -48 B | SBB -48 B | SBB-48B |

# **NTNP32AA** (continued)

### NTNP32AA DS-1 IMA connector pin outs

| | | | |
|---|---|---|---|
| 1 | Line 1 TXRING | 26 | |
| 2 | Line 1 TXTIP | 27 | |
| 3 | Line 0 TXTIP | 28 | Line 2 RXRING |
| 4 | Line 7 TXRING | 29 | Line 1 RXTIP |
| 5 | Line 7 TXTIP | 30 | Line 0 RXRING |
| 6 | Line 6 TXRING | 31 | Line 3 TXTIP |
| 7 | | 32 | Line 2 TXTIP |
| 8 | | 33 | |
| 9 | Line 5 RXRING | 34 | Line 5 TXTIP |
| 10 | Line 4 RXRING | 35 | |
| 11 | Line 4 RXTIP | 36 | Line 4 TXRING |
| 12 | Line 7 RXRING | 37 | |
| 13 | Line 7 RXTIP | 38 | |
| 14 | Line 6 RXRING | 39 | |
| 15 | Line 6 RXTIP | 40 | Line 3 RXRING |
| 16 | Line 3 TXRING | 41 | Line 3 RXTIP |
| 17 | Line 2 TXRING | 42 | Line 2 RXTIP |
| 18 | Line 0 TXRING | 43 | Line 1 RXRING |
| 19 | Line 5 TXRING | 44 | Line 0 RXTIP |
| 20 | | | |
| 21 | Line 4 TXTIP | | |
| 22 | Line 6 TXTIP | | |
| 23 | | | |
| 24 | | | |
| 25 | Line 5 RXTIP | | |

### NTNP32AA ethernet connector pin outs

| | |
|---|---|
| 1 | TX+ |
| 2 | TX- |
| 3 | RX+ |
| 4 | |
| 5 | |
| 6 | RX- |

### NTNP32AA RS232 connector pin outs

| | |
|---|---|
| 1 | |
| 2 | RX |
| 3 | TX |
| 4 | |
| 5 | GND |
| 6 | |

# Technical data

## Power requirements

The NTNP32AA has the following power requirements

- -40 V minimum
- -48 V nominal
- -60 V maximum

# NTNP44AA

## Product description

The NTNP44AA Combo 4+4 ADSL-DMT line card

- is a voice and data interface to the subscriber loop for the Universal Edge 9000 (UE9000)
- terminates four subscriber loop pairs for analog voice telephone service and standard compliant ADSL-DMT ATM data services.

### Location

The NTNP44AA can reside in any of slots 0-7 and 8-15 in the UE9000 shelf.

## Functional description

The NTNP44AA terminates four fully compliant ADSL DMT subscriber loops. Each loop interface has a splitter circuit to either separate or join the lifeline voice service with the value-added ATM data cell traffic for the subscriber. The voice traffic routes to the TDM common equipment cards through the Memphis ASIC. The data traffic routes to the ATM common equipment card.

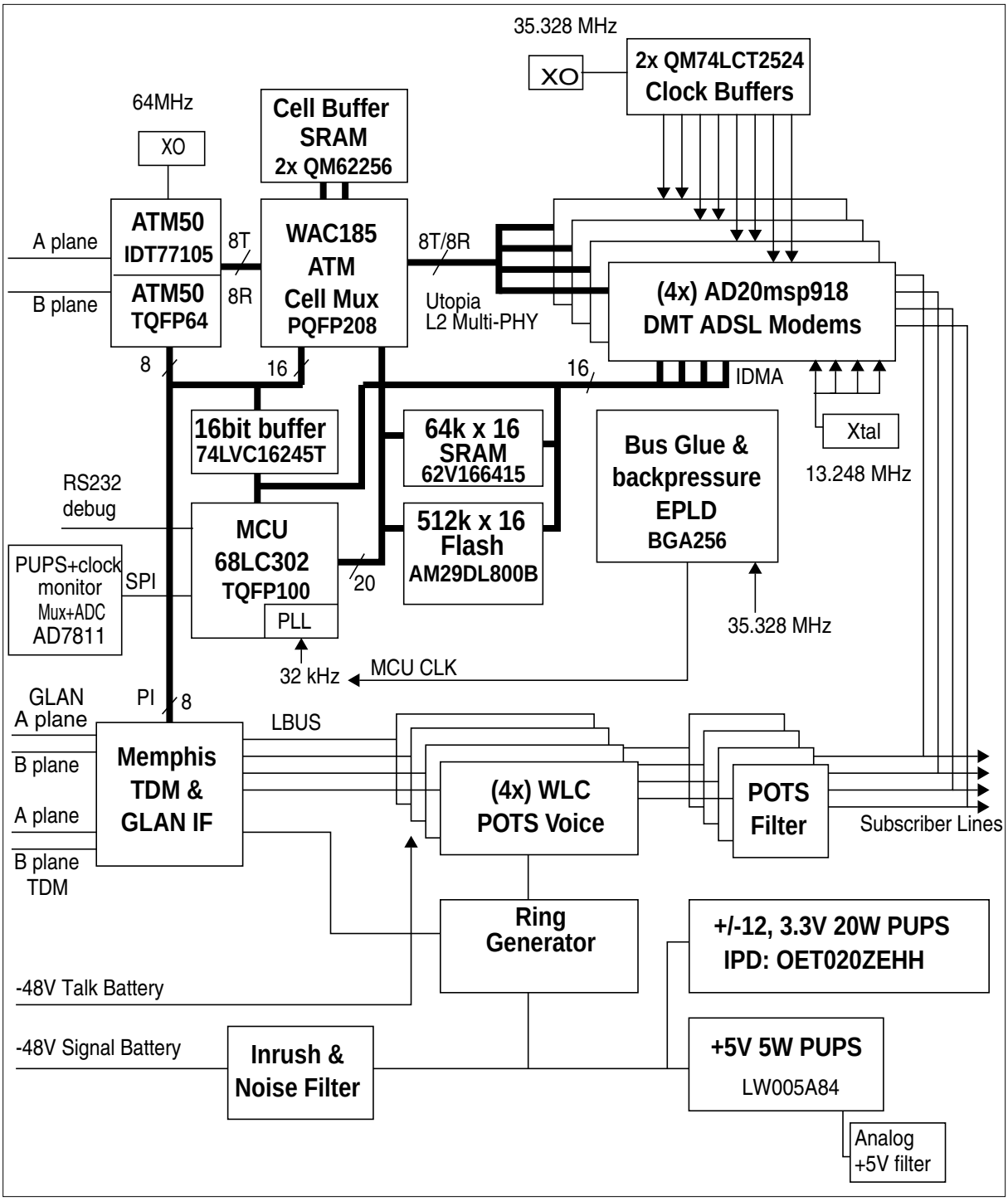
### Functional blocks

The NTNP44AA includes the functional blocks that follow:

- ATM ADSL and control
- TDM voice
- power supplies

The figure that follows shows the relationship of the functional blocks.

**NTNP44AA functional blocks**



## NTNP44AA (continued)

### ATM ADSL and control

The ATM ADSL subsystem transports cells between the ATM switch card and all the ADSL modems on the card through a backplane serial link and an ATM cell multiplexer chip. The ATM serial link to the backplane is redundant.

### TDM voice

The POTS voice circuits support four circuits

### Power supplies

The line card is powered from -48 V signal battery. Two 48 V point-of-use power supplies (PUPS) provide the following voltages for the card:

- single 5 V, 5 W output
- triple +/- 12 V and +3.3 V, 20 W output

# Signaling

## Pin outs

The figures that follow shows the pin outs for NTNP44AA.

**NTNP44AA connector P1 pin outs**

| | |
|---|---|
| 1 | RING0 |
| 2 | RING1 |
| 3 | RING2 |
| 4 | RING3 |
| 5 | |
| 6 | |
| 7 | |
| 8 | |
| 9 | |
| 10 | |
| 11 | |
| 12 | |
| 13 | |
| 14 | |
| 15 | |
| 16 | |
| 17 | |
| 18 | |
| 19 | |
| 20 | |
| 21 | |
| 22 | |
| 23 | |
| 24 | |
| 25 | |
| 26 | TIP0 |
| 27 | TIP1 |
| 28 | TIP2 |
| 29 | TIP3 |

**NTNP44AA connector P2 pin outs**

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | ATMAUSP02 | ATMAUSN02 | GND | ATMBUSNP02 | ATMBUSNP02 |
| 2A 2B 2C 2D 2E | GND | GND | GND | GND | GND |
| 3A 3B 3C 3D 3E | ATMADSP02 | ATMADSN02 | GND | ATMBDSP02 | ATMBDSN02 |
| 4A 4B 4C 4D 4E | GND | GND | GND | GND | GND |
| 5A 5B 5C 5D 5E | SLOT-IDO | ATMA_ACT | GND | ATMB_ACT | GND |
| 6A 6B 6C 6D 6E | SLOT-ID1 | PLANASEL0 | GND | PLANASEL1 | PLANASEL2 |
| 7A 7B 7C 7D 7E | GLANADS02 | SLOTID3 | GND | SLOT-ID4 | GLANBUS02 |
| 8A 8B 8C 8D 8E | SLOT-ID2 | GLANAUS02 | GND | GLANBDS02 | IDP |
| 9A 9B 9C 9D 9E | TDMAUS02 | GND | PROW | GND | TDMBUS02 |
| 10A 10B 10C 10D 10E | GND | CLKA02 | GND | CLKB02 | GND |
| 11A 11B 11C 11D 11E | TDMADS02 | GND | PCOL | GND | TDMBDS02 |
| 12A 12B 12C 12D 12E | | | | | |
| 13A 13B 13C 13D 13E | | | | | |
| 14A 14B 14C 14D 14E | | | | | |
| 15A 15B 15C 15D 15E | TDMAUS03 | GND | GND | GND | TDMBUS02 |
| 16A 16B 16C 16D 16E | GND | GND | GND | GND | GND |
| 17A 17B 17C 17D 17E | TDMADS03 | NC | NC | NC | TDMBDS03 |
| 18A 18B 18C 18D 18E | NC | TBRTN | NC | TB | NC |
| 19A 19B 19C 19D 19E | TBRTN | TBRTN | NC | TB | TB |
| 20A 20B 20C 20D 20E | TBRTN | TBRTN | NC | TB | TB |
| 21A 21B 21C 21D 21E | TBRTN | TBRTN | NC | TB | TB |
| 22A 22B 22C 22D 22E | | | | | |
| 23A 23B 23C 23D 23E | TB1_AIT | TB1_AIR | NC | TB1_AOT | TB1_AOR |
| 24A 24B 24C 24D 24E | | | | | |
| 25A 25B 25C 25D 25E | TB2_AIT | TB2_AIR | NC | TB2_AOT | TB2_AOR |

**NTNP44AA connector P3 pin outs**

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | | SBA -48 V SBRTN | SBA -48 V SBRTN | SBA -48 V SBRTN | SBA -48 V SBRTN |
| 2A 2B 2C 2D 2E | | | | | |
| 3A 3B 3C 3D 3E | | | | | |

# Technical data

## Power requirements

The NTNP44AA has the following power requirements

- 42 V minimum
- 48 V nominal
- 56 V maximum

# NTNP50AA

## Product description

The NTNP50AA POTS 32 Multi-circuit Line Card (POTS32) is a line card module used in the Universal Edge 9000 (UE9000).

### Location

The NTNP50AA POTS 32 line card resides in any of slots 0-7 and 8-15 in the UE9000 shelf.

## Functional description

The NTNP50AA POTS Multi circuit line card (POTS 32)

- uses the single in line package version of the World Line Card
- serves 32 subscriber loops
- has an onboard point-of-use power supply (PUPS) that generates dc voltages required to power the electronics from a -48 V power distribution on the backplane
- has an onboard ringing generator pre-set to ring at 20 Hz superimposed on -48 V dc
- is compatible with terminal sets with input and balance impedance according to North American standards
- is protected from electronic overvoltage in hostile electrical environments
- includes software selectable loop feed current limit characteristics with software selectable automatic loss equalization for short loops
- has two test-in / test-out busses, test bus 1 and test bus 2, and each subscriber interface circuit can access either bus
- has a hold clip circuit that allows the UE9000 shelf to place all loop interface circuits into protection. This allows the circuits to be removed from any external voltages.
- has an interface to the backplane through the Memphis line card interface application-specific integrated circuit (ASIC)
- has a Grace LAN (GLAN) bus, which is a three-wire serial interface (clock, downstream data, and upstream data) which provides control oriented information

### Functional blocks

NTNP50AA includes the functional blocks that follow:

- supervision
- transmission

- overvoltage protection
- B11 overcurrent protection
- relays
- WLC single in-line package (SIP) modules
- point-of-use power supply (PUPS)
- ringing generator
- talk battery and signal battery current limiting

### Supervision

The supervision block includes loop detection, ringing supervision, a loop current limiting function, and dial pulse detection.

### Transmission

The transmission block includes loop termination, voice path, hybrid balance, equalization loss pads, and analog-to-digital and digital-to-analog conversion of the voice frequency signal.

### Overvoltage protection

The overvoltage protection block increases the survivability of the card in hostile electrical environments.

### B11 overcurrent protection

The B11 overcurrent protection block protects against ground faults on the ring lead and against short circuits between the tip and ring leads by sensing the condition and limiting the current that can flow in the ring to a value that will not cause the line card any damage.

### Relays

The relays block includes the following relays.

- The test-in relay in each line interface circuit allows access to the tip and ring for circuit testing purposes.
- The test-out relay in each line interface circuit allows bridging access to the tip and ring for loop testing purposes.
- The cutover / protection relay is used to isolate a subscriber loop interface circuit from the loop and is used for a variety of purposes such as line circuit protection from hazardous potentials, diagnostics, and office installation.
- The ringing relay connects the ringing generator output to the line circuit tip and ring in conjunction with office talk battery to ring the telephone connected to a subscriber loop interface circuit.

## NTNP50AA (continued)

### WLC single in-line package (SIP) module

The WLC SIP module block includes a loop interface circuit and a 5 V regulator. There is one module for each subscriber for a total of 32 modules on each NTNP50AA card.

### PUPS

The PUPS block supplies +3.3 V, +5 V, +10 V, and +15 V outputs to the card from a -48 V input to reduce the number of backplane pins and simplify backplane cabling.

### Ringing generator

The ringing generator block provides ringing voltage to the line circuits. Having a ringing generator on each line card reduces the number of backplane pins and simplifies backplane cabling. The following table lists the characteristics of the on board ringing generator.

**Ringing generator characteristics**

| Characteristic | Value | Purpose |
|---|---|---|
| Input | -48 V | Input power |
| Output | 86 Vrms at nominal 20 Hz, superimposed on a dc offset equal to the talk battery voltage | Ringing voltage output. The ringing generator is capable of ringing 15 VA or 15 REN (ringing equivalent number) at the shortest loop length. |
| | Frequency selective ringing (FSR) | |
| | Frequencies of 25 Hz or 50 Hz are software selectable | Alternate output frequencies |
| Zero crossing indicator | | Indicates the output dc voltage zero crossing to prolong life of ringing relays |
| dc feed resistance | 205 Ω nominal | |

### Talk battery and signal battery current limiting

The talk battery and signal battery current limiting block performs the following:

- Talk battery current is limited to approximately 1.6 A. This circuit operates in the presence of a lightning strike to ensure that excess energy is shunted to ground, not to talk battery.
- Signal battery current is limited by a soft-start circuit. This circuit limits the current inrush during hot-swap.
- Lightning protection technology designed to meet first level lightning surge requirements up to 2 kV and all second level lightning surge requirements. In addition, each line circuit has a unidirectional clamping device to protect each circuit from arcing across test bus relays.

## Signaling

This section identifies the pin-out information for the NTNP50AA.

## NTNP50AA (continued)

### Pin outs

The figure that follows shows the pin outs for NTNP50AA.

**NTNP50AA connector P1 pin outs**

| | | | |
|---|---|---|---|
| 1 | RING1 | 33 | TIP1 |
| 2 | RING2 | 34 | 1IP2 |
| 3 | RING3 | 35 | TIP3 |
| 4 | RING4 | 36 | TIP4 |
| 5 | RING5 | 37 | TIP5 |
| 6 | RING6 | 38 | TIP6 |
| 7 | RING7 | 39 | TIP7 |
| 8 | RING8 | 40 | TIP8 |
| 9 | RING9 | 41 | TIP9 |
| 10 | RING10 | 42 | TIP10 |
| 11 | RING11 | 43 | TIP11 |
| 12 | RING12 | 44 | TIP12 |
| 13 | RING13 | 45 | TIP13 |
| 14 | RING14 | 46 | TIP14 |
| 15 | RING15 | 47 | TIP15 |
| 16 | RING16 | 48 | TIP16 |
| 17 | RING17 | 49 | TIP17 |
| 18 | RING18 | 50 | TIP18 |
| 19 | RING19 | 51 | TIP19 |
| 20 | RING20 | 52 | TIP20 |
| 21 | RING21 | 53 | TIP21 |
| 22 | RING22 | 54 | TIP22 |
| 23 | RING23 | 55 | TIP23 |
| 24 | RING24 | 56 | TIP24 |
| 25 | RING25 | 57 | TIP25 |
| 26 | RING26 | 58 | TIP26 |
| 27 | RING27 | 59 | TIP27 |
| 28 | RING28 | 60 | TIP28 |
| 29 | RING29 | 61 | TIP28 |
| 30 | RING30 | 62 | TIP30 |
| 31 | RING31 | 63 | TIP31 |
| 32 | RING32 | 64 | TIP32 |

### NTNP50AA connector P2 pin outs

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | | | GND | | |
| 2A 2B 2C 2D 2E | GND | GND | GND | GND | GND |
| 3A 3B 3C 3D 3E | | | GND | | |
| 4A 4B 4C 4D 4E | GND | GND | GND | GND | GND |
| 5A 5B 5C 5D 5E | ID0 | | GND | | GND |
| 6A 6B 6C 6D 6E | ID1 | PLANASEL0 | GND | PLANASEL1 | PLANASEL2 |
| 7A 7B 7C 7D 7E | GLANADS | ID3 | GND | ID4 | GLANBUS |
| 8A 8B 8C 8D 8E | ID2 | GLANAUS | GND | GLANBDS | IDP |
| 9A 9B 9C 9D 9E | TDMAUS | GND | ROW | GND | TDMBUS |
| 10A 10B 10C 10D 10E | GND | GND | GND | CLKB | GND |
| 11A 11B 11C 11D 11E | TDMADS | GND | COL | GND | TDMBDS |
| 12A 12B 12C 12D 12E | | | | | |
| 13A 13B 13C 13D 13E | | | | | |
| 14A 14B 14C 14D 14E | | | | | |
| 15A 15B 15C 15D 15E | TB1_AIT | TB1_AIR | | TB1_AOT | TB1_AOR |
| 16A 16B 16C 16D 16E | | | | | |
| 17A 17B 17C 17D 17E | | | | | |
| 18A 18B 18C 18D 18E | TB2_AIT | TB2_AIR | | TB1_AOT | TB2_AOR |
| 19A 19B 19C 19D 19E | | | | | |
| 20A 20B 20C 20D 20E | | | | | |
| 21A 21B 21C 21D 21E | TBRTN | TBRTN | HOLD_CLIP | TB | TB |
| 22A 22B 22C 22D 22E | TBRTN | TBRTN | TBB | TB | TB |
| 23A 23B 23C 23D 23E | TBRTN | TBRTN | TBB | TB | TB |
| 24A 24B 24C 24D 24E | TBRTN | TBRTN | TBB | TB | TB |
| 25A 25B 25C 25D 25E | TBRTN | TBRTN | TBB | TB | TB |

### NTNP50AA connector P3 pin outs

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | | SBA | SBA | SBA | SBA |
| 2A 2B 2C 2D 2E | | SBRTN | SBRTN | SBRTN | SBRTN |
| 3A 3B 3C 3D 3E | | SBB | SBB | SBB | SBB |

### NTNP50AA connector P4 pin outs

| | |
|---|---|
| 1 | GND |

## **NTNP50AA** (end)

## Technical data

The following table lists the technical data for the NTNP50AA.

**Technical data for the NTNP50AA**

| Characteristic | Value | Comments |
|---|---|---|
| Input voltage | -56 Vdc to -42.5 Vdc | |
| Talk battery | -48.0 V to -53.5 V | Normal range |
| | -42.75 V to -55.8 V | Extreme conditions |
| dc loop current limit | 50 mA | |
| dc feed resistance during ringing | 205 Ω nominal | This value is not selectable. |
| Power dissipation | 20 W | Typical |
| | 50 W | Maximum |
| Off-hook supervision limit | When loop draws more than 12 mA or total resistance is less than 1250 Ω | |
| On-hook supervision limit | When external loop resistance is greater than 8000 Ω | |
| Ambient temperature | -40 ° C to 65 ° C | |

# 12 NTNXnnaa

## NTNX13CA through NTNX65BA

# NTNX13CA

## Product description

The NTRX51AA cooling unit assembly contains the NTNX13CA cooling unit voltage limiter. The NTRX51AA cooling unit assembly measures 0.254 m (10 in.). The NTNX13CA allows the use of -48V fans for applications that require a battery voltage of -48V or -60V.

## Functional description

The NTNX13CA provides two modes of operation. When the input voltage is less than -56V, the NTNX13CA does not control the voltage output to the fans. When the input voltage is less than -56V, the NTNX13CA filters for noise that goes back to the battery. When the input voltage is higher than -56V, the NTNX13CA filters for noise. The NTNX13CA limits the maximum voltage output to the fans at -56V nominal.

### Functional blocks

The NTNX13CA has the following functional blocks:

- voltage limiter
- noise filter
- overvoltage protection
- current limit
- disconnect

### Voltage limiter

This block acts as a series regulator or field effective transistor (FET). This regulator limits the output voltage at -55V when the input voltage is higher than -56V. At lower input voltages, the FET regulator provides a fixed voltage drop of approximately 1.5V. The FET regulator provides this drop so that the ouput voltage follows the input voltage.

### Noise filter

This block provides an active filter that stabilizes the ac voltage across the FET regulator. This action reduces noise that goes back to the fan motors.

### Overvoltage protection

This block monitors the output voltage from the noise filter. The voltage can exceed a threshold of approximately -60V. When voltage exceeds this threshold, the system uses disconnect relay. The disconnect relay bypasses the FET regulator to prevent damage to the fans.

### Current Limit

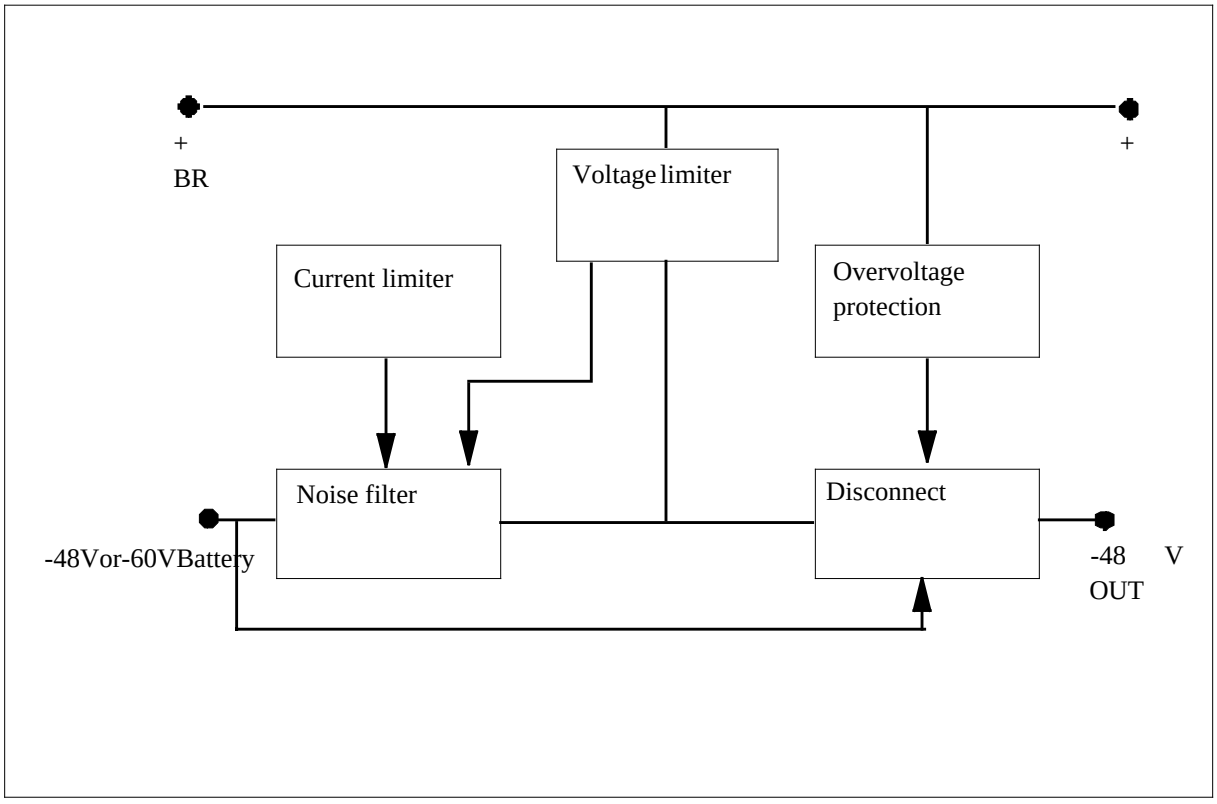
This block reduces the maximum output current to a safe value when the current in the FET regulator exceeds the threshold limit.

### Disconnect

This block operates with the overvoltage protection block. The disconnect block provides the ability to disconnect the FET regulator. The disconnect block provides the ability to switch to a voltage–dropping resistor when the voltage limiter fails. This action ensures that the fans continue to operate when the input is above -56V. High voltage can damage the fans. Switching to a voltage–dropping resistor makes sure the fans are not subject to high voltage.

The following figure indicates the relationship between the functional blocks.

**NTNX13CA functional blocks**



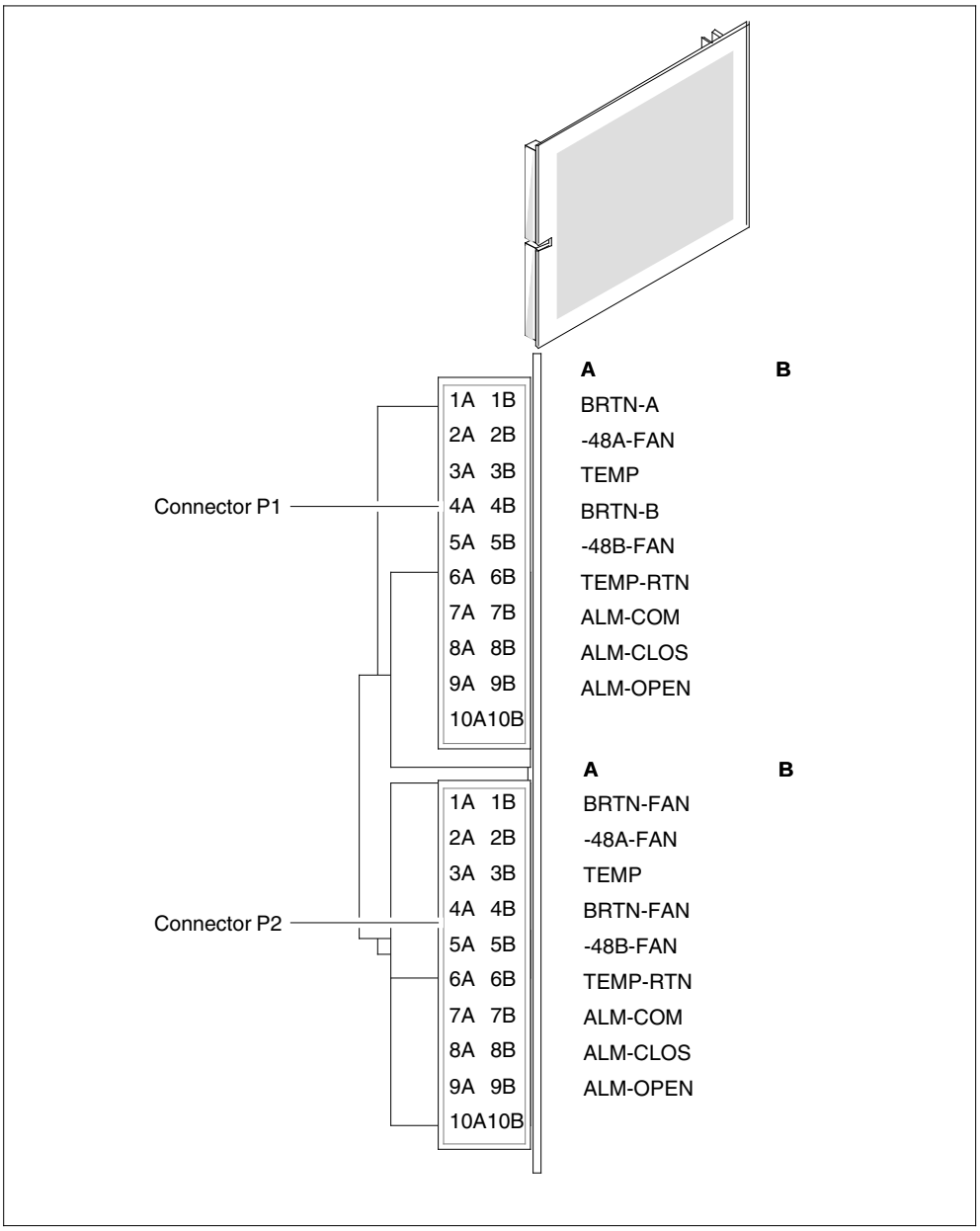

## Signaling

### Pin numbers

The pin numbers for the NTNX13CA appear in the following figure.

## **NTNX13CA** (continued)

**NTNX13CA pin numbers**




# Technical data

### Power requirementsInput

The nominal input voltage is -48V or -60V, but a range from -52V to -72V is also appropriate. The maximum input current is 1.5A.

## Output

The output specifications of the NTNX13CA appear in the following table.

**Output specifications**

| | | |
|---|---|---|
| Voltage | -48V nominal | -56V maximum |
| High voltage shutdown | 60V ± 2V | |
| Low voltage shutdown | 39V ± 1V | |
| Maximum current | 1.5 A | |
| Current limit | 2A | |
| Voltage limiter threshold | 55V ± 1.5V | |

# NTNX14AA

## Product description

The NTNX14AA remote line concentrating cabinet is a special version of the line concentrating module. This line concentrating module can connect to a maximum of 640 subscriber lines. The central–side (C–side) of the remote line concentrating cabinet (RLCC) can connect over DS–1 links to a line group controller (LGC). The C–side of the RLCC can connect over DS–1 links to a line trunk controller (LTC). The RLCC can be a maximum of 161 km (100 mi) from the LGC or LTC. The RLCC can connect to a Remote Switching Center (RSC), which connects to an LGC or LTC. The RLCC can be a maximum of 80 km (50 mi) from the RSC.

The available emergency stand–alone (ESA) service provides plain ordinary telephone service (POTS) between subscribers connected to the same line concentrating module. The same host interface equipment (HIE) controls the line concentrating module. The ESA provides the POTS to the subscribers if loss of every DS–1 signaling channel to the host office occurs.

The RLCC complies with the US electromagnetic interference (EMI) requirements. The RLCC contains a remote maintenance module shelf, and a shelf of host interface equipment. The RLCC also contains a dual–shelf line concentrating module, and an NTNX27AA cooling unit.

## Parts

The NTNX14AA remote line concentrating cabinet consists of the following parts:

- host interface equipment assembly
- remote maintenance module assembly
- RLCM–C frame supervisory panel
- line concentrating module shelf

### Host interface equipment assembly

The NT6X1101 HIE assembly is one shelf of the RLCC. The HIE allows the RLCC to support DS–1 and C–side links. The HIE converts between DS–1 links and DS30A links in the line concentrating module in the RLCC.

The HIE shelf includes two or three DS–1 interface cards, two link control cards, and ringing generators if analog ringing is a requirement. The C–side of each link control card connects to each DS–1 card, the other link control card, and the NT6X1301 remote maintenance module.

### Remote maintenance module assembly

The NT6X1301 remote maintenance module (RMM) shelf provides maintenance and operational support for remote offices that connect to a DMS–100 central office. The NT6X1301 is a modified version of the NT2X58 maintenance trunk module shelf. This module supports metallic test access, incoming/outgoing test trunks, line test units, scan and signal distribution points. When ESA is included, this module supports NT2X48AB digital four–channel receivers. The RMM shelf contains a control card (NT6X74AA), and a group CODEC DMS–100/200 card (NT2X59AA). The RMM shelf also contains a pair of power converters (NT2X06AB and NT6X09AA), and a maximum of 14 service cards. The requirements of the office will determine the type of cards used. Some of the service cards used in the RMM are for metallic test access functions.

### RLCM-C frame supervisory panel

The NTNX26AA FSP provides the talk jacks, fuse alarm features, and power control for the RLCC. The NTNX26AA FSP contains the 48–V dc power distribution circuit breakers for the ringing generators. The circuit breakers are in the HIE shelf, and several converters in the cabinet.

### Line concentrating module shelf

The RLCC contains two NTNX2802 line concentrating module (LCM) shelves. Each shelf has a control complex and power converter. The control complex includes a line concentrating module processor and eight digroup control cards. The DS30A links connect six of the C–side digroup control ports to the host line group controller. The other two ports connect to the digroup control cards on the other LCM shelf and are used for link sharing.

A specially equipped HIE shelf and a specially equipped RMM shelf are required for each LCM that has the available ESA.

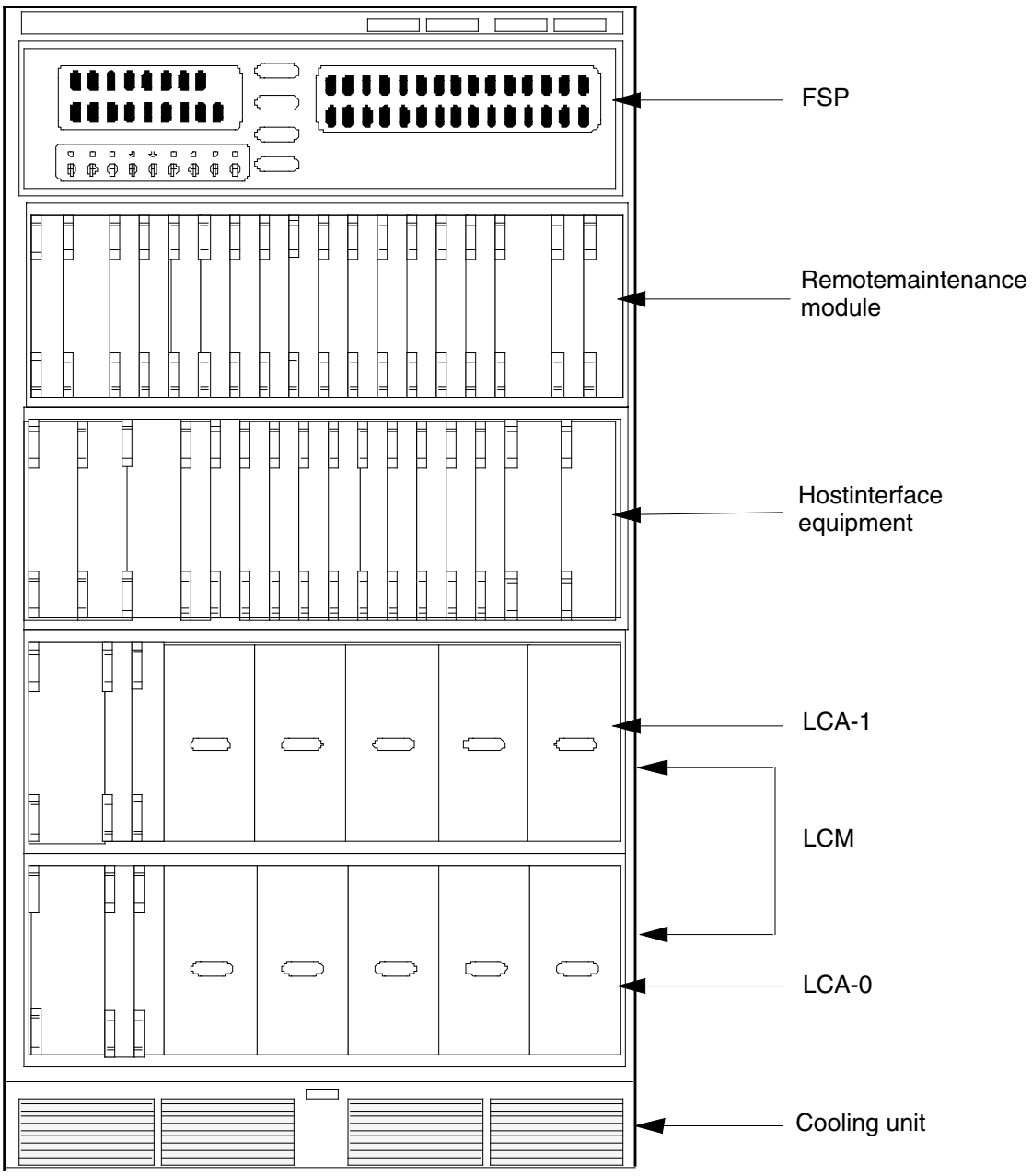
Each shelf in the LCM contains five NT6X05AA line drawers. Each line drawer contains a bus interface card and two line subgroups. Each line subgroup includes a maximum of 32 line cards, one for each subscriber line that the line subgroup services.

## Design

The design of the NTNX14AA cabinet appears in the following figure.

# **NTNX14AA** (end)

**NTNX14AA parts**




**Note:** This illustration is not drawn to scale.

## Product description

The NTNX26AA RLCM–C frame supervisory panel (FSP) provides the power, power control and alarm circuits for the elements in the remote line concentrating cabinet (RLCC) frame. The system uses all of the following to provide power control:

- nine circuit breakers
- an NT6X36AA alarm card (CD1)
- an NT0X91AA converter drive and alarm card (CD2)
- an NT0X91AE converter drive and protection card (CD3)

Converter fail lines from the power converters in the RLCC are connected to light–emitting diode (LED) frame fail indicators on the front panel of the FSP. The converter fail lines also operate fail LEDs. The diodes are located below the associated power–feed circuit breakers on the front panel of the FSP.

## Parts

The FSP consists of the following parts:

- NT0X91AA—FSP drive and alarm card
- NT0X91AE—alarm drive and protective circuit network
- NT6X36AA—line concentrating module FSP alarm card

### FSP drive and alarm card

The FSP uses the NT0X91AA alarm and converter drive card to monitor every circuit breaker and fuse alarm. The converter drive part of the card controls the -48V dc feeds to the two power converters. The NT0X91AE converter does not drive these two power converters. The alarm part of the NT0X91AA card receives input from the converter fail bus and the guard contacts. The above input involves the guard contacts of fuses F02 to F04. When the alarm circuit receives an input, the frame fail lamp is lit. This light indicates a connection between aisle alarm 1 and aisle alarm 2. Aisle alarm 2 also provides a connection for an end aisle alarm lamp.

### Alarm drive and protective circuit network

The FSP uses the NT0X91AE to provide power control and protection to the shelves of the RLCC. When a circuit breaker is closed, the system cannot apply the –48V dc feed to the converter in shelf position 65. The system can supply power to the converter with the use of the correct series of power–up applications. The correct power–up sequence involves application of the ON/OFF, RESET and CONVERTER DRIVE leads. Some of the printed circuit board connection fingers on NT0X91AA do not trip. This failure to

## **NTNX26AA** (continued)

trigger a connection can occur when the NT0X91AE is withdrawn and reinserted. The removal and insertion of the NT0X91AE can cause transient or other types of power surges to occur.

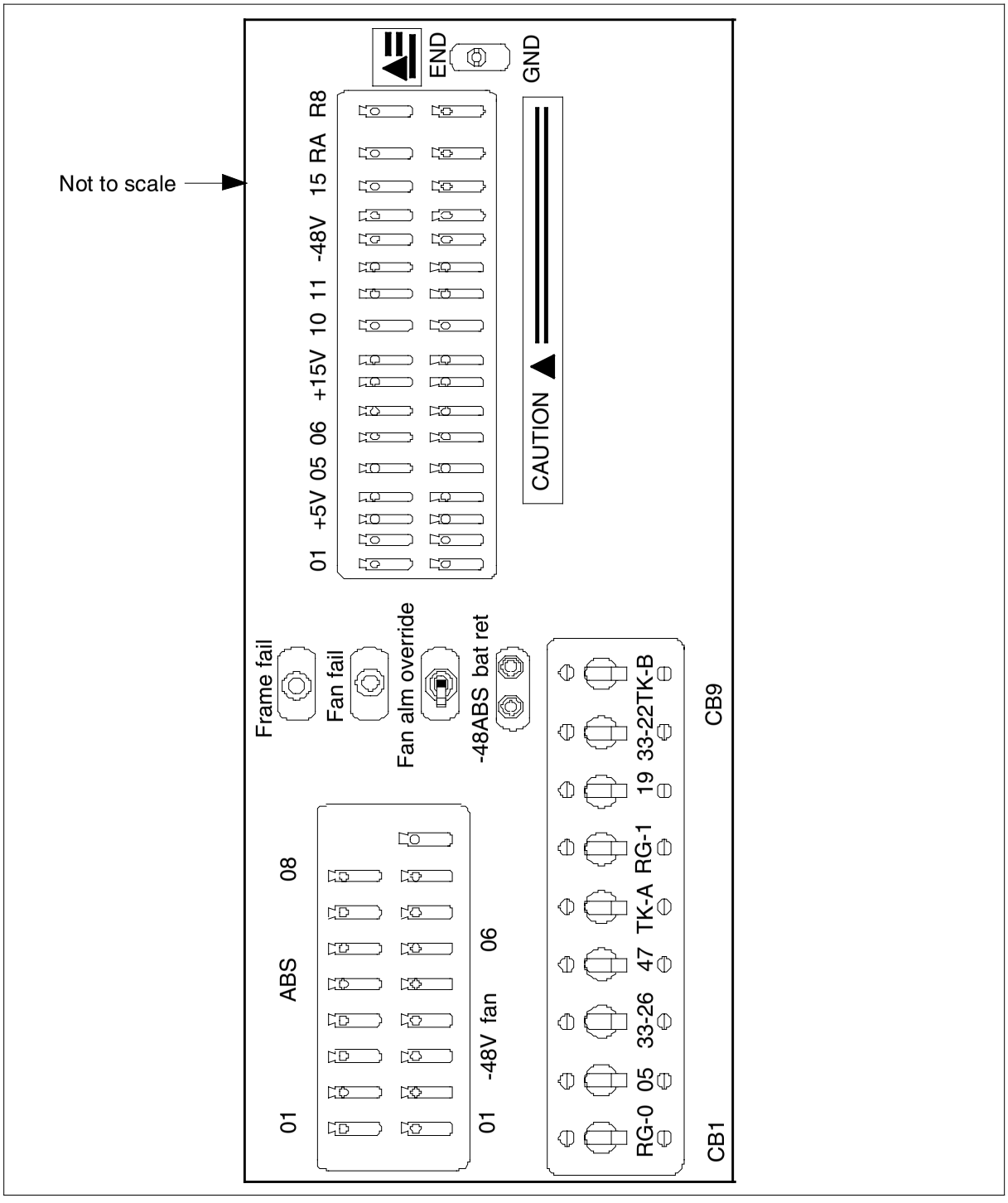
### Line concentrating module FSP alarm card

The FSP uses the NT6X36AA alarm card to indicate a dangerous or threatening condition to the power system or other cards. When the aisle alarm loop is closed, the system responds to the alarm condition. The system lights the frame fail lamp and the end aisle lamp. Alarm conditions can include fan fail, fuse fail, tripped circuit breakers CB8 and CB9, and T1 alarms. If the problem occurs in a power converter or ringing generator, the alarm LED is lit.

## Design

The front view of the NTNX26AA frame supervisory panel appears in the following figure. The cards inside the FSP are not visible in the figure.

**NTNX26AA parts**



# NTNX27AA

## Product description

The NTNX27AA cooling unit is at the bottom of the NTNX14AA remote line concentrating cabinet. The cooling unit includes circulation fans for cooling the shelves of circuit cards above the cooling unit in the cabinet.

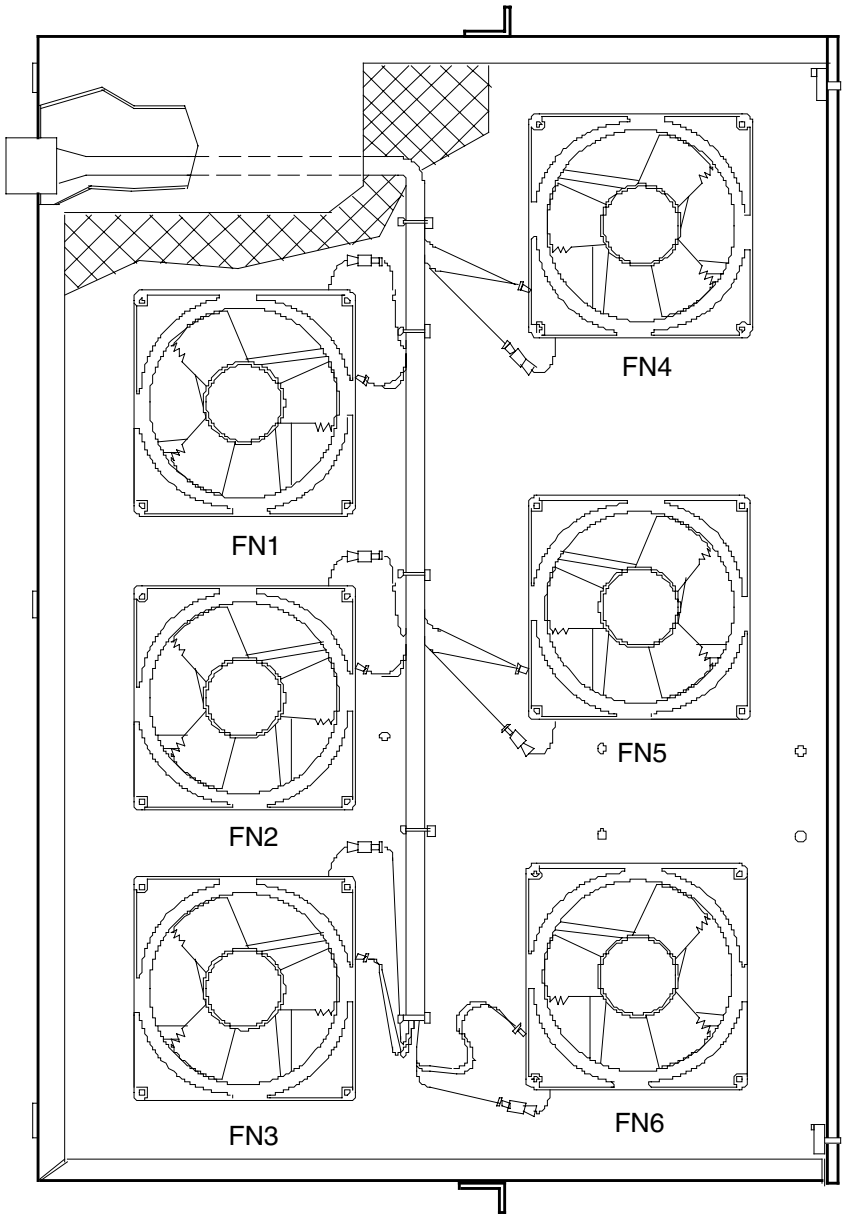
## Parts

The cooling unit includes six circulation fans. The circulation fans provide forced–air convection cooling for the four shelves of cards in the remote line concentrating cabinet.

## Design

The design of the NTNX27AA cooling unit appears in the following figure.

**NTNX27AA parts**




**Note**: This illustration is not drawn to scale.

# NTNX27CA

## Product description

The NTNX27CA cooling unit is at the bottom of the following types of cabinets.

- NTRX32CA—Cabinetized trunk module equipment (CTME)
- NTRX33DA—Cabinetized input/output equipment (CIOE)
- NTRX35CA—Cabinetized dual shelf network (CDSN)
- NTRX36BA—Cabinetized common peripheral equipment (CCPE)
- NTRX46CA—Cabinetized international peripheral equipment (CIPE)
- NTRX47BA—Cabinetized international digital controller (CIDC)
- NTRX48BA—Cabinetized international message and buffer switch (CMS7)
- NTRX56AA—Zoned miscellaneous equipment cabinet (CMIS)

The cooling unit contains circulation fans to cool the shelves of circuit cards above the cooling unit in the cabinet.

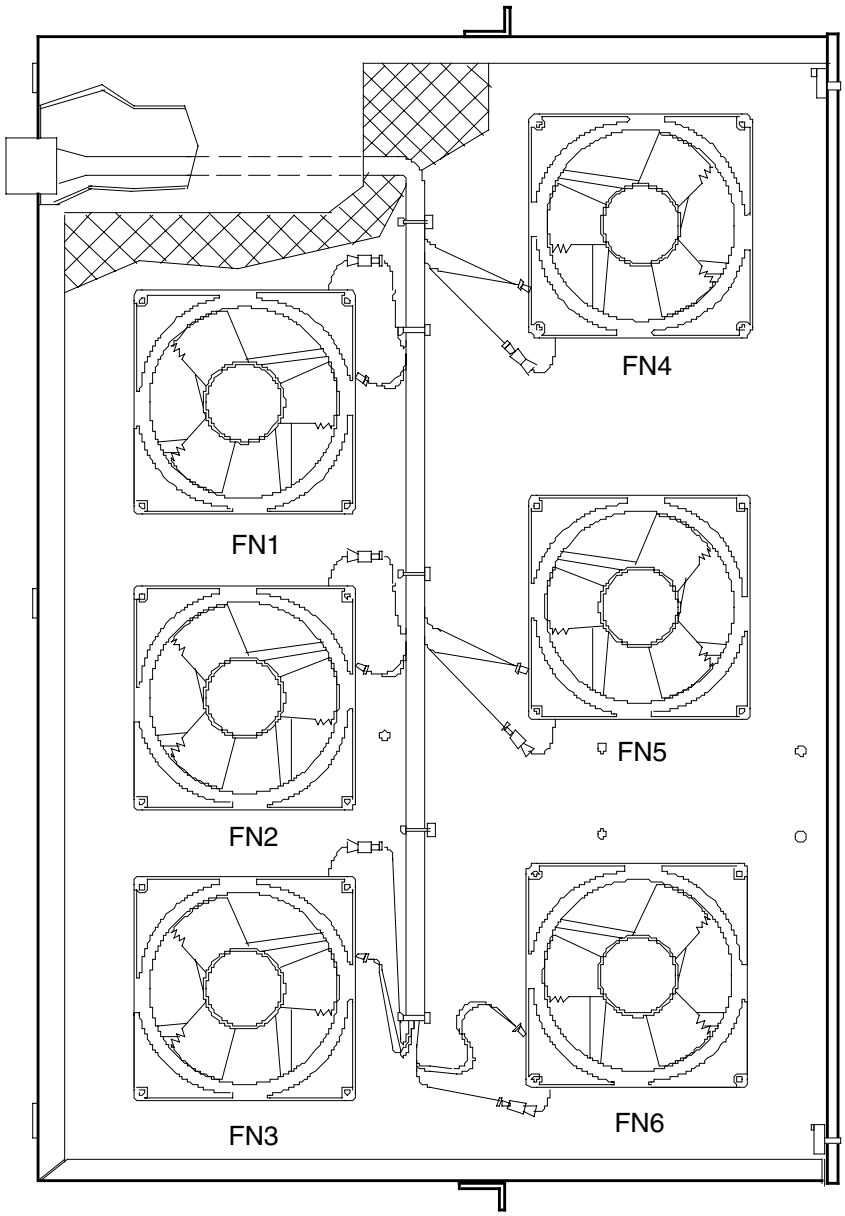
## Parts

The cooling unit contains six circulation fans. The circulation fans provide forced–air convection cooling for the four shelves of cards in the remote line concentrating cabinet.

## Design

The design of the NTNX27CA cooling unit appears in the following figure.

**NTNX27CA parts**




**Note**: This illustration is not drawn to scale.

# NTNX27DA

## Product description

The NTNX27DA cooling unit is at the bottom of the following types of cabinets.

- NTRX30CA—Cabinetized lineconcentration equipment (CLCE)
- NTRX30DA—Cabinetized line module ISDN (CLMI)

The cooling unit includes circulation fans to cool the shelves of circuit cards above the cooling unit in the cabinet.

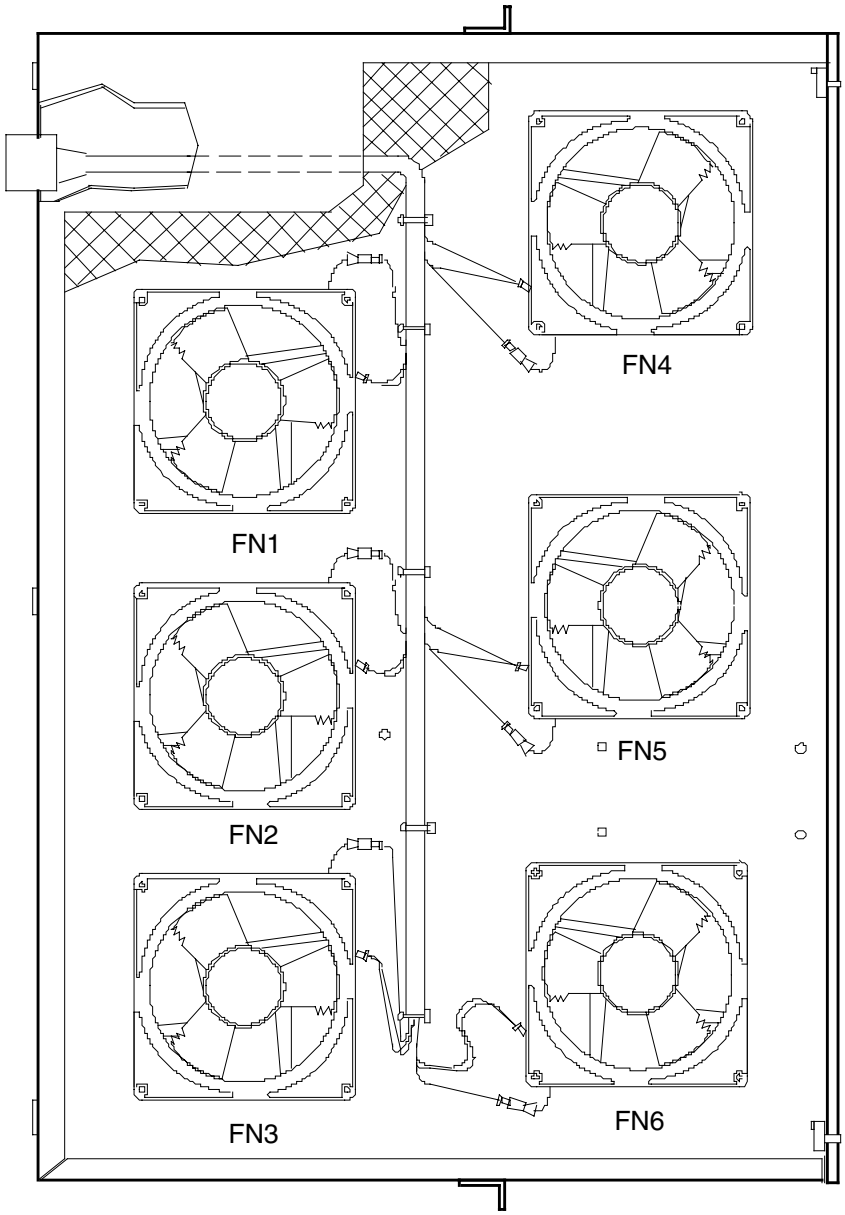
## Parts

The cooling unit contains six circulation fans. The circulation fans provide forced–air convection cooling for the four shelves of cards in the remote line concentrating cabinet.

## Design

The design of the NTNX27DA cooling unit appears in the following figure.

**NTNX27DA parts**




**Note:** This illustration is not drawn to scale.

# NTNX51BD

## Product description

The NTNX51BD provides three basic functions. The three basic functions are audio, digital voice trunk interface and micro–channel interface.

The digital signal processor on the NTNX51BD card handles the audio functions. The digital signal processor handles the audio functions after the signals are adjusted from balanced to unbalanced in the transmit path. The transmit path is the path from operator to network. The receive path refers to the path from network to operator.

The audio functions provide the following:

- sidetone, acoustic limiting, echo control and volume control
- two headset taps
- an interface to headsets

The digital DS–0A trunk provides a voice trunk interface from the TOPS MPX position to the network through a channel bank. The digital voice trunk interface has the following characteristics:

- operates at 64 kbit/s with a DS–0A tandem link interface
- requires an externally sourced composite clock
- provisioned with a 6–wire interface (2 for RX data, 2 for TX data and 2 for RX composite clock)

The micro–channel interface has the following:

- software command register
- data register
- hardware command register
- interrupt line IRQ3-

The software command register receives digital signal processor commands from the PS/2. The software command register is a write–only register from the PS/2. The software command register is a read–only register from the digital signal processor on the card.

The data register receives state messages from the digital signal processor. The PS/2 reads the state messages. The 8 bit data register is read only to the PS/2 and write only for the digital signal processor.

The hardware command register is a mixed read–write and read–only register. This register has bits 0–7 assigned to the following hardware functions:

- Bit 0 represents a write pending flag that is an active high signal. This bit indicates a last command received interrupt pending.
- Bit 1 represents a read pending flag that is an active high signal. This bit indicates message waiting interrupt pending.
- Bit 2 represents a write interrupt enable that is an active high signal. This bit enables the write pending interrupt line to the PS/2. You can reset this bit to 0. This action disables the last command received interrupt. The write pending flag remains set.
- Bit 3 represents a read interrupt enable which is an active high signal. This bit allows the read pending interrupt line to the PS/2. When you reset this bit to 0, the message waiting interrupt is disabled. The read pending flag remains set.
- Bit 4 represents headset 1 state that is an active low signal. When headset 1 is present, this signal is driven low.
- Bit 5 represents headset 2 state that is an active low signal. When headset 2 is present, this signal is driven low.
- Bit 6 represents CLKLOSS state that is an active low signal. When loss of the receive composite clock occurs, this bit is driven low.
- Bit 7 represents SWRESET that is an active low signal. When the PS/2 sets this bit low, the bit initializes the board like a powerup reset.

Interrupt line IRQ3- is a shared interrupt line to the PS/2 micro–processor. The write pending flag interrupt drives this line low when you set the write to 1. The read pending flag interrupt drives this line low when you set the read interrupt enable to 1. The interrupt clears when the hardware command register is read. This action informs the PS/2 which interrupt causes IR13- to go low.

The NTNX51BD is backwards compatible with the NTNX51BC version.

### Location

The user installs the on one of the three expansion I/O slots of the PS/2 (MPX) terminal base. The MPX terminal position uses the PS/2 model 55SX as the base terminal. An NT TOPS MPX logo indicates this terminal.

## Functional description

The NTNX51BD is a modified version of the NTNX58BA. The NTNX58BD provides the same functionality as the BA version in the PS/2 position. The BD version provides the same operator interface. The BD version provides a

## **NTNX51BD** (continued)

DS–0A digital voice trunk interface between the MPX position and the network through a channel bank. If the base position changes to a PS/2 position, the interface to the backplane must change to a micro–channel interface.

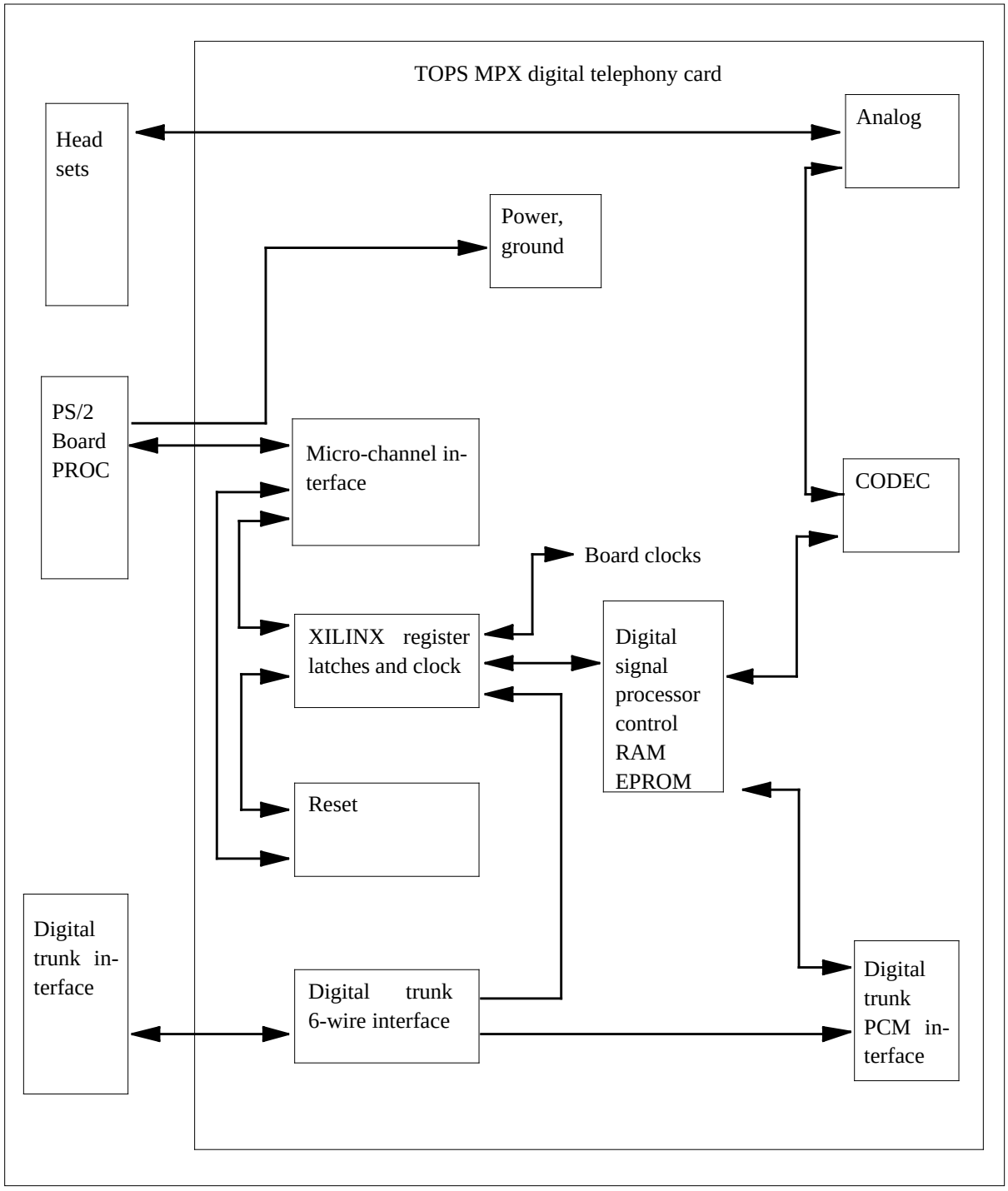
### Functional blocks

The NTNX51BD has the following functional blocks:

- power and ground
- micro–channel interface
- register latch block
- digital trunk interface block
- trunk PCM latch block
- clock generation and clock lock block
- reset block
- digital signal processor control block
- CODEC block
- analog block

The relationship between the functional blocks appears in the following figure.

**NTNX51BD functional blocks**



## **NTNX51BD** (continued)

### Power and ground

The NTNX51BD receives +5V, +12V, –12V and logic ground from the micro–channel card edge finger connector P1. The frame ground is in the common feature for the card. The faceplate of the card connects the PS/2 frame ground to the card. Logic and frame ground are capacitively coupled from each other on the card. The card generates analog ground (+6V) and CODEC reference voltage 8.5V or 2.5V above analog ground (AGND).

### Micro–channel interface block

This interface contains the 88C01 micro–channel interface chip and the 88C01 configuration EEPROM. The other circuits in this block are the XCVR from the 8–bit data bus interface and an open collector interrupt line IRQ3-. The IRQ3- goes back to the PS/2 micro–processor. This block generates four output signals to read and write to the latched register block.

### Register latch block

This block contains all the latch and handshaking circuits for the

- software command register
- data register
- hardware command register
- digital signal processor state register

The handshaking circuits preserve the timing characteristics of the NTNX58BD so that firmware changes are not required. The XILINX part contains this block of circuits.

### Digital trunk interface block

This interface is a 6–wire digital voice trunk interface that operates at 64 kbit/s. This block converts the receive (RX) voice and RX composite clock 100% bipolar data streams to unipolar data streams. When the composite clock changes to a unipolar signal, the byte clock and bit clock are removed. The clocks are passed on to the XILINX SP to generate all clocks used on the card. The bit clock, receive 64 kbit/s clock, is also passed to the programmable array logic (PAL) for clock loss detection. When the RX voice signal changes to a unipolar signal, the unipolar signal is passed on to the trunk pulse code modulation (PCM) latch block. This block also converts the two unipolar transmit (TX) voice signals from the trunk PCM latch block into a TX bipolar data stream.

### Trunk PCM latch block

This block converts the serial receive (RX) voice data to parallel voice data and buffers the data for the digital signal processor (DSP). This block also buffers

the transmit (TX) voice data for the digital voice trunk and converts the buffered parallel voice data to a serial format. The serial format TX voice data runs through a PAL to convert the serial format to two unipolar data streams with the proper digital trunk timing. The digital trunk interface block receives the unipolar data streams.

### Clock generation and clock lock block

This block of circuits in the XILINX part, generates phase locked clocks used throughout the card. These clocks are phase locked to the falling edge of the byte clock (8 kHz) received from the digital voice trunk composite clock.

This block generates the following clocks:

- BLOAD- (– = active low)
- B2.56MHz
- B2.56.MHz (inverted B2.56 MHz clock)
- B64KCLK
- 128KCLK
- 256KCLK
- 1.28MCLK

### Reset block

This block contains the reset circuits for the card. The micro–channel reset signal (CHRESET) on powerup can reset the card. The PS/2 micro–processor can also reset the card when you write a 0 in bit 7 of the hardware command register.

### Digital signal processor control block

This block is centered around the TMS320C25 digital signal processor. The block contains the RAM that the digital signal processor uses. This block also contains the firmware that the digital signal processor contained in UV EPROMs uses. The digital signal processor input and output enables are also part of this block.

This block provides the following:

- message interface control to the PS/2 planar board
- PCM interface control to the digital voice trunk
- headset detect circuits to detect headset source impedances from 30 ohms to 70 ohms
- PCM interface to the CODEC

## **NTNX51BD** (continued)

- all speech processing except the padding of signals to meet transmission level point (TLP) requirements at the headset jacks
- board diagnostics

### CODEC block

This block allows the analog to digital and digital to analog conversions. This block interfaces interfaces the digital signal processor to the analog portion of the board.

### Analog block

The two parts of the analog block are transmit and receive. The interface is a two headset interface. When the user jacks a headset in a headset jack, the headset detect circuits becomes active.

The transmit block performs the following functions:

- converts balanced to unbalanced for input to the CODEC
- matches 50 OHM headset source impedance
- contains the resistor pad required to interface to the CODEC
- contains the headset detect circuit

The receive block does the following:

- converts unbalanced to balanced for output to the headset
- matches 300 OHM headset load
- contains the resistor pad required to interface from the CODEC

## Signaling

### Pin numbers

The card contains four connectors:

- micro–channel card edge connector
- teledapt headset one jack
- teledapt headset two jack
- teledapt digital voice trunk jack

The micro–channel card edge connector interfaces with the PS/2 planar card (motherboard). The connector has pins 1A to 58A and 1B to 58B. Pins 46A, 46B, 47A and 47B are for the key slot location. These pins are not available for electrical interface functions. The connector uses 75 pins.

The teledapt headset one jack connector is a four–position, four–contact low profile teledapt plug. The user can access the teledapt headset one jack connector through the faceplate. The connector uses all pins.

The Teledapt headset two jack connector is a four–position, four–contact low profile teledapt plug. The user can access the teledapt headset two jack connector through the faceplate. The connector uses all pins.

The teledapt digital voice trunk jack connector is a six–position, six–contact low profile teledapt plug. The user can access the teledapt digital voice trunk jack connector through the faceplate. The connector uses all pins.

**Micro–channel edge connector (Sheet 1 of 3)**

| Signal | Pin |
|---|---|
| GND | 3A, 3B, 5B, 9B, 13B, 17B, 21B, 25B, 29B, 33B, 37B, 41B, 43A, 45B, 50B, 54B, 58B |
| +5 | 7A, 11A, 15A, 31A, 39A, 48A, 56A |
| +12 | 19A, 35A, 52A |
| -12 | 23A, 37A |
| MAKE24 | 2A |
| Address A0 | 18A |
| Address A1 | 17A |
| Address A2 | 16A |
| Address A3 | 14A |
| Address A4 | 13A |
| Address A5 | 12A |
| Address A6 | 10A |
| Address A7 | 9A |
| Address A8 | 8A |
| Address A9 | 6A |
| Address A10 | 5A |
| Address A11 | 4A |

## **NTNX51BD** (continued)

**Micro–channel edge connector (Sheet 2 of 3)**

| Signal | Pin |
|---|---|
| Address A12 | 20B |
| Address A13 | 19B |
| Address A14 | 18B |
| Address A15 | 16B |
| Address A16 | 15B |
| Address A17 | 14B |
| Address A18 | 12B |
| Address A19 | 11B |
| Address A20 | 10B |
| Address A21 | 8B |
| Address A22 | 7B |
| Address A23 | 6B |
| -ADL | 20A |
| -CD DS 16 | 55A |
| -SO | 32A |
| –S1 | 33A |
| M/–IO | 34A |
| -CMD | 34B |
| CD CHRDY | 36A |
| -CD SFDBK | 36B |
| -CDSETUP | 1A |
| -REFRESH | 45A |
| 14.3MHZ OSC | 4B |
| CHRESET | 42B |

**Micro–channel edge connector (Sheet 3 of 3)**

| Signal | Pin |
|---|---|
| MicroD0 | 37A |
| MicroD1 | 38B |
| MicroD2 | 38A |
| MicroD3 | 39B |
| MicroD4 | 40B |
| MicroD5 | 40A |
| MicroD6 | 41A |
| MicroD7 | 42A |
| IRQ3 | 23B |

**Teledapt head one jack**

| Signal | Pin |
|---|---|
| RHD | 1 |
| RHD- | 2 |
| XHG- | 3 |
| XHD | 4 |

**Teledapt headset one jack**

| Signal | Pin |
|---|---|
| RHD2 | 1 |
| RHD2- | 2 |
| XHD2- | 3 |
| XHD2 | 4 |

## **NTNX51BD** (continued)

**Teledapt digital voice trunk jack**

| Signal | Pin |
|---|---|
| CCRXT | 1 |
| CCRXR | 2 |
| RXDATAT | 3 |
| RXDATAR | 4 |
| TXDATAT | 5 |
| TXDATAR | 6 |

# Technical data

Connectors J1 and J2 are for the headsets. Connector J3 is for the DS–0A digital voice trunk interface. Connector P1 is for the micro–channel adapter connector.

## Power requirements

The maximum power available appears as follows:

- 1.6A at +5V (5V±5%)
- 175 mA at +12V (12V±10%)
- 40 mA at -12V (-12V ±10%)

Average use appears as follows:

- .59A at +5V
- 150mA at +12V
- 20mA at -12V

**Power requirements (Sheet 1 of 2)**

| Signal | Reference to ground | Comment |
|---|---|---|
| +5 | 5V | digital power |
| +12 | 12V | analog power |
| -12 | -12V | analog power |
| +5V | 5V | nonfused power |
| +12V | 12V | nonfused power |

**Power requirements (Sheet 2 of 2)**

| Signal | Reference to ground | Comment |
|---|---|---|
| -12V | -12V | nonfused power |
| GND | GND | logic ground |
| AGND | 6V | analog ground |
| VREF | 8.5V | CODEC reference |
| CHASSISGND(1) | isolated from logic | PS/2 frame ground |

The specification for the isolation between frame and logic grounds is 750V direct current.

# NTNX63AB

## Product description

The TOPS multipurpose (MP) memory card provides 6 Mbytes of dynamic RAM (DRAM). This card replaces the previous version (NTNX63AA) that provides 4 Mbytes of memory.

### Location

The NTNX63AB is in the TOPS controller shelf of the TOPS–MP controller equipment frame.

## Functional description

The NTNX63AB provides program and data storage for the TOPS–MP system. The NTNX63AB uses a logic cell array (LCA) to provide an interface. This interface is between the address bus (A–bus) of the system and the onboard memory array. The LCA firmware provides known addressing. The previous version (NTNX63AA) provides variable addressing.

### Functional blocks

The NTNX63AB has the following functional blocks:

- A–bus interface
- address multiplexer (MUX)
- address interface
- control interface
- data interface
- parity generation block
- DRAM control block
- memory interface
- memory array.

### A–bus interface

The A–bus interface provides the onboard buffers that handle data transfers to and from the system backplane on one side. The A–bus interface provides the DRAM control circuits and memory data bus on the other side.

### Address MUX

The address MUX assigns the row (A1-A10) and column (A11-A20) addresses to the memory array.

### Address interface

The address interface buffers the incoming address lines and passes the address to the LCA of the DRAM control block.

### Control interface

The control interface provides the control lines to perform read and write operations. The control interface provides a DRAM refresh.

### Data interface

The data interface provides the bidirectional A–bus with access to the memory array. The data interface provides the control and status registers.

### Parity generation block

The parity generation block provides a parity bit in each byte of data during memory write cycles. During memory read cycles, the assignment of another parity bit occurs for parity checking purposes. The LCA in the DRAM control block performs the detection.

### DRAM control block

The LCA that contains the memory control and status registers composes the DRAM control block.

The DRAM control block performs the following functions:

- controls memory access
- issues memory refresh every 15.4 μs
- handles parity set up (odd or even)
- detects parity errors and asserts a memory interrupt bit.

### Memory interface

The memory interface provides buffering for all data bus signals to and from the memory array.

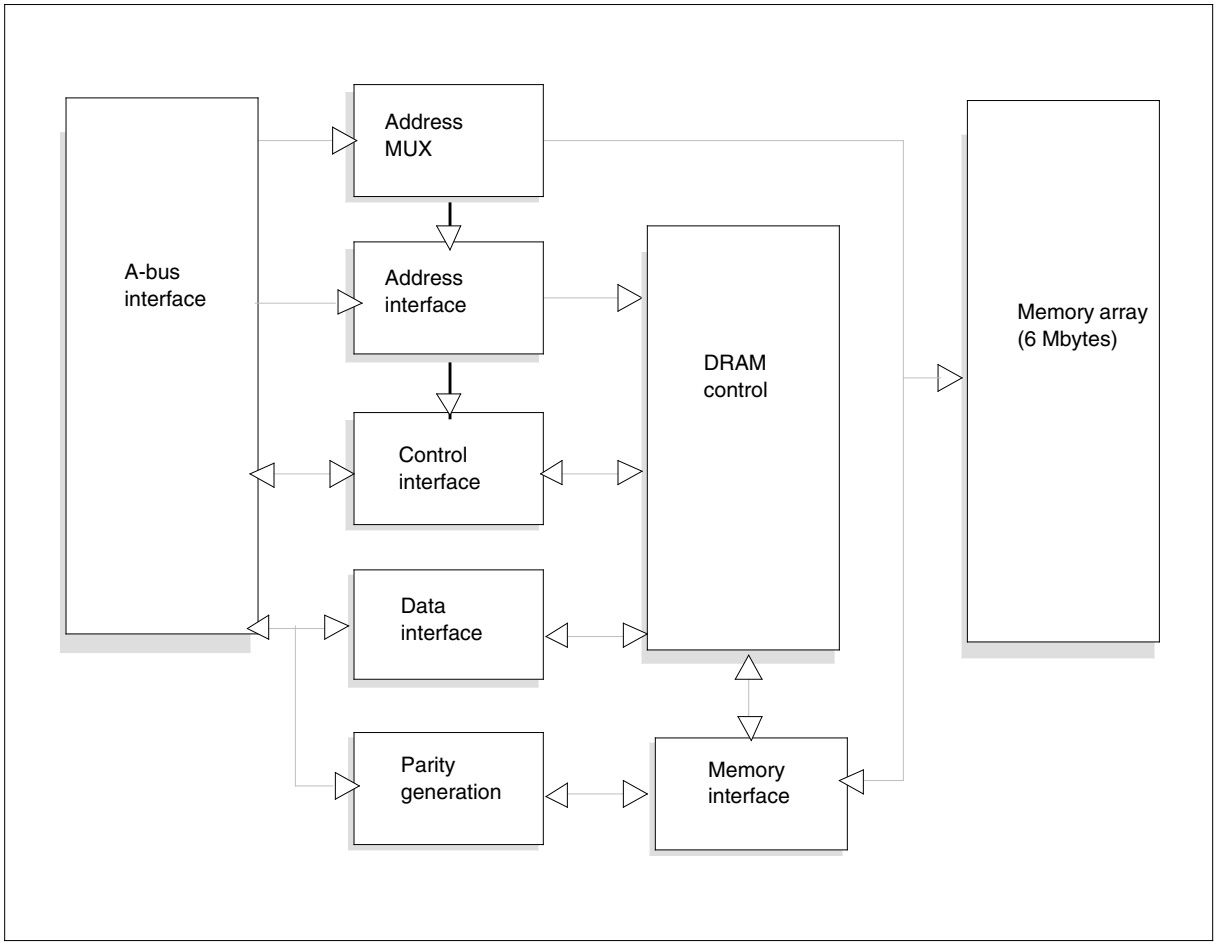
### Memory array

The memory array contains DRAM. The memory array is 6 Mbytes or 3 Mwords in size. Bytes or words can access the memory array.

The relationship between the functional blocks appears in the following figure.

## NTNX63AB (continued)

**NTNX63AB functional blocks**




# Technical data

### Power requirements

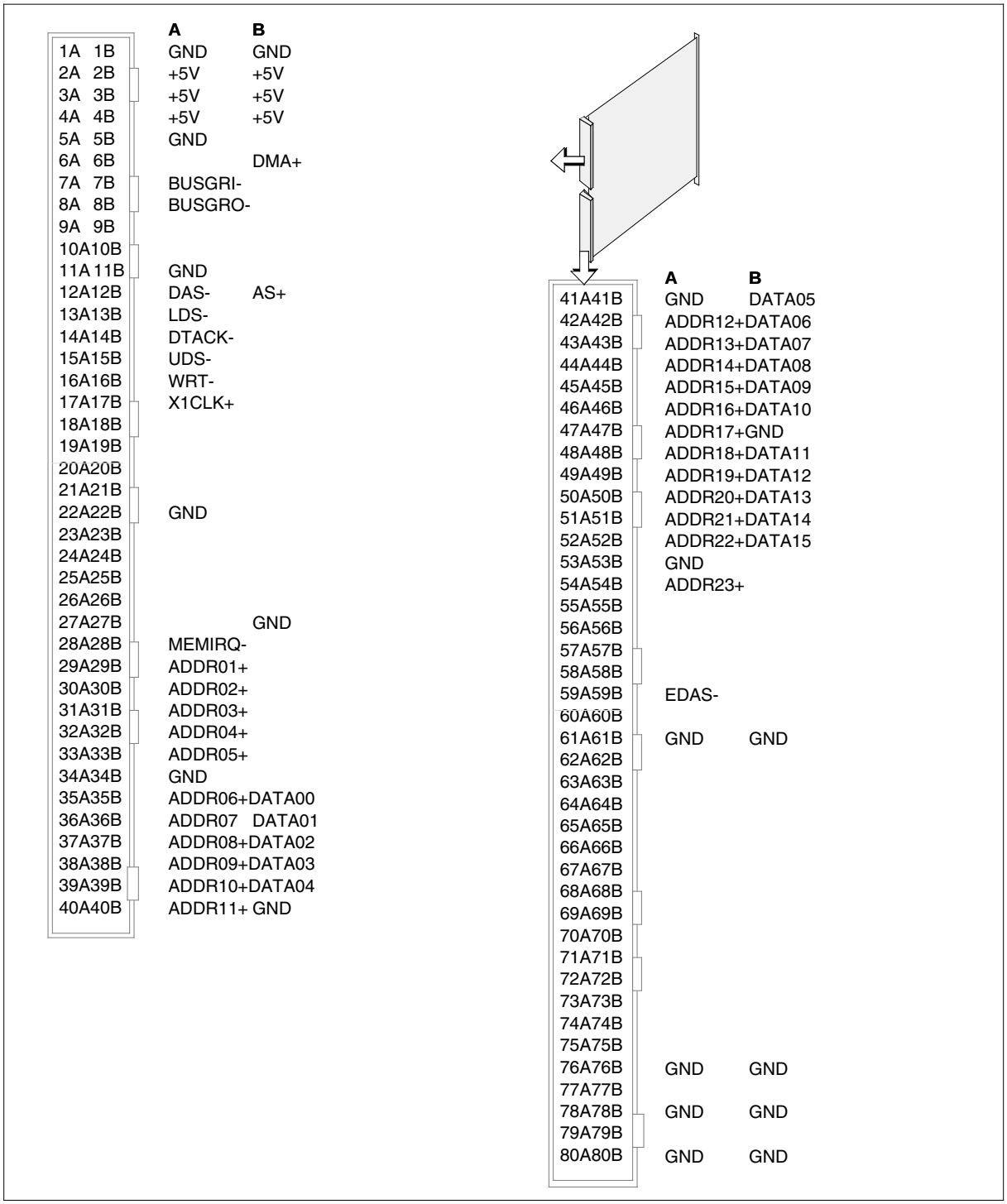
The minimum supply voltage for the NTNX63AB is +5V and the maximum supply current is 1.3A.

# Signaling

### Pin numbers

The pin numbers for the NTNX63AB appears in the following figure.

### NTNX63AB pin numbers



# NTNX65BA

## Product description

The TOPS master processor input/output controller card provides an interface. The interface is between the single board computer (SBC) system memory and the mass storage subsystem (MSS) of the TOPS controller (TPC) system.

## Functional description

The NTNX65BA controller card allows the Winchester drive and the floppy disk drive to communicate with the TPC system. The main function of the card is to decode address bus (A–bus) address lines and manipulate A–bus control signals. This function allows the NTNX65BA to control data flow to and from the SCSI bus. The NTNX65BA uses the NCR 5380 SCSI chip to perform these functions.

### Functional blocks

The NTNX65BA card has the following functional blocks:

- A–bus interface
- SCSI interface.

### A–bus interface

The A–bus interface allows the NTNX65BA to communicate with the SBC system memory and the TPC system. This interface allows external manipulation of internal registers that control the NTNX65BA functionality and the SCSI bus. The NTNX65BA is a slave device on the TPC A–bus.

### SCSI interface

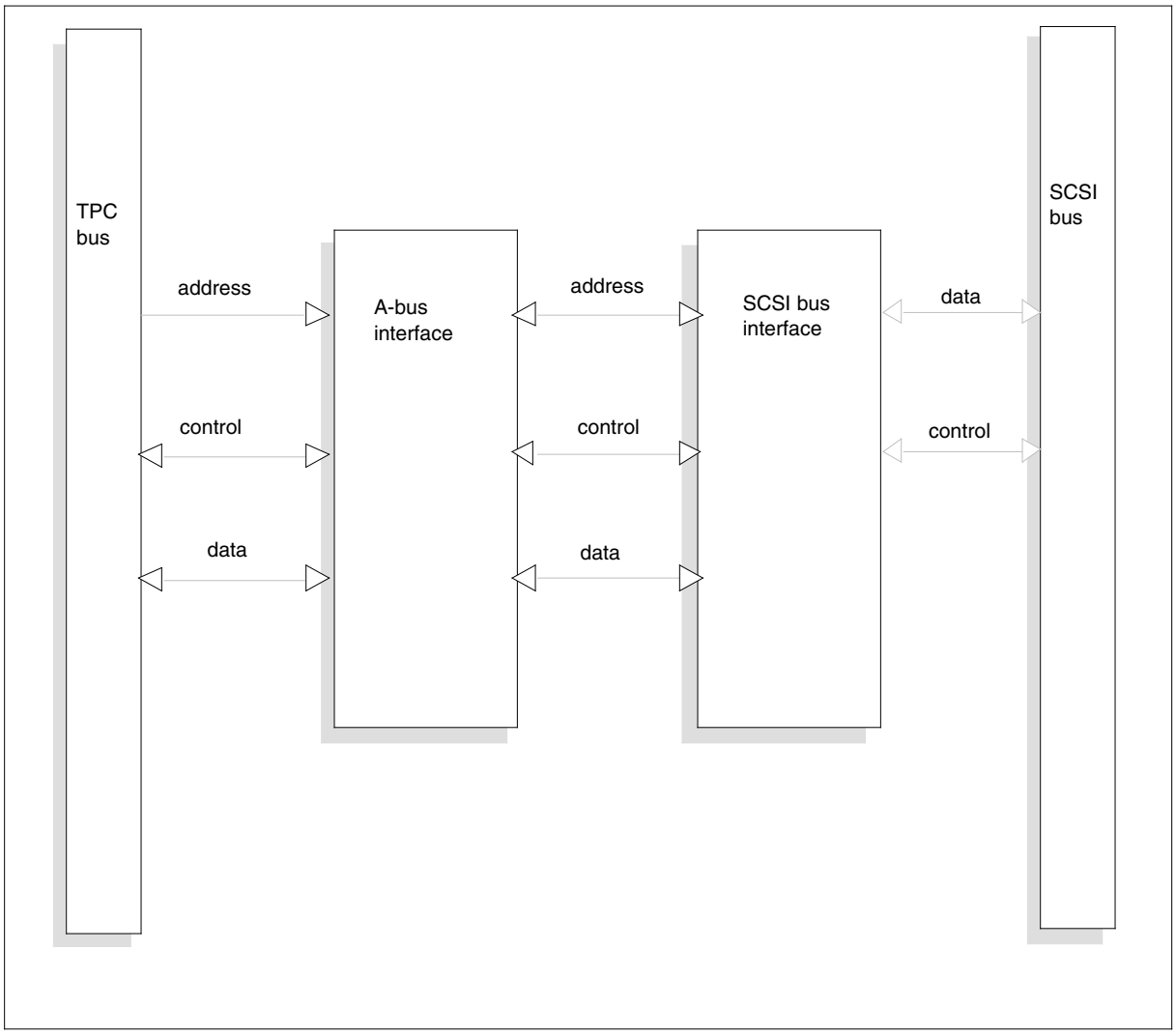
The SCSI interface allows the NTNX65BA to communicate with:

- the floppy disk and controller pack (NTNX68CA)
- the Winchester disk and controller pack (NTNX68DA).

The NTNX65BA is the master device on the SCSI bus when the NTNX65BA communicates with the disk drive controllers.

The relationship between the functional blocks appears in the following figure.

**NTNX65BA functional blocks**



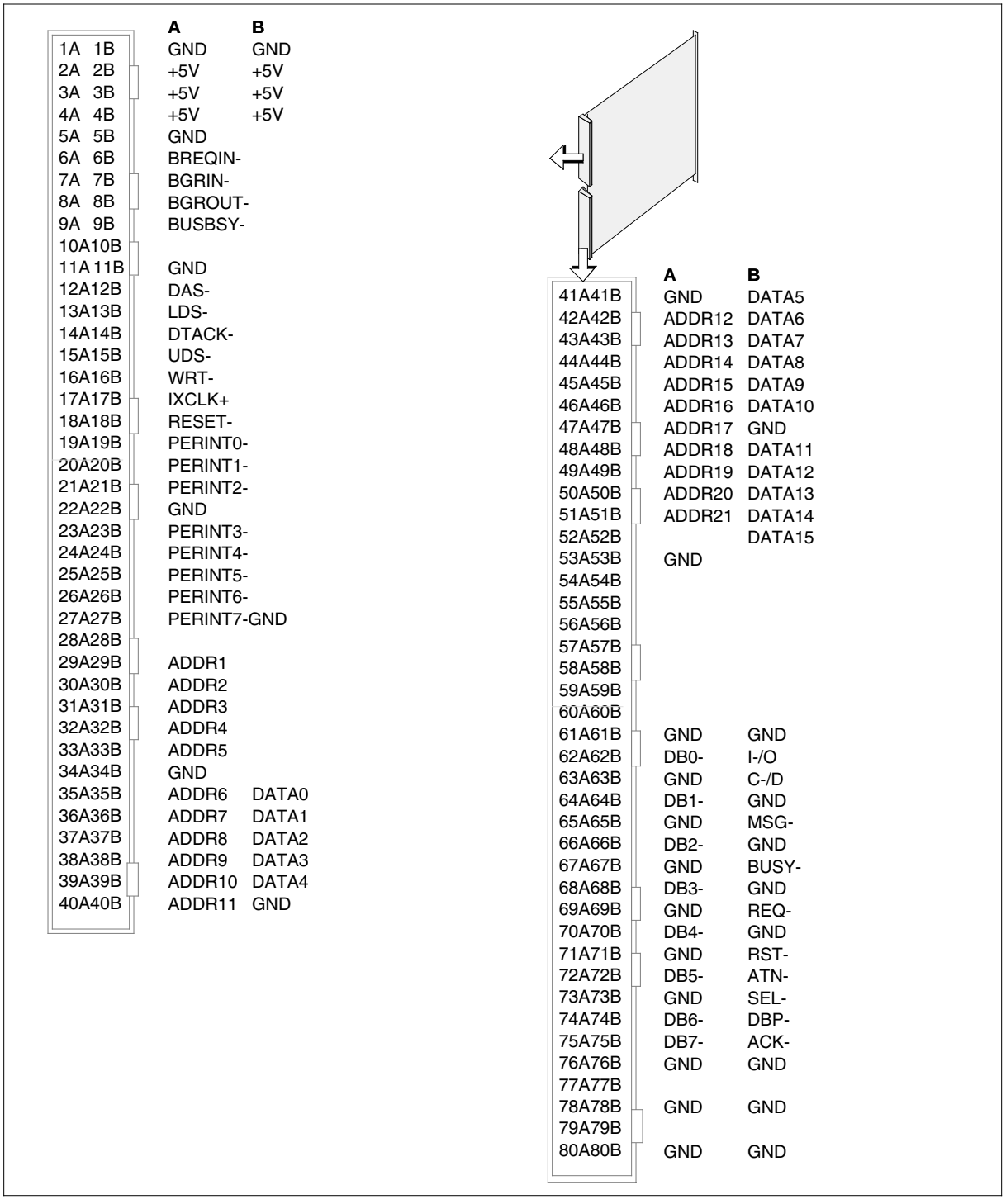

# Signaling

## Pin numbers

The pin numbers for the NTNX65BA appear in the following figure.

# **NTNX65BA** (continued)

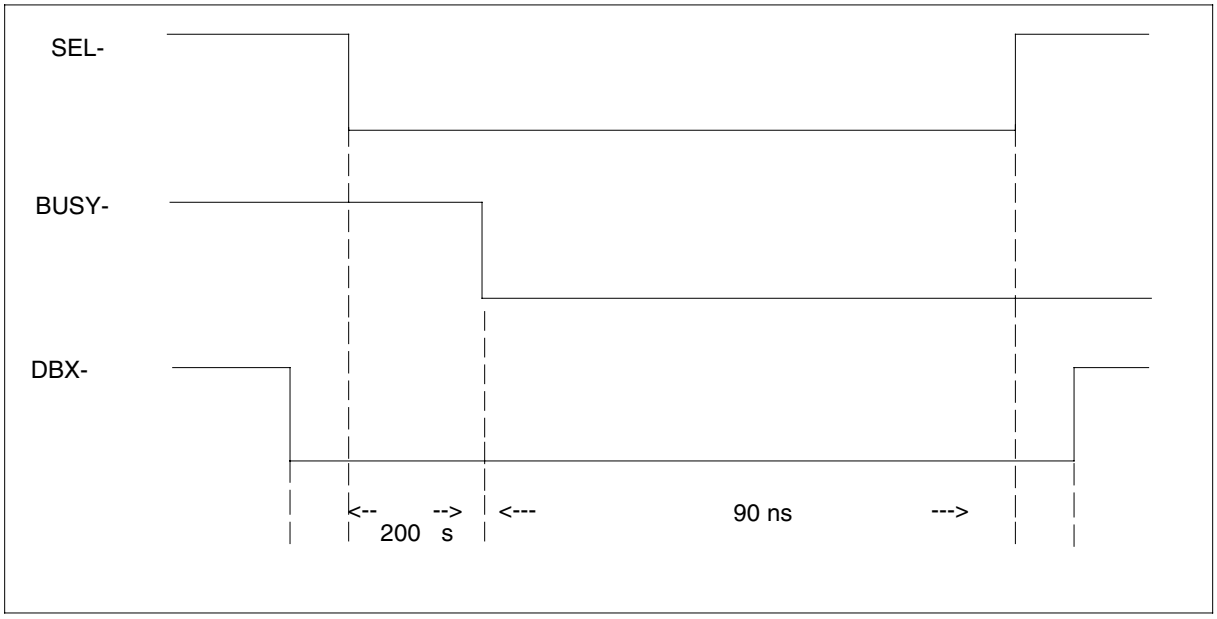
### NTNX65BA pin numbers



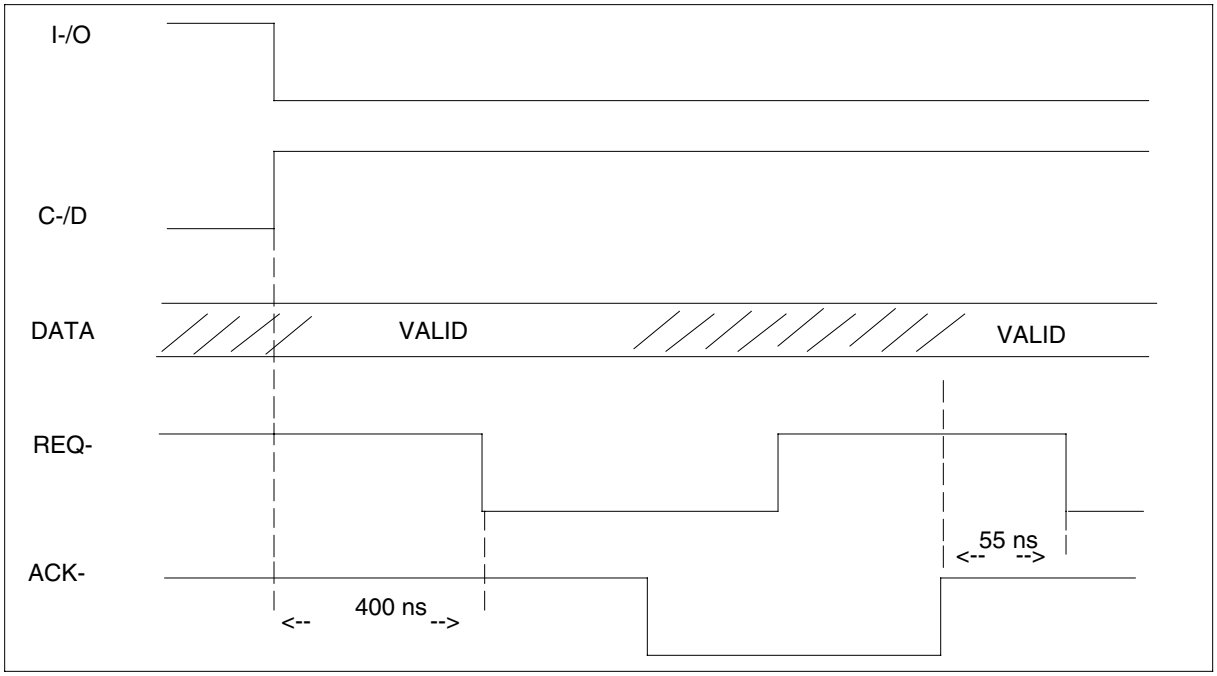
### Timing

The timing for the NTNX65BA appears in the following figures.

**NTNX65BA to disk pack controller select timing**

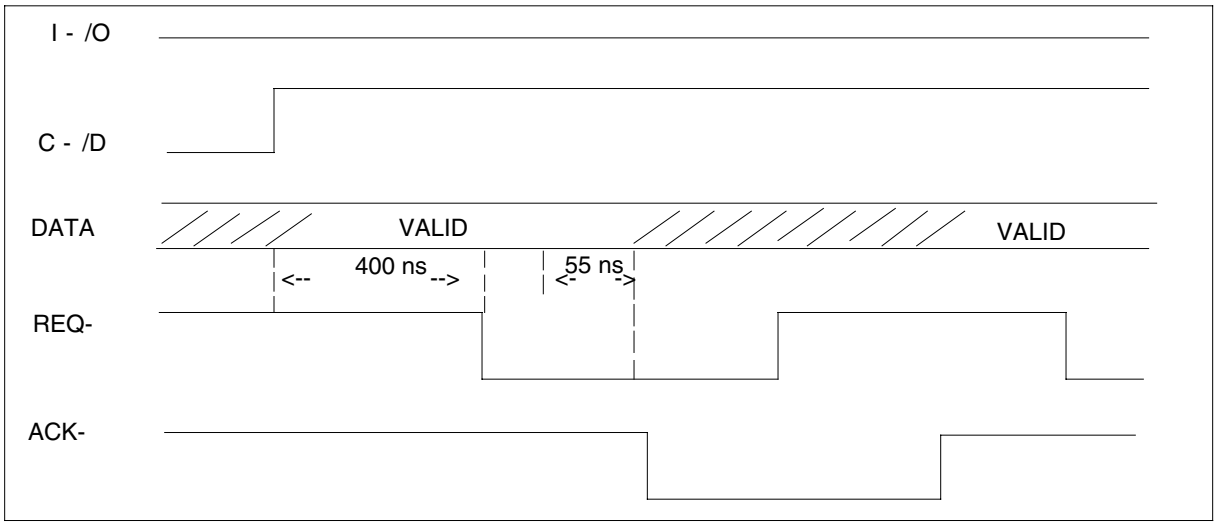



**NTNX65BA data timing from disk packs NTNX68CA/NTNX68DA**



## **NTNX65BA** (end)

**NTNX65BA data timing to disk packs NTNX68CA/NTNX68DA**




# Technical data

### Power requirements

The nominal supply voltage for the NTNX65BA is 5 V and the nominal supply current is 2 A.

# 13 NTNYnnaa

## NTNY01AA through NTNY23AA

# NTNY01AA

## Product description

The NTNY01AA Universal Edge 9000 (UE9000) DMS Bay frame provides the following loop services and functions to the DMS-100 switch and to core data network typologies:

- all current DMS voice band services found on line concentrating modules (LCM), except for coin, P-phone, ISDN, and 1MM
- termination of certain multi-megabit subscriber loop data services, including asymmetrical digital subscriber line (ADSL) discreet multi-tone (DMT) and ADSL G.Lite (future)
- interface into the line group controller (LGC) / line trunk controller (LTC) / remote cluster controller 2 (RCC2) through DS-30B links
- shelf interface into third-party ATM network edge switch equipment and associated element management system
- shelf interface to DMS battery plant, Metallic Test Access resources, and system alarms

## Parts

The NTNY01AA consists of different equipment shelves and the following components, of which the shelf, cooling unit, and breaker interface panel are discussed next:

- NTNP10BA UE9000 shelf
- NTNY17AA breaker interface panel (BIP)
- NTNY18AA UE9000 cooling unit (CU) shelf
- NT7E70AA FiberWorld 7 ft. frame
- NT4K15CA air filter unit assembly
- NT4K13AA drip tray

### NTNP10BA UE9000 shelf

The UE9000 shelf has the following features:

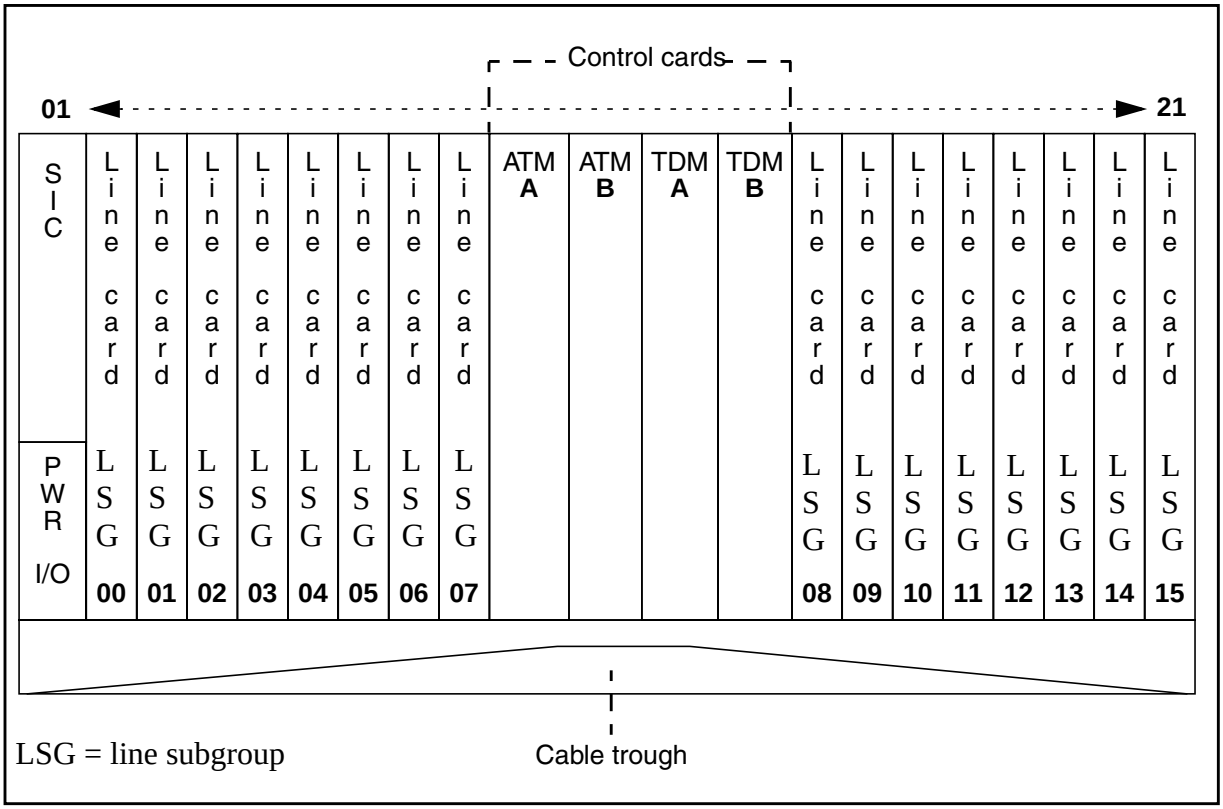
- 21 card positions that contain up to
  - — 16 multi-line cards
  - — 2 voice control cards
  - — 2 data control cards

  Slot 1 contains the following two cards (one above the other)
  - — one for power input/output
  - — one for shelf interface card
- backplane guide pins for card alignment
- card keying that provides 64 key positions
- front access of cards, connectors, and cabling
- removable front cover

The following figure provides a front view of the UE9000 shelf assembly showing slot assignments and line card / line subgroup numbering schemes.

## **NTNY01AA** (continued)

**NTNP10BA: UE9000 DMS shelf assembly: front view**




### NTNY17AA breaker interface panel

The NTNY17AA breaker interface panel (BIP)

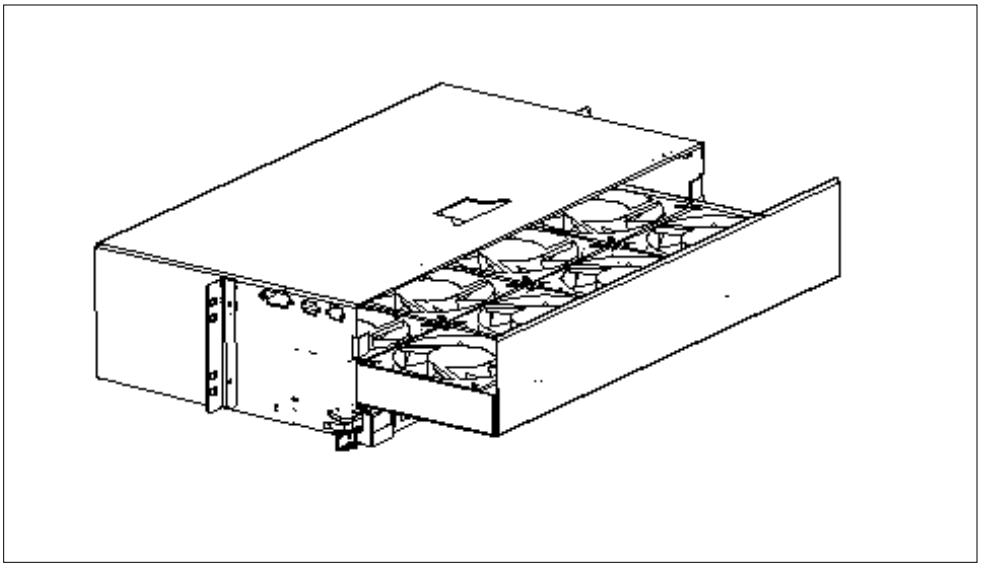
- collects and distributes power and alarm cabling for the UE9000 frame
- supports up to 120 A of power to frame assemblies

The BIP is mounted at the top of a UE9000 DMS or Media Gateway (MG) Bay frame.

### NTNY18AA UE9000 CU shelf

The CU shelf contains eight 5-inch square fan assemblies that provide approximately 600 CFM of air. The following figure shows the NTNY18AA cooling unit.

**NYNT18AA cooling unit shelf**

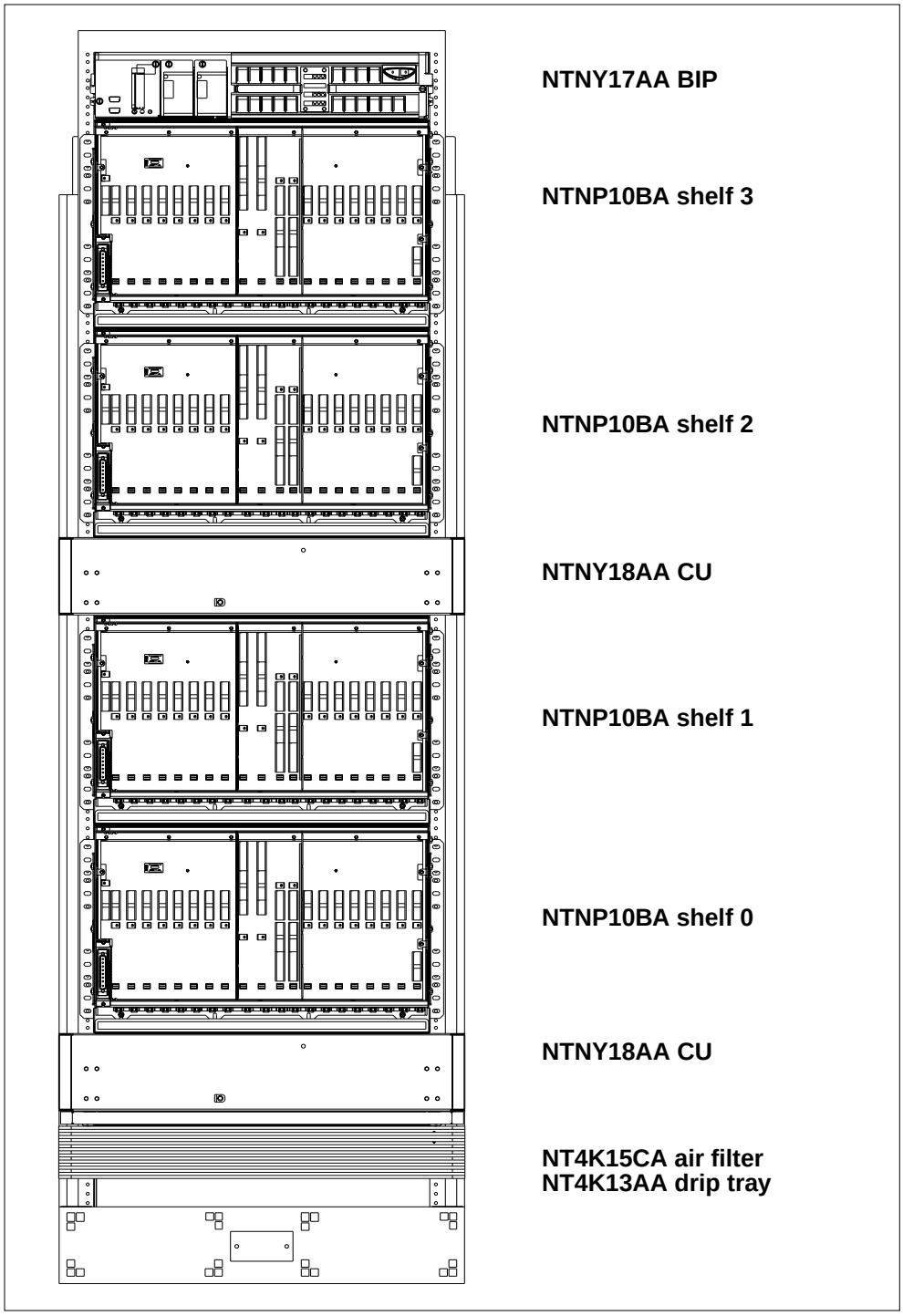


## Design

The design of the NTNY01AA appears in the following figure.

## **NTNY01AA** (continued)

**NTNY01AA equipment frame components**




***Note 1:*** This diagram is not to scale.

***Note 2:*** This gure sho ws the NTNY01AA with all provisionable shelves added.

## **NTNY01AA** (end)

# NTNY17AA

## Product description

The NTNY17AA breaker interface panel (BIP) shelf

- collects and distributes power and alarm cabling for the Universal Edge 9000 (UE9000) frame
- supports up to 120 A of power to frame assemblies

The BIP is mounted at the top of a UE9000 frame.

## Components

The NTNY17AA includes the components that follow:

- NTNY24AA alarm card
- NTNY25AA talk battery filters
- breakers
- power connections for input power
- power cable stubs for shelf power
- aisle alarm connections

### NTNY25AA: Talk battery filter

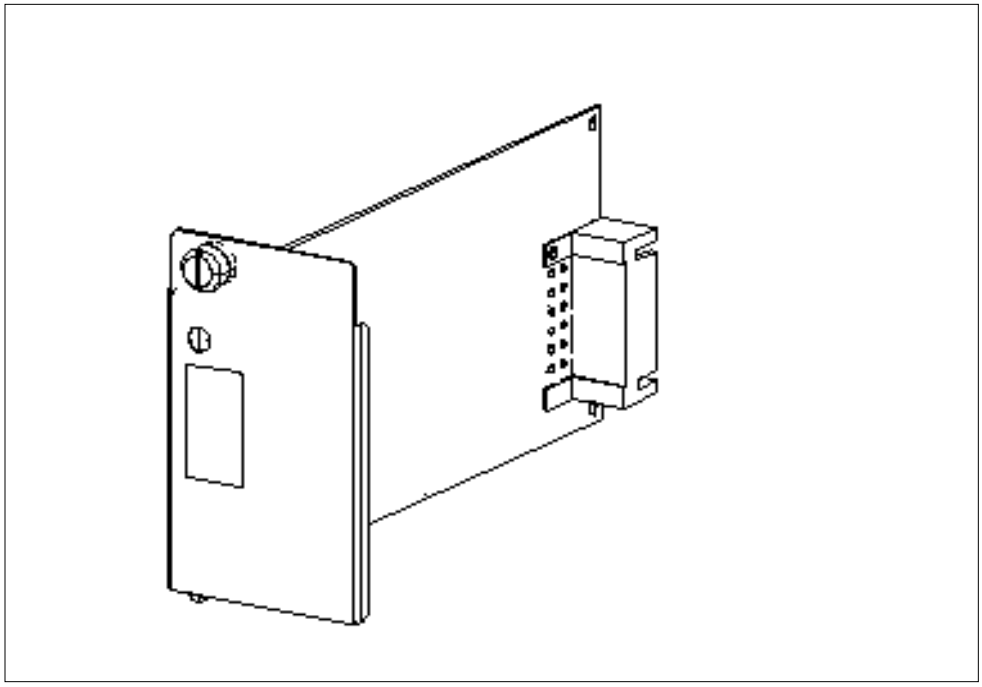
Up to two NTNY25AA talk battery filter modules mount inside the BIP. The two talk battery filters are Diode-Or'd. The NTNY25AA provides the following functions.

- a filtered power feed battery supply for subscriber loops
- an alarm when a capacitor fuse fails
- a "walk-in" feature for capacitor charging that limits inrush current

The following figure shows the talk battery filter module.

## **NTNY17AA** (continued)

**NTNY25AA talk battery filter**



### NTNY24AA: Alarm card assembly

The NTNY24AA Alarm Card

- collects
  - — alarm contacts from the fuses and circuit breakers in the BIP
  - — alarms from the four UE9000 DMS shelves and two cooling unit shelves
- provides 1 alarm for each scan point for transmission to scan points on an office alarm unit (OAU) elsewhere in the DMS system.

Alarm collection output lights a frame-level LED and an aisle lamp. The output returns to the UE9000 DMS for distributions to the UE9000 DMS common equipment.

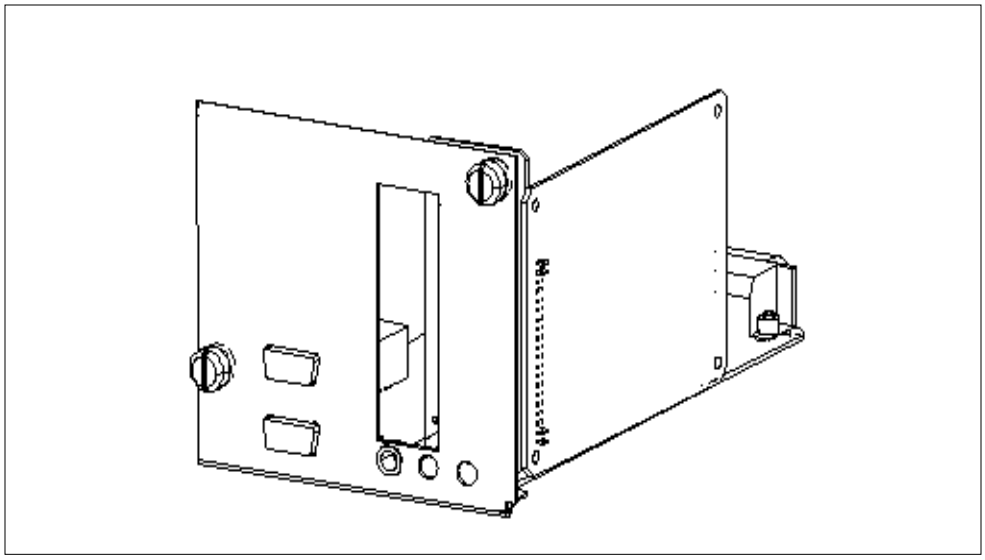
The alarm card monitors:

- ABS and ABS return
- converter fail for PUPS on UE9000 DMS cards
- fan fail

- operation of circuit breakers or fuses in the BIP in response to an overcurrent on a branch
- ringing generator fail
- talk battery fail

For each UE9000 shelf, each circuit card provides an alarm output to indicate hardware failures that normal software audits are unable to detect. Failure of the PUPS is monitored and individual circuit cards can have other sources of failure that require frame alarm generation. The alarm outputs form the UE9000 circuit cards are collected at the shelf interconnect card and control the shelf alarm indication the BIP. The following figure shows the alarm card.

**NTNY24AA alarm card**



## Signal battery distribution

Signal battery to the UE9000 shelves is redundant to prevent loss of service caused by signal battery plant failure.

Signal battery feeds are protected by two 15A breakers/shelf located in the BIP and by 1A fuses on each circuit card for the UE9000 loads.

## **NTNY17AA** (end)

### Talk battery distribution

The UE9000 shelves require two TBF filters in the BIP to ensure a noise-free DC supply for subscriber loops. Each TBF has

- 4 associated 15A circuit breakers in the BIP to protect current to the shelves
- 1 10A fuse at the shelf interconnect card

To accommodate a customer requirement, talk battery is not redundant to the UE9000 shelves. The system can run in simplex mode to reduce battery depletion during ac power outages. Both an A and a B feed are supplied to each shelf. A talk battery A feed supplies the line cards on the left half of the shelf, and a talk battery B feed supplies the line cards on the right half.

# NTNY23AA

## Product description

The NTNY23AA Shelf Interconnect card (SIC) is used in the Universal Edge 9000 shelf.

### Location

The NTNY23AA resides in the upper half of slot 0 in the UE9000 shelf.

## Functional description

The NTNY23AA Shelf Interface card works with the NTNY17AA Breaker Interface panel (BIP) relay alarm card to provide

- an interface to the BIP via an RS422 duplex interconnect. Over this link, instructions to and from the BIP facilitate the following features
  - — station alarms (Critical/Major/Minor) can be originated from the UE9000 shelf.
  - — user Alarm Outputs can be originated in the UE9000 shelf
  - — user outputs from the BIP are available
  - — user Alarm Inputs to the BIP are available to the UE9000 shelf. These are inputs to the BIP (such as door alarms / station or cabinet power alarms) which are broadcast to all the UE9000 shelves over the RS422 links. User alarm inputs are available.
- a unique frame ID from the BIP alarm card to the UE9000 shelves in a frame to facilitate auto discovery at a frame level.
- unique shelf ID from the BIP alarm card via the BIP/SIC cable to each of the four UE9000 shelves in a frame to facilitate auto discovery at a shelf level.
- a hardwired line card cutover function which allows all cutover relays on all of the line cards in the shelf to be held open during installation and board-to-board testing, regardless of the state of the system software, so long as signal and talk batteries are maintained to the shelf.
- control for the Metallic Test Access buses for the UE9000 shelf. Both buses A and B are available on 9-pin D-subs on the SIC front plate. Two D-subs are provided on the front plate, wired through a relay matrix, that provides the following functions for each of the test pairs of the two test buses:
  - — a bypass of the shelf for the frame test pairs for metallic testing of wideband services on other shelves without the parasitics of the shelf.
  - — a means of terminating the descending frame test pairs onto the shelf's backplane test pairs and disconnect the descending frame test pairs for

## **NTNY23AA** (continued)

metallic testing of wideband services on the shelf without the parasitics of shelves above.

— a means of terminating the ascending frame test pairs onto the shelf's backplane test pairs and disconnect the descending frame test pairs for metallic testing of wideband services on the shelf without the parasitics of shelves below.

— a means of 'bridging' the shelf test pairs onto the frame test pairs for metallic testing of narrowband services on the shelf to provide the "daisy-chain" functionality

— provide a means of "loop back" of the frame test pairs utilizing relay matrix for verification of the metallic test access facilities

- the voltage threshold monitoring for the UE9000 shelf. Both Signal battery supplies A and B and Talk Battery supplies A and B are monitored onto the shelf.
- the voltage threshold monitoring of both signal battery supplies A and B on board the UE9000 SIC to report loss of power redundancy on the UE9000 SIC due to a fuse failure on the SIC. This added functionality was added to this non-redundant pack to detect the previously undetectable simplex power fault of the SIC due to a blown fuse on the circuit card.
- an interface for the shelf serial IDPROM. The IDPROM is actually positioned on the NTNP20AA Power I/O Card as a 'permanent' part of the shelf. The SIC card provides both the write and read facility for this PROM. A write protect facility prevents the IDPROM from being over-written in the case of a hardware or software failure.
- three LED's similar to the other resident cards in the UE9000 shelf. The function of the LED's are:

  — SIC Card Fail. This red LED is powered directly from the TDM card through the backplane.

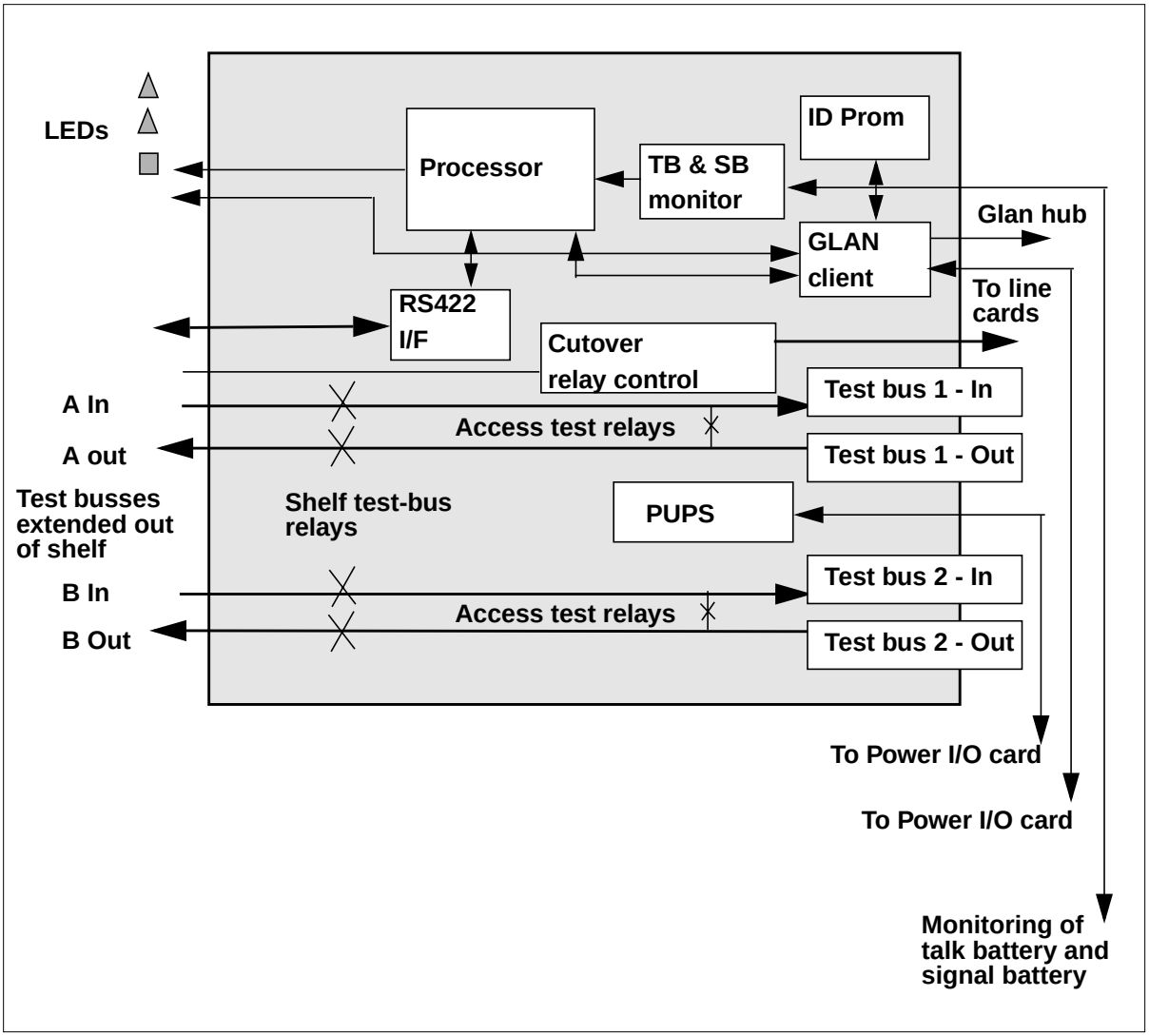
  — Shelf Fail. This red LED is controlled by the on board micro controller and can be lit by commands to the SIC.

  — Card Active. This green LED is controlled by the GLAN interface on the SIC and is powered when the SIC is in its normal working state.
- all I/O faceplate access points to the SIC card are 1500V isolated from the logic circuitry on the SIC.
- the SIC interface to the backplane is via the GLAN. This is a point to point LAN from a hub on the TDM Control Card.
- is smaller than the other provisionable cards in the NTNP10BA shelf
- provides cutover relay control

The TDM and ATM common equipment cards can operate the interface circuits through messaging across the GLAN messaging links.

The figure that follows shows the relationship of the functional blocks.

**NTNY23AA functional blocks**



## **NTNY23AA** (continued)

# Signaling

### Pin outs

The figure that follows shows the pin outs for NTNY23AA.

**NTNY23AA RS-422 alarm interface connector pin outs**

| | |
|---|---|
| 1 | RXD+ |
| 2 | RXD- |
| 3 | SHFIDBIT2 |
| 4 | SHFIDBIT1 |
| 5 | SHFIDBIT0 |
| 6 | AIFGND |
| 7 | TXD- |
| 8 | TXD+ |

**NTNY23AA cutover jumper pin outs**

| | |
|---|---|
| 1 | CORLY1 |
| 2 | CORLY2 |

**NTNY23AA upper and lower MTA connector pin outs**

| | |
|---|---|
| 1 | TB1_AIR |
| 2 | TB2_AIR |
| 3 | Not connected |
| 4 | TB1_AOR |
| 5 | TB2_AOR |
| 6 | TB1_AIT |
| 7 | TB2_AIT |
| 8 | TB1_AOT |
| 9 | TB2_AOT |

**NTNY23AA backplane connector pin outs**

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | SHFIDD0 | SHFIDCS | SHFIDWE | SHFIDDI | SHFID5V |
| 2A 2B 2C 2D 2E | SHFIDCK | GND | GND | SHFID5V | SHFID5V |
| 3A 3B 3C 3D 3E | NC | NC | NC | NC | NC |
| 4A 4B 4C 4D 4E | SBRTN | SBRTN | SBRTN | SBRTN | SBRTN |
| 5A 5B 5C 5D 5E | SBA | SBA | SBA | SBA | SBA |
| 6A 6B 6C 6D 6E | SBB | SBB | SBB | SBB | SBB |
| 7A 7B 7C 7D 7E | NC | NC | NC | NC | NC |
| 8A 8B 8C 8D 8E | TBRTN | TBRTN | TBRTN | TBRTN | TBRTN |
| 9A 9B 9C 9D 9E | TBA | TBA | CORLY | TBB | TBB |
| 10A 10B 10C 10D 10E | NC | NC | NC | NC | NC |
| 11A 11B 11C 11D 11E | TB2_AOR | TB2_AOT | NC | TB2_AIR | TB2_AIT |
| 12A 12B 12C 12D 12E | NC | NC | NC | NC | NC |
| 13A 13B 13C 13D 13E | NC | NC | NC | NC | NC |
| 14A 14B 14C 14D 14E | NC | NC | NC | NC | NC |
| 15A 15B 15C 15D 15E | TB1_AOR | TB1_AOT | NC | TB1_AIR | TB1_AIT |
| 16A 16B 16C 16D 16E | NC | NC | NC | NC | NC |
| 17A 17B 17C 17D 17E | GND | GND | COL4 | GND | GND |
| 18A 18B 18C 18D 18E | GND | CLKB01 | GND | CLKA01 | GND |
| 19A 19B 19C 19D 19E | GND | GND | ROW1 | GND | GND |
| 20A 20B 20C 20D 20E | TDMADS01 | GND | GND | GND | TDMBDS01 |
| 21A 21B 21C 21D 21E | GND | GND | GND | GND | GND |
| 22A 22B 22C 22D 22E | GLANBUS0 | GLANBDS01 | GND | GLANAUS01 | GLANADS01 |
| 23A 23B 23C 23D 23E | PLANSEL2 | PLANSEL1 | GND | PLANSEL0 | GND |
| 24A 24B 24C 24D 24E | GND | GND | GND | GND | GND |
| 25A 25B 25C 25D 25E | SHFRBIT0 | SHFRBIT1 | GND | SHFRBIT2 | SHFRBIT3 |

# Technical data

## Power requirements

The NTNY23AA has the following power requirements

- -40 V minimum
- -48 V nominal
- -60 V maximum

# 14 NTRXnnaa

## NTRX2572 through NTRX91AA

# NTRX2572

## Product description

The NTRX2572 spare fuse holder stores additional fuses. The NTRX3135 and NTRX3145 kits provide this spare fuse holder. Each fuse holder stores 18 fuses, 9 on the top shelf and 9 on the bottom shelf.

### Location

The spare fuse holder occupies the 10th slot in a modular supervisory panel (MSP) of a cabinetized power distribution center (CPDC) and cabinetized remote miscellaneous equipment (CRME).

## Functional description

The NTRX2572 is a part of the NTRX3135 and NTRX3145 CPDC MSP kit. The NTRX2572 contains the following:

- MSP
- alarm module
- breaker module
- thermal breaker module
- power alarm module
- ABS module
- cable assemblies
- fuses
- hardware to mount the fuse holder

The NTRX3135 CPDC MSP kit and NTRX3145 CPDC MSP kit contain a NTRX2572 Spare fuse holder.

### Dimensions

The following are the dimensions for the NTRX2572:

- height: 262 mm (10.3 in.)
- depth: 318 mm (12.5 in.)
- width: 28.5 mm (1.125 in.)

## Design

The following tables describe the main parts that the NTRX3135 and NTRX3145 CPDC MSP kits contain. The design of the NTRX2572 appears in the following figure.

**NTRX3135 CPDC MSP kit (Sheet 1 of 2)**

| Quantity | PEC | CPC | Description |
|---|---|---|---|
| 1 | NTRX40AA | B0233244 | Modular supervisory panel |
| 1 | NTRX41AA | B0233284 | Alarm module |
| 1 | NTRX42AA | B0233282 | Breaker module |
| 1 | NTRX43AA | B0233281 | Thermal breaker module |
| 1 | NTRX41BA | B0237148 | Power alarm module |
| 1 | NTRX4105 | B0237149 | power alarm back panel PCP |
| 1 | NTRX41EA | B0237334 | ABS module |
| 1 | | P0739810 | Designation label |
| 5 | | P097P242 | Fuse block designation |
| 5 | | A0205209 | Fuse, 3/4 A |
| 2 | NTRX4064 | B0237332 | ABS CB cable assembly |
| 1 | NTRX4065 | B0237331 | ABS TB cable assembly |
| 2 | NTRX4070 | B0237654 | MSP power cable assembly |
| 1 | NTRX4071 | B0237653 | MSP alarm jumper |
| 2 | NTRX4072 | B0237652 | EAS jumper cable assembly |
| 1 | NTRX4074 | B0237719 | MSP cable assembly |
| 2 | NTRX4086 | B0237829 | MSP jumper cable assembly |
| 3 | | A0205210 | Dummy fuse |
| 1 | | P0741149 | Fuse designation label |
| 2 | | P0739591 | Shelf spacer bracket |
| 4 | | P0734474 | Rear panel, blank, 4.80 in. |

## NTRX2572 (continued)

**NTRX3135 CPDC MSP kit (Sheet 2 of 2)**

| Quantity | PEC | CPC | Description |
|---|---|---|---|
| 5 | | P0734476 | Rear panel, blank, 1.20 in. |
| 34 | | P0559409 | Screw, tapping |
| 1 | NTRX4073 | B0237651 | MSP cable assembly |
| 1 | NTRX4085 | B0237830 | MSP alarm cable assembly |
| 1 | | P0737433 | Cover, contact |
| 4 | | P097F813 | Screw, .216-24 by .500 STL |
| 1 | | P0183220 | Lockwasher, ext .211 ID |
| 1 | | P0284154 | Washer, flat, metallic |
| 1 | | P0746307 | CB label |
| 1 | | P0734475 | Rear panel, blank, 2.40 in. |
| 1 | NTRX2572 | B0242602 | Spare fuse holder |

**NTRX3145 CPDC MSP kit (Sheet 1 of 2)**

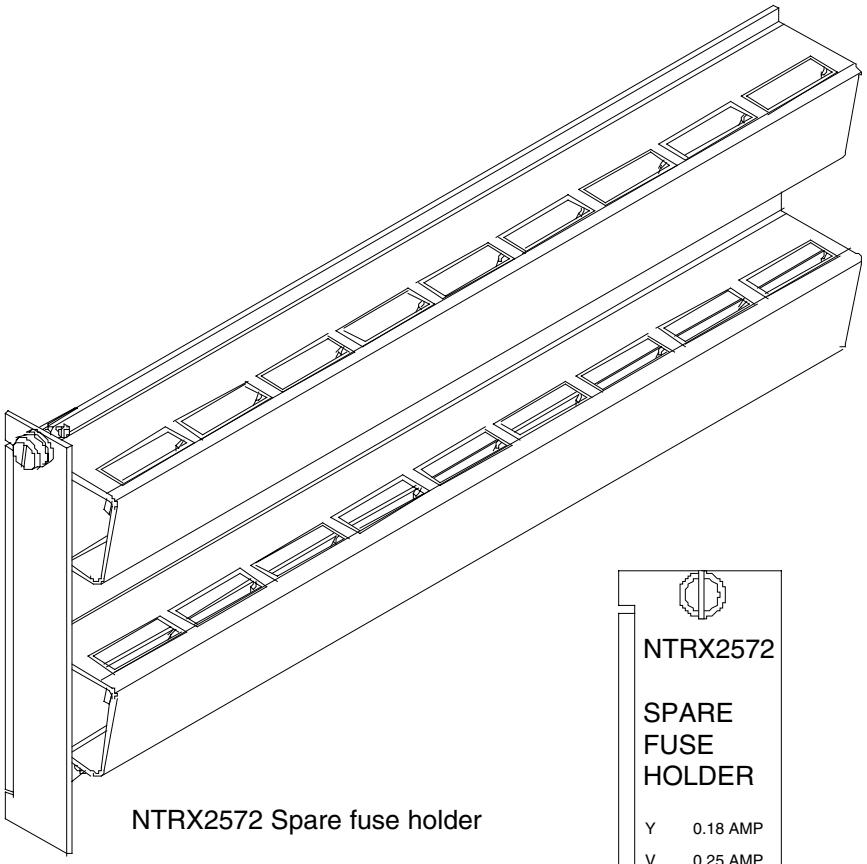
| Quantity | PEC | CPC | Description |
|---|---|---|---|
| 1 | NTRX40AA | B0233244 | Modular supervisory panel |
| 1 | NTRX41AA | B0233284 | Alarm module |
| 1 | NTRX42AA | B0233282 | Breaker module |
| 1 | NTRX43AA | B0233281 | Thermal breaker module |
| 1 | NTRX41BA | B0237148 | Power alarm module |
| 1 | NTRX4105 | B0237149 | power alarm back panel PCP |
| 1 | NTRX41EA | B0237334 | ABS module |
| 1 | | P0739810 | Designation label |
| 5 | | P097P242 | Fuse block designation |
| 5 | | A0205209 | Fuse, 3/4 A |
| 2 | NTRX4064 | B0237332 | ABS CB cable assembly |

**NTRX3145 CPDC MSP kit (Sheet 2 of 2)**

| Quantity | PEC | CPC | Description |
|---|---|---|---|
| 1 | NTRX4065 | B0237331 | ABS TB cable assembly |
| 2 | NTRX4070 | B0237654 | MSP power cable assembly |
| 1 | NTRX4071 | B0237653 | MSP alarm jumper |
| 2 | NTRX4072 | B0237652 | EAS jumper cable assembly |
| 1 | NTRX4074 | B0237719 | MSP cable assembly |
| 2 | NTRX4086 | B0237829 | MSP jumper cable assembly |
| 3 | | A0205210 | Dummy fuse |
| 2 | | P0739591 | Shelf spacer bracket |
| 4 | | P0734474 | Rear panel, blank, 4.80 in. |
| 5 | | P0734476 | Rear panel, blank, 1.20 in. |
| 34 | | P0559409 | Screw, tapping |
| 1 | NTRX4073 | B0237651 | MSP cable assembly |
| 1 | NTRX4085 | B0237830 | MSP alarm cable assembly |
| 1 | | P0745750 | Fuse designation |
| 1 | NTRX3138 | B0239513 | Alarm cable assembly |
| 1 | | P0746307 | CB label |
| 1 | | P0734475 | Rear panel, blank, 2.40 in. |
| 1 | NTRX2572 | B0242602 | Spare fuse holder |

## **NTRX2572** (continued)

**NTRX2572 fuse holder**



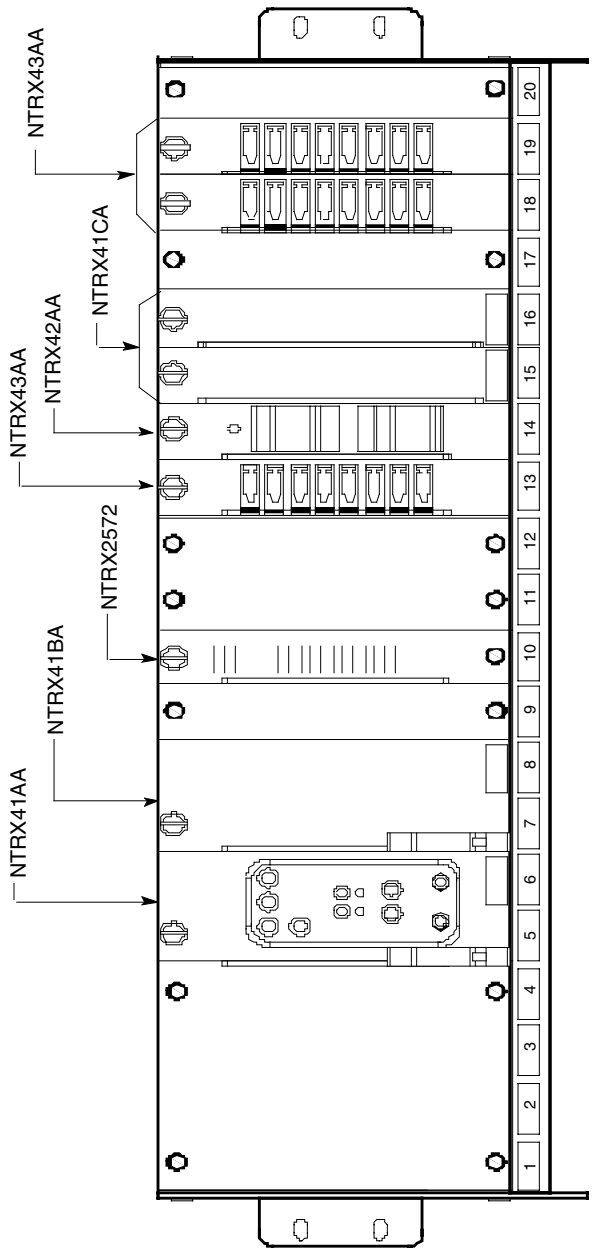
NTRX2572 Spare fuse holder




Front

**Note:** This diagram is not to scale.

**NTRX40AA front view with door open (NTRX3145 kit)**




**Note**: This diagram is not to scale.

# NTRX30AA

## Product description

The NTRX30AA cabinetized line concentration equipment (CLCE) maintains the current functionality of the DMS-100 LCE. The NTRX30AA contains two duplicated line concentrating modules (LCM).

Line drawer fusing is on the sides of the shelves for the NTRX30AA. The position of the fusing allows for an improved backpanel that combines two standard DMS-100 backplanes to one backplane. The backpanel decreases more than 50 percent of the line concentrating equipment cabling. The backpanel decreases the cabling because the one backpanel now contains the wiring between the two original backpanels. Some of the previous power connections between backpanel and line drawers now occur on a connectorized mounting plate at the rear of the cabinet. This mounting plate reduces noise and voltage drops.

## Parts

The NTRX30AA contains two provisionable NT6X30 ringing generators (RG). The NTRX30AA contains the following parts:

- NTMX26BA—Frame supervisory panel with cooling unit
- NTNX27DA—16 in. cooling unit
- NT6X04AB—Line concentrating modules

### Frame supervisory panel

The frame supervisory panel (FSP) is in the top of the cabinet at shelf position 61. The NTMX26BA FSP provides the following services to the CLCE:

- provides the normal functions of power distribution and alarms in the cabinet
- supports duplicated NT6X30 ringing generators, that are above the NTMX26BA FSP
- controls a pair of frame fail lights (NT9X0174), at the top of the cabinet. One frame fail light is at the front and the other is at the rear of the cabinet.
- includes an integral cooling unit, that the user can access from the rear of the cabinet

### 16-in. cooling unit

In addition to the cooling unit attached to the FSP, the NTRX30AA uses a separate cooling unit, NTNX27DA, at the bottom of the cabinet. The NTNX27DA unit uses dual-speed fans to provide forced-air cooling. The fans normally operate at a low speed to reduce noise reduction. The fans operate at a high speed when a thermal stress or fan fault condition occurs.

### Line concentrating modules

The NTRX30AA can be provisioned with a maximum of two LCMs. Each LCM has ten line drawers that provide a 640 line card capacity. Each line drawer contains two subgroups. Labels for the subgroups are on the front of the line drawer. A NTRX30AA can provision 1280 single line cards. Each LCM uses a single backplane for the duplicated controller, processor, and power converter cards. These cards are on the right side of the shelf. Removal of the line cards and installation at this location from the next line drawer can occur.

### Two ringing generators

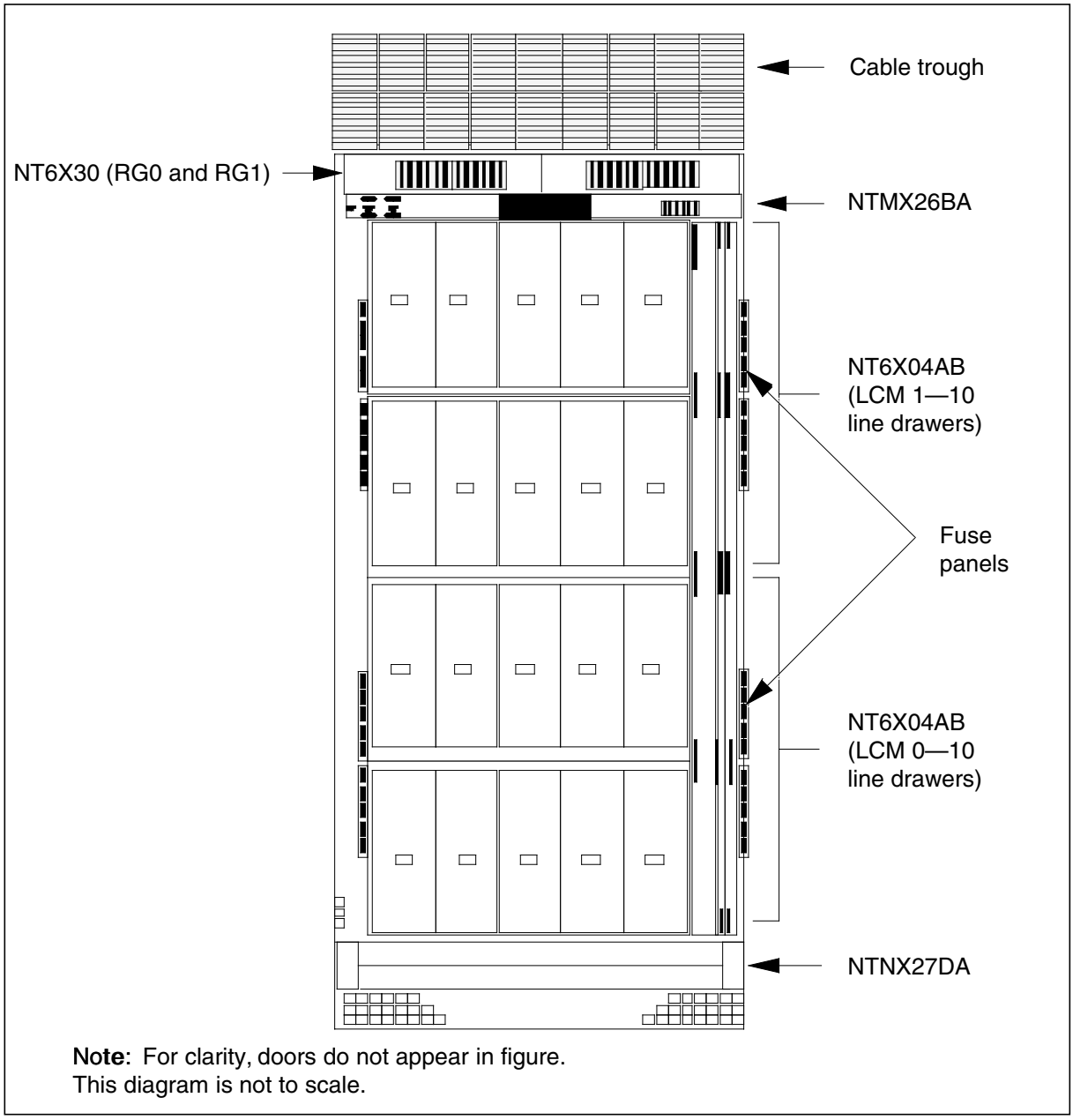
Two RGs attach with the FSP to the top of the frame. Each RG is a programmable generator that can output different ringing waveforms. An RG outputs waveforms when the RG receives a drive-signal.

## Design

The design of the NTRX30AA appears in the following figure.

# **NTRX30AA** (end)

**NTRX30AA parts**




**Note:** For clarity, doors do not appear in figure.
This diagram is not to scale.

# NTRX30BA

## Product description

The cabinetized line module ISDN (CLMI) contains two duplicated line concentrating modules (LCM) and can support ISDN services.

Fuse panels contain fuses for the line drawers. The fuse panels are in the appropriate LCMs at the right side of the shelf.

Each module has two backplanes.

## Parts

The NTRX30BA contains two NT6X30 ringing generators (RG), that can be provisioned, and the other following parts:

- NTBX31AA—LCMs
- NTMX26BA—Frame supervisory panel (FSP)
- NTNX27DA—Cooling unit

### Line concentrating modules

The NTRX30BA can be provisioned with a maximum of two LCMs. Each LCM has eight line drawers that provide 480 single-slot 2BIQ lines. Each line drawer contains two subgroups. Labels for the subgroups are on the front of the line drawer. An NTRX30BA can provision 1024 single line cards. Each LCM uses two backplanes for the duplicated controller, processor, and power converter cards. These cards are on the right side of the shelf. This location allows for easy removal or insertion of line from the next line drawer.

### Frame supervisory panel

The FSP is in the top of the cabinet at shelf position 61. The NTMX26BA FSP provides the following services to the NTRX30BA:

- provides the normal functions of power distribution and alarms in the cabinet
- supports duplicated NT6X30 ringing generators, that are above the NTMX26BA FSP
- controls a pair of frame fail lights (NT9X0174), at the top of the cabinet. One frame fail light is at the front and the other is at the rear of the cabinet.
- includes an integral cooling unit, that the user can access from the rear of the cabinet

### 16-in. cooling unit

In addition to the cooling unit attached to the FSP, the CLMI uses a separate cooling unit, NTNX27DA, at the bottom of the cabinet. The NTNX27DA uses

## **NTRX30BA** (continued)

dual-speed fans to provide forced-air cooling. The fans normally run at a low speed to reduce noise. The fans operate at a high speed when a thermal stress or fan fault condition occurs.

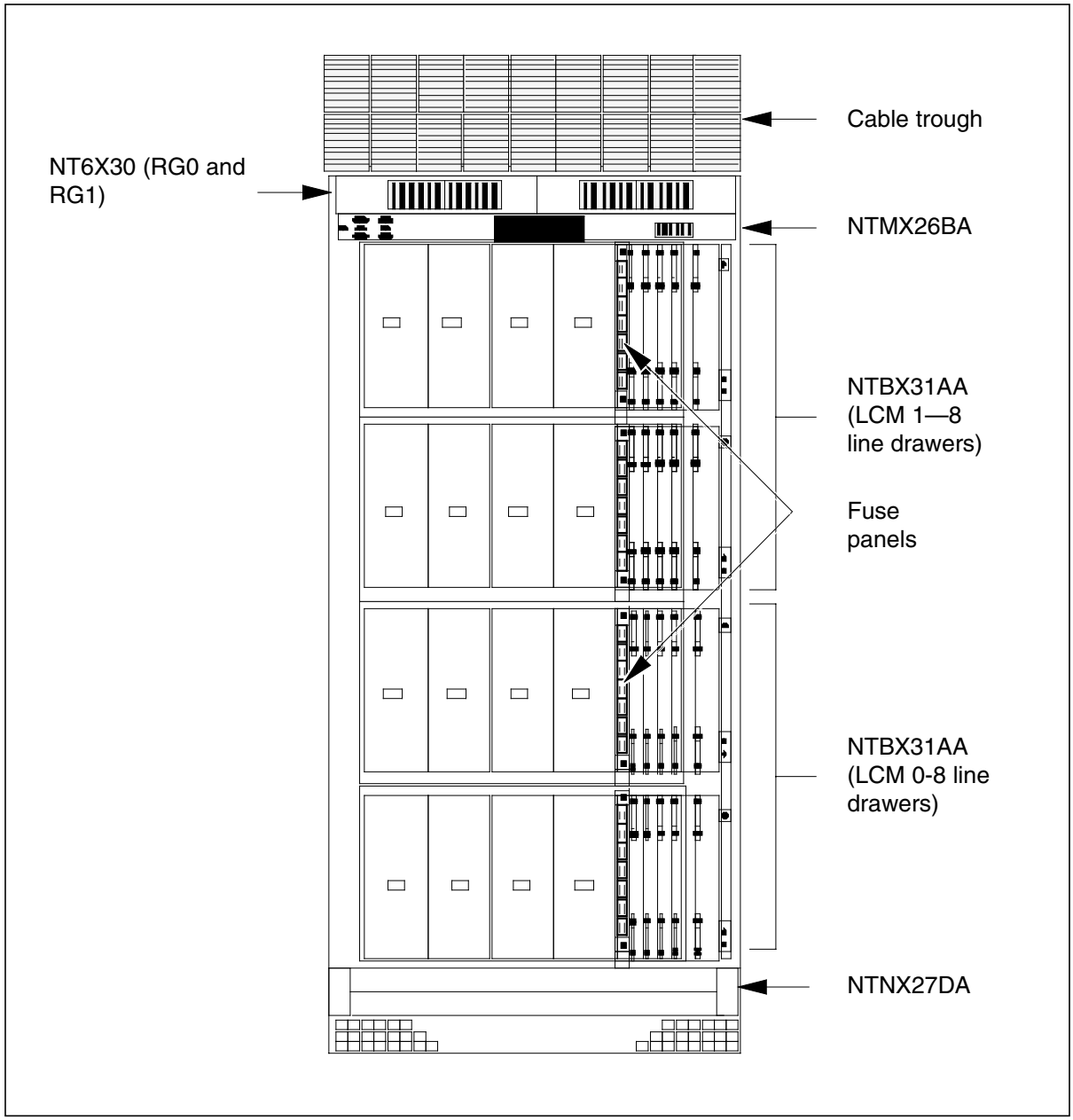
### Two ringing generators

Two RGs attach with the FSP to the top of the frame. Each RG is a programmable generator that can output different ringing waveforms when a correct drive-signal occurs.

## Design

The design of the NTRX30BA appears in the following figure.

**NTRX30BA parts**




***Note:*** For clarity, doors do not appear in figure. This diagram is not to scale.

# NTRX30CA

## Product description

The NTRX30CA cabinetized line concentration equipment (CLCE) maintains the current functionality of the DMS-100 LCE. The NTRX30CA contains two duplicated line concentrating modules (LCM).

Each LCM has ten line drawers that provide a capacity of a maximum of 640 line cards. An CLCE can provision a maximum of 1280 single line cards.

Each LCM also uses a single backplane for the duplicated controller, processor, and power converter cards. These cards are on the right side of each shelf. The location allows for easy removal and insertion of line cards from the next line drawer.

Line drawer fusing is on the sides of the appropriate shelves for the NTRX30CA. The position of the fusing allows for an improved backpanel that combines two standard DMS-100 backplanes. The backpanel decreases line concentrating equipment cabling by more than 50 percent. The backpanel decreases the cabling because the backpanel now contains the wiring between the two back panels. Some of the previous power connections between backpanel and line drawers now occur on a connectorized mounting plate at the rear of the cabinet. This mounting plate reduces noise and voltage drops.

An EMI filter adapter filters CLCE lines at the EMI bulkhead. The CLCE uses 78-pin D-sub connectors at the bulkhead and interfacing to 64-pin key telephone connectors mounted on the customer location distribution frames (DF blocks). A total of 40 tip and ring connector interfaces are available on the CLCE. Each tip and ring connector interface refers to one line sub group (LSG) of 32 lines. The filter meets EN Class B requirements.

## Parts

The NTRX30CA contains two provisionable NT6X30 ringing generators (RG) and the following parts:

- NTRX40AA—modular supervisory panel
- NTNX27DA—16-in. (406 mm) cooling unit
- NT6X04AB—line concentrating modules

### Modular supervisory panel

The modular supervisory panel (MSP) is in the top of the cabinet at shelf position 61. The NTRX40AA MSP provides the following services to the CLMI:

- normal functions of power distribution and alarms in the cabinet
- duplicated NT6X30 ringing generators, that are above the NTRX40AA
- control of a pair of frame fail lights (NT9X0174), at the top of the cabinet. One frame fail light is at the front and the other is at the rear of the cabinet.

### 16-in. cooling unit

The NTRX30CA uses a separate cooling unit, NTNX27DA, at the bottom of the cabinet. The cooling unit operates with 48-V and 60-V power. This NTNX27DA unit uses dual-speed fans to provide forced-air cooling. The fans normally run at a low speed to reduce noise. The fans operate at a high speed when a thermal stress or fan fault condition occurs.

### Line concentrating modules

The NTRX30CA can be provisioned with a maximum of two LCMs. Each LCM has ten line drawers that provide a 640 line card capacity. Each line drawer contains two subgroups. Labels for the subgroups are on the front of the line drawer. The NTRX30CA can provision 1280 single line cards. Each LCM uses a single backplane for the duplicated controller, processor, and power converter cards. These cards are on the right side of the shelf. This location allows for the easy removal or insertion of line cards from the next line drawer.

### Two ringing generators

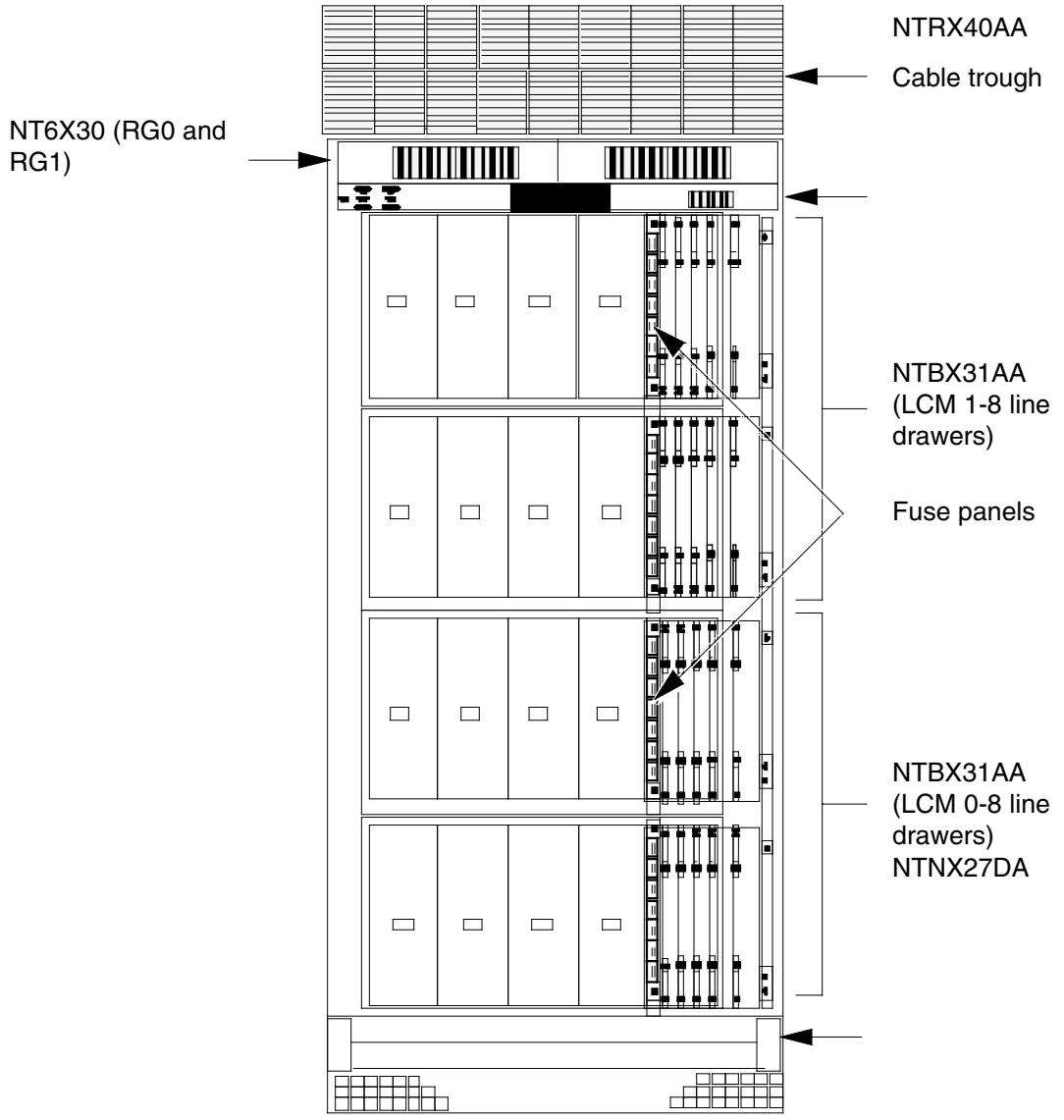
Two RGs attach with the FSP to the top of the frame. Each RG is programmable and can generate different ringing waveforms. The RG generates waveforms when the RG receives a drive signal.

## Design

The design of the NTRX30CA appears in the following figure.

# **NTRX30CA** (end)

**NTRX30CA parts**




**Note**: For clarity, doors do not appear in figure. This diagram is not to scale.

## Product description

The cabinetized line module ISDN (CLMI) contains two duplicated line concentrating modules (LCM) and supports integrated service digital network (ISDN) services. Each LCM has line drawers that provide a capacity of 480 lines. One CLMI can provide a maximum of 960 ISDN lines.

Fuse panels contain fuses for the line drawers. Fuse panels are in the appropriate LCMs at the right side of the shelf.

Each module has two backplanes.

An EMI filter adapter filters CLMI lines at the EMI bulkhead. The NTRX30DA uses 78-pin D-sub connectors at the bulkhead. The NTRX30DA interfaces to 64-pin key telephone connectors on the customer locations distribution frames (DF blocks). A total of 32 connector interfaces are available on the CLMI. Each connector interface corresponds to one line sub group (LSG) of 30 lines. The filter adapters meet EN Class B requirements.

## Parts

The NTRX30DA contains two provisionable NT6X30 ringing generators (RG) and the following parts:

- NTBX31AA—LCM
- NTRX40AA—modular supervisory panel (MSP)
- NTNX27DA—cooling unit, 406 mm (16 in)

### Line concentrating modules

The NTRX30DA can be provisioned with a maximum of two LCMs. Each LCM has eight line drawers that provide 480 single-slot 2BIQ lines. Each line drawer contains two subgroups. Labels for the subgroups are on the front of the line drawer. An NTRX30DA can provision 1024 single line cards. Each LCM uses two backplanes for the duplicated controller, processor, and power converter cards. These cards are on the right side of the shelf. The location allows for the removal or insertion of line cards from the next line drawer.

## **NTRX30DA** (continued)

### Modular supervisory panel

The MSP is in the top of the cabinet at shelf position 61. The NTRX40AA MSP provides the following services to the NTRX30DA:

- normal functions of power distribution and alarms in the cabinet
- duplicated NT6X30 ringing generators, that are above the NTRX30DA
- control of a pair of frame fail lights (NT9X0174), at the top of the cabinet. One frame fail light is at the front and the other is at the rear of the cabinet.

### 16-in. cooling unit

The CLCE uses a separate cooling unit, NTNX27DA, at the bottom of the cabinet. The cooling unit operates with 48V and 60V power. The NTNX27DA uses dual-speed fans to provide forced-air cooling. The fans normally run at a low speed to reduce noise. The fans operate at a high speed when a thermal stress or fan fault condition occurs.

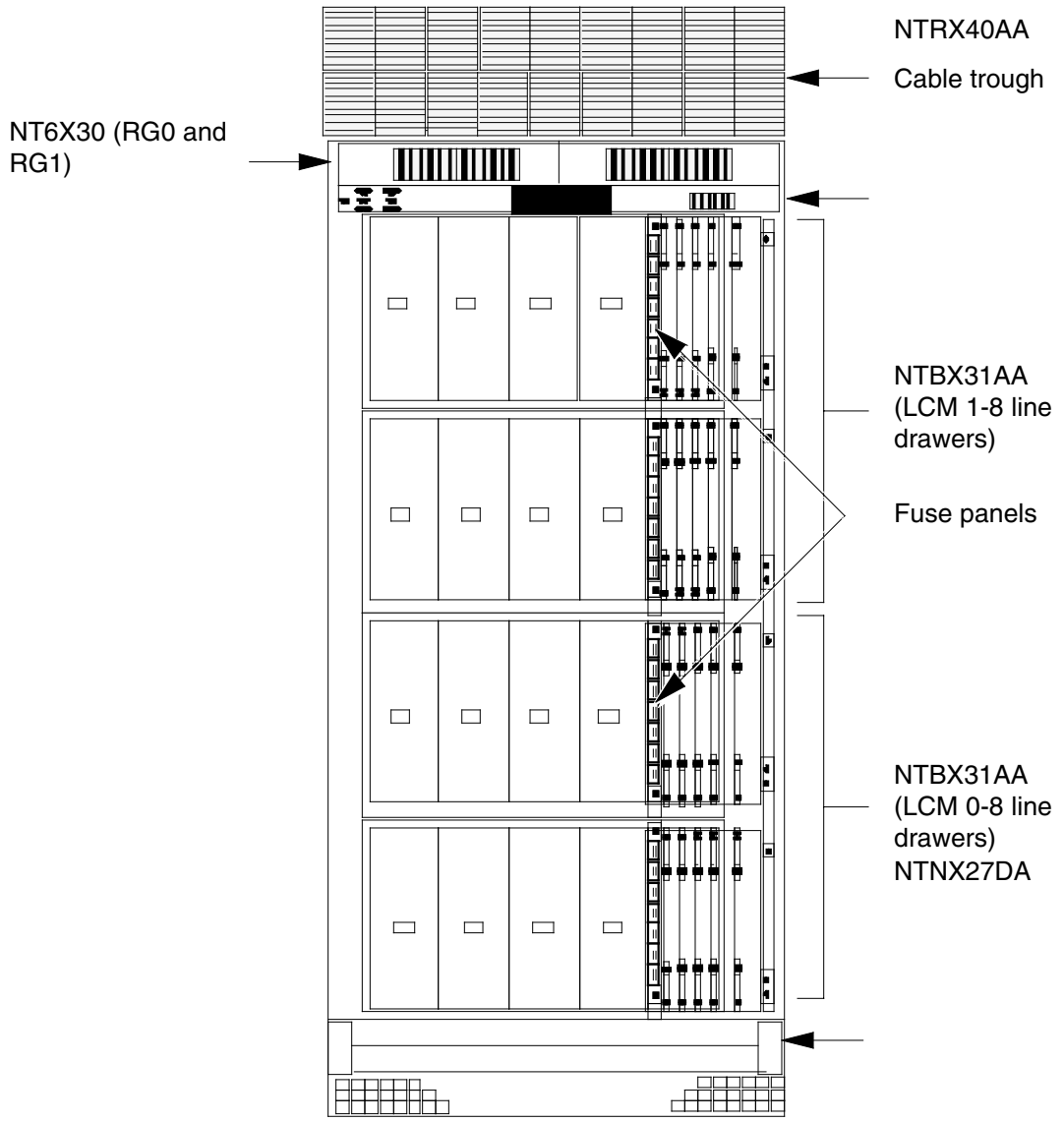
### Two ringing generators

Two RGs attach with the FSP to the top of the frame. Each RG is programmable and can generate different ringing waveforms. An RG generates waveforms when an RG receives a drive-signal.

## Design

The design of the NTRX30DA appears in the following figure.

**NTRX30DA parts**




**Note:** For clarity, doors do not appear in figure. This diagram is not to scale.

# NTRX31AA

## Product description

The cabinetized power distribution center (CPDC) is a single cabinet that distributes power to the cabinets in the appropriate lineup. The NTRX31AA provides dc power distribution and protection and optional inverted ac power for endguard outlets. The NTRX31AA is the first cabinet in a lineup of a maximum of 11 cabinets.

The office alarm unit (OAU) provides alarm control. The NTRX31AA acts as the interface between equipment lineups and the OAU. The OAU is in the first NTRX32AA cabinetized trunk module equipment (CTME).

The NTRX31AA provides a common product for different applications in hosts and remotes. The NTRX31AA also provides a configuration for small applications with the option for seamless growth. The NTRX31AA provides electromagnetic interference (EMI) compliance at the system level for all power distribution. The NTRX31AA also provides EMI compliance at the cabinet level for all input power cabling.

### Cabling

The dc power plant for the office provides power to the NTRX31AA. The dc power plant provides power at a nominal voltage of -48V through separate battery feeders, A and B. The power returns from each to the power plant through battery return conductors. The battery return conductors are the same size as the battery feeders.

The power distributes from the fuse or breaker panels in the NTRX31AA to the frame supervisory panels (FSP) in the different equipment frames in the lineup. The power distributes through secondary battery feeders. Power returns to the through return feeders of the same size.

The NTRX31AA obtains the required dc voltages other than -48V from dc-dc converters. The dc-dc converters are powered from -48V and are in each equipment frame.

The external cabling enters the NTRX31AA from the top or bottom of the cabinet for. Internal cabling for all loads exit and enter through the side of the cabinet. This condition does not apply to the loads in an NT9X01 or NT9X95AA type cabinet. The NT9X95AA type cabinet accepts horizontal cabling. Feeds for the NT9X01 cabinet exit through filter capacitors on the NTRX31AA EMI bulkhead. The feeds route externally to the NT9X01 cabinets. To change the NT9X01 cabinet to the NT9X95AA type removes the NT9X01 external power filters.

## Parts

The NTRX31AA contains the following parts:

- NTMX26CD—Frame supervisory panel
- Power distribution shelf or shelves (2 maximum), at shelf positions 30 and 46 in the NTRX31AA.

  Each shelf includes one of the following:

  — one breaker panel assembly and one breaker panel to junction box kit. The assembly and kit must be from the following list. The assembly and kit are combined according to the rules described in the part descriptions that follows this list:

  – -NTRX02AA—Breaker panel assembly, non-SuperNode lineup

  – -NTRX02AB—Breaker panel assembly, SuperNode

  – -NTRX02AD—Breaker panel assembly, SONET/DMS (S/DMS)

  – -NTRX02AE—Breaker panel 1 to junction box kit

  – -NTRX02AC—Breaker panel 2 to junction box kit

  — a specific bulkhead assembly, that contains one of the following assemblies. The assemblies are provisioned according to the rules described in the following part descriptions:

  – -NTZZ13MA—SuperNode bulkhead panel assembly, that contains the following parts:

  – -NTRX01AK—Connector plate assembly return

  – -NTRX01AM—Connector plate assembly feed

  – -NTRX73AC—EMI skin panel

  – -NTRX73AF—Mid lineup EMI panel

  — NTRX01AN—ENET plane 0 feed bulkhead assembly

  — NTRX01AP—ENET plane 1 feed bulkhead assembly

  — NTRX01AQ—ENET plane 0 return bulkhead assembly

  — NTRX01AR—ENET plane 1 return bulkhead assembly

- NTRX01AD—Power cable junction box
- NTRX31AD—500W inverter kit (optional)
- P0715616—Bulkhead filler panel
- P0715769—16 in. filler panel

## **NTRX31AA** (continued)

### Frame supervisory panel

The NTMX26CD frame supervisory panel (FSP) has the design features of the current PDC FSP designs in the NT0X40 series. Alarms from the NTRX31AA route through the FSP to the OAU.

The FSP includes a frame fail light at the top of the front of the cabinet. The FSP also includes an electrostatic discharge wrist strap. The wrist strap is in the front of the cabinet.

### Power distribution shelf

The power distribution shelf (PDS) or shelves provide wiring and circuit breaker protection to distribute power to DMS-100 equipment. The NTRX31AA distributes a maximum of 200A of 48V dc power. The NTRX31AA distributes the power on each of the separate A and B feed buses of the NTRX31AA.

A recommended 250A power board fuse provides overload protection. Distribution of the bulk dc power to equipment loads occurs through 30-A circuit breakers.

One or two PDSs can be provisioned. This condition does not apply to a lineup with a SuperNode-based NT9X0113 cabinet. When this condition occurs, one PDS is provisioned at shelf position 30. The provisioning of a PDS shelf depends on the types of DMS-100 equipment frames that the NTRX31AA provides power to. The part combinations for shelves 30 and 46 appear in the following table.

A dc breaker panel is available. The dc breaker panel contains 42 circuit breakers (21 on each of the A and B buses). The breaker panel provides capacitive filtering for each bus. This function requires one breaker on each bus. This condition allows 20 breakers for each bus for secondary distribution.

An optional NTRX31AD inverter can provide ac voltage to serve optional convenience outlets located in equipment lineup endguards. This optional inverter requires one 30A breaker.

### Supplementary power distribution shelf (optional)

A supplementary NTRX02 power distribution shelf can be provisioned. See the previous part description.

### Power cable junction box

The NTRX01AD power cable junction box provides connection for supplementary shelves and is standard equipment on the NTRX31AA.

### 500W inverter (optional)

The 500W inverter is an optional component that serves convenience outlets in equipment lineup endguards. The NTRX31AD inverter kit contains the A0367433 LaMarche inverter. The LaMarche inverter changes the -48V (nominal) dc, from the office battery, to 110V ac.

### Bulkhead filler panel

The NTX31AA uses two P0715616 bulkhead filler panels when the NTRX31AA is in a lineup without one of the following:

- a SuperNode
- link peripheral processor (LPP)
- an ENET mounted in a NT9X0113 cabinet

## **NTRX31AA** (continued)

### 16-in. filler panel

The NTRX31AA includes one P0715769 16 in. (0.41 m) filler panel. This filler panel is at shelf position 14. One or two additional panels must fill PDS shelf spaces that are not in use at shelf positions 30 and 46.

**Power distribution shelf provisioning options (Sheet 1 of 7)**

| Lineup | Shelf pos. | PEC | Product description |
|---|---|---|---|
| Non-SuperNode | 46 | NTRX02AA[1] | Breaker panel assembly[1] |
| | 30 | NTRX02AA[1] | Breaker panel assembly[1] |
| | 46 | NTRX02AE[2] | Breaker panel 1 to junction box kit[2] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 46 | NTMX2643[3] | -48V alarm battery supply (ABS) cable[3] |

***Note 1:*** One NTRX02AA breaker panel is in shelf position 30 or 46. One NTRX02AA is in each shelf to power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in use shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is provisioned in shelf position 30.

***Note 3:*** One NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable for each NTRX31AA are provided. The cables are provided when two breaker panels are required or a single breaker panel is provisioned in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided when only a single panel is provisioned in shelf position 30.

***Note 4:*** One NTRX02AB breaker panel assembly is in shelf position 30 only to power lineups with a SuperNode cabinet. Lineups can have a SuperNode ENET cabinet. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01AN ENET plane 0 feed bulkhead assembly and one NTRX01AQ ENET plane 0 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31AA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf positions 30 or 46 when shelf 30 or 46 does not have a breaker panel.

***Note 7:*** One NTRX01AP ENET plane 1 feed bulkhead assembly and one NTRX01AR ENET plane 1 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31AA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs, as listed.

***Note 9:*** One NTRX02AD breaker panel is in shelf position 30 or 46. The NTRX02AD can be in each shelf to power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup.

**Power distribution shelf provisioning options (Sheet 2 of 7)**

| Lineup | Shelf pos. | PEC | Product description |
|---|---|---|---|
| | 46 | NTMX2644[3] | ABS return cable[3] |
| | 30 | NTNX2692[3] | -48V ABS cable[3] |
| | 30 | NTNX2693[3] | ABS return cable[3] |
| NTX905AB ENET, Plane 0 in lineup | 30 | NTRX02AB[4] | Breaker panel assembly[4] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 30 | NTRX01AN[5] | ENET Plane 0 feed bulkhead assembly[5] |
| | 46 | NTRX01AQ[5] | ENET Plane 0 return bulkhead assembly[5] |

***Note 1:*** One NTRX02AA breaker panel is in shelf position 30 or 46. One NTRX02AA is in each shelf to power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in use shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is provisioned in shelf position 30.

***Note 3:*** One NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable for each NTRX31AA are provided. The cables are provided when two breaker panels are required or a single breaker panel is provisioned in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided when only a single panel is provisioned in shelf position 30.

***Note 4:*** One NTRX02AB breaker panel assembly is in shelf position 30 only to power lineups with a SuperNode cabinet. Lineups can have a SuperNode ENET cabinet. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01AN ENET plane 0 feed bulkhead assembly and one NTRX01AQ ENET plane 0 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31AA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf positions 30 or 46 when shelf 30 or 46 does not have a breaker panel.

***Note 7:*** One NTRX01AP ENET plane 1 feed bulkhead assembly and one NTRX01AR ENET plane 1 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31AA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs, as listed.

***Note 9:*** One NTRX02AD breaker panel is in shelf position 30 or 46. The NTRX02AD can be in each shelf to power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup.

## **NTRX31AA** (continued)

**Power distribution shelf provisioning options (Sheet 3 of 7)**

| Lineup | Shelf pos. | PEC | Product description |
|---|---|---|---|
| | 46 | P0715769[6] | 16-in. filler face plate[6] |
| NTX905AB ENET, Plane 1 in lineup | 30 | NTRX02AB[4] | Breaker panel assembly[4] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 30 | NTRX01AP[7] | ENET Plane 1 feed bulkhead assembly[7] |
| | 46 | NTRX01AR[7] | ENET Plane 1 return bulkhead assembly[7] |
| | 46 | P0715769[6] | 16-in. filler face plate[6] |
| SuperNode | 30 | NTRX02AB[4] | Breaker panel assembly[4] |

***Note 1:*** One NTRX02AA breaker panel is in shelf position 30 or 46. One NTRX02AA is in each shelf to power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in use shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is provisioned in shelf position 30.

***Note 3:*** One NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable for each NTRX31AA are provided. The cables are provided when two breaker panels are required or a single breaker panel is provisioned in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided when only a single panel is provisioned in shelf position 30.

***Note 4:*** One NTRX02AB breaker panel assembly is in shelf position 30 only to power lineups with a SuperNode cabinet. Lineups can have a SuperNode ENET cabinet. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01AN ENET plane 0 feed bulkhead assembly and one NTRX01AQ ENET plane 0 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31AA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf positions 30 or 46 when shelf 30 or 46 does not have a breaker panel.

***Note 7:*** One NTRX01AP ENET plane 1 feed bulkhead assembly and one NTRX01AR ENET plane 1 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31AA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs, as listed.

***Note 9:*** One NTRX02AD breaker panel is in shelf position 30 or 46. The NTRX02AD can be in each shelf to power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup.

**Power distribution shelf provisioning options (Sheet 4 of 7)**

| Lineup | Shelf pos. | PEC | Product description |
|---|---|---|---|
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 30 | NTRX2692[3] | -48V ABS cable[3] |
| | 30 | NTNX2693[3] | ABS return cable[3] |
| | 46 | P0715769[6] | 16-in. filler face plate[6] |

***Note 1:*** One NTRX02AA breaker panel is in shelf position 30 or 46. One NTRX02AA is in each shelf to power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in use shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is provisioned in shelf position 30.

***Note 3:*** One NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable for each NTRX31AA are provided. The cables are provided when two breaker panels are required or a single breaker panel is provisioned in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided when only a single panel is provisioned in shelf position 30.

***Note 4:*** One NTRX02AB breaker panel assembly is in shelf position 30 only to power lineups with a SuperNode cabinet. Lineups can have a SuperNode ENET cabinet. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01AN ENET plane 0 feed bulkhead assembly and one NTRX01AQ ENET plane 0 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31AA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf positions 30 or 46 when shelf 30 or 46 does not have a breaker panel.

***Note 7:*** One NTRX01AP ENET plane 1 feed bulkhead assembly and one NTRX01AR ENET plane 1 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31AA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs, as listed.

***Note 9:*** One NTRX02AD breaker panel is in shelf position 30 or 46. The NTRX02AD can be in each shelf to power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup.

## **NTRX31AA** (continued)

**Power distribution shelf provisioning options (Sheet 5 of 7)**

| Lineup | Shelf pos. | PEC | Product description |
|---|---|---|---|
| SuperNode NT9X0113 cabinet in lineup | 30 | NTZZ13MA[8] | SuperNode bulkhead panel assembly, that contain components:[8]<br>• NTRX01AK—Connect or plate assembly return<br>• NTRX01AM—Connect or plate assembly feed<br>• NTRX73AC—EMI skin panel<br>• NTRX73AF—Mid lineup EMI panel |

***Note 1:*** One NTRX02AA breaker panel is in shelf position 30 or 46. One NTRX02AA is in each shelf to power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in use shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is provisioned in shelf position 30.

***Note 3:*** One NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable for each NTRX31AA are provided. The cables are provided when two breaker panels are required or a single breaker panel is provisioned in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided when only a single panel is provisioned in shelf position 30.

***Note 4:*** One NTRX02AB breaker panel assembly is in shelf position 30 only to power lineups with a SuperNode cabinet. Lineups can have a SuperNode ENET cabinet. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01AN ENET plane 0 feed bulkhead assembly and one NTRX01AQ ENET plane 0 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31AA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf positions 30 or 46 when shelf 30 or 46 does not have a breaker panel.

***Note 7:*** One NTRX01AP ENET plane 1 feed bulkhead assembly and one NTRX01AR ENET plane 1 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31AA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs, as listed.

***Note 9:*** One NTRX02AD breaker panel is in shelf position 30 or 46. The NTRX02AD can be in each shelf to power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup.

**Power distribution shelf provisioning options (Sheet 6 of 7)**

| Lineup | Shelf pos. | PEC | Product description |
|---|---|---|---|
| | 46 | P0715769[6] | 16-in. filler face plate[6] |
| S/DMS (without SuperNode) | 46 | NTRX02AD[9] | Breaker panel assembly (S/DMS)[9] |
| | 30 | NTRX02AD[9] | Breaker panel assembly (S/DMS)[9] |
| | 46 | NTRX02AE[2] | Breaker panel 1 to junction box kit[2] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 46 | NTMX2643[3] | -48V ABS cable[3] |
| | 46 | NTMX2644[3] | ABS return cable[3] |

***Note 1:*** One NTRX02AA breaker panel is in shelf position 30 or 46. One NTRX02AA is in each shelf to power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in use shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is provisioned in shelf position 30.

***Note 3:*** One NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable for each NTRX31AA are provided. The cables are provided when two breaker panels are required or a single breaker panel is provisioned in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided when only a single panel is provisioned in shelf position 30.

***Note 4:*** One NTRX02AB breaker panel assembly is in shelf position 30 only to power lineups with a SuperNode cabinet. Lineups can have a SuperNode ENET cabinet. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01AN ENET plane 0 feed bulkhead assembly and one NTRX01AQ ENET plane 0 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31AA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf positions 30 or 46 when shelf 30 or 46 does not have a breaker panel.

***Note 7:*** One NTRX01AP ENET plane 1 feed bulkhead assembly and one NTRX01AR ENET plane 1 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31AA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs, as listed.

***Note 9:*** One NTRX02AD breaker panel is in shelf position 30 or 46. The NTRX02AD can be in each shelf to power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup.

## **NTRX31AA** (continued)

**Power distribution shelf provisioning options (Sheet 7 of 7)**

| Lineup | Shelf pos. | PEC | Product description |
|---|---|---|---|
| | 30 | NTNX2692[3] | -48V ABS cable[3] |
| | 30 | NTNX2693[3] | ABS return cable[3] |

***Note 1:*** One NTRX02AA breaker panel is in shelf position 30 or 46. One NTRX02AA is in each shelf to power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in use shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is provisioned in shelf position 30.

***Note 3:*** One NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable for each NTRX31AA are provided. The cables are provided when two breaker panels are required or a single breaker panel is provisioned in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided when only a single panel is provisioned in shelf position 30.

***Note 4:*** One NTRX02AB breaker panel assembly is in shelf position 30 only to power lineups with a SuperNode cabinet. Lineups can have a SuperNode ENET cabinet. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01AN ENET plane 0 feed bulkhead assembly and one NTRX01AQ ENET plane 0 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31AA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf positions 30 or 46 when shelf 30 or 46 does not have a breaker panel.

***Note 7:*** One NTRX01AP ENET plane 1 feed bulkhead assembly and one NTRX01AR ENET plane 1 RTN bulkhead assembly are provided when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31AA.

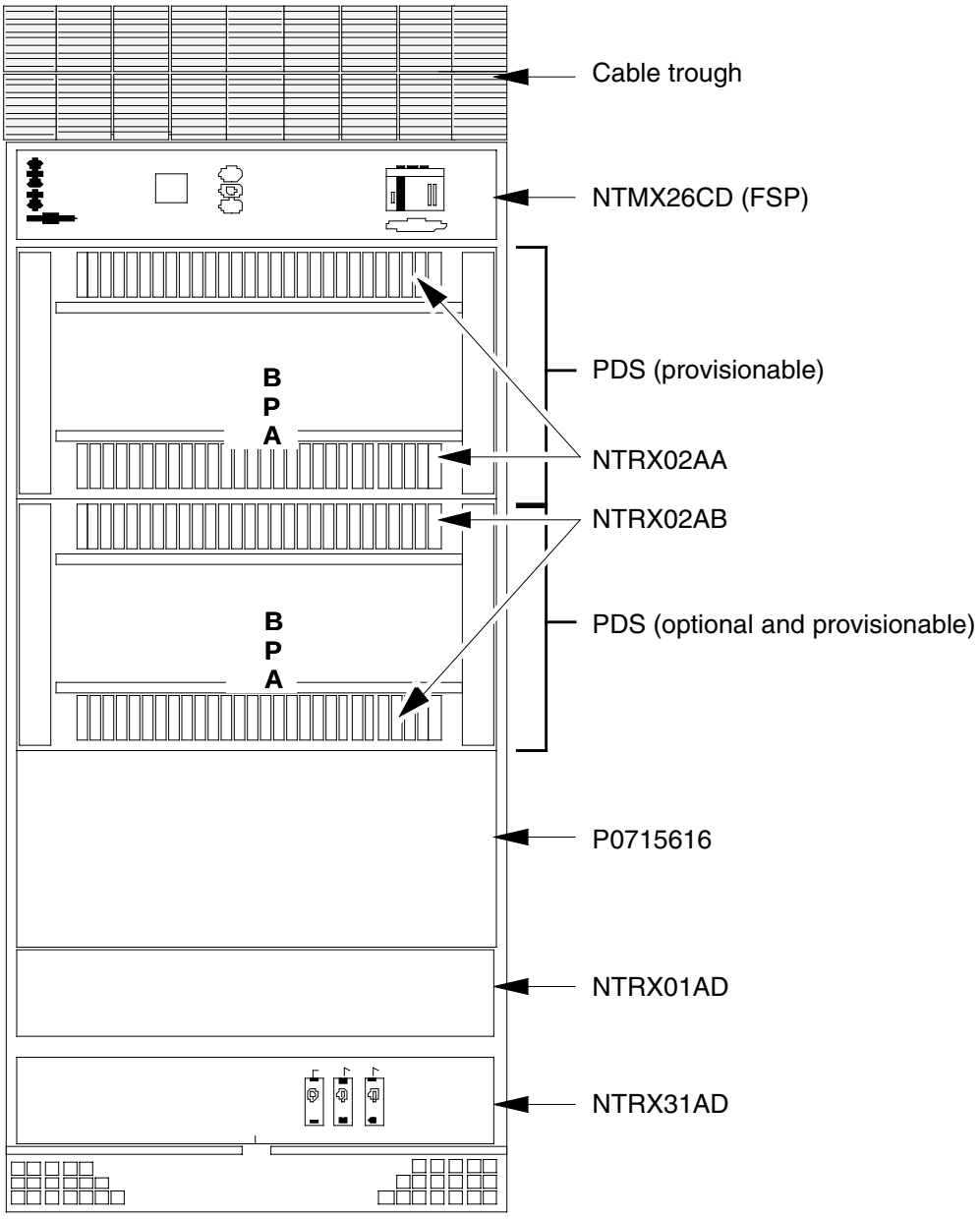
***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs, as listed.

***Note 9:*** One NTRX02AD breaker panel is in shelf position 30 or 46. The NTRX02AD can be in each shelf to power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup.

## Design

The design of the NTRX31AA parts appears in the following figure.

**NTRX31AA parts**




**Note**: NTRX31AAFor clarity, front panels do not appear in figure. This diagram is not to scale.

# NTRX31BA

## Product description

The NTRX31BA cabinetized power distribution center (CPDC) is a single cabinet that distributes power to the cabinets in the correct order. The NTRX31BA provides dc power distribution and protection and optional inverted ac power for endguard outlets. The NTRX31BA is the first cabinet in a lineup of a maximum of 11 cabinets.

The office alarm unit (OAU) provides alarm control. The NTRX31BA is the interface between equipment lineups and the OAU. The OAU is in the first NTRX31BA cabinetized trunk module equipment (CTME).

The NTRX31BA provides a common product for different applications in hosts and remotes. The NTRX31BA also provides a configuration for small applications. This configuration has the option of seamless growth. The NTRX31BA provides electromagnetic interference (EMI) compliance at the system level for all power distribution. The NTRX31BA also provides EMI compliance at the cabinet level for all input power cabling.

### Cabling

The dc power plant for the office supplies power to the NTRX31BA. The dc power plant provides power at a nominal voltage of -48/60V through separate battery feeders, A and B. The power returns from each NTRX31BA to the power plant through battery return conductors. The battery return conductors are the same size as the battery feeders.

The power distributes from the fuse and breaker panels in the NTRX31BA. The power feeds to the frame supervisory panels (FSP) in the different equipment frames in the lineup through secondary battery feeders. Power returns to the NTRX31BA through return feeders of the same size.

The NTRX31BA receives required dc voltages other than -48/60V from dc-dc converters. The dc-dc converters are powered from -48/60V and are in each equipment frame.

External cabling enters from the top or the bottom of the cabinet for the NTRX31BA. Internal cabling for all loads exit and enter through the side of the cabinet. This condition does not apply to the loads in an NT9X01 or NT9X95AA type cabinet. The NT9X95AA type cabinet accepts horizontal cabling. The feeds for the NT9X01 cabinet exit through filter capacitors on the NTRX31BA EMI bulkhead. The feeds route to these cabinets on the outside. Conversion to the NT9X95AA type eliminates the NT9X01 external power filters.

## Parts

The NTRX31BA has a number of the following parts:

- NTMX26CE—frame supervisory panel (FSP)
- a maximum of two power distribution shelves, at shelf positions 30 and 46 in the NTRX31BA

  Each shelf includes one of the following:

  — one breaker panel assembly and one breaker panel to junction*box kit. The assembly and kit must be from the following list. The parts combine according to the rules in the descriptions that follow the list.*

    – NTRX02BB—breaker panel assembly, SuperNode

    – NTRX02BD—breaker panel assembly, synchronous optical network (SONET)/DMS (S/DMS)

    – NTRX02AE—breaker panel 1 to junction box kit

    – NTRX02AC—breaker panel 2 to junction box kit

  — a specified bulkhead assembly that contains one of the following assemblies, provisioned according to the rules described in the descriptions that follow:

    – NTZZ13MA—SuperNode bulkhead panel assembly, that contains the following parts:

      – NTRX01BK—connector plate assembly return

      – NTRX01BM—connector plate assembly feed

      – NTRX73AC—EMI skin panel

      – NTRX73AF—mid-lineup EMI panel

    – NTRX01BN—enhanced network (ENET) plane 0 feed bulkhead assembly

    – NTRX01BP—ENET plane 1 feed bulkhead assembly

    – NTRX01BQ—ENET plane 0 return bulkhead assembly

    – NTRX01BR—ENET plane 1 return bulkhead assembly

- NTRX01AD—power cable junction box
- NTRX31AD—500W inverter kit (optional)
- P0715616—bulkhead filler panel
- P0715769—16 in. (410 mm) filler faceplate

## **NTRX31BA** (continued)

### Frame supervisory panel

The NTMX26CE frame supervisory panel (FSP) has the design features of the current PDC FSP designs in the NT0X40 series. Alarms from the NTRX31BA route through the FSP to the OAU.

The FSP includes a frame fail light at the top of the front of the cabinet. The FSP also includes an electrostatic discharge wrist strap. The wrist strap is in the front of the cabinet.

### Power distribution shelf

The power distribution shelf (PDS) or shelves have wiring and circuit breaker protection to distribute power to DMS-100 equipment. The NTRX31BA distributes a maximum of 300A of 48/60V dc power. The NT6X31BA distributes the power on each of the separate A and B feed buses of the NTRX31BA.

A 350-A power board fuse provides overload protection. Distribution of the bulk dc power to equipment loads occurs through 30A circuit breakers.

The NTRX31BA can have one or two PDSs. For a lineup with a SuperNode NT9X0113 cabinets, one PDS is at shelf position 30. The types of DMS-100 equipment frames to which the NTRX31BA provides power determines the PDSs. The groups of parts for shelves 30 and 46 appears in the table on page 4.

A dc breaker panel is available. The dc breaker panel contains 42 circuit breakers (21 on each of the A and B buses). The breaker panel provides capacitive filtering of each bus. One breaker on each bus provides this function. Each bus has 20 breakers for secondary distribution.

An available NTRX31AD inverter can provide ac voltage to serve available convenience outlets in equipment lineup end guards. This inverter requires one 30-A breaker.

### Auxiliary power distribution shelf (optional)

The NTRX31BA can have an auxiliary NTRX02 power distribution shelf. Refer to the previous description.

### Power cable junction box

The NTRX01AD power cable junction box provides connection for auxiliary shelves. The NTRX01AD power cable junction box is standard equipment on the NTRX31BA.

### 500-W inverter (optional)

The 500-W inverter is available to serve convenience outlets in equipment lineup end guards. The NTRX31AD inverter kit contains the A0367433 LaMarche inverter. The LaMarche inverter changes the nominal -48/60V dc voltage from the office battery to 110V ac voltage.

### Bulkhead filler panel

The NTRX31BA uses two P0715616 bulkhead filler panels when in a lineup without one of the following:

- a SuperNode
- link peripheral processor (LPP)
- an ENET mounted in an NT9X0113 cabinet

## NTRX31BA (continued)

### 16-in. filler faceplate

The NTRX31BA includes an P0715769 16 in. (410 mm) filler faceplate. This faceplate is at shelf position 14. One or two other panels must fill PDS shelf spaces that are not in use at shelf positions 30 and 46.

**Power distribution shelf provisioning (Sheet 1 of 7)**

| Lineup | Shelf position | Product engineering code (PEC) | Product description |
|---|---|---|---|
| Non-SuperNode | 46 | NTRX02BA[1] | Breaker panel assembly[1] |
| | 30 | NTRX02BA[1] | Breaker panel assembly[1] |
| | 46 | NTRX02AE[2] | Breaker panel 1 to junction box kit[2] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |

***Note 1:*** One NTRX02BA breaker panel is in shelf position 30 or 46. One NTRX02BA is in each shelf when you power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is in shelf position 30.

***Note 3:*** Each NTRX31BA has one NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable. This condition occurs when two breaker panels are required or a single breaker panel is in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided. This condition occurs when only a single panel is in shelf position 30.

***Note 4:*** One NTRX02BB breaker panel assembly is in shelf position 30 when you power lineups with a SuperNode cabinet. This condition includes SuperNode ENET. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01BN ENET plane 0 feed bulkhead assembly and one NTRX01BQ ENET, plane 0, RTN bulkhead assembly is provided. This condition occurs when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31BA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf position 30 or 46. This condition occurs when shelf positions 30 or 46 do not have a breaker panel.

***Note 7:*** The NTRX31BA has one NTRX01BP ENET plane 1 feed bulkhead assembly and one NTRX01BR ENET, plane 1, RTN bulkhead assembly. This condition occurs when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31BA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs.

***Note 9:*** When you power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup, one of the following conditions applies. One NTRX02BD breaker panel is in shelf position 30 or 46, or one NTRX02BD is in each shelf.

**Power distribution shelf provisioning (Sheet 2 of 7)**

| Lineup | Shelf position | Product engineering code (PEC) | Product description |
|---|---|---|---|
| | 46 | NTMX2643[3] | -48V alarm battery supply (ABS) cable[3] |
| | 46 | NTMX2644[3] | ABS return cable[3] |
| | 30 | NTNX2692[3] | -48V ABS cable[3] |
| | 30 | NTNX2693[3] | ABS return cable[3] |
| NTX905AB ENET, plane 0 in lineup | 30 | NTRX02BB[4] | Breaker panel assembly[4] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 30 | NTRX01BN[5] | ENET plane 0 feed bulkhead assembly[5] |

***Note 1:*** One NTRX02BA breaker panel is in shelf position 30 or 46. One NTRX02BA is in each shelf when you power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is in shelf position 30.

***Note 3:*** Each NTRX31BA has one NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable. This condition occurs when two breaker panels are required or a single breaker panel is in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided. This condition occurs when only a single panel is in shelf position 30.

***Note 4:*** One NTRX02BB breaker panel assembly is in shelf position 30 when you power lineups with a SuperNode cabinet. This condition includes SuperNode ENET. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01BN ENET plane 0 feed bulkhead assembly and one NTRX01BQ ENET, plane 0, RTN bulkhead assembly is provided. This condition occurs when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31BA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf position 30 or 46. This condition occurs when shelf positions 30 or 46 do not have a breaker panel.

***Note 7:*** The NTRX31BA has one NTRX01BP ENET plane 1 feed bulkhead assembly and one NTRX01BR ENET, plane 1, RTN bulkhead assembly. This condition occurs when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31BA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs.

***Note 9:*** When you power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup, one of the following conditions applies. One NTRX02BD breaker panel is in shelf position 30 or 46, or one NTRX02BD is in each shelf.

## **NTRX31BA** (continued)

**Power distribution shelf provisioning (Sheet 3 of 7)**

| Lineup | Shelf position | Product engineering code (PEC) | Product description |
|---|---|---|---|
| | 46 | NTRX01BQ[5] | ENET plane 0 return bulkhead assembly[5] |
| | 46 | P0715769[6] | 16-in. (410-mm) filler faceplate[6] |
| NTX905AB ENET, plane 1 in lineup | 30 | NTRX02BB[4] | Breaker panel assembly[4] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 30 | NTRX01BP[7] | ENET plane 1 feed bulkhead assembly[7] |
| | 46 | NTRX01BR[7] | ENET plane 1 return bulkhead assembly[7] |
| | 46 | P0715769[6] | 16-in. (410-mm) filler faceplate[6] |

***Note 1:*** One NTRX02BA breaker panel is in shelf position 30 or 46. One NTRX02BA is in each shelf when you power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is in shelf position 30.

***Note 3:*** Each NTRX31BA has one NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable. This condition occurs when two breaker panels are required or a single breaker panel is in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided. This condition occurs when only a single panel is in shelf position 30.

***Note 4:*** One NTRX02BB breaker panel assembly is in shelf position 30 when you power lineups with a SuperNode cabinet. This condition includes SuperNode ENET. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01BN ENET plane 0 feed bulkhead assembly and one NTRX01BQ ENET, plane 0, RTN bulkhead assembly is provided. This condition occurs when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31BA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf position 30 or 46. This condition occurs when shelf positions 30 or 46 do not have a breaker panel.

***Note 7:*** The NTRX31BA has one NTRX01BP ENET plane 1 feed bulkhead assembly and one NTRX01BR ENET, plane 1, RTN bulkhead assembly. This condition occurs when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31BA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs.

***Note 9:*** When you power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup, one of the following conditions applies. One NTRX02BD breaker panel is in shelf position 30 or 46, or one NTRX02BD is in each shelf.

**Power distribution shelf provisioning (Sheet 4 of 7)**

| Lineup | Shelf position | Product engineering code (PEC) | Product description |
|---|---|---|---|
| SuperNode | 30 | NTRX02BB[4] | Breaker panel assembly[4] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 30 | NTRX2692[3] | -48V ABS cable[3] |
| | 30 | NTNX2693[3] | ABS return cable[3] |
| | 46 | P0715769[6] | 16-in. (410-mm) filler faceplate[6] |

***Note 1:*** One NTRX02BA breaker panel is in shelf position 30 or 46. One NTRX02BA is in each shelf when you power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is in shelf position 30.

***Note 3:*** Each NTRX31BA has one NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable. This condition occurs when two breaker panels are required or a single breaker panel is in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided. This condition occurs when only a single panel is in shelf position 30.

***Note 4:*** One NTRX02BB breaker panel assembly is in shelf position 30 when you power lineups with a SuperNode cabinet. This condition includes SuperNode ENET. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01BN ENET plane 0 feed bulkhead assembly and one NTRX01BQ ENET, plane 0, RTN bulkhead assembly is provided. This condition occurs when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31BA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf position 30 or 46. This condition occurs when shelf positions 30 or 46 do not have a breaker panel.

***Note 7:*** The NTRX31BA has one NTRX01BP ENET plane 1 feed bulkhead assembly and one NTRX01BR ENET, plane 1, RTN bulkhead assembly. This condition occurs when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31BA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs.

***Note 9:*** When you power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup, one of the following conditions applies. One NTRX02BD breaker panel is in shelf position 30 or 46, or one NTRX02BD is in each shelf.

## NTRX31BA (continued)

**Power distribution shelf provisioning (Sheet 5 of 7)**

| Lineup | Shelf position | Product engineering code (PEC) | Product description |
|---|---|---|---|
| SuperNode NT9X0113 cabinet in lineup | 30 | NTZZ13MA[8] | SuperNode bulkhead panel assembly, that contains the following components:[8]<br>• NTRX01AK—connector plate assembly return<br>• NTRX01AM—connector plate assembly feed<br>• NTRX73AC—EMI skin panel<br>• NTRX73AF—mid-lineup EMI panel |
| | 46 | P0715769[6] | 16-in. (410-mm) filler faceplate[6] |

***Note 1:*** One NTRX02BA breaker panel is in shelf position 30 or 46. One NTRX02BA is in each shelf when you power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is in shelf position 30.

***Note 3:*** Each NTRX31BA has one NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable. This condition occurs when two breaker panels are required or a single breaker panel is in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided. This condition occurs when only a single panel is in shelf position 30.

***Note 4:*** One NTRX02BB breaker panel assembly is in shelf position 30 when you power lineups with a SuperNode cabinet. This condition includes SuperNode ENET. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01BN ENET plane 0 feed bulkhead assembly and one NTRX01BQ ENET, plane 0, RTN bulkhead assembly is provided. This condition occurs when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31BA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf position 30 or 46. This condition occurs when shelf positions 30 or 46 do not have a breaker panel.

***Note 7:*** The NTRX31BA has one NTRX01BP ENET plane 1 feed bulkhead assembly and one NTRX01BR ENET, plane 1, RTN bulkhead assembly. This condition occurs when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31BA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs.

***Note 9:*** When you power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup, one of the following conditions applies. One NTRX02BD breaker panel is in shelf position 30 or 46, or one NTRX02BD is in each shelf.

**Power distribution shelf provisioning (Sheet 6 of 7)**

| Lineup | Shelf position | Product engineering code (PEC) | Product description |
|---|---|---|---|
| S/DMS (without SuperNode) | 46 | NTRX02BD[9] | Breaker panel assembly (S/DMS)[9] |
| | 30 | NTRX02BD[9] | Breaker panel assembly (S/DMS)[9] |
| | 46 | NTRX02AE[2] | Breaker panel 1 to junction box kit[2] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 46 | NTMX2643[3] | -48V ABS cable[3] |
| | 46 | NTMX2644[3] | ABS return cable[3] |

***Note 1:*** One NTRX02BA breaker panel is in shelf position 30 or 46. One NTRX02BA is in each shelf when you power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is in shelf position 30.

***Note 3:*** Each NTRX31BA has one NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable. This condition occurs when two breaker panels are required or a single breaker panel is in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided. This condition occurs when only a single panel is in shelf position 30.

***Note 4:*** One NTRX02BB breaker panel assembly is in shelf position 30 when you power lineups with a SuperNode cabinet. This condition includes SuperNode ENET. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01BN ENET plane 0 feed bulkhead assembly and one NTRX01BQ ENET, plane 0, RTN bulkhead assembly is provided. This condition occurs when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31BA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf position 30 or 46. This condition occurs when shelf positions 30 or 46 do not have a breaker panel.

***Note 7:*** The NTRX31BA has one NTRX01BP ENET plane 1 feed bulkhead assembly and one NTRX01BR ENET, plane 1, RTN bulkhead assembly. This condition occurs when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31BA.

***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs.

***Note 9:*** When you power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup, one of the following conditions applies. One NTRX02BD breaker panel is in shelf position 30 or 46, or one NTRX02BD is in each shelf.

## **NTRX31BA** (continued)

**Power distribution shelf provisioning (Sheet 7 of 7)**

| Lineup | Shelf position | Product engineering code (PEC) | Product description |
|---|---|---|---|
| | 30 | NTNX2692[3] | -48V ABS cable[3] |
| | 30 | NTNX2693[3] | ABS return cable[3] |

***Note 1:*** One NTRX02BA breaker panel is in shelf position 30 or 46. One NTRX02BA is in each shelf when you power non-SuperNode-based cabinets in a lineup.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit when a breaker panel assembly is in shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit when a breaker panel assembly is in shelf position 30.

***Note 3:*** Each NTRX31BA has one NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable. This condition occurs when two breaker panels are required or a single breaker panel is in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided. This condition occurs when only a single panel is in shelf position 30.

***Note 4:*** One NTRX02BB breaker panel assembly is in shelf position 30 when you power lineups with a SuperNode cabinet. This condition includes SuperNode ENET. The lineup can have only one SuperNode cabinet.

***Note 5:*** One NTRX01BN ENET plane 0 feed bulkhead assembly and one NTRX01BQ ENET, plane 0, RTN bulkhead assembly is provided. This condition occurs when an NT9X05AB ENET cabinet, plane 0, is in the same lineup as the NTRX31BA.

***Note 6:*** One P0715769 16-in. (410-mm) filler faceplate is in shelf position 30 or 46. This condition occurs when shelf positions 30 or 46 do not have a breaker panel.

***Note 7:*** The NTRX31BA has one NTRX01BP ENET plane 1 feed bulkhead assembly and one NTRX01BR ENET, plane 1, RTN bulkhead assembly. This condition occurs when an NT9X05AB ENET cabinet, plane 1, is in the same lineup as the NTRX31BA.

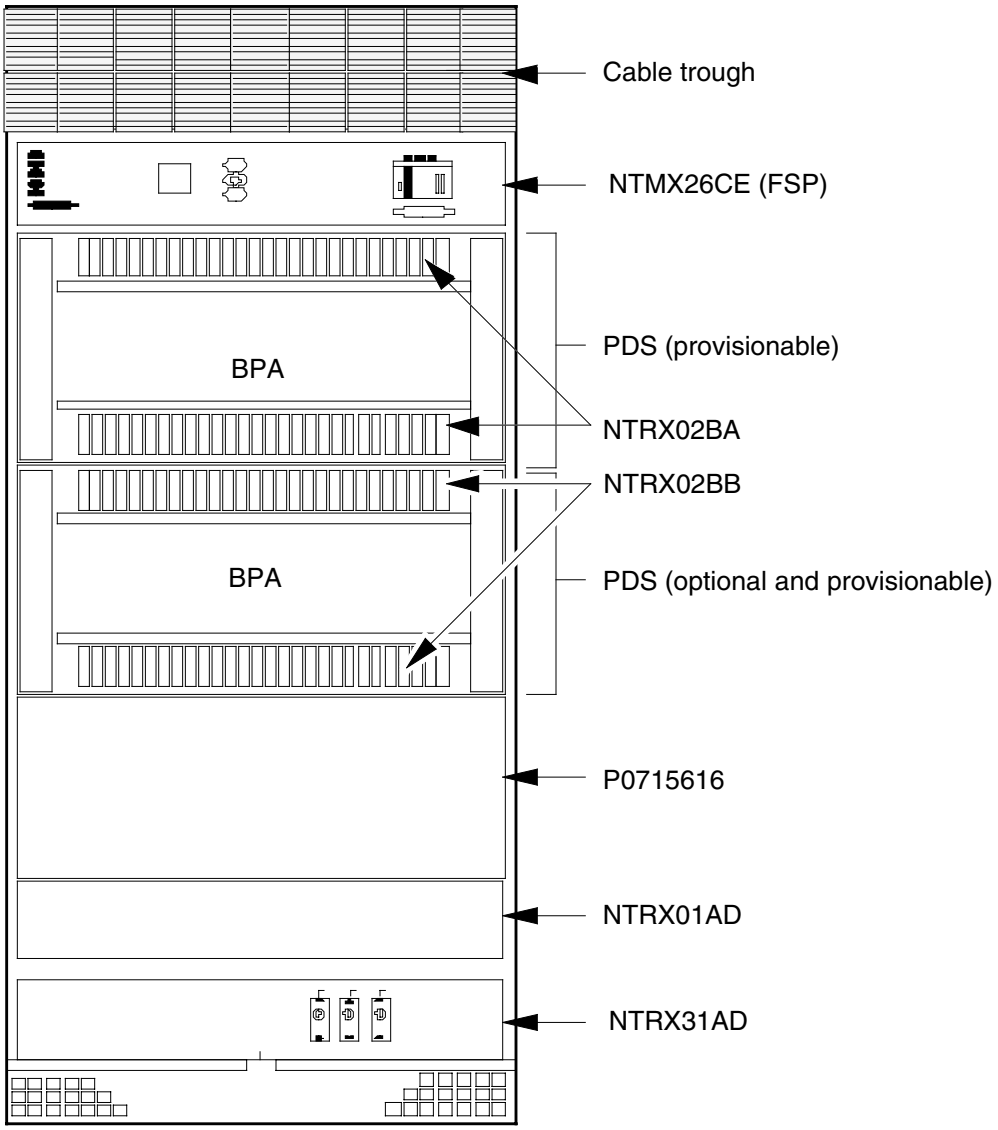
***Note 8:*** The NTZZ13MA is a building block code and refers to the composite PECs.

***Note 9:*** When you power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in a lineup, one of the following conditions applies. One NTRX02BD breaker panel is in shelf position 30 or 46, or one NTRX02BD is in each shelf.

## Design

The design of the NTRX31BA parts appears in the following diagram.

**The NTRX31BA parts**




**Note:** The front panels show the NTRX31BA parts. This diagram is not to scale.

# NTRX31CA

## Product description

The NTRX31CA cabinetized power distribution center (CPDC) is a single cabinet used to distribute power to the cabinets in the corresponding alignment. The provides dc power distribution and protection and optional inverted ac power for endguard outlets. The is the first cabinet in an alignment.

The NTRX31CA provides a common product for applications in both hosts and remotes. The NTRX31CA provides a compressed configuration for small applications with the option for seamless growth. The provides electromagnetic interference (EMI) compliance at the system level. The compliance is for power distribution and at the cabinet level for input power cabling.

### Cabling

The dc power plant for the office supplies power to the NTRX31CA at a nominal voltage of -48/60V. The power plant supplies power through battery feeders A and B. Battery return conductors return the power from each NTRX31CA to the power plant. The conductors are the same size as the battery feeders.

The fuse and breaker panels distribute the power in the NTRX31CA to the modular supervisory panels (MSP). The MSP panels are in the various equipment frames in the alignment through secondary battery feeders. The power returns to the through return feeders of the same size.

Required dc voltages other than -48/60V are obtained from dc–dc converters. The converters are powered from -48/60V and are in each equipment frame.

The NTRX31CA accepts external cabling that has top or bottom entry. Internal cabling for all loads exit and enter through the side of the cabinet. The loads in an NT9X01 or NT9X95AA style cabinet, exit and enter through the side of the cabinet. The NT9X95AA style cabinet accepts horizontal cabling. Feeds for the NT9X01 cabinet exit through feedthrough filter capacitors in the EMI bulkhead. The feeds route from the outside to these cabinets. Conversion to the NT9X95AA style eliminates the NT9X01 external power filters.

## Parts

The NTRX31CA contains a group of the following parts:

- NTRX40AA—modular supervisory panel
- power distribution shelf or shelves (2 maximum), at shelf positions 30 and 46 in the

Each shelf includes:

- one breaker panel assembly and one breaker panel to junction box kit. These parts are limited to the parts in the list below. These parts combine according to the rules described in the parts descriptions that follow the list:
  - NTRX02BA—breaker panel assembly, non–SuperNode alignment
  - NTRX02BB—breaker panel assembly, SuperNode
  - NTRX02BD—breaker panel assembly, SONET/DMS (S/DMS)
  - NTRX02AE—breaker panel 1 to junction box kit
  - NTRX02AC—breaker panel 2 to junction box kit
- or a specific bulkhead assembly, composed of one of the following assemblies provisioned according to the rules. The following part descriptions describe these rules:
  - NTZZ13MA—SuperNode bulkhead panel assembly, consisting of these components:
  - NTRX01BK—connector plate assembly return
  - NTRX01BM—connector plate assembly feed
  - NTRX73AC—EMI skin panel
  - NTRX73AF—mid–alignment EMI panel
- NTRX01BN—ENET plane 0 feed bulkhead assembly
- NTRX01BP—ENET plane 1 feed bulkhead assembly
- NTRX01BQ—ENET plane 0 return bulkhead assembly
- NTRX01BR—ENET plane 1 return bulkhead assembly
- NTRX01AD—power cable junction box
- NTRX31AD—500–W inverter kit (optional)
- P0715616—bulkhead filler panel
- P0715769—16 –in. (410 mm) filler faceplate

### Modular supervisory panel

The NTRX40AA modular supervisory panel (MSP) reflects the design features of the PDC FSP designs present in the NT0X40 series. Alarms from the routes through the MSP to the OAU.

## **NTRX31CA** (continued)

The MSP includes a frame fail light mounted at the top of the front of the cabinet. The MSP includes an electrostatic discharge wrist strap in the front of the cabinet.

### Power distribution shelf

The power distribution shelf (PDS) or shelves provide wiring and circuit breaker protection to distribute power to DMS–100 equipment. The distributes a maximum of 300A of 48/60–V dc power. The NTRX31CA distributes power on each of the NTRX31CA separate A and B feed buses.

A recommended 350–A power board fuse provides overload protection. Distribution of the bulk dc power to equipment loads occurs through 30–A circuit breakers.

One or two PDSs can be provisioned, except for an alignment with a SuperNode–based NT9X0113 cabinet. One PDS is provisioned at shelf position 30. The provisioning of PDS shelves varies according to the types of DMS–100 equipment frames the NTRX31CA provides power to. The table on page four lists the possible part groups for shelves 30 and 46.

A dc breaker panel is available and contains a total of 42 circuit breakers. There are 21 circuit breakers available on each of the A and B buses. The breaker panel provides capacitive filtering of each bus. One breaker on each bus is dedicated to this function. Each bus has 20 breakers for secondary distribution.

An available NTRX31AD inverter can provide ac voltage to serve available support outlets in equipment alignment end guards. This inverter requires one 30–A breaker.

### Supplementary power distribution shelf (optional)

You can provision a supplementary NTRX02 power distribution shelf. Refer to the previous description.

### Power cable junction box

The NTRX01AD power cable junction box provides connection for supplementary shelves and is standard equipment on the .

### 500–W inverter (optional)

The 500–W inverter is an available part that serves support outlets in equipment alignment end guards. The NTRX31AD inverter kit contains the A0367433 LaMarche inverter. The LaMarche inverter converts voltage. The inverter converts the dc voltage of -48/60V (nominal) from the office battery to an ac voltage of 110V.

### Bulkhead filler panel

The NTRX31CA uses two P0715616 bulkhead filler panels. Use the panels when the following conditions apply:

- is in an alignment without a SuperNode
- NTRX31CA is in an alignment without a link peripheral processor (LPP)
- NTRX31CA is in an alignment without ENET mounted in an NT9X0113 cabinet.

## NTRX31CA (continued)

### 16–in. filler faceplate

One P0715769 16 in. (410 mm) filler faceplate comes standard with the NTRX31CA, and mounts at shelf position 14. Use one or two other panels to fill PDS shelf spaces not used at shelf positions 30 and 46.

**Power distribution shelf provisioning options (Sheet 1 of 4)**

| Lineup | Shelf pos. | PRC | Product description |
|---|---|---|---|
| Non–SuperNode | 46 | NTRX02BA[1] | Breaker panel assembly[1] |
| | 30 | NTRX02BA[1] | Breaker panel assembly[1] |
| | 46 | NTRX02AE[2] | Breaker panel 1 to junction box kit[2] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 46 | NTMX2643[3] | –48V alarm battery supply (ABS) cable[3] |

***Note 1:*** One NTRX02BA breaker panel is in shelf position 30 or 46. Each shelf has one NTRX02BA to power non-SuperNode-based cabinets in an alignment.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit for the use of a breaker panel assembly in shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit for a provisioned breaker panel assembly in shelf position 30.

***Note 3:*** Each NTRX31CA provides for one NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable. The cables are provided when two breaker panels are required. The cables are also provided for a provisioned single breaker panel in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided for a provisioned single panel. The panel is in shelf position 30.

***Note 4:*** One NTRX02BB breaker panel assembly is in shelf position 30. Only one breaker panel is present when a SuperNode (including SuperNode ENET) cabinet powers alignments. Only one SuperNode cabinet is in the alignment.

***Note 5:*** One NTRX01BN ENET plan 0 feed bulkhead assembly and one NTRX01BQ ENET plan 0 RTN bulkhead assembly are provided. The assemblies are provided when an NT9X05AB ENET cabinet, plane 0, is in the same alignment as the NTRX31CA.

***Note 6:*** Shelf powitions 30 or 46 provides one P0715769 16-in. (410-mm) filler faceplate when either is unequipped with a breaker panel.

***Note 7:*** One NTRX01BP ENET plane 1 feed bulkhead assembly and one NTRX01BR ENET plane 1 RTN bulkhead assembly are provided. The assemblies are provided when an NT9X05AB ENET cabinet, plane 1, is in the same alignment as the NTRX31CA.

***Note 8:*** NTZZ13MA is a building block code and refers to the composite PECs, as listed.

***Note 9:*** One NTRX02BD breaker panel is in shelf position 30 or 46. Each shelf has one NTRX02BD to power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in an alignment.

**Power distribution shelf provisioning options (Sheet 2 of 4)**

| | | | |
|---|---|---|---|
| | 46 | NTMX2644[3] | ABS return cable[3] |
| | 30 | NTNX2692[3] | –48V ABS cable[3] |
| | 30 | NTNX2693[3] | ABS return cable[3] |
| NTX905AB ENET, plane 0 in alignment | 30 | NTRX02BB[4] | Breaker panel assembly[4] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 30 | NTRX01BN[5] | ENET plane 0 feed bulkhead assembly[5] |
| | 46 | NTRX01BQ[5] | ENET plane 0 return bulkhead assembly[5] |
| | 46 | P0715769[6] | 16–in. (410–mm) filler faceplate[6] |

***Note 1:*** One NTRX02BA breaker panel is in shelf position 30 or 46. Each shelf has one NTRX02BA to power non-SuperNode-based cabinets in an alignment.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit for the use of a breaker panel assembly in shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit for a provisioned breaker panel assembly in shelf position 30.

***Note 3:*** Each NTRX31CA provides for one NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable. The cables are provided when two breaker panels are required. The cables are also provided for a provisioned single breaker panel in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided for a provisioned single panel. The panel is in shelf position 30.

***Note 4:*** One NTRX02BB breaker panel assembly is in shelf position 30. Only one breaker panel is present when a SuperNode (including SuperNode ENET) cabinet powers alignments. Only one SuperNode cabinet is in the alignment.

***Note 5:*** One NTRX01BN ENET plan 0 feed bulkhead assembly and one NTRX01BQ ENET plan 0 RTN bulkhead assembly are provided. The assemblies are provided when an NT9X05AB ENET cabinet, plane 0, is in the same alignment as the NTRX31CA.

***Note 6:*** Shelf powitions 30 or 46 provides one P0715769 16-in. (410-mm) filler faceplate when either is unequipped with a breaker panel.

***Note 7:*** One NTRX01BP ENET plane 1 feed bulkhead assembly and one NTRX01BR ENET plane 1 RTN bulkhead assembly are provided. The assemblies are provided when an NT9X05AB ENET cabinet, plane 1, is in the same alignment as the NTRX31CA.

***Note 8:*** NTZZ13MA is a building block code and refers to the composite PECs, as listed.

***Note 9:*** One NTRX02BD breaker panel is in shelf position 30 or 46. Each shelf has one NTRX02BD to power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in an alignment.

## **NTRX31CA** (continued)

**Power distribution shelf provisioning options (Sheet 3 of 4)**

| | | | |
|---|---|---|---|
| NTX905AB ENET, plane 1 in alignment | 30 | NTRX02BB[4] | Breaker panel assembly[4] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 30 | NTRX01BP[7] | ENET plane 1 feed bulkhead assembly[7] |
| NTX905AB ENET, plane 1 in alignment (continued) | 46 | NTRX01BR[7] | ENET plane 1 return bulkhead assembly[7] |
| | 46 | P0715769[6] | 16–in. (410–mm) filler faceplate[6] |
| SuperNode | 30 | NTRX02BB[4] | Breaker panel assembly[4] |
| | 30 | NTRX02AC[2] | Breaker panel 2 to junction box kit[2] |
| | 30 | NTRX2692[3] | -48V ABS cable[3] |

***Note 1:*** One NTRX02BA breaker panel is in shelf position 30 or 46. Each shelf has one NTRX02BA to power non-SuperNode-based cabinets in an alignment.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit for the use of a breaker panel assembly in shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit for a provisioned breaker panel assembly in shelf position 30.

***Note 3:*** Each NTRX31CA provides for one NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable. The cables are provided when two breaker panels are required. The cables are also provided for a provisioned single breaker panel in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided for a provisioned single panel. The panel is in shelf position 30.

***Note 4:*** One NTRX02BB breaker panel assembly is in shelf position 30. Only one breaker panel is present when a SuperNode (including SuperNode ENET) cabinet powers alignments. Only one SuperNode cabinet is in the alignment.

***Note 5:*** One NTRX01BN ENET plan 0 feed bulkhead assembly and one NTRX01BQ ENET plan 0 RTN bulkhead assembly are provided. The assemblies are provided when an NT9X05AB ENET cabinet, plane 0, is in the same alignment as the NTRX31CA.

***Note 6:*** Shelf powitions 30 or 46 provides one P0715769 16-in. (410-mm) filler faceplate when either is unequipped with a breaker panel.

***Note 7:*** One NTRX01BP ENET plane 1 feed bulkhead assembly and one NTRX01BR ENET plane 1 RTN bulkhead assembly are provided. The assemblies are provided when an NT9X05AB ENET cabinet, plane 1, is in the same alignment as the NTRX31CA.

***Note 8:*** NTZZ13MA is a building block code and refers to the composite PECs, as listed.

***Note 9:*** One NTRX02BD breaker panel is in shelf position 30 or 46. Each shelf has one NTRX02BD to power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in an alignment.

**Power distribution shelf provisioning options (Sheet 4 of 4)**

| | | | |
|---|---|---|---|
| | 30 | NTNX2693[3] | ABS return cable[3] |
| | 46 | P0715769[6] | 16–in. (410–mm) filler faceplate[6] |
| SuperNode NT9X0113 cabinet in lineup | 30 | NTZZ13MA[8] | SuperNode bulkhead panel assembly, which consists of these components:[8]<br>NTRX01AK—connector plate assembly return<br>NTRX01AM—connector plate assembly feed<br>NTRX73AC—EMI skin panel<br>NTRX73AF—mid–lineup EMI panel |

***Note 1:*** One NTRX02BA breaker panel is in shelf position 30 or 46. Each shelf has one NTRX02BA to power non-SuperNode-based cabinets in an alignment.

***Note 2:*** Use one NTRX02AE breaker panel 1 to junction box kit for the use of a breaker panel assembly in shelf position 46. Use one NTRX02AC breaker panel 2 to junction box kit for a provisioned breaker panel assembly in shelf position 30.

***Note 3:*** Each NTRX31CA provides for one NTMX2643 -48V ABS cable and one NTMX2644 ABS return cable. The cables are provided when two breaker panels are required. The cables are also provided for a provisioned single breaker panel in shelf position 46. One NTNX2692 -48V ABS cable and one NTNX2693 ABS return cable are provided for a provisioned single panel. The panel is in shelf position 30.

***Note 4:*** One NTRX02BB breaker panel assembly is in shelf position 30. Only one breaker panel is present when a SuperNode (including SuperNode ENET) cabinet powers alignments. Only one SuperNode cabinet is in the alignment.

***Note 5:*** One NTRX01BN ENET plan 0 feed bulkhead assembly and one NTRX01BQ ENET plan 0 RTN bulkhead assembly are provided. The assemblies are provided when an NT9X05AB ENET cabinet, plane 0, is in the same alignment as the NTRX31CA.

***Note 6:*** Shelf powitions 30 or 46 provides one P0715769 16-in. (410-mm) filler faceplate when either is unequipped with a breaker panel.

***Note 7:*** One NTRX01BP ENET plane 1 feed bulkhead assembly and one NTRX01BR ENET plane 1 RTN bulkhead assembly are provided. The assemblies are provided when an NT9X05AB ENET cabinet, plane 1, is in the same alignment as the NTRX31CA.

***Note 8:*** NTZZ13MA is a building block code and refers to the composite PECs, as listed.

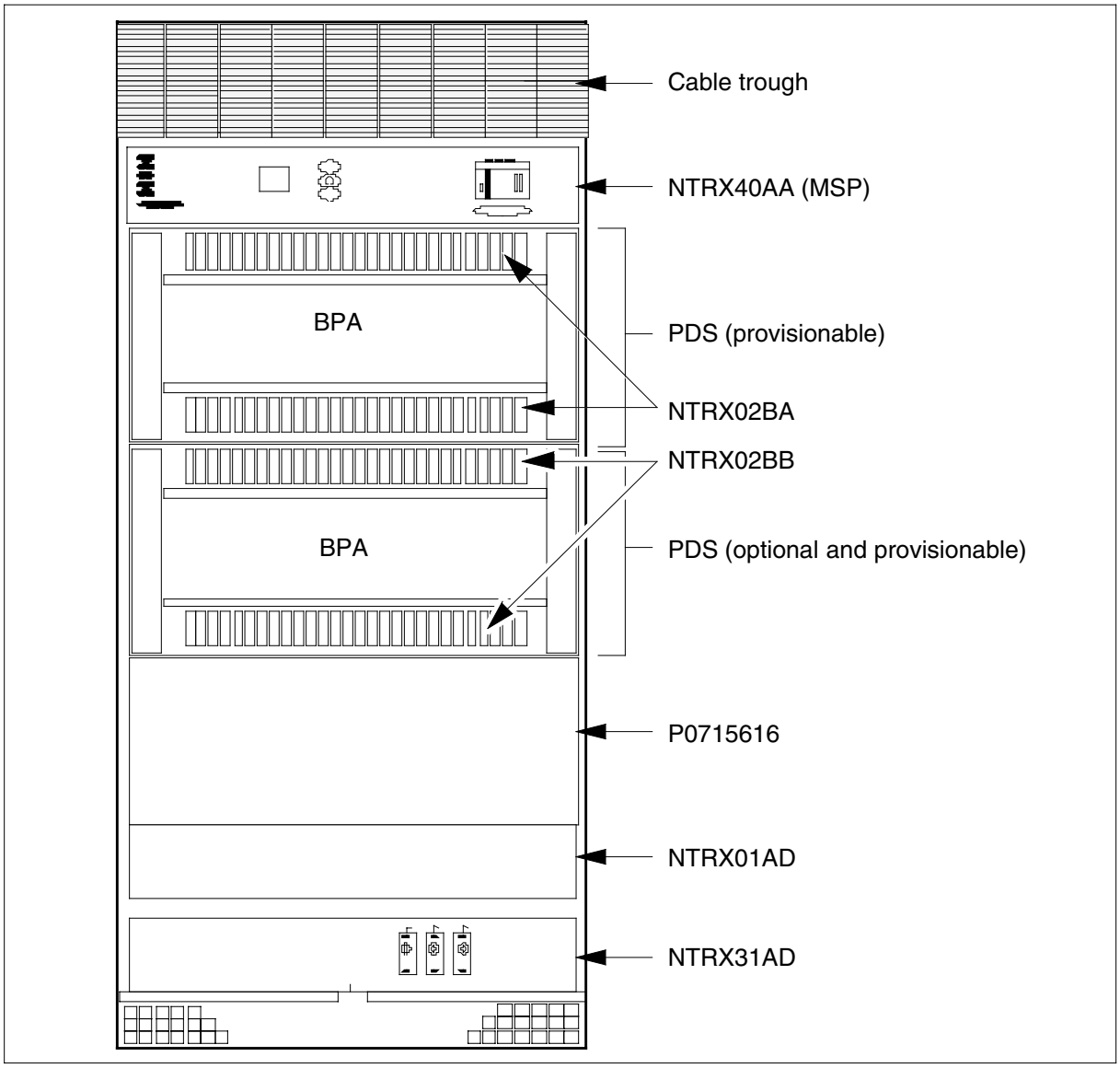
***Note 9:*** One NTRX02BD breaker panel is in shelf position 30 or 46. Each shelf has one NTRX02BD to power S/DMS-based, non-SuperNode (ECORE, ENET, LPP) cabinets in an alignment.

## Design

The design of the NTRX31CA appears in the following figure.

# **NTRX31CA** (end)

**NTRX31CA parts**




***Note:*** Front panels appear to describe the NTRX31CA parts. This diagram is not to scale.

# NTRX31DH

## Product description

The NTRX31DH Inverter unit is a 500-W dc to ac inverter. The inverter provides a protected 120V (ac) at 60 Hz supply from an input source of -48V (dc) nominal. The unit can provide 500W with a total harmonic distortion of less than 5%.

This unit is equipped with two dual ac receptacles on the rear for ac output. The receptacles supply power to four devices; the total cannot exceed 500W. The -48V(dc) input connects to the unit by terminals on the rear of the unit. Circuit breakers (labeled *DC In on/off and AC Out on/off) are on the front panel. The circuit breakers supply the dc input to the inverter and distribute the inverter to the ac receptacles.*

A rack-mountable case encloses the inverter. The case can mount the following frames:

- a Miscellaneous equipment (MIS) frame
- an Input/output equipment (IOE) frame
- a Modem equipment (MOE) frame.

## Parts

The NTRX31DH contains the following parts:

- Inverter Fail Alarm lamp
- circuit breakers
  - — DC In on/off switch
  - — AC Out on/off switches
- AC output receptacles
  - — Circuit 1
  - — Circuit 2
- Alarm Mode Select switch
- Inverter Failure terminal block
- Terminal G chassis ground bus
- BR (battery return) terminal
- -48V terminal

## **NTRX31DH** (continued)

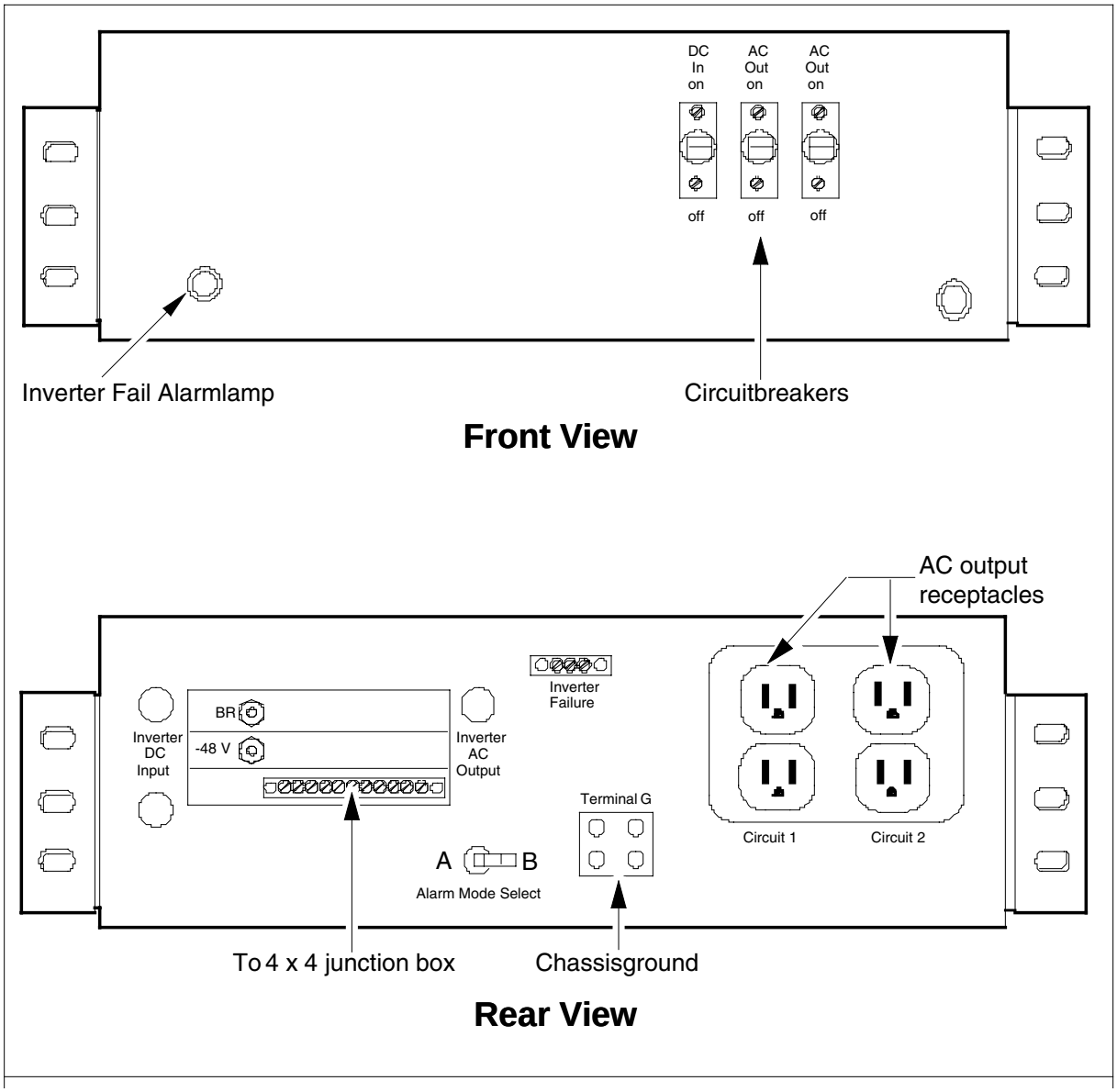
## Design

The design of the NTRX31DH appears in the following figure.

**NTRX31DH parts**

| PEC | Slot | Description |
|---|---|---|
| - | - | *AC output receptacles*<br>Two dual ac receptacles provide access to the normal 120V (ac), 60 Hz output. |
| - | - | *Inverter Fail Alarm lamp*<br>Illuminates (red) when -48V is not present. |
| - | - | *Circuit breakers*<br>Two **AC Out on/off** switches to control the ac output circuits labeled **Circuit 1** and **Circuit 2**. One**DC In on/off**switch to control the dc input (labeled **BR** and **-48V**). |
| - | - | *Alarm Mode Select switch*<br>When in the **A** position, a voltage failure occurs before the breaker stage (called INVERTER FAILURE ALARM) can detect the failure. When in the **B** position, when a voltage failure at the output of the inverter occurs the failure trips the alarm. A name for a failure at the output inverter is AC BRK/INV FAIL COMBINED ALARM. The default setting is position **A** (INVERTER FAILURE ALARM). |
| - | - | *Inverter Failure terminal block*<br>Three-position terminal block used to wire the NTRX31DH for inverter failure. |
| - | - | *Terminal G*<br>Four post terminals used for chassis ground. |
| - | - | *BR (battery return) terminal*<br>25-20 stud post used for battery return input termination. |
| - | - | *-48V terminal*<br>25-20 stud post used for -48V (dc) return input termination. |
| - | - | *Terminal block*<br>11-position block used for termination of two sets of circuits: ac equipment grounding (ACEG1 and 2), ac line (L1 and 2) and ac neutral (N1 and 2) wiring to a 4 x 4 junction box. |

**NTRX31DH front and rear views**



# NTRX32AA

## Product description

The Cabinetized Trunk Module Equipment (CTME) provides the same basic functions as the DMS-100 Trunk Module Equipment (TME) frame (NT0X46AB). This cabinet contains the system alarm circuits, trunk and transmission test circuits, and different analog and digital service circuits.

## Parts

The NTRX32AA contains a group of the following parts:

- NTNX26MA—Frame supervisory panel (FSP)
- NTNX27CA—Cooling unit
- NT0X84AA—Cage filler panel assembly
- NT2X5229—8-wire trunk shelf assembly
- NT2X58CA—Maintenance trunk module
- NT2X58CB—Maintenance trunk module (MTM) for digital recorded announcement (DRA)
- NT3X89AA—Alarm X-CONN shelf
- P0684448—2-in. filler panel

### Frame supervisory panel

The NTNX26MA FSP is in the top of the cabinet at shelf position 60. The NTNX26MA distributes and controls power and alarms in the cabinet. The FSP provides a frame fail light.

### Cooling unit

The forced air from an NTNX27CA fan unit in the base of the cabinet cools the NTRX32AA.

### Cage filler panel assembly

The NT0X84AA cage filler panel assembly fills shelf positions that are not used. The assembly fills shelf positions 47, 33, 19, and 05.

### 8-wire trunk shelf assembly

The NT2X5229 shelf assembly contains the NT2X52AS TM8 common circuit pack. The TM8 is a trunk module with 120 pairs (8-wire circuits) of conductors wired to the distribution cabinet. The shelf contains a maximum of 15 interface cards.

A maximum of four NT2X5229 shelf assemblies can mount in the NTRX32AA, at positions 47, 33, 19, and 05.

### Maintenance trunk module

The NT2X58CA MTM is like the NT2X52 trunk module (TM) in operation. The primary function of the TM is different from the primary function of the MTM. The primary function of the MTM is to interface service, test, and maintenance circuits and scanner and signal distributor cards.

When the MTM does not use other features, a maximum of four MTM shelves can mount in the NTRX32AA. The shelves mount in shelf positions 47, 33, 19, and 05.

The NT3X89AA alarm crosspoint unit (AXU) and the primary alarm MTM comprise an operating pair. The MTM is abbreviated in this condition as OAU. The MTM and the NT3X89AA must mount together in the same cabinet. The AXU must mount in position 47. In the first cabinet, the primary alarm MTM must mount in position 33. The abbreviated name for this pair of shelves is AXU/OAU.

The secondary alarm MTM is in position 47 of the second NTRX32AA.

### Maintenance trunk module for digital recorded announcement

The NT2X58CB MTM for DRA shelf provides a set of one or more phrases. The phrases are routed to a subscriber as a recorded announcement. The digital recorded announcement machine stores the DRA. The system software initiates the DRA.

### Alarm X-conn shelf

The AXU functions as a cross-connect facility for the office alarm system. The AXU is not a trunk module. Each office can receive a maximum of one AXU.

The AXU (NT3X89AA) and primary alarm MTM (NT2X58CA) comprise an operating pair and must mount together in the same cabinet. The AXU is limited to position 47. In the first cabinet, the primary alarm MTM is limited to position 33.

### 2-in. filler panel

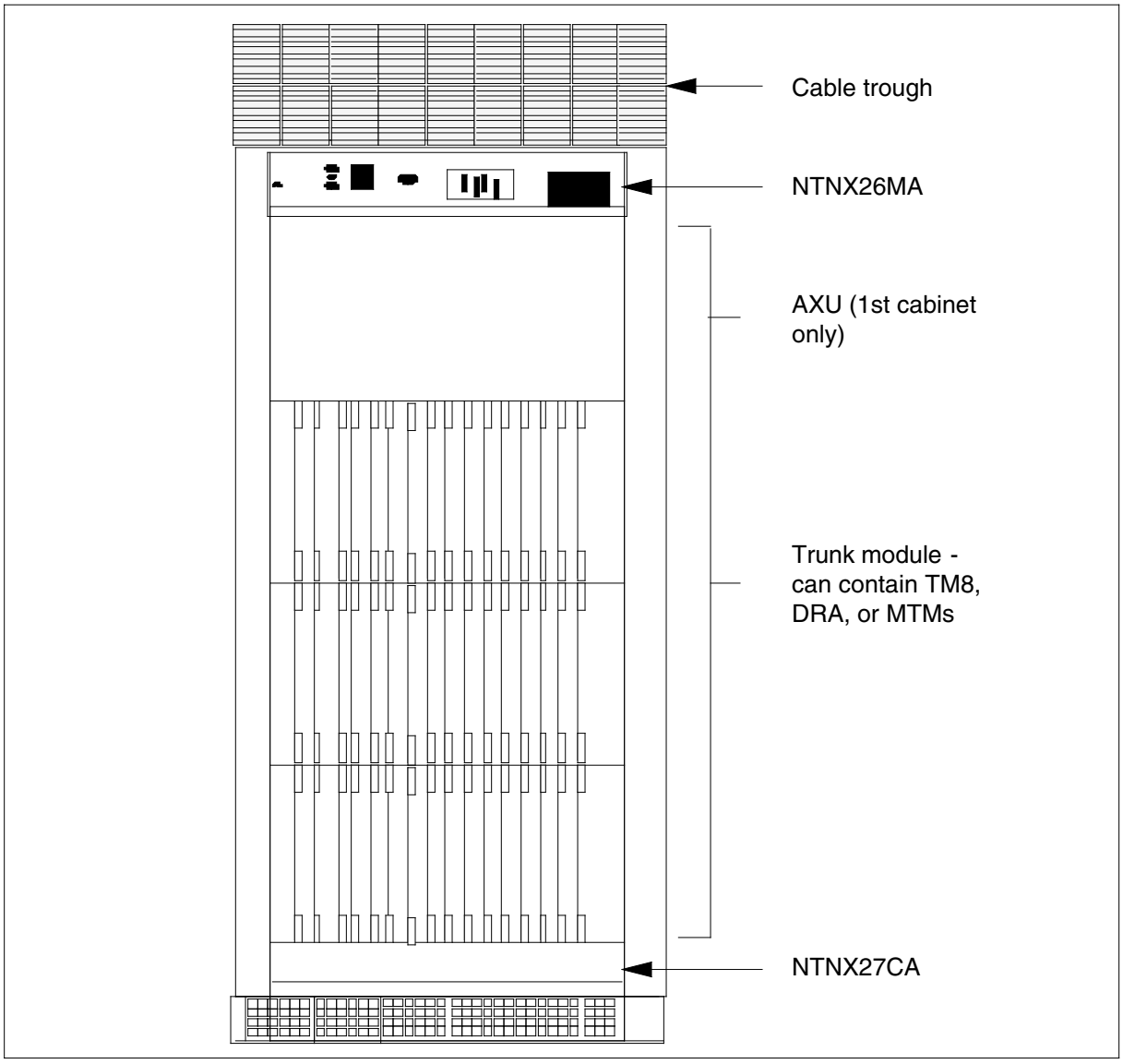
The P0684448 filler panel mounts at shelf position 65, above the FSP. The P0684448 fills in the space that is not used at position 65.

## Design

The design of the NTRX32AA appears in the following figure.

# **NTRX32AA** (end)

**NTRX32AA parts**




***Note:*** Front panels are removed in order to illustrate NTRX32AA parts. This diagram is not drawn to scale.

# NTRX32BA

## Product description

The NTRX32BA cabinetized trunk module equipment (CTME) provides the same basic functions as the DMS-100 trunk module equipment (TME) frame (NT0X46AB). This cabinet contains the system alarm circuits, trunk and transmission test circuits, and different analog and digital service circuits.

## Parts

The NTRX32BA contains a group of the following parts:

- NT0X84AA—cage filler panel assembly
- NT2X5231—international T8A shelf assembly
- NT2X5232—international TM8 shelf assembly
- NTRX58BC—international maintenance trunk module shelf assembly
- NT2X58BD—maintenance trunk module (MTM) for digital recorded announcement (DRA)
- NT3X89AA—alarm X-conn shelf
- NTNX40AA—modular supervisory panel (MSP)
- NTRX51AA—cooling unit

### Cage filler panel assembly

The NT0X84AA cage filler panel assembly fills shelf positions that are not used. The assembly fills shelf positions 47, 33, 19, and 05.

### International T8A shelf assembly

The NT2X5231 shelf assembly contains the NT2X52CB IT8A common fill. The IT8A is a trunk assembly with 120 pairs (8-wire circuits) of conductors wired to the distribution cabinet. The shelf can contain a maximum of 15 interface cards.

A maximum of four NT2X5231 shelf assemblies can be mounted in the NTRX32BA, at positions 47, 33, 19, and 05.

### International TM8 shelf assembly

The NT2X5232 shelf assembly contains the NT2X52CA ITM8 common fill. ITM8 is a trunk module with 120 pairs (8-wire circuits) of conductors wired to the distribution cabinet. The shelf can contain a maximum of 15 interface cards.

A maximum of four NT2X5232 shelf assemblies can mount in the NTRX32BA, at positions 47, 33, 19, and 05.

## **NTRX32BA** (continued)

When the IMTM does not use other features, a maximum of four IMTM shelves can be in the NTRX32BA. The shelves mount in shelf positions 47, 33, 19, and 05.

### International maintenance trunk module

The NT2X58BC IMTM is like the NT2X52 trunk module (TM) in operation. The primary function of the IMTM is to integrate service, test, and maintenance circuits and scanner and signal distributor cards.

The NT3X89AA alarm crosspoint unit (AXU) and the primary alarm MTM (abbreviated here OAU) comprise an operating pair. The NT3X89AA and the MTM must be mounted together in the same cabinet. The AXU appears only in position 47. In the first cabinet, the primary alarm MTM appears only in position 33. The abbreviated name for this pair of shelves is AXU/OAU.

The secondary alarm MTM is in position 47 of the second NTRX32BA.

### Maintenance trunk module for digital recorded announcement

The NT2X58BD IMTM for DRA shelf provides a set of one or more phrases. The phrases are routed to a subscriber as a recorded announcement. The digital recorded announcement machine stores the DRA. The system software initiates the DRA. The DRA can mount at shelf positions 47, 33, 19, and 05.

### Alarm X-conn shelf

The AXU functions as a cross-connect facility for the office alarm system. The AXU is not a trunk module. Each office can contain a maximum of one AXU.

The NT3X89AA AXU and NT2X58BC primary alarm IMTM comprise an operating pair and must mount together in the same cabinet. The AXU appears only in position 47. In the first cabinet, the primary alarm MTM appears only in position 33.

### Modular supervisory panel

The NTNX40AA MSP is in the top of the cabinet at shelf position 60. The NTNX40AA distributes and controls power and alarms in the cabinet. The MSP provides a frame fail light.

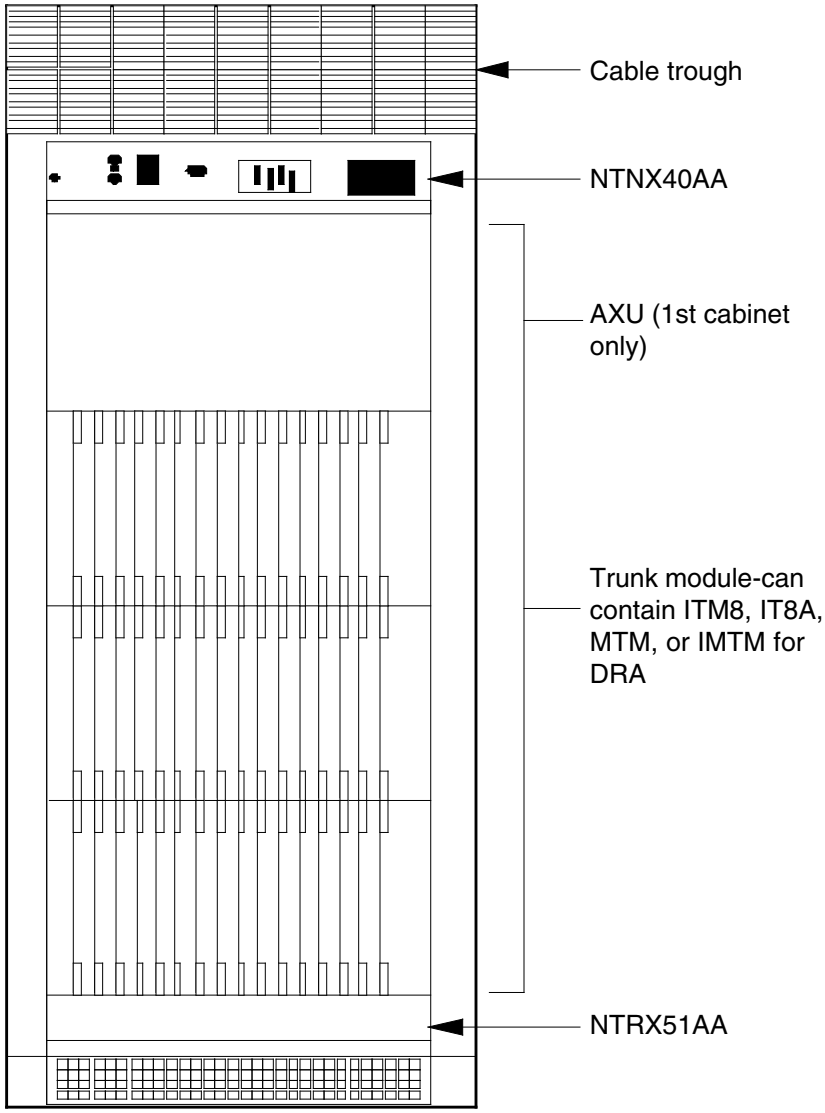
### Cooling unit

The forced air from a fan unit, integrated into the base of the cabinet at shelf position 00, cools the NTRX51AA.

## Design

The design of the NTRX32BA appears in the following figure.

**NTRX32BA parts**




**Note:** Front panels are removed to illustrate NTRX32BA parts. This illustration is not drawn to scale.

# NTRX32CA

## Product description

The cabinetized trunk module equipment (CTME) provides the same functions as the DMS-100 trunk module equipment (TME) frame (NT0X46AB). This cabinet contains the following:

- system alarm circuits
- trunk and transmission test circuits
- miscellaneous analog and digital service circuits

## Parts

The NTRX32CA is a combination of the following parts:

- NTRX40AA—modular supervisory panel (MSP)
- NTNX27CA—cooling unit
- NT0X84AA—cage filler panel assembly
- NT2X5229—8-wire trunk shelf assembly
- NT2X58CA—maintenance trunk module
- NT2X58CB—maintenance trunk module (MTM) for digital recorded announcement (DRA)
- NT3X89AA—alarm X-conn shelf
- P0684448—2 in. (51 mm) filler panel

### Modular supervisory panel

The NTRX40AA MSP is in the top of the cabinet, at shelf position 60. The NTRX40AA MSP distributes and controls power and alarms in the cabinet. The MSP provides a frame fail light.

### Cooling unit

Forced air from an NTNX27CA fan unit cools the NTRX32CA. The fan is in the base of the cabinet.

### Cage filler panel assembly

The NT0X84AA cage filler panel assembly fills in shelf positions 47, 33, 19 and 05.

### 8-wire trunk shelf assembly

The NT2X5229 shelf assembly contains the NT2X52AS TM8 common circuit pack. The TM8 is a trunk module with 120 pairs (8-wire circuits) of conductors wired to the distribution cabinet. A maximum of 15 interface cards can be assigned to the shelf.

You can mount a maximum of four NT2X5229 shelf assemblies in the NTRX32CA, at positions 47, 33, 19 and 05.

### Maintenance trunk module

The NT2X58CA MTM is like the NT2X52 trunk module (TM) in operation. The primary function of the MTM is to integrate service, test and maintenance circuits and scanner and signal distributor cards.

You can mount a maximum of four MTM shelves in the NTRX32CA. You can mount the shelves at shelf positions 47, 33, 19 and 05 when the MTM works alone.

The MTM can combine with the NT3X89AA alarm crosspoint unit (AXU). The primary alarm MTM is abbreviated as OAU. The two comprise a functional pair and must mount together in the same cabinet. The AXU must be in position 47. In the first cabinet, the primary alarm MTM must be in position 33. The abbreviated name for this pair of shelves is AXU/OAU.

The secondary alarm MTM is in position 47 of the second NTRX32CA.

### Maintenance trunk module for digital recorded announcement

The NT2X58CB MTM for DRA shelf provides a set of one or more phrases. The system routes these phrases to a subscriber as a recorded announcement. The digital recorded announcement machine stores the DRA. The system software initiates the DRA.

### Alarm X-conn shelf

The AXU functions as a cross-connect facility for the office alarm system. The AXU is not a trunk module. A maximum of one AXU is available for each office.

The AXU (NT3X89AA) and primary alarm MTM (NT2X58CA) are a functional pair. You must mount the AXU and primary alarm MTM together in the same cabinet. The AXU must be in position 47. In the first cabinet, the primary alarm MTM must be in position 33.

### 2 in. filler panel

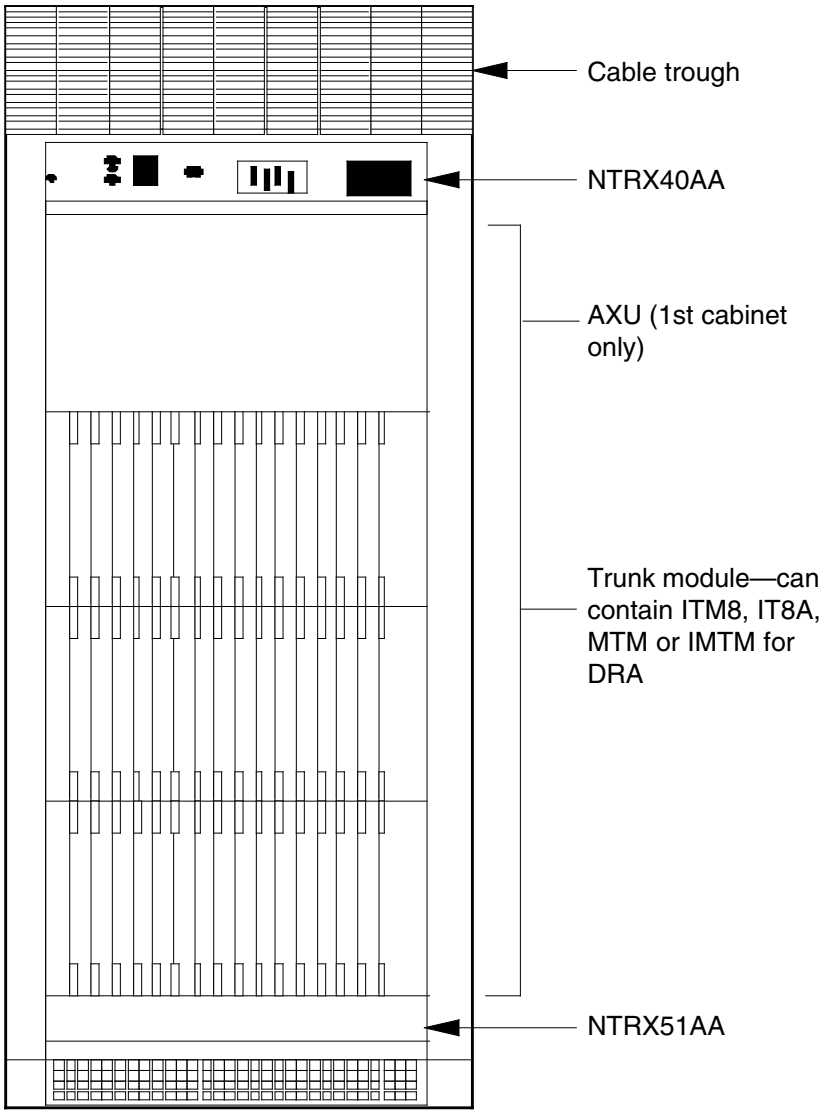
The P0684448 filler panel is at shelf position 65. The P068448 is above the FSP. The P068448 fills in the space at this position.

## Design

The design of the NTRX32CA appears in the following figure.

# NTRX32CA (end)

**NTRX32CA parts**




**Note:** Front panels appear removed to illustrate NTRX32CA parts. This illustration is not to scale.

# NTRX33AA

## Product description

The NTRX33AA cabinetized input/output equipment (CIOE) contains the input/output (I/O) devices. These I/O devices interface the MAP with the DMS-100 Family parts. You can mount these I/O devices on a frame.

The NTRX33AA maintains the functionality of the NT0X43 IOE frame.

## Parts

An equipped NTRX33AA is a combination of the following parts:

- NTNX26MA—Frame supervisory panel (FSP)
- NTNX27CA—Cooling unit
- NT0X44AB—Magnetic tape drive unit (MTD)
- NT0X44BB—International magnetic tape drive unit
- NT0X84AA—Cage filler panel assembly
- NT1X61AD—Input/output controller shelf (IOC)
- NT3X95AB—Stratum II remote oscillator shelf
- NT3X95BB—Stratum 2.5 remote oscillator shelf
- NT4X00AF—Dual disk drive unit (DDU)
- NT8X48AD—Distributed processing peripheral shelf (DPP)
- P0575239—Filler panel
- P0729518—Personality plate

### Frame supervisory panel

The FSP for the NTRX33AA is in the top of the cabinet, in shelf position 60. The FSP distributes and controls power and alarms in the cabinet. The FSP provides a frame fail light.

### Cooling unit

A NTNX27CA fan unit in the base of the cabinet cools the NTRX33AA.

### Magnetic tape drive unit

The NT0X44AB magnetic tape drive unit (Cook) stores customer information. This information relates to the operation of the DMS-100 Family of digital switches. The automatic message accounting system (AMA) uses the tape unit or a hard disk unit to store call accounting information.

The NT0X44AB tape drive unit uses a reel-to-reel format.

## **NTRX33AA** (continued)

### International magnetic tape drive unit

The NT0X44BB international magnetic tape drive unit (Cook) stores customer information. This information relates to the operation of the DMS-100 Family of digital switches. For example, the AMA uses the tape unit or a hard disk unit to store call accounting information.

The NT0X44BB tape drive unit mounted uses a reel-to-reel format.

### Cage filler panel assembly

The NT0X84AA cage filler panel assembly fills in shelf position 05 when the panel is not in use.

### Input/output controller shelf

The IOC is an equipment shelf that provides an interface for a maximum of 36 input/output devices and the central message controller. The IOC contains a peripheral processor that independently performs local tasks. These tasks relieve the load on the central processing unit.

### Stratum II remote oscillator shelf

The NT3X95AA stratum II remote oscillator shelf contains two NT3X16AA stratum 2 oscillator and interface cards. The oscillator shelf contains dedicated power converters. One NT3X16AA card remains in active mode. The other card remains inactive and is available as a backup to the active card.

The NT3X95AB shelf substitutes for the NT3X95AA shelf in isolated system ground (ISG) offices. The AB shelf is the ISG version of the AA card.

The function of the NT3X16AA oscillator and interface card defines the function of the NT3X95AA shelf.

The NT3X16AA card provides a clock frequency signal that controls circuit timing. The signal controls timing in the peripherals, networks and interfaces of the DMS-100 Family of digital switches.

The NT3X16AA card is part of the synchronizable master clock system. The NT3X16AA card operates with the NT3X15DA Stratum 2 synchronizable master clock card and the NT3X14 synchronizable master clock system.

### Stratum 2.5 remote oscillator shelf

The NT3X95BB stratum 2.5 remote oscillator shelf contains the following:

- four NT3X16BB stratum 2.5 oscillator and interface cards
- two dedicated power converters for the active and inactive cards

One NT3X16BB card remains in active mode. One card remains in an inactive mode. Two optional cards are in hot standby mode.

Place these two optional hot standby cards in service manually when this action is necessary. The inactive card automatically comes on line when a problem occurs with the active card.

The NT3X95BB shelf substitutes for the NT3X95BA shelf in ISG offices. The BB shelf is the ISG version of the BA card.

The function of the NT3X16BB oscillator and interface card defines the function of the NT3X95BB shelf.

The NT3X16BB card provides a clock frequency signal that controls circuit timing. The signal controls timing in the peripherals, networks and interfaces of the DMS-100 Family of digital switches.

The NT3X16BB card is part of the synchronizable master clock system.

The NT3X16BB card operates with the NT3X15DA stratum 2 synchronizable master clock card and the NT3X14 synchronizable master clock system.

### Dual disk drive unit

The NT4X00AF DDU contains two 228.7 Mbyte, 5.25 in. (133 mm) disk drive units and two associated NT1X78AA power converters. The DDU functions as the primary mass storage system of the office.

The NT4X00AF DDU must be in shelf position 05 in the NTRX33AA.

### Distributed processing peripheral shelf

The NT8X48AD DPP is a peripheral module that allows remote polling of AMA information. The DPP contains two 760-Mbyte disk drives and the necessary interfaces and cables.

When used in the NTRX33AA, the DPP is in shelf position 33. An MTD normally fills this position. The DPP requires a P0729518 personality (filler) plate in shelf position 47.

### Filler panel

The P0575239 filler panel fills shelf positions 47 and 33 when the shelf positions are not in use. When a DPP is in shelf position 33, this restriction does not apply. When a DPP is in shelf position 33, a P0729518 plate is in shelf position 47.

## **NTRX33AA** (end)

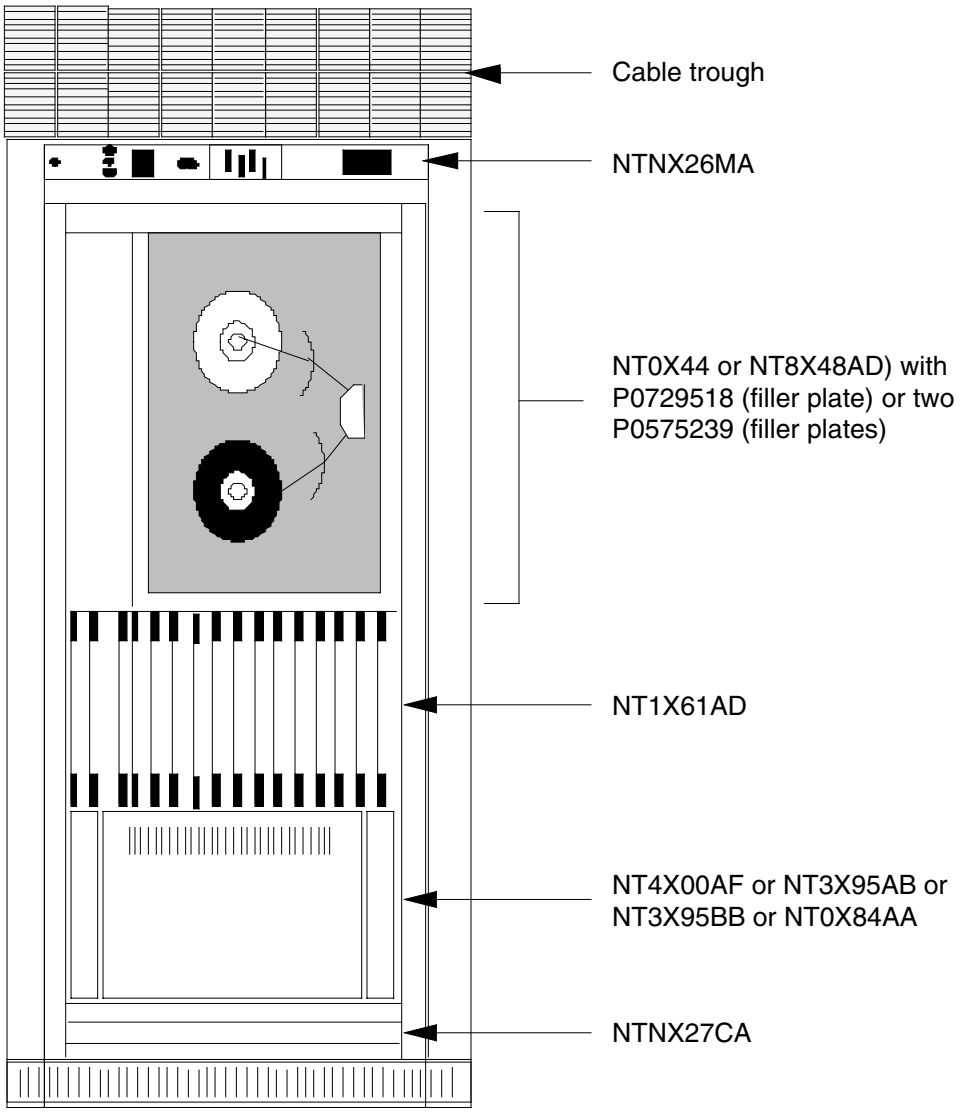
### Personality plate (DPP)

When a DPP is in shelf position 33, a P0729518 plate is in shelf position 47.

## Design

The design of the NTRX33AA appears in the following figure.

**NTRX33AA parts**




**Note:** Front panels appear removed to illustrate NTRX33AA parts. This illustration is not to scale.

# NTRX33CA

## Product description

The NTRX33CA cabinetized input/output equipment (CIOE) houses specified input/output (I/O) devices. The CIOE houses all devices that connect the MAP terminal with the DMS–100 Family parts. You can mount the I/O devices that connect the MAP terminal with the DMS–100 family parts on a frame.

The NTRX33CA maintains all the functionality of the NT0X43 IOE frame.

## Parts

A fully equipped NTRX33CA contains a combination of the following parts:

- NT0X44AB—magnetic tape drive (MTD) unit
- NT0X44BB—international MTD unit
- NT0X84AA—cage filler panel assembly
- NT1X61AD—input/output controller (IOC) shelf
- NT3X95AC—stratum II remote oscillator shelf
- NT4X00AF—dual disk drive unit (DDU) shelf
- NT8X48AD—distributed processing peripheral (DPP) shelf
- NTNX27CA—cooling unit, -48V (dc)
- NTRX40AA—modular supervisory panel (MSP)
- NTRX51AA—cooling unit, -60V (dc)
- P0575239—filler panel
- P0729518—filler panel

### Magnetic tape drive unit

The NT0X44AB magnetic tape drive unit (Cook) stores customer information related to the operation of the DMS–100 Family. For example, the Automatic Message Accounting (AMA) system uses the tape unit or a hard disk unit to store call accounting information.

The NT0X44AB tape drive unit uses a reel–to–reel format.

### International magnetic tape drive unit

The NT0X44BB international magnetic tape drive unit (Cook) stores customer information related to the operation of the DMS–100 Family. For example, the AMA uses the tape unit or a hard disk unit to store call accounting information.

The NT0X44BB tape drive unit uses a reel–to–reel format.

## NTRX33CA (continued)

### Cage filler panel assembly

The NT0X84AA cage filler panel assembly and P0726351 blank personality plate fill in shelf position 05, if 05 is not in use.

When shelf positions 33 and 47 are not in use, two P0575239 filler panel assemblies and one P0715616 blank personality plate fill the positions.

### Input/output controller shelf

The NT1X61AD IOC is an equipment shelf. The NT1X61AD IOC provides an interface for a maximum of nine input/output devices and the central message controller. The IOC contains a peripheral processor that performs local tasks to relieve the load on the central processing unit.

### Stratum II remote oscillator shelf

The NT3X95AC stratum II remote oscillator shelf houses two NT3X16AB stratum II oscillator and interface cards and dedicated power converters. One NT3X16AB statum 2 synchronizable clock card is active. The other card is not active. The card that is not active is available as a backup to the active card.

The function of the NT3X16AB oscillator and interface card define the function of the NT3X95AC.

The NT3X16AB card provides a clock frequency signal. This signal controls circuit timing in the peripherals, networks, and interfaces of the DMS–100 Family.

The NT3X16AB card is part of the synchronizable master clock system. The NT3X16AB operates with the NT3X15DA stratum II synchronizable master clock card and the NT3X14 synchronizable master clock system.

### Dual disk drive unit

The NT4X00AF DDU contains two NT4X00AG 228.7 Mbyte, 133 mm (5.25 in.) disk drive units and two associated NT1X78AA power converters. The DDU functions as the primary mass storage system of the office.

The NT4X00AF DDU is in shelf position 05 in the NTRX33CA.

### Distributed processing peripheral shelf

The NT8X48AD DPP is a peripheral module that allows remote polling of AMA information. The DPP is provisionable with the following option:

- two NT6M72DA or NT6M72DD 380 Mbyte disk drives, or
- two NT6M72EA 760 Mbyte disk drives and the necessary interfaces and cabling

In the NTRX33CA, the DPP is in shelf position 33. If the DPP is not mounted in shelf position 33, you can install an MTD at this position. The DPP requires a P0729518 personality (filler) plate in shelf position 47.

### Cooling unit

A fan unit forced–air cools the NTRX27CA. The fan unit is in the base of the cabinet. The NTRX51AA uses the cooling unit when the -60V (dc) application is provisioned.

### Modular supervisory panel

The NTRX40AA MSP for the NTRX33CA is in the top of the cabinet, at shelf position 60. The MSP distributes and controls power and alarms in the cabinet. The MSP provides a frame fail light.

### Filler panel

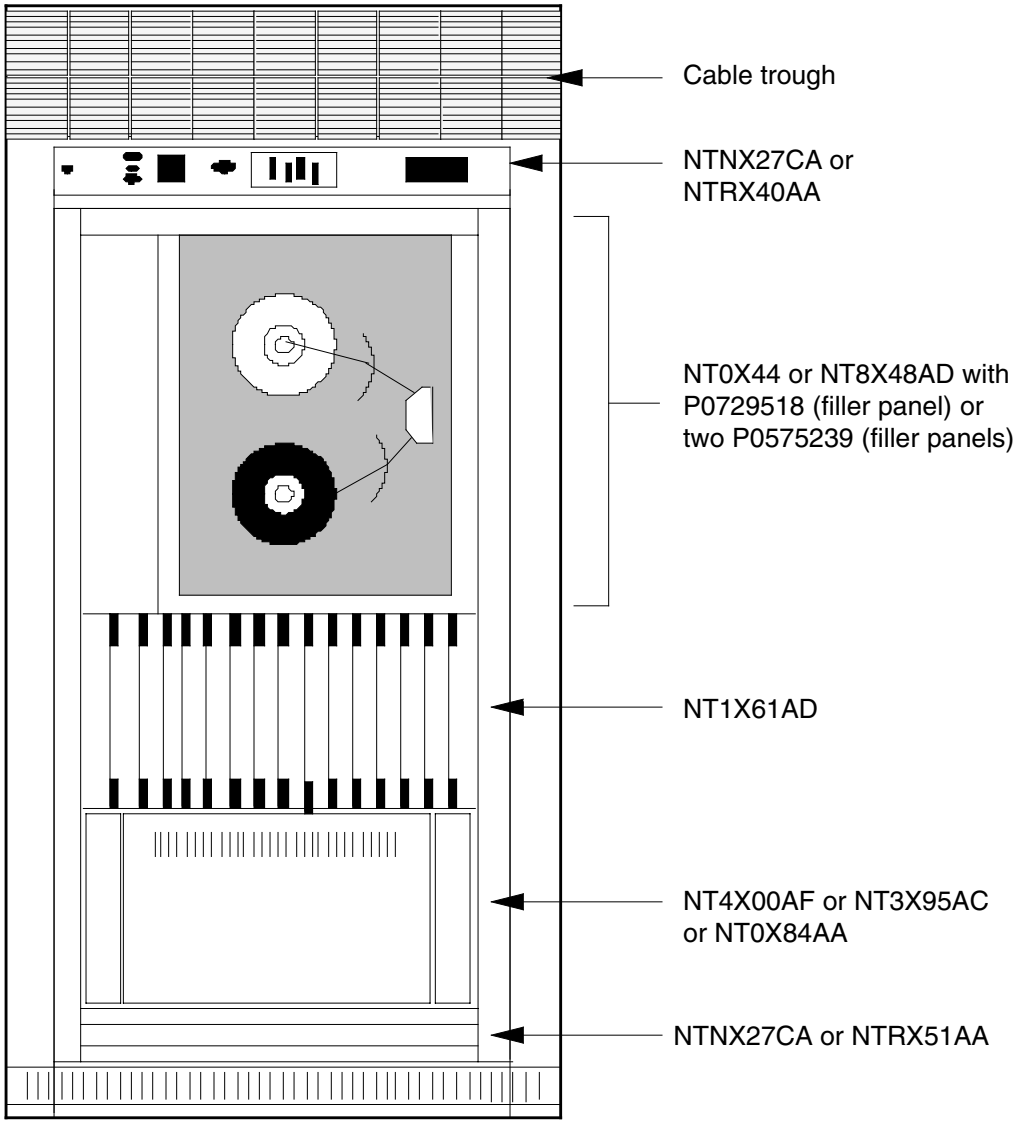
The P0575239 filler panel fills in shelf positions 47 and 33 when the shelf positions are not in use. The filler panel does not fill in shelf positions 47 and 33 when a DPP is in shelf position 33. When a DPP is in shelf position 33, you must mount a P0729518 plate in shelf position 47.

## Design

The design of the NTRX33CA device appears in the following figure.

# **NTRX33CA** (end)

**NTRX33CA parts**




**Note:** Front panels are removed in this figure to illustrate NTRX33CA parts. This figure is not to scale.

# NTRX33DA

## Product description

The NTRX33DA cabinetized input/output equipment (CIOE) houses specified input/output (I/O) devices. The CIOE houses all devices that connect the MAP terminal with the DMS-100 Family parts. You can mount the I/O devices that connect the MAP terminal with the DMS-100 Family parts on a frame.

The NTRX33DA maintains all the functionality of the NT0X43 IOE frame.

## Parts

A fully equipped NTRX33DA is a combination of the following parts:

- NTNX26MA—frame supervisory panel (FSP)
- NTNX27CA—cooling unit
- NT0X44AB—magnetic tape drive unit (MTD)
- NT0X44BB—international magnetic tape drive unit
- NT0X84AA—cage filler panel assembly
- NT1X61AD—input/output controller shelf (IOC)
- NT3X95AB—stratum II remote oscillator shelf
- NT3X95BB—stratum 2.5 remote oscillator shelf
- NT4X00AF—dual disk drive unit (DDU)
- NT8X48AD—distributed processing peripheral shelf (DPP)
- P0575239—filler panel
- P0729518—personality plate

### Frame supervisory panel

The FSP for the NTRX33DA is in the top of the cabinet, in shelf position 60. The FSP distributes and controls power and alarms in the cabinet. The FSP provides a frame fail light.

### Cooling unit

An NTNX27CA fan unit in the base of the cabinet cools the NTRX33DA with forced air.

### Magnetic tape drive unit

The NT0X44AB magnetic tape drive unit (Cook) stores customer information related to the operation of the DMS-100 office. For example, the Automatic Message Accounting (AMA) system uses the tape unit or a hard disk unit to store call accounting information.

## **NTRX33DA** (continued)

The NT0X44AB tape drive unit uses a reel-to-reel format.

### International magnetic tape drive unit

The NT0X44BB international magnetic tape drive unit (Cook) stores customer information related to the operation of the DMS-100 Family. The AMA can use the tape unit or a hard disk unit to store call accounting information.

The NT0X44BB tape drive unit uses a reel-to-reel format.

### Cage filler panel assembly

If 05 is not used, the NT0X84AA cage filler panel assembly fills in shelf position 05.

### Input/output controller shelf

The IOC is an equipment shelf. The IOC provides an interface for a maximum of 36 input/output devices and the central message controller. The IOC contains a peripheral processor. The processor performs local tasks to relieve the load on the central processing unit. The IOC is in shelf position 19.

### Stratum II remote oscillator shelf

The NT3X95AA stratum II remote oscillator shelf houses two NT3X16AA stratum II oscillator and interface cards with dedicated power converters. One NT3X16AA card is active. The other card is not active. The card that is not active is available as a backup to the active card.

The NT3X95AB shelf substitutes for the NT3X95AA shelf in isolated system ground (ISG) offices. The AB shelf is the ISG version of the AA card.

The function of the NT3X16AA oscillator and interface card defines the function of the NT3X95AA shelf.

The NT3X16AA card provides a clock frequency signal. The signal controls circuit timing in the peripherals, networks, and interfaces of the DMS-100 Family.

The NT3X16AA card is part of the synchronizable master clock system. The NT3X16AA operates with the NT3X15DA stratum II synchronizable master clock card and the NT3X14 synchronizable master clock system.

### Stratum 2.5 remote oscillator shelf

The NT3X95BB stratum 2.5 remote oscillator shelf houses four NT3X16BB stratum 2.5 oscillator and interface cards. The oscillator shelf houses two dedicated power converters for the active and inactive cards. Of the four cards,

one NT3X16BB card is active and one card is not active. Two optional cards are in hot standby mode.

You must manually place the two optional hot standby cards in service when these cards are needed. The card that is not active automatically comes on line in the event of a problem with the active card.

The NT3X95BB shelf substitutes for the NT3X95BA shelf in ISG offices. The BB shelf is the ISG version of the BA card.

The function of the NT3X16BB oscillator and interface card defines the function of the NT3X95BB.

The NT3X16BB card provides a clock frequency signal. The signal controls circuit timing in the peripherals, networks, and interfaces of the DMS-100 Family.

The NT3X16BB card is part of the synchronizable master clock system. The NT3X16BB operates with the NT3X15DA stratum II synchronizable master clock card and the NT3X14 synchronizable master clock system.

### Dual disk drive unit

The NT4X00AF DDU contains two 228.7 Mbyte, 133 mm (5.25 in.) disk drive units and two associated NT1X78AA power converters. The DDU functions as the primary mass storage system of the office.

You can mount the NT4X00AF DDU only in shelf position 05 in the NTRX33DA.

### Distributed processing peripheral shelf

The NT8X48AD DPP is a peripheral module that allows remote polling of AMA information. The DPP contains two 760-MB disk drives and interfaces and cabling.

In the NTRX33DA, the DPP is in shelf position 33. If the DPP is not in shelf position 33, you can install a MTD at this position. The DPP requires a P0729518 personality (filler) plate in shelf position 47.

### Filler panel

The P0575239 filler panel fills in shelf positions 47 and 33 when the panels are not in use. The filler panel does not fill shelf positions 47 and 33 when a DPP is in in shelf position 33. When a DPP is in in shelf position 33, a P0729518 plate is in shelf position 47.

## **NTRX33DA** (end)

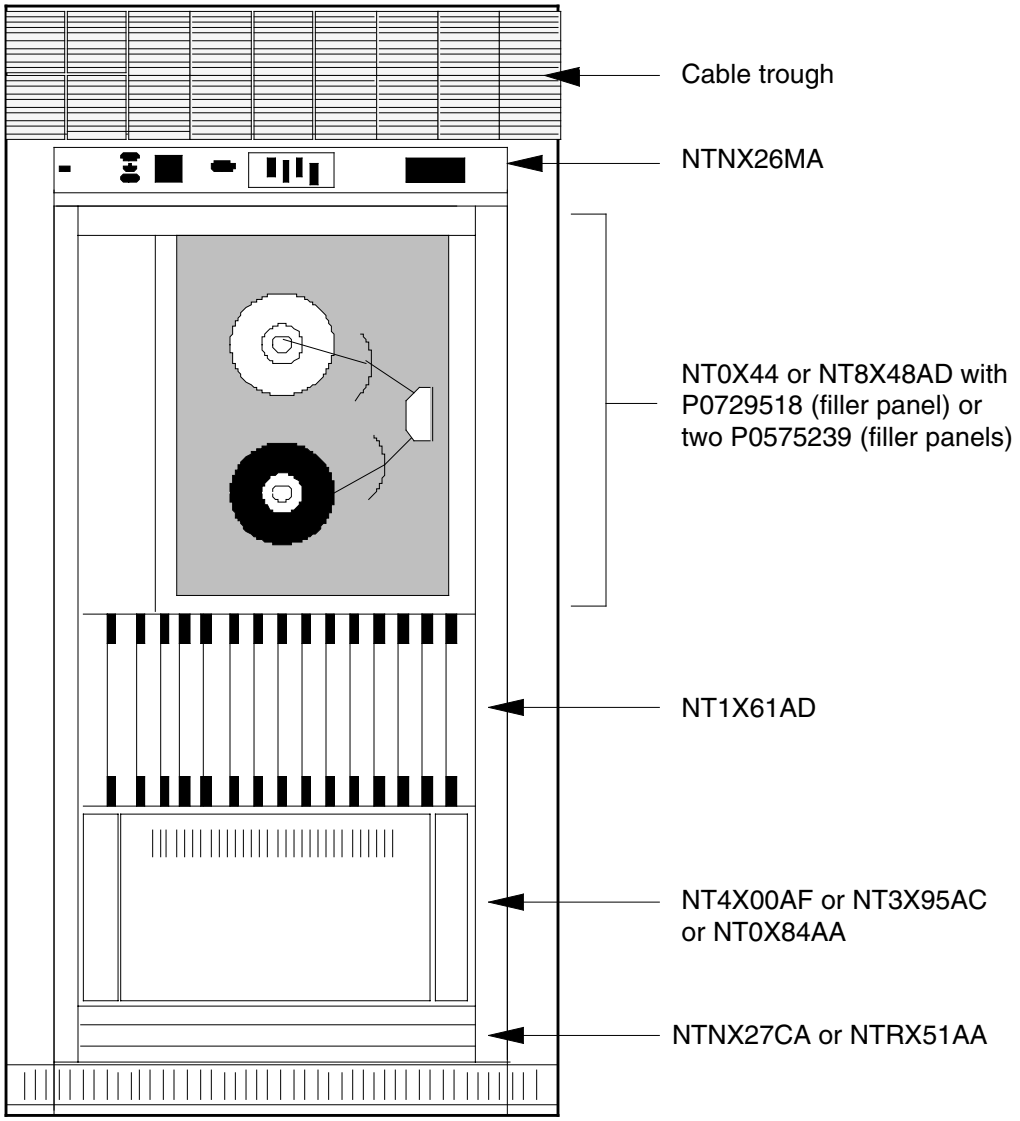
### Personality plate (DPP)

When a DPP is in in shelf position 33, a P0729518 plate is in shelf position 47.

## Design

The design of the NTRX33DA appears in the following figure.

**NTRX33DA parts**




**Note:** Front panels appear removed in the figure to illustrate NTRX33DA parts. This figure is not to scale.

# NTRX34AB

## Product description

The zoned miscellaneous equipment cabinet (CMIS) performs the same functions as the NT0X02AB miscellaneous equipment frame (MIS). The NTRX34AB accommodates different DMS-100 common systems and the hardware that different types of equipment require. Nortel Networks does not manufacture some of this equipment.

The NTRX34AB is provisionable. A customer can select from a list of equipment types. The Frame supervisory panel (FSP) and cooling unit are required at the top and bottom of the NTRX34AB. The FSP and cooling unit are not required when the NTRX34AB functions as an intermediate distribution frame.

The NTRX34AB offers electromagnetic interference (EMI) compliance by inter-lineup connections through shielded cables. The lines that leave the office use filtered connectors on the bulkhead.

The NTRX34AB equipment shelves have different heights. The heights are different from the standard 14 in. height of the DMS-100 shelves. The NTRX34AB has eight zones. Each zone is 178 mm (7 in.) high. Each equipment occupies one zone or multiple zones. All equipment has a corresponding personality plate and zone that associates with the equipment.

## Parts

The NTRX34AB contains a collection of some of the parts of the following parts:

- A0379066 (also listed as M1-1063-901)—Pylon RG-2 ringing generator
- NTNX27CA—Cooling unit
- NTRX31AD—500W LaMarche inverter unit
- NTRX34FI—CMIS terminal block assembly
- NTRX45AA—CMIS frame supervisory panel
- NTZZ18XA—Digital alarm scanner (DAS)
- NT3J00BA—Multiple loop test applique (MLT)
- NT3X25AA—Common equipment shelf assembly
- NT3X25BA—Terminal block assembly
- NT5X69AA—Inactive system timing circuit (ISTC)
- NT5X85AA—Audible/visual alarm extension unit
- NT5X86AA—Audible alarm cutoff control unit

## **NTRX34AB** (continued)

- NT7F18AB—Digital test head/remote office test line unit (DTH-ROTL)
- 905-5222-001—RM4200 data set shelf 115V ac
- 905-5222-003—RM4200 data set shelf -48V dc

### Pylon RG-2 ringing generator

The A0379066 Pylon RG-2 ringing generator (RG) provides an RG that can be mounted in the NTRX34AB. The A0379066 appears as M1-1063-901. The A0379066 has the NT5X85AA audible/visual alarm extension unit.

### Cooling unit

An NTNX27CA fan unit in the base of the cabinet cools the NTRX34AB with forced air.

### 500W LaMarche inverter

The NTRX31AD 500W LaMarche inverter provides 115V ac to units that require a 115V ac source. The units that require a 115V ac source are mounted in the same NTRX34AB as the inverter. The NTRX31AD inverter kit contains the A0367433 LaMarche inverter. The LaMarche inverter converts the -48V (nominal) dc from the office battery to 115V ac.

### CMIS terminal block assembly

Some units do not have dedicated connector plates. These units require the NTRX34FI CMIS terminal block assembly and the associated bulkhead connector mounting plate (P0730995).

### CMIS frame supervisory panel

The NTRX45AA CMIS FSP contains power control and alarm circuits. The power control and alarm circuits provide interfaces between the power distribution center and the equipment mounted in the NTRX34AB.

The FSP provides a focal point for a person to monitor the NTRX34AB. The NTRX45AA provides alarms to warn of problems in the NTRX34AB. An example of a problem is a cooling unit or power inverter that does not work, or operates out of range. The FSP has a frame fail light at the top of the front of the cabinet. The FSP has an electrostatic discharge wrist strap in the front of the cabinet.

### Digital alarm scanner

The NTZZ18XA DAS hardware is provisioned when the DMS office must interface with the Bell Operating Companies Switching Control Centers. The DAS hardware allows the J1P056A-1 DAS to be mounted in the NTRX34AB. Nortel Networks does not supply the DAS.

### Multiple loop test applique

The NT3J00BA MLT applique shelf can mount a maximum of 10 MLT circuit packs required for loop testing.

### Common equipment shelf assembly

The NT3X25AA common equipment shelf provides multiple 115V ac outlets. The outlets power a maximum of two standalone modems and associated data telephone sets, or other standalone equipment.

### Terminal block assembly

The NT3X25BA can locally cross-connect NTRX34AB-mounted equipment, like a bank of modems.

### Inactive system timing circuit

The NT5X69AA inactive system timing circuit records the duration of system downtime.

### Audible/visual alarm extension unit

The NT5X85AA audible/visual alarm extension unit is provisioned when the number of audible alarm panels (NT0X66AA) exceeds two. The NT5X85AA unit is provisioned when the number of exit alarm display panels (NT0X64AA) exceeds four.

The M1-1063-901 Pylon RG-2 is provisioned with the NT5X85AA.

### Audible alarm cutoff control unit

The NT5X86AA audible alarm cutoff control unit is provisioned when selective audible alarm cutoff control requires. This unit can control a maximum of six audible circuits. Use the NT5X86AA with the NT5X86AB audible cutoff key panel. The NT5X86AB is mounted from the outside.

### Digital test head/remote office test line unit

The NT7F18AB DTH/ROTL comes with the circuit packs required to perform the ROTL function.

### RM4200 data set shelf 115-V ac

The 905-5222-001 Case/Datatel RM4200 data set shelf can accommodate a maximum of 16 Datatel 4200 series modems. The 905-5222-001 requires a 115V ac feed, normally from the NTRX31AD inverter. A single NTRX31AD inverter can power a maximum of three 905-5222-001 modem shelves.

## **NTRX34AB** (continued)

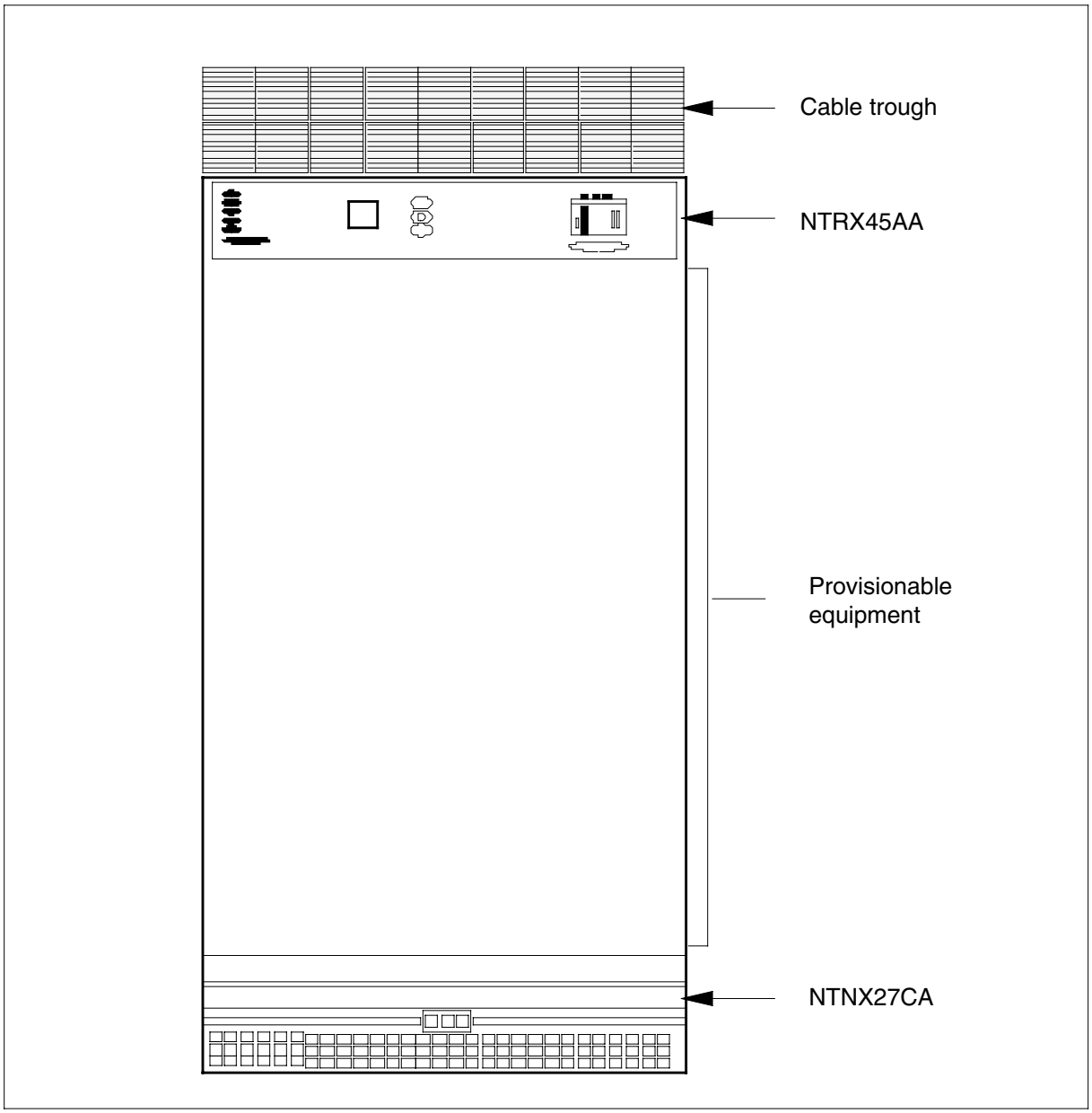
### RM4200 data set shelf -48V dc

The 905-5222-003 Case/Datatel RM4200 data set shelf can accommodate a maximum of 16 Datatel 4200 series modems. The -48V dc feed from the office supply powers the 905-5222-003.

## Design

The design of the NTRX34AB appears in the following figure.

**NTRX34AB parts**



***Note:*** Front panels do not appear in this figure to illustrate NTRX34AB parts. This figure is not drawn to scale.

# NTRX34BA

## Product description

The NTRX34BA cabinetized miscellaneous equipment (CMIS) performs the same functions as the NT0X02AB miscellaneous equipment frame (MIS). The NTRX34BA accommodates different DMS-100 common systems and the hardware that different types of equipment require. Nortel Networks does not manufacture some of this equipment.

The NTRX34BA is provisionable. A customer can select from a list of equipment types. The modular supervisory panel (MSP) and cooling unit are required at the top and bottom of the NTRX34BA. The MSP and cooling unit are not required when the NTRX34BA functions as an intermediate distribution frame.

The NTRX34BA offers electromagnetic interference (EMI) compliance by inter-lineup connections through shielded cables. The lines that leave the office use filtered connectors on the bulkhead.

The NTRX34BA equipment shelves have different heights. The heights are different from the standard 359 mm (14 in.) height of the DMS-100 shelves. The NTRX34BA divides into eight zones. Each zone is 179 mm (7 in.) high. Each piece of equipment occupies one zone or multiple zones.

## Parts

The NTRX34BA contains a collection of some of the following parts:

- A0382364—Benning 60 V dc to 220 V ac, 500 VA (volt ampere) inverter
- A0383125—Stollman ISDN terminal adapter
- A0382126—Racal RD2422 PAG-3 modem
- NT3X25BA—terminal block assembly shelf
- NT3X25CA—common equipment assembly shelf
- NTRX27CA—cooling unit, -48V (dc)
- NTRX40AA—CMIS modular supervisory panel
- NTRX51AA—cooling unit, -60V (dc)
- P0715616—filler faceplate
- P0715775—cover plate
- P0737132—universal mounting plate
- Nokia shelf TF21462, 483 mm (19 in.)
- Retronika V.11/V.35 converter

### Benning 60V dc to 220V ac, 500 VA inverter

The A0382364 inverter is a TEBEVERT-switched-node, single-phase inverter. The A0382364 has a dc input of 60V to 220V. The rated output is 500VA. This inverter has a contactor switch facility. The switching time is less than 100 ms.

### Stollman ISDN terminal adapter

The A0383125 integrated services digital network (ISDN) terminal adapter allows for link-up and data transmission. The A0383125 provides link-up and data transmission by way of two sets of data terminal equipment (DTE). The DTEs have V.11 or V.24 junctions. The DTEs connect to the ISDN terminal. The A0383125 supports junctions for the following terminal devices. The terminal devices have a maximum of 38 kbit/s synchronously and asynchronously with a maximum of 64 kbit/s synchronously.

### Racal RD2422 PAG-3 modem

The A0382126 modem has a standard transmission rate of the CCITT Recommendation V.21 (duplex), V.22 and V.23 (half duplex) bits. The A0382126 has standard modem capabilities with 7 or 8 data bits, parity (odd, even, or none) and maximum signframe. The modem has automatic callback of 16 numbers. The modem has a dial store of 15 numbers.

### Terminal block assembly shelf

The NT3X25BA can cross-connect NTRX34BA-mounted equipment, like a local bank of modems.

### Common equipment assembly shelf

The NT3X25CA common equipment shelf provides multiple 115-V ac outlets. The outlets power a maximum of two standalone modems and associated data telephone sets or other standalone equipment. The NT3X25CA can occupy shelf positions 05, 12, 19, 26, 33, 40, 47 and 54. When the NTRX34BA uses a 60V dc to 220V ac 500 VA inverter, the NT3X25CA cannot use shelf positions 5 and 12. For every two NT3X25CA shelves mounted opposite each other, use one universal mounting plate (P0737132). To cover each connector opening not used in P0737132, use one cover plate (P0715775).

### Cooling unit

The NTRX34BA uses the NTRX51AA cooling unit when the -60V dc application is provisioned. A fan unit in the base of the cabinet cools the NTRX27CA with forced air.

### CMIS modular supervisory panel

The NTRX40AA CMIS MSP contains power control and alarm circuits. The circuits distribute dc voltages of -48V or -60V between the power distribution center and the equipment in the NTRX34BA.

## **NTRX34BA** (continued)

The MSP provides a focal point for a person to monitor the NTRX34BA. The NTRX40AA provides alarms to warn of problems in the NTRX34BA. One example is a cooling unit or power inverter that does not work or that operates out of range. The MSP includes a frame fail light mounted at the top of the front of the cabinet. The MSP has an electrostatic discharge wrist strap in the front of the cabinet.

### Filler faceplate

The P0715616 filler faceplate comes with the NTRX34BA. The P0715616 fills shelf positions 03, 18, 34 and 49 when the positions are not used.

### Nokia shelf

The original equipment manufacturer (OEM) delivers the Nokia shelf to the customer on site. This shelf comprises three zones of equipment. Each zone has three Nokia TU2122.4 data interface units (DIU) and one Nokia TC21100 multiplex (MUX) unit. Each shelf uses one Nokia TV21611 power interface adapter (PIA).

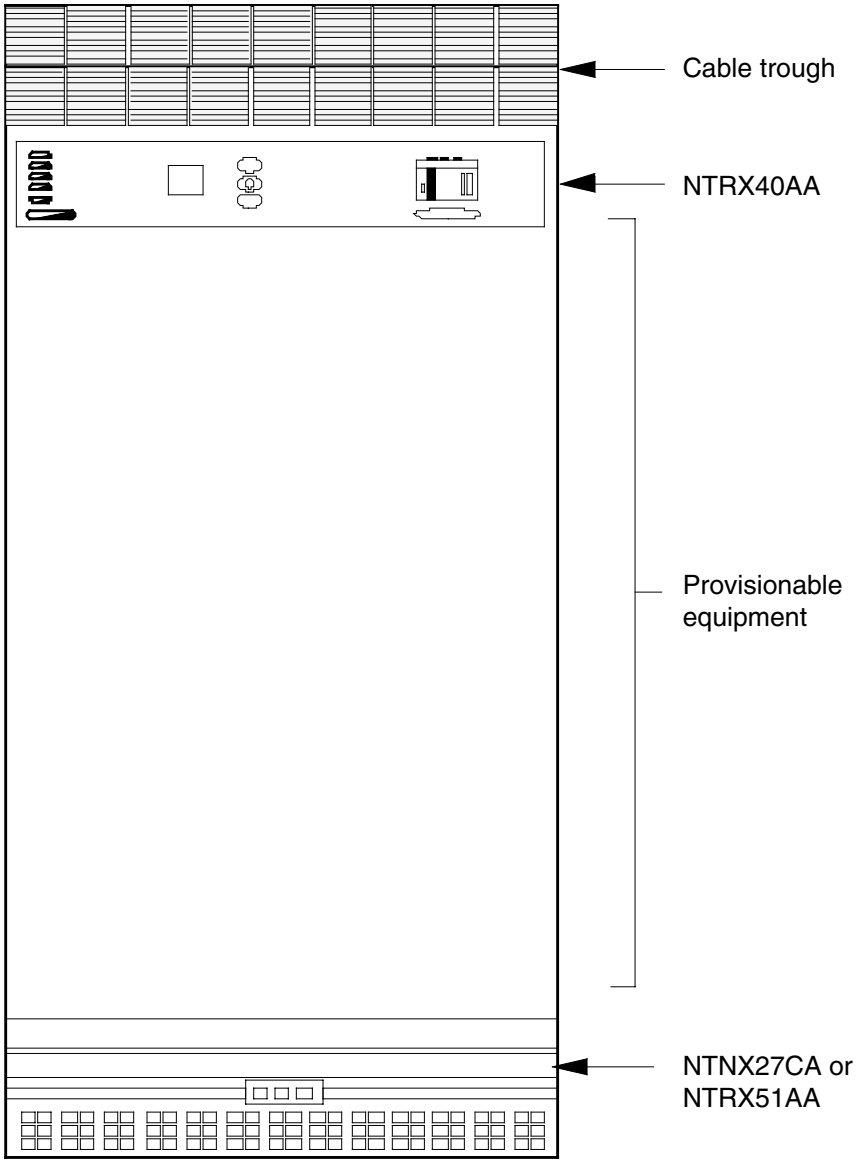
### Retronika V.11/V.35 converter

The OEM delivers this converter to the customer on site. The converter converts the following interfaces to the indicated full duplex interfaces. The converter uses an adapter cable to simulate any interface on the data terminal equipment (DTE) and on the data circuit-terminating equipment (DCE).

## Design

The design of the NTRX34BA appears in the following figure.

**NTRX34BA parts**




**Note:** This figure is not drawn to scale.

# NTRX35AA

## Product description

The cabinetized dual shelf network (CDSN) contains two duplicated dual shelf network (DSN) modules. The cabinet is a modular, standard wired design. The cabinet contains shelves.

Connections to and from the network module connect through a bulkhead for electromagnetic interference (EMI) compliance.

The NTRX35AA functions with E-CORE.

## Parts

The NTRX35AA contains the following parts:

- NTNX27CA—Cooling unit
- NT7X34AA—Frame supervisory panel
- NT8X1101—Network module shelf assembly
- P0684448—2 in. filler plate
- P0730029—Personality plate

### Cooling unit

The NTNX27CA fan unit in the base of the cabinet cools the NTRX35AA with forced air.

### Frame supervisory panel

The NT7X34AA frame supervisory panel (FSP) contains power control and alarm circuits. The circuits provide interfaces between the power distribution center and the equipment in the CMIS.

The FSP provides a focal point for a person to monitor the NTRX35AA. The NT7X34AA provides alarms to warn of problems in the NTRX35AA. An example of a problem is a cooling unit that does not work, or operates out of range. The FSP includes a frame fail light that is mounted at the top of the front of the cabinet. The FSP has an electrostatic discharge wrist strap in the front of the cabinet.

### Dual shelf network

The NT8X1101 shelf assembly houses parts that make an NT8X11 network module (NM). As an NM, the NT8X11 NM establishes and maintains two-way, four-wire speech and signaling paths. The NT8X11 NM maintains paths between the NT8X11 NM and the peripheral modules (PM) for the duration of a call.

The NT8X11 NM is mounted as a pair, one NM for each plane, in the NTRX35AA. Two pairs can be mounted in a single , one pair for each network.

### Personality plate

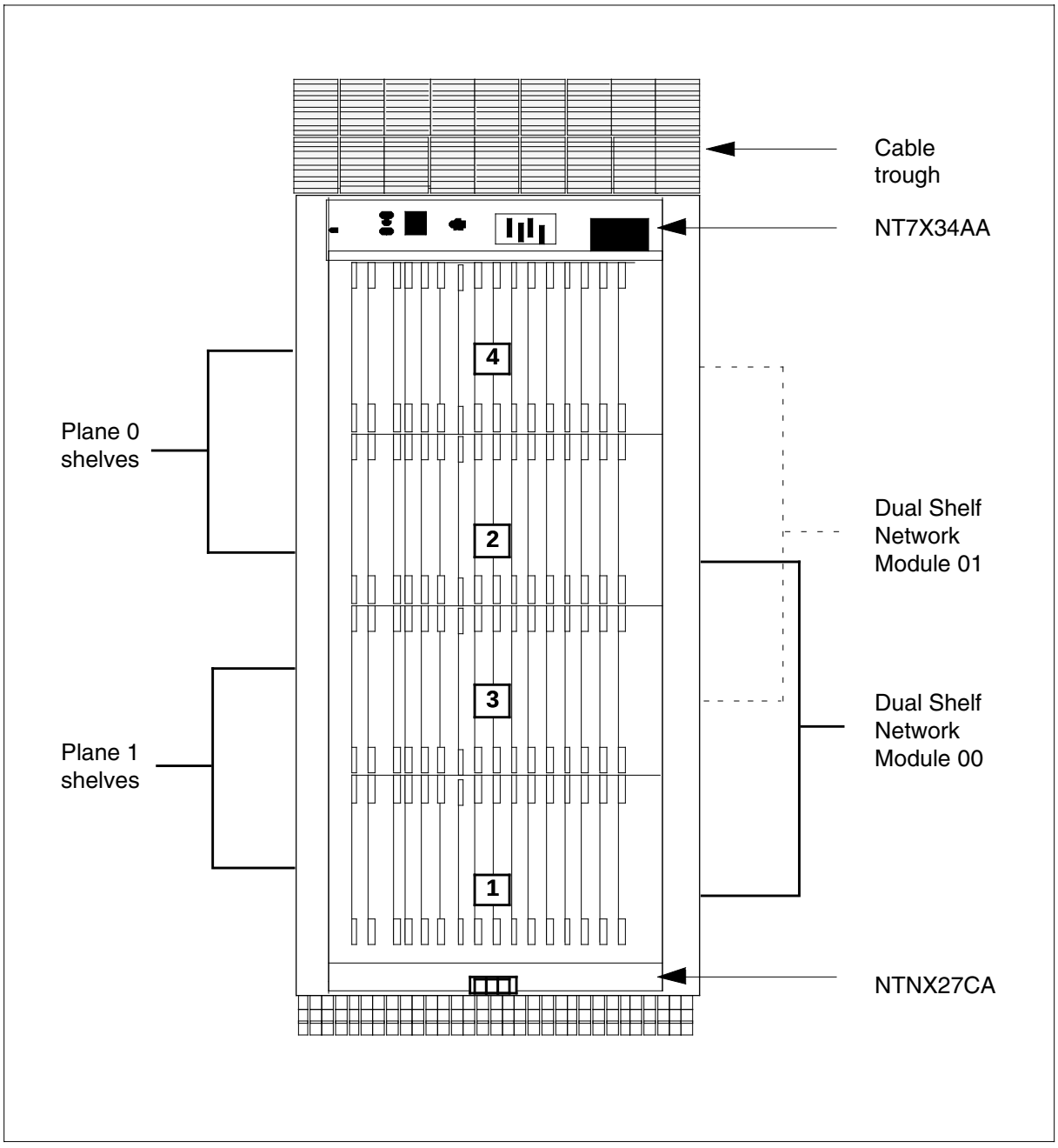
The P0730029 personality plate comes with the NTRX35AA. The personality plate fills shelf positions 47, 33, 19, and 05 when the positions are not used.

## Design

The design of the NTRX35AA appears in the following figure.

## **NTRX35AA** (end)

**NTRX35AA parts**




***Note:*** Front panels do not appear in this figure to illustrate NTRX35AA parts. This figure is not drawn to scale.

# NTRX35BA

## Product description

The cabinetized dual-shelf network (CDSN) contains two duplicated dual-shelf network (DSN) modules. The cabinet is a modular, standard wired design. The cabinet is equipped with shelves.

Connections to and from the network module connect through a bulkhead for electromagnetic interference (EMI) compliance.

The NTRX35BA functions with SuperNode.

## Parts

The NTRX35BA contains the following parts:

- NT6X02AB—filler faceplate
- NT8X1101—network module shelf assembly
- NTNX27CA—cooling unit, -48V (dc)
- NTRX40AA—modular supervisory panel, -48V or -60V (dc)
- NTRX51AA—cooling unit, -60V (dc)

### Filler faceplate

The NT6X02AB filler faceplate comes with the NTRX35BA. The faceplate fills shelf positions 47 and 19 when the NT6X02AB only uses one network module (NM).

### Cooling unit

An NTNX27CA or NTRX51AA fan unit in the base of the cabinet cools the NTRX35BA with forced air.

### Modular supervisory panel

The NTRX40AA modular supervisory panel (MSP) contains power control and alarm circuits. The circuits provide interfaces between the power distribution center and the equipment in the CDSN.

The MSP provides a focal point for a person to monitor the NTRX35BA. The NTRX40AA provides alarms to warn of problems in the NTRX35BA. An example of a problem is a cooling unit that does not work, or operates out of range. The MSP includes a frame fail light mounted at the top of the front of the cabinet. The MSP includes an electrostatic discharge wrist strap in the front of the cabinet.

## **NTRX35BA** (continued)

### Network module shelf assembly

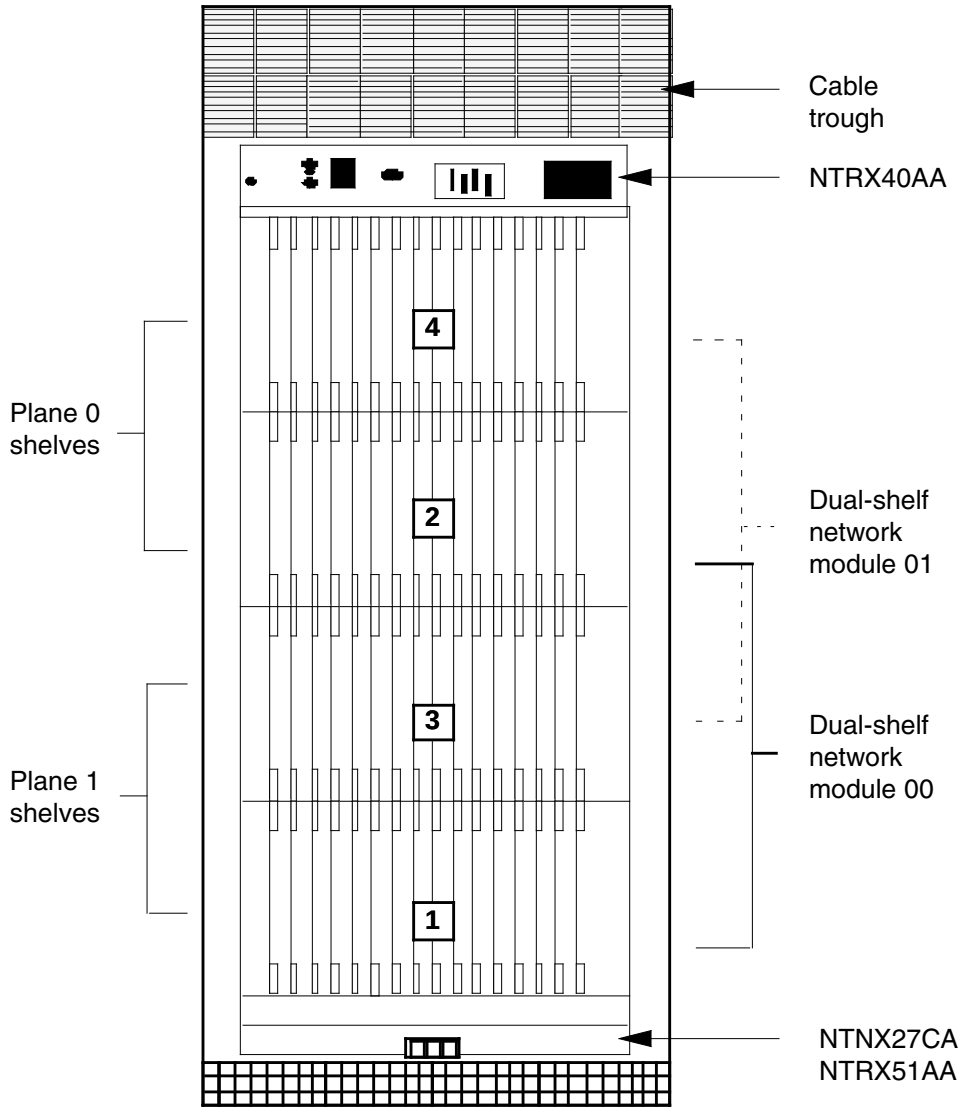
The NT8X1101 shelf assembly houses parts that make an NT8X11 NM. The NT8X11 NM establishes and maintains two-way, four-wire speech and signaling paths. The NT8X11 NM maintains paths between the NT8X11 NM and the peripheral modules (PM) for the duration of a call.

The NT8X11 NM is mounted as a pair, one NM for each plane, in the NTRX35BA. Two pairs can be mounted in a single NTRX35BA, one pair for each network.

## Design

The design of the NTRX35BA appears in the following figure.

**NTRX35BA parts**




**Note**: Front panels do not appear in this figure to illustrate the NTRX35BA parts. This figure is not drawn to scale.

# NTRX35CA

## Product description

The cabinetized dual shelf network (CDSN) contains two completely duplicated dual shelf network (DSN) modules. The cabinet is a modular, standard wired design with shelves.

All connections to and from the network module connect through a bulkhead for electromagnetic interference (EMI) compliance.

Use of the NTRX35CA can occur only with ECORE.

## Parts

The NTRX35CA contains the following parts:

- NTNX27CA—cooling unit
- NTRX40AA—modular supervisory panel
- NT8X1101—network module shelf assembly
- P0684448—2 in. (51 mm) filler plate
- P0730029—personality plate

### Cooling unit

The NTRX35CA is forced-air cooled with an NTNX27CA fan unit in the base of the cabinet.

### Modular supervisory panel

The NTRX40AA modular supervisory panel (MSP) contains power control and alarm circuits. These circuits provide interfaces between the power distribution center and the equipment in the CMIS.

The MSP also provides a focal point for a person to monitor the NTRX35CA. The NTRX50AA provides alarms to warn of problems in the NTRX35CA. Examples of these problems include a cooling unit that does not operate or that operates beyond an acceptable range. The MSP has a frame fail light at the top of the front of the cabinet. The MSP has an electrostatic discharge wrist strap in the front of the cabinet.

### Dual shelf network

The NT8X1101 shelf assembly houses the components of an NT8X11 network module (NM). The NT8X11 NM establishes and maintains two-way, four-wire speech and signaling paths. These paths are between the NT8X11 and the peripheral modules (PM) for the duration of a call.

The NT8X11 NM is mounted with the pair of the NT8X11 NM in the NTRX35CA. One NM is present for each plane. A single NTRX35CA can contain two pairs, one pair for each network.

### Personality plate

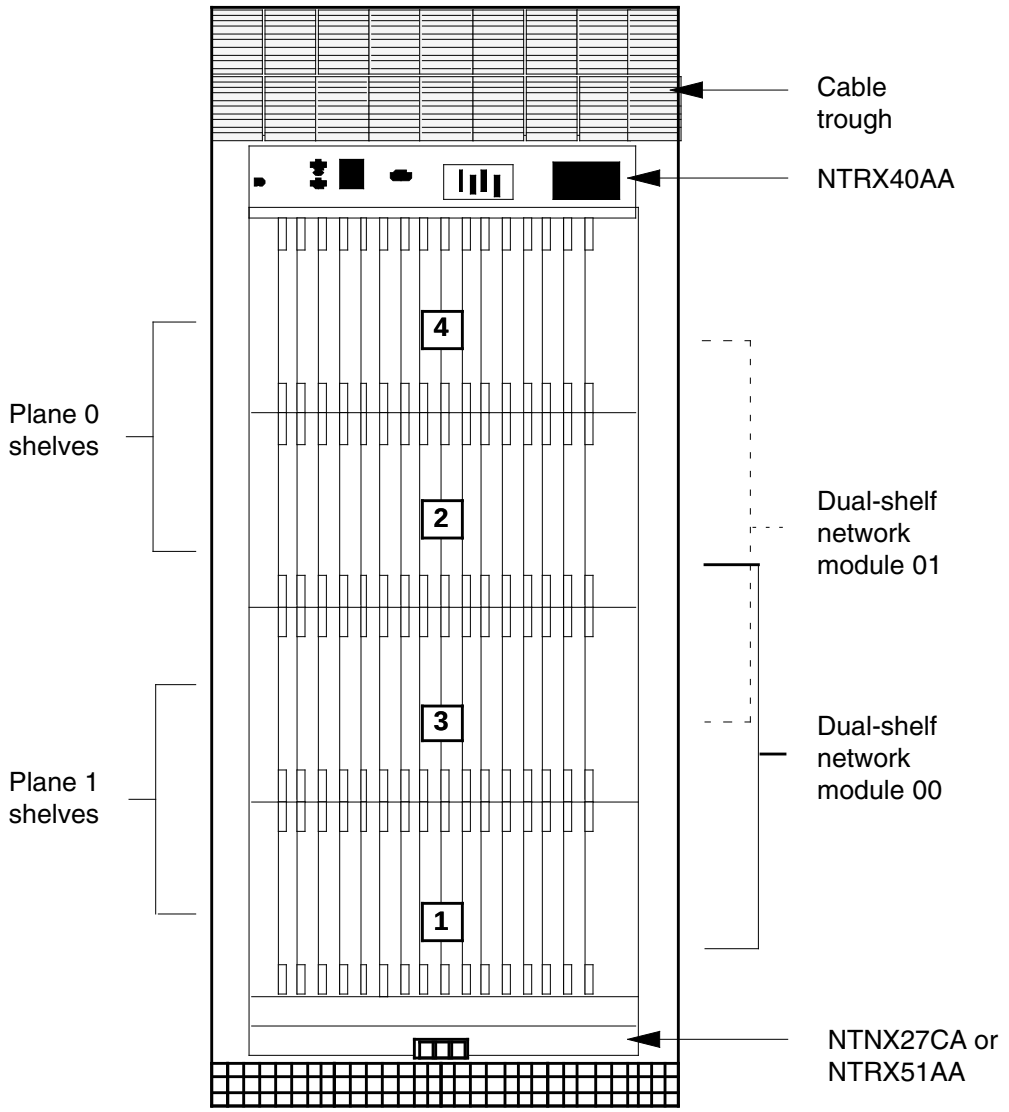
The P0730029 personality plate comes with the NTRX35CA. The P0730029 fills shelf positions 47, 33, 19, and 05 when the shelves are not in use.

## Design

The design of the NTRX35CA appears in the following figure.

# NTRX35CA (end)

**NTRX35CA parts**




**Note:** Front panels do not appear in this figure of NTRX35CA parts. This figure is not to scale.

# NTRX36AB

## Product description

The cabinetized common peripheral equipment (CCPE) is a general purpose cabinet version of the ISDN-ready NT6X01AB common peripheral controller equipment frame. The CCPE can house many different shelves that appear below under parts.

All connections to the network and DS-1 links occur through the cabinet bulkhead for electromagnetic interference (EMI) compliance.

## Parts

The CCPE contains the following parts:

- NTNX26NA—Frame supervisory panel (FSP)
- NTNX27CA—Cooling unit
- NT6X0223—ISDN-ready shelf assembly

The CCPE has a set of any one group of the following shelves. These shelves identify with the NT6X02 PECs:

- Line group controller (LGC)
- ISDN LGC (LGCI)
- Digital trunk controller (DTC)
- ISDN DTC (DTCI)
- Line trunk controller (LTC)
- Subscriber module for SLC-96 (SMS)
- Subscriber module rural (SMR)
- Subscriber module urban (SMU)
- Subscriber module-100S remote (SMS-R)

### Frame supervisory panel

The NTNX26NA CCPE FSP contains power control and alarm circuits. The circuits provide interfaces between the power distribution center and the equipment in the CCPE.

The FSP provides a focal point to allow the user to monitor the CCPE. The NTNX26NA provides alarms to warn of problems in the CCPE. Examples of these problems are a cooling unit that does not work or that operates beyond an acceptable range. The FSP has a frame fail light at the top of the front of the cabinet. The FSP has an electrostatic discharge wrist strap in the front of the cabinet.

## NTRX36AB (continued)

### ISDN-ready shelf assembly

Two adjacent shelves on positions 47 and 33 and a pair of shelves on positions 19 and 05 house each module.

### Cooling unit

Forced air from an NTNX27CA fan unit integrated in the base of the cabinet cools the CCPE.

### Cabinetized line group equipment

The cabinetized line group equipment (CLGE) defines the function of the CCPE when the cabinet must house the LGC and LGCI.

### Cabinetized digital trunk equipment

The cabinetized digital trunk equipment (CDTE) defines the function of the CCPE when the cabinet must house the DTC and DTCI. A toll office requires only CDTE.

### Cabinetized subscriber module equipment

The cabinetized subscriber module equipment (CSME) defines the function of the CCPE when the cabinet must house the SMR, SMS, SMU, or SMS-R.

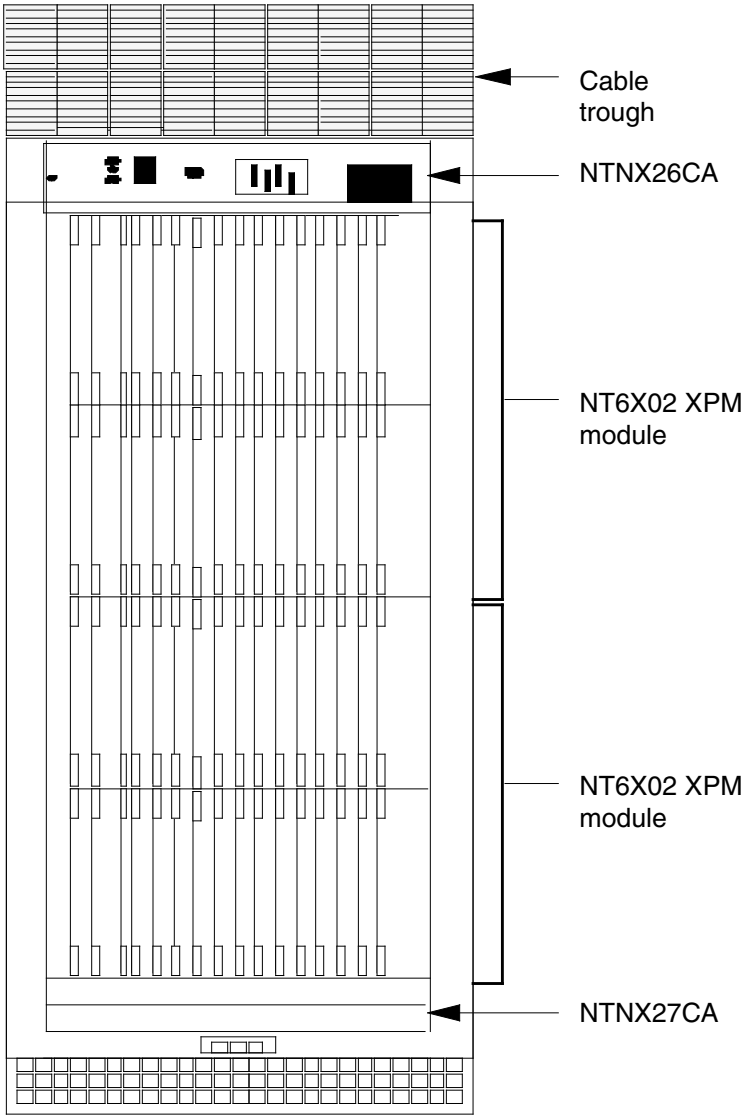
### Cabinetized line trunk equipment

The cabinetized line trunk equipment (CLTE) defines the function of the CCPE when the cabinet must house the LTC, and LTCI.

## Design

The design of the CCPE appears in the following figure.

**NTRX36AB parts**




**Note:** Front panels do not appear in this figure of NTRX36AB parts. This figure is not to scale.

# NTRX36BA

## Product description

The NTRX36BA cabinetized common peripheral equipment (CCPE) is a general purpose cabinet. The NTRX36BA CCPE is a version of the ISDN-ready NT6X01AB common peripheral controller equipment frame. The CCPE can contain many different shelves which follow under "parts".

All connections to the network and DS-1 links occur through the cabinet bulkhead for electromagnetic interference (EMI) compliance.

## Parts

The CCPE contains the following parts:

- NT6X0223—ISDN-ready shelf assembly
- NTRX40AA—modular supervisory panel (MSP)
- NTNX27CA—cooling unit

The CCPE has a set of any one group of the following shelves, all identified with NT6X02 PECs:

- line group controller (LGC)
- ISDN LGC (LGCI)
- digital trunk controller (DTC)
- ISDN DTC (DTCI)
- line trunk controller (LTC)
- subscriber module for SLC-96 (SMS)
- subscriber module rural (SMR)
- subscriber module urban (SMU)
- subscriber module-100S remote (SMS-R)

### ISDN-ready shelf assembly

Two adjacent shelves on positions 47 and 33 and a pair of shelves on positions 19 and 05 contain each module.

### Modular supervisory panel

The NTRX40AA CCPE MSP contains power control and alarm circuits. The circuits provide interfaces between the power distribution center and the equipment mounted in the CCPE.

The MSP provides a focal point to allow the user to monitor the CCPE. The NTNX26NA provides alarms to warn of problems in the CCPE. Examples of

these problems include a cooling unit that does not operate or that operates beyond an acceptable range. The MSP has a frame fail light at the top of the front of the cabinet. The MSP has an electrostatic discharge wrist strap in the front of the cabinet.

### Cooling unit

An NTNX27CA fan unit is in the base of the cabinet. Forced air from the fan unit cools the CCPE.

### Cabinetized line group equipment

The cabinetized line group equipment (CLGE) defines the function of the CCPE when the cabinet must contain the LGC and LGCI.

### Cabinetized digital trunk equipment

The cabinetized digital trunk equipment (CDTE) defines the function of the CCPE when the cabinet must contain the DTC and DTCI. A toll office requires only CDTE.

### Cabinetized subscriber module equipment

The cabinetized subscriber module equipment (CSME) defines the intended function of the CCPE when the cabinet must contain the SMR, SMS, SMU, or SMS-R.

### Cabinetized line trunk equipment

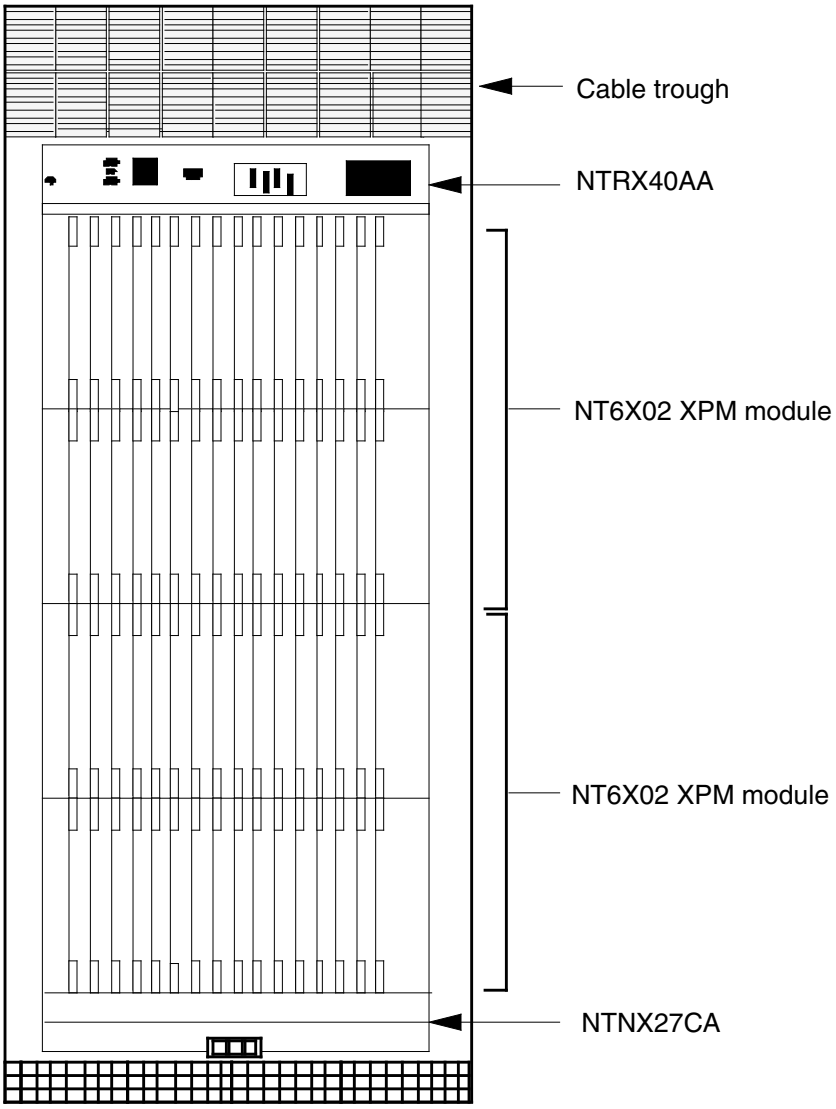
The cabinetized line trunk equipment (CLTE) defines the function of the CCPE when the cabinet must contain the LTC, and LTCI.

## Design

The design of the CCPE appears in the following figure.

# **NTRX36BA** (end)

**NTRX36BA parts**




**Note**: Front panels do not appear in this figure of NTRX36BA parts. This figure is not to scale.

# NTRX37AA

## Product description

The NTRX37AA cabinetized speech link connecting cabinet is the cabinetized version of the NT0X56AA speech link connection frame.

The NTRX37AA provides a patch cord cross-connecting facility in the speech links between the peripheral and network subsystems. The network interface ports of the peripheral equipment terminate on peripheral speech link (PSL) connecting panels. The peripheral face ports of the network modules terminate on network speech link (NSL) connecting panels. Connectorized patch cords complete the connections between ports of the two groups.

The NTRX37AA can hold a maximum of eight PSL/NSL pairs. The NTRX37AA has an EMI cabinet.

## Parts

The NTRX37AA contains the following parts:

- NT0X56BB—Network speech link panel
- NT0X56BC—Peripheral speech link panel
- NE-P4Q—Speech link patch cords (provisionable)

### Network speech link panel

The peripheral face ports of the network modules terminate on the NSL.

### Peripheral speech link panel

The network interface ports of the peripheral equipment terminate on the PSL. Assignment of PSL and NSL are fixed and alternating. All assignments are provisionable.

### Speech link patch cords

The NE-P4Q speech link patch cords connect the NSL and PSL panels. The cross connection of NT0X56BB NSLs to NT0X56BC PSLs requires different lengths of speech link patch cords. The distance between the mated panels determines the lengths of the patch cords. A list of the product engineering

## **NTRX37AA** (continued)

codes (PEC) and associated lengths of available speech link patch cords appears in table 1.

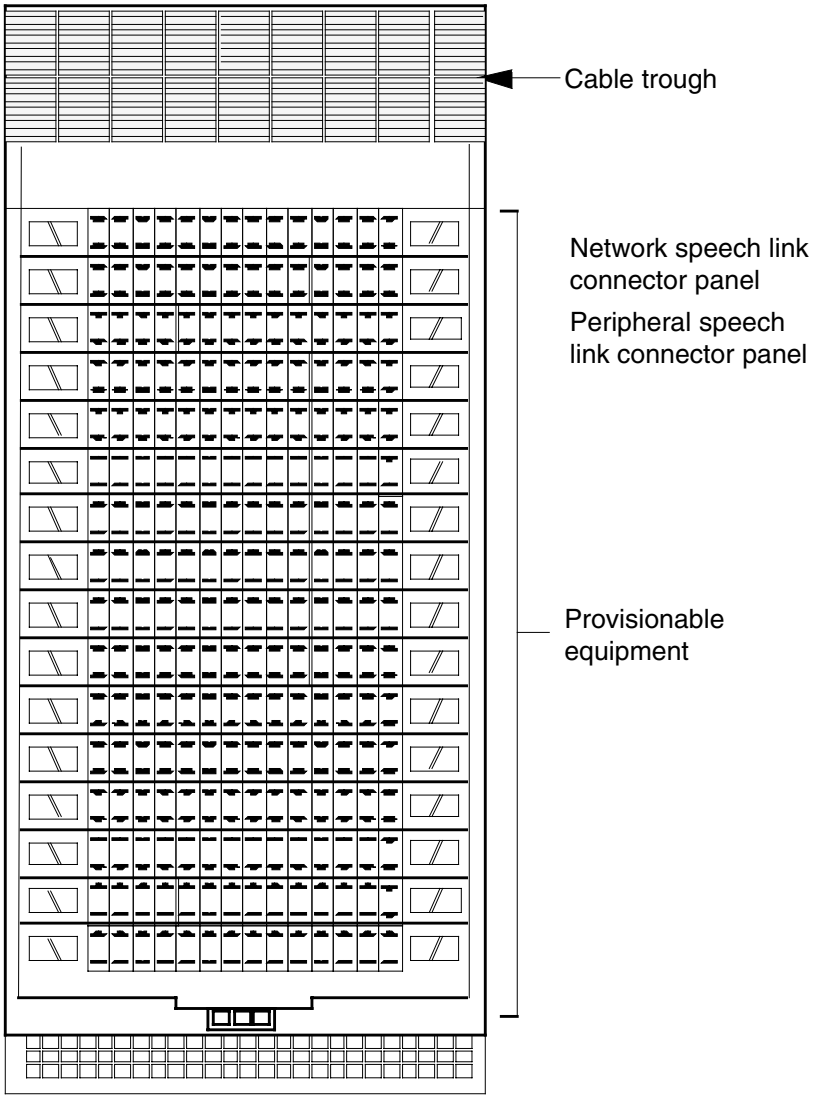
**Available speech link patch cords**

| Length | | | |
|---|---|---|---|
| **Feet** | **Meters** | **Connector color** | **Product eng. code (PEC)** |
| 2.0 | 0.61 | White | NE-P4QDK |
| 3.0 | 0.91 | Yellow | NE-P4QDL |
| 4.0 | 1.22 | Orange | NE-P4QDM |
| 5.0 | 1.52 | Red | NE-P4QDN |
| 6.5 | 1.98 | Green | NE-P4QDP |
| 8.0 | 2.44 | Brown | NE-P4QDR |
| 10.0 | 3.05 | White | NE-P4QDS |
| 15.0 | 4.57 | Yellow | NE-P4QDT |
| 20.0 | 6.1 | Orange | NE-P4QDU |
| 25.0 | 7.62 | Red | NE-P4QDW |
| 30.0 | 9.14 | Green | NE-P4QDX |

## Design

The design of the NTRX37AA appears in the following figure.

**NTRX37AA parts**




**Note:** Front panels do not appear in this figure of NTRX37CA parts. This figure is not to scale.

# NTRX37BA

## Product description

The NTRX37BA cabinetized speech link connecting cabinet is the cabinetized version of the NT0X56AA speech link connection frame.

The NTRX37BA provides a patch cord cross-connect facility in the speech links between the peripheral and network subsystems. The network interface ports of the peripheral equipment terminate on peripheral speech link (PSL) connecting panels. The peripheral face ports of the network modules terminate on network speech link (NSL) connecting panels. Connectorized patch cords complete the connections between ports of the two groups.

The NTRX37BA can hold a maximum of eight PSL/NSL pairs for a total capacity of 16 panels. The NTRX37BA has an electromagnetic interference (EMI) cabinet.

The NTRX37BA has designated fixed positions for the NSL and PSL panels. The panels are mounted at the top of the NTRX37BA and down. For the NT0X56BB NSL, the mounting positions are 58, 51, 44, 37, 30, 23, 16, and 09. For the NT0X56BC PSL, the mounting positions are 54, 47, 40, 33, 26, 19, 12, and 05.

## Parts

The NTRX37BA contains the following components:

- NE-P4Q—speech link patch cords (provisionable)
- NT0X56BB—network speech link panel
- NT0X56BC—peripheral speech link panel
- P0715616—filler faceplate (blank)
- P0730031—filler faceplate (right side)
- P0730032—filler faceplate (left side)

### Speech link patch cords

The NE-P4Q speech link patch cords connect the NSL and PSL panels. The cross connection of NT0X56BB NSLs to NT0X56BC PSLs require speech link patch cords of different lengths. The distance between the mated panels determines the patch cord lengths. Table 1 provides a list of the PECs and associated lengths of available speech link patch cords.

### Network speech link panel

The peripheral face ports of the network modules terminate on the NSL. Each network in a cabinetized double shelf network (CDSN) requires two

NT0X56BB NSL panels. A CDSN has two networks. This CDSN requires four panels.

### Peripheral speech link panel

The network interface ports of the peripheral equipment terminate on the PSL. Assignments of PSL and NSL are fixed and alternating. All parts are provisionable.

The following equipment require two NT0X56BC PSL panels. One panel is for each plane.

- every eight units of peripheral type equipment in the trunk module equipment cabinet (CTME)
- every four units of peripheral type equipment in the following:
  - digital trunk equipment cabinet (CDTE)
  - line group equipment cabinet (CLGE)
  - subscriber module equipment cabinet (CSME)
  - line trunk equipment cabinet (CLTE)

### Filler faceplate (blank)

The P0715616 filler faceplate (blank) covers shelf positions 47, 33, 19, and 05 when the positions are not in use. A list of the PECs and required number of filler faceplates appear in the following tables.

### Filler faceplate (left side)

The P0730032 filler faceplate (left side) covers shelf positions 47, 33, 19, and 05 when the positions are not in use. A list of the PECs and required number of filler faceplates appear in the following tables.

### Filler faceplate (right side)

The P0730031 filler faceplate (right side) covers shelf positions 47, 33, 19, and 05 when the positions are not in use. A list of the PECs and required number of filler faceplates appear in the following tables.

**Available juncture patch cords (Sheet 1 of 2)**

| Length | | | |
|---|---|---|---|
| **Meters** | **Feet** | **Connector color** | **PEC** |
| 0.61 | 2.0 | White | NE-P4QDK |
| 0.91 | 3.0 | Yellow | NE-P4QDL |

## **NTRX37BA** (continued)

**Available juncture patch cords (Sheet 2 of 2)**

| Length | | | |
|---|---|---|---|
| **Meters** | **Feet** | **Connector color** | **PEC** |
| 1.22 | 4.0 | Orange | NE-P4QDM |
| 1.52 | 5.0 | Red | NE-P4QDN |
| 1.98 | 6.5 | Green | NE-P4QDP |
| 2.44 | 8.0 | Brown | NE-P4QDR |
| 3.05 | 10.0 | White | NE-P4QDS |
| 4.57 | 15.0 | Yellow | NE-P4QDT |
| 6.10 | 20.0 | Orange | NE-P4QDU |
| 7.62 | 25.0 | Red | NE-P4QDW |
| 9.14 | 30.0 | Green | NE-P4QDX |

**Available filler faceplates (Sheet 1 of 2)**

| No. of NSL and PSL panels | Required no. of P0715616 | Required no. of P0730031 | Required no of P0730032 |
|---|---|---|---|
| 1 | 6 | 1 | 1 |
| 2 | 6 | 1 | 1 |
| 3 | 6 | 1 | 1 |
| 4 | 6 | 1 | 1 |
| 5 | 4 | 2 | 2 |
| 6 | 4 | 2 | 2 |
| 7 | 4 | 2 | 2 |
| 8 | 4 | 2 | 2 |
| 9 | 2 | 3 | 3 |
| 10 | 2 | 3 | 3 |
| 11 | 2 | 3 | 3 |
| 12 | 2 | 3 | 3 |

**Available filler faceplates (Sheet 2 of 2)**

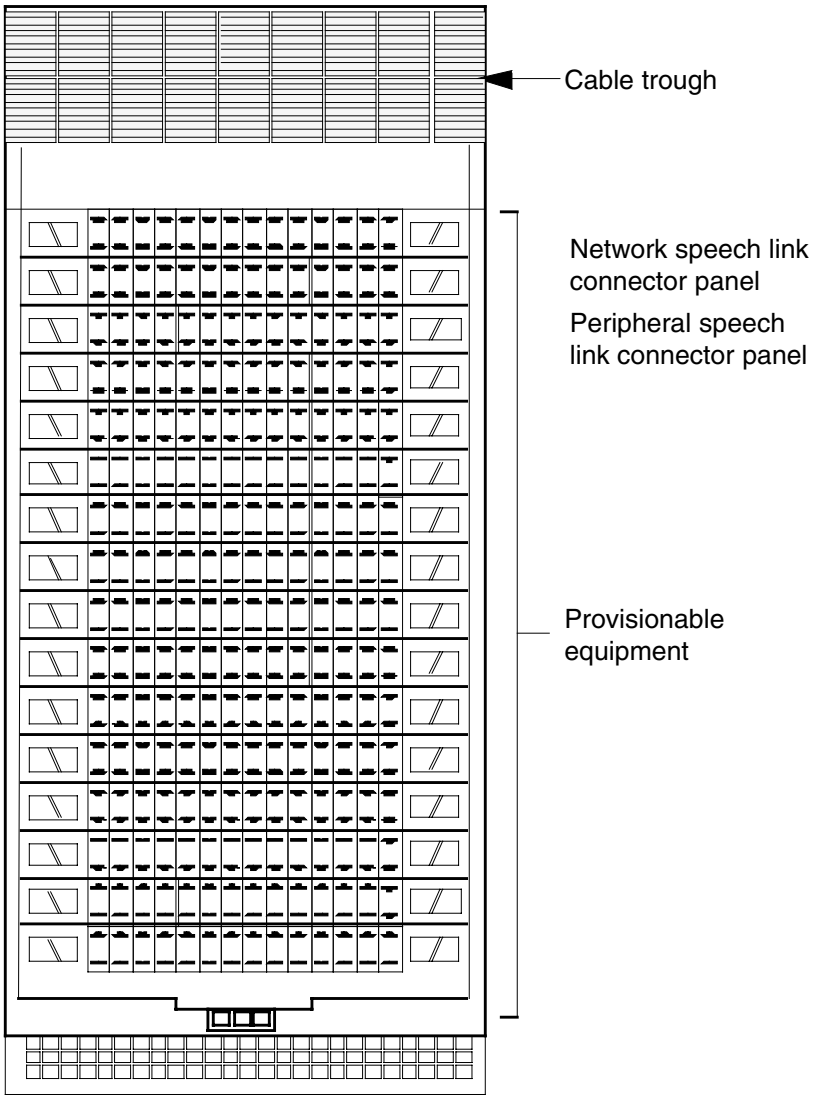
| No. of NSL and PSL panels | Required no. of P0715616 | Required no. of P0730031 | Required no of P0730032 |
|---|---|---|---|
| 13 | 0 | 4 | 4 |
| 14 | 0 | 4 | 4 |
| 15 | 0 | 4 | 4 |
| 16 | 0 | 4 | 4 |

## Design

The design of the NTRX37BA appears in the following figure.

# **NTRX37BA** (end)

**NTRX37BA parts**




**Note:** Front panels do not appear in this figure of NTRX37BA parts. This figure is not to scale.

## Production description

The NTRX37CA cabinetized speech link connecting cabinet is the cabinetized version of the NT0X56AA speech link connection frame.

The NTRX37CA provides a patch cord cross-connect facility in the speech links between the peripheral and network subsystems. The network interface ports of the peripheral equipment terminate on peripheral speech link (PSL) connecting panels. The peripheral face ports of the network modules terminate on network speech link (NSL) connecting panels. Connectorized patch cords complete the interconnections between ports of the two groups.

The NTRX37CA can hold a maximimum of eight PSL/NSL pairs. The NTRX37CA has an EMI cabinet.

## Parts

The NTRX37CA has the following parts:

- NT0X56BB—network speech link panel
- NT0X56BC—peripheral speech link panel
- NE-P4Q—speech link patch cords (provisionable)

### Network speech link panel

The peripheral face ports of the network modules terminate on the NSL.

### Peripheral speech link panel

The network interface ports of the peripheral equipment terminate on the PSL. Assignments of PSL and NSL are fixed and alternating. All assignments are provisionable.

### Speech link patch cords

The NE-P4Q speech link patch cords connect the NSL and PSL panels. The cross connections of NT0X56BB NSLs to NT0X56BC PSLs require speech link patch cords of different lengths. The distance between the mated panels

## NTRX37CA (continued)

determines the patch cord lengths. A list of the PECs and associated lengths of available speech link patch cords appears in the following table.

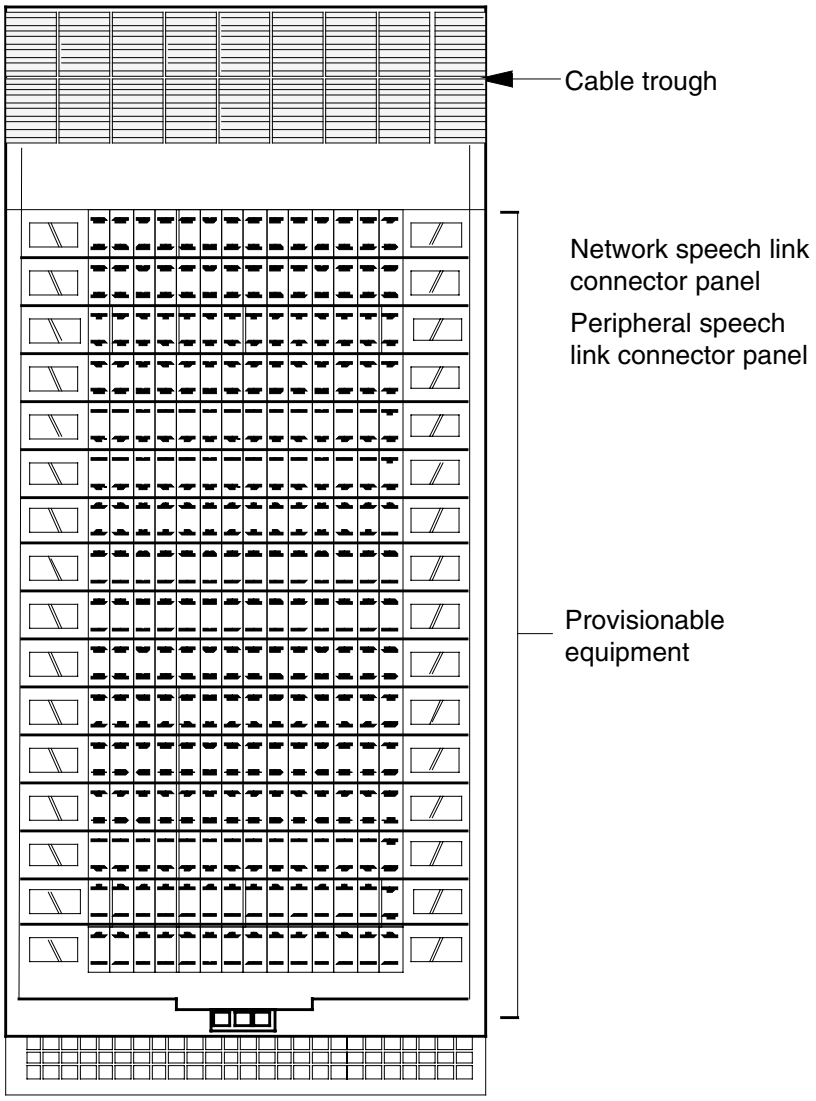
**Available speech link patch cords**

| Length | | | |
|---|---|---|---|
| **Meters** | **Feet** | **Connector color** | **PEC** |
| 0.61 | 2.0 | White | NE-P4QDK |
| 0.91 | 3.0 | Yellow | NE-P4QDL |
| 1.22 | 4.0 | Orange | NE-P4QDM |
| 1.52 | 5.0 | Red | NE-P4QDN |
| 1.98 | 6.5 | Green | NE-P4QDP |
| 2.44 | 8.0 | Brown | NE-P4QDR |
| 3.05 | 10.0 | White | NE-P4QDS |
| 4.57 | 15.0 | Yellow | NE-P4QDT |
| 6.1 | 20.0 | Orange | NE-P4QDU |
| 7.62 | 20.0 | Red | NE-P4QDW |
| 9.14 | 30.0 | Green | NE-P4QDX |

## Design

The design of the NTRX37CA appears in the following figure.

**NTRX37CA parts**




**Note:** Front panels do not appear in this figure of NTRX37AA parts. This figure is not to scale.

# NTRX38AA

## Product description

The cabinetized digital network interconnect cabinet (CDNI) is the cabinetized version of the NT0X18AA/CB digital network interconnect frame.

The NTRX38AA provides a junctoring facility to interconnect the junctor face ports of network modules in a specified plane. Juncture patch cords perform the junctoring function. The patch cords are mounted behind NT0X18DD digital network junctor (NJC) connecting panels.

Bulkhead filtering provides electromagnetic interference compliance.

## Parts

The NTRX38AA contains NT0X18DD network juncture connecting panels and NE-P4Q juncture patch cords. The patch cords are provisionable.

### Network juncture connecting panels

The NJCs are panels in the NTRX38AA frame. These panels accept patch cords and allow the arrangement of junctor patterns.

### Juncture patch cords

The juncture patch cords are interface equipment. This equipment is at the end of a interoffice circuit or intraoffice trunk that provides circuit and signaling compatibility. The distance between the mated panels determine the length of the required patch cords. A list of the product engineering codes (PEC) and lengths of available juncture patch cords appears in the following table.

**Available juncture patch cords (Sheet 1 of 2)**

| Length | | | |
|---|---|---|---|
| **Feet** | **Meters** | **Connector color** | **Product eng.code (PEC)** |
| 2.0 | 0.61 | Black-White | NE-P4QDY |
| 3.0 | 0.91 | Black-Yellow | NE-P4QEA |
| 4.0 | 1.22 | Black-Orange | NE-P4QEB |
| 5.0 | 1.52 | Black-Red | NE-P4QEC |
| 6.5 | 1.98 | Black-Green | NE-P4QED |
| 8.0 | 2.44 | Black-Brown | NE-P4QEE |

**Available juncture patch cords (Sheet 2 of 2)**

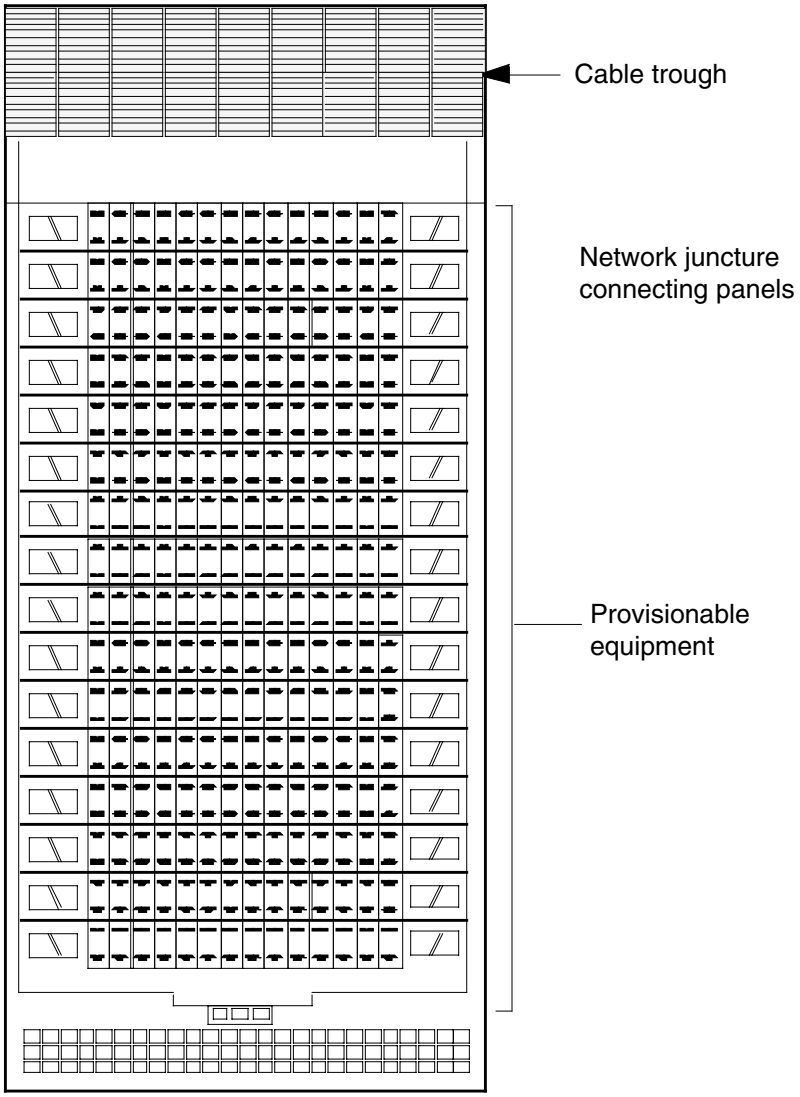
| Length | | | |
|---|---|---|---|
| **Feet** | **Meters** | **Connector color** | **Product eng.code (PEC)** |
| 10.0 | 3.05 | Black-White | NE-P4QEF |
| 15.0 | 4.57 | Black-Yellow | NE-P4QEG |

## Design

The design of the NTRX38AA parts appears in the following figure.

# **NTRX38AA** (end)

### NTRX38AA parts




**Note:** Front panels do not appear in this figure of NTRX38AA parts. This figure is not to scale.

# NTRX38BA

## Product description

The cabinetized digital network interconnect cabinet (CDNI) is the cabinetized version of the NT0X18AA, CB digital network interconnect frame.

The NTRX38BA provides a junctoring facility to interconnect the junctor face ports of network modules in a specified plane. Juncture patch cords perform the junctoring function. The patch cords are behind the NT0X18DD digital network junctor (NJC) connecting panels.

Bulkhead filtering provides electromagnetic interference (EMI) compliance.

## Parts

The NTRX38BA contains the following parts:

- NE-P4Q—juncture patch cords
- NT0X18DD—network juncture connecting panel
- P0715596—filler faceplate (right side)
- P0715616—filler faceplate (blank)
- P0730030—filler faceplate (left side)

### Juncture patch cords

Juncture patch cords are interface equipment. This equipment is at the end of a interoffice circuit or intraoffice trunk that provides circuit and signaling compatibility. The distance between the mated panels determines the length of the required juncture patch cords. A list of the PECs and lengths of available juncture patch cords appears in the table on page -116.

### Network juncture connecting panels

The NJCs are panels in the NTRX38BA frame that accept patch cords. The panels allow the organization of junctor patterns. A maximum of 16 NJC panels are provisionable.

### Filler faceplate (right side)

The P0715596 filler faceplate on the right side covers shelf positions 47, 33, 19, and 05 when the positions are not in use. A list of the PECs and the required number of filler faceplates appears in the table on page -116.

### Filler faceplate (blank)

The P0715616 filler faceplate that is blank covers shelf positions 47, 33, 19, and 05 when the positions are not in use. A list of the PECs and the required number of filler faceplates appears in the table on page -116.

## NTRX38BA (continued)

### Filler faceplate (left side)

The P0730030 filler faceplate on the left side covers shelf positions 47, 33, 19, and 05 when the positions are not in use. A list of the PECs and corresponding required number of filler faceplates appears in the table on page -116.

**Available juncture path cords**

| Length | | | |
|---|---|---|---|
| **Meters** | **Feet** | **Connector color** | **PEC** |
| 0.61 | 2.0 | Black-white | NE-P4QDY |
| 0.91 | 3.0 | Black-yellow | NE-P4QEA |
| 1.22 | 4.0 | Black-orange | NE-P4QEB |
| 1.52 | 5.0 | Black-red | NE-P4QEC |
| 1.98 | 6.5 | Black-green | NE-P4QED |
| 2.44 | 8.0 | Black-brown | NE-P4QEE |
| 3.05 | 10.0 | Black-white | NE-P4QEF |
| 4.57 | 15.0 | Black-yellow | NE-P4QEG |

**Available filler faceplates (Sheet 1 of 2)**

| No. of NJC panels | Required no. of P0715596 | Required no. of P0730030 | Required no. of P0715616 |
|---|---|---|---|
| 1 | 1 | 1 | 6 |
| 2 | 1 | 1 | 6 |
| 3 | 1 | 1 | 6 |
| 4 | 1 | 1 | 6 |
| 5 | 2 | 2 | 4 |
| 6 | 2 | 2 | 4 |
| 7 | 2 | 2 | 4 |
| 8 | 2 | 2 | 4 |
| 9 | 3 | 3 | 2 |
| 10 | 3 | 3 | 2 |

**Available filler faceplates (Sheet 2 of 2)**

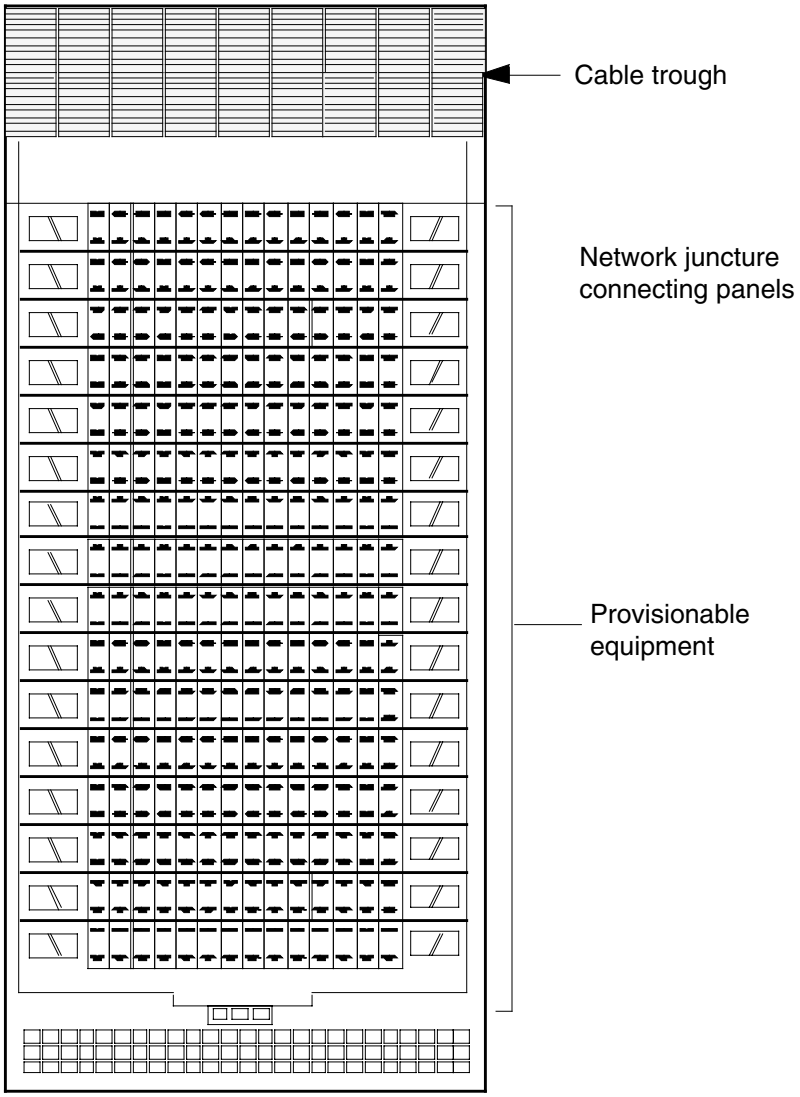
| No. of NJC panels | Required no. of P0715596 | Required no. of P0730030 | Required no. of P0715616 |
|---|---|---|---|
| 11 | 3 | 3 | 2 |
| 12 | 3 | 3 | 2 |
| 131 | 4 | 4 | 0 |
| 14 | 4 | 4 | 0 |
| 15 | 4 | 4 | 0 |
| 16 | 4 | 4 | 0 |

## Design

The design of the NTRX38BA appears in the following figure.

# **NTRX38BA** (end)

### NTRX38BA parts




**Note:** Front panels do not appear in this figure of NTRX38BA parts. This figure is not to scale.

# NTRX38CA

## Product description

The cabinetized digital network interconnect cabinet (CDNI) is the cabinetized version of the NT0X18AA/CB digital network interconnect frame.

The NTRX38CA provides a junctoring facility to interconnect the junctor face ports of network modules in a specified plane. Juncture patch cords perform the junctoring function. The patch cords are mounted behind NT0X18DD digital network junctor (NJC) connecting panels.

Bulkhead filtering provides electromagnetic interference (EMI) compliance.

## Parts

The NTRX38CA contains NT0X18DD network juncture connecting panels and NE-P4Q juncture patch cords. The patch cords are provisionable.

### Network juncture connecting panels

The NJCs are panels in the NTRX38CA frame that accept patch cords. This condition allows the arrangement of junctor patterns.

### Juncture patch cords

Juncture patch cords are the interface equipment. This interface equipment is at the end of a interoffice circuit or intraoffice trunk that provides circuit and signaling compatibility. The distance between the mated panels determine the required length of juncture patch cords. A list of the PECs and lengths of available juncture patch cords appears in the following table.

**Available juncture link patch cords (Sheet 1 of 2)**

| Length | | | |
|---|---|---|---|
| **Meters** | **Feet** | **Connector color** | **PEC** |
| 0.61 | 2.0 | Black-white | NE-P4QDY |
| 0.91 | 3.0 | Black-yellow | NE-P4QEA |
| 1.22 | 4.0 | Black-orange | NE-P4QEB |
| 1.52 | 5.0 | Black-red | NE-P4QEC |
| 1.98 | 6.5 | Black-green | NE-P4QED |
| 2.44 | 8.0 | Black-brown | NE-P4QEE |

## **NTRX38CA** (continued)

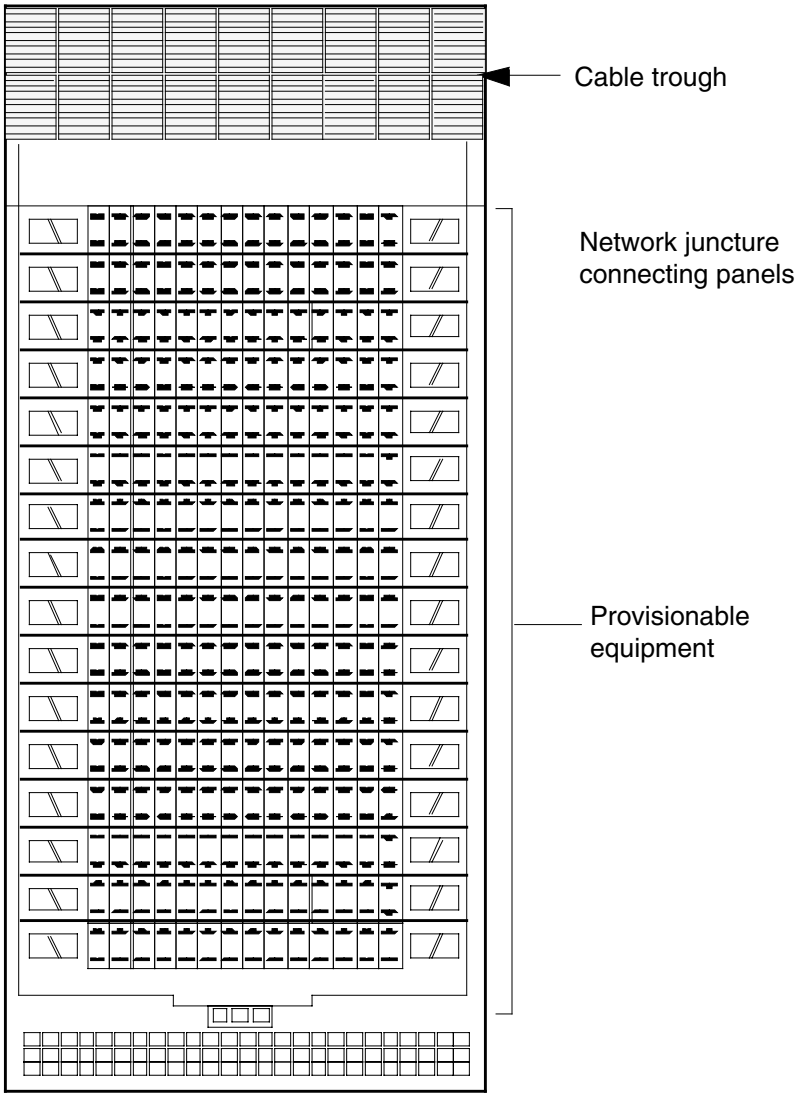
**Available juncture link patch cords (Sheet 2 of 2)**

| **Length** | | | |
|---|---|---|---|
| **Meters** | **Feet** | **Connector color** | **PEC** |
| 3.05 | 10.0 | Black-white | NE-P4QEF |
| 4.57 | 15.0 | Black-yellow | NE-P4QEG |

## Design

The design of the NTRX38CA appears in the following figure.

**NTRX38CA parts**




**Note:** Front panels do not appear in this figure of NTRX38CA parts. This figure is not to scale.

# NTRX40AA

## Product description

The NTRX40AA modular supervisory panel (MSP) is a part of the C28 cabinets. The MSP provides power distribution and protection, alarm indication and control and basic maintenance functions. The MSP includes the following:

- fan-fail and frame-fail indicator
- fuse-fail alarm output
- front and rear alarm battery supply (ABS) test jacks
- four front-panel services jacks

The service jacks are two telephone pairs **TEL-A** and **TEL-B** and two data pairs **DATA-A** and **DATA-B**.

The panel has a maximum of two talk battery filters, ten circuit breakers, eight fuses and other plug-in cards. The MSP is in shelf position 61, in a cabinetized power distribution center (CPDC) in shelf position 63 and in a frame in shelf position 46.

## Parts

The NTRX40AA contains the following provisionable parts:

- NTRX41AA—alarm card
- NTRX42AA—breaker card (10 A)
- NTRX42BA—breaker card (15 A)
- NTRX42CA—breaker card (20 A)
- NTRX43AA—fuse card
- NTRX43BA—thermal breaker card
- NTRX44AA—talk battery filter (TBF) card
- NTRX53AA—C-feed card
- NTRX54AA—fan power control & filter (FPC/F) card
- NTRX54BA—fan power control (FPC) card
- Front panel controls and indicators
- Mechanical interlock

The NTRX40AA contains the following CPDC provsionable parts:

- NTRX41BA—power alarm circuit card
  - — NTRX4105—power alarm backpanel printed circuit pack (PCP)
- NTRX41DA—enhanced alarm system (EAS) kit
  - — NTRX41CA—EAS circuit card
- NTRX41EA—alarm battery supply (ABS) distribution card

## Provisionable parts

### Alarm card

The NTRX41AA alarm card monitors and reports alarms. This card operates with an input voltage of -48 or -60V.

The user installs the alarm card in slot position five. The alarm occupies two card positions in the MSP. The alarm card interfaces with the alarm backplane with the 4x30 NORCON connector. The polarizing key setting must be at C (top) and 3 (bottom).

The NTRX41AA alarm card monitors and detects the following types of faults:

- converter faults
- thermal breaker failures
- fan failure on one or two cooling units
- failures in the talk battery modules
- inverter failure in the cabinet
- cabinet temperature that exceeds limits

If one of the first five conditions occur, the NTRX41AA raises alarms and sends signals to the office alarm unit (OAU). The NTRX41AA also provides maintenance facilities. The maintenance facilities include telephone, data, and alarm battery supply (ABS) jacks.

### Breaker cards

The NTRX42AA, -BA, -CA breaker cards contain two circuit breakers of -48 or -60V. Each circuit breaker provides two 10A, 15A or 20A power feeds. A maximum of ten breaker cards can be provisioned in the MSP.

***Note:*** The maximum combined number of breaker and fuse/thermal breaker cards is 13.

## **NTRX40AA** (continued)

The user installs the breaker card next to the fuse or thermal breaker card. The breaker card occupies one card position in the MSP. The breaker card accommodates two sealed breakers of the same amperage. The breaker card is completely connectorized and provides power inputs with a 6.35 mm (0.25 in.) quick connect plug for each breaker. The breaker card provides power/alarm output with a 24-pin Positronics power-lok connector.

The breaker card receives two input feeds from the CPDC. The breaker card allows the two front-mounted breakers of the breaker card to limit the input current. The breakers are also equipped with automatic recovery from low battery and the standard DMS converter interface. This condition allows the breakers to monitor converters.

The functions of the breaker are as follows:

- to monitor and detect converter failures
- to trip breakers when over-current conditions exist
- to trip breakers on converter failure
- to provide termination points for CPDC feeds
- to provide battery feed samples for the alarm module
- to respond to automatic recovery from low battery (ARLB) conditions

### Fuse circuit card

The NTRX43AA fuse card provides a maximum of eight current-limited feed outputs at an available fuse rating (0.18 to 5A). The fuse card provides one alarm output. This card operates with an input battery voltage of -48 or -60V.

***Note:*** The QFF fuses are not supplied with this card. The QFF fuses are provisioned at the cabinet level.

The fuse card installation starts in slot position seven. The fuse card occupies one card position in the MSP.

***Note:*** The MSP requires a minimum of one fuse card.

The card is completely connectorized. The card provides separate power input ports with two 6.35 mm (0.25 in.) quick connect plugs for two groups of fuses each. The card provides an 18-pin Positronics power-lok output connector. The card provides alarm output with a separate 2-pin Molex connector.

The NTRX43AA provides the following functions:

- acts as termination point for CPDC feeds
- supplies eight current-limited outputs for miscellaneous circuits
- reports fuse and breaker failures to the alarm module

### Thermal breaker card

The NTRX43BA thermal breaker card provides a maximum of eight current-limited feed outputs at an available fuse rating (0.18 to 5A). This card provides one alarm output. This card operates with an input battery voltage of -48 or -60V.

***Note:*** The breakers are not supplied with this card. The breakers are provisioned at the cabinet level.

The thermal breaker card occupies one card position in the MSP. The card is completely connectorized. The card provides separate power input ports with two 6.35 mm (0.25 in.) quick connect plugs for two groups of four breakers each. The card provides an 18-pin Positronics power-lok output connector. The card provides alarm output with a separate 2-pin Molex connector.

### Talk battery filter card

The NTRX44AA talk battery filter card provides a filtered power feed of a maximum of 20A. This card also provides inrush current protection (soft-start) to prevent CPDC breaker trips. The NTRX44AA operates with an input battery voltage of -48 or -60V.

Installation of the TBF card in slot position one or three occurs. The TBF occupies two card positions in the MSP. The card is completely connectorized. The card provides power input and output with two 6.35 mm (0.25 in.) quick connect plugs. The card provides alarm output with 2-pin Molex connectors. The alarm output can be fail and loss-of-power.

The NTRX44AA provides the following functions:

- termination point for CPDC feeds
- filtered battery feed through connector interfaces
- soft-start a current-limiting startup circuit provides to prevent CPDC breaker trip
- two fail alarms

### C-feed circuit card

The NTRX53AA C-feed card receives A-feed and B-feed inputs from the CPDC. This card provides a combined, filtered C-feeds of a maximum 10A

## **NTRX40AA** (continued)

each and an alarm output. This card operates with an input battery voltage of -48 or -60V.

> ***Note:*** This card is not recommended for new applications. This card supports current system requirements only.

Installation of the C-feed card occurs next to the breaker card. The C-feed card occupies two card positions in the MSP. The card is completely connectorized. The card provides A-feed and B-feed input with two 6.35 mm (0.25 in.) quick connect plugs. The card provides power/alarm output with an 18-pin Positronics power-lock connector.

### Fan power control and filter card

The NTRX54AA fan power control and filter card (FPC/F) receives A-feed and B-feed inputs from the CPDC. This card provides a combined, filtered, voltage and current-limited C-feed for 48V (dc) fans and an alarm output. This card operates with an input battery voltage of -48 or -60V.

The user installs the FPC/F card in slot position 19. The FAC/F card occupies two card positions in the MSP. This card is completely connectorized. This card provides A-feed and B-feed input with two 6.35 mm (0.25 in.) quick connect plugs. This card provides power/alarm output with an 18-pin Positronics power-lok connector.

The FPC/F card provides a nominal regulated 48V for fan operation. This card filters the noise the fans generate. The following are features of the card:

- 48 and 60V compatible
- dual battery feeds for redundancy
- regulated output voltage
- battery noise filter
- current limiter
- continuous fan power when converter failure occurs
- continuous fan when under-voltage or over-voltage occurs
- fail safe over-voltage
- alarm indication with alarm signal and LED when an over-voltage, under-voltage, fuse failure or converter failure occurs

### Fan power control card

The NTRX54BA fan power control card (FPC) receives A-feed and B-feed inputs from the CPDC. This card provides a combined C-feed for the 48V (dc)

fans and an alarm output. This card operates with an input battery voltage of -48 or -60V.

Installation of the FPC card occurs in slot position 19. The FPC card occupies two card positions in the MSP. This card is completely connectorized. This card provides A-feed and B-feed input with two 6.35 mm (0.25 in.) quick connect plugs. This card provides power/alarm output withan 18-pin Positronics power-lok connector.

The FPC provides a nominal regulated 48 V for fan operation. The following are features of this card:

- fuse failure alarm
- redundant feed operation

## CPDC-specific parts

### Power alarm circuit card

The NTRX41BA power alarm card monitors and reports alarms on CPDC equipment. This equipment includes a maximum of four breaker panels, one inverter and one breaker. This breaker supplies ABS to the lineup. This card is in use with the NTRX41AA alarm circuit card. This card operates with an input battery voltage of -48 or -60V.

The user installs the power card alarm in slot position seven. The power card alarm occupies two card positions in the MSP. This card interfaces with the NTRX4105 power alarm backpanel printed circuit pack (PCP) with a 4x30 NORCON connector.

### Power alarm backpanel PCP

The NTRX4105 power alarm backpanel PCP provides the interface between the NTRX41BA power alarm card and all the CPDC MSP cards. This backpanel also provides an interface to connect the alarm circuits from the lineup to the OAU. The lineup is CPDC, ABS, EAS

### Enhanced alarm system kit

A maximum of four NTRX41DA enhanced alarm system kits can be provisioned for the CPDC MSP. Each kit includes one NTRX41CA EAS card, one NTRX4067 EAS cable assembly and one MSP card label.

### Enhanced alarm system card

The NTRX41CA EAS card monitors one A-feed and one B-feed at the CPDC. This new feature detects total feed loss and generates an alarm at the maintenance trunk module (MTM). This feature uses the NTRX41BA power alarm card to generate this alarm. This card operates with an input battery voltage of -48 or -60V.

## **NTRX40AA** (continued)

The user installs the EAS card in adjacent slots that start at slot position 15. The EAS card occupies one card position in the MSP. This card is completely connectorized. This card provides A-feed and B-feed input with two power 6.35 mm (0.25 in.) quick connect plugs. This card provides alarm input/output with three 2-pin Molex connectors.

### Alarm battery supply distribution card

The NTRX41EA alarm battery supply distribution card provides ABS input termination (6 AWG maximum) and (fused) output distribution at the CPDC. This card operates with an input battery voltage of -48 or -60V.

Installation of the ABS card occurs behind slot positions 10 and 11 on the rear of the MSP. This card requires four card positions: two to mount the card and two (one on each side) for access. The card has a transparent safety cover.

### Front panel controls and indicators

The front panel includes circuit breakers and the associated LEDs, fuses, test jacks and the **Fan Fail** and **Frame Fail** LEDs. The user can operate the circuit breakers manually. A problem in the associated power converter can also trip the circuit breaker. An associated LED is above each circuit breaker. The fuses have a mechanical indicator that is visible when a guard contact closes.

### Mechanical interlock

The MSP also includes a mechanical interlock that allows access to only two of the circuit breakers at a time. The mechanical interlock is a small cover that slides. This interlock makes sure circuit breakers cannot be accidentally tripped.

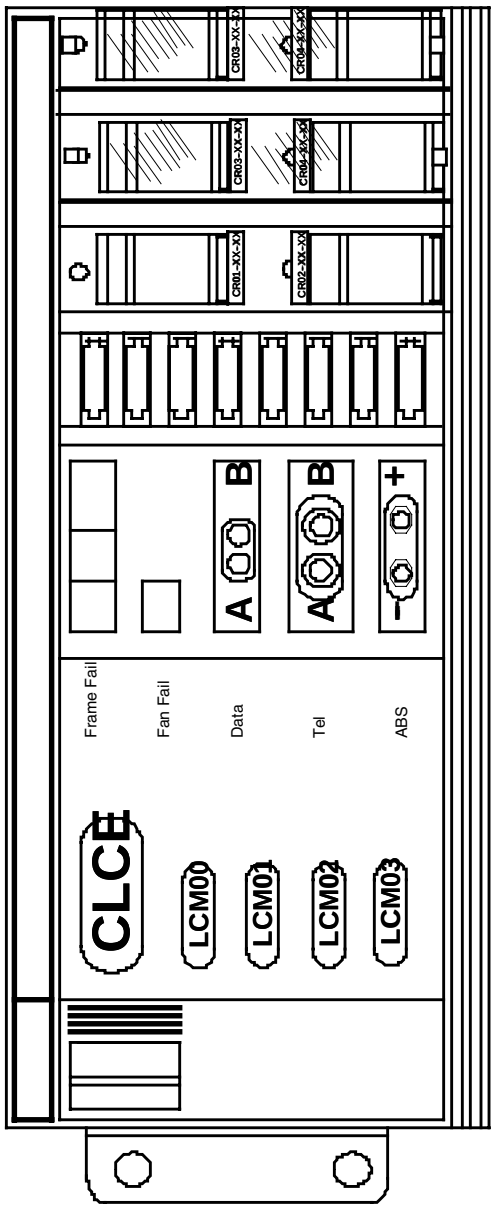
### Blank panels

Blank panels provide safety enclosures over empty card positions in the MSP. The enclosures are on the front and rear. The blank panels are in one-slot (P0734476), two-slot (P0734475) and four-slot (P0734474) sizes.

## Design

The design of the MSP appears in the following figure.

**NTRX40AA parts**




**Note:** This figure is not to scale.

# NTRX41AA

## Product description

The NTRX41AA alarm card monitors and reports alarms for cabinets in a central office environment. This card operates with an input battery voltage of -48 V or -60V.

The NTRX41AA includes the modular supervisory panel (MSP).

## Functional description

The primary function of the NTRX41AA alarm card is to monitor and detect the following types of faults:

- converter faults
- thermal breaker failures
- fan failure on one or two cooling units
- failures in the talk battery modules
- inverter failure in the cabinet
- cabinet temperature that exceeds limits

If any of the first five conditions occur, the NTRX41AA raises alarms and sends signals to the office alarm unit. The NTRX41AA provides maintenance facilities like telephone, data, and alarm battery supply (ABS) jacks.

### Functional blocks

The NTRX41AA has the following functional blocks:

- alarm circuit
- maintenance block

### Alarm circuit

The alarm circuit has transistor logic. The following four alarm inputs activate the transistor logic:

- battery-input voltage triggers a FRAMEFAIL signal for an inverter alarm, talk battery module alarm, or fuse module alarm
- battery-return voltage triggers a FRAMFAIL signal for a converter fail alarm and line concentrating equipment (LCE) alarm
- 90 Vrms triggers a FRAMEFAIL signal for a ringing generator on an LCE cabinet
- battery-input voltage generates a FANFAIL signal and triggers an alarm for the cooling units

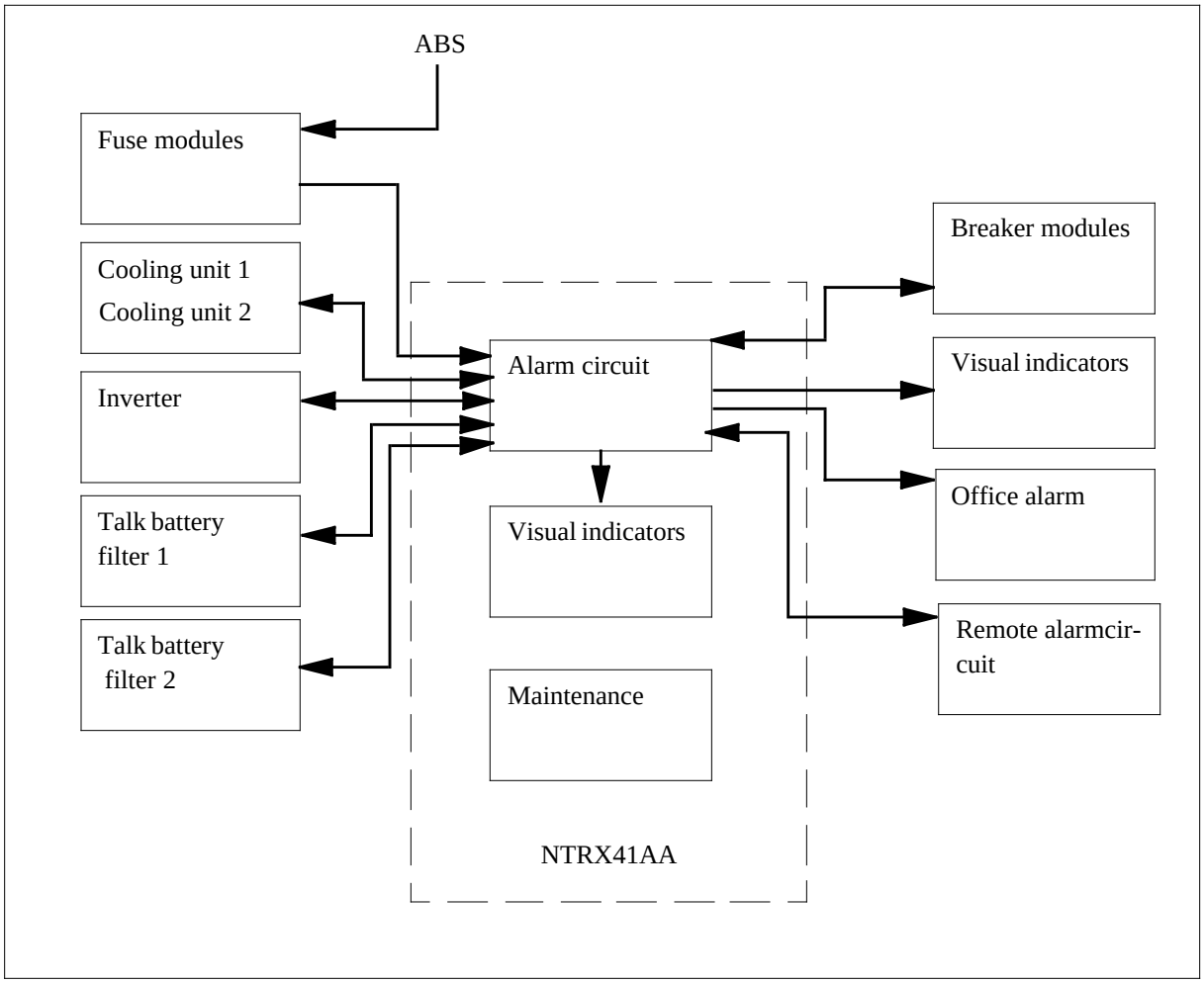
The alarm circuit provides two light-emitting diodes (LED) as visual indicators of the FRAMEFAIL and FANFAIL signals. The alarm circuit can operate two additional external LEDs with a connector interface.

### Maintenance block

The NTRX41AA provides maintenance features like jacks for telephone, data, and alarm-battery supply. These features allow communication and data transmission between offices.

The relationship between the functional blocks appears in the following figure.

**NTRX41AA functional blocks**



## **NTRX41AA** (continued)

# Signaling

### Pin numbers

The pin numbers for the NTRX41AA appear in the following table.

**Connector J1 (Sheet 1 of 2)**

| Pin | D | C | B | A |
|---|---|---|---|---|
| 1 | RINGALM2 | | | RINGALM1 |
| 2 | | | | |
| 3 | | | | |
| 4 | BAT2 | K2 | BAT1 | K1 |
| 5 | BAT4 | K4 | BAT3 | K3 |
| 6 | BAT6 | K6 | BAT5 | K5 |
| 7 | BAT8 | K8 | BAT7 | K7 |
| 8 | BAT10 | K10 | BAT9 | K9 |
| 9 | BAT12 | K12 | BAT11 | K11 |
| 10 | BAT14 | K14 | BAT13 | K13 |
| 11 | BAT16 | K16 | BAT15 | K15 |
| 12 | BAT18 | K18 | BAT17 | K17 |
| 13 | BAT20 | K20 | BAT19 | K19 |
| 14 | | FRAMEFAIL | | FRMFLTST |
| 15 | INVALM | FUSEALM | FAN48 | FAN48 |
| 16 | D1B | D1A | TTB | TTA |
| 17 | -48V2 | -48V2 | -48V1 | -48V1 |
| 18 | -48V4 | -48V4 | -48V3 | -48V3 |
| 19 | FAIL4 | FAIL3 | FAIL2 | FAIL1 |
| 20 | FAIL8 | FAIL7 | FAIL6 | FAIL5 |
| 21 | FAIL12 | FAIL11 | FAIL10 | FAIL9 |
| 22 | FAIL16 | FAIL15 | FAIL14 | FAIL13 |

**Connector J1 (Sheet 2 of 2)**

| Pin | D | C | B | A |
|---|---|---|---|---|
| 23 | FAIL20 | FAIL19 | FAIL18 | FAIL17 |
| 24 | | FANALM2 | | FANALM1 |
| 25 | | | | |
| 26 | FANLMPTST | ACO | AISALM2 | AISALM1 |
| 27 | D2B | D2A | TRB | TRA |
| 28 | BR | BR | BR | BR |
| 29 | | TEMPSW2 | | TEMPSW1 |
| 30 | +15FG | +15FG | +5FG | +5FG |

## Technical data

### Power requirements

The nominal input voltage is -48V or -60V. The NTRX41AA can accept a range of -42V to -75V. The maximum input current is 0.75A.

# NTRX42AA

## Product description

The NTRX42AA is a breaker module with the modular supervisory panel (MSP). The NTRX42AA contains two circuit breakers of -48V or -60V. The circuit breakers provide two 10A power feeds.

## Functional description

The NTRX42AA receives two input feeds from the power distribution center (PDC). The NTRX42AA allows the two breakers mounted on the front to limit the input current. The breakers have automatic recovery from low battery and the standard DMS converter interface that allows the breakers to monitor converters.

The primary functions of the NTRX42AA are as follows:

- monitor and detect converter failures
- trip breakers when overcurrent conditions occur
- trip breakers on converter failure
- provide termination points for PDC feeds
- provide battery feed samples for the alarm module
- respond to ARLB conditions

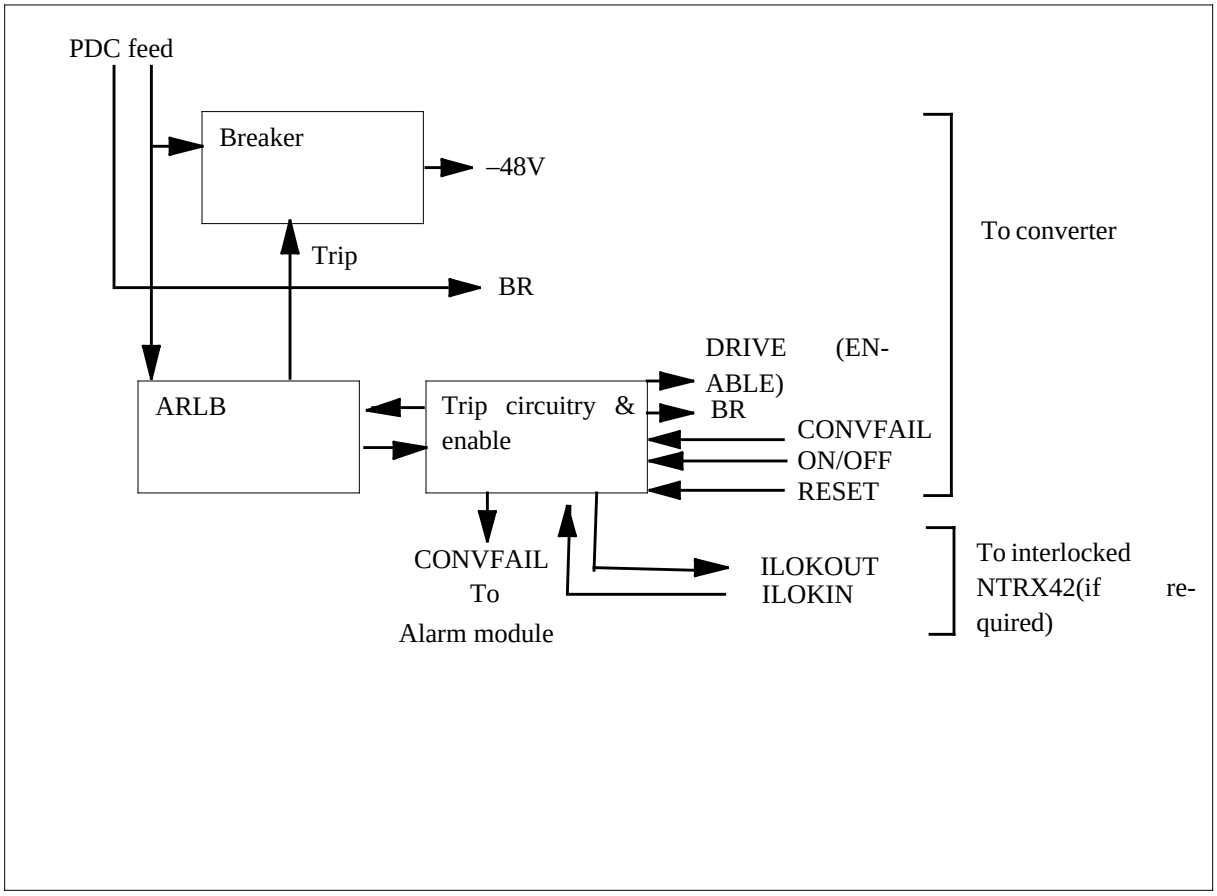
### Functional blocks

The NTRX42AA has the following functional blocks:

- automatic recovery from low battery (ARLB)
- trip circuits and enable
- breakers

The relationship between the functional blocks appears in the following figure.

**NTRX42AA functional blocks**




## Automatic recovery from low battery

The breaker module sends the NT6L62AA ARLB hybrid a sample of each of the two input battery feeds of the breaker. The ARLB provides two outputs to the NTRX42AA. One output controls the two relays on each breaker module. When the sampled voltage is less than -41.5V±0.5V, the relays depower to prevent breaker trip. The relays remove the DRIVE or ENABLE signal that causes the converters to shut down. The battery voltage must increase above -44.5V±0.5V before the RESET relay can start again.

## Trip and enable circuit

A transistor circuit can trip the associated circuit breaker. A transistor circuit trips the breaker when alarm relay releases in the associated power converter or ringing generator occurs. This circuit provides the DRIVE or ENABLE signal for the converters that require these signals.

## NTRX42AA (continued)

### Breakers

The breaker module contains two 10 A magnetic breakers. One breaker is on top of the other breaker. The breakers operate over the complete -48V to -60V range.

## Signaling

### Pin numbers

The pin numbers for the NTRX42AA appear in the following table.

**Connector J1**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | -48VSW1 | 13 | CONVFAIL2 |
| 2 | not used | 14 | ILOKIN |
| 3 | ON/OFF1 | 15 | DRIVE2 |
| 4 | OEM-ALM1 | 16 | not used |
| 5 | OEM-ALM2 | 17 | BAT RTN1 |
| 6 | ON/OFF2 | 18 | BR1 |
| 7 | not used | 19 | RESET1 |
| 8 | -48VSW2 | 20 | CONVFAIL1 |
| 9 | not used | 21 | CONVFAIL2 |
| 10 | DRIVE1 | 22 | RESET2 |
| 11 | ILOKOUT | 23 | BR2 |
| 12 | CONVFAIL1 | 24 | BAT RTN2 |

## Technical data

### Power requirementsInput

The nominal input voltage is -48V or -60V. The NTRX42AA accepts a range between -42V to -72V. The maximum input current is 20A.

## Output specifications

The specified outputs for the NTRX42AA appear in the following table.

**Outputs**

| | |
|---|---|
| Voltage | -48V/-60V |
| High voltage shutdown | -72V |
| Low voltage shutdown | -42V |
| Maximum current | 2 x 10A |
| Minimum current | 0 A |

# NTRX42BA

## Product description

The NTRX42BA is a breaker module with a modular supervisory panel (MSP). The NTRX42BA contains two circuit breakers of -48V or -60V that provide two 15A power feeds.

## Functional description

The NTRX42BA receives two input feeds from the power distribution center (PDC). The NTRX42BA allows the two breakers on the front to limit the input current. The breakers have automatic recovery from low battery (ARLB). The breakers have the standard DMS converter interface that allows the breakers to monitor converters.

The primary functions of the NTRX42BA are as follows:

- monitor and detect converter failures
- trip breakers when over-current conditions occur
- trip breakers on converter failure
- provide termination points for PDC feeds
- provide battery feed samples for the alarm module
- respond to ARLB conditions

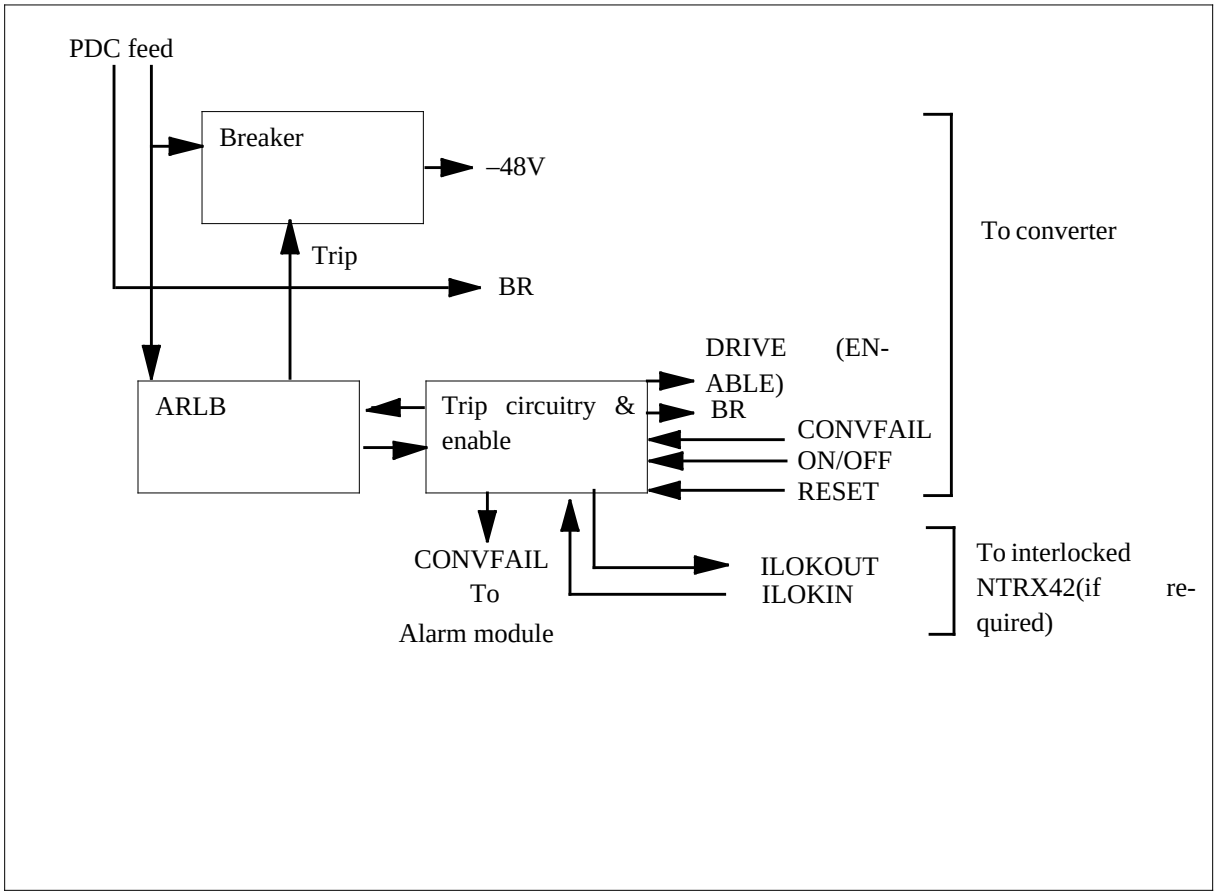
### Functional blocks

The NTRX42BA has the following functional blocks:

- ARLB
- trip circuits and enable
- breakers

The relationship between the functional blocks appears in the following figure.

**NTRX42BA functional blocks**




## Automatic recovery from low battery

The breaker module sends the NT6L62AA ARLB hybrid a sample of each of the two input battery feeds of the breaker. The ARLB provides two outputs to the NTRX42BA. The outputs control the two relays on each breaker module. When the sampled voltage is less than -41.5V±0.5V, the relays depower to prevent breaker trip. The relays remove the DRIVE or ENABLE signal. This condition causes the converters to shut down. The battery voltage must increase above -44.5V±0.5V before the RESET relay starts again.

## Trip and enable circuit

A transistor circuit trips the associated circuit breaker when an alarm relay release in the associated power converter or ringing generator occurs. This circuit provides the DRIVE or ENABLE signal for the converters that require these signals.

## NTRX42BA (continued)

### Breakers

The breaker module contains 15A magnetic breakers. One breaker is on top of the other breaker. The breakers operate over the complete -48V to -60V range.

## Signaling

### Pin numbers

The pin numbers for the NTRX42BA appear in the following table.

**Connector J1**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | -48VSW1 | 13 | CONVFAIL2 |
| 2 | not used | 14 | ILOKIN |
| 3 | ON/OFF1 | 15 | DRIVE2 |
| 4 | OEM-ALM1 | 16 | not used |
| 5 | OEM-ALM2 | 17 | BAT RTN1 |
| 6 | ON/OFF2 | 18 | BR1 |
| 7 | not used | 19 | RESET1 |
| 8 | -48VSW2 | 20 | CONVFAIL1 |
| 9 | not used | 21 | CONVFAIL2 |
| 10 | DRIVE1 | 22 | RESET2 |
| 11 | ILOKOUT | 23 | BR2 |
| 12 | CONVFAIL1 | 24 | BAT RTN2 |

## Technical data

### Power requirements Input

The nominal input voltage is -48V or -60V. The NTRX42BA accepts a range from -42V to -72V. The maximum input current is 30A.

## Output

The specified outputs for the NTRX42BA appear in the following table.

**Outputs**

| | |
|---|---|
| Voltage | -48V or -60V |
| High voltage shutdown | -72V |
| Low voltage shutdown | -42V |
| Maximum current | 2 x 15A |
| Minimum current | 0 A |

# NTRX42CA

## Product description

The NTRX42CA is a breaker module provisioned with a modular supervisory panel (MSP). The NTRX42CA contains two circuit breakers of -48V or -60V that provide two 20A power feeds.

## Functional description

The NTRX42CA receives two input feeds from the power distribution center (PDC). The NTRX42CA allows the two breakers mounted on the front to limit the input current. The breakers have automatic recovery from low battery. The standard DMS converter interface allows the breakers to monitor converters.

The primary functions of the NTRX42CA are as follows:

- monitor and detect converter failures
- trip breakers when overcurrent conditions occur
- trip breakers on converter failure
- provide termination points for PDC feeds
- provide battery feed samples for the alarm module
- respond to ARLB conditions

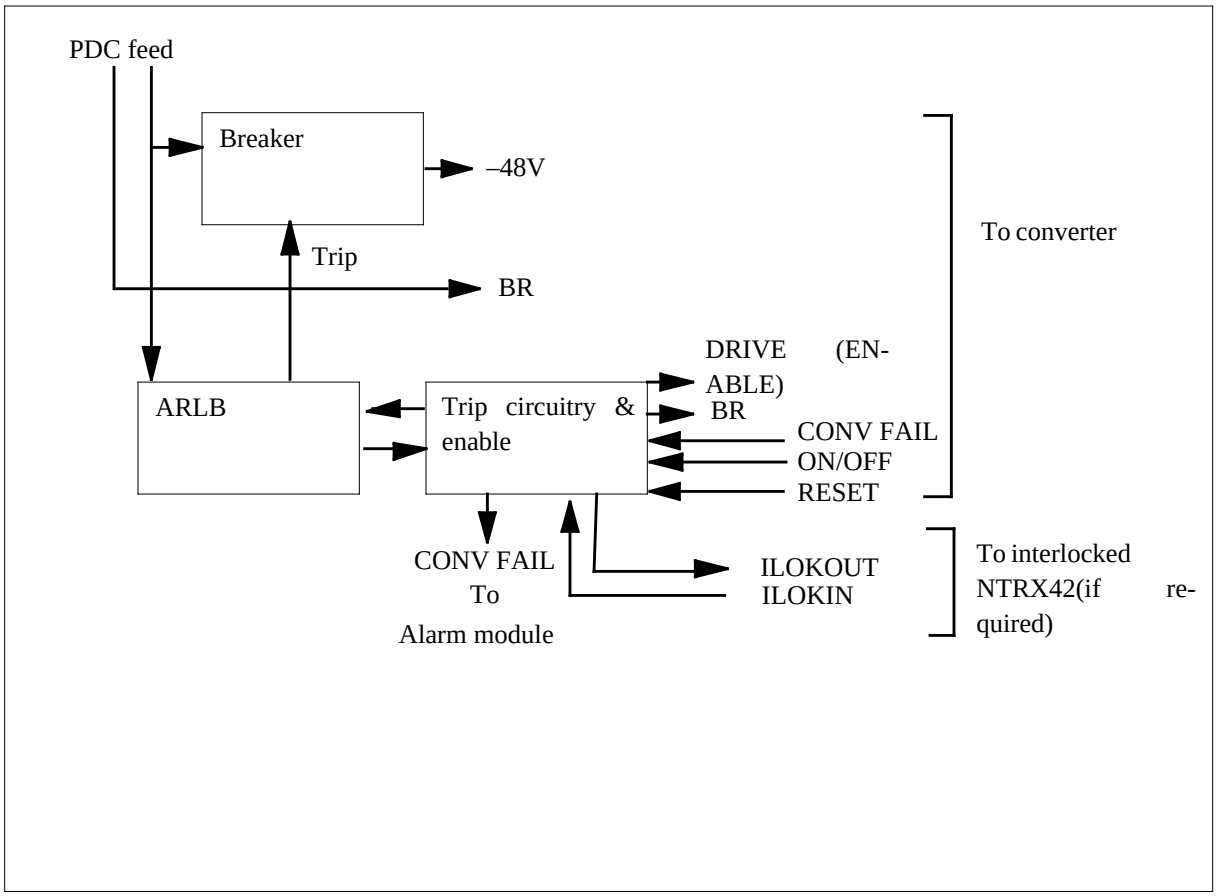
### Functional blocks

The NTRX42CA has the following functional blocks:

- automatic recovery from low battery (ARLB)
- trip circuit and enable
- breakers

The relationship between the functional blocks appears in the following figure.

**NTRX42CA functional blocks**




### Automatic recovery from low battery

The breaker module sends the NT6L62AA ARLB hybrid a sample of each of the two input battery feeds of the breaker. The ARLB provides two outputs to the NTRX42CA. One output controls the two relays on each breaker module. When the sampled voltage is less than -41.5V±0.5V, the relays depower to prevent breaker trip. The relays remove the DRIVE or ENABLE signal. This condition causes the converters to shut down. The battery voltage must increase above -44.5V±0.5V before the RESET relay starts again.

### Trip and enable circuit

A transistor circuit trips the associated circuit breaker. This condition occurs when an alarm relay release in the associated power converter or ringing generator occurs. This circuit provides the DRIVE or ENABLE signal for the converters that require the signal.

## NTRX42CA (continued)

### Breakers

The breaker module has 20A magnetic breakers. One breaker is on top of the other breaker. The breakers operate over the complete -48V to -60V range.

## Signaling

### Pin numbers

The pin numbers for the NTRX42CA appear in the following table.

**Connector J1**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | -48VSW1 | 13 | CONVFAIL2 |
| 2 | not used | 14 | ILOKIN |
| 3 | ON/OFF1 | 15 | DRIVE2 |
| 4 | OEM-ALM1 | 16 | not used |
| 5 | OEM-ALM2 | 17 | BAT RTN1 |
| 6 | ON/OFF2 | 18 | BR1 |
| 7 | not used | 19 | RESET1 |
| 8 | -48VSW2 | 20 | CONVFAIL1 |
| 9 | not used | 21 | CONVFAIL2 |
| 10 | DRIVE1 | 22 | RESET2 |
| 11 | ILOKOUT | 23 | BR2 |
| 12 | CONVFAIL1 | 24 | BAT RTN2 |

## Technical data

### Power requirements Input

The nominal input voltage is -48V or -60V. The NTRX42CA accepts a range from -42V to -72V. The maximum input current is 40A.

## Output

The specified outputs for the NTRX42CA appear in the following table.

**Outputs specifications**

| | |
|---|---|
| Voltage | -48V or -60V |
| High voltage shutdown | -72V |
| Low voltage shutdown | -42V |
| Maximum current | 2 x 20A |
| Minimum current | 0A |

# NTRX43AA

## Product description

The NTRX43AA fuse module provides a maximum of eight current–limited feed outputs and one alarm output for cabinets. The NTRX43AA provides these outputs for a central office. This card operates with input battery voltage of -48V or -60V.

The NTRX43AA contains the modular supervisory panel (MSP). This module does not contain the QFF fuses. The cabinet level provisions the QFF fuses.

## Functional description

The NTRX43AA provides the following functions:

- termination point for power distribution center (PDC) feeds
- eight current–limited outputs for miscellaneous circuits
- reports fuse and breaker failures to the NTRX41AA alarm module

### Functional blocks

Connector P1 on the NTRX43AA provides the power feed for fuses F01 to F04. Connector P2 provides the power feed for fuses F05 to F08. These fuses are on the faceplate of the NTRX43AA. Connector J1 provides the fused outputs with currents that range from 0.18 A to 5.0A. Connector P3 provides alarm outputs that report fuse failure to the NTRX41AA alarm module.

## Signaling

### Pin numbers

The pin numbers for the NTRX43AA appear in the following tables.

**Power input connectors P1 and P2**

| Connector/Pin | Signal |
|---|---|
| P1 1 to 9 | -48V or -60V |
| P1 10 to 18 | BAT RTN |
| P2 1 to 9 | -48V or -60V |
| P2 10 to 18 | BAT RTN |

**NTRX43AA output connector J1**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | -48V OUT 1 | 10 | -48V OUT 5 |
| 2 | -48V OUT 2 | 11 | BAT RTN5 |
| 3 | -48V OUT 4 | 12 | BAT RTN6 |
| 4 | -48V OUT 6 | 13 | BAT RTN3 |
| 5 | -48V OUT7 | 14 | BAT RTN4 |
| 6 | -48V OUT 8 | 15 | NC |
| 7 | BAT RTN1 | 16 | NC |
| 8 | BAT RTN2 | 17 | BAT RTN7 |
| 9 | -48V OUT 3 | 18 | BAT RTN8 |

**Fail alarm connector P3**

| Pin | Signal |
|---|---|
| 1 | FUSEALM |
| 2 | FUSEALM |

# Technical data

## Power requirements

The nominal input voltage is -48V or -60V. The NTRX43AA accepts a range from -42V to -75V. The maximum input current is 30A.

## Output

The specified outputs for the NTRX43AA appear in the following table.

**Output specifications**

| Parameter | Value |
|---|---|
| Maximum voltage | -72V |
| Maximum current | 5. A |
| Minimum voltage | -42V |
| Minimum current | 0.18A |

# NTRX44AA

## Product description

The NTRX44AA talk battery module provides a filtered power feed of a maximum of 20A. The NTRX44AA provides a feed for cabinets in a central office environment. This card provides inrush current protection (soft-start) to protect from power distribution center (PDC) breaker trips.

The NTRX44AA contains the modular supervisory panel (MSP). The NTRX44AA accepts -48V or -60V battery input.

## Functional description

The NTRX44AA provides the following functions:

- termination point for PDC feeds
- filtered battery feed through connector interfaces
- soft-start that a current-limiting startup circuit provides to protect from PDC breaker trip
- two fail alarms

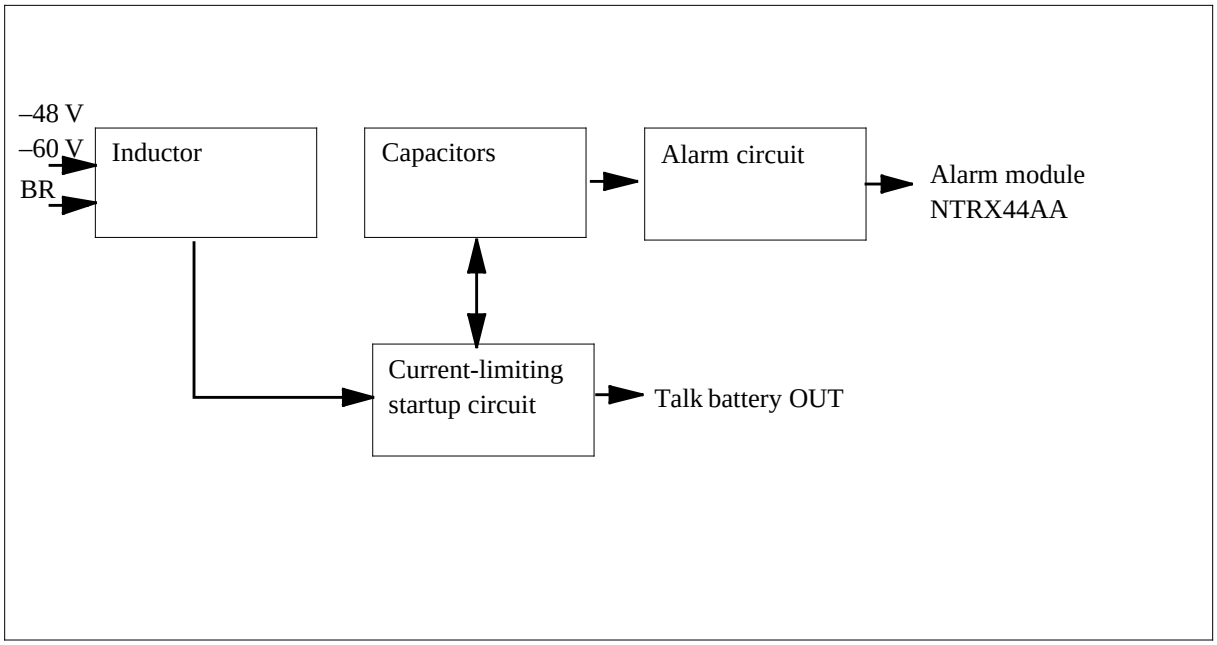
### Functional blocks

The NTRX44AA has the following functional blocks:

- inductor
- capacitors
- current-limiting startup circuit
- alarm circuit

The relationship between the functional blocks appears in the following figure.

**NTRX44AA functional blocks**




### Inductor

The NTRX44AA uses the 20A QHP77C bracket-mounted power inductor.

### Capacitors

The NTRX44AA uses six 80V capacitors that provide 6800 µF capacity.

### Current-limiting startup circuit

This circuit limits the inrush current on startup. This circuit does not cause the PDC breaker to trip. A thermistor charges the capacitors. When the capacitors are charged, a relay receives power. The contacts of the relay connect the capacitors to the output. This soft-start occurs 5 s after input power is applied.

### Alarm circuit

This block reports filter failure in the NTRX44AA to the alarm module (NTRX41AA) through connector P3. The alarm module generates a FRAMEFAIL alarm. This block reports complete power loss to the maintenance trunk monitor (MTM) through connector P4.

## **NTRX44AA** (continued)

# Signaling

### Pin numbers

The pin numbers for the NTRX44AA appear in the following tables.

**PDC power input connector P1**

| Pin | Signal |
|---|---|
| A | -48V or -60V |
| B | -48V or -60V |
| C | BAT RTN |
| D | BAT RTN |

**Talk battery output connector P2**

| Pin | Signal |
|---|---|
| A | TALKBAT |
| B | TALKBAT |
| C | BAT RTN |
| D | BAT RTN |

**FAIL alarm connector P3**

| Pin | Signal |
|---|---|
| 1 | TALKALM |
| 2 | TALKALM |
| ***Note:*** Only pin 1 can connect to alarm module NTRX44AA. | |

**FAIL alarm connector P4**

| Pin | Signal |
|---|---|
| 1 | LOSS1 |
| 2 | LOSS2 |
| ***Note:*** Only pin 1 can connect to alarm module NTRX44AA. | |

# Technical data

## Power requirements

The nominal input voltage is -48V or -60V. The NTRX44AA accepts a range of -42V to -75V. The maximum steady-state input current is 20A. The maximum inrush current is 50A.

## Output

The specified outputs for the NTRX44AA appear in the following table.

**NTRX44AA Output specifications**

| | |
|---|---|
| Voltage | -48V or -60V |
| High voltage shutdown | -75V |
| Low voltage Shutdown | -42V |
| Maximum current | 20A |
| Attenuation | 40 dB @1 kHz |
| Output impedance | 50Ω *@300 to 3500 Hz* |

# NTRX46AA

## Product description

The NTRX46AA cabinetized international peripheral equipment is the international version of the NTRX36AB cabinetized control peripheral equipment.

The NTRX46AA contains two dual shelf extended peripheral modules (XPM) configured as line group controllers (LGC) or digital trunk controllers (DTC). Each shelf contains two LGC/DTC processor boards (NT6X45BA).

The NTRX46AA cabinet connects to the network through DS30 trunks (twisted pairs) or DS512 trunks (fiber optic cables). The cabinet connects the LCMs with DS30A trunks (twisted pairs). All connections to the network, line card modules or PCM-30 trunks pass through the bulkhead for electromagnetic interference (EMI) compliance.

## Parts

The NTRX46AA contains the following parts:

- NTNX26NA—Frame supervisory panel (FSP)
- NTNX27CA—Cooling unit
- NT6X0216—Common peripheral controller shelf assembly (offshore)

### Frame supervisory panel

The NTNX26NA FSP is at the top of the cabinet. The NTNX26NA FSP distributes -48V dc power to shelves and contains cabinet alarms.

### Cooling unit

The NTNX27CA cooling unit is at the bottom of the cabinet. A fan unit in the bottom of the cabinet cools the NTRX46AA with forced air.

### Common peripheral controller shelf assembly (offshore)

Two pairs of shelves contain each module (cabinetized line group equipment [CLGE] and cabinetized digital trunk equipment [CDTE]). One pair of shelves is in positions 47 and 33. The other pair of shelves is in positions 19 and 05. The pairs of shelves are next to each other in the cabinet.

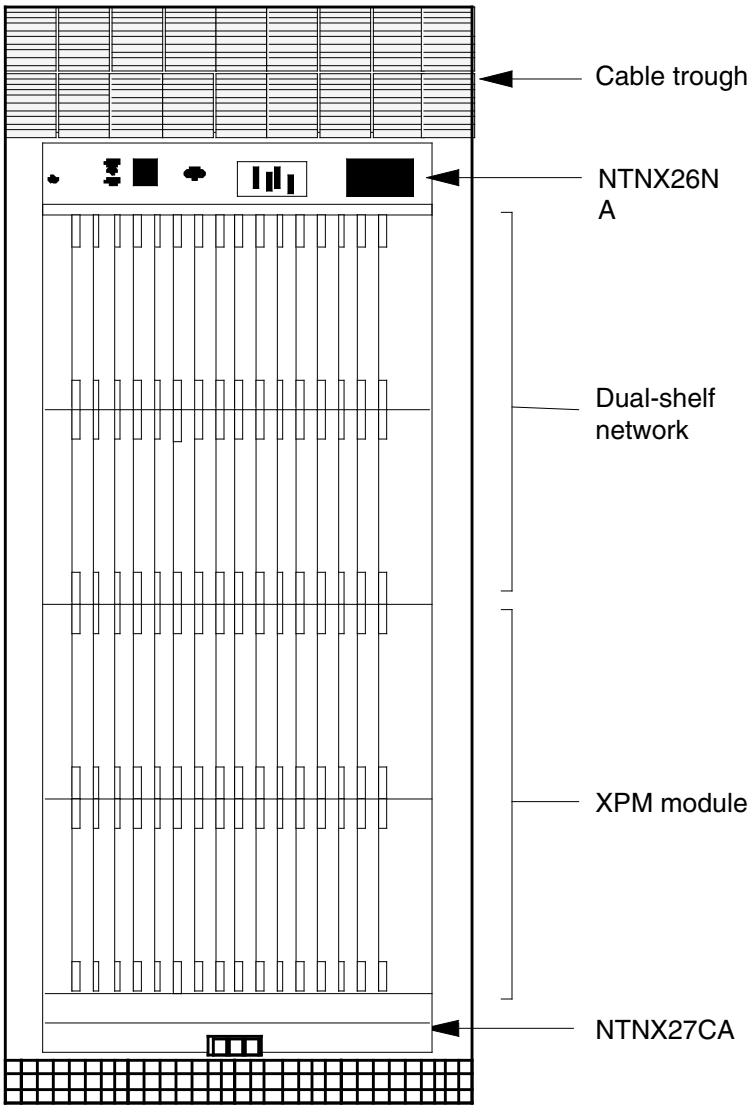
The CLGE defines the function of the CIPE when the cabinet contains the LGC and ISDN LGC.

The CDTE defines the function of the CIPE when the cabinet contains the DTC and ISDN DTC. A toll office requires only CDTE.

## Design

The design of the NTRX46AA appears in the following figure.

**NTRX46AA parts**




**Note**: Front panels are removed to describe NTRX46AA parts. This figure is not to scale.

# NTRX46BA

## Product description

The NTRX46BA cabinetized international peripheral equipment fiber ISDN (CIPE) is the international version of the NTRX46BA cabinetized control peripheral equipment.

The NTRX46BA contains two dual-shelf extended peripheral modules (XPM) configured as line group controllers (LGC) or digital trunk controllers (DTC). Each shelf contains two LGC/DTC processor boards (NT6X45BA).

The NTRX46BA cabinet connects to the network through DS30 trunks (twisted pairs) or DS512 trunks (fiber optic cables). All connections to the network, line card modules, or PCM-30 trunks pass through the bulkhead for electromagnetic interference (EMI) compliance.

## Parts

The NTRX46BA contains the following parts:

- NT6X0216—common peripheral controller shelf assembly (offshore)
- NTNX27CA—cooling unit, -48V (dc)
- NTRX40AA—modular supervisory panel (MSP)
- NTRX51AA—cooling unit, -60V (dc)
- P0734655—filler faceplate
- P0734654—filler faceplate
- P0734653—filler faceplate
- P0734652—filler faceplate

### Common peripheral controller shelf assembly (offshore)

Two pairs of adjacent shelves contain each module (cabinetized line group equipment (CLGO) and cabinetized digital trunk equipment (CDTO). One pair of shelves is in positions 47 and 33. The other pair of shelves is in positions 19 and 05.

The CLGO defines the function of the CIPE when the cabinet contains the LGC and ISDN LGC.

The CDTO defines the function of the CIPE when the cabinet contains the DTC and ISDN DTC. A toll office requires only CDTO.

### Modular supervisory panel

The NTRX40AA modular supervisory panel (MSP) is at the top of the cabinet. The NTRX40AA distributes dc voltages of -48V or -60V to shelves. The NTRX40AA contains cabinet alarms.

### Cooling unit

The NTRX27CA cooling unit is at the bottom of the cabinet. The NTRX27CA provides forced-air cooling through a fan unit in the bottom of the cabinet.

### Cooling unit

The NTRX51AA cooling unit is at the bottom of the cabinet. The NTRX51AA provides forced-air cooling through a fan unit in the bottom of the cabinet.

### Filler faceplate

The P0734652 filler faceplate covers shelf position 05 when shelf 05 is not used.

### Filler faceplate

The P0734653 filler faceplate covers shelf position 19 when shelf 19 is not used.

### Filler faceplate

The P0734654 filler faceplate covers shelf position 33 when shelf 33 is not used.

### Filler faceplate

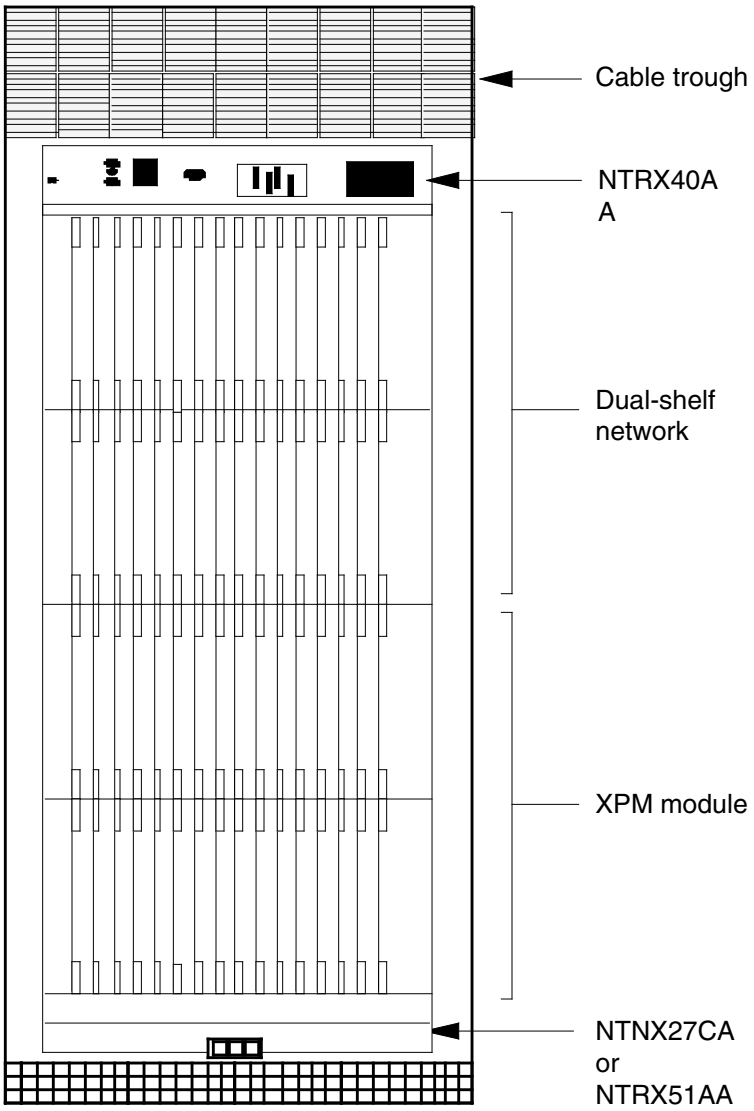
The P0734655 filler faceplate covers shelf position 47 when shelf 47 is not used.

## Design

The design of the NTRX46BA appears in the following figure.

# **NTRX46BA** (end)

**NTRX46BA parts**




**Note:** Front panels are removed to describe NTRX46BA parts. This figure is not drawn to scale.

# NTRX46CA

## Product description

The NTRX46CA cabinetized international peripheral equipment fiber ISDN (CIPE) is the international version of the NTRX36AB cabinetized control peripheral equipment.

The NTRX46CA contains two dual-shelf extended peripheral modules (XPM) configured as line group controllers (LGC) or digital trunk controllers (DTC). Each shelf contains two LGC/DTC processor boards (NT6X45BA).

The NTRX46CA cabinet connects to the network through DS30 trunks (twisted pairs) or DS512 trunks (fiber optic cables). All connections to the network, line card modules, or PCM-30 trunks pass through the bulkhead for electromagnetic interference (EMI) compliance.

## Parts

The NTRX46CA contains the following parts:

- NT6X0216—common peripheral controller shelf assembly (offshore)
- NTNX27CA—cooling unit, -48V (dc)
- NTRX40AA—modular supervisory panel (MSP)
- NTRX51AA—cooling unit, -60V (dc)
- P0734655—personality plate
- P0734654—personality plate
- P0734653—personality plate
- P0734652—personality plate

### Common peripheral controller shelf assembly (offshore)

Two pairs of shelves contain module cabinetized line group equipment (CLGO) and cabinetized digital trunk equipment (CDTO). One pair of shelves is in positions 47 and 33. The other pair of shelves is in positions 19 and 05.

The CLGO defines the function of the CIPE when the cabinet contains the LGC and ISDN LGC.

The CDTO defines the function of the CIPE when the cabinet contains the DTC and ISDN DTC. A toll office requires only CDTO.

## NTRX46CA (continued)

### Modular supervisory panel

The NTRX40AA MSP is located at the top of the cabinet and distributes dc voltages of -48V or -60V to shelves. The NTRX40AA MSP contains cabinet alarms.

### Cooling unit

The NTRX27CA cooling unit is at the bottom of the cabinet. The NTRX27CA provides forced-air cooling through a fan unit at the bottom of the cabinet.

### Cooling unit

The NTRX51AA cooling unit is located at the bottom of the cabinet. The NTRX51AA provides forced-air cooling through a fan unit at the bottom of the cabinet.

### Personality plate

The P0734652 personality plate covers shelf position 05 when shelf 05 is not used.

### Personality plate

The P0734653 personality plate covers shelf position 19 when shelf 19 is not used.

### Personality plate

The P0734654 personality plate covers shelf position 33 when shelf 33 is not used.

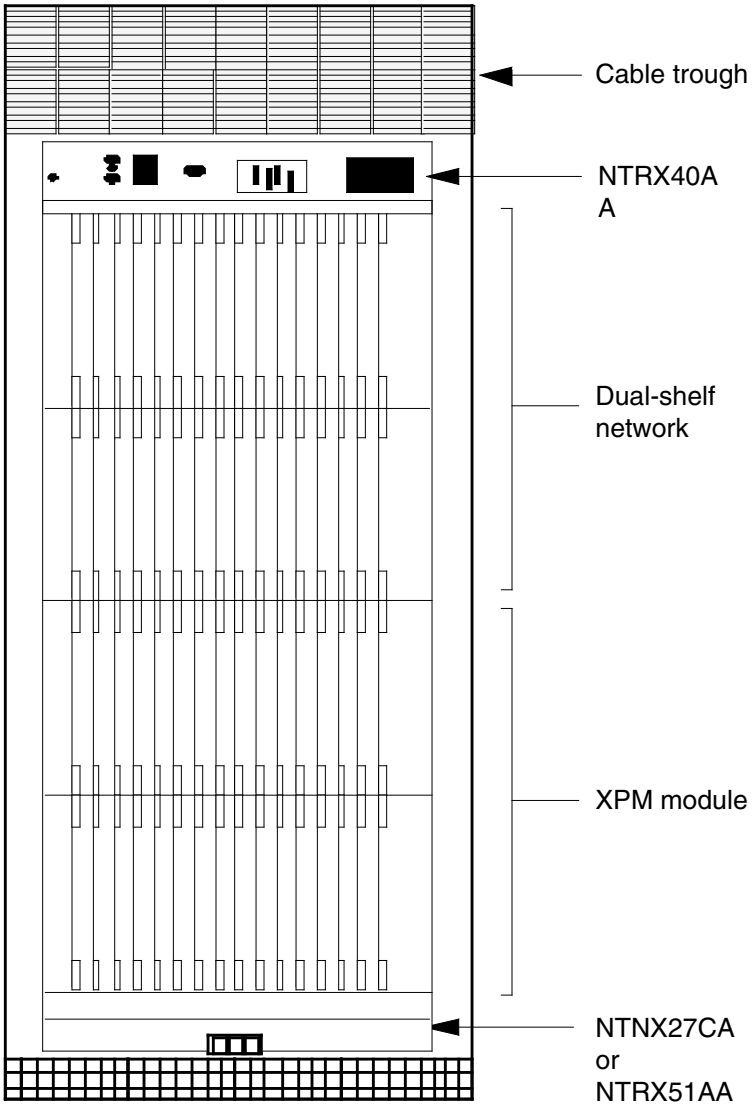
### Personality plate

The P0734655 personality plate covers shelf position 47 when shelf 47 is not used.

## Design

The design of the NTRX46CA appears in the following figure.

**NTRX46CA parts**




**Note:** Front panels are removed to describe NTRX46CA parts. This figure is not to scale.

# NTRX47AA

## Product description

The cabinetized international digital controller (CIDC) contains two dual shelf extended peripheral modules (XPM). These dual shelf XPMs can be line group controllers (LGC) or digital trunk controllers (DTC). Each shelf contains three LGC/DTC processor cards.

All external connections except power are through the bulkhead. The CIDC can provide the following interfaces:

- DS30 or DS512
- PCM-30 with or without DS-0
- DS30A
- Echo canceller

The DS-0 I/F card (NT6X55CA) can be in slot 1 or unit 1 of the module.

## Parts

The NTRX47AA contains the following parts:

- NTNX27CA—Cooling unit
- NT6X0211—International common peripheral controller array shelf assembly
- NT7X34DA—Frame supervisory panel (FSP)

### Cooling unit

The NTNX27CA cooling unit is at the bottom of the cabinet. The NTNX27CA provides forced-air cooling through a fan unit in the bottom of the cabinet.

### International common peripheral controller array shelf assembly

Two pairs of shelves contain each module (line group equipment [LGE] and digital trunk equipment [DTE]). One pair of shelves is in positions 47 and 33. The other pair of shelves is in positions 19 and 05.

The cabinetized LGE (CLGE) defines the intended function of the CIDC. This condition occurs when the cabinet contains the LGC and ISDN LGC.

The cabinetized DTE (CDTE) defines the intended function of the CIDC. This condition occurs when the cabinet contains the DTC and ISDN DTC. A toll office requires only CDTE.

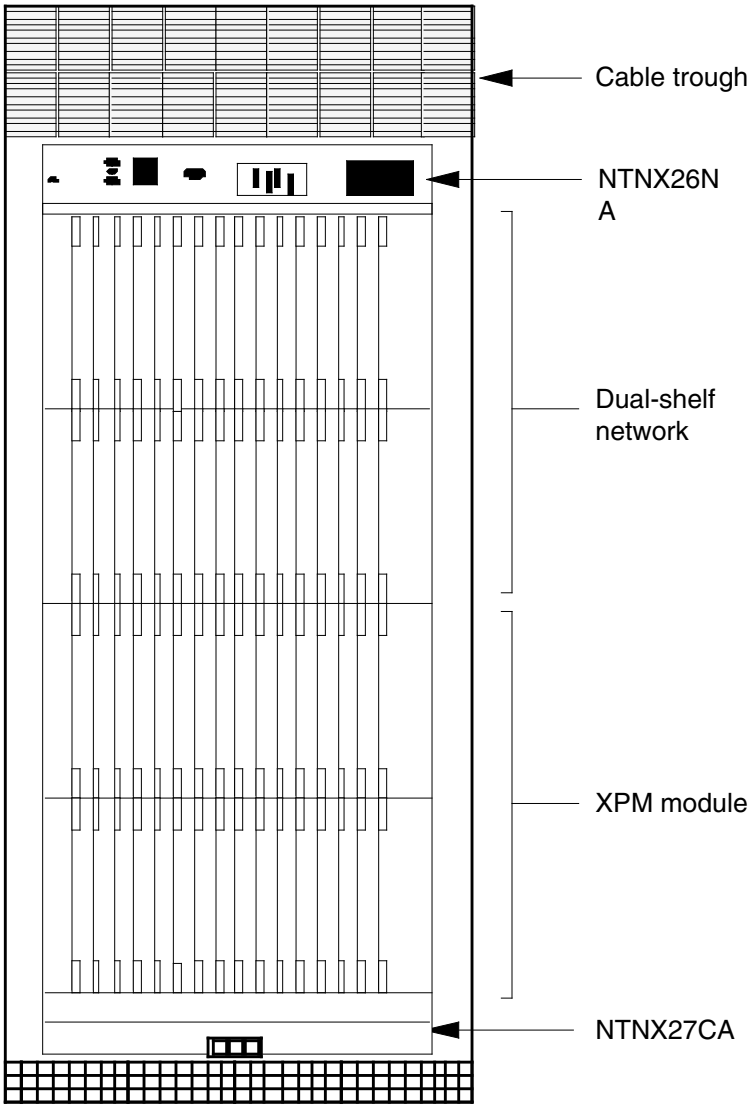
### Frame supervisory panel

The NT7X34DA FSP is at the top of the cabinet and distributes -48V dc power to shelves. The NT7X34DA FSP contains cabinet alarms.

## Design

The design of the NTRX47AA appears in the following figure.

**NTRX47AA parts**




**Note:** Front panels are removed to describe NTRX47AA parts. This figure is not drawn to scale.

# NTRX47BA

## Product description

The cabinetized international digital controller (CIDC) contains two dual shelf extended peripheral modules (XPM). These modules are configured as line group controllers (LGC) or digital trunk controllers (DTC). Each shelf contains three LGC/DTC processor cards.

External connections are through the bulkhead. Power is not through the bulkhead. The CIDC can provide the following interfaces:

- DS30 or DS512
- PCM–30 with or without DS0
- DS30A
- echo canceller

The DS0 I/F card (NT6X55CA) can be assigned in slot 1 or unit 1 of the module.

## Parts

The NTRX47BA contains the following parts:

- NT6X0211—international common peripheral controller array shelf assembly
- NTRX40AA—modular supervisory panel (MSP)
- NTNX27CA—cooling unit

### International common peripheral controller array shelf assembly

Two shelves that are next to each other contain each module. The modules are line group equipment [LGE] and digital trunk equipment [DTE]). The shelves are one pair of shelves in positions 47 and 33 and one pair in positions 19 and 05.

The cabinetized LGE (CLGE) defines the intended function of the CIDC when the cabinet is configured to contain the LGC and ISDN LGC.

The cabinetized DTE (CDTE) defines the intended function of the CIDC when the cabinet is configured to contain the DTC and ISDN DTC. A toll office only requires CDTE.

### Modular supervisory panel

The NTRX40AA MSP is at the top of the cabinet and distributes -48V dc power to shelves and contains cabinet alarms.

### Cooling unit

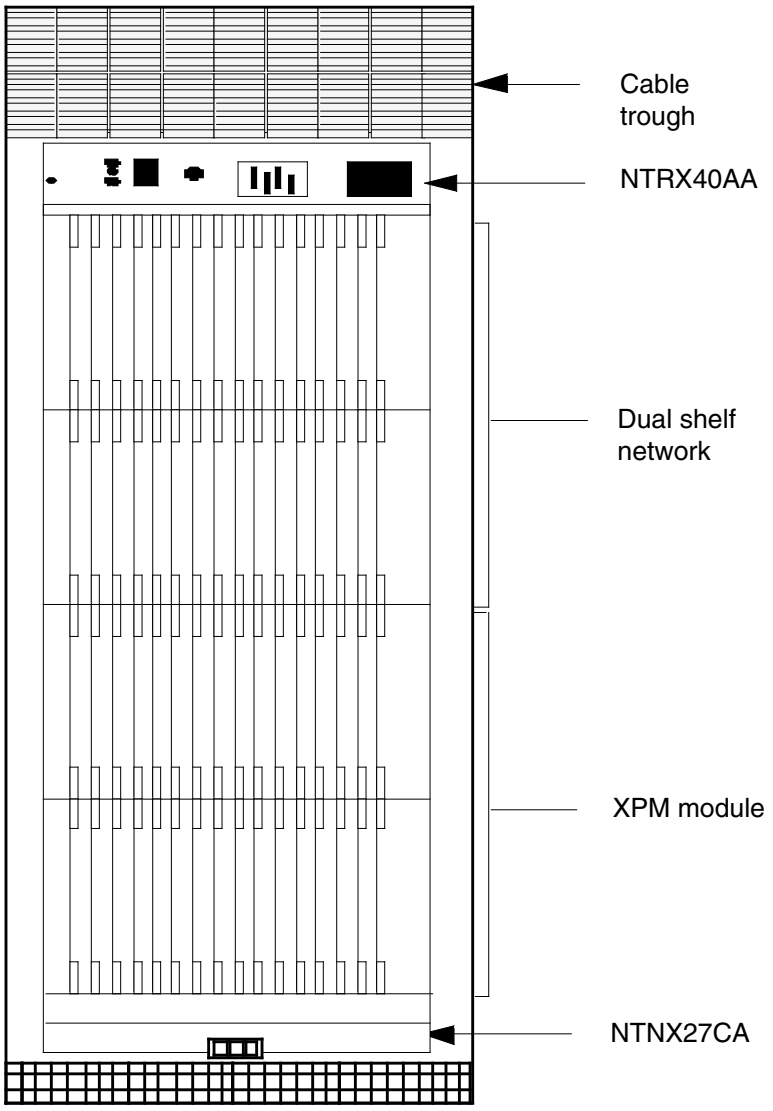
The NTNX27CA cooling unit is at the bottom of the cabinet. This unit provides forced–air cooling with a fan unit integrated in the base of the cabinet.

## Design

The design of the NTRX47BA appears in the following figure.

# **NTRX47BA** (end)

**NTRX47BA parts**




**Note:** This figure does not include front panels to show NTRX47BA parts. This diagram is not drawn to scale.

# NTRX48AA

## Product description

The cabinetized international message and buffer switch (CMS7) contains two message switch and buffer 7 (MSB7) shelves. The CMS7 also contains two signalling terminal array shelf (STA7) shelves.

The MSB7 shelves connect to each plane of the cabinetized dual shelf network. The shelves connect to each plane through the cabinetized speech link connection through bulkhead DS30 cabling. Each MSB7 shelf can take four signalling terminals for each cabinet.

## Parts

The NTRX48AA contains the following parts:

- NTNX26HA—Frame supervisory panel (FSP)
- NTNX27CA—Cooling unit
- NT6X0801—Signalling terminal shelf assembly
- NT6X3201—STA7 shelf assembly

### Frame supervisory panel

The NTNX26HA FSP is at the top of the NTRX48AA. The NTNX26HA FSP distributes power, control, and alarms to the cabinet.

### Cooling unit

An NTNX27CA fan unit integrated in the base of the cabinet provides the CMS7 with forced-air cooling.

### Signaling terminal shelf assembly

The CMS7 contains two signalling terminal shelf assemblies at shelf positions 33 and 47.

### Signaling terminal array 7 shelf assembly

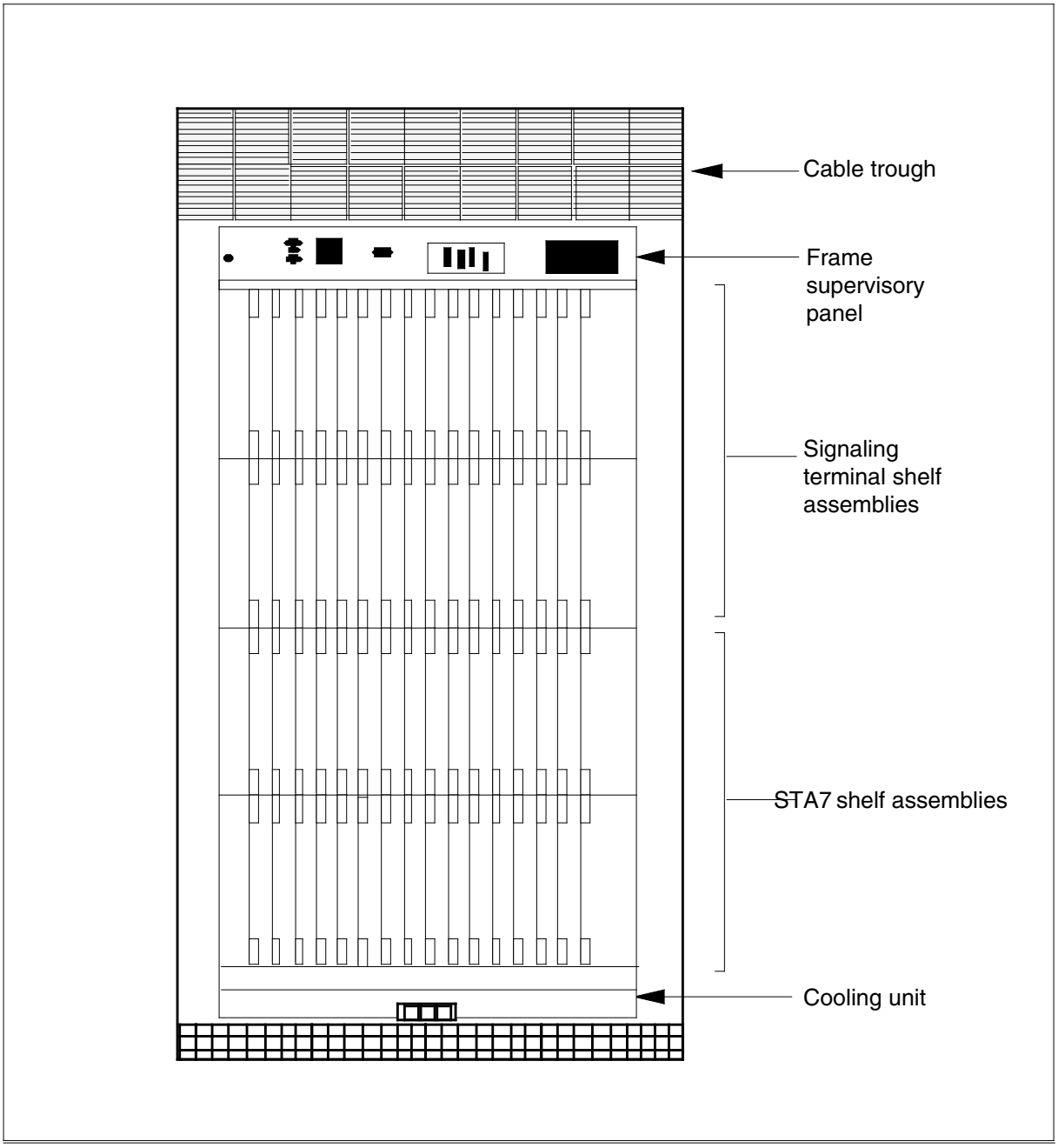
The CMS7 contains two STA7 shelf assemblies at shelf positions 05 and 19.

## Design

The design of the NTRX48AA appears in the following figure.

## **NTRX48AA** (end)

**NTRX48AA parts**




***Note:*** This figure does not include the front panels to show NTRX48AA parts. This figure is not drawn to scale.

# NTRX48BA

## Product description

The cabinetized international message and buffer switch (CMS7) contains two message switch and buffer 7 (MSB7) shelves. The CMS7 also contains two signaling terminal array shelves (STA7).

The MSB7 shelves connect to each plane of the cabinetized dual shelf network. The shelves connect to each plane through the cabinetized speech link connection with bulkhead DS30 cabling. Each MSB7 shelf can take four signaling terminals in each cabinet.

## Parts

The NTRX48BA contains the following parts:

- NT6X0801—signaling terminal shelf assembly
- NT6X3201—STA7 shelf assembly
- NTRX40AA—modular supervisory panel (MSP)
- NTNX27CA—cooling unit

### Signaling terminal shelf assembly

The CMS7 contains two signaling terminal shelf assemblies at shelf positions 33 and 47.

### Signaling terminal array 7 shelf assembly

The CMS7 contains two STA7 shelf assemblies at shelf positions 05 and 19.

### Modular supervisory panel

The NTRX40AA MSP is at the top of the NTRX48BA. The NTRX40AA MSP distributes power, control, and alarms to the cabinet.

### Cooling unit

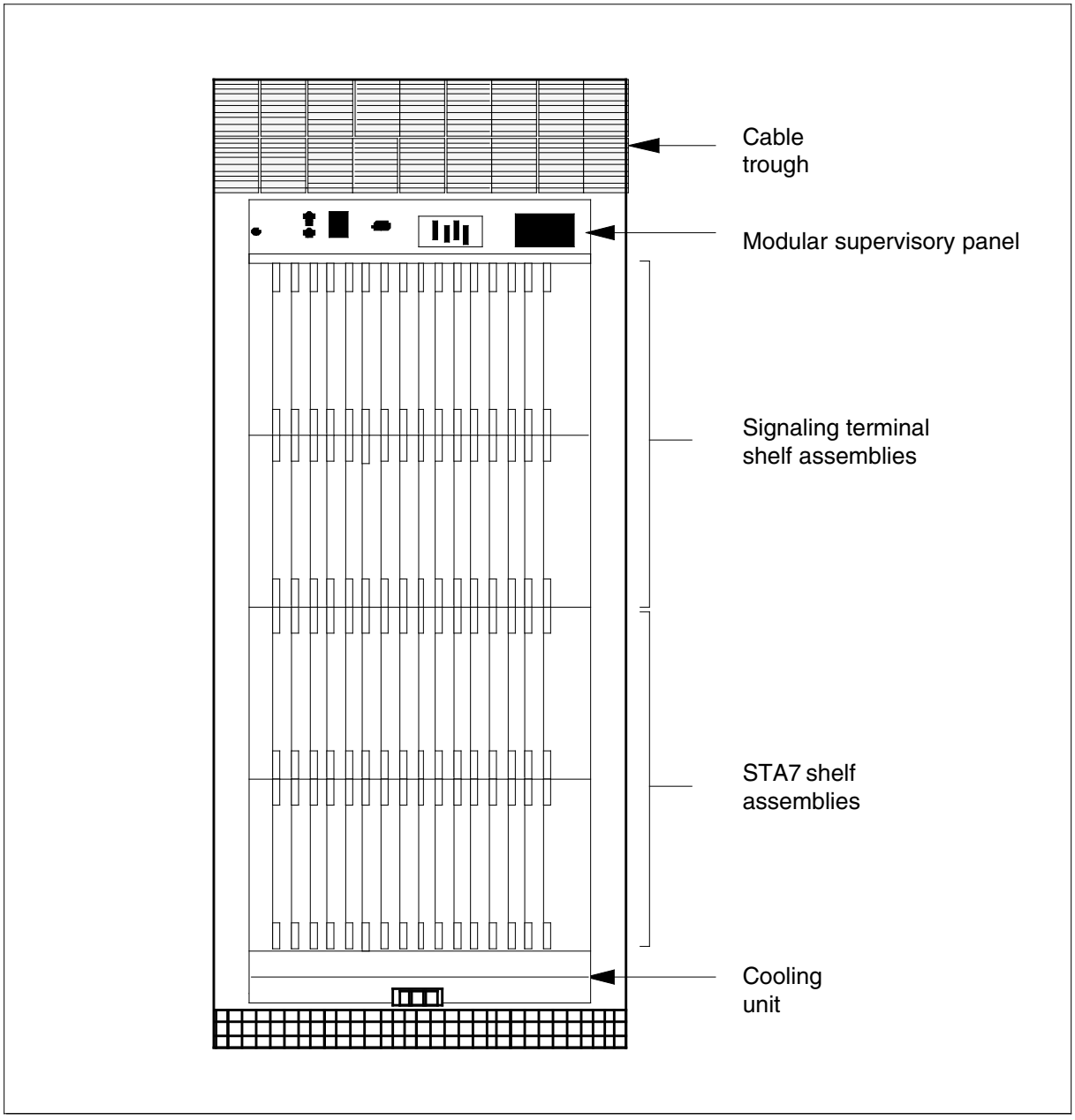
An NTNX27CA fan unit integrated in the base of the cabinet provides the CMS7 with forced-air cooling.

## Design

The design of the NTRX48BA appears in the following figure.

# **NTRX48BA** (end)

**NTRX48BA parts**




***Note:*** This figure does not include the front panels to show NTRX48BA parts. This figure is not drawn to scale.

# NTRX49AA

## Product description

The cabinetized miscellaneous spares storage (CMSS) can be provisioned with shelves and shelf inserts. The shelves and shelf inserts provide storage for circuit packs and a utility tray for technician tools. The NTRX49AA provides framework, hardware, and ground braid assembly.

## Parts

The NTRX49AA contains the following parts:

- NTNX2201—Storage shelf assembly
- NTNX2203—SuperNode spares circuit pack shelf assembly
- NTNX2204—Storage shelf assembly insert
- NT3X55BA—Line card storage chassis

### Storage shelf assembly

The NTNX2201 storage shelf assembly can be in positions 03, 17, 31 and 45. Always provision the NTNX2201 from the bottom up. The NTNX2201 assembly provides a card cage and sliders in the front and the rear to mount spare circuit packs. The shelf can accommodate a maximum of 54 circuit packs (22.2 mm [.875 in.] wide) or 42 circuit packs (28.5 mm [1.124 in.] wide). You can provision one NTNX2201 for each mounting position.

### SuperNode spares circuit pack shelf assembly

The assembly provides a card cage and sliders to store a maximum of two power converters and 20 SuperNode-size cards on the front side. The assembly provides a card cage and sliders to store a maximum of 26 paddle boards on the rear side.

The NTNX2203 SuperNode spares circuit pack shelf assembly can be in positions 04, 18, 32, and 46. Always provision the NTNX2203 from the bottom up. When you mix NTNX2201 with NTNX2203 assemblies, provision the NTNX2201 shelf assemblies first.

The NTNX2203 is provisioned in position 46 when NTNX2201 is provisioned in position 31.

### Storage shelf assembly insert

The NTNX2204 storage shelf assembly insert provides storage for odd size circuit packs. The shelf insert can store a maximum of 22 circuit packs. You can install two shelf insert assemblies in the bottom NTNX2201 shelf at location 03. One NTNX2204 shelf insert is in the left side of NTNX2201 from

## **NTRX49AA** (continued)

the front. The second NTNX2204 in the left side of NTNX2201 from the rear of the cabinet.

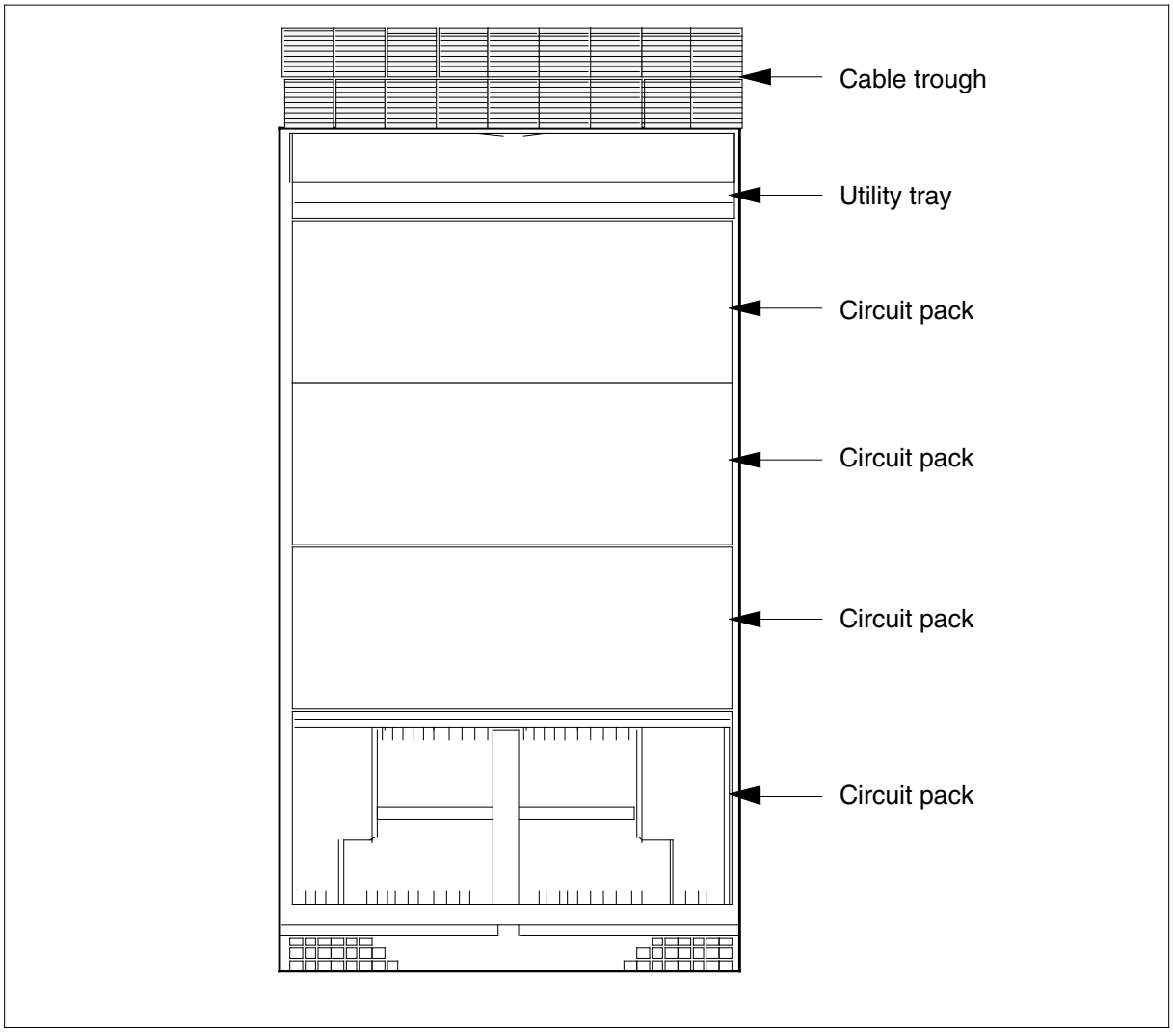
### Line card storage chassis

A line card storage chassis is provided when line cards are provisioned. If the system requires line cards and three or more networks, two line card storage chassis must be provided.

## Design

The design of the NTRX49AA appears in the following figure.

**NTRX49AA parts**



***Note:*** This figure does not include the front panels to identify NTRX49AA parts. This figure is not to scale.

# NTRX49BA

## Product description

The cabinetized miscellaneous spares storage (CMSS) can be provisioned with shelves and shelf inserts. The shelves and shelf inserts provide storage for circuit packs and a utility tray for technician tools. The NTRX49BA provides framework, hardware, and ground braid assembly.

## Parts

The NTRX49BA contains the following parts:

- NT3X55BA—line card storage chassis
- NTNX2201—storage shelf assembly
- NTNX2203—SuperNode spares circuit pack shelf assembly
- NTNX2204—storage shelf assembly insert

### Line card storage chassis

A line card storage chassis is provided when line cards are provisioned. If the system requires line cards and a maximum of three networks, two line card storage chassis must be provided.

### Storage shelf assembly

The NTNX2201 storage shelf assembly can be in positions 03, 17, 31 and 45. Always provision the NTNX2201 from the bottom up. The NTNX2201 assembly provides a card cage and sliders in the front and the rear to mount spare circuit packs. The shelf can accommodate a maximum of 54 circuit packs (22.2 mm [.875 in.] wide) or 42 circuit packs (28.5 mm [1.124 in.] wide). You can provision one NTNX2201 in each mounting position.

### SuperNode spares circuit pack shelf assembly

The assembly provides a card cage and sliders to store a maximum of two power converters and 20 SuperNode-size cards on the front side. The assembly provides a card cage and sliders to store a maximum of 26 paddle boards on the rear side.

The NTNX2203 SuperNode spares circuit pack shelf assembly can be in positions 04, 18, 32, and 46. Always provision the NTNX2203 from the bottom up. When you mix NTNX2201 with NTNX2203 assemblies, provision the NTNX2201 shelf assemblies first.

The NTNX2203 is provisioned in position 46 when the NTNX2201 is provisioned in position 31.

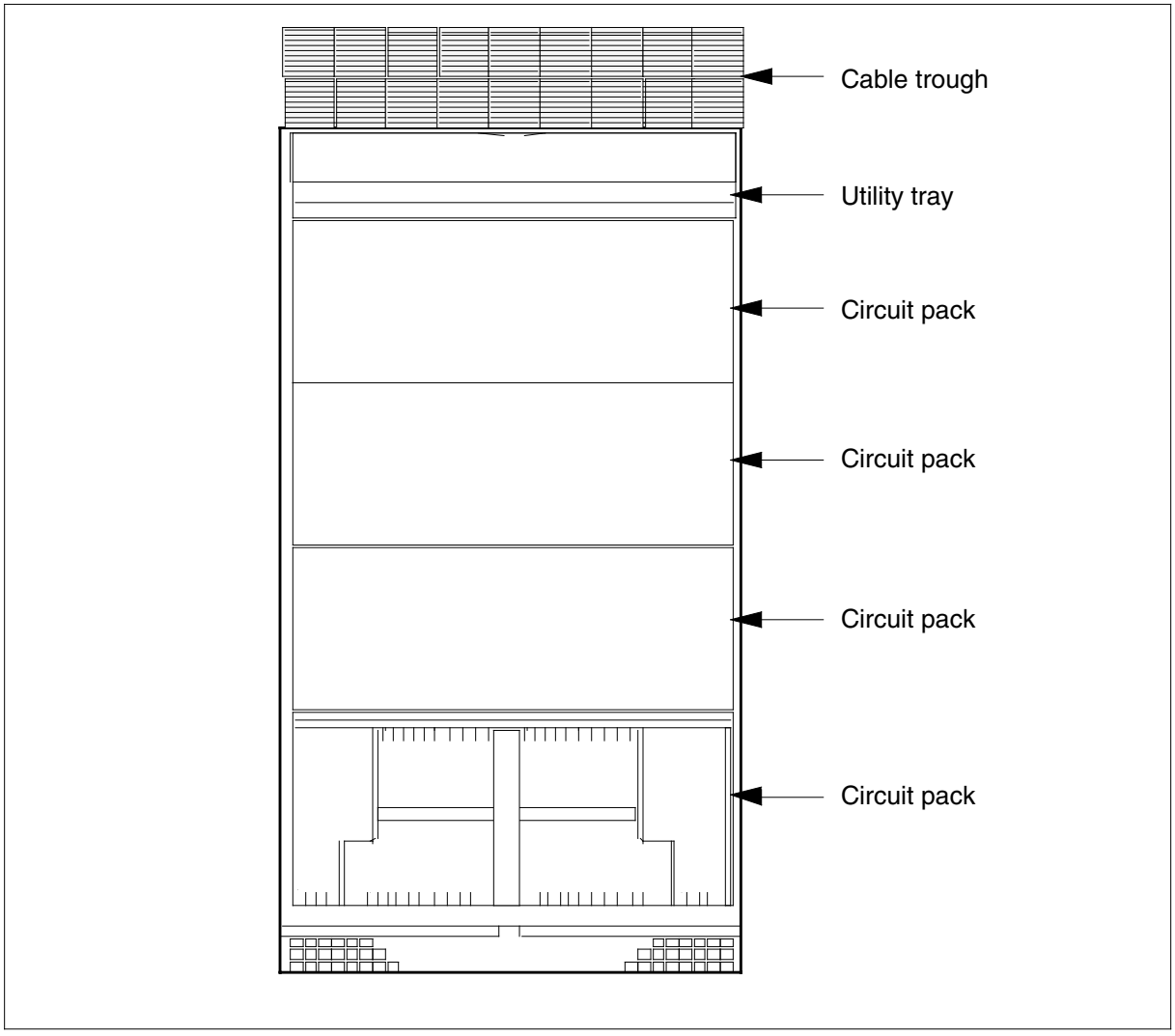
### Storage shelf assembly insert

The NTNX2204 storage shelf assembly insert provides storage for odd size circuit packs. The shelf insert can store a maximum of 22 circuit packs. You can install two shelf insert assemblies in the bottom NTNX2201 shelf at location 03. One NTNX2204 shelf insert is in the left side of NTNX2201 from the front. The second NTNX2204 is in the left side of NTNX2201 from the rear of the cabinet.

## Design

The design of the NTRX49BA appears in the following figure.

**NTRX49BA parts**



## **NTRX49BA** (end)

***Note:*** This figure does not include the front panels to show NTRX49BA parts. This figure is not drawn to scale.

# NTRX50FA

## Product description

The SuperNode Data Manager fault tolerant (SDM-FT) product is a high performance computing platform. The SDM-FT is integrated into the Digital Multiplex System (DMS) architecture from a physical, maintenance and alarm point of view. This platform can host many different services and applications to provide the DMS SuperNode switch enhanced operations administrations maintenance and provisioning (OAM&P) services

The SDM-FT has direct DS-512 links to the message switch (MS) to communicate with the computing module (CM). Ethernet local area network (LAN) ports are available for connecting to the operating company LAN. Remote access to console ports is through modems for maintenance purposes.

## Functional description

The main function of the SDM-FT is to make sure a single hardware failure does not create an interruption of service. This assurance is achieved by redundant hardware and devices within the operating system that detect hardware failure and if required switch activity to the standby hardware component

The SDM-FT is in a cabinetized SDM (CSDM). The CSDM contains a:

- main chassis
- optional input output expansion chassis
- modular supervisory panel (MSP)
- cooling fan unit

### System features

Capabilities of the SDF-FT platform are:

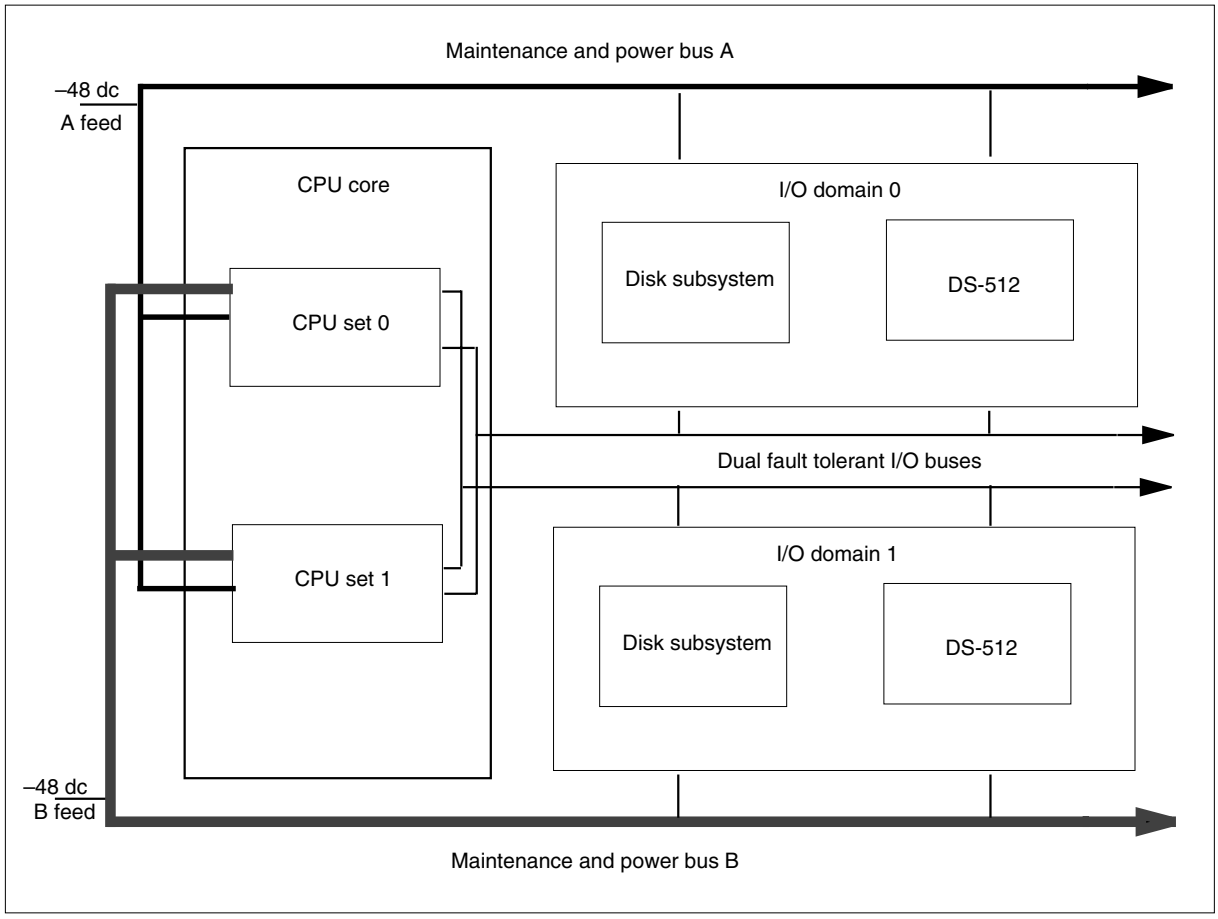
- System wide in-service (InSv) field replaceable units.
- Modules powered directly from operating company, battery feed power supply units.
- Front modules can be separately turned off and on through software control.
- Redundant separately powered fan trays that automatically adjust their speed depending on chassis temperature.
- If one fan tray fails, a single fan tray can provide enough cooling under normal operating conditions.
- The central processing unit (CPU) core is powered by A and B battery feeds.

## **NTRX50FA** (continued)

- The CPU-core includes redundant active and standby CPU-sets that run in lock step. In the event an active CPU-set fails, the switch from the active CPU-set to the standby CPU-set takes a maximum of 150ms.
- Dynamic random access memory (RAM) capacity can expand to 512 Mbyte per CPU-set.
- Device drivers that switch to the standby hardware if the active hardware fails.
- Redundant input output area 0 and 1, powered in order by battery feeds A and B.
- Separate input output buses for each input output area accessed by both CPU-sets in the CPU-core.
- Redundant input output areas make sure continuous available Ethernet and continuous disk mirroring.
- Automatic re-synchronize of replaced disk drives performed as a background task, without affecting service.
- Mirrored disk storage up to 22 GB.
- Direct redundant DS-512 links to the MS.
- Latent fault checking on the standby hardware.
- Operating company alarm interface to report operating system and single power feed failures and total system outages.

The next diagram is a diagram of the NTRX50FA fault tolerant architecture.

**NTRX50FA fault tolerant architecture**




The SDM-FT hardware includes a CPU-core and dual input output areas. The CPU-core contains all the main processing power and memory capacity of the system. The CPU-core contains up of two CPU modules call CPU-sets. The CPU-sets run in lock-step as master and checker, executing the same instructions. Only the master has control of both input output buses. Before the master assigns an input output transaction to the input output buses, the master compares its results to the checker. Any differences causes an exception, the recovery from the fault is performed by the corresponding exception handler. This operation is transparent to the application software. On exit the exception handler turns off the faulty CPU-set and the surviving CPU-set has ownership

## **NTRX50FA** (continued)

of the input output buses to continue processing instructions. Three different CPU-sets are available with the SDM-FT:

- CPU-set with 128 Mbyte dynamic RAM
- CPU-set with 256 Mbyte dynamic RAM
- CPU-set with 512 Mbyte dynamic RAM

The input output areas contain duplicate input output hardware in active standby mode. The disk drives in the CPU-core, switch activity to the inactive hardware if the active hardware has a failure. The switch over is transparent. The disk drives in both input and output areas are always active. The disk drive software performs fault checking on the standby input output hardware to provide advance indication of any hardware failure.

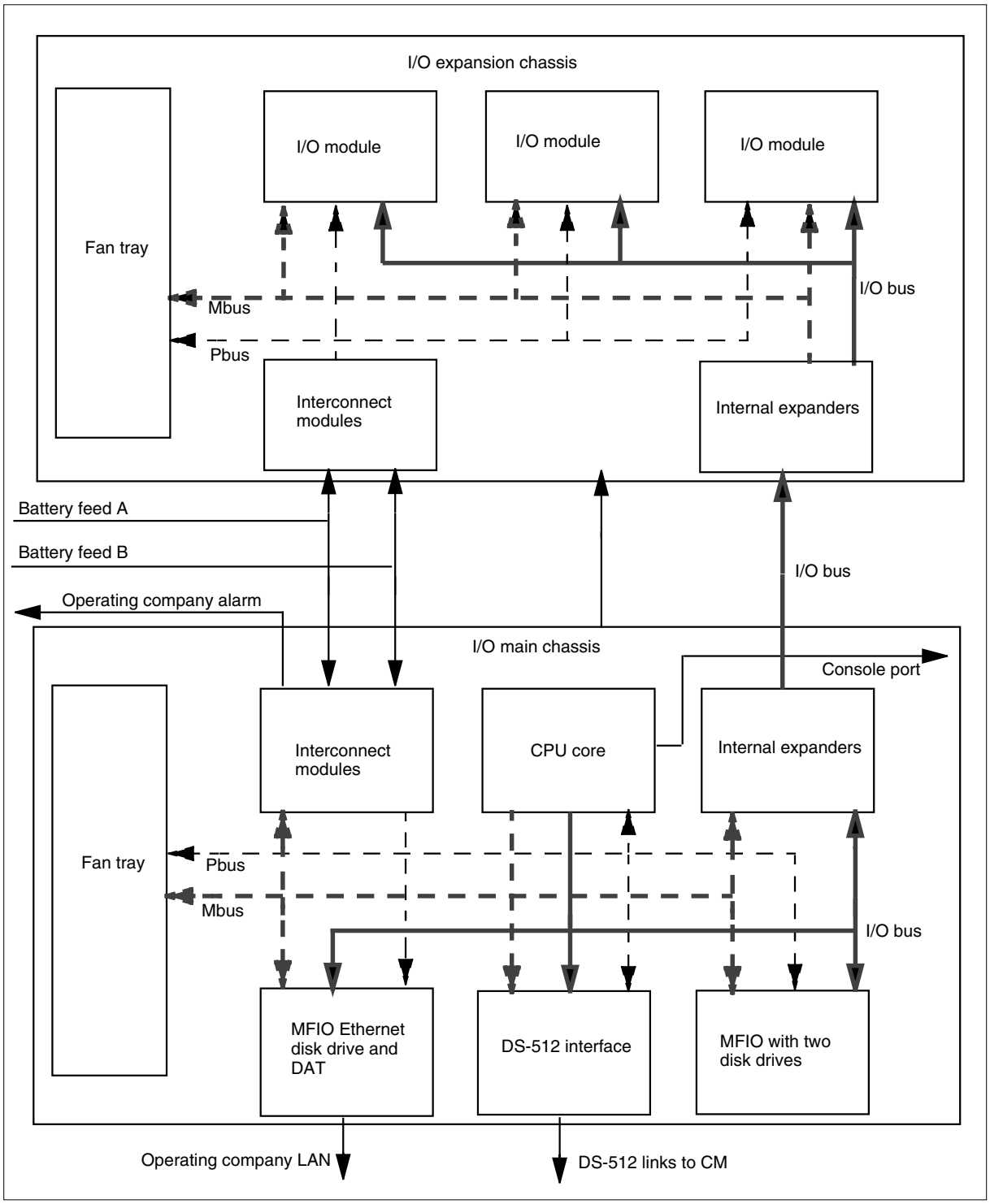
### Block diagram

The next diagram provides a diagram that displays the major functional blocks of the NTRX50FA.

Legend for the block diagram:

- Mbus (maintenance bus)
- Pbus (power bus)
- I/O module (input output module)
- DAT (digital audio tape)
- MFIO (multi-function input output)

### NTRX50FA functional block diagram



## NTRX50FA (continued)

### Main chassis

The main chassis contains a mid-mount backplane, sixteen 25.4 mm front (controller) slots and sixteen 25.4 mm back (personality) slots. Use multiple slots for modules requiring additional space. The center six slots on the front are dedicated for three double wide CPU-sets which form the CPU-core. The SDM-FT CPU-core is equipped with two CPU-sets. The five remaining slots on either side form the two input output areas.

### Expansion chassis

The optional expansion chassis extends the main chassis input output areas and provides additional input output slots. The expansion chassis is identical to the main chassis, except for the backplane. The backplane in the expansion chassis does not contain any CPU-sets. Like the main chassis, the expansion chassis accepts controller modules at the front side and personality modules at the back side.

### Input output bus

The input output bus provides the primary path between the CPU-core and the input output subsystems. There are two identical input output busses, each routed to one of two redundant input output subsystems, forming two separate input output areas. The input output bus connects to the expansion chassis through internal expanders and flexible cables.

### Maintenance bus

The maintenance bus includes signals required to monitor and control modules in the system. The maintenance bus occurs by the CPU-set and used by all other modules in the system including the CPU-set. There are two identical maintenance buses, each routed to one of two maintenance areas. The maintenance buses can be internal or external. Signals rout from the CPU-core to all other modules that are in the chassis. The expansion chassis routes its maintenance bus to its modules in the same way. The maintenance buses of the two chassis connect through external flexible cables.

### Power bus

The power bus includes the lines required to distribute the -48V dc supply to all system modules. Each chassis has two power busses originating from the interconnect modules. Each input output area is powered by a single power bus. The CPU-core is powered by both power buses.

### Internal expander

Use the internal expander to extend the input output busses from the main chassis to the input output expansion chassis. Use one internal expander per input output area.

### Fan tray

Both main and expansion chassis are separately cooled by forced air. Each chassis is equipped with two fan trays each with three fans. Fan trays are powered by power bus A and B for redundancy. Each fan tray is removable, ensuring constant cooling during service to one fan tray.

The fan trays are above the card cage for the front (control) modules. The back (personality) modules are not forced air cooled. The fan trays pull air through the modules and force air out the top and back of the chassis. The fan trays interface to the backplane to receive power and maintenance bus instructions. Use filler modules in empty front slots to ensure enough airflow over active modules.

### Interconnect modules

The main and expansion chassis have an interconnect module per input output area, located at the top back of the chassis. Install the interconnect module directly into the backplane. Each interconnect module has four interfaces. Failure of the interconnect module affects the power supply to an input output area and fan tray.

### Input output modules

Main chassis input output slots 1 to 5 are mirrored in sequence to slots 12 to 16. Expansion chassis input output slots 1 to 8 are mirrored in sequence to slots 9 to 16. The input output modules can be arranged in pairs and are in corresponding slots to enable the pair to operate in active standby mode of operation.

### DS-512 interface module

The SDM-FT is supplied with a DS-512 module capable of two fiber link interfaces in each input output area. A direct fiber link is supplied by the DS-512 module between both planes of the MS and SDM-FT input output areas. Each input output area of the SDM-FT has an independent link to both MS planes. All four links are active during normal operation. In the event of a single DS-512 module failing, the remaining two links provide redundant connectivity between the SDM-FT and the MS. Both the front and back modules are in single slots.

### Multi-function input output module

The multi-function input output module uses a small computer system interface (SCSI) and an Ethernet interface. The SCSI interface is local to the multi-function input output module. Each multi-function input output module provides space for up to two SCSI devices. The SCSI devices can be two 3.5-in. disk drives or one 3.5 in. disk drive and a 5.25-in. media drive.

## **NTRX50FA** (continued)

Available versions of the multi-function input output module are:

- multi-function input output module with 2 GB disk drive, DAT drive and Ethernet
- multi-function input output module with two 2 GB disk drives and Ethernet

The minimum SDM-FT hardware configuration must have two multi-function input output modules, each with a 2 GB disk, DAT drive and Ethernet.

## Technical content

This section provides technical content information for the SDM-FT.

### Main chassis technical content

Physical dimensions for the main chassis are:

- Height: 533 mm (21 in.)
- Width: 482 mm (19 in.)
- Depth: 541 mm (21.3 in.)
- Weight: 91 kg (200 lb.)

Electrical specifications for the main chassis are:

- DC inputs: 2 total, 1 per power bus
- DC input voltage: -36 to -72 VDC

Environmental specifications for the main chassis are:

- Operating temperature: 0 to 38°C (32 to 100.4°F)
  - 0 to 50° C (32 to 122°F) up to 72 consecutive h
- Non-operating temperature: -55 to +85° C (-67 to 185° F)

Humidity specifications for the main chassis are:

- Operating: 20% to 80% (non-condensing)
- Operating: 10% to 80% (non-condensing up to 72 consecutive h)
- Non-operating: 5% to 90% (non-condensing)

Equipment grounding for the main chassis are:

- network equipment building system (NEBS) 4.7
- Isolated frame ground, logic ground and battery return

Acoustic noise level for the main chassis is:

- 60 dBA configured

### Expansion chassis technical content

Physical dimensions for the expansion chassis are:

- Height: 533 mm (21 in.)
- Width: 482 mm (19 in.)
- Depth: 541 mm (21.3 in.)
- Weight: 91 kg (200 lb.)

Electrical specifications for the main chassis are:

- DC inputs: 2 total, 1 per power bus
- DC input voltage: -36 to -72 VDC

Environmental specifications for the expansion chassis are:

- Operating temperature: 0 to 38°C (32 to 100.4°F)
  - 0 to 50°C (32 to 122°F) up to 72 consecutive h
- Non-operating temperature: -55 to +85°C (-67 to 185°F)

Humidity specifications for the expansion chassis are:

- Operating: 20% to 80% (non-condensing)
- Operating: 10% to 80% (non-condensing up to 72 consecutive h)
- Non-operating: 5% to 90% (non-condensing)

Equipment grounding for the expansion chassis are:

- network equipment building system (NEBS) 4.7
- Isolated frame ground, logic ground and battery return

Acoustic noise level for the expansion chassis is:

- 60 dBA configured

# NTRX54AA

## Product description

The fan power control and filter card (FPC/F) receives A and B feed inputs from the (cabinetized) power distribution center (C)PDC. The FPC/F provides a combined, filtered, voltage and current limited C-feed for 48 V (dc) fans and an alarm output. The card can operate at -48 and -60V (dc) input in a central office (CO) environment.

The card includes two faceplate mounted fuse holders that have 5A fuses and a light-emitting diode (LED). A captive screw provides positive retention and conductive coupling to the shelf. The captive screw attaches to the faceplate.

### Location

The FPC/F card is in the last two card positions in a modular supervisory panel (MSP). The FPC/F card is fully connectorized. The FPC/F provides A and B feed inputs through two 6.35 mm (0.25 in.) quick connect plugs (A0381899). The FPC/F provides power/alarm output through an 18-pin Positronics power-lok connector (A0380977).

## Functional description

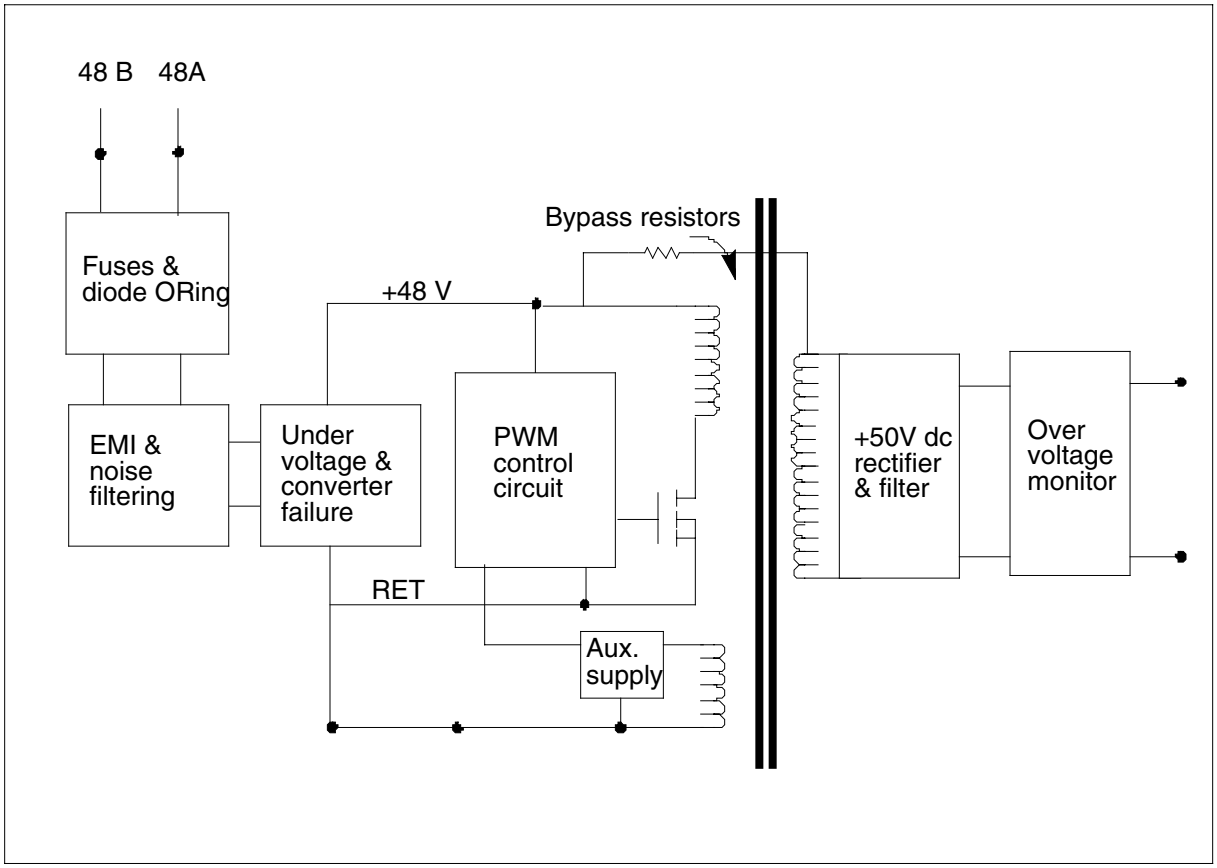
The FPC/F card provides a nominal regulated 48V for fan operation. This card also provides filtering for noise that the fans generate. Features include:

- 48 and 60V compatible
- dual battery feeds for redundancy
- regulated output voltage
- battery noise filter
- current limiter
- continuous fan power in the event of converter failure
- continuous fan in the event of under-voltage or over-voltage
- fail safe over-voltage
- alarm indication through alarm signal and LED in the event of over-voltage, under-voltage, fuse failure, or converter failure

### Functional blocks

The functional blocks of the FPC/F card appear in the following figure.

**NTRX54AA functional blocks**




## Fuses and diode ORing

Each of the two incoming feeds to the power supply are fused separately. After the feeds are fused, feeds are diode ORed to provide a combined feed. The diodes are available in Battery (BAT) and Battery Return (RTN) lines. This condition provides two functions: true redundancy and isolation of feeds from each other.

## EMI and noise filtering

A common-mode electromagnetic interference (EMI) filter reduces noise that can return to the source. A differential mode filter reduces switching noise that can return to the source.

## **NTRX54AA** (continued)

### Under-voltage monitor and converter failure

The following conditions can occur when the power converter shuts down the activation of the fans:

- An under-voltage condition can occur at the input of the power converter. In this condition, the power converter shuts down. The bypass resistors provide power to the fans.
- A fault condition can occur in the power converter and cause a blown power protection fuse. In this condition, the power converter shuts down. The bypass resistors provide power to the fans.

### Power processing

This converter incorporates a power metal oxide semiconductor field effect transistor (MOSFET) in a single flyback mode. The control method is a constant frequency current mode with pulse-width modulation. A current resistor senses the MOSFET current and the output current.

### Power transformer, rectifier, and filter

The power transformer converts the input voltage to the required output voltage. The MOSFET switches the dc voltage with the pulse width modulation (PWM) controller across the power transformer. The power transformer is reflected to the secondary of the transformer. The output rectifier converts this voltage. Output capacitors provide correct filtering for this voltage.

### Output over-voltage

An output over-voltage shutdown feature is available. If the regulated output voltage rises above a fixed level, the system sends a signal to the modulator to shut down the converter. If an over-voltage occurs, fan power continues. The bypass resistors provide power to the fans.

## Signaling

Three connectors are available: the P1 Input, P2 Input, and the J1 output. These connectors are on the rear of the NTRX54AA. The following table describes the pin numbers of the P1 Input (battery A) connector.

**Power input (P1) connector**

| Connector number | Signal | Function | Description |
|---|---|---|---|
| P1 / A, B | L - (A) | Input | -48 (-60) V (dc) |
| P1 / C, D | L + (A) | Input | BAT RTN |

The pin numbers of the P2 Input (battery B) connector appear in the following table.

**Power input (P2) connector**

| Connector number | Signal | Function | Description |
|---|---|---|---|
| P2 / A, B | L - (B) | Input | -48 (-60) V (dc) |
| P2 / C, D | L + (B) | Input | BAT RTN |

The pin numbers of the J1 Output (18-pin) connector appear in the following table.

**18-pin output (J1) connector**

| Pin number | Signal | Function | Description |
|---|---|---|---|
| 1 - 9 | L - (OUT) | Output | -48 (-60) V (dc) |
| 18 | FAIL | Output | O/C -> BR through 3.0 k and LED on output failure causes Frame Fail to alarm module |
| 10 - 17 | L + (OUT) | Output | BAT RTN from fans |

## Technical data

This section describes the technical specifications for the FPC/F card. These specifications include power requirements, environmental conditions, and equipment dimensions.

## NTRX54AA (continued)

### Power requirements

The input power requirements for the FPC/F card appear in the following table.

**Power input requirements(A and B)**

| | Limits | | |
|---|---|---|---|
| | | Alarm | |
| **Signal** | **Norm** | **Minimum** | **Maximum** |
| Voltage | -48/-60V (dc) | -39V (dc) | -71V (dc) |
| Current | | | 2.0 A |
| Noise to battery | | | 13 dBrnC |
| ***Note:*** Noise-to-battery is measured at nominal input voltage. | | | |

The output power requirements for the FPC/F card appear in the following table.

**Power output requirements(A and B)**

| | Limits | | |
|---|---|---|---|
| | | Alarm | |
| **Signal** | **Norm** | **Minimum** | **Maximum** |
| Voltage | -48V (dc) | -44V (dc) | -52V (dc) |
| Current | | | 1.5 A |
| Current limit | 1.6 A | 1.5 A | 1.7 A |
| Over-voltage disconnect threshold | -56.3V (dc) | -55.2V (dc) | -57.5V (dc) |

## Environmental conditions

The FPC/F card performs under limited environmental conditions. These limited conditions appear in the following table.

**Ambient conditions**

| Condition | Operating range | Short-term range |
|---|---|---|
| Temperature | 0°C to 40°C<br>(32°F to 104°F) | 0°C to 50°C<br>(32°F to 122°F) |
| Humidity | 5% to 95% | N/A |

## Equipment dimensions

The FPC/F card dimensions are 101.6 mm (4 in.) in height, 60.9 mm (2.4 in.) in width, and 254 mm (10 in.) in depth. The approximate weight is 0.9 kg (2 lb).

# NTRX54BA

## Product description

The fan power control (FPC) receives A and B feed inputs from the (cabinetized) power distribution center (C)PDC. The FPC provides a combined C feed for the 48V(dc) fans and an alarm output. The card can operate at -48 and -60V (dc) input in a central office (CO) environment.

The card includes two faceplate mounted fuse holders that have 5A fuses and a light emitting diode (LED). A captive screw provides positive retention and conductive coupling to the shelf. The captive screw attaches to the faceplate.

### Location

The FPC card is in the last two card positions in a modular supervisory panel (MSP). The FPC card is connectorized. The card provides A and B feed input through two 6.35 mm (0.25 in.) quick connect plugs (A0381899). The card also provides power/alarm output through an 18–pin Positronics power–lok connector (A0380977).

## Functional description

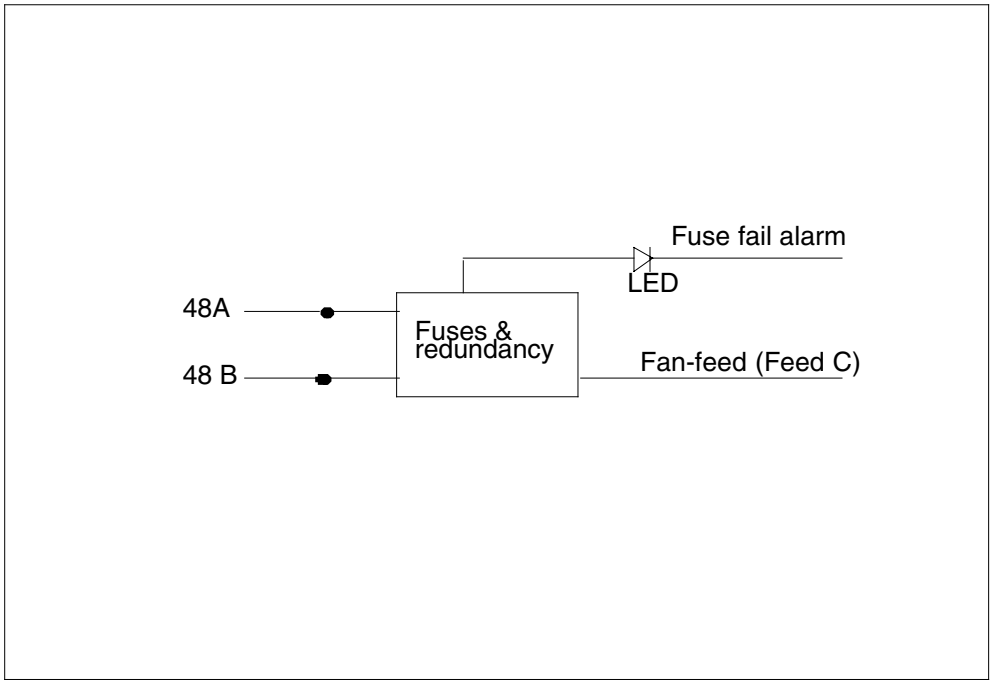
The FPC card provides a nominal regulated 48V for fan operation. Features include:

- fuse failure alarm
- redundant feed operation

### Functional blocks

The functional blocks of the FPC card appear in the following figure.

**NTRX54BA functional blocks**




### Feed combining

This functionality combines feeds A and B to provide redundancy. If one of the feeds is not present, the other feed supplies the power.

### Fuse fail alarm

This alarm provides an alarm indication if a fuse failure occurs.

## Signaling

Three connectors are available: the P1 Input, P2 Input, and the J1 output. These connectors are available on the rear of the NTRX54BA . The pin numbers of the P1 Input (battery A) connector appear in the following table.

**Power input (P1) connector**

| Connector number | Signal | Function | Description |
|---|---|---|---|
| P1 / A, B | L - (A) | Input | -48V (dc) |
| P1 / C, D | L + (A) | Input | BAT RTN |

## **NTRX54BA** (continued)

The pin numbers of the P2 Input (battery B) connector appear in the following table.

**Power input (P2) connector**

| Connector number | Signal | Function | Description |
|---|---|---|---|
| P2 / A, B | L - (B) | Input | -48V (dc) |
| P2 / C, D | L + (B) | Input | BAT RTN |

The pin numbers of the J1 Output (18–pin) connector appear in the following table.

**18–pin output (J1) connector**

| Pin number | Signal | Function | Description |
|---|---|---|---|
| 1 - 9 | L - (FAN1) | Output | -48V (dc) |
| 18 | FAIL | Output | O/C -> BR through 3.0 k and LED on output failure causes Frame Fail to alarm module |
| 10 - 17 | L + (FAN) | Output | BAT RTN from fans |

## Technical data

This section describes the technical specifications for the FPC card. These specifications include power requirements, environmental conditions, and equipment dimensions.

## Power requirements

The input power requirements for the FPC card appear in the following table.

**Power input requirements(A and B)**

| | Limits | | |
|---|---|---|---|
| | | Alarm | |
| **Signal** | **Norm** | **Minimum** | **Maximum** |
| Voltage | -48V (dc) | -39V (dc) | -56V (dc) |
| Current | 1.5A | | 2.5A |

The output power requirements for the FPC card appear in the following table.

**Power output requirements(A and B)**

| | Limits | | |
|---|---|---|---|
| | | Alarm | |
| **Signal** | **Norm** | **Minimum** | **Maximum** |
| Voltage | -48V (dc) | | -56V (dc) |
| Current | 1.5A | 0.0A | 3.0 A |

## Environmental conditions

The FPC card performs under limited environmental conditions. These limited conditions appear in the following table.

**Ambient conditions**

| Condition | Operating range | Short-term range |
|---|---|---|
| Temperature | 0°C to 50°C | N/A |
| | (32°F to 122°F) | N/A |
| Humidity | 5% to 95% | N/A |

## Equipment dimensions

The FPC card dimensions are 101.6 mm (4 in.) in height, 60.9 mm (2.4 in.) in width, and 254 mm (10 in.) in depth. The approximate weight is 0.68 kg (1.5 lb).

# NTRX56AA

## Product description

The cabinetized miscellaneous equipment cabinet (CMIS) that has a zone, performs the same functions as the NT0X02AB miscellaneous equipment frame (MIS). The NTRX56AA accommodates different DMS-100 common systems and the hardware required for different equipment. Nortel Networks does not manufacture some of this equipment.

The NTRX56AA is completely provisionable so that a customer can select from a list of equipment types. The frame supervisory panel (FSP) and cooling unit (CU) are always required at the top and bottom of the NTRX56AA. If the system uses as an intermediate distribution frame, the FSP and CU are not required.

The NTRX56AA provides electromagnetic interference (EMI) compliance. The NTRX56AA provides compliance through inter-lineup connections, through shielded cables. The lines that leave the office use filtered connectors on the bulkhead.

The NTRX56AA equipment shelves differ in height. The height of the shelves is different from the standard 359 mm (14 in.) height of the DMS-100 shelves. The NTRX56AA contains eight zones. Each zone is 179 mm (7 in.) high. Each equipment is in one zone or multiple zones. Each piece of equipment has a profile plate and zone that corresponds.

## Parts

The NTRX56AA contains a collection of some of the following parts:

- A0379066 (M1-1063-901)—Pylon RG-2 ringing generator
- NTNX27CA—CU
- NTRX31AD—500W LaMarche inverter unit
- NTRX34FI—CMIS terminal block assembly
- NTRX40AA—modular supervisory panel (MSP)
- NTZZ18XA—digital alarm scanner (DAS)
- NT3J00BA—multiple loop test (MLT) applique
- NT3X25AA—common equipment shelf assembly
- NT3X25BA—terminal block assembly
- NT5X69AA—inactive system timing circuit (ISTC)
- NT5X85AA—audible/visual alarm extension unit
- NT5X86AA—audible alarm cutoff control unit

- NT7F18AD—digital test head/remote office test line unit (DTH/ROTL)
- 905-5222-001—RM4200 data set shelf 115V ac
- 905-5222-003—RM4200 data set shelf -48V dc.

### Pylon RG-2 ringing generator

The A0379066 (M1-1063-901) Pylon RG-2 ringing generator provides an RG that can mount in the NTRX56AA. The A0379066 is provisioned with the NT5X85AA audible/visual alarm extension unit.

### CU

An NTNX27CA fan unit integrated in the base of the cabinet provides the NTRX56AA with forced-air cooling.

### 500-W LaMarche inverter

The NTRX31AD 500-W LaMarche inverter provides 115V ac to units that require a 115V ac source. The inverter provides 115V ac to units mounted in the same NTRX56AA as the inverter. The NTRX31AD inverter kit contains the A0367433 LaMarche inverter. The LaMarche inverter converts the -48V nominal dc from the office battery to 115V ac.

### CMIS terminal block assembly

The following must be provided for units that do not have dedicated connector plates:

- NTRX34FI CMIS terminal block assembly
- the associated bulkhead connector mounting plate P0730995.

### Modular supervisory panel

The NTRX40AA MSP contains power control and alarm circuits. These circuits provide interfaces (I/Fs) between the power distribution center and the equipment mounted in the NTRX56AA.

The MSP provides a focal point for persons to monitor the NTRX56AA. The NTRX40AA provides alarms to warn of problems in the NTRX56AA. Problems include a CU or power inverter that does not function or functions out of an acceptable range. The MSP includes a frame fail light and an electrostatic discharge wrist strap. These parts are mounted at the front of the cabinet.

### Digital alarm scanner

The NTZZ18XA DAS hardware is available when the DMS office is required to connect with the Bell Operating Companies Switching Control Centers. The

## NTRX56AA (continued)

DAS hardware allows the J1P056A-1 DAS to mount in the NTRX56AA. Nortel Networks does not supply the DAS.

### Multiple loop test applique

The NT3J00BA MLT applique shelf can mount a maximum of ten MLT circuit packs required for loop tests.

### Common equipment shelf assembly

The NT3X25AA common equipment shelf provides multiple 115-V ac outlets. This voltage powers a maximum of two modems that stand alone. This voltage powers associated data telephone sets or other equipment that stands alone.

### Terminal block assembly

The NT3X25BA is provisioned to locally cross-connect NTRX56AA-mounted equipment, like a bank of modems.

### Inactive system timing circuit

The NT5X69AA inactive system timing circuit records the duration of system down time.

### Audible/visual alarm extension unit

The NT5X85AA audible/visual alarm extension unit is provisioned when the number of audible alarm panels NT0X66AA exceeds two. The unit is provisioned when the number of exit alarm display panels NT0X64AA exceeds four.

The M1-1063-901 Pylon RG-2 is provisioned with the NT5X85AA.

### Audible alarm cutoff control unit

The NT5X86AA audible alarm cutoff control unit is provisioned when selective audible alarm cutoff control is required. This unit can control a maximum of six audible circuits. Use the NT5X86AA with the NT5X86AB mounted from the outside audible cutoff key panel.

### Digital test head/remote office test line unit

The NT7F18AB DTH/ROTL comes complete with the circuit packs required to perform the ROTL function.

### RM4200 data set shelf 115V ac

The 905-5222-001 Case/Datatel RM4200 data set shelf can accommodate a maximum of 16 Datatel 4200 series modems. The 905-5222-001 requires a 115V ac feed, normally from the NTRX31AD inverter. A single NTRX31AD inverter can power a maximum of three 905-5222-001 modem shelves.

### RM4200 data set shelf -48V dc

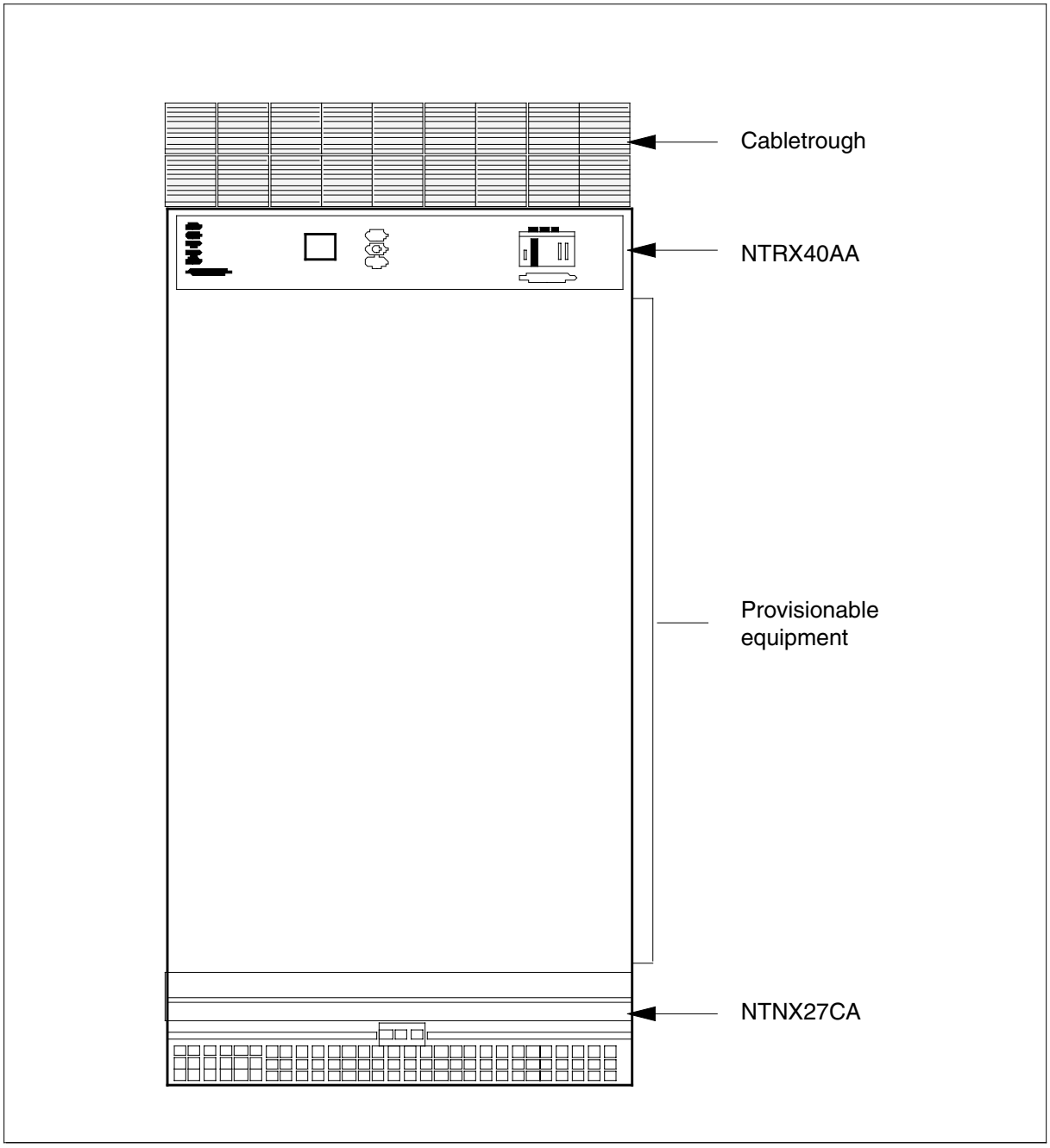
The 905-5222-003 Case/Datatel RM4200 data set shelf can accommodate a maximum of 16 Datatel 4200 series modems. The -48V dc feed from the office supply powers the 905-5222-003.

## Design

The design of the NTRX56AA appears in the following figure:

# **NTRX56AA** (end)

**NTRX56AA parts**




***Note:*** This illustration is not drawn to scale

# NTRX90AA

## Product description

The NTRX90AA cooling unit (CU) is at the bottom of the cabinetized line concentration equipment (CLCE) and the cabinetized line module ISDN (CLMI). This cooling unit includes three circulation fans that cool the shelves of the circuit cards. The circuit cards, are above the cooling unit in the cabinet. The CU is a 406 mm (16 in.) deep unit. In 48V applications, the NTRX90AA CU uses the NTRX54BA fan power control module (CM). This module is in the modular supervisory panel (MSP) of the cabinet. In 60V applications, use the NTRX54AA fan power CM. This module is in the MSP of the cabinet.

## Parts

The NTRX90AA CU is a subset of the NTRX93AA CU kit. The CU kit includes an air filter, slider brackets, a fan power/alarm cable, and the hardware to mount the NTRX90AA.

- NTRX93AA—CU kit, 406 mm (16 in.)
  - — NTRX4025—fan power/alarm cable
  - — NTRX90AA —CU, 406 mm (16 in.)
  - — A0346832—air filter, 406 mm (16 in.)
  - — P0740324—right slider bracket, 406 mm (16 in.)
  - — P0741148—left slider bracket, 254/406 mm (10/16 in.).

### Fan power/alarm cable

The NTRX4025 power connector for the CU mounts from the rear, self-aligning connector. When the unit is in position in the cabinet, the connector mates.

### Cooling unit

The NTRX90AA CU includes three circulation fans and an air filter.

### Air filter

The CU air filter A346832 serves as a flow diffuser. The air filter is in the unit, directly above the fans. The CU air filter A346832, filters particles as required. You can remove the filter for replacement. To remove the filter, slide the filter out from the front of the unit.

### Slider brackets

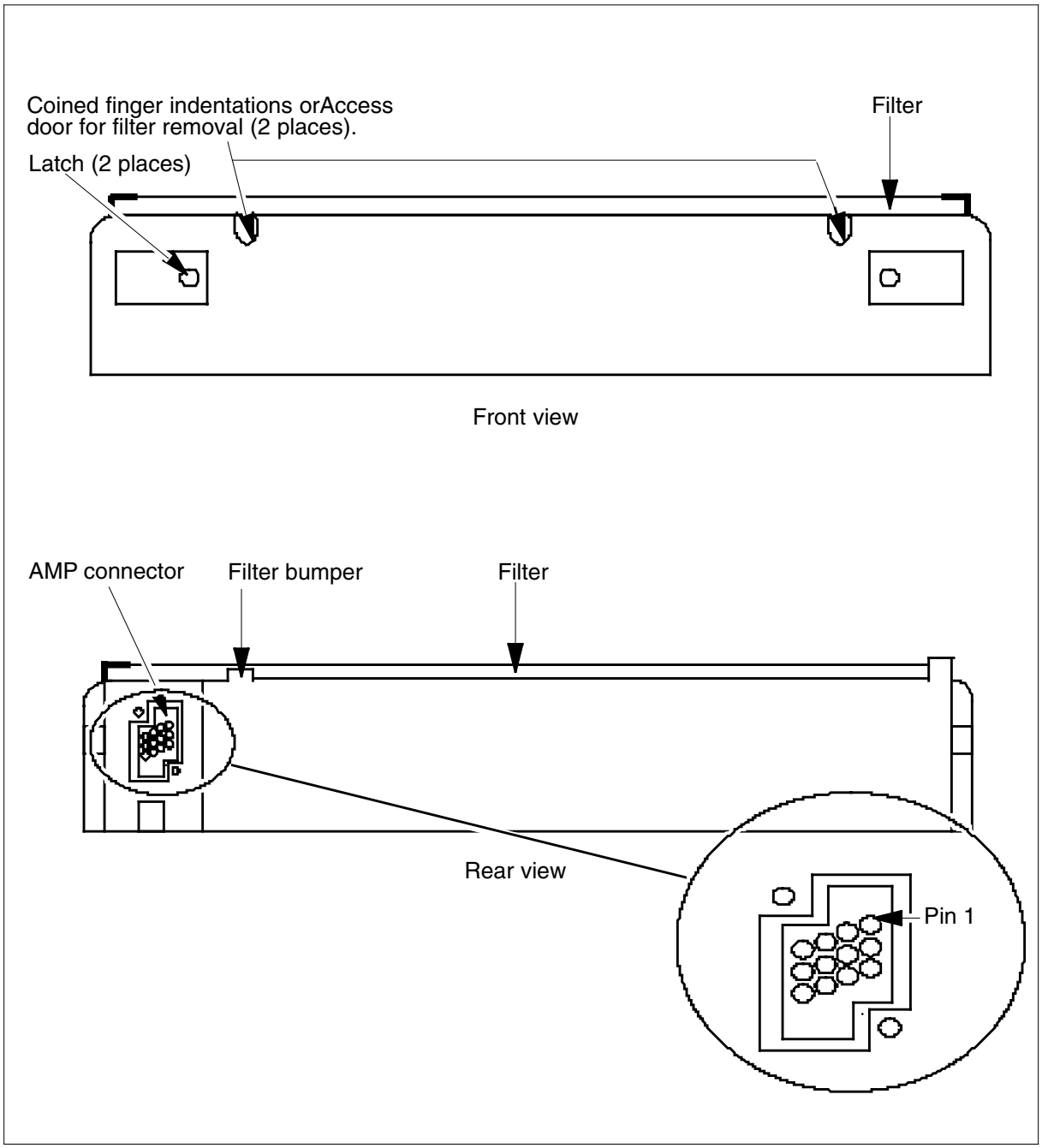
The CU uses two slider brackets: the P0740324, right slider and the P0741148, left slider. These slider brackets support the CU on each side and mount to the cabinet. The Slam-lock latches secure the CU in the operating position on the slider brackets.

## **NTRX90AA** (continued)

## Design

The design of the NTRX90AA CU appears in the following figure:

**NTRX90AA parts**



***Note:*** This illustration is not drawn to scale.

## Signaling

The power/alarm connector located on the lower left-rear of the NTRX90AA is a 12-position drawer-type connector. The following table describes the pin numbers of this connector on the NTRX90AA:

**Pin numbers**

| Pin number | Signal name |
|---|---|
| 1 | -48 V |
| 2 | BR |
| 3 | Not used |
| 4 | Not used |
| 5 | Not used |
| 6 | Not used |
| 7 | ALM output |
| 8 | ALM input |
| 9 | FRM GND |

## Technical data

The technical data section provides specifications for the NTRX90AA power requirements, equipment dimensions and environmental conditions.

### Power requirements

The NTRX90AA operates between -39.5V dc and -56V dc at a maximum of 1.75A.

### Equipment dimensions

The CU dimensions are 93 mm (3.68 in.) in height, 607 mm (23.88 in.) in width, and 416 mm (16.37 in.) in depth. The approximate weight is 11.35 kg (25 lb).

## **NTRX90AA** (end)

### Environmental conditions

The following table lists the environmental conditions required for the NTRX90AA:

**Ambient conditions**

| Condition | Operating range | Short-term range |
|---|---|---|
| Temperature | 5°C to 40°C<br>(40°F to 104°F) | 0°C to 50°C<br>(32°F to 122°F) |
| Relative humidity | 20% to 55% | 10% to 80% |

In addition to the environmental conditions expressed in the table above, the qualities of the performance and reliability parameters are defined as follows:

- A relative humidity of 80% is expected at an ambient temperature of 21°C (69.8°Φ) μαξιμυμ. Ατ αν αμβιεντ τεμπερατυρε οφ 50°C (122°F), the relative humidity is expected to be 20% maximum.
- Normal temperature and humidity ranges are defined as those that do not adversely affect the continuous operation or grade of service (GOS).
- Short term is a maximum of 72 hours continuous and no more than 180 h in one year.
- Measure temperature and relative humidity at a point: 1.5 m (5 ft.) above floor level and mid-aisle or 380 mm (15 in.) in front of the appropriate equipment.
- The CU when mounted in a cabinet meets network equipment building system (NEBS) zone 4 earthquake specifications.

# NTRX91AA

## Product description

The NTRX91AA cooling unit (CU) is at the bottom of the C28 type cabinets that require forced cooling, except the line equipment. This CU includes three circulation fans. The fans cool the shelves of the circuit cards above the CU in the cabinet. The CU is a 254 mm (10 in.) deep. In 48V applications, the NTRX91AA CU uses the NTRX54BA fan power control module (CM). This module is in the modular supervisory panel (MSP) of the cabinet. In 60V applications, use the NTRX54AA fan power CM. This module is in the MSP of the cabinet.

## Parts

The NTRX91AA CU is a subset of the NTRX92AA CU kit. The kit includes an air filter, slider brackets, a fan power/alarm cable, and the hardware to mount the unit.

- NTRX92AA—CU kit, 254 mm (10 in.)
  - — NTRX4025—fan power/alarm cable
  - — NTRX91AA—CU, 254 mm (10 in.)
  - — A0361371—air filter, 254 mm (10 in.)
  - — P0740325—right slider bracket, 254 mm (10 in.)
  - — P0741148—left slider bracket, 254/406 mm (10/16 in.).

### Fan power/alarm cable

The NTRX4025 power connector for the CU is a rear-mounted, self-aligning connector. This connector mates when the unit slides in position in the cabinet.

### Cooling unit

The NTRX91AA CU includes three circulation fans and an air filter.

### Air filter

The CU air filter A0361371 serves as a flow diffuser. The air filter is in the unit, directly above the fans. The CU air filters particles as required. You can remove the filter for replacement. To remove the filter, slide the filter out from the front of the unit.

### Slider brackets

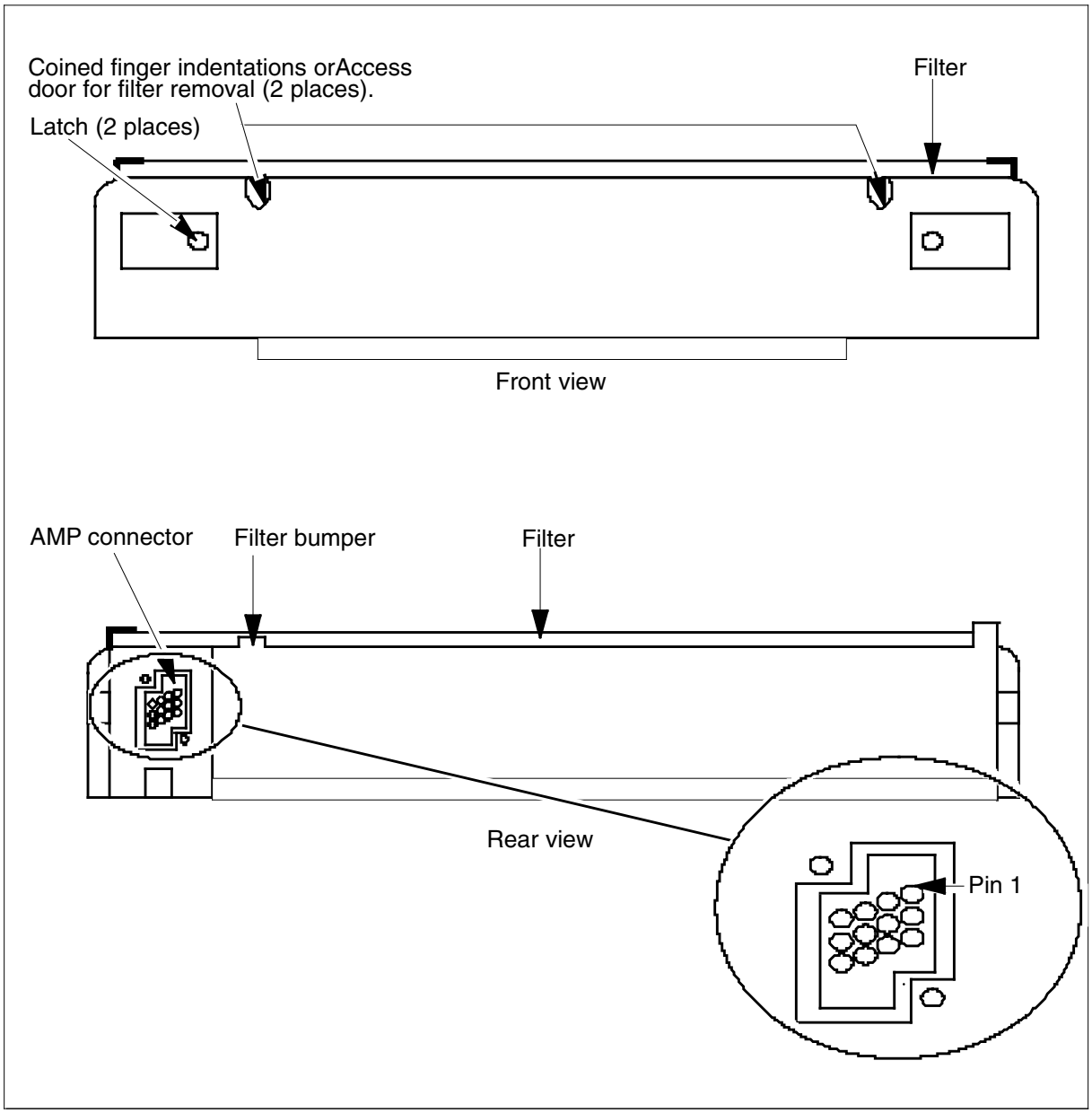
The CU uses two slider brackets: the P0740325, right slider and the P0741148, left slider. These slider brackets support the CU on each side and mount to the cabinet. The Slam-lock latches secure the CU in the operating position on the slider brackets.

## **NTRX91AA** (continued)

## Design

The design of the NTRX91AA CU appears in the following figure:

**NTRX91AA parts**




***Note:*** This illustration is not drawn to scale.

## Signaling

The power/alarm connector, on the lower left-rear of the NTRX91AA, is a 12-position drawer-type connector. The pin numbers of this connector on the NTRX91AA appear in the following table:

**Pin numbers**

| Pin number | Signal name |
|---|---|
| 1 | -48 V |
| 2 | BR |
| 3 | Not used |
| 4 | Not used |
| 5 | Not used |
| 6 | Not used |
| 7 | ALM output |
| 8 | ALM input |
| 9 | FRM GND |

## Technical data

The technical data section provides specifications for the NTRX91AA power requirements, equipment dimensions, and environmental conditions.

### Power requirements

The NTRX91AA operates between -39.5V dc and -56V dc at a maximum of 1.75A.

### Equipment dimensions

The CU dimensions are 93 mm (3.68 in.) in height, 607 mm (23.88 in.) in width, and 270 mm (10.64 in.) in depth. The approximate weight is 11.35 kg (25 lb).

## **NTRX91AA** (end)

### Environmental conditions

The following table lists the environmental conditions required for the NTRX91AA:

**Ambient conditions**

| Condition | Operating range | Short-term range |
|---|---|---|
| Temperature | 5°C to 40°C<br>(40°F to 104°F) | 0°C to 50°C<br>(32°F to 122°F) |
| Relative humidity | 20% to 55% | 10% to 80% |

In addition to the environmental conditions that appear in the table, the descriptions of the qualities of the performance and reliability parameters are:

- A relative humidity of 80% is expected at a maximum ambient temperature of 21°C (69.8°Φ). Αt αν αμβιεντ τεμπερατυρε οφ 50°C (122°F), the relative humidity is expected to be 20% maximum.
- Normal temperature and humidity ranges do not affect the continuous operation or grade of service (GOS).
- Short term is a maximum of 72 h continuous and a maximum of 180 h in one year.
- Measure temperature and relative humidity at a point 1.5 m (5 ft.) above floor level and mid-aisle. You can measure temperature and relative humidity 380 mm (15 in.) in front of the appropriate equipment. Choose the lowest point.
- The CU mounted in a cabinet meets network equipment building system (NEBS) zone 4 earthquake specifications.

# 15 NTSXnnaa

## NTSX05 through NTSX06

# NTSX05

## Product description

The NTSX05 is a PowerPC 603e–based unified processor (UP) circuit card. The NTSX05 circuit card is the main processor card for the Common Peripheral Module (CPM) and the Extended Peripheral Module (XPM+).

The NTSX05 includes two front access receptacle sockets for PCMCIA FLASH memory cards.

The NTSX05 circuit card is backward compatible with the unified processor NTMX77 and the cellular access processor NTAX74. The NTSX05 can work in one unit, while a MTX77 or NTAX74 circuit card is in the other unit. Each NTSX05 version requires a specific software version.

The three versions of NTSX05 are as follows:

- NTSX05AA
  - — CPU: 166 MHz PowerPC upgrade available up to 300MHz
- NTSX05CA
  - — based on NTSX05AA
  - — CPU: 200 MHz PowerPC upgrade available up to 300 MHz
  - — backward compatible with NTSX05AA
- NTSX05DA
  - — based on NTSX05CA
  - — CPU: 200 MHz PowerPC upgrade available up to 300 MHz
  - — full-duplex 10/100 megabit per second (Mbps) ethernet port accessible through the backpanel
  - — backward compatible with NTSX05CA and NTSX05AA

### Location

The NTSX05 is in slot 12 on the XPM+ shelf. The NTSX05 card is in each unit. On a CPM shelf, the card is in slot 3 for unit 0 and slot 25 for unit 1.

## Functional description

The NTSX05 is the main processing unit on the XPM+ and CPM shelf. This processing unit interfaces with the other circuit cards of the unit through the A-bus. The NTSX05 contains two receptacle sockets for NTSX06 PCMCIA packlets. Two other functions of the NTSX05 are unit activity control and an interface to the mate unit.

### Functional blocks

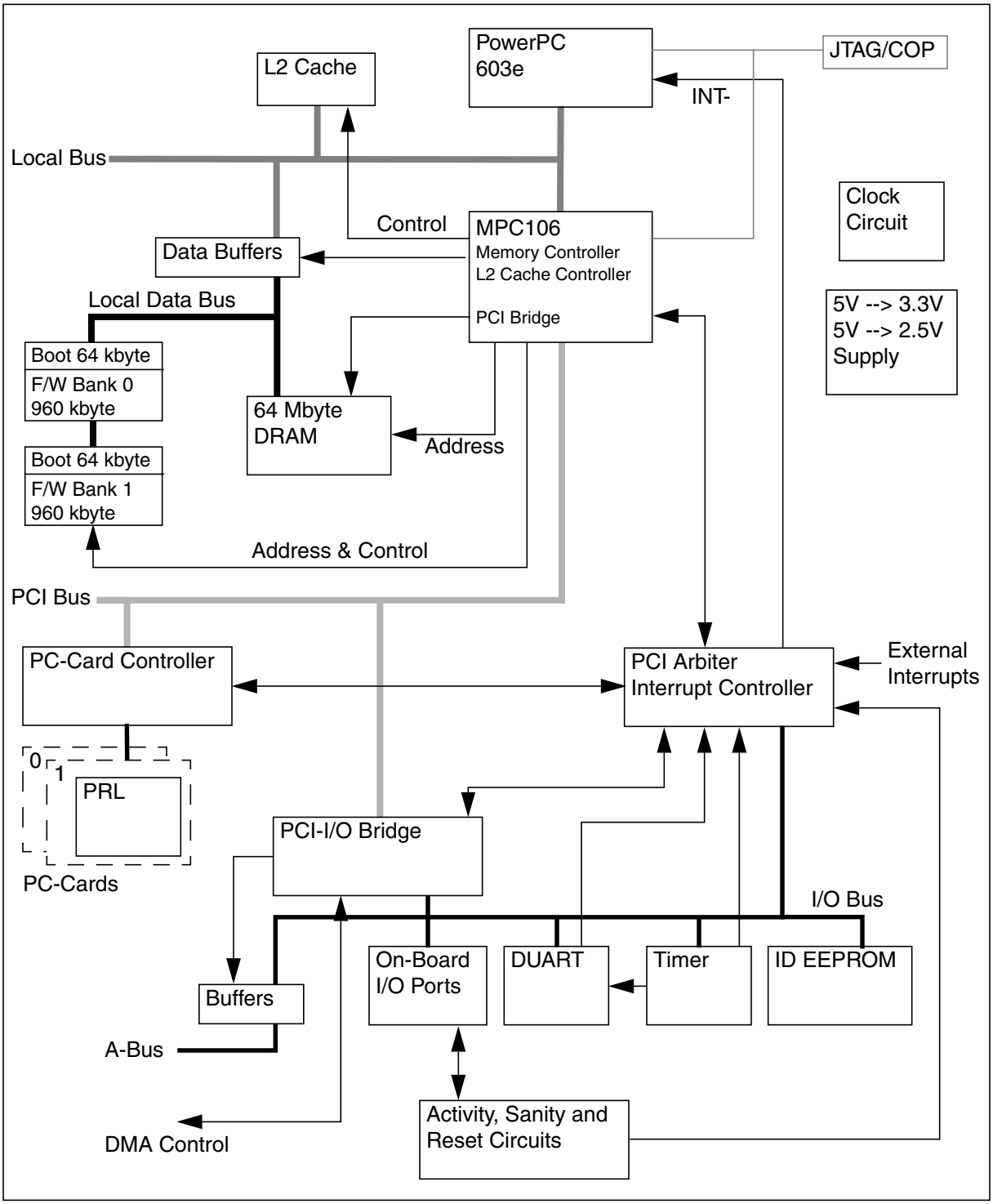
The NTSX05 contains the following functional blocks:

- CPU PowerPC 603e
- clock circuit
- PCI bridge and memory control
- FLASH EEPROMs
- ID EEPROM
- level-2 cache memory
- PC card controller and sockets
- ethernet port (NTSX05DA)
- PCI I/O bridge
- PCI arbiter
- interrupt controller
- DUART
- timer
- on-board I/O ports
  - shelf type port
  - control register
  - command port
  - status register
  - reset status register
  - general register
- sanity timer
- activity control
- reset

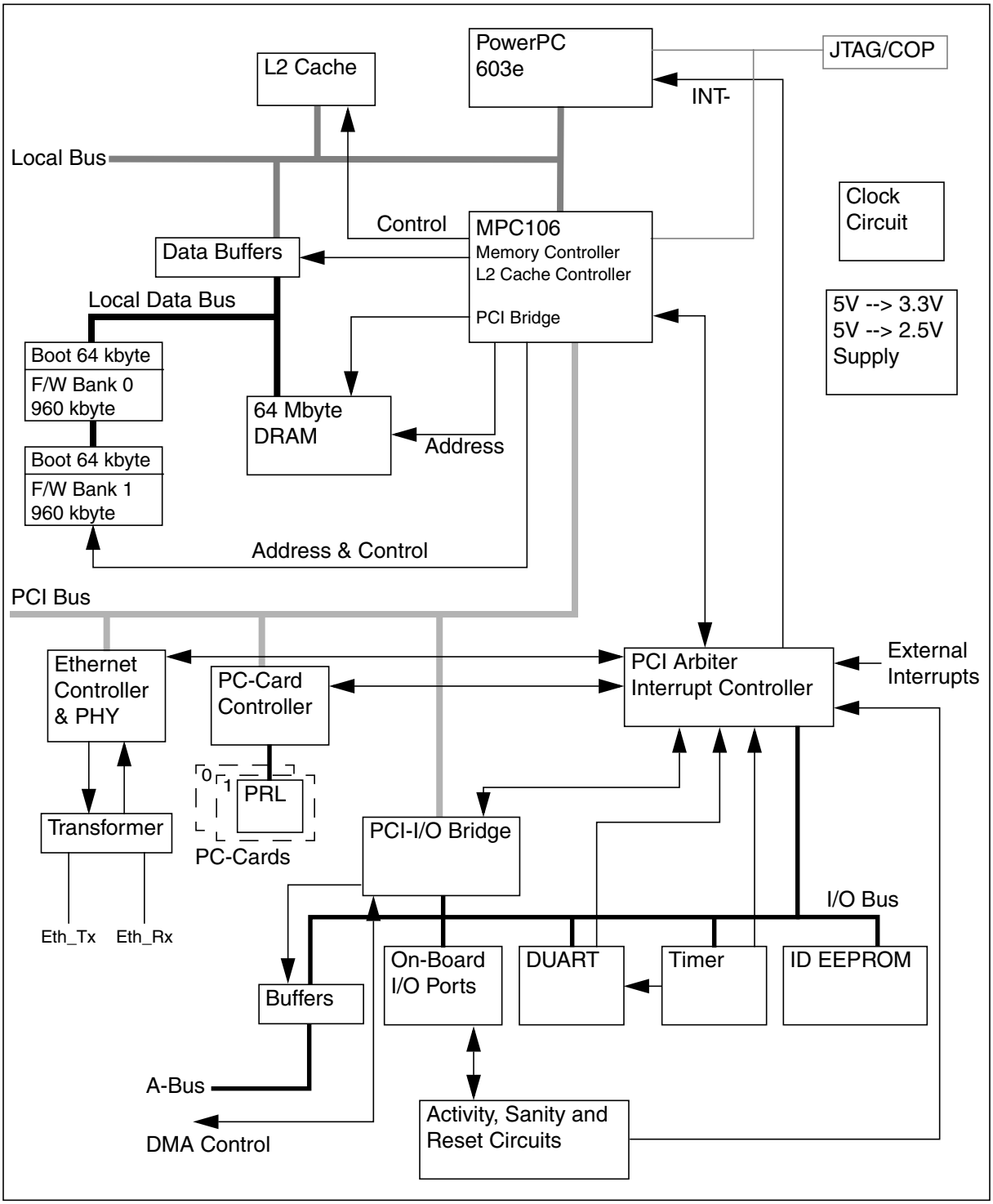
The relationship between the functional blocks appears in the following figure.

## **NTSX05** (continued)

### NTSX05AA and NTSX05CA functional blocks



**NTSX05DA functional blocks**



## **NTSX05** (continued)

### CPU PowerPC 603e

The CPU is a PowerPC 603e processor with the capacity for 64 bits of data and 32 bits of address storage.

The CPU of the NTSX05 versions operates as follows:

- NTSX05AA: CPU 166 MHz upgrade available up to 300 MHz
- NTSX05CA: CPU 200 MHz upgrade available up to 300 MHz
- NTSX05DA: CPU 200 MHz upgrade available up to 300 MHz

### Clock circuit

The clock circuit generates a clock frequency of 66.67 MHz for the 603e local bus and 32 MHz for the I/O bus.

### PCI bridge and memory control

MPC106 chip controls the PCI bridge and memory control functions.The MPC106 chip controls all accesses from the 603e processor to the DRAM, EEPROM, and level-2 cache. The MPC106 chip also controls accesses through the PCI bus to the PC cards and the PCI I/O bridge. The MPC106 accepts read/write cycles to the DRAM.

### Dynamic RAM

The system memory contains a DRAM bank. The MPC106 PCI bridge memory controller controls the DRAM bank. The bank contains 64 Mbytes using 8 Mbytes times 8 bit devices.

The DRAM is used as the main program and data store of the processor.

### FLASH EEPROM

The boot and firmware memory banks uses four identical 512 Kbytes FLASH EEPROMs times 8 bits. The MPC106 memory controller controls the EEPROMs. The four chips form two banks of 1 Mbytes each. The design supports the option of populating only the two lower chips. The two lower chips are organized as two 512 Kbytes banks.

The lower 64 Kbytes in each of the lower chips is a read-only boot sector. The other 448 kbytes plus the higher 512 Kbytes chip, is the firmware bank. The firmware bank can be either 448 Kbytes or 960 Kbytes. The size of firmware bank depends on if the two higher chips are on the board or not.

One bank is executable (read only) and the other is read writable.

### ID EEPROM

The ID EEPROM holds board identification information, such as PEC and version of the card.

### Level-2 cache memory

The level-2 cache block contains fast static RAM devices. The RAM devices functions as an intermediate stage between the level-1 cache (on the 603e chip) and the main system memory. Level-2 cache stores the code and data needed for immediate use by the processor. The size of the cache memory is up to 1 Mbyte. Configurations of 0, 256 kbyte, 512 kbyte are also supported. The MPC106 controls the level-2 cache and maintains its coherency with the level-1 cache and the DRAM.

### PC card controller and sockets

The PC card controller supports two separate PCMCIA revision 2.1 sockets. The PC card controller provides the interface between the processor and the PCMCIA packlets. The PCMCIA packlets can be either memory or I/O. The PCMCIA signals are internally buffered to allow for hot insertion and removal of the packlets. The sockets are accessed from the front.

### Ethernet port

The NTSX05DA card contains an ethernet port that is a full duplex 10/100 Mbps ethernet port accessible through the backplane. The PCI bus connected ethernet controller controls the ethernet port. The ethernet port is capable of being either a PCI master or a PCI target device. The NTSX05DA does not support the EPC card as the NTSX05CA. An additional ethernet port can be added by inserting ethernet PC card to one of the PC card slots.

### PCI I/O bridge

The PCI-I/O bridge connects the PCI bus with the I/O bus. The I/O bus is connected to the on-board I/O ports and through buffers to the A-bus. The PCI-I/O bridge provides both as a target and as a master.

As a target, the PCI-I/O bridge accepts and handles PCI transactions. The PCI transactions are initiated by the MPC106 for reading/writing from either the I/O bus or the A-bus. As a master, the PCI I/O bridge accepts and handles DMA requests from the A-bus.

The PCI I/O bridge also contains the A-bus arbiter logic. The A-bus arbiter logic gives A-bus to an external agent on DMA request.The A-bus arbiter also includes several timers to handle error problems during bus transactions.

## NTSX05 (continued)

### PCI arbiter

The PCI arbiter receives bus requests from the PCI bus masters. The PCI arbiter supports up to 4 PCI masters. The PCI masters on the NTSX05 are:

- MPC106
- PCI I/O bridge
- PC card controller
- PCI connector (for test/debug purposes only)

### Interrupt controller

The interrupt controller interfaces between the external interrupt sources and the processor. The interrupt controller contains 16 interrupt inputs that go to the same INT line toward the processor. One additional interrupt connects to the NMI (Non-Maskable-Interrupt) line towards the MPC106.

### DUART

The DUART is accessed by the processor through the PCI-I/O bridge. Two serial ports on the NTSX05 contain DUART:

- The black plane monitor provides means to connect a terminal directly to the PM backplane, using a monitor program, for debug and maintenance purposes.
- The Inter-Module-Communication (IMC) connects the NTSX05 to the processor in the mate unit.

The DUART mode of operation is programmed by the processor, and interrupts are sent to the interrupt controller when a byte is sent or received. The baud rates are generated by a programmable timer. The baud rates for the IMC link and the Backplane-monitor can be programmed independently. A loop-back feature is available for testing.

### Timer

The programmable timer chip has three counters. The counters have the following functions:

- One counter operates as a real time clock and interrupts the CPU each 10 ms.
- Two counters generate the baud rate for the DUART.

## On-board I/O ports and registers

There are several registers which control the NTSX05 operation. The registers are accessed through the PCI I/O bridge. The registers are as follows:

- shelf type port
- control register
- command port
- status register
- reset status register
- general register

### Shelf type port

The shelf type port is a 8-bit read-only port. The NTSX05 uses the shelf type port to determine the system that NTSX05 is plugged into.The NTSX05 is connected directly to an array of switches that is on the backplane. The switches indicate the system configuration.

### Control register

The control register is a 16-bit read/write register. By setting or clearing the register, the processor controls various functions of the hardware. An example of a hardware function is turn on or off the in-service LED on the faceplate. A reset clears the register.

### Command port

The command port is a write only 8-bit port. The command port is a mechanism for the processor to maintain a pulse indicating and action to be performed by circuitries in the NTSX05. The pulse affects the reset port, clear sanity timer and drop activity devices.

### Status register

The status register is a 16-bit read-only port. The register holds information about current operational conditions. An example is the power status of the mate unit. The status register bits cannot be directly adjusted by the processor, only non processor hardware controls the status register bits.

### Reset status register

The reset status register is a 8-bit read-only port. The register holds information that is related to the NTSX05 reset process. The register also holds the reset state and external refresh status bits.

### General register

The 16-bit general purpose register is a stand alone read/write register. The register is cleared during power up but not by other reset sources.

## **NTSX05** (continued)

### Sanity timer

A sanity timer protects the system from software failures. The sanity timer is a free running counter with two states. When the timer first expires, the expiration is registered and an interrupt is sent to the interrupt controller. If the timer and the first state are not cleared by another sanity expiration interval, the circuitry forces a shelf reset and an activity drop. The sanity timer cannot be disabled by the processor but the expiration time is programmable. The timer is reset from 4 sources:

- a processor access to the SanAck bit in the command port
- a unit reset
- the NTSX05 increasing activity
- forcing the SANDIS pin on the backplane to ground

### Activity control

The activity control circuit on the NTSX05 generates the activity status for the unit. The activity control generates the Active signal for the unit, and monitors the Drop, MateAct, and Active signals.

The unit starts activity when the following occurs:

- no activity drop condition is present
- the mate unit is detected to be inactive

The Drop signal is generated when the following occurs:

- processor writes to the DropAct bit in the command port
- reset of the unit

### Reset

The system sends a power up reset signal to the CPU when the following occurs:

- the NTSX05 is not fully inserted into the shelf
- power supervisor triggers one of the following:
  - — a power up
  - — +5 V power is below 4.52 V
  - — +3.3 V power is below 2.93 V
  - — +2.5 V power is below 2.23 V
- the PCI I/O bridge programmable device is not configured

The system sends a hard reset signal to the CPU when the following occurs:

- a power up reset
- a processor access to the reset port
- an external reset from the message card
- the expiration of the two sanity timer intervals

## Technical data

### Power requirements

The power supply circuits on the NTSX05 include the following:.

- The +5 V, +12 V and -12 V input circuits supplies power from the backplane to the board.
- The 5 V to 3.3 V power converter receives 5 V supply from the +5 V input circuit and supplies 3.3 V to the board. The 3.3 V output can supply a maximum of 7 A.
- The 5 V to 2.5 V power converter receives 5 V supply from the +5 V input circuit and supplies 2.3 V to the board. The 2.5 V output can supply a maximum of 3 A.

## Signaling

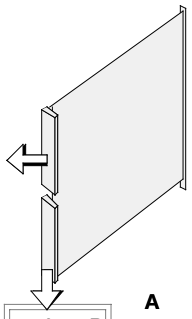
### Pin numbers

The pin numbers for NTSX05 appear in the following figure.

# **NTSX05** (end)

### NTSX05 pin numbers

| | | A | B |
|---|---|---|---|
| 1A | 1B | GND | GND |
| 2A | 2B | +5V | +5V |
| 3A | 3B | +5V | +5V |
| 4A | 4B | +5V | +5V |
| 5A | 5B | SENSA-* | GND |
| 6A | 6B | BREQ- | BGOUT- |
| 7A | 7B | BUSGI- | MODRST- |
| 8A | 8B | ACTIVE0- | MSGRST- |
| 9A | 9B | BUSBSY- | MATECLKFAIL** |
| 10A | 10B | 32MHz | |
| 11A | 11B | GND | ACTIVE1-** |
| 12A | 12B | DAS- | AS+* |
| 13A | 13B | LDS- | 16MHz |
| 14A | 14B | DTACK- | |
| 15A | 15B | UDS- | |
| 16A | 16B | RDWRT- | SANDIS-*** |
| 17A | 17B | 8MHz | |
| 18A | 18B | RSTIN-* | |
| 19A | 19B | PERINT0-* | |
| 20A | 20B | PERINT1- | MSGIRQ- |
| 21A | 21B | PERINT2-* | ECS-* |
| 22A | 22B | GND | MATEPWRFAIL- |
| 23A | 23B | PERINT3-* | RMC- |
| 24A | 24B | PERINT4-* | |
| 25A | 25B | PERINT5-* | MATEACT- |
| 26A | 26B | PERINT6-* | OWNACT- |
| 27A | 27B | PERINT7-* | GND |
| 28A | 28B | | |
| 29A | 29B | ADDR1 | |
| 30A | 30B | ADDR2 | APV+12* |
| 31A | 31B | ADDR3 | |
| 32A | 32B | ADDR4 | |
| 33A | 33B | ADDR5 | HACKOUT* |
| 34A | 34B | GND | HDOUT |
| 35A | 35B | ADDR6 | HDIN |
| 36A | 36B | ADDR7 | BPV+12* |
| 37A | 37B | ADDR8 | TACKIN* |
| 38A | 38B | ADDR9 | TDOUT* |
| 39A | 39B | ADDR10 | TDIN* |
| 40A | 40B | ADDR11 | GND |



| | | A | B | |
|---|---|---|---|---|
| 41A | 41B | GND | BERR-* | |
| 42A | 42B | ADDR12 | DS-* | |
| 43A | 43B | ADDR13 | DSACK0-* | |
| 44A | 44B | ADDR14 | EPCRST-*** | |
| 45A | 45B | ADDR15 | CKFAIL** | |
| 46A | 46B | ADDR16 | BREAK-* | |
| 47A | 47B | ADDR17 | GND | |
| 48A | 48B | ADDR18 | ST3* | |
| 49A | 49B | ADDR19 | ST2* | |
| 50A | 50B | ADDR20 | ST1* | |
| 51A | 51B | ADDR21 | ST0* | |
| 52A | 52B | ADDR22 | | |
| 53A | 53B | GND | | |
| 54A | 54B | PWRSTAT-* | | |
| 55A | 55B | ETH_RX+* | ETH_RX-* | (NTSX05DA) |
| 56A | 56B | ETH_TX+* | ETH_TX-* | (NTSX05DA) |
| 57A | 57B | | ADDR0* | |
| 58A | 58B | DATA0 | ACTIVE3-*** | |
| 59A | 59B | DATA1 | GND | |
| 60A | 60B | DATA2 | DCHFAIL-** | |
| 61A | 61B | DATA3 | ACTIVE2-** | |
| 62A | 62B | DATA4 | | |
| 63A | 63B | DATA5 | | |
| 64A | 64B | GND | | |
| 65A | 65B | DATA6 | | |
| 66A | 66B | DATA7 | | |
| 67A | 67B | DATA8 | | |
| 68A | 68B | DATA9 | | |
| 69A | 69B | DATA10 | | |
| 70A | 70B | DATA11 | GND | |
| 71A | 71B | DATA12 | UNIT0-* | |
| 72A | 72B | DATA13 | ST0 | |
| 73A | 73B | DATA14 | ST1 | |
| 74A | 74B | DATA15 | ST2 | |
| 75A | 75B | SWACK+ | ST3 | |
| 76A | 76B | SENSB- | ST4 (CPMXPM-) | |
| 77A | 77B | +12V | +12V | |
| 78A | 78B | GND | GND | |
| 79A | 79B | -12V | -12V | |
| 80A | 80B | GND | GND | |

**Legend**

* disconnected from CPM backplane, valid only for XPM+
** disconnected from XPM+ backplane, valid only for CPM
*** disconnected from CPM and XPM+ backplane

Note: on XPM+ the pin number 8A is BGOUT- and 6B is ACTIVE0-

# NTSX06

## Product description

The NTSX06 FLASH memory cards provide additional memory to allow the Common Peripheral Module (CPM) or the Extended Peripheral Module (XPM+) to load the main memory code again from the local FLASH ROM. The NTSX06 FLASH memory cards conform to the Personal Computer Memory Card International Association (PCMCIA) standards.

The three NTSX06 FLASH memory cards are as follows:

- NTSX06AA
  - — a filler card that has no functionality
- NTSX06BA
  - — 64 Mbyte peripheral (PRL) memory packlet
- NTSX06CA
  - — 128 Mbyte PRL memory packlet

### Location

The NTSX06 packlets are in the two front access receptacle slots in the faceplate of the NTSX05 processor card.

# 16 NTTRnnaa

## NTTR40AA through NTTR87AA

# NTTR40AA

## Product description

The Star Remote Module Outside (SRMO) cabinet is designed for outside use. The SRMO cabinet contains the Star Module. The Star Module is a very small remote that connects to the Star Hub.

The SRMO cabinet supports the following line types connected to the line cards:

- integrated services digital network (ISDN)
- coin
- Meridian business set (MBS)
- plain old telephone service (POTS)

The SRMO cabinet is mounted on a concrete pad, wood pole, or wood deck.

## Parts

The NTTR40AA includes the following components:

- telephony subsystem (TSS), including all the telephony electronics
- cabinet structure, including front access door and top cover
- power equipment, including 100 V ac/220 V ac to 50 V dc rectifier and four 12 V batteries, and ac power panel
- environmental controls, including fans, heaters, temperature sensors, humidity sensors, and thermostats
- optional transmission components, including support for an LTU for fiber optic or copper termination and a fiber optic organizer

### Telephony subsystem

The telephony subsystem includes a

- backplane
- seven main distribution frame (MDF) blocks
- converter and ringer card (NTTR72AA)
- line maintenance unit (NTTR71AA)
- Star Module Controller (SMC) processor card (NTTR70AA)
- card cage and up to 64 line cards
- four electromagnetic interference (EMI) filter cards (NTTR66AA)
- dc panel (NTTR67AA)

### Cabinet structure

The cabinet is a closed design, having no ventilation. The cabinet has a front door and a decorative roof. Vent holes in the battery compartment allow battery gases to vent to the outside. Access to the cabinet is through the front door only.

### Power equipment

The power equipment in the SRMO cabinet includes the following:

- ac panel, including a main ac breaker, ac power outlet, and rectifier breaker
- ac/dc rectifier
- batteries that provide 48 V standby power

### Environmental controls

The following environmental control devices are provided to enable the equipment in the cabinet to operate in different weather conditions

- two 90 mm circulation fans
- one 50 W heater located under the battery compartment to warm the batteries in low temperature conditions
- one 100 W heater located under the TSS to warm the TSS cards in low temperature conditions
- thermostats to control heaters in low temperature conditions and to control power converters in high temperature conditions
- temperature sensors to measure cabinet and battery compartment temperatures for battery voltage compensation
- humidity sensor located on the LMU

### Transmission equipment

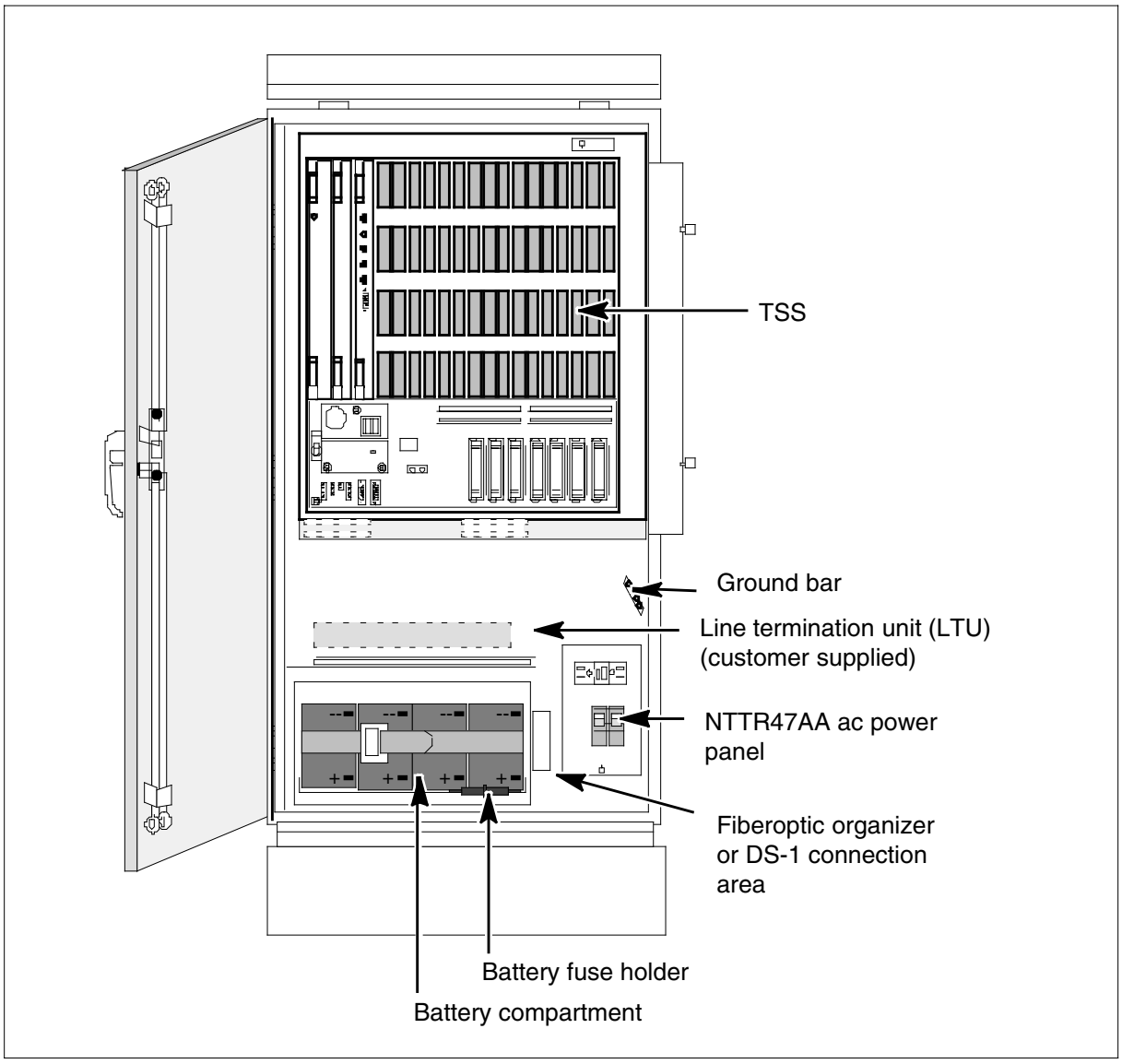
Space is available for one line termination unit (LTU).

## Design

The following figure shows the design of NTTR40AA.

# **NTTR40AA** (end)

### NTTR40AA components



# NTTR45AA

## Product description

The Star Remote Module Equipment (SRME) cabinet is designed for inside use. The SRME cabinet contains the Star Module. The Star Module is a very small remote that connects to the Star Hub.

The SRME cabinet supports the following line types connected to the line cards:

- integrated services digital network (ISDN)
- coin
- Meridian business set (MBS)
- plain old telephone service (POTS)

The cabinet mounts on a wall.

## Parts

NTTR45AA includes the following components:

- telephony subsystem (TSS), including all the telephony electronics
- cabinet structure, including TSS wall mount frame and front access cover
- power equipment, including 100 V ac/220 V ac to 50 V dc rectifier and four 12 V batteries

### Telephony subsystem

The telephony subsystem includes a

- backplane
- seven main distribution frame (MDF) blocks
- converter and ringer card (NTTR72AA)
- line maintenance unit (NTTR71AA)
- Star Module Control (SMC) processor card (NTTR70AA)
- card cage and up to 64 line cards
- four electromagnetic interference (EMI) filter cards (NTTR66AA)
- dc panel (NTTR67AA)

### Cabinet structure

The SRME cabinet consists of a front decorative cover and the wall mount frame that houses the TSS. The cabinet ventilation uses natural convection

## **NTTR45AA** (end)

through openings at the bottom of the front door and the top of the enclosure. Access to the TSS electronics is through the lift–off front cover.

### Power equipment

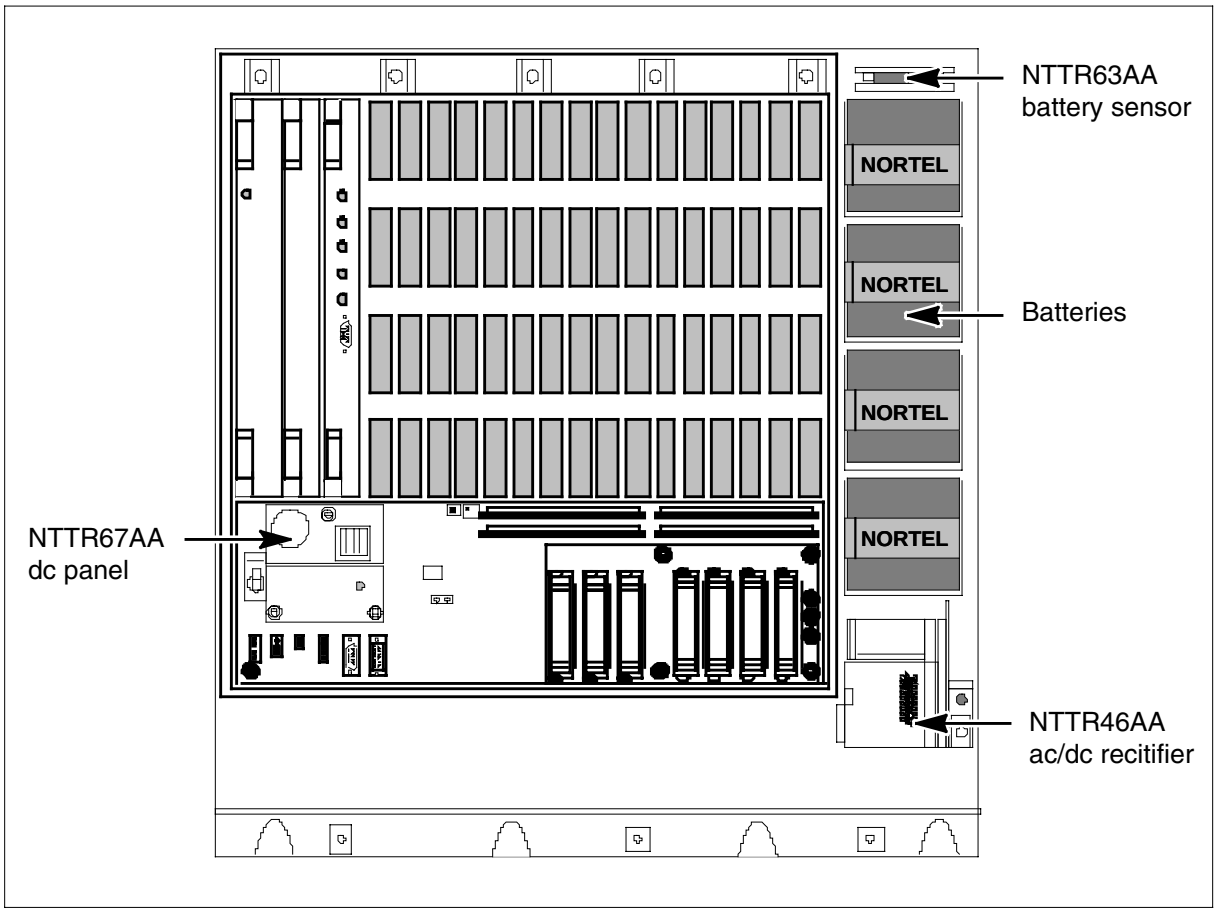
The power equipment in the SRME cabinet includes the following:

- ac/dc rectifier
- batteries that provide 48 V standby power

## Design

The following figure shows the layout of NTTR45AA.

**NTTR45AA components**



# NTTR46AA

## Product description

The ac/dc rectifier converts the ac input power to -48 V dc required by the Star Module.

A rectifier alarm is output to the NTTR70AA Star Module Controller (SMC) card when there is a dc output failure at the rectifier because of

- ac failure
- rectifier failure
- ac circuit breaker trip in the ac panel

### Location

The NTTR46AA ac/dc rectifier is on the TSS cover in the SRMO cabinet. In the SRME cabinet, the rectifier is below the batteries.

## Functional description

NTTR46AA includes the functional blocks that follow:

- input electromagnetic interference (EMI) filter, that attenuates the conducted and radiated emission signals from the converter towards the ac source
- power factor correction, that causes the input current to be sinusoidal as the input ac voltage to achieve a unity power factor
- power factor correction and converter control circuit, that causes the input current to be exactly in phase with the input voltage
- dc to dc converter, that converts the 380 V dc input voltage to a rectified 54 V dc, 300 W regulated output
- output overvoltage protection circuit, that detects the output overvoltage and sends to the control unit the signal to shut down the converter
- input undervoltage protection circuit, that detects the input undervoltage and sends to the control unit the signal to shut down the converter
- output EMI filter, that reduces the output ripple and noise to meet the equipment requirements for clean output voltage

## **NTTR46AA** (continued)

## Signaling

The following table identifies the connectors and the signaling that occurs through the connectors.

**NTTR46AA connectors and pins**

| Connector | Pin | Signal name |
|---|---|---|
| P1 | 1 | PHASE |
| | 2 | NEUTRAL |
| | 3 | GND |
| P2 | 1 | -48VRECT |
| | 2 | BRTN |
| | 3 | BATTEST |
| | 4 | ACFAIL |
| | 5 | RECT_TEMP1 |
| | 6 | RECT_TEMP2 |
| | 7 | FAN_TEST |

## Technical data

The following table lists the specifications of the NTTR46AA.

**NTTR46AA output specifications (Sheet 1 of 2)**

| | Minimum | Typical | Maximum | Comments |
|---|---|---|---|---|
| Voltage | -52 V dc | -54.5 V dc | -57 V dc | |
| Regulation line and load | | | 3% | |
| Noise and ripple | | | 250 mV peak to peak | dc to 20 Mhz |
| Static output current | | | 5.5 A | |
| Dynamic voltage regulation | | | 5% | 2 A output current step |
| Output current limit | 6 A | | 8 A | |
| Short circuit current | | | 10 A | |

**NTTR46AA output specifications (Sheet 2 of 2)**

| | Minimum | Typical | Maximum | Comments |
|---|---|---|---|---|
| Over voltage limits | 60 V | | 65 V | Output voltage shuts down with no automatic restart |
| Output voltage when voltage reducer is active | -44 V | | -47 V | |

## Power requirements

The power requirements for the NTTR46AA are as follows:

- input voltage
- minimum of 95 V ac
- maximum of 264 V ac
- input frequency
- minimum of 47 Hz
- maximum of 63 Hz
- input current, operating
- input current, inrush
- minimum of 10 A root mean square (rms)
- maximum of 20 A rms
- power factor correction
- minimum of .98
- maximum of 1.0

# NTTR47AA

## Product description

The NTTR47AA ac panel connects outside 110 or 220 V ac power to the Star Remote Module Outside (SRMO) cabinet. The ac panel contains the following:

- protection against electrical faults
- relay to activate and deactivate the battery heater. The relay is controlled by the NTTR70AA Star Module Controller (SMC) card.
- connections to mechanical thermostats to activate and deactivate the telephony subsystem (TSS) heater and battery heater
- green light emitting diode (LED) that indicates that ac power is available
- ac bus to distribute power
- two circuit breakers
  - — main circuit breaker, 16 A
  - — telephony equipment circuit breaker, 6 A
- ground fault protection service outlet, 10 A maximum

### Location

The NTTR47AA ac panel is mounted at the rear of the SRMO cabinet at the bottom right side.

## Functional description

NTTR47AA includes the following functional blocks:

- main breaker that provides ac input power, protects the system against major faults, and acts as a secondary protection to the line and service breakers
- rectifier breaker that protects against faults on the rectifier or the TSS
- SMC relay allows the SMC to control the battery heater operation
- thermostat TSW1 operates the TSS heater
- thermostat TSW2 protects the TSS and battery compartments from overheating

## Signaling

The following table identifies the connectors and the signaling that occurs through the connectors.

**NTTR47AA connectors and pins**

| Connector | Pin | Signal name |
|---|---|---|
| J1 | 1 | RECT_L |
| | 2 | RECT_N |
| | 3 | BAT_HTR_L |
| | 4 | BAT_HTR_N |
| | 5 | TSW1_L |
| | 6 | TSS_HTR_N |
| | 7 | RECT_GND |
| | 8 | TSW2_1 |
| | 9 | TSW2_2 |
| J2 | 1 | -48 VDC |
| | 2 | HTR_CONT |
| | 3 | +ACFAIL |
| | 4 | -ACFAIL |
| J3 | 1 | NEUTRAL |
| | 2 | GROUND |

## Technical data

This section identifies the technical data for the NTTR47AA.

## **NTTR47AA** (end)

### Power requirements

The power requirements for the NTTR47AA are as follows:

- for 110 V ac supply, the following values apply
  - — minimum of 97 V
  - — maximum of 132 V
  - — normal of 120 V
- for 230 V ac supply, the following values apply
  - — minimum of 198 V
  - — maximum of 253 V
  - — normal of 230 V

# NTTR60AA

## Product description

The ringing generator supplies ringing voltage to the line drawers. The NTTR60AA generates ringing signals and the dc voltages required for the automatic number identification (ANI) and coin functions. The ring output frequency and amplitude are set manually during installation using the four dual inline package (DIP) switches on the ringing generator card.

### Location

The NTTR60AA ringing generator card is in slots 1 and 22 of the Star Hub control shelf.

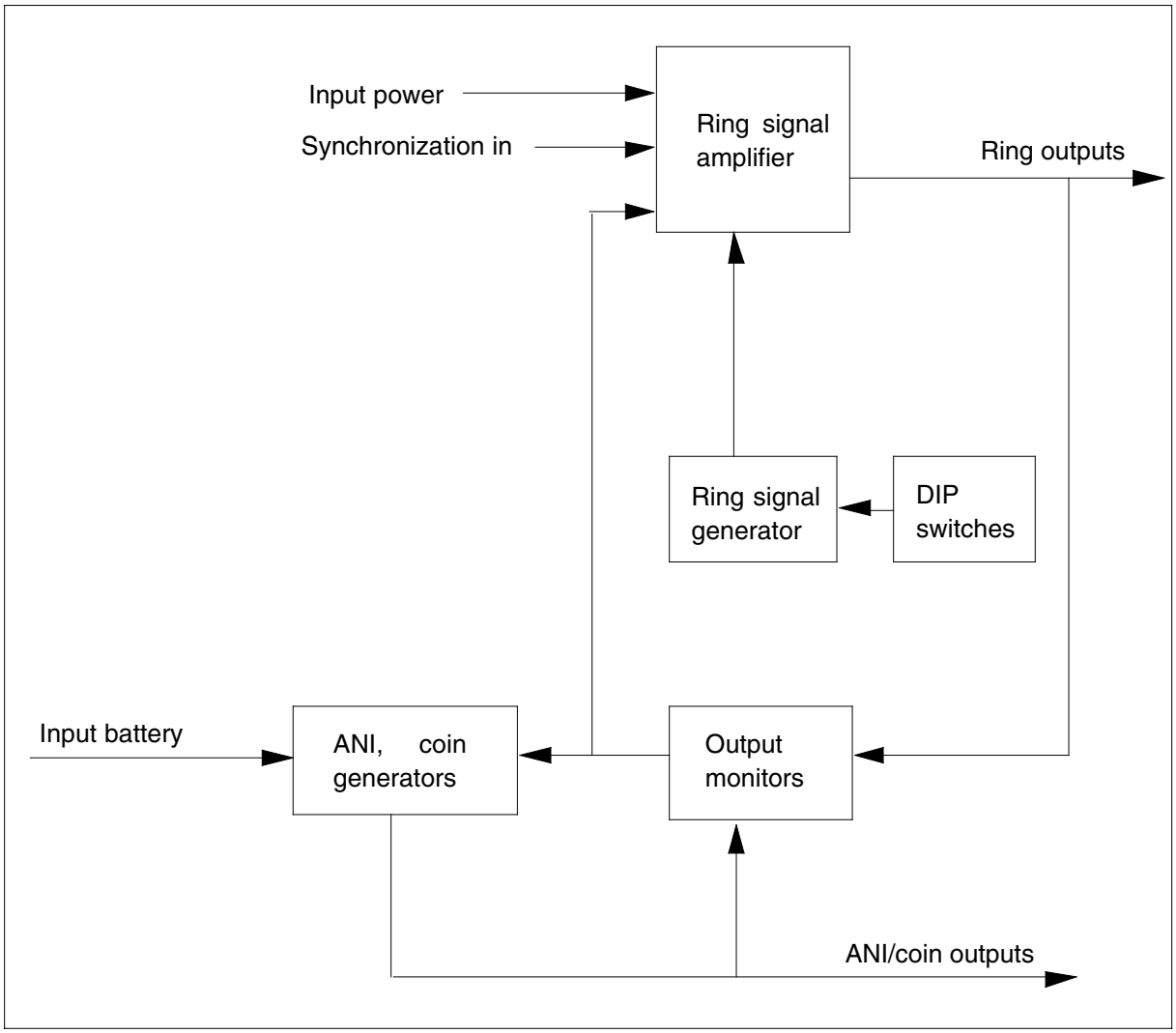
## Functional description

The NTTR60AA generates ringing signals and the dc voltages the ANI and coin functions require. Set the ring output frequency and amplitude manually during installation with the four DIP switches. Set the output frequency and amplitude to meet the ringing requirements for the operating company.

The following figure shows the relationship of the functions in the NTTR60AA.

## **NTTR60AA** (continued)

**NTTR60AA functional blocks**




# Signaling

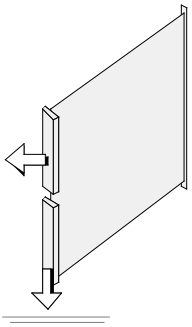
The following paragraph identifies the signaling between the NTTR60AA and the Star Hub backplane.

### Pin numbers

The figure that follows shows the pin numbers for NTTR60AA.

### NTTR60AA pin numbers

| | A | B |
|---|---|---|
| 1A 1B | +5V | |
| 2A 2B | SW:30 | SW:40 |
| 3A 3B | SW:16 | SW:32 |
| 4A 4B | SW:8 | SW:12 |
| 5A 5B | SW:38 | SW:4 |
| 6A 6B | SW:31 | SW:37 |
| 7A 7B | SW:11 | SW:15 |
| 8A 8B | SW:3 | SW:7 |
| 9A 9B | SW:35 | SW:36 |
| 10A 10B | SW:14 | SW:30 |
| 11A 11B | SW:6 | SW:10 |
| 12A 12B | +15V | SW:2 |
| 13A 13B | SW:34 | -5V |
| 14A 14B | SW:29 | SW:33 |
| 15A 15B | SW:9 | SW:13 |
| 16A 16B | SW:1 | SW:5 |
| 17A 17B | ACSHDN | |
| 18A 18B | | |
| 19A 19B | | |
| 20A 20B | | |
| 21A 21B | | |
| 22A 22B | | HVSHDN |
| 23A 23B | RG-REF | |
| 24A 24B | | |
| 25A 25B | | |
| 26A 26B | +130 ADJ | |
| 27A 27B | | |
| 28A 28B | | |
| 29A 29B | | |
| 30A 30B | +52ADJ | |
| 31A 31B | | |
| 32A 32B | | |
| 33A 33B | | |
| 34A 34B | | |
| 35A 35B | | |
| 36A 36B | | |
| 37A 37B | -130ADJ | |
| 38A 38B | -12V | |
| 39A 39B | -52ADJ | |
| 40A 40B | TPGND | +5V |



| | A | B |
|---|---|---|
| 41A 41B | +12V | |
| 42A 42B | | |
| 43A 43B | +300 | |
| 44A 44B | +300R | |
| 45A 45B | | |
| 46A 46B | | |
| 47A 47B | FSPLINK | |
| 48A 48B | -ACT | RG-SYNC |
| 49A 49B | SYNC64K | AFI |
| 50A 50B | | -CUR |
| 51A 51B | | FUSEALARM |
| 52A 52B | | |
| 53A 53B | -52V | |
| 54A 54B | RMS | XOVER |
| 55A 55B | +52V | AF0 |
| 56A 56B | RTIP | -130V |
| 57A 57B | RTIP | RTIP |
| 58A 58B | LEDPOWER | +130V |
| 59A 59B | FSPMON | FSPMON |
| 60A 60B | LOGICGND | LOGICGND |
| 61A 61B | LOGICGND | LOGICGND |
| 62A 62B | LOGICGND | LOGICGND |
| 63A 63B | LOGICGND | LOGICGND |
| 64A 64B | | |
| 65A 65B | | |
| 66A 66B | | |
| 67A 67B | | |
| 68A 68B | | |
| 69A 69B | | |
| 70A 70B | ABSBR | |
| 71A 71B | | |
| 72A 72B | | |
| 73A 73B | RTIP | RTIP |
| 74A 74B | RTIP | RTIP |
| 75A 75B | RRING | RRING |
| 76A 76B | -48V | -48V |
| 77A 77B | -48V | -48V |

## **NTTR60AA** (continued)

## Technical data

Information about NTTR60AA ringing generator appears in the following tables.

**NTTR60AA coded ringing and superimposed ringing**

| Voltage ac | | Voltage dc | | | | Cadence in seconds | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | Setting |
| Ring | R-T | Ring | Tip | R-T | Hz | 1 | 2 | 3 | 4 | No. | 87654321 |
| 240 | 86 | -26 | -26 | -52 | 20 | 2 | 2 | 1 | 1 | 1 - 4 | 00000000 |
| 240 | 86 | -18 | 18 | -38 | 20 | 2 | 2 | 1 | 1 | 1 & 2 | 00000010 |
| 240 | 86 | 18 | -18 | +38 | 20 | 2 | 2 | 1 | 1 | 3 & 4 | 00000100 |
| 240 | 86 | -18 | 18 | -38 | 20 | 2 | 2 | 1 | 1 | 1 & 2 | 01111000 |
| 240 | 86 | 18 | -18 | +38 | 20 | 2 | 2 | 1 | 1 | 3 & 4 | 01111010 |
| 240 | 86 | -26 | 26 | -52 | 20 | 1.84 | 1.84 | 1.84 | 1.84 | 1 & 2 | 01111001 |
| 240 | 86 | 26 | -26 | +52 | 20 | 1.84 | 1.84 | 1.84 | 1.84 | 3 & 4 | 01111011 |
| 295 | 105 | -26 | 26 | -52 | 20 | 1.84 | 1.84 | 1.84 | 1.84 | 1 & 2 | 00110111 |
| 295 | 105 | 26 | -26 | +52 | 20 | 1.84 | 1.84 | 1.84 | 1.84 | 3 & 4 | 01000111 |
| 295 | 105 | -26 | 26 | -52 | 20 | 2 | 2 | 1 | 1 | 1 & 2 | 00110110 |
| 295 | 105 | 26 | -26 | +52 | 20 | 2 | 2 | 1 | 1 | 3 & 4 | 01000110 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF

***Note 3:*** Ringing ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts root mean square (RMS)

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

**NTTR60AA synchromonic ringing for Bell operating company (BOC)**

| | Voltage ac | | Voltage dc | | | | Cadence in seconds | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| Low | 255 | 90 | -26 | 26 | -52 | 16 | 2 | 2 | 1 | 1 | 1 | 00001000 |
| | 255 | 90 | -26 | 26 | -52 | 20 | 2 | 2 | 1 | 1 | 1 | 00011000 |
| | 270 | 95 | -26 | 26 | -52 | 30 | 2 | 2 | 1 | 1 | 2 | 00101000 |
| | 280 | 100 | -26 | 26 | -52 | 42 | 2 | 2 | 1 | 1 | 3 | 01000000 |
| | 310 | 110 | -26 | 26 | -52 | 54 | 2 | 2 | 1 | 1 | 4 | 01010000 |
| | 353 | 125 | -26 | 26 | -52 | 66 | 2 | 2 | 1 | 1 | opt | 01100000 |
| Mid | 295 | 105 | -26 | 26 | -52 | 16 | 2 | 2 | 1 | 1 | 1 | 00001010 |
| | 295 | 105 | -26 | 26 | -52 | 20 | 2 | 2 | 1 | 1 | 1 | 00011010 |
| | 310 | 110 | -26 | 26 | -52 | 30 | 2 | 2 | 1 | 1 | 2 | 00101010 |
| | 325 | 115 | -26 | 26 | -52 | 42 | 2 | 2 | 1 | 1 | 3 | 01000010 |
| | 353 | 125 | -26 | 26 | -52 | 54 | 2 | 2 | 1 | 1 | 4 | 01010010 |
| | 395 | 140 | -26 | 26 | -52 | 66 | 2 | 2 | 1 | 1 | opt | 01100010 |
| High | 340 | 120 | -26 | 26 | -52 | 16 | 2 | 2 | 1 | 1 | 1 | 00001100 |
| | 340 | 120 | -26 | 26 | -52 | 20 | 2 | 2 | 1 | 1 | 1 | 00011100 |
| | 340 | 120 | -26 | 26 | -52 | 30 | 2 | 2 | 1 | 1 | 2 | 00101100 |
| | 365 | 130 | -26 | 26 | -52 | 42 | 2 | 2 | 1 | 1 | 3 | 00100100 |
| | 395 | 140 | -26 | 26 | -52 | 54 | 2 | 2 | 1 | 1 | 4 | 01010100 |
| | 410 | 145 | -26 | 26 | -52 | 66 | 2 | 2 | 1 | 1 | opt | 01100100 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; in voltage columns, R-T = ring to tip in volts RMS

***Note 3:*** Riinging ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

## **NTTR60AA** (continued)

**NTTR60AA harmonic ringing (BOC)**

| | Voltage ac | | Voltage dc | | | | Cadence in seconds | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| Low | 255 | 90 | -26 | 26 | -52 | 16 2/3 | 2 | 2 | 1 | 1 | 1 | 00001000 |
| | 270 | 95 | -26 | 26 | -52 | 25 | 2 | 2 | 1 | 1 | 1 | 00011000 |
| | 280 | 100 | -26 | 26 | -52 | 33 1/3 | 2 | 2 | 1 | 1 | 2 | 00101000 |
| | 310 | 110 | -26 | 26 | -52 | 50 | 2 | 2 | 1 | 1 | 4 | 01010000 |
| | 353 | 125 | -26 | 26 | -52 | 66 2/3 | 2 | 2 | 1 | 1 | opt | 01100000 |
| Mid | 295 | 105 | -26 | 26 | -52 | 16 2/3 | 2 | 2 | 1 | 1 | 1 | 00001010 |
| | 310 | 105 | -26 | 26 | -52 | 25 | 2 | 2 | 1 | 1 | 1 | 00011010 |
| | 325 | 110 | -26 | 26 | -52 | 33 1/3 | 2 | 2 | 1 | 1 | 2 | 00101010 |
| | 353 | 115 | -26 | 26 | -52 | 50 | 2 | 2 | 1 | 1 | 3 | 01000010 |
| | 395 | 140 | -26 | 26 | -52 | 66 2/3 | 2 | 2 | 1 | 1 | 4 | 01010010 |
| High | 340 | 120 | -26 | 26 | -52 | 16 2/3 | 2 | 2 | 1 | 1 | 1 | 00001100 |
| | 340 | 120 | -26 | 26 | -52 | 25 | 2 | 2 | 1 | 1 | 2 | 00011100 |
| | 365 | 130 | -26 | 26 | -52 | 33 1/3 | 2 | 2 | 1 | 1 | 3 | 00101100 |
| | 395 | 140 | -26 | 26 | -52 | 42 | 2 | 2 | 1 | 1 | 4 | 00100100 |
| | 410 | 145 | -26 | 26 | -52 | 66 2/3 | 2 | 2 | 1 | 1 | opt | 01100100 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; in voltage columns, R-T = ring to tip in volts RMS

***Note 3:*** Ringing ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

**NTTR60AA decimonic ringing (BOC)**

| | Voltage ac | | Voltage dc | | | | Cadence (seconds) | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| Low | 255 | 90 | -26 | 26 | -52 | 20 | 2 | 2 | 1 | 1 | 1 | 00011000 |
| | 270 | 95 | -26 | 26 | -52 | 30 | 2 | 2 | 1 | 1 | 2 | 00101000 |
| | 280 | 100 | -26 | 26 | -52 | 40 | 2 | 2 | 1 | 1 | 3 | 00111000 |
| | 310 | 110 | -26 | 26 | -52 | 50 | 2 | 2 | 1 | 1 | 4 | 01001000 |
| | 353 | 125 | -26 | 26 | -52 | 60 | 2 | 2 | 1 | 1 | opt | 01011000 |
| Med | 295 | 105 | -26 | 26 | -52 | 20 | 2 | 2 | 1 | 1 | 1 | 00011010 |
| | 310 | 110 | -26 | 26 | -52 | 30 | 2 | 2 | 1 | 1 | 2 | 00101010 |
| | 325 | 115 | -26 | 26 | -52 | 40 | 2 | 2 | 1 | 1 | 3 | 00111010 |
| | 353 | 125 | -26 | 26 | -52 | 50 | 2 | 2 | 1 | 1 | 4 | 01001010 |
| | 395 | 140 | -26 | 26 | -52 | 60 | 2 | 2 | 1 | 1 | opt | 01011010 |
| High | 340 | 120 | -26 | 26 | -52 | 20 | 2 | 2 | 1 | 1 | 1 | 00011100 |
| | 340 | 120 | -26 | 26 | -52 | 30 | 2 | 2 | 1 | 1 | 2 | 00101100 |
| | 365 | 130 | -26 | 26 | -52 | 40 | 2 | 2 | 1 | 1 | 3 | 00111100 |
| | 395 | 140 | -26 | 26 | -52 | 50 | 2 | 2 | 1 | 1 | 4 | 01001100 |
| | 410 | 145 | -26 | 26 | -52 | 60 | 2 | 2 | 1 | 1 | opt | 01011100 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; in voltage columns, R-T = ring to tip in volts RMS

***Note 3:*** Riinging ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

## **NTTR60AA** (continued)

**NTTR60AA synchromonic ringing for Rural Electrification Association (REA) (Sheet 1 of 2)**

| | Voltage ac | | Voltage dc | | | | Cadence (seconds) | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| Low | 255 | 90 | -26 | 26 | -52 | 16 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00001001 |
| | 255 | 90 | -26 | 26 | -52 | 20 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00011001 |
| | 270 | 95 | -26 | 26 | -52 | 30 | 1.95 | 1.35 | 1.35 | 1.35 | 2 | 00101001 |
| | 280 | 100 | -26 | 26 | -52 | 42 | 1.95 | 1.35 | 1.35 | 1.35 | 3 | 01010000 |
| | 310 | 110 | -26 | 26 | -52 | 54 | 1.95 | 1.35 | 1.35 | 1.35 | 4 | 01010001 |
| | 353 | 125 | -26 | 26 | -52 | 66 | 1.95 | 1.35 | 1.35 | 1.35 | opt | 01100001 |
| Med | 295 | 105 | -26 | 26 | -52 | 16 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00001011 |
| | 295 | 105 | -26 | 26 | -52 | 20 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00011011 |
| | 310 | 110 | -26 | 26 | -52 | 30 | 1.95 | 1.35 | 1.35 | 1.35 | 2 | 00101011 |
| | 325 | 115 | -26 | 26 | -52 | 42 | 1.95 | 1.35 | 1.35 | 1.35 | 3 | 01000011 |
| | 353 | 125 | -26 | 26 | -52 | 54 | 1.95 | 1.35 | 1.35 | 1.35 | 4 | 01010011 |
| | 395 | 140 | -26 | 26 | -52 | 66 | 1.95 | 1.35 | 1.35 | 1.35 | opt | 01100011 |
| High | 340 | 120 | -26 | 26 | -52 | 16 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00001101 |
| | 340 | 120 | -26 | 26 | -52 | 20 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00011101 |
| | 340 | 120 | -26 | 26 | -52 | 30 | 1.95 | 1.35 | 1.35 | 1.35 | 2 | 00101101 |
| | 365 | 130 | -26 | 26 | -52 | 42 | 1.95 | 1.35 | 1.35 | 1.35 | 3 | 01000101 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; in voltage columns, R-T = ring to tip in volts RMS

***Note 3:*** Ringing ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

**NTTR60AA synchromonic ringing for Rural Electrification Association (REA) (Sheet 2 of 2)**

| | Voltage ac | | Voltage dc | | | | Cadence (seconds) | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| | 395 | 140 | -26 | 26 | -52 | 54 | 1.95 | 1.35 | 1.35 | 1.35 | 4 | 01010101 |
| | 410 | 145 | -26 | 26 | -52 | 66 | 1.95 | 1.35 | 1.35 | 1.35 | opt | 01100101 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; in voltage columns, R-T = ring to tip in volts RMS

***Note 3:*** Ringing ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

**NTTR60AA harmonic (REA) (Sheet 1 of 2)**

| | Voltage ac | | Voltage dc | | | | Cadence (seconds) | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| Low | 255 | 90 | -26 | 26 | -52 | 16 2/3 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00001001 |
| | 270 | 95 | -26 | 26 | -52 | 25 | 1.95 | 1.35 | 1.35 | 1.35 | 2 | 00100001 |
| | 280 | 100 | -26 | 26 | -52 | 33 1/3 | 1.95 | 1.35 | 1.35 | 1.35 | 3 | 00110001 |
| | 310 | 110 | -26 | 26 | -52 | 50 | 1.95 | 1.35 | 1.35 | 1.35 | 4 | 01001001 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; In voltage columns, R-T = ring to tip in volts RMS

***Note 3:*** Ringing ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

## **NTTR60AA** (continued)

**NTTR60AA harmonic (REA) (Sheet 2 of 2)**

| | Voltage ac | | Voltage dc | | | | Cadence (seconds) | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| | 353 | 125 | -26 | 26 | -52 | 66 2/3 | 1.95 | 1.35 | 1.35 | 1.35 | opt | 01101001 |
| Med | 295 | 105 | -26 | 26 | -52 | 16 2/3 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00010011 |
| | 310 | 110 | -26 | 26 | -52 | 25 | 1.95 | 1.35 | 1.35 | 1.35 | 2 | 00100011 |
| | 325 | 115 | -26 | 26 | -52 | 33 1/3 | 1.95 | 1.35 | 1.35 | 1.35 | 3 | 00110011 |
| | 353 | 125 | -26 | 26 | -52 | 50 | 1.95 | 1.35 | 1.35 | 1.35 | 4 | 01001011 |
| | 395 | 140 | -26 | 26 | -52 | 66 2/3 | 1.95 | 1.35 | 1.35 | 1.35 | opt | 01101011 |
| High | 340 | 120 | -26 | 26 | -52 | 16 2/3 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00010101 |
| | 340 | 120 | -26 | 26 | -52 | 25 | 1.95 | 1.35 | 1.35 | 1.35 | 2 | 00100101 |
| | 365 | 130 | -26 | 26 | -52 | 33 1/3 | 1.95 | 1.35 | 1.35 | 1.35 | 3 | 00110101 |
| | 395 | 140 | -26 | 26 | -52 | 50 | 1.95 | 1.35 | 1.35 | 1.35 | 4 | 01001101 |
| | 410 | 145 | -26 | 26 | -52 | 66 2/3 | 1.95 | 1.35 | 1.35 | 1.35 | opt | 01101101 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; In voltage columns, R-T = ring to tip in volts RMS

***Note 3:*** Ringing ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

**NTTR60AA decimonic ringing (REA) (Sheet 1 of 2)**

| | Voltage ac | | Voltage dc | | | | Cadence (seconds) | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| Low | 255 | 90 | -26 | 26 | -52 | 20 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00011001 |
| | 270 | 95 | -26 | 26 | -52 | 30 | 1.95 | 1.35 | 1.35 | 1.35 | 2 | 00101001 |
| | 280 | 100 | -26 | 26 | -52 | 40 | 1.95 | 1.35 | 1.35 | 1.35 | 3 | 00111001 |
| | 310 | 110 | -26 | 26 | -52 | 50 | 1.95 | 1.35 | 1.35 | 1.35 | 4 | 01001001 |
| | 353 | 125 | -26 | 26 | -52 | 60 | 1.95 | 1.35 | 1.35 | 1.35 | opt | 01011001 |
| Med | 295 | 105 | -26 | 26 | -52 | 20 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00011011 |
| | 310 | 110 | -26 | 26 | -52 | 30 | 1.95 | 1.35 | 1.35 | 1.35 | 2 | 00101011 |
| | 325 | 115 | -26 | 26 | -52 | 40 | 1.95 | 1.35 | 1.35 | 1.35 | 3 | 00111011 |
| | 353 | 125 | -26 | 26 | -52 | 50 | 1.95 | 1.35 | 1.35 | 1.35 | 4 | 01001011 |
| | 395 | 140 | -26 | 26 | -52 | 60 | 1.95 | 1.35 | 1.35 | 1.35 | opt | 01011011 |
| High | 340 | 120 | -26 | 26 | -52 | 20 | 1.95 | 1.35 | 1.35 | 1.35 | 1 | 00011101 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; In voltage columns, R-T = ring to tip in volts RMS

***Note 3:*** Ringing ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

## **NTTR60AA** (continued)

**NTTR60AA decimonic ringing (REA) (Sheet 2 of 2)**

| | Voltage ac | | Voltage dc | | | | Cadence (seconds) | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| | 340 | 120 | -26 | 26 | -52 | 30 | 1.95 | 1.35 | 1.35 | 1.35 | 2 | 00101101 |
| | 365 | 130 | -26 | 26 | -52 | 40 | 1.95 | 1.35 | 1.35 | 1.35 | 3 | 00111101 |
| | 395 | 140 | -26 | 26 | -52 | 50 | 1.95 | 1.35 | 1.35 | 1.35 | 4 | 01001101 |
| | 410 | 145 | -26 | 26 | -52 | 60 | 1.95 | 1.35 | 1.35 | 1.35 | opt | 01011101 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; In voltage columns, R-T = ring to tip in volts RMS

***Note 3:*** Ringing ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

**NTTR60AA harmonic (REA) (Sheet 1 of 3)**

| | Voltage ac | | Voltage dc | | | | Cadence (seconds) | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| Low | 189 | 67 | -26 | 26 | -52 | 25 | 1.95 | 1.35 | 1.35 | 1.35 | 1-4 | 01110001 |
| Med | 210 | 75 | -26 | 26 | -52 | 25 | 1.95 | 1.35 | 1.35 | 1.35 | 1-4 | 01110011 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; In voltage columns, R-T = ring to tip in vots RMS

***Note 3:*** Ringing ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

**NTTR60AA harmonic (REA) (Sheet 2 of 3)**

| | Voltage ac | | Voltage dc | | | | Cadence (seconds) | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| High | 230 | 82 | -26 | 26 | -52 | 25 | 1.95 | 1.35 | 1.35 | 1.35 | 1-4 | 01110101 |
| Low | 189 | 67 | -26 | 26 | -52 | 25 | 2 | 2 | 1 | 1 | 1-4 | 01111000 |
| Med | 210 | 75 | -26 | 26 | -52 | 25 | 2 | 2 | 1 | 1 | 1-4 | 01111010 |
| High | 230 | 82 | -26 | 26 | -52 | 25 | 2 | 2 | 1 | 1 | 1-4 | 01110100 |
| Japan | 215 | 76 | 0 | 0 | 0 | 16 | 2 | 2 | 1 | 1 | 1-4 | 01110111 |
| UK | 210 | 75 | -26 | 26 | -52 | 25 | 1 | 1 | 0.4 | 0.6 | 1-4 | 01110110 |
| China | 240 | 86 | -26 | 26 | -52 | 25 | 1.25 | 1.25 | 1.25 | 1.25 | 1-4 | 01111100 |
| Ethiopia | 240 | 86 | -26 | 26 | -52 | 25 | - | - | - | - | 1-4 | 01111100 |
| Papua, New Guinea | 240 | 86 | -26 | 26 | -52 | 25 | - | - | - | - | 1-4 | 01111100 |
| Romania | 240 | 86 | -26 | 26 | -52 | 25 | - | - | - | - | 1-4 | 01111100 |
| Burma | 240 | 86 | -26 | 26 | -52 | 25 | - | - | - | - | 1-4 | 01111100 |
| Bezeq | 240 | 86 | -26 | 26 | -52 | 25 | - | - | - | - | 1-4 | 01111100 |
| Bolivia | 240 | 86 | -26 | 26 | -52 | 25 | - | - | - | - | 1-4 | 00011000 |
| Brazil | 240 | 86 | -26 | 26 | -52 | 25 | 1.25 | 1.25 | 1.25 | 1.25 | 1-4 | 01111100 |
| Australia | 255 | 90 | -26 | 26 | -52 | 25 | 1 | 1 | 0.4 | 0.6 | 1-4 | 01111110 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; In voltage columns, R-T = ring to tip in vots RMS

***Note 3:*** Ringing ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

## **NTTR60AA** (continued)

**NTTR60AA harmonic (REA) (Sheet 3 of 3)**

| | Voltage ac | | Voltage dc | | | | Cadence (seconds) | | | | Switches | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Type** | **Ring** | **R-T** | **Ring** | **Tip** | **R-T** | **Hz** | **1** | **2** | **3** | **4** | **No.** | **Setting** |
| Morocco | 226 | 80 | -26 | 26 | -52 | 50 | 1.7 | 1.7 | 0.8 | 0.8 | 1-4 | 01111110 |
| Germany | 183 | 65 | -30 | 30 | -60 | 25 | 2 | 2 | 1 | 1 | 1-4 | 01111101 |
| Philippines | 255 | 90 | -26 | 26 | -52 | 20 | 1.25 | 1.25 | 1.25 | 1.25 | 1-4 | 01111111 |
| Russia | 270 | 95 | -26 | 26 | -52 | 25 | - | - | - | - | 1-4 | 01101111 |
| Gruzia | 270 | 95 | -26 | 26 | -52 | 25 | - | - | - | - | 1-4 | 00100000 |

***Note 1:*** The arrow on the DIP switch indicates the ON direction. The reverse direction is OFF. Any of SW1 to SW4 not in use should have all eight sections set to OFF.

***Note 2:*** In Setting column, 0 = ON, 1 = OFF; In voltage columns, R-T = ring to tip in vots RMS

***Note 3:*** Ringing ac voltage is peak to peak.

***Note 4:*** Tip ac voltage is always 0.

***Note 5:*** R-T = ring to tip in volts RMS

***Note 6:*** opt = the specified setting can be done on any SW1 to SW4.

Information about tolerances appear in the following tables.

**NTTR60AA frequency tolerances**

| Frequency | Tolerances |
|---|---|
| 16 to 33–1/3 Hz | ±1/3 Hz |
| 40 to 60–2/3 Hz | ±1% |
| 25 Hz international | ±1/3 Hz |

**NTTR60AA ac ringing voltage tolerances (Sheet 1 of 2)**

| Nominal | Low | High |
|---|---|---|
| 67 | 65 | 69 |
| 75 | 73 | 77 |
| 82 | 80 | 84 |

**NTTR60AA ac ringing voltage tolerances (Sheet 2 of 2)**

| Nominal | Low | High |
|---|---|---|
| 86 | 84 | 88 |
| 90 | 87.3 | 92.7 |
| 95 | 92.1 | 97.8 |
| 100 | 97 | 103 |
| 105 | 101.9 | 108.1 |
| 110 | 106.7 | 113.3 |
| 115 | 111.6 | 118.4 |
| 120 | 116.4 | 123.6 |
| 125 | 121.2 | 128.7 |
| 130 | 126.1 | 133.9 |
| 140 | 135.8 | 144.2 |
| 145 | 140.7 | 149.3 |

## Power requirements

The NTTR60AA requires -39.5 V to -75 V with a nominal value of 2.5 A to a maximum of 4 A.

# NTTR66AA

## Product description

The NTTR66AA electromagnetic interference (EMI) filter card is

- a voice frequency (VF) filter card that attenuates high frequency signals from the voice frequency lines
- an EMI common mode filter for 16 line card pairs
- an EMI filter for the DS–1 links to the Star Module telephony subsystem (TSS)

### Location

The NTTR66AA is at the bottom of the TSS in the Star Module.

## Functional description

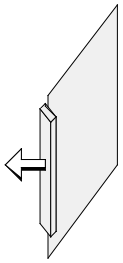
The NTTR66AA card includes a printed circuit board, one connector, and eight EMI filters.

## Signaling

The following figure shows the pin outs for the NTTR66AA

**NTTR66AA pin outs**

| | A | B |
|---|---|---|
| 1A 1B | FGND | FGND |
| 2A 2B | TIP0 | RING0 |
| 3A 3B | LCTIP0 | LCRING0 |
| 4A 4B | TIP1 | RING1 |
| 5A 5B | LCTIP1 | LCRING1 |
| 6A 6B | TIP2 | RING2 |
| 7A 7B | LCTIP2 | LCRING2 |
| 8A 8B | TIP3 | RING3 |
| 9A 9B | LCTIP3 | LCRING3 |
| 10A 10B | TIP4 | RING4 |
| 11A 11B | LCTIP4 | LCRING4 |
| 12A 12B | TIP5 | RING5 |
| 13A 13B | LCTIP5 | LCRING5 |
| 14A 14B | TIP6 | RING6 |
| 15A 15B | LCTIP6 | LCRING6 |
| 16A 16B | TIP7 | RING7 |
| 17A 17B | LCTIP7 | LCRING7 |
| 18A 18B | FGND | FGND |
| 19A 19B | TIP8 | RING8 |
| 20A 20B | LCTIP8 | LCRING8 |
| 21A 21B | TIP9 | RING9 |
| 22A 22B | LCTIP9 | LCRING9 |
| 23A 23B | TIP10 | RING10 |
| 24A 24B | LCTIP10 | LCRING10 |
| 25A 25B | TIP11 | RING11 |
| 26A 26B | LCTIP11 | LCRING11 |
| 27A 27B | TIP12 | RING12 |
| 28A 28B | LCTIP12 | LCRING12 |
| 29A 29B | TIP13 | RING13 |
| 30A 30B | LCTIP13 | LCRING13 |
| 31A 31B | TIP14 | RING14 |
| 32A 32B | LCTIP14 | LCRING14 |
| 33A 33B | TIP15 | RING15 |
| 34A 34B | LCTIP15 | LCRING15 |
| 35A 35B | FGND | FGND |



## Technical data

The following paragraph identifies the power requirements for the NTTR66AA.

### Power requirements

The NTTR66AA EMI filter card does not have any power requirements.

# NTTR67AA

## Product description

The NTTR67AA Star Module dc panel receives power from the ac/dc rectifier and from batteries. The dc panel

- distributes the main -48 V to the
  - — NTTR72AA power supply
  - — line termination unit (LTU)
  - — fans
- provides the talk battery filter and fuse
- controls the battery voltage protection
- houses the
  - — -48 V, 10 A main power circuit breaker
  - — talk battery filters
  - — power test points
  - — fuses
    - – .50 A auxiliary fuse for customer equipment
    - – .50 A LTU fuse
    - – .50 A fans and heaters fuse
    - – 5 A talk battery filter fuse

### Location

The NTTR67AA is in the Star Module telephony subsystem (TSS) below the control cards.

## Functional description

This section provides the functional description of the NTTR67AA card.

### Functional blocks

NTTR67AA includes the following functional blocks:

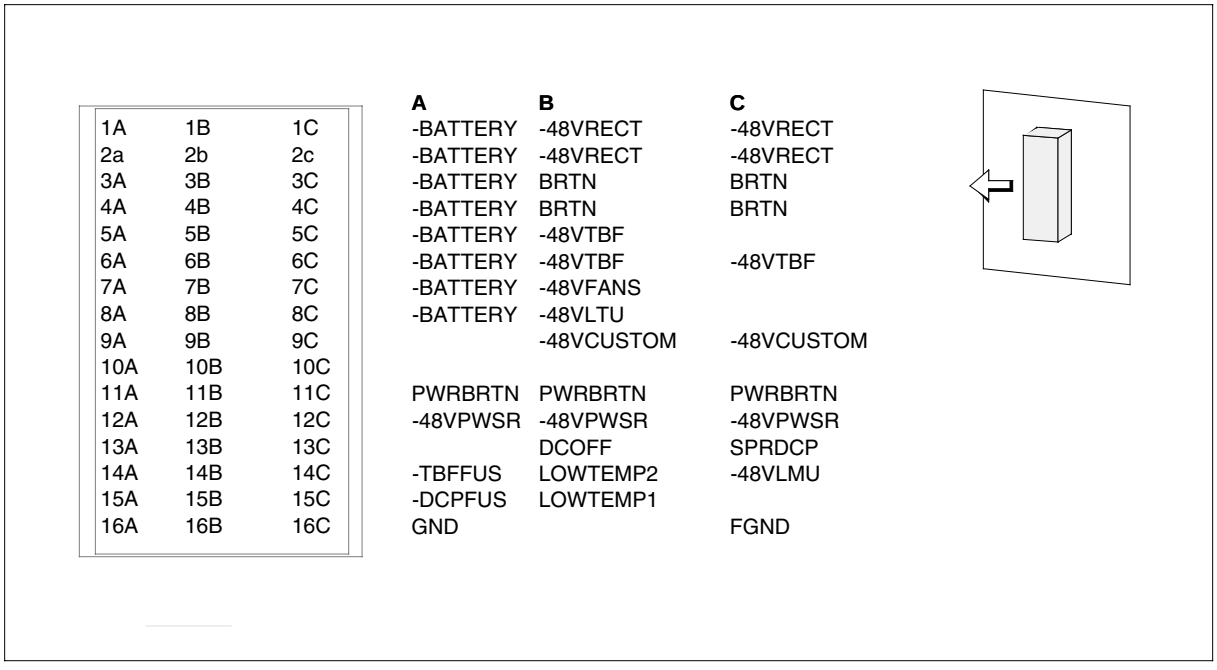
- circuit breaker, that provides an input overcurrent protection and connects and disconnects the input voltage
- electromagnetic interference filter (EMI), that reduces conducted and radiated EMI of the switching power supply converters to a level below specified limits
- talk battery filter, that reduces audio noise from the -48 V rectifier

- low voltage battery disconnect, that disconnects the batteries from the load when the batteries have discharged below 42 to 44 V
- fuses
  - — talk battery filter fuse for the line cards, that connects in series with the line cards through the talk batter filter
  - — line termination unit and fans fuses, that connects to the LTU, customer–provided equipment, and fans
- alarm, that supplies alarm signals from blown fuses
- reversal protection, that protects circuits from battery voltage reversal
- inrush current limiter, that blocks the input peak current from the talk battery filter charging current
- voltage disconnect, that disconnects input voltage in a high temperature condition
- OK LED, that is lit when the dc input voltage is OK and not lit when dc input voltage is not available or the circuit breaker is tripped

## Signaling

The figure that follows shows the pin outs for NTTR67AA.

**NTTR67AA pin outs**



## **NTTR67AA** (end)

## Technical data

The following paragraph identifies the power requirements for the NTTR67AA.

### Power requirements

The NTTR67AA has the following voltage requirements:

- -56 V dc ±.5 V at 0°C
- -53 V dc ±.5 V at 40°C

# NTTR70AA

## Product description

The NTTR70AA Star Module Controller (SMC) card is the control card for the Star Module. The SMC

- controls the switching matrix and the connection to the host
- switches 64 line cards to up to 46 DS0 channels (48 channels of two DS-1 links minus two message channels) using a switching matrix
- supports up to two DS-1 links to the Star Hub
- uses 4 Mbytes of flash memory and 16 Mbytes of DRAM for in-service loading

### Location

The NTTR70AA SMC card is in the Star Module telephony subsystem (TSS) card cage.

## Functional description

The NTTR70AA SMC card controls the Star Module and performs the following:

- controls the 64 line cards
- controls and monitors the dc panel and line maintenance unit (LMU) card
- supports high-level data link control (HDLC)/link access procedure on the D-channel (LAPD) protocol
- supports integrated services digital network (ISDN)
- supports system timing through the digital phase lock loop (DPLL)
- monitors scan and distribution points

There are five light emitting diodes (LED) on the faceplate that tell operating company personnel about alarms, the service condition, and the synchronization state of the C-side link.

The 4 Mbytes of flash memory enable the SMC card to keep its load if the SMC card is pulled out or the Star Module is powered down. If there is a power failure, the Star Module recovers automatically using the software load in memory.

The SMC card has three dual inline package (DIP) switches. The purpose and settings for these switches follow.

## **NTTR70AA** (continued)

DIP switches 1 and 2 define the type of grounding connections for the Star Module. The following table identifies the switch settings based on the grounding connections required by the Star Module.

**SMC DIP switches S1 and S2 settings**

| Function | | Switch number | DIP switch settings | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| Grounding receive shield | Disable | 1 | On | On | On | Off | Off | Off | Off | Off |
| | | 2 | | | | | | | | |
| | Enable Direct | 1 | On | On | On | Off | Off | Off | Off | On |
| | | 2 | | | | | | | | |
| | Enable capacitor | 1 | On | On | On | Off | Off | Off | Off | Off |
| | | 2 | | | | | | | | On |

DIP switch 3 on the SMC card defines the type of interface for the Star Hub. The following table identifies the switch settings based on the type of interface required by the Star Module.

**SMC DIP switch S3 settings**

| Mode | DIP switch settings | | | | Distance to Star Hub | |
|---|---|---|---|---|---|---|
| | S3_1 | S3_2 | S3_3 | S3_4 | Feet | Meters |
| DS-1 extended superframe (ESF) binary eight bit zero substitution (B8ZS) code suppression | Off | Off | Off | Off | 0-133 | 0-41 |
| | Off | Off | Off | On | 133-266 | 41-81 |
| | Off | Off | On | Off | 266-399 | 81-122 |
| | Off | Off | On | On | 399-533 | 122-163 |
| | Off | On | Off | Off | 533-655 | 163-200 |

# Signaling

The following paragraph and figures identify the signaling between the NTTR77AA and the Star Hub backplane.

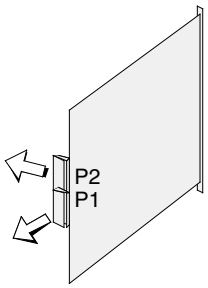
### Pin outs

The figure that follows shows the pin outs for NTTR70AA.

### NTTR70AA pin outs

P2

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | LMUOUT | LMUIN | | ISDNTYP0 | ISDNTYP1 |
| 2A 2B 2B 2D 2E | C195LMU | -FPLMU | GND | FAIL5V | FAIL100V |
| 3A 3B 3C 3D 3E | -ABORT | -INTACK | GND | -LMUINT | SPRISDN |
| 4A 4B 4C 4D 4E | -DCPFUS | -TBFFUS | DOOR | -48FANS | HEATER |
| 5A 5B 5C 5D 5E | FAN0PRT | FAN1OPRT | | DISTB0 | DISTB1 |
| 6A 6B 6C 6D 6E | SCAN0 | SCAN1 | | DISTA0 | DISTA1 |
| 7A 7B 7C 7D 7E | FAN0SCAN | GND | | FAN1SCAN | GND |
| 8A 8B 8C 8D 8E | PEN1 | MTR1 | CUTO1 | SYNC1 | LCLK1 |
| 9A 9B 9C 9D 9E | LBUS31 | LBUS30 | GND | LBUS29 | LBUS28 |
| 10A 10B 10C 10D 10E | LBUS27 | LBUS26 | | LBUS25 | LBUS24 |
| 11A 11B 11C 11D 11E | LBUS23 | LBUS22 | GND | LBUS21 | LBUS20 |
| 12A 12B 12C 12D 12E | LBUS19 | LBUS18 | | LBUS17 | LBUS16 |
| 13A 13B 13C 13D 13E | GND | | | | GND |
| 14A 14B 14C 14D 14E | LBUS15 | LBUS14 | GND | LBUS13 | LBUS12 |
| 15A 15B 15C 15D 15E | LBUS11 | LBUS10 | | LBUS9 | LBUS8 |
| 16A 16B 16C 16D 16E | LBUS7 | LBUS6 | GND | LBUS5 | LBUS4 |
| 17A 17B 17C 17D 17E | LBUS3 | LBUS2 | | LBUS1 | LBUS0 |
| 18A 18B 18C 18D 18E | GND | | | | GND |
| 19A 19B 19C 19D 19E | PEN0 | MTR0 | CUTO0 | SYNC0 | LCLK0 |
| 20A 20B 20C 20D 20E | DCOFF | LOWTEMP2 | LOWTEMP1 | LOWTEMP2 | BATTEMMP1 |
| 21A 21B 21C 21D 21E | DCPSMC | EXTBAT | BATTEST | BRTN | PWRRTN |
| 22A 22B 22C 22D 22E | RXR0 | RXR1 | | TXR0 | TXR1 |
| 23A 23B 23C 23D 23E | RXT0 | RXT1 | RXGND | TXT0 | TXT1 |
| 24A 24B 24C 24D 24E | | | | FGND | FGND |
| 25A 25B 25C 25D 25E | TACCR | PGND | GND | PGND | TACCT |




P1

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A 1B 1C 1D 1E | GND | | GND | | GND |
| 2A 2B 2B 2D 2E | +15 V | -LMUINSRT | +5.1 V | +5.1 V | +5.1 V |
| 3A 3B 3C 3D 3E | -LMURST | SPRLMU | +5.1 V | +5.1 V | +5.1 V |
| 4A 4B 4C 4D 4E | ADD0 | ADD1 | | ADD2 | ADD3 |
| 5A 5B 5C 5D 5E | DATA0 | DATA1 | GND | DATA2 | DATA3 |
| 6A 6B 6C 6D 6E | DATA4 | DATA5 | GND | DATA6 | DATA7 |
| 7A 7B 7C 7D 7E | GND | R_W | | -CSLMU | GND |
| 8A 8B 8C 8D 8E | PEN | MTR3 | CUTO3 | SYNC3 | LCLK3 |
| 9A 9B 9C 9D 9E | LBUS63 | LBUS62 | GND | LBUS61 | LBUS60 |
| 10A 10B 10C 10D 10E | LBUS59 | LBUS58 | | LBUS57 | LBUS56 |
| 11A 11B 11C 11D 11E | LBUS55 | LBUS54 | GND | LBUS53 | LBUS52 |
| 12A 12B 12C 12D 12E | | | | | |
| 13A 13B 13C 13D 13E | | | | | |
| 14A 14B 14C 14D 14E | | | | | |
| 15A 15B 15C 15D 15E | LBUS51 | LBUS50 | | LBUS49 | LBUS48 |
| 16A 16B 16C 16D 16E | LBUS47 | LBUS46 | GND | LBUS45 | LBUS44 |
| 17A 17B 17C 17D 17E | LBUS43 | LBUS42 | | LBUS41 | LBUS40 |
| 18A 18B 18C 18D 18E | LBUS39 | LBUS38 | GND | LBUS37 | LBUS36 |
| 19A 19B 19C 19D 19E | LBUS35 | LBUS34 | | LBUS33 | LBUS32 |
| 20A 20B 20C 20D 20E | PEN2 | MTR2 | CUTO2 | SYNC2 | LCLK2 |
| 21A 21B 21C 21D 21E | BPTYPE | FIBLOSS | FIBFAIL | DCFAIL | SPRO |
| 22A 22B 22C 22D 22E | -ACFAIL | GND | FREQ | GND | SPRSRVC |
| 23A 23B 23C 23D 23E | SVOLT | SCOIN | RMS | ACTCOIN | CURBIT |
| 24A 24B 24C 24D 24E | SPOL | SRING | GND | -INSRVC | -FAIL15 |
| 25A 25B 25C 25D 25E | RVRS | SPRPWRS0 | | PWRTYP | SPRPWRS1 |

## **NTTR70AA** (end)

# Technical data

The following paragraph identifies the power requirements for the NTTR70AA.

### Power requirements

The following table lists the power requirements for the NTTR70AA.

**Power requirements**

| Supply voltage | Minimum | Nominal | Maximum | Supply current |
|---|---|---|---|---|
| +5 V | +4.75 V | +5 V | +25.25 V | 1.8A |
| +15 V | +14. V | +15 V | +25 V | 0.3 A |

# NTTR71AA

## Product description

The NTTR71AA line maintenance unit (LMU) card is a digital signal processor (DSP) controlled by the NTTR70AA Star Module Controller (SMC) card. The LMU does not require a separate load. Instead it is loaded as part of the SMC loadfile. The LMU

- supports line metallic and loop maintenance for the integrated services digital network (ISDN) and plain old telephone service (POTS) lines
- supports temperature and humidity measurements for Star Modules in a Star Remote Module Outside (SRMO) cabinet
- reports the temperature and humidity measurements and alarms to the scan and distribution points
- monitors battery voltage and charging activities

### Location

The LMU is in the Star Module telephony subsystem (TSS) card cage.

## Functional description

This section provides the functional description of the NTTR71AA.

### Functional blocks

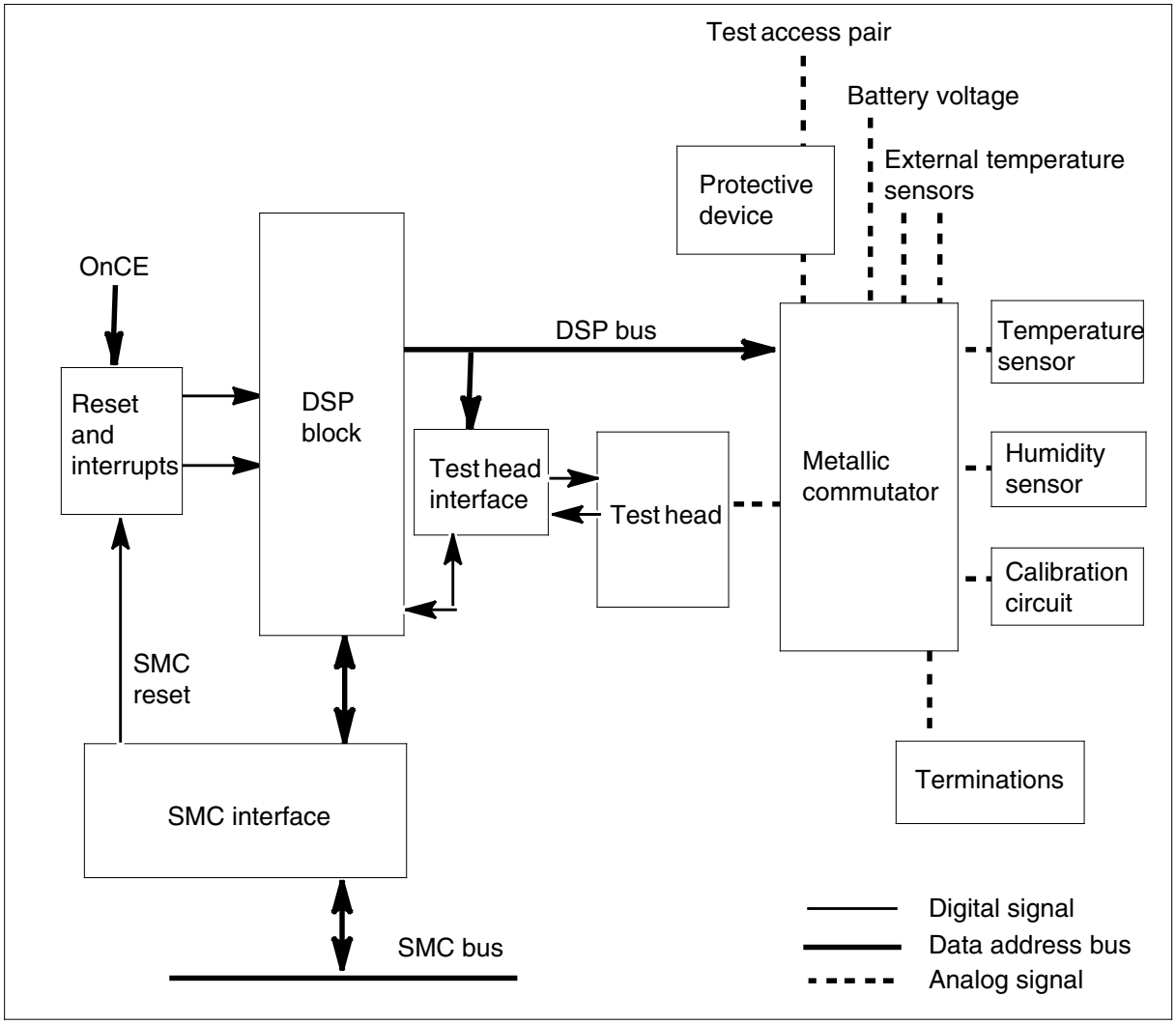
NTTR71AA includes the following functional blocks:

- DSP block
- reset and interrupts block
- test head interface
- test head block

The figure that follows shows the relationship of the functional blocks.

## **NTTR71AA** (continued)

**NTTR71AA functional blocks**




### DSP block

The DSP block contains the processor, memory, and address coding/encoding. The DSP communicates with the NTTR70AA SMC card. The DSP also communicates with the test head block through the test head interface block. Measurement data and stimulus and feedback signals are sent to the DSP from the test head.

### Reset and interrupt block

The reset and interrupts block provides the following reset and interrupts to the DSP:

- power up
- SMC
- on–chip emulator (OnCE) reset

### Test head block

The test head block connects between the DSP and the test access pair to perform different measurements. It also provides different terminations for the test access pair.

### Test head interface block

The test head interface block connects the serial bus of the test head with the serial bus of the DSP block.

## Signaling

The following paragraph identifies the signaling between the NTTR71AA and the backplane of the Star Module.

### Pin outs

The figure that follows shows the pin outs for NTTR71AA.

# **NTTR71AA** (end)

**NTTR71AA pin outs**

P1

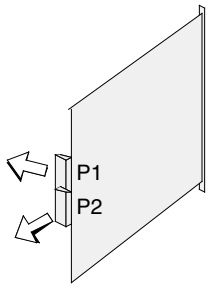
| | 1B | 1C | 1D | 1E |
|---|---|---|---|---|
| 1A | | | | |
| 2A | 2B | 2B | 2D | 2E |
| 3A | 3B | 3C | 3D | 3E |
| 4A | 4B | 4C | 4D | 4E |
| 5A | 5B | 5C | 5D | 5E |
| 6A | 6B | 6C | 6D | 6E |
| 7A | 7B | 7C | 7D | 7E |
| 8A | 8B | 8C | 8D | 8E |
| 9A | 9B | 9C | 9D | 9E |
| 10A | 10B | 10C | 10D | 10E |
| 11A | 11B | 11C | 11D | 11E |

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A | | GND | GND | GND | |
| 2A | | | +5.1V | +5.1V | +5.1V |
| 3A | GND | | +5.1V | +5.1V | +5.1V |
| 4A | ADD0 | ADD1 | | ADD2 | ADD3 |
| 5A | DATA0 | DATA1 | GND | DATA2 | DATA3 |
| 6A | DATA4 | DATA5 | GND | DATA6 | DATA7 |
| 7A | GND | R_W | | -CSLMU | GND |
| 8A | -LMUINT | -INTACK | | -ABORT | -LMURST |

P2

| | 1B | 1C | 1D | 1E |
|---|---|---|---|---|
| 1A | | | | |
| 2A | 2B | 2B | 2D | 2E |
| 3A | 3B | 3C | 3D | 3E |
| 4A | 4B | 4C | 4D | 4E |
| 5A | 5B | 5C | 5D | 5E |
| 6A | 6B | 6C | 6D | 6E |
| 7A | 7B | 7C | 7D | 7E |
| 8A | 8B | 8C | 8D | 8E |
| 9A | 9B | 9C | 9D | 9E |
| 10A | 10B | 10C | 10D | 10E |
| 11A | 11B | 11C | 11D | 11E |

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1A | LMUOUT | LMUIN | | C195LMU | FPLMU |
| 2A | | | | | SPRLMU |
| 3A | | | | | |
| 4A | | | | | |
| 5A | | | PGND | | |
| 6A | TACCR | TACCR | | TACCT | TACCT |
| 7A | | | PGND | | |
| 8A | -48VTBF | BRTN | | | |
| 9A | | | GND | +15V | +15V |
| 10A | +BATTERY | -BATTERY | | BATCUR | |
| 11A | LOWTEMP2 | LOWTEMP1 | GND | BATTEMP2 | BATTEMP1 |




## Technical data

The following paragraph identifies the power requirements for the NTTR71AA.

### Power requirements

The following table lists the power requirements for the NTTR71AA.

**Power requirements**

| Supply voltage | Minimum | Nominal | Maximum | Supply current |
|---|---|---|---|---|
| +5 V | +4.75 V | +5 V | +5.25 V | 0.4 A |
| +15 V | +14.25 V | +15 V | +15.75 V | 0.02 A |
| -48V | -43 V | -48 V | -56 V | 0.1 A |

# NTTR72AA

## Product description

The NTTR72AA ringer and power supply card supplies

- +5 V and +15 V to the NTTR70AA Star Module Controller (SMC) card and NTTR71AA line maintenance unit (LMU) from the -48 V input
- ±2.7 V, ±30 V, ±2 V coded ringing voltage to POTS lines
- +5 V integrated services digital network (ISDN) power to ISDN line cards, if installed

### Location

The NTTR72AA occupies two slots in the telephony subsystem (TSS) card cage.

## Functional description

The power supply has the following features:

- output overvoltage protection
- input dc voltage from -40 to -60 V dc
- output currrent overload and short circuit protection
- +5.1 V and +15 V over and undervoltage detection. When the monitor detects a failure, the circuit is stopped.
- faceplate mounted light emitting diode (LED) provides power supply OK indication
- coin current detector
- ring multiplexer
- coin multiplexer

The coin and ringer function of the card provides four dc voltage outputs that are used for coin functions

The following are features of the coin and ringer function of the card:

- uses input dc voltage of -40 V dc to -60 V dc
- supplies +52 V, -52 V, +130 V, or -130 V coin output voltage
- generates ringing signal

## **NTTR72AA** (continued)

- provides over–voltage protection. The ringing generator stops when the
  - — +52 or -52 V output is ±8.2 V dc
  - — +130 V or -130 V output is ±43.3 V dc
- provides low voltage detection and over current protection on +52 V, -52 V, +130 V, and -130 V outputs

## Signaling

The following paragraph identifies the signaling between the NTTR72AA and the Star Module backplane.

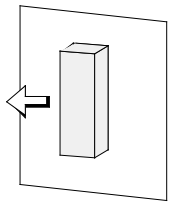
### Pin outs

The figure that follows shows the pin outs for NTTR72AA.

**NTTR72AA pin outs**

| | | |
|---|---|---|
| 1D | 1B | 1Z |
| 2D | 2b | 2Z |
| 3D | 3B | 3Z |
| 4D | 4B | 4Z |
| 5D | 5B | 5Z |
| 6D | 6B | 6Z |
| 7D | 7B | 7Z |
| 8D | 8B | 8Z |
| 9D | 9B | 9Z |
| 10D | 10B | 10Z |
| 11D | 11B | 11Z |
| 12D | 12B | 12Z |
| 13D | 13B | 13Z |
| 14D | 14B | 14Z |
| 15D | 15B | 15Z |
| 16D | 16B | 16Z |
| 17D | 17B | 17Z |
| 18D | 18B | 18Z |
| 19D | 19B | 19Z |
| 20D | 20B | 20Z |
| 21D | 21B | 21Z |
| 22D | 22B | 22Z |
| 23D | 23B | 23Z |
| 24D | 24B | 24Z |
| 25D | 25B | 25Z |
| 26D | 26B | 26Z |
| 27D | 27B | 27Z |
| 28D | 28B | 28Z |
| 29D | 28B | 29Z |
| 30D | 30B | 30Z |
| 31D | 31B | 31Z |
| 32D | 32B | 32Z |

| D | B | Z |
|---|---|---|
| GND | GND | GND |
| +5.1V | +5.1V | +12.7V |
| +15V | +15V | +15V |
| | SHTPWS | SPRPWSR0 |
| MTR3IN | RMS | ACTCOIN |
| FGND | -CURBIT | SPOL |
| | FREQ | SCOIN |
| MTR2IN | PWSTYP | SVOLT |
| RG UV TP | -INSRVC | SRING |
| COIN TP | MTR3OUT | RVRS |
| RG OV TP | MTR2OUT | |
| +5.1V TP | MTR1OUT | RING |
| +15 TP | MTR0OUT | TIP |
| MTR1IN | MTR0IN | BRTN |
| -48VPWRS | -48VPWRS | -48VPWRS |
| PWRBRTN | PWRBRTN | PWRBRTN |



## Technical data

Information about NTTR72AA ringing appears in the following tables.

## NTTR72AA (continued)

### Ringer

The following table lists the specifications of the ringer function of the NTTR72AA.

**Ringer specifications**

| | Minimum | Typical | Maximum | Comments |
|---|---|---|---|---|
| Output frequency voltage | 19 Hz | 20 Hz | 21 Hz | Frequency is set by the NTTR70AA SMC card |
| | 24 Hz | 25 Hz | 26 Hz | |
| | 29 Hz | 30 Hz | 31 Hz | |
| Output ac | 75 V rms | 80 V rms | 85 V rms | Sine wave |
| Output offset | Vin -2.25 | Vin | Vin +0.5V dc | Vin = input voltage |
| Output current | 0 | | 100 mA rms | |
| Load power factor | 0.47 | | 1 | |
| Harmonic distortion | | | 10% | |
| Ouput impedance | | | 40 Ω | dc resistance |
| | | | 200 Ω | ac resistance @ 60 Hz |
| Over voltage | 90 V rms | 105 V rms | 120 V rms | Will cause card to shut down with no automatic restart |
| Under voltage | 68 V rms | 72 V rms | 76 V rms | |
| Current limit | 20 V rms | 180 V rms | 250 V rms | |

### Coin

The following table lists the specifications of the coin function of the NTTR72AA.

**Coin specifications (Sheet 1 of 2)**

| | Minimum | Typical | Maximum | Comments |
|---|---|---|---|---|
| Output voltage 1 | 125 V dc | 130 V dc | 135 V dc | Isolated voltage |
| Output current 1 | 0 | | 125 mA rms | |
| Output ripple 1 | | | 500 mV rms | |

**Coin specifications (Sheet 2 of 2)**

| | Minimum | Typical | Maximum | Comments |
|---|---|---|---|---|
| Over voltage 1 | 140 V dc | 145 V dc | 150 V dc | Will cause card to shut down with no automatic restart |
| Under voltage 1 | 110 V dc | 115 V dc | 125 V dc | |
| Current limit 1 | 150 mA | | 300 mA | |
| Output voltage 2 | 48 V dc | 52 V dc | 54 V dc | |
| Output current 2 | 0 | | 125 mA rms | |
| Output ripple 2 | | | 500 mV rms | |
| Over voltage 2 | 54 V dc | | 60 V dc | Will cause card to shut down with no automatic restart |
| Under voltage 2 | 44 V dc | | 48 V dc | |
| Current limit 2 | 300 mA | | 600 mA | |

### +5.1 V power supply

The following table lists the specifications of the +5.1 V power supply function of the NTTR72AA.

**+5.1 V power supply specifications**

| | Minimum | Typical | Maximum | Comments |
|---|---|---|---|---|
| Output voltage | 5 V dc | 5.15 V dc | 5.3 V dc | |
| Output ripple | | | 50 mV rms | |
| Output current | 0.5 A | 2.5 A | 8 A | |
| Over voltage | 5.75 V dc | 6.75 V dc | 6.75 V dc | Will cause voltage output to shut down with no automatic restart |
| Current limit | 9 A | | 14 A | |

# NTTR72AA (end)

### +15 V power supply

The following table lists the specifications of the +15 V power supply function of the NTTR72AA.

**+15 V power supply specifications**

| | Minimum | Typical | Maximum | Comments |
|---|---|---|---|---|
| Output voltage | 14.5 V dc | 15 V dc | 15.5 V dc | |
| Output ripple | | | 150 mV rms | |
| Output current | 0.2 A | 2 A | 3 A | |
| Over voltage | 16 V dc | 17 V dc | 18 V dc | Will cause voltage output to shut down with no automatic restart |
| Undervoltage | 12 V dc | 13 V dc | 14 V dc | |
| Current limit | 4A | | 7 A | |

### +12.7 V regulator

The following table lists the specifications of the +12.7 V regulator function of the NTTR72AA.

**+12.7 V power supply specifications**

| | Minimum | Typical | Maximum | Comments |
|---|---|---|---|---|
| Output voltage | 12.4 V dc | 12.7 V dc | 13 V dc | |
| Output ripple | | | 100 mV rms | |
| Output current | 0 mA dc | 50 mA dc | 100 mA dc | |
| Over voltage | | N/A | | |
| Undervoltage | | N/A | | |
| Current limit | 150 mA dc | | 500 mA dc | |

### Power requirements

The NTTR72AA. requires -40 V to -60 V dc with a maximum input current of 3.25 A.

# NTTR73AA

## Product description

The universal maintenance pack (UMP) is a maintenance card that contains the functionalities of several circuit cards of a maintenance trunk module (MTM). For example, the MTM contains a line testing unit (LTU), monitor/talk (MONTALK)/system operator verification trunk (VER90), and metallic test access (MTA). The UMP supports

- firmware downloading—flash memory to enable the UMP to keep its load if the card removed or power is removed from the unit
- the following maintenance capabilities:
  - four separate test access pairs for each Star Remote Hub equipment (SRHE) frame
  - external tester interface with three wires that support one voice circuit, one sleeve wire interface, and several terminations
  - MONTALK interface for monitoring or talking to a line
  - support for call progress tones generation and 16 dual tone multifrequency (DTMF) receivers when the Star Hub is in emergency stand–alone (ESA) mode
  - accessible from both processors
  - line card testing
  - subscriber loop testing
- scan and distribution points
  - 8 user–defined distribution points for each UMP card
  - 12 user–defined scan points for each UMP card
- ISDN line tests, including
  - feed voltage measurements
  - dc resistance measurements
  - dc capacitance measurements
  - foreign voltage measurements
  - ISDN protocol tests, where the UMP card acts as an external interface

### Location

Slots 11 and 13 of the Star Hub control shelf.

## **NTTR73AA** (continued)

# Functional description

The UMP card connects to the remote controller packs (RCP) in the Star Hub through two DS30 links. The UMP card operates in one of two modes, depending on the shelf state.

- normal mode, the UMP can perform
  - — subscriber loop tests
  - — line card tests
  - — external tester interface
  - — MONTALK
  - — scan point monitoring
  - — distribution point
- emergency stand–alone (ESA) mode, the UMP can support
  - — 16 dual tone multifrequency receivers
  - — call progress tones generation

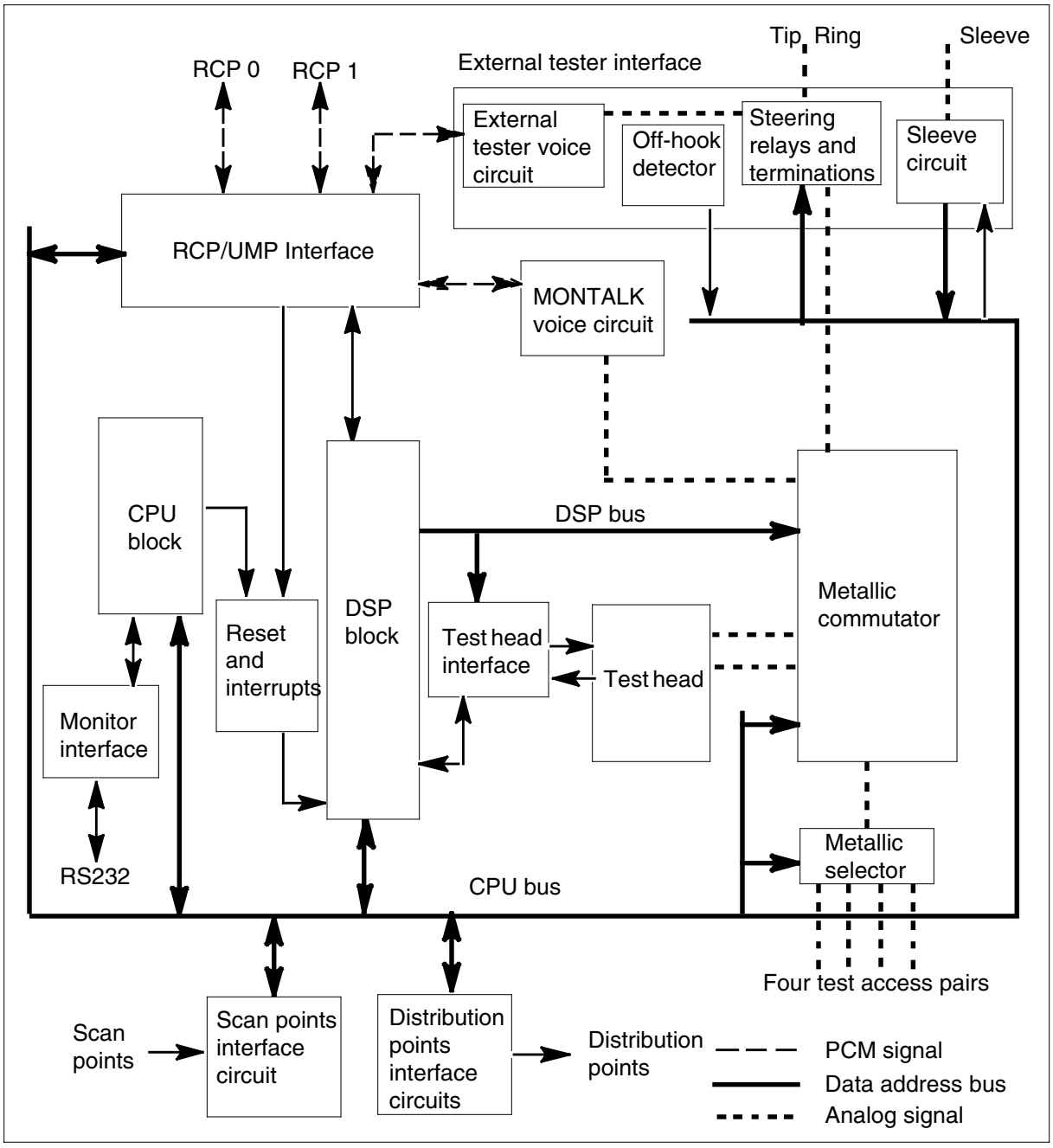
### Functional blocks

The NTTR73AA includes the following functional blocks:

- digital signal processor (DSP) block
- scan points interface circuit
- distribution points interface circuit
- metallic circuit selector
- sleeve circuit
- off–hook detector
- steering relays and terminations

The following figure shows the relationship of the functional blocks.

**NTTR73AA functional blocks**




## Central processing unit (CPU) block

The CPU block is based on the MC68302 processor from Motorola. The CPU block includes permanent storage on flash memory and temporary storage on static random access memory (SRAM).

## NTTR73AA (continued)

### RCP/UMP interface

The RCP/UMP interface controls the interface between the CPU and the RCPs and the PCM connections in the UMP.

### DSP block

The DSP block receives data from and transmits the data to the voice circuit through the RCP/UMP interface.

### Reset and interrupt block

The reset and interrupts block provides the reset and interrupt signals to the DSP.

### Monitor interface

The UMP communicates with an external monitor through the monitor interface and RS232 interface to provide debugging capabilities.

### Test head block

The test head block connects between the DSP and the metallic bus to support the different measurements that can be taken and, provides different terminations for the metallic bus. The DSP controls the test head through the test head interface.

### Test head interface block

The test head interface block connects the test head with the DSP block.

### External tester interface block

The external tester interface block includes

- an external tester voice circuit that connects the voice signals from external tip and ring wires to the PCM data circuits of the UMP
- an off–hook detector that detects the on–hook or off–hook state of the external interface
- a sleeve circuit

### MONTALK voice circuit

The MONTALK voice circuit connects between voice signals of a test access pair and the PCM data circuits of the UMP. The circuit is based on a voice codec and hybrid transformer.

### Metallic selector block

The metallic selector block selects one of four test access pairs and connects a test access pair to internal circuits of the UMP through the metallic commutator.

### Metallic commutator block

The metallic commutator block sets up connections between the following circuits:

- selected test access pair
- external tester tip and ring wires
- external tester voice circuit
- MONTALK voice circuit
- test head
- calibration circuit

### Scan points interface circuit

The scan points interface circuit allows the CPU to read the state of the 12 scan points and test the scan points.

### Distribution points interface circuit

The distribution points interface circuit allows the CPU to control eight distribution relays and checks their status.

### Steering relays and terminations block

The steering relays route the signal from the test access pair and the external tester wires to circuits in the UMP. The CPU controls the steering relays. This block also monitors signals to the external tester for polarity reversal and terminations.

## Signaling

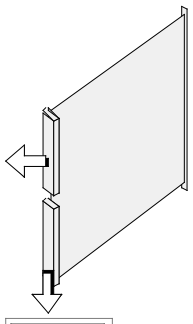
The following paragraph identifies the signaling between the NTTR73AA and the backplane of the Star Hub.

### Pin numbers

The figure that follows shows the pin outs for NTTR73AA.

# **NTTR73AA** (continued)

### NTTR73AA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | | |
| 3A 3B | TACT 0 | |
| 4A 4B | | TACT 0 |
| 5A 5B | TACR 0 | |
| 6A 6B | | TACR 0 |
| 7A 7B | TACT 1 | |
| 8A 8B | | TACT 1 |
| 9A 9B | TACR1 | |
| 10A 10B | | TACR1 |
| 11A 11B | PROTGND | PROTGND |
| 12A 12B | TACT1 | |
| 13A 13B | | TACT2 |
| 14A 14B | TACR2 | |
| 15A 15B | | TACR2 |
| 16A 16B | TACT3 | |
| 17A 17B | | TACT3 |
| 18A 18B | TACR3 | |
| 19A 19B | | TACR3 |
| 20A 20B | PROT GND | PROT GND |
| 21A 21B | | |
| 22A 22B | GND | GND |
| 23A 23B | +5.1 V | +5.1V |
| 24A 24B | +5.1 V | +5.1V |
| 25A 25B | +5.1 V | +5.1V |
| 26A 26B | C195 0 | FP 0 |
| 27A 27B | DIN 0 | DOUT 0 |
| 28A 28B | ACT 0 | RSTUMP0 |
| 29A 29B | C195 1 | FP 1 |
| 30A 30B | DIN 1 | DOUT 1 |
| 31A 31B | ACT1 | RSTUMP1 |
| 32A 32B | SPR0 | SPR1 |
| 33A 33B | | UNIT0 |
| 34A 34B | +15V | +15V |
| 35A 35B | DSI_OSI | GND OUT |
| 36A 36B | DSO | GND OUT |
| 37A 37B | DSCK | GND OUT |
| 38A 38B | DR | GND OUT |
| 39A 39B | ONCERST | +5V |
| 40A 40B | GND | GND |

| | A | B |
|---|---|---|
| 41A 41B | EXTTIP | EXTRING |
| 42A 42B | SLEEVE | PROT GND |
| 43A 43B | SCAN0 | SCAN1 |
| 44A 44B | SCAN1 | SCAN2 |
| 45A 45B | SCAN4 | SCAN5 |
| 46A 46B | SCAN6 | SCAN7 |
| 47A 47B | SCAN8 | SCAN9 |
| 48A 48B | SCAN10 | SCAN11 |
| 49A 49B | DIST0A | DIST0A |
| 50A 50B | DIST1A | DIST1B |
| 51A 51B | DIST2A | DIST2B |
| 52A 52B | DIST3A | DIST3B |
| 53A 53B | DIST4A | DIST4B |
| 54A 54B | DIST5A | DIST5B |
| 55A 55B | DIST6A | DIST6B |
| 56A 56B | DIST7A | DIST7B |
| 57A 57B | CATA | CATB |
| 58A 58B | MAJA | MAJB |
| 59A 59B | PHONET0 | PHONER0 |
| 60A 60B | PHONET1 | PHONER1 |
| 61A 61B | | |
| 62A 62B | | |
| 63A 63B | | |
| 64A 64B | | |
| 65A 65B | | |
| 66A 66B | | |
| 67A 67B | | |
| 68A 68B | GND | GND |
| 69A 69B | | |
| 70A 70B | | |
| 71A 71B | | |
| 72A 72B | +130V | 130V |
| 73A 73B | | |
| 74A 74B | 48V | 48V |
| 75A 75B | | |
| 76A 76B | BRTN | BRTN |
| 77A 77B | | |
| 78A 78B | | TXD |
| 79A 79B | | RXD |
| 80A 80B | GND | GND |

## Technical data

This section provides technical data about the NTTR73AA and electrical specifications for the following:

- RS232 connector
- UMP terminations
- test access pair
- MONTALK voice circuit
- external tester sleeve wire, voice circuit, and tip and ring
- distribution points
- scan points
- power requirements

### RS232 connector

The system uses only two wires of the RS232. The following table lists these wires and the electrical specifications for the RS232 connector.

**RS232 electrical specifications**

| Wire | Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|---|
| RxD | Turn–on threshold | 1.35 V | 1.8 V | 2.35 V |
| RxD | Turn–off threshold | 0.75 V | 1.0 V | 1.25 V |
| RxD | Input resistance | 3.0 k Ω | 5.4 k Ω | 7.0 k Ω |
| RxD | Maximum voltage | | | 25 V |
| TxD | High voltage | 9.2 V | 9.5 V | |
| TxD | Low voltage | -10.0 V | -10.3 V | |
| TxD | Off source resistance | 300 Ω | | |
| TxD | Maximum voltage | | | ±15 V |

## NTTR73AA (continued)

### UMP terminations

The following table lists the characteristics of UMP terminations.

**UMP terminations**

| Termination number | Resistance | Configuration |
|---|---|---|
| 1 | 1.69 k Ω | Tip-ring, tip-ground, ring-ground |
| 2 | 20 k Ω | Tip-ring, tip-ground, ring-ground |
| 3 | 900 Ω | Tip-ring |

### Test access pair

The operating characteristics of the test access pair is as follows:

- input impedance mode
  - — maximum output voltage (open circuit) - 160 Vdc
  - — maximum output current (short circuit) - 18 mA
- input breakdown voltage range - 420 V to 600 V

### MONTALK voice circuit

The following table lists the operating conditions of the MONTALK voice circuit.

**MONTALK voice circuit operating conditions**

| Characteristic | Value |
|---|---|
| Maximum input/output voice frequency voltage level | 1734 Vrms |
| Voice frequency range | 300 to 3400 Hz |
| Maximum input dc voltage level | 56 V |
| Maximum dc current | 50 mA |
| Maximum input ac voltage level (25 Hz) | 100 Vrms |
| Maximum ac current at 100 V, 25 Hz | 15 mA |

### External tester

This section gives the characteristics of the the external tester components.

### Sleeve wire

The sleeve wire has five electrical states that provide control information from the external tester. The following table lists these five states and the range of current flowing between the sleeve and ground.

**Sleeve wire states**

| State | Current range |
|---|---|
| Disconnect or open | -3 to +3 mA |
| High positive current | +21 to +210 mA |
| Low positive current | +6 to +18 mA |
| High negative current | -21 to -210 mA |
| Low negative current | -6 to -18 mA |

The input resistance is 200 Ω±10% when the external tester is in use. The sleeve wire is disconnected when the external tester is not in use.

The input breakdown voltage range is from 60 V to 95 V, without regard to the polarity.

### External tester voice circuit

The following table lists the operating conditions of the external tester voice circuit.

**External tester voice circuit operating conditions**

| Characteristic | Value |
|---|---|
| Maximum input/output voice frequency voltage level | 1734 Vrms |
| Voice frequency range | 200 to 3400 Hz |
| Maximum input dc voltage level | 56 V |
| Maximum dc current | 50 mA |

The input breakdown voltage range of the external tester voice circuit is as follows:

- external tip to ring range is from 60 V to 95 V without regard to the polarity
- positive voltage tip to ground and ring to ground is 1 V
- negative voltage tip to ground and ring to ground is from -60 V to -95 V

## **NTTR73AA** (continued)

### External tester tip and ring characteristics

The characteristics of the external tester tip and ring are as follows:

- the tip and ring circuits provide the following connections to the external tester, when not in a dialing state:
  - — the 35.7 kΩ (5%) delta across tip, ring, and ground
  - — tip and ring are ac coupled to the external tester voice circuit and the tone is software selected, and is normally high tone
  - — ring to tip is dc open
  - — tip to ground is dc open
  - — ring is connected to ground through 511 50 Ω
- the external tester voice circuit appears as a normal line circuit when it
  - — provides 200 Ω, 48 Vdc nominal battery feed on the ring side
  - — provides 200 Ω ground on the tip side
  - — permits operation with an external resistance of up to 1500Ω

### Distribution points electrical specifications

The following table lists the electrical specifications for the distributions points.

**Distribution points electrical specifications**

| Voltage characteristics | Values | |
|---|---|---|
| Maximum switching voltage | 200 Vdc | 250 Vac |
| Maximum switching power | 30 W (resistance) | 62.5 VA (resistance) |
| Maximum switching current | 1 A | |
| Maximum carrying current | 1.5 A | |
| Insulation resistance to ground | 1000 M Ω at 500 Vdc | |
| Breakdown voltage | Between any two points | 1000 Vac (for 1 minute) |
| Breakdown voltage | Between any point and ground | 1000 Vac (for 1 minute) |

### Scan points electrical specifications

The following are the operating conditions and ratings for the scan points:

- high–level input voltage
  - — +2.4 V minimum
  - — +40 V maximum
- low–level input voltage
  - — -40 V minimum
  - — +0.2 V maximum
- source output resistance is 10 kΩ maximum
- maximum input voltage
  - — 50 V when source output resistance is 0 Ω
  - — 100 V when source output resistance is 10 k Ω

### Power requirements

The following table lists the voltage and current requirements of the UMP card.

**Power requirements for the NTTR73AA**

| Supply voltage | Minimum voltage | Nominal voltage | Maximum voltage | Supply current |
|---|---|---|---|---|
| +5 V | +4.75 V | +5 | +5.25 V | 1.0 A |
| +15 V | +13.5 V | +15 V | +16.5 V | 0.6 A |
| -48 V | -42 V | -48 V | -60 V | 0.06 A |

# NTTR74AA

## Product description

The NTTR74AA alarms card checks and controls the distribution of power to the power converters, ringer cards, and line drawers.

### Location

The NTTR74AA alarms card is behind the faceplate of the frame supervisory panel (FSP) for the Star Hub.

## Functional description

The alarms card joins the power distribution function of the circuit breakers and the power monitoring function of the fuses.

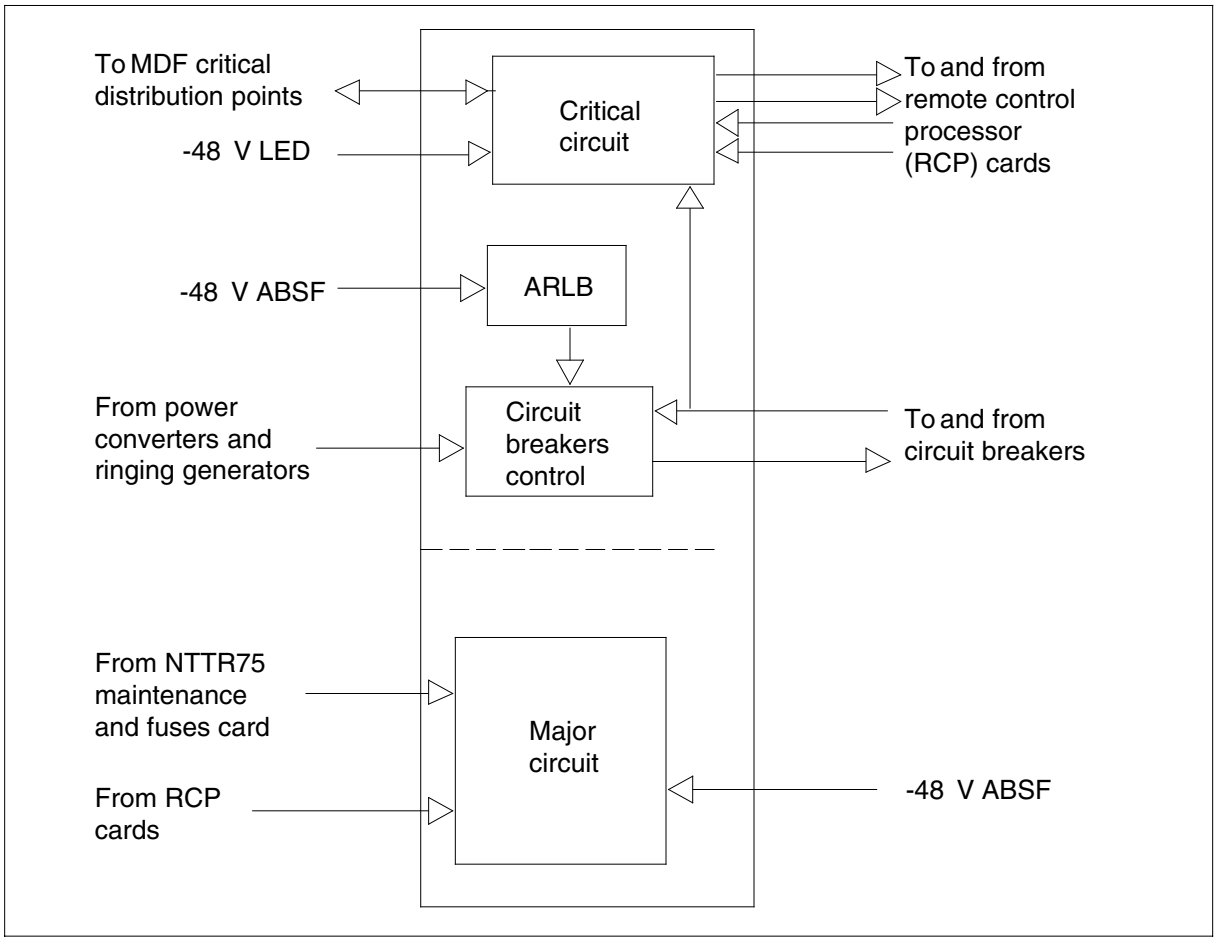
### Functional blocks

NTTR74AA includes the following functional blocks:

- control circuit for the circuit breakers and the automatic recovery from low battery (ARLB) and critical alarm circuits
- control circuit that monitors the status of +5 V, +15 V, -48 V, LEDs, ringing, -48 V ABS fuses, and controls the major alarm circuit

The figure that follows shows the relationship of the functional blocks.

**NTTR74AA functional blocks**




## Technical data

The following paragraph identifies the power requirements for the NTTR74AA.

### Power requirements

The alarms card has the following power requirements:

- minimum voltage of -39 Vdc
- nominal voltage of -48 Vdc
- maximum voltage of-60 Vdc
- nominal 60 mA current

# NTTR75AA

## Product description

The NTTR75AA maintenance and fuses card contains the alarms light emitting diodes (LED) and Star Hub fuses. The LEDs report alarm conditions for the Star Hub.

### Location

The NTTR75AA maintenance and fuses card is in the Star Hub FSP.

## Functional description

The maintenance and fuses card contains

- up to 66 fuses
- four light emitting diodes (LED)
- -48 V test points
- two telephone jacks
- two RS232 connectors

The maintenance and fuses card connects to the Star Hub backplane. The card provides the connections necessary for the NTTR74AA and the NTTR76AA cards in the frame supervisory panel (FSP).

### Functional blocks

NTTR75AA has the following functional blocks.

- The fuses section, which contains up to 66 fuses. There are six different groups of fuses for the different voltage levels supply and different customers.
- The maintenance section, which contains four alarm LED indicators, two RS232 connectors, two telephone jacks, and voltage test points.

## Technical data

The following paragraph identifies the power requirements for the NTTR75AA.

### Power requirements

The NTTR75AA maintenance and fuses card does not have any power requirements. The card transfers the power to other components.

# NTTR76AA

## Product description

The talk battery and circuit breakers card

- contains the circuit breakers that connect to the power sources (-48 V A–feed and -48 V B–feed) to the loads (converter and ringer cards)
- provides filtered battery filters to reduce audo frequency cross talk
- protects the frame supervisory panel (FSP) in the Star Hub against voltage transients on the main -48 V feed that can result from lightning or reversed polarity connections
- connects to the alarms card, the maintenance and fuses card, and the Star Hub backplane through cables and connectors

### Location

The talk battery and circuit breakers card is in the Star Hub FSP.

## Functional description

The talk battery and circuit breakers card has the circuit breakers and talk battery filters required to supply and protect power to the Star Hub.

## Technical data

The following paragraph identifies the power requirements for the NTTR76AA.

### Power requirements

The power requirements for the talk battery and circuit breaker card are as follows:

- -48 V A feed and -48 V B feed, with the following voltage values
  - — minimum of -39 V
  - — maximum of -60 V
  - — normal of -48 V
- talk A and B supply, with the following voltage values
  - — minimum of -39 V
  - — maximum of -60 V
  - — normal of -48 V

# NTTR77AA

## Product description

The remote controller pack (RCP) is the control card for the Star Hub. The RCP provides

- up to 32 message links
- 8 Mbytes of flash memory that enables the RCP to save its load if the card is pulled or the unit is powered down
- 8 Mbytes of dynamic random access memory (DRAM)
- processing
- clock synchronization
- switching matrix that switches any of the 40 input port channels to any time slot of the 40 output channels
- connection to local line drawers
- support for P–side DS–1 links
- two interlinks between the RCPs that allow communication between the processors and routes calls within the Star Hub. The interlinks support up to 62 calls.

### Location

The RCP card is in slots 7 and 17 of the Star Hub control shelf.

## Functional description

The remote controller pack controls the Star Hub and performs the following:

- receives and transmits up to 16 DS30 links (eight DS60) from and to the C–side (NTMX81 packlets)
- handles the message link from the host
- receives and transmits up to 32 DS30 links (16 DS60) from and to the P–side (NTMX81 packlets)
- handles the message channel from the remote line drawers (Star Modules)
- receives and transmits 18 DS30 and RCON/TCON message links from and to the local line drawers
- controls the two NTTR73AA universal maintenance packs (UMP) in the system through two DS30 links
- controls the three links to the mate RCP
- controls and monitors the status of the power supply cards
- controls and monitors the status of the ringer cards

- controls switching between all the incoming and outgoing links with an equal delay on all links
- operates synchronization to the host caused by the digital phase lock loop (DPLL) circuit on the pack. The DPLL circuit generates a system clock synchronized to the received recovery frame pulse from the first C–side link on the unit.
- generates clock and frame pulses for all the cards in the Star Remote system
- operates with the same timing of the clocks and frame pulse with the mate RCP present in the system
- supports emergency stand–alone (ESA) mode when the connection to the host fails
- selects the pack operation mode (DS–1) according to the backplane DIP switches position
- supports maintenance activities

## Signaling

The following paragraph and figures identify the signaling between the NTTR77AA and the Star Hub backplane.

### Pin numbers

The figure that follows shows the pin numbers for NTTR77AA.

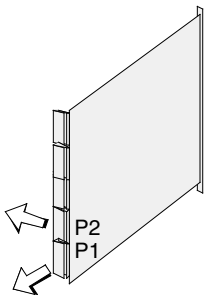
# **NTTR77AA** (continued)

### NTTR77AA pin numbers

P2

| | | | | |
|---|---|---|---|---|
| 1A | 1B | 1C | 1D | 1E |
| 2A | 2B | 2B | 2D | 2E |
| 3A | 3B | 3C | 3D | 3E |
| 4A | 4B | 4C | 4D | 4E |
| 5A | 5B | 5C | 5D | 5E |
| 6A | 6B | 6C | 6D | 6E |
| 7A | 7B | 7C | 7D | 7E |
| 8A | 8B | 8C | 8D | 8E |
| 9A | 9B | 9C | 9D | 9E |
| 10A | 10B | 10C | 10D | 10E |
| 11A | 11B | 11C | 11D | 11E |
| 15A | 15B | 15C | 15D | 15E |
| 16A | 16B | 16C | 16D | 16E |
| 17A | 17B | 17C | 17D | 17E |
| 18A | 18B | 18C | 18D | 18E |
| 19A | 19B | 19C | 19D | 19E |
| 20A | 20B | 20C | 20D | 20E |
| 21A | 21B | 21C | 21D | 21E |
| 22A | 22B | 22C | 22D | 22E |
| 23A | 23B | 23C | 23D | 23E |
| 24A | 24B | 24C | 24D | 24E |
| 25A | 25B | 25C | 25D | 25E |

| **A** | **B** | **C** | **D** | **E** |
|---|---|---|---|---|
| GND | GND | GND | -RXFP-0 | -RXFP-M |
| C195-SP | -ACT-SP | | C195UMP0 | C195UMP1 |
| FP-SP | RST-SP | | -FP-UMP0 | -FP-UMP1 |
| DIN-SP | DOUT-SP | | ACTUMP0 | ACTUMP1 |
| DIN-UMP0 | DIN-UMP1 | | DOUTUMP0 | DOUTUMP1 |
| DOUT0RCP | DOUT1RCP | GND | RSTUP0 | RSTUMP1 |
| DIN0-RCP | DIN1RCP | GND | C97L-CD | C97L-CM |
| PLLFPO | PLLFPI | C97-SPR | C97L--P0O | C97L-P1O |
| ACTSPR | DIN-SPR | DOUT-SPR | C97L-P0M | C97LP1M |
| GND | GND | GND | GND | GND |
| C324-CO | C324L-CM | | C324LP0O | C324LP1O |
| C324LP0M | C324LP1M | | | |
| GND | GND | GND | GND | GND |
| FP48L-CO | FP48L-CM | FP48L-P0O | FP48L-P1O | FP48L-P0M |
| F48LP1M | GND | FP48SPR | GND | GND |
| DOUTC0-2 | DOUTC0-3 | GND | DOUTC1-2 | DOUTC1-3 |
| DOUTP00-2 | DOUTP00-3 | GND | DOUTP01-2 | DOUTP01-3 |
| DOUP10-2 | DOUP10-3 | GND | DOUTP11-2 | DOUTP11-3 |
| DINC0-2 | DINC0-3 | GND | DINC1-2 | DINC1-3 |
| DINP00-2 | DINP00-3 | | DINP01-2 | DINP01-3 |
| DINP10-2 | DINP10-3 | GND | DINP11-2 | DINP11-3 |
| ACTL-C | ACTL-P0 | ACTL-P1 | | |




P1

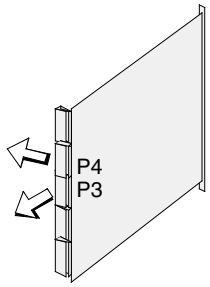
| | | | | |
|---|---|---|---|---|
| 1A | 1B | 1C | 1D | 1E |
| 2A | 2B | 2B | 2D | 2E |
| 3A | 3B | 3C | 3D | 3E |
| 4A | 4B | 4C | 4D | 4E |
| 5A | 5B | 5C | 5D | 5E |
| 6A | 6B | 6C | 6D | 6E |
| 7A | 7B | 7C | 7D | 7E |
| 8A | 8B | 8C | 8D | 8E |
| 9A | 9B | 9C | 9D | 9E |
| 10A | 10B | 10C | 10D | 10E |
| 11A | 11B | 11C | 11D | 11E |
| 15A | 15B | 15C | 15D | 15E |
| 16A | 16B | 16C | 16D | 16E |
| 17A | 17B | 17C | 17D | 17E |
| 18A | 18B | 18C | 18D | 18E |
| 19A | 19B | 19C | 19D | 19E |
| 20A | 20B | 20C | 20D | 20E |
| 21A | 21B | 21C | 21D | 21E |
| 22A | 22B | 22C | 22D | 22E |
| 23A | 23B | 23C | 23D | 23E |
| 24A | 24B | 24C | 24D | 24E |
| 25A | 25B | 25C | 25D | 25E |

| **A** | **B** | **C** | **D** | **E** |
|---|---|---|---|---|
| GND | GND | GND | GND | GND |
| +5.1 V | +5.1 V | +5.1 V | RXD-CPU | TXT-CPT |
| +5.1 V | +5.1 V | +5.1 V | RX-XNET | TX-XNET |
| +5.1 V | +5.1 V | +5.1 V | | CARD74 |
| +5.1 V | +5.1 V | +5.1 V | TALKALM | SPRIN3 |
| +5.1 V | +5.1 V | +5.1 V | GND | GND |
| GND | GND | GND | C97U-CO | C97U-CM |
| GND | GND | | C97U-P0O | C97U-P1O |
| C97RCPO | C97RCPI | | C97UP0M | C97UP1M |
| GND | GND | GND | GND | GND |
| C324U-CO | C324U-CM | | C324U-P0O | C324U-P1O |
| C324YP0M | C324UP1M | | C324CRPO | C324RCPI |
| GND | GND | GND | GND | GND |
| FP48UCO | FP48U-CM | FP48U-P0O | FP48UP0O | FP48UU-P0M |
| FP48U-P1M | FP48OUT | FP48-IN | ACTRCPI | ACTRCPO |
| DOUTC0-0 | DOUTC0-1 | GND | DOUTC1-0 | DOUTC1-1 |
| DOUTP00-0 | DOUTP00-1 | GND | DOUTP01-0 | DOUTP01-1 |
| DOUTP10-0 | DOUTP10-1 | GND | DOUTP11-0 | DOUTP11-1 |
| DINC0-0 | DINC0-1 | GND | DINC1-0 | DINC1-1 |
| DINP00-0 | DINP00-1 | | DINP01-0 | DINP01-1 |
| DINP10-0 | DINP10-1 | GND | DINP11-0 | DINP11-1 |
| ACTU-C | ACTU-P0 | ACTU-P1 | MSG-IN | MSG-OUT |

### NTTR77AA pin numbers (continued)

P4

| | | | | | A | B | C | D | E |
|---|---|---|---|---|---|---|---|---|---|
| 1A | 1B | | 1D | 1E | | | | | |
| 2A | 2B | | 2D | 2E | SVOLT0 | GND | | SBOLT1 | GND |
| 3A | 3B | | 3D | 3E | SCOIN0 | SPOL0 | | SCOIN1 | SPOL1 |
| 4A | 4B | | 4D | 4E | CURBIT0 | SRG0 | | CURBIT1 | SRG1 |
| 5A | 5B | | 5D | 5E | ACTP50O | SCTPS1O | | ACTPS0M | ACTPS1M |
| 6A | 6B | | 6D | 6E | FAIL0-O | FAIL1-O | | FAIL0-M | FAIL1-M |
| 7A | 7B | | 7D | 7E | PS0-SYN | PS1-SYN | | | GND |
| 8A | 8B | | 8D | 8E | RING-SYN | ACTANI-0 | | | ACTANI-1 |
| 9A | 9B | | 9D | 9E | AF1-0 | CUR-0 | | AF1-1 | CUR-1 |
| 10A | 10B | | 10D | 10E | XOVER-0 | RMS-0 | | XOVER-1 | RMS-1 |
| 11A | 11B | | 11D | 11E | AF0-0 | | | AF0-1 | GND |
| 15A | 15B | | 15D | 15E | | +15V-IN | | +12V-OUT | |
| 16A | 16B | | 16D | 16E | CLK-8- | CLKB+ | | CLK9- | CLK9+ |
| 17A | 17B | | 17D | 17E | FP8- | FP8+ | | FP9- | FP9+ |
| 18A | 18B | 18C | 18D | 18E | RD8 | TD8 | GND | RD9 | TD9 |
| 19A | 19B | | 19D | 19E | RCON8 | TON8 | | RCON9 | TCON9 |
| 20A | 20B | | 20D | 20E | ACTLD8 | GND | | ACTLD9 | GND |
| 21A | 21B | | 21D | 21E | CLK7- | CLK7+ | | CK10- | CLK10+ |
| 22A | 22B | | 22D | 22E | FP7- | FP7+ | | FP10- | FP10+ |
| 23A | 23B | 23C | 23D | 23E | RD7 | TD7 | GND | RD10 | TD10 |
| 24A | 24B | | 24D | 24E | RCON7 | TCON7 | | RCON10 | TCON10 |
| 25A | 25B | | 25D | 25E | ACTLD7 | GND | | ACTLD10 | GND |




P3

| | | | | | A | B | C | D | E |
|---|---|---|---|---|---|---|---|---|---|
| 1A | 1B | | 1D | 1E | CLK6- | CLK6+ | | CLK11- | CLK11+ |
| 2A | 2B | | 2D | 2E | FP6- | FP6+ | | FP11- | FP11+ |
| 3A | 3B | 3C | 3D | 3E | RD6 | TD6 | GND | RD11 | TD11 |
| 4A | 4B | | 4D | 4E | RCON6 | TCON6 | | RCON11 | TON11 |
| 5A | 5B | | 5D | 5E | ACTLD6 | GND | | ACTLD11 | GND |
| 6A | 6B | | 6D | 6E | CLK5- | CLK5+ | | CLK12- | CLK12+ |
| 7A | 7B | | 7D | 7E | FP5- | FP5+ | | FP12- | FP12+ |
| 8A | 8B | 8C | 8D | 8E | RD5 | TD5 | GND | RD12 | TD12 |
| 9A | 9B | | 9D | 9E | RCON5 | TCON5 | | RCON12 | TCON12 |
| 10A | 10B | | 10D | 10E | ACTLD5 | GND | | ACTLD12 | GND |
| 11A | 11B | | 11D | 11E | CLK4- | CLK4+ | | CLK13- | CLK13+ |
| 15A | 15B | | 15D | 15E | FP4- | FP4+ | | FP13- | FP13+ |
| 16A | 16B | 16C | 16D | 16E | RD4 | TD4 | GND | RD13 | TD13 |
| 17A | 17B | | 17D | 17E | RCON4 | TCON4 | | RCON13 | TCON13 |
| 18A | 18B | | 18D | 18E | ACTLD4 | GND | | ACTLD13 | GND |
| 19A | 19B | | 19D | 19E | CLK3- | CLK3+ | | CLK14- | CLK14+ |
| 20A | 20B | | 20D | 20E | FP3- | FP3+ | | FP14- | FP14+ |
| 21A | 21B | 21C | 21D | 21E | RD3 | TD3 | GND | RD14 | TD14 |
| 22A | 22B | | 22D | 22E | RCON3 | TCON3 | | RCON14 | TCON14 |
| 23A | 23B | | 23D | 23E | ACTLD3 | GND | | ACTLD14 | GND |
| 24A | 24B | | 24D | 24E | CLK2- | CLK2+ | | CLK15- | CLK15+ |
| 25A | 25B | | 25D | 25E | FP2- | FP2+ | | FP15- | FP15+ |

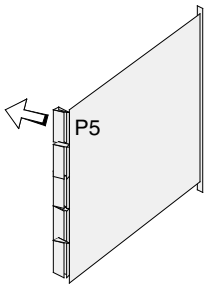
# **NTTR77AA** (continued)

### NTTR77AA pin numbers (continued)

P5

| | | | | |
|---|---|---|---|---|
| 1A | 1B | 1C | 1D | 1E |
| 2A | 2B | | 2D | 2E |
| 3A | 3B | | 3D | 3E |
| 4A | 4B | | 4D | 4E |
| 5A | 5B | | 5D | 5E |
| 6A | 6B | 6C | 6D | 6E |
| 7A | 7B | | 7D | 7E |
| 8A | 8B | | 8D | 8E |
| 9A | 9B | | 9D | 9E |
| 10A | 10B | | 10D | 10E |
| 11A | 11B | 11C | 11D | 11E |
| 15A | 15B | | 15D | 15E |
| 16A | 16B | | 16D | 16E |
| 17A | 17B | | 17D | 17E |
| 18A | 18B | | 18D | 18E |
| 19A | 19B | | 19D | 19E |
| 20A | 20B | | 20D | 20E |
| 21A | 21B | 21C | 21D | 21E |
| 22A | 22B | | 22D | 22E |
| 23A | 23B | | 23D | 23E |
| | | 24C | | |
| | | 25C | | |

| **A** | **B** | **C** | **D** | **E** |
|---|---|---|---|---|
| RD2 | TD2 | GND | RD15 | TD15 |
| RCON2 | TCON2 | | RCON15 | TCON15 |
| ACTLD2 | GND | | ACTLD15 | GND |
| CLK1- | CLK1+ | | CLK16- | CLK16+ |
| FP1- | FP1+ | | FP16- | FP16+ |
| RD1 | TD1 | GND | RD16 | TD16 |
| RCON1 | TCON1 | | RCON16 | TCON16 |
| ACTLD1 | GND | | ACTLD16 | GND |
| CLK0- | CLK0+ | | CLK17 | CLK17+ |
| FP0- | FP0+ | | FP17- | FP17+ |
| RD0 | TD0 | GND | RD17 | TD17 |
| RCON0 | TCON0 | | RCON17 | TCON17 |
| ACTLD0 | GND | | ACTLD17 | GND |
| SW4 | SW5 | | | |
| SW0 | SW1 | | SW2 | SW3 |
| LOCKIN | LOCKOUT | | CLKSELI | CLKSELO |
| MINORSET | MAJSET | | CATSET | UNIT0 |
| MAJSCAN | CATSCAN | BRTN | SPRO1 | SPRO2 |
| TMS | FUSALMS | | PWRI0 | PWRI1 |
| TRSTZ | TCK | | RCPSPRI0 | RCPSPRO0 |
| TDO | TDI | GND | RDPSPRI1 | RCPSPRO1 |
| GND | BTYPE0 | GND | BTYPE1 | GND |



## Technical data

The following paragraph identifies the power requirements for the NTTR77AA.

### Power requirements

The following table lists the power requirements for the NTTR77AA.

**Power requirements**

| Supply voltage | Minimum | Nominal | Maximum | Supply current | Supply ripple (peak–to–peak) |
|---|---|---|---|---|---|
| +5 V | +4.75 V | +5 V | +5.25 V | 3 A | 100 mV |
| +15 V | +14.5 V | +15 V | +15 .5 V | 0.3 A | 100 mV |
| +12 V | +11.5 V | +12 V | +12.5 V | 0.1 A | 100 mV |

# NTTR80AA

## Product description

The NTTR80AA frame is the Star Remote Hub Equipment (SRME) frame. The SRME frame is a seven-foot frame that contains a single control shelf and three line drawer shelves. Each shelf contains up to six line drawers for a total of 18 line drawers in the frame. The frame supports up to 1152 line cards.

The SRME frame supports the following line types connected to the line drawers:

- integrated services digital network (ISDN)
- coin
- Meridian business set (MBS)
- plain ordinary telephone service (POTS)

## Parts

The NTTR80AA contains the following parts:

- NTTR5010—lower line drawer shelf
- NTTR5020—upper line drawer shelf
- NTTR5030—air baffle with fuse holders
- NTTR8603—control shelf enclosure that includes the backplane and frame supervisory panel (FSP)

### Upper and lower line drawer shelves

The upper and lower line drawer shelves contain up to six line drawers each. The SRME frame contains up to 18 line drawers for a total of up to 1152 lines.

### Air baffle with fuse holders

The air baffle is above the control shelf. The air baffle enables cooling of the FSP and the line drawers. Spare fuses are in the fuse holders above the FSP access cover.

### Control shelf

The control shelf contains the following circuit cards:

- central side (C-side) and peripheral side (P-side) communication cards, which are the quad pulse-coded modulation (PCM) carrier cards (NTTR87AA). Each NTTR87AA card contains up to four dual DS-1 interface packlets (NTMX81AA).
- remote controller pack (NTTR77AA)
- universal maintenance pack (NTTR73AA)

- ringing generator card (NTTR60AA)
- power converter (NT6X53AA)

The control shelf also contains the frame supervisory panel (FSP). The following paragraph describes the FSP.

### Frame supervisory panel

The FSP is in the top area of the control shelf and provides power and alarming requirements for the

- distribution of -48 V to the power converters
- alarm monitoring and control
- maintenance features (jacks for telephone, data, and alarm battery supply)

The FSP contains the following components:

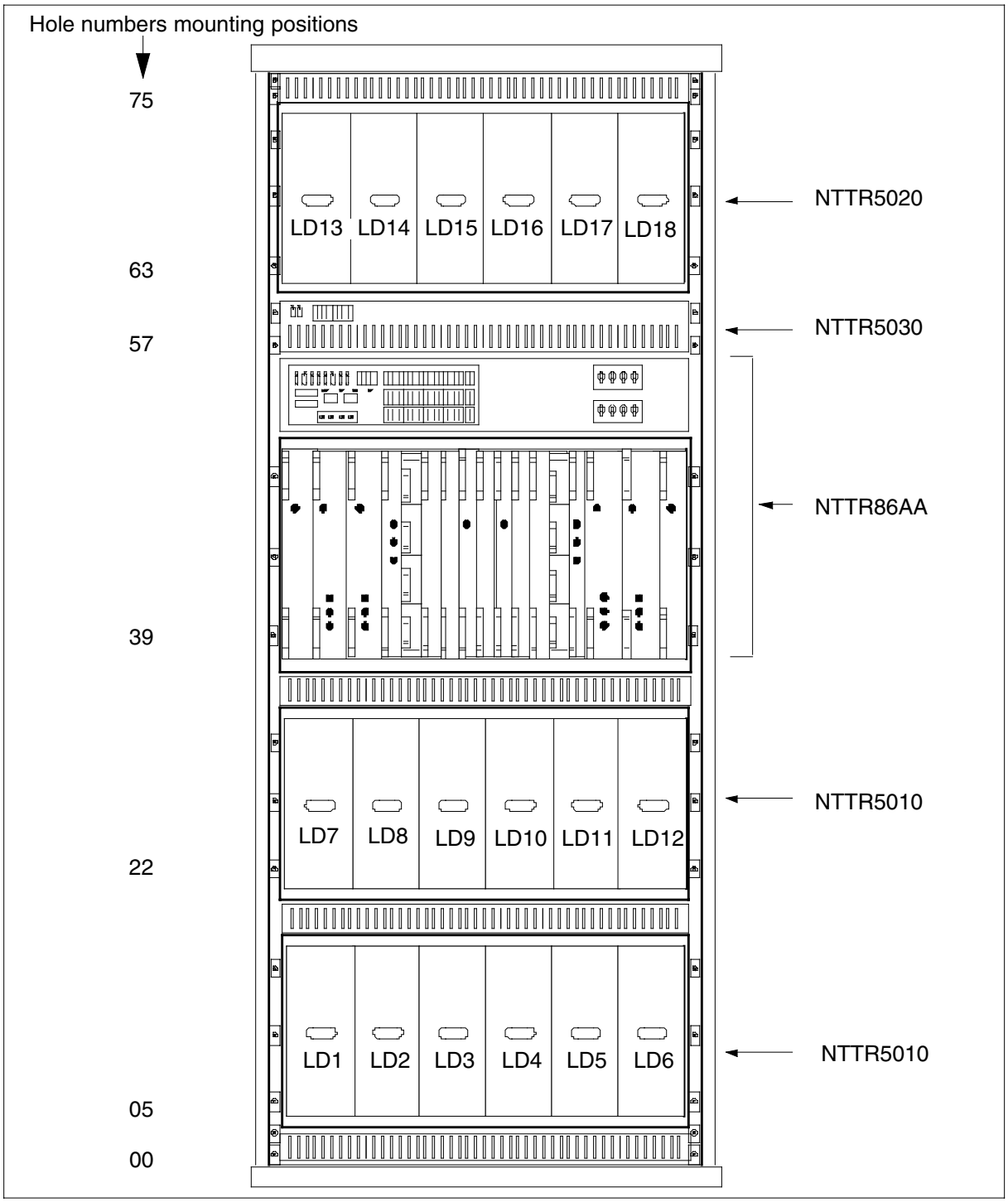
- NTTR74AA alarm card
- NTTR75AA maintenance and fuses card
- NTTR76AA talk battery and circuit breaker card

## Design

The following figure shows the design of the NTTR80AA.

# **NTTR80AA** (end)

### NTTR80AA parts



# NTTR87AA

## Product description

The Quad Pulse–code modulation (PCM) Carrier pack is a 3.048 m x 3.81 m (10 inch x 12.5 inch) frame that fits in dedicated slots in the Star Hub control shelf. The NTTR87AA accepts four smaller packlets. These packlets plug into the NTTR87AA from the front of the card.

The NTTR87AA has a metal frame and five connectors where a printed circuit board (PCB) connects. The PCB contains ac terminal resistors. The PCB does not contain active components.

### Location

The NTTR87AA is in slots 8, 9, 10, 14, 15, and 16 on the control shelf of the Star Hub.

- Slots 8 and 16 connect to the host peripheral module (PM) and support a maximum of 16 DS–1 central side (C–side) ports.
- Slots 9, 10, 14, and 15 support DS–1 links on the peripheral side (P–side) for up to 16 Star Modules.

## Functional description

The NTTR87AA accepts a maximum of four packlets. These packlets are dual DS–1 interface packlets. The NTTR87AA also accepts blank packlets instead of dual DS–1 interface packlets when the system configuration requires no DS–1 packlets. The NTTR87AA allows addition, removal, and maintenance to dual DS–1 interface packlets.

## Signaling

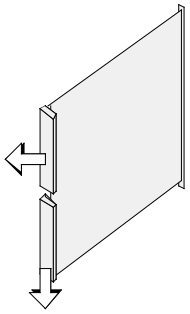
The following paragraph identifies the signaling between the NTTR87AA and the Star Hub backplane.

### Pin numbers

The following figure identifies the pin numbers for NTTR87AA.

# **NTTR87AA** (continued)

### NTTR87AA pin numbers



| | A | B |
|---|---|---|
| 1A 1B | GND | GND |
| 2A 2B | +5V | +5V |
| 3A 3B | +5V | +5V |
| 4A 4B | +5V | +5V |
| 5A 5B | +5V | +5V |
| 6A 6B | C97 | C97 |
| 7A 7B | C324 | C324 |
| 8A 8B | -FP48 | -FP48 |
| 9A 9B | GND | GND |
| 10A 10B | DOUTC0 | DOUTC0 |
| 11A 11B | DOUTC1 | DOUTC1 |
| 12A 12B | DINC0 | CINC0 |
| 13A 13B | DINC1 | DINC1 |
| 14A 14B | -ACTV | -MSGEN |
| 15A 15B | MSGIN | MSGOUT |
| 16A 16B | -RXFP0 | -RXFP0M |
| 17A 17B | GND | GND |
| 18A 18B | SPRQPC0 | SPRQPC1 |
| 19A 19B | | |
| 20A 20B | | |
| 21A 21B | | |
| 22A 22B | | |
| 23A 23B | SENDT0 | SENDR0 |
| 24A 24B | | |
| 25A 25B | SENDT1 | SENDR1 |
| 26A 26B | | GND |
| 27A 27B | SENDT2 | SENDR2 |
| 28A 28B | GND | GND |
| 29A 29B | SENDT3 | SENDR3 |
| 30A 30B | GND GND | |
| 31A 31B | RECT1 | RECR0 |
| 32A 32B | | GND |
| 33A 33B | RECT1 | RECR1 |
| 34A 34B | GND | GND |
| 35A 35B | RECT2 | RECR2 |
| 36A 36B | | GND |
| 37A 37B | RECT3 | RECR3 |
| 38A 38B | GND | GND |
| 39A 39B | -BITS0 | -BITS0M |
| 40A 40B | +12V | +12V |

| | A | B |
|---|---|---|
| 41A 41B | | |
| 42A 42B | | |
| 43A 43B | | |
| 44A 44B | GND | GND |
| 45A 45B | | |
| 46A 46B | C97 | C97 |
| 47A 47B | C324 | C324 |
| 48A 48B | -FP48 | -FP48 |
| 49A 49B | GND | GND |
| 50A 50B | DOUTC2 | DOUTC2 |
| 51A 51B | DOUTC3 | DOUTC3 |
| 52A 52B | DINC2 | DINC2 |
| 53A 53B | DINC3 | DINC3 |
| 54A 54B | -ACTV | -MSGEN |
| 55A 55B | MSGIN | MSGOUT |
| 56A 56B | -RXFP1 | -RXFP1M |
| 57A 57B | GND | GND |
| 58A 58B | | |
| 59A 59B | SENDT4 | SENDR4 |
| 60A 60B | | GND |
| 61A 61B | SENDT5 | SENDR5 |
| 62A 62B | | GND |
| 63A 63B | SENDT6 | SENDR6 |
| 64A 64B | GND | GND |
| 65A 65B | SENDT7 | SENDR7 |
| 66A 66B | GND | GND |
| 67A 67B | RECT4 | RECR4 |
| 68A 68B | | GND |
| 69A 69B | RECT5 | RECR5 |
| 70A 70B | GND | GND |
| 71A 71B | RECT6 | RECR6 |
| 72A 72B | | GND |
| 73A 73B | RECT7 | RECR7 |
| 74A 74B | GND | GND |
| 75A 75B | | |
| 76A 76B | -BITS1 | -BITS1M |
| 77A 77B | | |
| 78A 78B | GND | GND |
| 79A 79B | | |
| 80A 80B | GND | GND |

## Technical data

The following paragraph identifies the power requirements for the NTTR87AA.

### Power requirements

The NTTR87AA pack does not have any current requirements. The pack transfers the –5V and –12V from the backplane to the NTMX81 packlets.

DMS-100 Family

# Hardware Description Manual

Volume 5 of 5

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